A Simple CMOS Self-Aligned Double-Gate Poly-Si TFT Technology

Zhibin Xiong, Haitao Liu, Chunxiang Zhu[+]
Johnny K. O. Sin*
Dept. of EEE, HKUST, Clear Water Bay, Hong Kong
*Tel: (852) 2358-7052; Email: eesin@ust.hk
[+]Dept. of ECE, NUS, Singapore

Poly-Si TFT technology is the most promising candidate for the ultimate goal of building fully-integrated flat panel display system on glass (SOG) [1]. It has been experimental demonstrated that double-gate structure is capable to provide a significant improvement in current drive, better saturation characteristics and a steeper subthreshold slope [2]. Thus, it is very attractive for both analog and digital applications. However, this structure is not a self-aligned structure. It results in significant performance variation and poor scalability. A few self-aligned double-gate TFTs have been demonstrated [3, 4], but all of them are complicated and require the use of critical process such as chemo-mechanically polishing (CMP). In this paper, a simple CMOS self-aligned double-gate (SADG) poly-Si TFT technology is reported. Experimental results show that this technology provides excellent saturation characteristics, high current drive, and low leakage current.

The self-aligned double-gate TFT devices were fabricated using a low temperature process (≤ 600 °C). Fig. 1 shows the schematic cross-sections of the major fabrication steps. Glass wafers with 3000Å low temperature oxide (LTO) were used as starting substrates. First, a 2000Å poly-Si film was deposited, implanted with phosphorus, and patterned using wet etch. Following this, a 1000Å LTO was deposited as gate oxide, and a 300Å a-Si was then deposited as the channel layer (Fig. 1(a)). After that a thick layer of LTO was deposited and coated with positive photo-resist. Back-light exposure was used to define the protected region, and the exposed LTO was removed (Fig. 1 (b)). This technique was used before to obtain self-aligned single gate ultra-thin channel TFT devices [5]. After that, a photolithography step was used to define the active area, and wet etch was used to remove the rest of the LTO and the ultra-thin a-Si layer. Following this, a 3000Å thick layer of a-Si was deposited as thick source/drain regions. After that, source/drain regions of the N- and P-channel devices were implanted with phosphorous and boron, respectively. A photolithography step was followed to define the active area. Then, the thick a-Si film was left behind (Fig. 1 (c)). Then the isolation LTO was removed, and a 1000Å LTO was deposited as top gate oxide. And a 3000Å a-Si film was deposited, implanted with phosphorus, and patterned as top gate (Fig. 1 (d)). After that a layer of 3500Å of LTO was deposited, and contact holes to the gate, source, and drain were defined. Metal Induced Lateral Crystallization (MILC) was used to recrystallize the a-Si film. The glass wafers were then sintered at 400 ^{o}C for 30 mins after metallization and patterning. For comparison, conventional self-aligned single-gate (SG) TFTs were also fabricated in the same run.

The measured I_d-V_d of the SADG TFT shows that the kink effect is suppressed significantly even at high drain bias (e.g. at V_{ds}=20 V), and good saturation characteristics are obtained. The good current saturation characteristics are attributed to a combination of the effective reduction in the drain field and the fully-depletion of the ultra-thin channel [5]. Fig. 2 shows the gate transfer characteristics of the SADG TFT and the conventional single gate TFT. The SADG TFT has much higher on-state current than that of the single gate TFT. For n-channel devices, the SADG TFT has 4.2 times higher on-current at high gate biases (V_{gs}=20 V). For p-channel devices, the SADG TFT has 3.6 times higher on-current at high gate biases (V_{gs}=-20 V). The higher than two times of on-current is due to the enhancement in mobility.

In summary, a novel self-aligned double-gate Poly-Si TFT was fabricated. The experimental results show that excellent current saturation characteristics, high current drive, and low off-current are obtained. The SADG TFT is very promising for fully-integrated flat panel display system on glass applications.

REFERENCES

[1]. M. Stewart, R. Howell, L. Pires, M. Hatalis, W. Howard, and O. Prache, Proc. of IEDM, pp. 871-874, 1998.
[2]. A. Kumar K. P., J. K. O. Sin, C. T. Nguyen, and P. K. Ko, IEEE Trans. Electron Devices, vol. 45, no. 12, pp. 2514-2520, 1998.
[3]. S. D. Zhang, R. Han, J. K. O. Sin, and M. Chan, IEEE Trans. Electron Devices, vol. 49, no. 5, pp. 718-724, 2002.
[4]. A. Hara, M. Takei, K. Yoshino, F. Takeuchi, M. Chida, and N. Sasaki, Proc. of IEDM, pp. 211-214, 2003.
[5]. Z. Xiong, H, Liu, C. Zhu, and J. K. O. Sin, Proc. of the 6th Intl. Symposium on Thin Film Transistor Technologies, pp. 42-46, 2002.

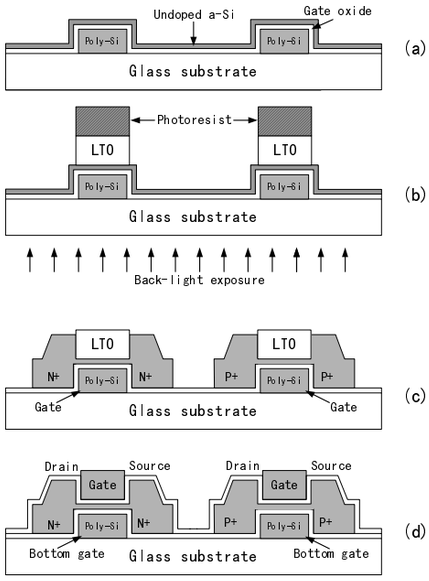

Fig. 1 Major fabrication steps of the SADG poly-Si TFT technology with complementary devices.

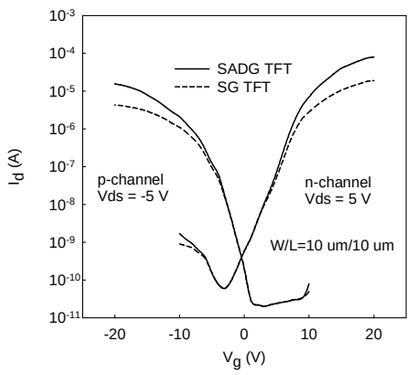

Fig. 2 Comparison of the I_d-V_g characteristics of the SADG TFT and conventional SG TFT.