Influence of Channel Position on Characteristics of p-Channel c-Si TFT Inside a Location-Controlled Grain

V. Rana, R. Ishihara, Y.v.Andel, *Y. Hiroshima, *D. Abe, *S. Inoue, *T. Shimoda, J.W.Metselaar and C. I. M. Beenakker

Delft Institute of Microelectronics and Submicrontechnology (DIMES),
Delft Univ. of Technol., Delft, The Netherlands

*Technology Platform Research Center, Seiko-Epson Corp., Nagano, Japan

Precise location-controlled grain allows us to eliminate the grain boundaries from active area of thin-film transistor. The μ-Czochralski (grain-filter) process [1] provides a precise way to control position of grain in excimer-laser crystallization. The n-channel c-Si TFTs fabricated inside a location-controlled grain by μ-Czochralski (grain-filter) process showed a field-effect electron mobility (μ_{FEe}) and subthreshold slope of ~ 600 cm^2/Vs, 0.20 V/dec. respectively by positioning the current flow direction parallel to the direction of radial defects [2]. For application to CMOS circuitries, p-channel c-Si TFTs should have a high performance too. The objective of this study is to investigate the effect of the position of p-channel c-Si TFTs inside a grain on the TFT characteristics.

The TFTs used in this experiment were fabricated with μ-Czochralski process. The schematic diagram of c-Si TFT is shown in Fig. 1. 100 or 250 nm thick a-Si was deposited by LPCVD on the thermally oxidized having the grid of grain-filter. The samples were crystallized with XeCl excimer-laser. The channel of the transistor is designed such that channel position with respect to grain-filter, changes in different directions. 80 nm thick ECR-PECVD SiO_2 was deposited as a gate insulator. The source and drain were doped of boron by ion shower using Al gate pattern as a mask. Afterwards, the N_2 annealing was carried out for one hour. The channel length and width, measured by SEM was 2.03 and 1.87 μm respectively.

Figure 3 shows the transfer characteristics of the p-channel c-Si TFTs having 250 nm silicon thickness and 80 nm thick ECR-PECVD SiO_2 as a gate insulator fabricated with various channel positions. The energy density of the excimer-laser pulse was 1.025 J/cm^2. By shifting the channel position from the top of the grain-filter (C), there is no change in subthreshold characteristics with a S value of 0.16V/dec.. This suggests the fact that the defects near the bottom of the grain-filter do not affect the subthreshold characteristics, as opposed to the n-channel counterparts. There is however improvement in the ON current by positioning TFTs at X, which does not posses the grain filter and has current flow direction parallel to the radial defects. Table 1 shows μ_{FEh}, S value, off-current (I_{OFF}) and threshold voltage (V_{TH}) for c-Si TFTs. It is evident from table 1 that c-Si TFTs at the X position give the highest μ_{FEh} (250 cm^2/Vs), since the carrier of motion is not impeded by the defects generated radially from the grain-filter.

In summary, dependence of channel position inside a location-controlled grain on the p-channel c-Si TFT characteristics was investigated. By avoiding the grain-filter from the channel region, the μ_{FEh} improves while there is no change in the subthreshold characteristics. The c-Si TFT, shifted in the current flow direction with respect to the center of the grain filter gave a high mobility of 250 cm^2/Vs and subthreshold slope of 0.16V/dec. successfully.

References:

[1] P. C. Van der Wilt, B.D. van Dijk, G.J. Bertens, R. Ishihara, and C.I.M. Beenakker, Appl. Phy.Lett., vol. 72 No.12, p.1819, 2001

[2] V.Rana, R.Ishihara, Y. Hiroshima, D. Abe, S. Inoue, T. Shimoda, J.W.Metselaar and C. I. M Beenakker, in AMLCD'03 , pg. 17

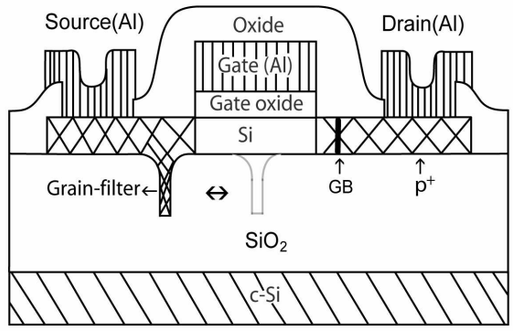

Fig.1 Cross-section of p-channel TFTs with different positions

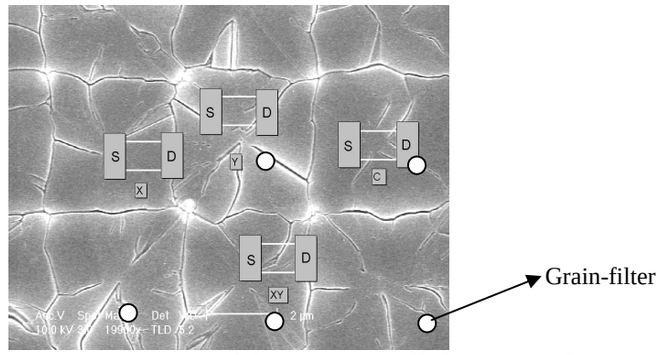

Fig.2 SEM image of location-controlled grain with different positions

Table 1. Characteristic values of p-channel c-Si TFTs for various positions with respect to grain-filter

Channel Position	Mobility (cm^2/Vs)	S (V/dec).	Off-Current (A)*1E-14	V_{th}(V)
X	250 ± 21 (11%)	0.16± 0.04 (23%)	7.6 ± 2.8 (36%)	-2.7± 0.7 (25%)
Y	150 ± 12 (8%)	0.14 ± 0.01 (7%)	5.6± 1.3 (22%)	-2.9± 0.3 (15%)
XY	198± 21 (8%)	0.16± 0.034 (20%)	1.4± 5.7 (43%)	-2.9± 0.5 (16%)
C	181±11 (6%)	0.15± 0.04 (26%)	3.5±1.3 (37%)	-2.9±0.4 (15%)

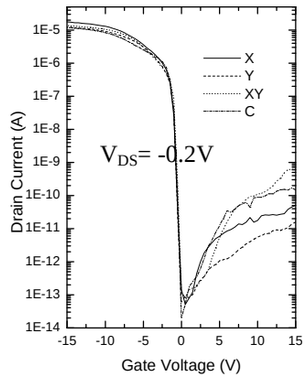

Figure 3. I_D –V_G characteristics of p-channel c-Si TFTs for various positions with respect to grain filter for 250nm silicon thickness