Improvement of Hysteresis Characteristics in p-channel Poly-Si TFTs

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Introduction: Active matrix organic light emitting diode (AMOLED) display has a better image quality in terms of viewing angle, contrast ratio, and response time than liquid crystal displays (LCDs). Recently, many companies have been trying to penetrate the small-sized applications market with mobile phones, personal digital assistances and digital still cameras. However, it still has some critical issues such as the reliability of OLED materials, recoverable or irrecoverable residual images, and image non-uniformity.[1][2] Among them, the recoverable residual image is mainly related to the hysteresis characteristics of TFT.[3] In this work, they are observed in p-channel Poly-Si TFT and surface treatment conditions before gate oxide deposition are considered to improve them. Also, the amplitude of the hysteresis level is compared according to process conditions.

Experimental: The structure of p-channel TFT is shown in Figure 1. It has a top coplanar structure. The fabrication process is as follows until gate oxide is deposited. A SiO_2 buffer of 3000Å thickness and an a-Si:H film of 500Å thickness are deposited on a glass substrate by plasma-enhanced chemical vapor deposition (PECVD). The a-Si:H film is crystallized by excimer laser annealing after dehydrogenation. Following the active layer patterning, a gate oxide layer of 1,500Å thickness is deposited by PECVD. We consider three kinds of surface treatment conditions before gate oxide deposition. First, 0.25% HF solution is applied for 30s. Second, the surface of the active layer is cleaned by de-ionized water and is exposed to ultraviolet light with a wavelength of 172 nm, power density of 6.5 mW/cm^2 and exposure time of 35s. Third, H_2 plasma treatment with 130 Pas. of pressure, 200 Watts of power and the discharge time of 30s in PECVD is processed.

Results and discussion: Figure 2 shows the Ids-Vgs characteristics of p-channel TFT measured by changing the sweep direction of Vgs. When the Vgs sweeps from –15V to 10V, the threshold voltage is larger than that measured under the opposite sweep condition. The hysteresis level of a TFT can be defined on the basis of the difference of the threshold voltage measured with changing the sweep direction. In the case of Figure 2, the hysteresis level is 0.6V. Figure 3 shows the hysteresis level with surface treatment condition. The sample treated with 0.25% HF solution has a hysteresis level of 0.4V. On the other hand, the samples with ultraviolet exposure and H_2 plasma treatment have 0.25V and 0.23V, respectively. The difference in threshold voltage according to the sweep direction can be explained by hole trapping in the oxide trap states and interface trap states between the poly-Si layer and gate insulator.[4][5] Holes can be trapped and de-trapped repeatedly depending on the applied voltage. As hole trapping occurs at the bias condition for a high drain current, the threshold voltage increases and the channel current decreases depending on the quantity of the trapped charge. If the bias condition is changed to that for a low drain current, the trapped charge is de-trapped and the drain current increases.

Conclusion: The surface treatment using HF solution, ultraviolet light, or H_2 plasma before gate oxide deposition reduces interface trap states between the poly-Si layer and gate insulator. We can minimize the hysteresis level of p-channel TFT from 0.66V to 0.23V through the surface treatment.

References

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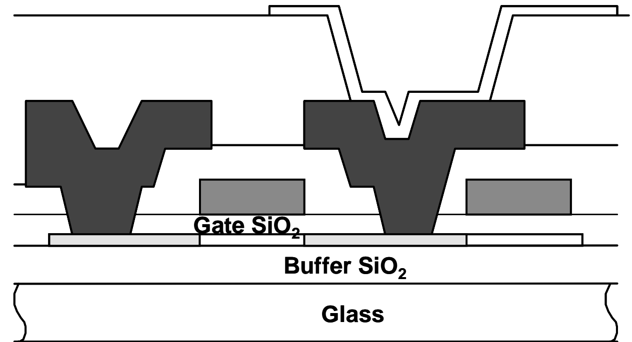

Fig. 1 Cross-sectional view of p-channel TFT

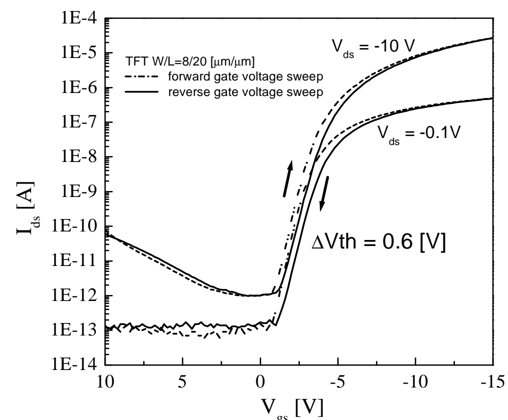

Fig. 2 Ids-Vgs characteristics of p-channel TFT

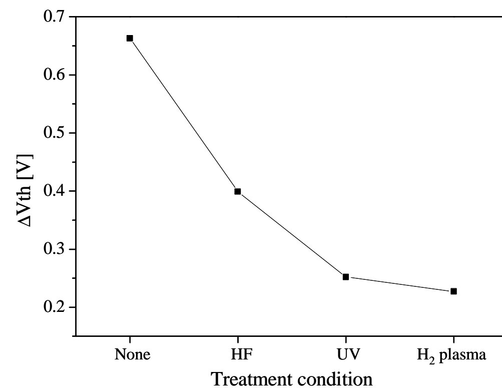

Fig. 3 Hysteresis level with surface treatment condition