**Thin-Film Transistors Based on Spin-Coated Chalcogenide Semiconductor Channels**

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Low-cost solution-based fabrication of thin-film field-effect transistors (TFTs) has become a key goal among the materials science community, primarily as a result of applications potentially enabled by the new technologies (e.g., flexible displays, electronic newspapers, smart cards / fabric). Paramount to this search is the need to identify thin-film deposition processes that simultaneously offer high-throughput deposition (e.g., spin coating, printing, stamping), as well as continuous and uniform films. As circuit device components are scaled to smaller dimensions and reduced operational parameters, control of film thickness to ultrathin dimensionality also represents an important aspect to any proposed film-deposition process.

Among the various components of TFTs that must be deposited, the semiconducting channel provides a significant challenge for solution deposition. The challenge arises because of a strong dependence of the device properties on the film quality and the desire to select high-mobilty semiconductors, which are generally covalently-bonded solids and not very soluble. Most work on solution-processed TFTs has focused on organic-based channel layers, with highest demonstrated mobilites in the range of 1 $cm^2$/V-sec (same order of magnitude as amorphous silicon).[1] In this talk, we discuss a new approach for spin-coating ultrathin crystalline inorganic films based on the low-temperature decomposition of highly-soluble hydrazinium precursors of main group metal (e.g., Ge, Sn, In, Sb) chalcogenides.[2] Resulting metal chalcogenide channel layer films are only a few unit cells thick (Fig. 1), with remarkably large mobilities – an order of magnitude better than previous studies involving high-thoughput solution-based deposition.

Using this technique, we were able to demonstrate TFTs based on spin-coated $SnS_{2-x}Se_x$, as well as other semiconducting metal chalcogenides, yielding n-type transport, large current densities ( > $10^5$ A/$cm^2$) and mobilities greater than 10 $cm^2$/V-s (Fig. 2).[2] Initial studies considered films spin coated from hydrazine. Currently, we are working to replace the hydrazine with less toxic solvent systems (we have demonstrated, for example, replacement of over 50% of the hydrazine with water).[3] While the technology is still new, with a number of technical hurdles to be addressed, the convenient processing, high performance and ultrathin nature of the solution-processed films may enable the field of solution-processed semiconductors to be extended to higher-end TFT applications (e.g., intelligent sensor arrays and RFID tags, flexible input/output screens and very large area displays) than currently being envisioned for traditional soluble organic-based semiconductors.

REFERENCES:
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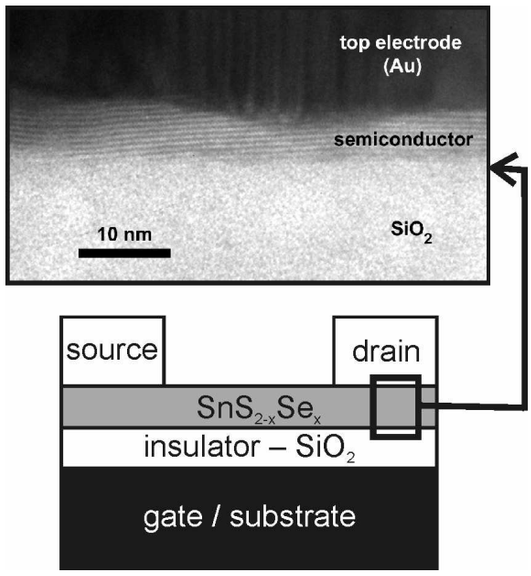


**Fig. 1.** The TFT device consists of a heavily *n*-doped silicon wafer as the substrate / gate, a thermally grown $SiO_2$ gate dielectric, a spin-coated chalcogenide channel layer, and patterned Au source and drain electrodes. The magnified region shows a transmission electron microscope (TEM) cross-sectional image of a device based on a spin-coated $SnS_{1.4(1)}Se_{0.5(1)}$ film.[2]

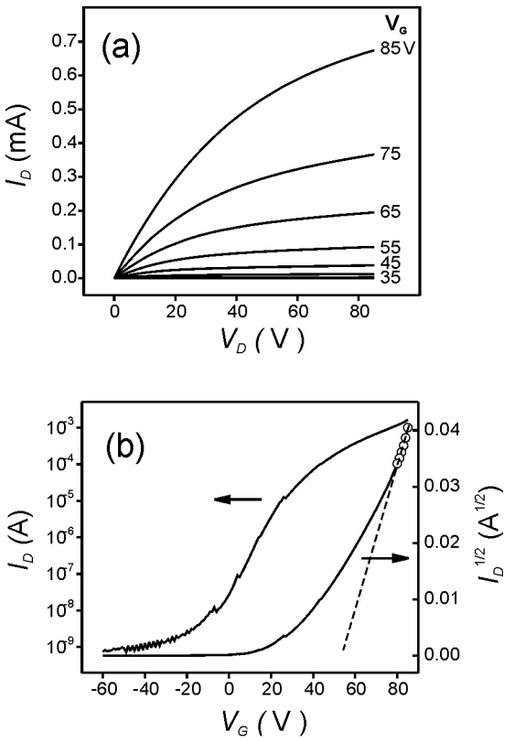


**Fig. 2.** TFT device characteristics for spin-coated $SnS_{1.4}Se_{0.5}$ chalcogenide channel layer.[2] The gate dielectric consists of 2100 Å of thermally grown $SiO_2$ and channel length and width are L = 14 μm and W = 250 μm, respectively: (a) Drain current, $I_D$, versus drain voltage, $V_D$, as a function of gate voltage, $V_G$. (b) Plots of $I_D$ and $I_D^{1/2}$ versus $V_G$ at constant $V_D$ = 85 V, used to calculate current modulation, $I_{on}/I_{off}$, and saturation regime mobility, $\mu_{sat}$, for the same device.