Bottom Contact Organic Thin-Film Transistors with Thiol-based SAM Treatment

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We demonstrate the importance of the optimization of dipping conditions in depositing thiol-based self-assembled monolayer (SAM) on the source/drain electrodes to improve the characteristics of bottom-contact organic thin-film transistors (TFTs) [1]. Fig.1 shows the schematic cross section of the pentacene TFTs used in this work, using heavily doped silicon as the gate electrode with thermally grown silicon dioxide of 300nm as the gate dielectric layer. Au/Cr source/drain electrodes of 50nm/1nm thickness were formed by photolithography with lift-off method. Octadecanethiol (ODT) SAMs were formed by dipping the electrode surface in 0.1mM octane solution of ODT for periods from 1 minute to 4 days. Finally, 50nm thick pentacene film was deposited by thermal evaporation at a pressure of 2×10^{-6} Torr without heating the substrate. Fig.2 shows the transfer characteristics of the pentacene TFTs. With ODT treatment for 1 minute, the field effect mobility increased by 25% and the off current decreased about one order of magnitude, compared with that without the treatment. However, the elongated treatment for 20 min decreased the mobility, accompanied by the threshold voltage shift. In case of long-time treatment for 4 days, the on current decreased less than 10⁻⁸ A and the switching characteristic was missing.

From the sum-frequency vibrational spectroscopy (SFVS) measurement, we found that in the case of short dipping time, the thiol SAMs were in low-density and lying-down phase. Further, we estimated that the thickness of SAMs in this phase may be suitable for forming a good contact at the interface between the electrodes and semiconductor on the basis of the consideration of the energy barrier height, schematically depicted in **Fig.3**[2] [3][4].

This work is partially supported by the "Advanced Organic Device Project" under a contract between OITDA and the New Energy and Industrial Technology Development Organization (NEDO). The authors thanks Drs. T.Kamata and M.Yoshida of National Institute of Advanced Industrial Science and Technology (AIST) for valuable discussions.

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Fig.1 Schematic TFT cross section.



Fig.2 Transfer characteristics. The channel length L is 2000 μ m and the channel width W is 400 μ m (Vds=-20V). The field effect mobility of TFT with ODT treatment for 1 min is 0.24cm²/Vs.



Fig.3 Model of energy barrier at the interface between the electrode and semiconductor.