The effect of gate dielectric surface treatment on the device performanceof a pentacene thin film transistor

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Organic thin film transistor (TFTs) has a potential to realize flexible, lightweight devices on plastic substrates. To realize actual devices, the control of the device performance, the device stability, and the device fluctuation is a key issue. The gate dielectric/channel interface will have strong influence on that point, because the source-drain current in a TFT flows near the interface. To control and improve the interface, surface treatment of the gate dielectric is believe to be effective, however, the surface treatment would cause two effects: morphological change of the channel and the change of the electronic state at the interface. We believe the separation of these two effects is significant. In this presentation, we successfully suppress the morphological change and directly extract the change of the electronic state due to the surface treatment in pentacene TFTs.

We fabricate two types of top-contact pentacene TFTs at room temperature. One is fabricated on a thermally grown SiO_2/Si substrate, and the other is fabricated on a SiO_2/Si substrate whose surface is treated with 1,1,1,3,3,3-hexamethyldisilazane (HMDS). Other the HMDS treatment, the two types of TFTs are fabricated simultaneously.

Figure 1(a) shows the surface morphology of the pentacene channel of the untreated TFT, and Fig. 1(b) is the one of the HMDS treated TFT. In these figures, the average grain size and the shape of individual grains are appearently the same, indicating that HMDS-treatment does not induce any clear morphological change of the pentacene channel.

The electrical properties are significantly different between the untreated TFT and the HMDS-treated one. Figure 2 shows transfer characteristics of the TFTs with the same device dimensions. In the HMDS-treated TFT, ON current and the field-effect mobility increase, and the OFF current and the subthreshold slope are suppressed, resulting in the overall performance enhancement.

The experimental results have well reproducibility, suggesting that the observed performance improvement is mainly due to the change of the electronic states at the gate dielectric/pentacene channel interface. The observed improvement is explained by the change of the number of interfacial trapping state, indicating that the surface treatment is effective to reduce the trapping state.

In our presentation, we would like to show more details of sample fabrication and device characteristics.

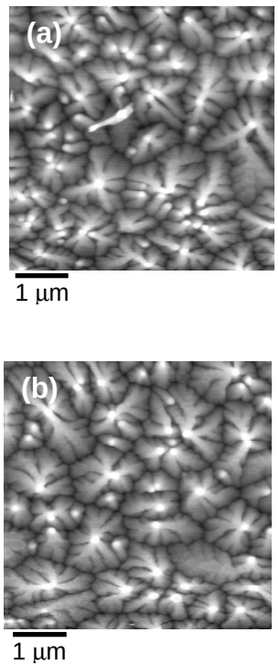

Fig. 1. AFM images of pentacene channels of the untreated TFT (a) and the HMDS-treated one (b). The channels are formed by thermal evaporation at the substrate temperature of 23 °C with the flux rate of 0.2 Å/s.

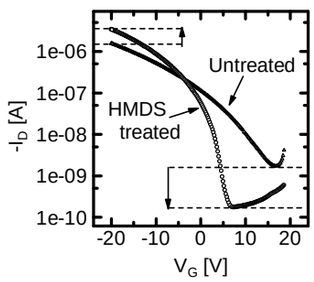

Fig. 2. Transfer characteristics of pentacene TFTs. The triangles are for untreated TFT, and the circles for the HMDS-treated one. The channel width is 1 mm, and the channel length is 200 μm for each TFT.