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High Performance P-Channel Schottky Barrier Thin-Film Transistors with PtSi Source/Drain

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Previously we have proposed and demonstrated a novel Schottky barrier (SB) poly-Si TFT with field-induced-drain (FID) extension [1]-[5]. $CoSi_2$ source/drain (S/D) was employed in previous device fabrication. The $CoSi_2$ S/D device is capable of ambipolar operation as the $CoSi_2$ material possesses a near-mid-gap work function. However, the $CoSi_2$ S/D device also suffers from low current drive because of the large barrier height. To improve the device characteristics, low barrier silicide materials, such as PtSi for p-channel [6] and $ErSi_2$ for n-channel [7], is needed. In this work, we fabricated and characterized devices featuring PtSi S/D. Compared to $CoSi_2$ S/D counterparts, significant improvement in p-channel performance is achieved.

Figure 1 shows the cross-sectional view of a fabricated SB device with FID structure. Detailed process flow could be found in our previous reports [1][5]. In this study, the 50 nm-thick poly-Si channel layer was prepared by solid-phase crystallization (SPC). Gate oxide (15 nm) and passivation oxide (80 nm) were deposited by PECVD. Either PtSi or $CoSi_2$ (i.e., control) was formed to serve as the metallic source/drain of the SB TFTs by the self-aligned silicidation (SALICIDE) scheme.

Figure 2 shows p-channel subthreshold characteristics of the devices with either $CoSi_2$ or PtSi S/D. It can be seen that the use of PtSi results in significant performance improvements including steeper subthreshold slope, larger on-current, and higher on/off current ratio. The higher on/off current ratio in the PtSi S/D device is a result of a higher on-current and a smaller off-state leakage current. The lower off-state current is ascribed to a larger barrier height for thermionic emission of electrons, which dominates the off-state conduction of p-channel operation [3]. In fact, the performance of n-channel operation for the PtSi S/D device is significantly degraded, as shown in Fig. 3. This is reasonable since the barrier height for electrons in PtSi/Si junction is extremely high (> 0.8 eV).

References

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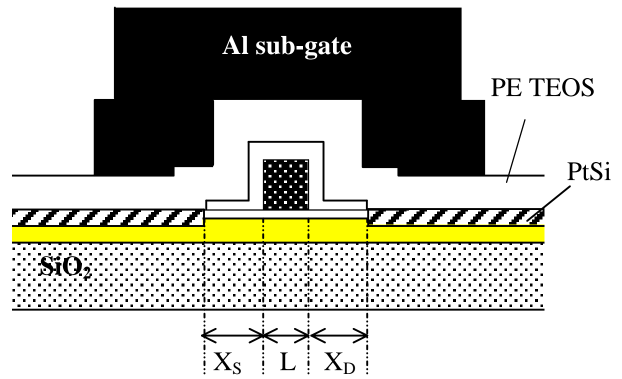

Fig.1 Cross-sectional view of the SB poly-Si TFT.

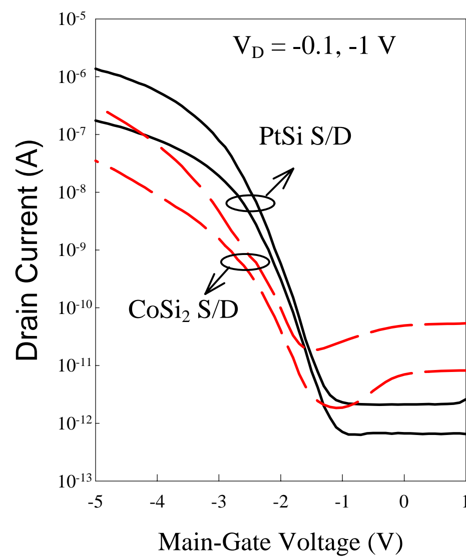

Fig.2 P-channel subthreshold characteristics of SBTFT with $CoSi_2$ and PtSi S/D. (L/W = 0.8/20 μm/ μm, X_S=X_D = 0.2 μm, and sub-gate bias = 4.5 V.)

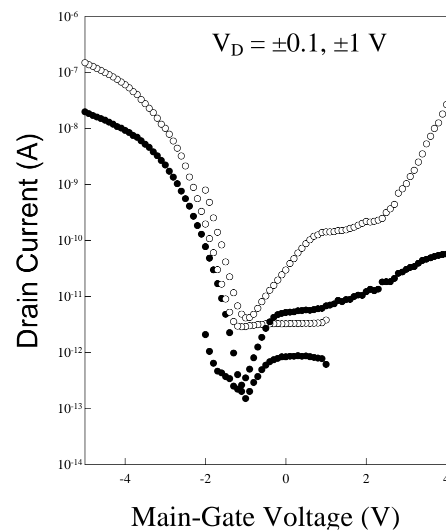

Fig.3 Ambipolar subthreshold characteristics of SBTFT with PtSi S/D. (L/W = 5/20 μm/ μm, X_S= X_D = 1 μm, and sub-gate bias = ± 4.5 V.)