Characterization of Charged States of Si Quantum Dots Floating Gate in MOS Structures

S. Miyazaki, T. Shibaguch and M. Ikeda
Graduate School of Advanced Sciences of Matter,
Hiroshima University
Kagamiyama 1-3-1, Higashi-Hiroshima 739-8530, Japan

Si quantum dots (Si-QDs) embedded in the gate oxide of MOS devices as a floating gate are attracting much attention for its feasibility of multiple-valued memory operations even at room temperatures [1-2]. In this work, we have studied electronic charging and discharging characteristics of Si quantum dots (Si-QDs) floating gate in n-MOS and p-MOS devices and demonstrated discrete charged states of the Si-QDs floating gate.

Hemispherical Si nanocrystals were prepared on 2.8~3.3nm-thick SiO_2, which were thermally-grown at 1000ºC on p-Si(100) with an acceptor concentration of $1x10^{15}cm^{-3}$ and n-Si(100) with a donor concentration of $3x10^{16}cm^{-3}$, by controlling the early stages of LPCVD using SiH_4 at 575ºC. Typically, the areal dot density and the average dot height were $2.5x10^{11}cm^{-2}$ and 8nm, respectively. To form a 7.5nm-thick control oxide, the dot surface was slightly oxidized at 850ºC in 2% O_2 diluted with N_2 to form a 1nm-thick SiO_2 layer and covered uniformly with a 3.3nm-thick amorphous Si layer from the thermal decomposition of 10% Si_2H_6 diluted with He at 440ºC, and subsequently the Si layer was fully oxidized at 1000ºC in dry O_2. Al-gates with a size of 1mm in diameter were formed for MOS capacitors and n+ poly-Si gates for n-MOSFETs with a doubly-stacked Si-QDs floating gate, respectively.

In capacitance-voltage (C-V) measurements of Al-gate MOS capacitors, unique hysteresis characteristics originating from the charging and discharging of the Si-QDs floating gate for MOS capacitors on p-type and n-type Si(100) are clearly observed with a symmetric patter reflecting the Fermi level of the substrate as shown in Fig. 1. This confirms that the undoped Si-QDs floating gate acts as a storage node for both electrons and holes. Namely, the contribution of traps with a specific energy state to the observed C-V hysteresis is ruled out. Taking into account corresponding current-voltage (I-V) characteristics, in each case, the capacitance peak observed around the flat-band condition is attributed to the voltage shift caused by the emission of remaining charges in the Si-QDs floating gate to the Si(100) substrate and thus the C-V curve at negative gate voltages for the MOS capacitor on p-Si(100) or at positive gate voltages for the case on n-Si(100) over the flat-band condition is identical to that predicted for an uncharged gate dielectric.

Under irradiation of ~30klx white light through a fiber-optics equipped with an infrared filter from a 100W halogen lamp, a distinct capacitance peak appears in the inversion region as well and shift toward higher voltage side with increasing sweep rate of the gate voltage as demonstrated in Fig. 2. In the inversion condition for the case on p-Si(100), since electrons photogenerated in the vicinity of the area masked with the Al gate flow into beneath the gate oxide, the observed capacitance peak indicates that the injection of electrons to the electrically-neutral Si-QDs occurs in unison at a certain gate voltage as in the case of electron emission from the charged Si-QDs near the flat-band condition.

In the drain current-gate voltage characteristics of n-MOSFETs with the Si-floating gate, it is also found that three step shifts in the threshold voltage at room temperature.

In conclusion, discrete charged states of the Si-QDs floating gate have been confirmed for both electron and hole injections.

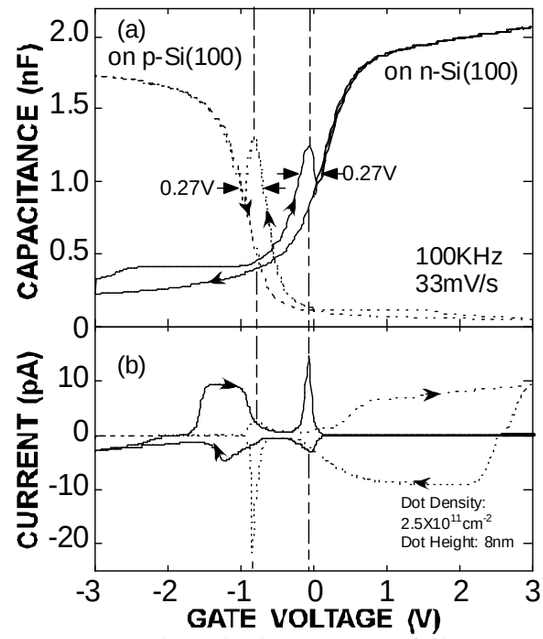

Fig. 1 C-V (a) and I-V (b) characteristics of Al-gate MOS capacitors with the Si-QDs floating gate measured at 100kHz at room temperature. The solid curves and dashed curves denote the results on n-type and p-type Si(100), respectively.

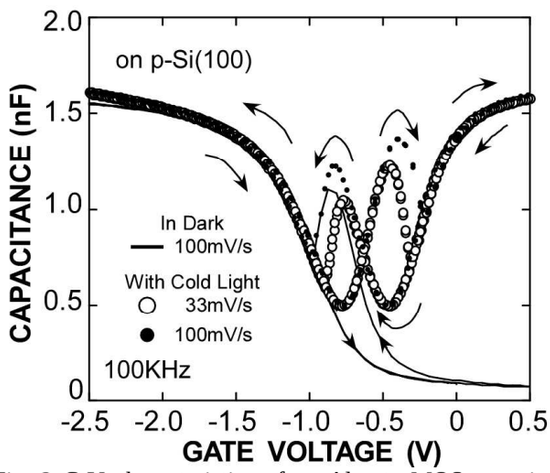

Fig. 2 C-V characteristics of an Al-gate MOS capacitor with the Si-QDs floating gate measured at 100kHz at room temperature under cold light illumination (open and solid circles) and in dark (solid lines). The sweep rate of the gate voltage was set at 100 or 33mV/s.

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