Design and Implementation of Ultra-Small and Ultra-Low-Power Digital Systems Utilizing A Hexagonal BDD Quantum Circuits on GaAs-based Hexagonal Nanowire Network Structures

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Key hardware in future ubiquitous society is intelligent digital systems on an ultra-small chip operating with ultra-low power. For its realization, further advanced LSI technology beyond the scaling limit of Si CMOS technology are required. As a possible approach, a novel hexagonal BDD quantum circuit[1,2] was proposed and has been investigated by the authors. The purpose of this paper is to study design and implementation of ultra-low-power minute digital systems utilizing hexagonal BDD quantum circuits on GaAs-based hexagonal nanowire network controlled by nano-Schottky wrap gates (WPGs).

The hexagonal BDD quantum circuit utilizes binary-decision-diagram architecture where a logic function is represented by a directed graph as shown in **Fig. 1(a)**. It consists of binary path-switch node devices. Arranging the devices for the graph formation results in a hexagonal layout naturally. The logic is evaluated by propagating messengers along the graph. Using a single electron (SE) or a few electrons as the messenger, and controlling them by small energy, power-delay product (PDP) decreases greatly and approach to quantum limit. To manipulate small number of electrons precisely, quantum transport through a quantum wire (QWR) or dot controlled by WPGs is used as shown in **Figs.1(b)** and **(c)**.

Fabricated WPG-based BDD node devices and fundamental logic elements on etched GaAs nanowire hexagons showed correct operations either in quantum regime at low temperature or in classical regime at room temperature. This is because WPG-controlled nanowires can also operate as conventional FETs by adjusting drain and gate voltages, corresponding to trading with PDP value. Then, the present circuits can avoid the problem of temperature for correct operation in quantum circuits.

The hexagonal BDD can implement any combinational circuits in planar without branch crossover. **Fig. 2(a)** shows a fabricated QWR-type 8-bit adder, where 84 devices are integrated using 25M devices/cm^2 fabrication process. This is the highest scale of device integration in the quantum nano-device circuits. Various subsystems for arbitrary bit can be designed and typical ones were fabricated and confirmed correct operations as shown in **Fig. 2(b)**.

Feasibility of this approach for digital system implementation was clarified by successful design of a static 2-bit processor, called nanoprocessor (NPU), as shown in **Fig. 3**. Execution core is the quantum BDD-based ALU. Sequential circuits and level adjusters are designed with WPG-controlled nanowire FETs, thus whole of the system can be implemented on a hexagonal network structure. Operation of each component has been confirmed by experiment or simulation. Estimated system power consumption was only 10 nW at 10 MHz in quantum regime. GHz operation capability of systems was found from measured cutoff frequency over 2 GHz of discrete WPG devices.

For further high-density integration of the system with narrower nanowires, formation of embedded GaAs nanowires by selective MBE growth has been investigated. As shown in **Fig.4**, hexagonal networks over 200M nodes/cm^2 could be successfully formed, which will realize 20 x 29 μm^2 size of the 2-bit NPU. Node devices using embedded nanowires were fabricated and characterized[3], showing good prospects of the nanowire networks for implementing the systems in high dense.

[1] H. Hasegawa and S. Kasai, Physica E **11** (2001) 149.
[2] S. Kasai and H. Hasegawa, IEEE EDL **23** (2002) 446.
[3] T. Tamura, M. Yumoto, T. Sato and H. Hasegawa, to be presented at 2004 EMC, Jun. 23-25, 2004, Nortre Dame.

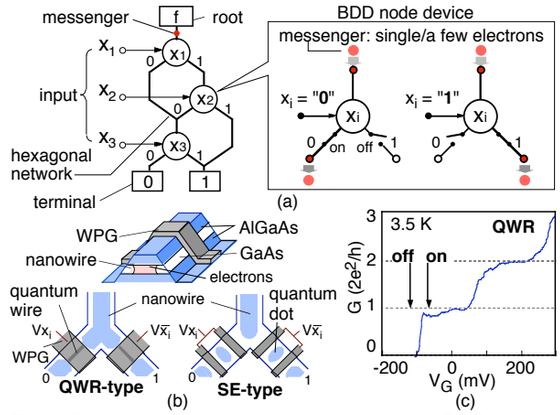

Fig. 1 Concept and implementation of hexagonal BDD circuits.

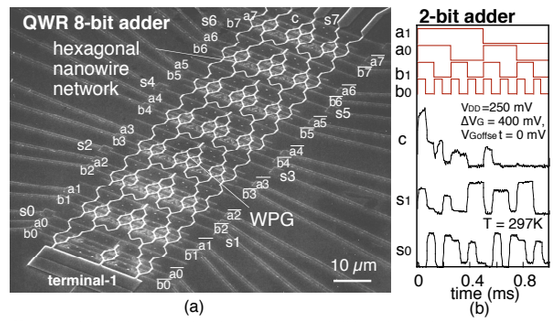

Fig. 2 (a) Fabricated 8-bit adder and (b) 2-bit adder operation.

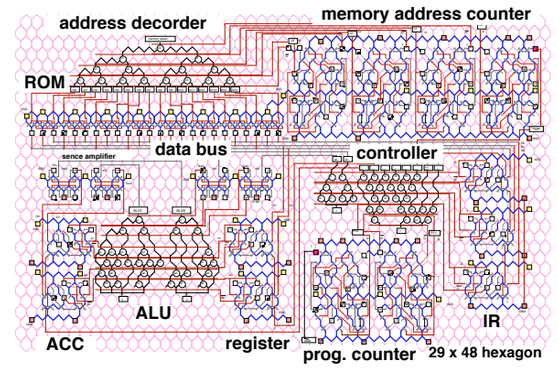

Fig. 3 Hexagonal BDD-based 2-bit nanoprocessor design.

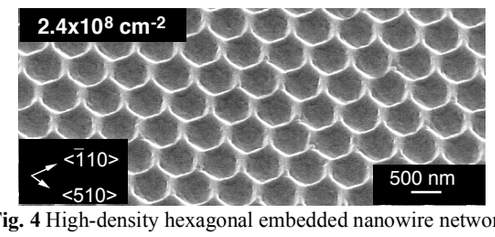

Fig. 4 High-density hexagonal embedded nanowire network.