Abs. 1050, 206th Meeting, © 2004 The Electrochemical Society, Inc.

# POLISHING OF EPITAXIALY GROWN POLY-SOI SUBSTRATES BY MEANS OF FIXED ABRASIVE CMP FOR BONDING PURPOSES

Martin Kulawski[1], Hannu Luoto[1], Kimmo Henttinen[1], Jari Mäkinen[2], Maria Hokkanen[2], Frauke Weimar[3], Feben T. Gobena[4]

[1]:VTT Microelectronics, Tietotie 3, P.O. Box 1208, FIN-02044 VTT; Espoo; Finland
[2]:Okmetic Oy; Piitie 2; P.O. Box 44; FIN-01301 Vantaa; Finland
[3]:3M Deutschland GmbH; Carl-Schurz-Str.1; D-41453 Neuss; Germany
[4]:3M Center, Bldg. 251-03-A07, St.Paul, MN 55144-1000

Contact: martin.kulawski@vtt.fi

Silicon-on-Insulator (SOI) substrates are becoming more and more popular in IC-Industry. But especially in the Micromechanical area (MEMS) many applications are benefiting from this technology. However often a thick film of silicon is needed leading to other than the in the IC-Technology often used Smart-Cut™ technique and its related [1].

For special material requests a different manufacturing process besides the bonding of two wafers and the subsequent grinding and polishing is required. This can be due to extreme doping level or mechanical properties.

One approach is, to grow epitaxialy a thick silicon film on top of the oxidized handle wafer. As the film can only grow in polycrystalline form on top of the oxide its surface appears very rough and irregular and a high probability is given that bigger defects are included.

To result in a POLY-SOI substrate for further processing the straight forward way to smoothen the surface, removing the irregularities and to planarize the film is to perform a polishing step.

Chemical Mechanical Polishing (CMP) is not only known for its capabilities to planarize structures but also used for decades in the manufacturing of silicon. However utilizing it on polycrystalline material and taking care that all surface roughness and possible defects are removed while simultaneously the sensitive grain boundaries should not be attacked leads to a new challenge. The work presented in this paper incorporates the use of the fixed abrasive technology to planarize the as-grown film regardless its roughness or defects.

6” wafers were oxidized and a poly-silicon layer was epitaxialy grown on top of the oxide. Surface roughness was measured by atomic force microscopy (AFM) and film thickness was investigated by optical reflection as well as Fourier-Transform infrared radiation (FTIR). Polishing was done using conventional techniques and experimental fixed abrasive pads from 3M.

It is shown that by introducing the fixed abrasive polishing to the CMP procedure a flat and smooth POLY-SOI wafer can be made (see Figure 1 and 2), suitable for subsequent bonding. Surface roughness values of 1nm rms and below are reached by less than 3 µm removal versus more than 1 µm rms of incoming roughness.

Additionally a comparison study is made with conventional polishing under use of different pads and slurries.

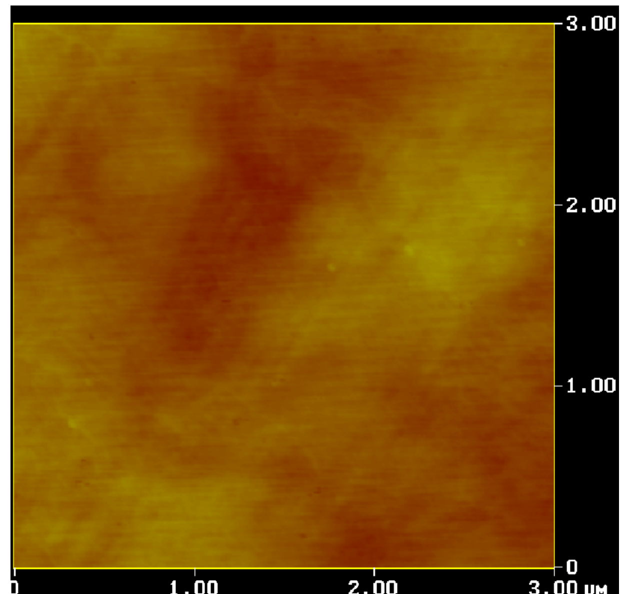


Figure 1: Polished POLY-SOI surface. No grain boundaries or particle residues are visible after Fixed Abrasive Polishing

| Image Statistics | |
|---|---|
| Img. Z range | 3.902 nm |
| Img. Mean | -0.000003 nm |
| Img. Raw mean | 0.150 nm |
| Img. Rms (Rq) | 0.675 nm |
| Img. Ra | 0.556 nm |
| Img. Rmax | 3.954 nm |
| Img. Srf. area | 9.001 µm² |

Figure 2: Table of surface roughness values for Figure 1. The average value of roughness is clearly below 1 nm

## REFERENCES

[1]: FRANCOIS J. HENLEY & MICHAEL I. CURRENT, Semiconductor Fabtech, 12th Edition, PP.204