Experimental Study and Simulation of Stress-Induced Cavities in Silicon

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Since the introduction of local oxidation as a major component of IC isolation schemes, we have observed surface defects formed in silicon in the center of regions covered with nitride films. Such defects generated under the patterned Si_3N_4/SiO_2 films during annealing of silicon wafers were studied in [1]. The authors showed that the defects were cavities and proved that their growth depended on mechanical stresses in silicon caused by the films. However, the mechanism of cavity formation was still unknown.

In this paper, the formation of cavities in silicon under nitride films is studied experimentally and simulated. For the first time, the development of stress-induced trenches is reported.

CZ (100) 150 mm silicon wafers were used in the experiments. The wafers were oxidized at 950 °C in dry oxygen to grow 175 Å of pad oxide. Subsequently, a layer of LPCVD silicon nitride was deposited. Two values of the nitride film thickness were employed to vary the level of stress in underlying silicon: 5000 Å and 3400 Å. Then the films were patterned using conventional lithography and plasma etch to obtain different nitride geometries. The wafers were annealed in nitrogen at 800, 900, 1000, or 1100 °C for 60 min. Then the oxide and nitride films were removed in hydrofluoric acid, and the silicon surface was examined using optical microscopy, which revealed the formation of cavities in various structures. All of the cavities were found in the middle of nitride-covered regions. The visible size of the cavities varied, depending on structure geometry, nitride thickness, and to a lesser degree, anneal temperature. In some structures, the cavities were so close to each other that a continuous trench was formed in the middle of the structure. The shape and size of the identified cavities were evaluated with an atomic force microscope (AFM). The largest trenches had a volume of almost 1 μm^3 per 1 μm of their length (Fig. 1).

The results of the trench volume measurements were compared to the corresponding estimates obtained using simulation of point defect fluxes. A model for the stress-induced redistribution of point defects in silicon [2] was used in the simulation. It incorporates equilibrium conditions different for defects at the surface and in the bulk of silicon, and takes into account stress-dependent surface generation and recombination of point defects and their surface diffusion. In the model, equilibrium concentrations of intrinsic point defects depend exponentially on hydrostatic pressure in silicon. For bulk interactions, the calculations yielded the activation volumes of about 2.5 $Å^3$ for interstitials and 2.3 $Å^3$ for vacancies. The activation volumes for point defect surface generation and recombination close to 18 $Å^3$ were used.

The formation of cavities in silicon under patterned nitride films was simulated using the developed model. The simulations showed that the difference between the bulk and surface activation volumes provided interstitials near the silicon surface in excess of the bulk equilibrium concentration. This caused essential mass transfer of silicon from the areas under the middle of nitride films where pressure was at maximum. The reverse diffusion of vacancies contributed to this mass transfer. It was shown that stress-induced surface diffusion of silicon atoms [3] played the major role in the development of surface depressions in silicon.

Employed in computer simulations, the model qualitatively explained the intriguing phenomenon of stress-induced cavity formation. The results of the calculations are interpreted as indicating a potential capability of the stress-induced point defect diffusion to establish fluxes sufficient for the cavity growth.

From the performed calibration, values of 10^{-3} cm^2/s and 0.9 eV were found for the pre-exponential and activation energy of the silicon self-diffusion coefficient on the surface of Si structures under the patterned Si_3N_4/SiO_2 films. A satisfactory correlation between the experimental and simulation data (Fig. 2) indicates that the stress-induced surface diffusion of silicon atoms is a probable mechanism of the cavity growth in silicon.

Various methods of strain engineering aimed at increasing transistor drive current have recently gained wide popularity. Obviously, such technologies are especially susceptible to the stress-induced defects. The presence of cavities in active device regions would be harmful, especially for gate oxide integrity. Therefore, the results of the present study are valuable from the perspective of preventing or controlling stress-induced cavities in silicon device manufacturing.

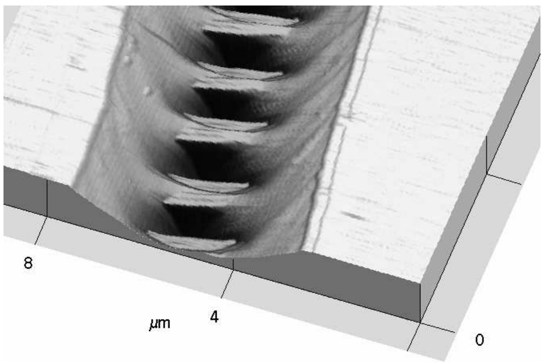

Fig. 1. AFM image of stress-induced cavities in silicon forming a continuous trench.

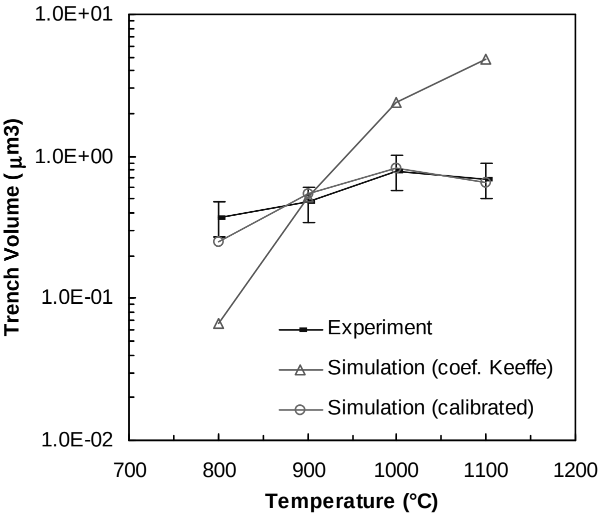

Fig. 2. Stress-induced trench volume per 1 μm of length vs. anneal temperature.

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