Dielectric Degradation of Gate SiO_2 Films by Cu Contamination Posterior $_t$o MOS Capacitor Fabrication

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Introduction

To suppress resistance-capacitance delay in ultra-large scale integrated circuits, Cu has been applied as a wiring material, because of the resistivitity lower than Al. However, it is to be feared that the diffused Cu deteriorates the electronic device characteristics because of high diffusivity during thermal treatment even at low process temperature.

MOS structures have been generally fabricated prior to Cu wiring processes. There are few reports of dielectric degradation of the gate SiO_2 films by the Cu contamination posterior to fabrication of the MOS structures. After Cu wiring processes, a sintering heat treatment at about 400C is indispensable to improve the instability of the electric characteristics at the Si/SiO_2 interface or to relax the process damage generated by wiring processes. There is enough possibility that Cu atoms invade into the MOS devices and deteriorate the device characteristics, especially the dielectric characteristics of the gate SiO_2, since Cu has a high diffusivity.

In this manuscript, an influence of Cu contamination posterior to the MOS structure fabrication on the dielectric characteristics of the gate SiO_2 films is investigated.

Experiment-1 Cu contamination through Si substrate from a contact hole

Gate oxides with a thickness of about 25 nm were thermally grown on (100)-oriented, CZ-grown, Si wafers in dry O_2 ambient. Phosphorus-doped polycrystalline Si film was deposited on the gate oxides. SiO_2 films, on which it is difficult to adsorb Cu atoms, were formed on both sample surfaces at 1000 C. After opening a hole of the SiO_2 film and the polycrystalline Si film at the center of the Si wafer with a diameter of about 1 mm, Cu atoms of $1x10^{15}$ cm^{-2} were adsorbed on the Si surface by immersing in Cu-included water. Next, the SiO_2 film on the polycrystalline film was removed, followed by photolithography and wet-etching of the polycrystalline Si film to form gate electrodes of 100 um x 100 um. A leakage current distribution of the Cu-contaminated MOS capacitors was measured.

Experiment-2 Cu-contamination from Si wafer backside surface

To contaminate the gate SiO_2 films by Cu, the Cu atoms of about 5 x 10^{13} cm^{-2} were adsorbed only on the Si wafer back surface. After Cu adsorption, the Si wafers were isothermally annealed at 400 C for 30 and 120 min. in N_2. To confirm the Cu contamination influence on the dielectric characteristics of the gate SiO_2, the annealing treatments at temperature higher than the actual process temperature were also performed in this study. Constant current stress-time dependent dielectric breakdown (CCS-TDDB) measurements [1,2] were performed as dielectric characteristic evaluation. In capacitance recovery measurements, MOS capacitors with guard-rings were used.

Results and discussion

The leakage currents at the gate voltage of 17V are measured as a function of the distance from the contamination hole to the measured MOS capacitors. Increase of the leakage current (hump) was reduced with increasing distance from the contamination hole. It is clear that the increase of the gate leakage current was attributed to the Cu-contamination of the gate SiO_2 films. The Cu contamination is a strongest factor inducing the humps. The current increases were unevenly distributed in the region of 4.5 mm from the contamination hole. Comparison of the calculation distribution and the leakage current distribution indicates that the appearance of the humps corresponds to the Cu arrival of more than 10^{11} cm^{-2}.

To confirm a precise influence of the Cu diffusion at 400 C, the MOS capacitors after the Cu contamination were isothermally annealed at 400 C. The gate voltage shifts during CCS-TDDB of $5x10^{-6}$ A/cm^2 were measured as a function of the stress time. In the case of the annealing time of 30 min, the Q_{BD} was slightly lower than the reference samples. In the case of 120 min, however, the number of the accidental breakdown events of the contaminated MOS capacitors was remarkably increased and the Q_{BD} of them was clearly decreased in comparison with the reference. The Cu contamination posterior to the MOS fabrication induced the leakage current increase and the degradation of the dielectric characteristics of the gate SiO_2 films.

Not all the Cu-contaminated capacitors had the humps or the low breakdown voltages. This indicates that there is a threshold amount of the Cu contamination which induces the dielectric characteristics [3]. The humps of the leakage current were not induced until the Cu atoms of the threshold amount arrive at the Si/SiO_2 interface. The experimental results suggest that some combination of the Cu atoms and other factors induced the dielectric degradation as described above. In the case of the contamination annealing at 400C, the threshold Cu contamination amount might be about $10^{11}cm^{-2}$. To precisely investigate a small amount of the Cu atoms, the generation-recombination lifetimes near the Si/SiO_2 interface were studied by the capacitance-time (C-t) method [4]. With increasing annealing temperature, the surface recombination velocities were increased and the generation lifetimes were decreased. Such annealing temperature dependence suggests that the Cu contamination at the Si/SiO_2 interface shortened the recovery time of the capacitance. The generation-recombine-tion centers correspond to the Cu atoms present at the Si/SiO_2 interface.

Considering the C-t results, we can explain the dielectric degradation described above as follows. The positive Cu ions were injected from anode through the gate SiO_2 films by the induced oxide electric field. The accumulated Cu ions near the anode degrade the dielectric characteristics [5]. With increasing annealing temperature, the number of the accumulated Cu ions increases and the degradation were accelerated. In the present experiments, the Cu atoms near the Si/SiO_2 interface were a main origin of the leakage current increase and dielectric breakdown deterioration since the negative gate voltage was applied.

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