Single Spin Silicon Etching Behavior Analysis by Quality Engineering (Taguchi Method)

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LSI packaging trend keeps the demand of thin wafers, recently less than 50μm thickness is the up-to-date devices production target. Mechanical grinding can provide the uniform thickness wafers and practical processing speed, however, always leaves the mechanical damage on the surface. This would seriously degrade the wafer and chip strength. Among several damage removal methods, wet etching is the only one of no damage causing process.

The silicon etching is the exothermic reaction, and difficult to control the etching uniformity with the conventional wet bench process. Therefore, the wet silicon etching is mainly used to remove the mechanical damage with few μm etching, while the parameter optimized single spin etching can make over 100μm etching amount uniform etching, hence no mechanical damage thinned wafers are obtained by it. (Fig. 1)

This single spin etching system is not so easy to make the mechanism model because of its parameter numbers and the reaction. Here the quality engineering method (Taguchi method) is applied to analyze the main parameters and define their tolerances. The divided area uniformity analysis successfully revealed the main parameters and contributed to make the robust system design.

Table 1 shows the example of the selected parameters with their experiment range. To make the parameter tolerance design, the parameters are experimented under three level conditions. Fig. 2 shows the etched amount distribution in wafers based on the L18 DOE. The # numbers mean the experiment conditions based on L18. The lines are actually measured thickness values. The black and white circles calculated just from the main parameters are in good accordance with the measured values. The critical parameters are under enough control.

Controlling the main parameters and multi step etching improves the etching uniformity range down to a few μm etching range, i.e. the wafer TTV difference in the etching is the same level of the flatness measurement tool resolution. This fine etching technology could be applied not only for final wafer thinning but also for the leading edge wafer manufacturing process.

Fig. 1 The etching amount distributions in a 200mm wafer is plotted as the targeted etching amount. All the 19 measurement points along the diameter are within the bars. The inner part of the dotted lines means the etching amount uniformity is less than 5% of max-min calculation. The single spin etching keeps less than 5% uniformity etching over 200μm etching amount range.

Table 1 The parameters used in the L18 Quality engineering analysis. Level 2 is the proved uniform etching condition.

Factor	level 1	level 2	level 3
Etching amount	40μm	100μm	-
Spin speed	w-20%	w	w+20%
Chemical flow	x-50%	x	x+50%
Boom swing	y-20%	y	y+20%
Chuck N2	z-20%	z	z+20%

Fig. 2 The etching amount distribution in 150mm wafers depending on the different spin etching conditions. The whole wafer uniform condition can exist between the symmetrical patterns.