Via-filling by Copper Electroplating using Current Waveform Control

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Miniaturization of printed circuit boards and the semiconductor devices have been progressed, because the electronic deices are sharply downsized. Especially, Portable products such as cellular phones, PDAs and wireless handheld devices continue to require higher functionality in the smallest possible footprint. In years past, multi-chip modules (MCMs) and system-on-chip (SOC) solutions have fulfilled these needs for the wireless industry. Today, system-in-package (SIP) technology is emerging as a more reliable alternative to MCM and SOC designs. Also, SIP solutions have been extensively studied to realize high-density packaging and high operation performance. In this technology, through Si chip electrode is the shortest connection as a key technology for 3D chip stacking.

In the previous research, we confirmed that void-free and bottom-up filling was accomplished by copper electroplating using a copper sulfate bath with polyethylene glycol (PEG), bis (3-sulfopropyl) disulfidedisodium (SPS) and janus green (JGB). It has obtained the similar result also by the damascene process or the build-up process. [1)-3)]

In this study, copper filling for 50μm via-holes with high aspect ratio were examined by controlling the additives and current waveform. The purpose of this study is via-filling by copper electroplating. In addition, the influence of additives on copper deposition was studied by using Linear Sweep Voltammetry (LSV) and Quartz Crystal Microbalance (QCM).

High copper concentration bath so-called decorative bath, which was used as the electroplating bath. PEG, SPS and JGB were used as additives. For LSV measurement, a copper rotating disk electrode and platinum were used as a working and counter electrode, respectively. Ag/AgCl electrode was used as a reference electrode.

Via-filling could not achieved by using PEG-SPS-JGB at 1A/dm^2. Fig.1 shows the thickness of deposited copper with and without additives at 0.1-5 A/dm^2. Thickness of deposited copper at high current density was decreased when PEG added to the electroplating bath. It is considered that copper deposition at high current density area was suppressed by the adsorption of large amount of PEG. From these results, PEG seemed to selectively adsorb at the corner area of via-holes, which concentrated the current lines, and copper deposition was inhibited at these area during electroplating. Accordingly, copper electroplating at high current density was employed for via-holes. Via-filling were achieved by plating at high current density in the initial stage as shown in Fig.2. Behavior of PEG at high current density on copper deposition was examined by using LSV. Fig. 3 shows the effect of pre-deposition with PEG for the LSV curves. From these results, copper deposition was inhibited by the pre-deposition since the adsorption of PEG were gradually increased with increasing the current densities. In order to elucidate the mechanism of copper deposition, the effects of JGB and SPS on copper deposition were also examined by LSV and QCM.

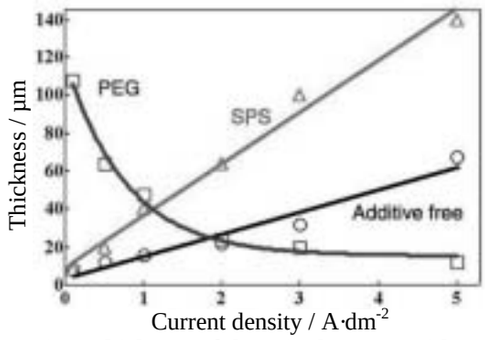

Fig.1 Thickness of deposited copper with and without additive at 0.1-5 A·dm^{-2}
PEG : 100 mg·dm^{-3}, SPS : 1 mg·dm^{-3}, JGB : 0.1 mg·dm^{-3}

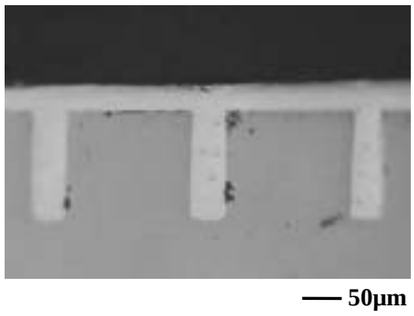

Fig.2 Cross sectional trench images of deposited copper by electro plating using current waveform

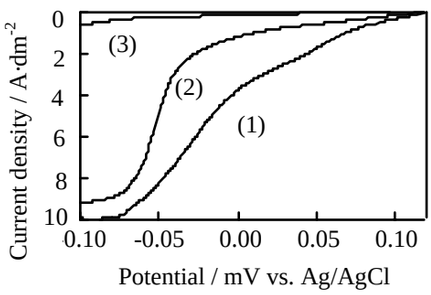

Fig. 3 The effect of pre-deposition with PEG at 1 and 5 A·dm^{-2} on LSV curves.
(1) Without pre-deposition, (2) Pre-deposition at 1 A·dm^{-2}, (3) Pre-deposition at 5 A·dm^{-2}

References

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