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Enhanced Mobility CMOS

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Introduction

This is an exciting time in the field of silicon-based heterostructure MOSFETs. The use of strain to enhance carrier transport in silicon has moved from Hall-effect measurements on modulation-doped strained Si/relaxed SiGe structures in physics laboratories in the early 1990's, to mainstream CMOS today. Research on biaxial tensile strained Si on relaxed SiGe has demonstrated that strain is a key parameter in controlling carrier mobility in silicon, and moreover that drain current enhancements associated with improved mobility in long-channel devices persist at short channels [1,2]. Indeed, despite scaling channel lengths into the sub 50-nm regime, mobility continues to be a critical parameter, and transport in MOSFETs remains far from ballistic [3,4]. This is partly because mobility is degraded by increased channel doping and vertical electric field as bulk devices are scaled. Research on strained Si on relaxed SiGe has demonstrated that recovering carrier mobility by engineering channel transport can have a significant impact. "Strained silicon" as well a mobility enhancement techniques in general are now included in the ITRS roadmap.

Strained Si R&D: Global vs. Local Stress Techniques

There are two dominant methods, global and local stress, for introducing strain in the silicon channel. Both methods produce changes in the silicon bandstructure due to the breaking of the crystal symmetry, and hence alter carrier scattering rates and effective masses. Given the difficulties associated with geometrical scaling, industrial interest in strain engineering of mobility has increased recently, as evidenced by the number of publications at the International Electron Devices Meeting (Fig. 1). Global stress techniques employ epitaxial technology to generate a thin layer of strained Si on relaxed SiGe grown on silicon. The silicon channel experiences biaxial tensile stress in the 1 to 2 GPa range, generally larger than obtained in local techniques. This method yields ~ 2X electron mobility enhancements at all vertical effective fields in the silicon channel (E_{eff}), and ~ 2X hole mobility enhancements at low E_{eff}, which decreases to 1X at vertical fields typical of bulk p-MOS. The global technique enhances mobility at all channel lengths and widths, and thus is more clearly separated from other effects such as series resistance.

Local stress, which relies on process techniques such as modifications to shallow trench isolation, high-stress capping layers around the gate, and materials such as epitaxial SiGe in the source/drain regions, is effective in small devices where it is possible to impact the stress in the center of the channel. This method is layout sensitive and complex, but has been implemented in 90 nm manufacturing [5]. With local stress it appears possible to maintain a high hole mobility enhancement with increasing E_{eff}, which has been an issue for strained Si. The improvement in n-MOSFET mobility is smaller than for biaxial tensile strained Si on relaxed SiGe.

Options Beyond the First Generation

There have been many demonstrations of drain current enhancement (~10 to 30%) in strained Si/relaxed SiGe CMOS manufacturing processes. Strained Si/relaxed SiGe bulk wafers are commercially available, and strained Si on relaxed SiGe on insulator has been demonstrated [6-8]. Beyond the first generation of strained Si are several options, including: (1) Ge-free strained Si Directly on Insulator (SSDOI) [9-11], and (2) high-Ge-content structures. Fig. 2 compares cross-section transmission electron micrographs of strained Si/relaxed SiGe and SSDOI technology. The SSDOI structure has a number of attractions. It eliminates issues associated with SiGe during MOSFET processing, such as Ge updiffusion and enhanced diffusion of n-type dopants in SiGe. To produce SSDOI, strained Si is grown by the usual method and transferred to a handle wafer by bonding and substrate removal. The strain is stable during high temperature processing after removal of the SiGe. SSDOI is also compatible with ultra-thin body and perhaps multi-gate MOSFETs, which offer improved electrostatic integrity, and hence the lowest I_{off} for a given I_{on}. High-Ge-contents can be used to obtain larger enhancements. Dual-channel structures that use ultra-thin strained Si/strained Ge, on relaxed $Si_{0.5}Ge_{0.5}$ yield 10X hole mobility enhancements and 2X electron mobility improvements in test devices [12].

Challenges and Summary

Fundamental understanding of the impact of 3D stress on mobility and high field transport is lacking. Mobility in multi-layer heterostructure channels requires investigation. Longer-term solutions will involve *combinations* of various technologies, including strain engineering (local and global techniques) and strained semiconductors on insulator.

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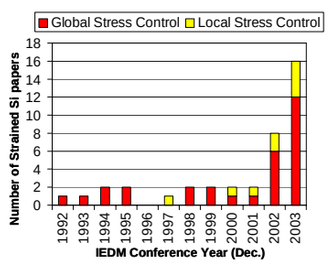

Fig. 1: Number of papers on strained Si at the International Electron Devices Meeting (IEDM).

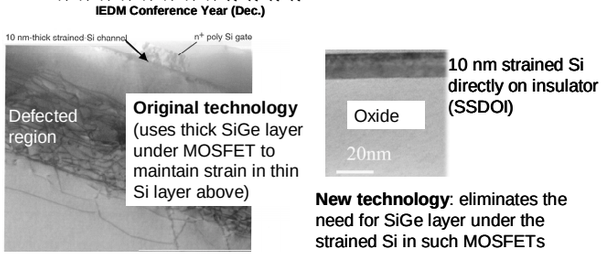

Fig. 2: Comparison of (a) bulk strained Si/relaxed SiGe to (b) SSDOI.