Complementary SiGe BiCMOS

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Abstract

We demonstrate high-speed, complementary SiGe:C HBTs in a BiCMOS technology based on a new, unconventional process architecture. For the pnp device, f_T/f_{max} values of 90GHz/125GHz at BV_{CEO} = 2.6V and a ring oscillator delay of 7.9ps were achieved. The simultaneously fabricated npn HBTs reach nearly the performance of the npn-only BiCMOS process confirmed by f_T/f_{max} values of 180GHz/185GHz and a ring oscillator delay of 4.6ps. A pnp-only BiCMOS flow produces peak f_T/f_{max} values for pnp devices of 115GHz/115GHz. Device design issues associated with the optimization of the transistor performance of the SiGe:C pnp HBTs as well as with the integration of these device with a BiCMOS process are discussed in detail.

Summary

A complementary bipolar technology offers significant performance advantages over an npn-only technology for high-speed analog and mixed-signal circuit applications, assuming that the performance of the pnp is comparable with that of an npn device (1). The performance of npn SiGe HBTs has been substantially increased by optimizing the vertical profile and the device construction assisted by adding carbon (2). In contrast, there has been little progress in the peak performance of pnp devices for more than 10 years, whether in complementary bipolar (CBi) (3), (4), (5), in CBiCMOS (6), (7), or in pnp-only (8) configurations.

Physical properties such as charge carrier mobilities, dopant diffusivities, or the band lineup in the Si/SiGe system make it difficult to realize pnp transistors with the same peak performance as that of npn's. Moreover, it has proven difficult to shape by epitaxy in a CVD reactor such narrow n-base layers as they are known for a p-type base.

The optimization of heterojunction pnp transistors within a CBiCMOS process for operation at high speed has to consider also implications resulting from the process architecture. In several approaches (4), (7), SOI wafers are used instead of bulk material, in order to reduce parasitic RC components and to avoid an extra well for the isolation of the complementary bipolar transistors. Beside the disadvantage of higher wafer costs, this may cause additional self-heating effects. Apart from differences in the isolation scheme, most of the known CBi(CMOS) processes use epitaxial buried subcollectors and deep trench isolation increasing the process complexity and making the integration with standard CMOS processes more complicate. In addition, special attention has to be focused on controlling dopant outdiffusion from the highly-doped collector wells (7), (9). Already the thermal cycle of a typical shallow trench formation compromises the freedom of the profile design essentially.

Based on our results published in (10), we present here a more detailed description of a novel complementary bipolar (CBi)CMOS process providing an isolated SiGe:C pnp HBT with an outstanding high speed performance. In particular, we show how the unconventional process flow helps to overcome drawbacks of previous approaches described above.

The pnp device has been integrated into a 200GHz npn BiCMOS technology (11). The performance gain of the pnp HBTs is mainly due to a highly tuned vertical doping profile taking advantage of the reduced P diffusion in the C-doped base combined with the special collector construction of previously reported 200GHz npn transistors (11). The key feature of both the npn and the pnp HBT process is the formation of the whole HBT structure in one active area without shallow trench isolation between the active emitter and the collector contact region. This construction allows one to integrate an isolated pnp into a CMOS process easily, while simultaneously minimizing collector resistance and capacitance. For high f_T values, steep collector well profiles have to be realized. This is achieved in the present approach by restricting the essential thermal budget for the highly-doped wells to the final RTP step for annealing the SD implants.

The high-speed capability of the pnp transistors is illustrated by Fig. 1. Transit frequencies f_T and maximum oscillation frequencies f_{max} vs. collector current are shown in Fig. 1 for pnp devices fabricated in the CBiCMOS process, and for pnp transistors of the pnp-only BiCMOS flow. Peak f_T/f_{max} values of 115GHz115GHz for the pnp-only preparation and 90GHz/125GHz for the CBiCMOS flow pave the way for a new platform of high-speed complementary bipolar circuits.

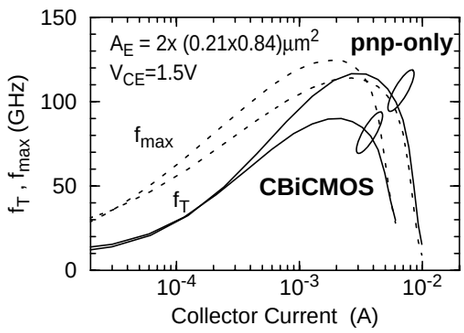

Fig. 1. Transit frequency f_T and maximum oscillation frequency f_{max} vs. collector current for pnp HBTs fabricated in the complementary BiCMOS and for pnp devices from a pnp-only BiCMOS. f_T and f_{max} were determined from the extrapolation of h_{21} and U at 30GHz with -20dB decay per frequency decade.

References

(1) J. D. Cressler, and G. Niu, *Silicon-Germanium heterojunction bipolar transistors*, Boston, London: Artech House, 2003.

(2) S. J. Jeng et al., "A 210-GHz f_T SiGe HBT with a non-selfaligned structure," *IEEE Electron. Device Lett.*, vol. 22, pp. 542-544, 2001.

(3) T. Onai, E. Ohue, Y. Idei, M. Tanabe, H. Shimamoto, K. Washio, and T. Nakamura, "Self-aligned complementary bipolar technology for low-power dissipation and ultra-high-speed LSI's," *IEEE Trans. Electron Devices*, vol. 42, pp. 413-417, 1995.

(4) M. C. Wilson et al., "Process HJ: A 30GHz npn and 20GHz pnp complementary bipolar process for high linearity RF circuits," *in Proc. BCTM*, p. 164, 1998.

(5) W. Klein and Bernd-Ulrich H. Klepser, "75 GHz bipolar production technology for the 21st century," *in Proc. ESSDERC*, p. 88, 1999.

(6) Y.-F. Chyan et al., "A 50GHz 0.25-µm implanted-base high-energy implanted-collector complementary modular BiCMOS (HEICBiC) technology for low-power wireless-communication VLSIs," *in Proc. BCTM*, p. 128, 1998.

(7) B. El-Kareh et al., "A 5V complementary-SiGe BiCMOS technology for high-speed precision analog circuits,"*in Proc. BCTM*, 11.4, 2003.

(8) D.L. Harame et al., "55 GHz polysilicon-emitter graded SiGe-base PNP transistors," *in Proc. VLSI Tech. Dig.*, p. 71, 1991.

(9) J. D. Cressler, J. Warnock, D. L. Harame, J. N. Burghartz, K. A. Jenkins, and Ching-Te Chuang, "A high-speed complementary silicon bipolar technology with 12-fJ power-delay product," *IEEE Electron. Device Lett.*, vol. 14, pp. 523-526, 1993.

(10) B. Heinemann et al. , "A complementary BiCMOS technology with high speed npn and pnp SiGe:C HBTs," IEDM Tech. Dig., p. 117, 2003.

(11) B. Heinemann et al. , "Novel collector design for high-speed SiGe:C HBTs," IEDM Tech. Dig., p. 775, 2002.