

0.13 μm SiGeC BiCMOS technology

A. Chantre, M. Laurens, P. Chevalier, A. Monroy
F. Deléglise, C. Fellous, L. Rubaldo, D. Dutartre
ST Microelectronics
850, rue Jean Monnet, F-38926 Crolles Cedex, France
E-mail: alain.chantre@st.com

Introduction

SiGeC BiCMOS technology is a strong contender for single-chip solutions for wireless and broadband communications systems. Various application fields like high bit-rate optical networking or automotive radar demand SiGe HBTs with f_T/f_{max} above 150GHz and high density CMOS to perform complex digital signal processing. This raises many device and integration issues which will be discussed in this paper and illustrated using results from ST 0.13 μm SiGeC BiCMOS technology.

160GHz 0.13 μm SiGeC BiCMOS technology

This technology (ST-BiCMOS9) combines a 0.13 μm CMOS backbone with >160GHz f_T/f_{max} SiGeC HBTs (1). The bipolar transistor features a non selective epitaxial (NSEG) base, a double-polysilicon quasi self-aligned (QSA) emitter/base (E/B) architecture, and a monocrystalline emitter (Fig. 1). Carbon doping of the SiGe base, arsenic doping of the emitter, and a novel BiCMOS integration scheme are used to solve thermal cycle and structural processing issues.

Fig. 2 demonstrates peak f_T/f_{max} values well above the 160GHz target (with 1.8V BV_{CEO}), despite the non self-aligned E/B structure. This result shows that the use of the robust QSA-NSEG HBT construction can be extended far into high-speed applications. The moderately high current density at peak f_T ($J_C \sim 8\text{mA}/\mu\text{m}^2$) is accommodated by a unique transistor layout with two rows of contacts on emitter (Fig. 1) to comply with electromigration rules of the core CMOS process. As shown in Fig. 2, a free high-voltage (3V BV_{CEO}) SiGeC HBT with 77GHz f_T and >160GHz f_{max} is also available. The Ge profile in the SiGeC base has been carefully optimized to enable proper operation of this device, without compromising the high-speed HBT.

The bipolar/CMOS integration scheme used in this technology minimizes perturbation to MOSFET characteristics by the added bipolar process steps, as demonstrated in Fig. 3. Manufacturability aspects including yield results, on-wafer homogeneity and lot-to-lot reproducibility data for the high-speed SiGeC HBT will be highlighted in the conference paper.

230GHz 0.13 μm self-aligned SiGeC HBT

A fully self-aligned (FSA) HBT version of this technology is also being investigated to explore ultimate performance limits of SiGeC HBTs in a full BiCMOS process. As shown in Fig. 4, the approach used is based on the selective epitaxial (SEG) base concept (2), which is mask-compatible with the QSA-NSEG approach. Compared to alternative E/B self-alignment schemes, the FSA-SEG construction minimizes transistor parasitics, at the expense of a more complex SiGeC base deposition process. However, this difficulty can be solved, and good process manufacturability and world class device performances such as shown in Fig. 5 (225GHz f_T and 230GHz f_{max}), will be demonstrated.

References

1. M. Laurens et al, BCTM Tech. Dig., p. 147 (2003)
2. P. Chevalier et al, ESSDERC Proc., p. 299 (2003)

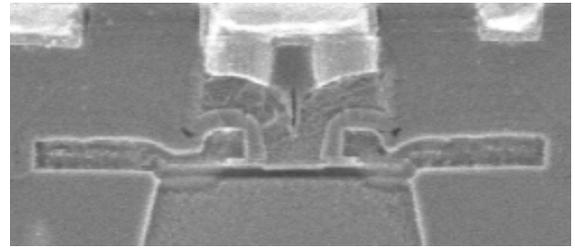


Fig. 1 : QSA-NSEG SiGeC HBT used in ST-BiCMOS9

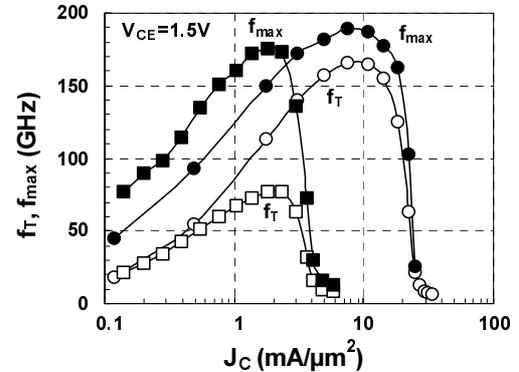


Fig. 2 : HF characteristics of high-speed ($A_E = 0.17 \times 9.7 \mu\text{m}^2$) and high-voltage ($A_E = 0.17 \times 5.6 \mu\text{m}^2$) SiGeC HBTs in ST-BiCMOS9

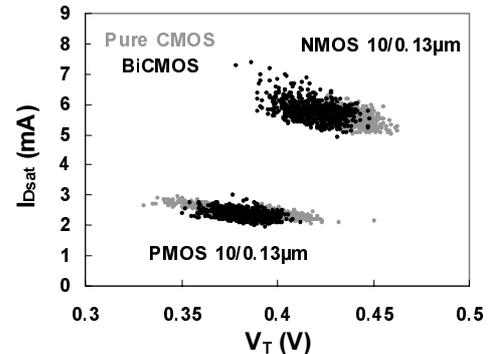


Fig. 3 : $I_{\text{Dsat}}-V_T$ characteristics for 1.2V low leak nFET and pFET: comparison between BiCMOS9 and 0.13 μm CMOS

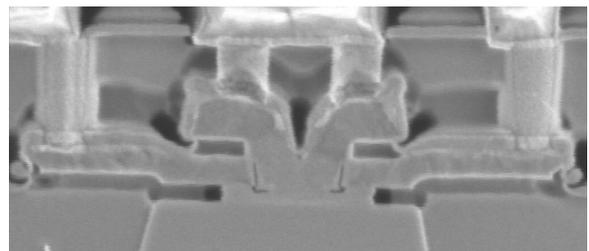


Fig. 4 : FSA-SEG SiGeC HBT fabricated using 0.13 μm technology

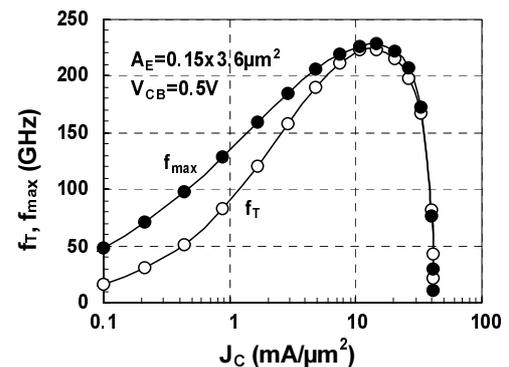


Fig. 5 : HF characteristics of FSA-SEG SiGeC HBT fabricated using 0.13 μm technology