Emitter-Base Design Tradeoffs in 120GHz SiGe HBTs

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email: josepha@us.ibm.com / Ph: 802-769-4698 / Fax: 802-769-9659**Suggested Subcommitte – HBTEmitter-Base Design Tradeoffs in 120GHz SiGe HBTs**

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We present a detailed study on the tradeoffs in emitter-base profile optimization for a 120GHz SiGe HBT. The influence of two key process variables on the HBT electrical characteristics were investigated. Results indicate that careful optimization of the emitter-base profile will be required to achieve critical HBT performance parameters.

High performance SiGe HBTs in a BiCMOS framework is highly desirable for market applications that push the frequency envelope such as SONET, high-speed instrumentation, and automotive. One can attain very high performance SiGe HBTs with f_T/f_{max} greater than 200 GHz by vertical and lateral scaling [1 - 3]. Vertical scaling mainly employs: (a) reducing base transit time (τ_b) by reducing basewidth and increasing built electric field using Ge ramp, (b) reducing the collector-base transit time and base push out by increasing the collector doping, and (c) reducing emitter delay time (τ_e) by forming abrupt and shallow emitter junctions.

The 120GHz f_T SiGe HBT integrated into the 0.18μm SiGe BiCMOS technology utilizes an aggressive Ge profile for reduced τ_b and an emitter profile for improved R_E and τ_e [4, 5]. For this device, we expect a stronger influence on the electrical characteristics as the emitter-base junction depth is varied. It is important, therefore, to understand the design tradeoffs of key process parameters that influence such variability.

The emitter intrinsic cap layer that sets EB junction and the Arsenic dose introduced into the emitter polysilicon film were chosen as the process variables. Process conditions chosen were: (a) high As dose with thin cap (HILO) and high As dose with 25% thick cap (HIHI), (b) 45% lower As dose with thin cap (LOLO) and 45% lower As dose with thick cap (LOHI). The influence of these two variables on key electrical parameters, such as, R_E, base-emitter turn on voltage (V_{BE}), current gain (β) and its temperature dependence, and f_T were characterized.

Table 1 summarizes the electrical characteristics of for a 0.2x6.4 μm^2 device with various process conditions. As expected, the HILO condition leads to increased I_C (lower V_{BE}), β, emitter-base capacitance (C_{BE}), indicative of a deeper EB junction. The advantage of lower R_E with higher As dose is obvious and is verified experimentally. A thicker cap is not only expected to lower the C_{BE} but also improve the V_{BE} variability within wafer due to the relative position of the EB depletion edge in the base region. We have found that the V_{BE} variability can be reduced as much as 3.5x by increasing the emitter cap. However, one pays the penalty of lower f_T (approximately 10 GHz between HILO and HIHI) for this tradeoff, potentially due to the increased emitter transit time (τ_e).

Figure 1 shows the Gummel characteristics for HIHI condition over temperature. Ideal behavior over wide bias and temperature range can be observed. In comparison to this condition, it is expected that a HILO condition will show a stronger temperature dependence of peak β primarily due to the deeper EB junction on the Ge ramp, as can be observed in Figure 2. We compare the AC behavior for all conditions in Figure 3. As expected, the reduction in C_{BE} with thicker cap layer improves the delay time at low-injection, but, the overall delay time is compromised. By using a HILO condition, one can obtain a 4% reduction in overall delay time due to improvements in R_E, β, and τ_b.

We have shown that the emitter-base profile design can be used as an optimization tool for high-performance SiGe HBTs.

Process	HILO	HIHI	LOHI	LOLO
V_{BE} at 10μA (mV)	692.2	705.7	705.3	701.3
R_E (Ohms)	1.27	1.67	2.05	2.3
β at Vbe=0.72V	355	254	273	309
C_{be} (fF/μm^2)	8.59	7.54	7.24	7.9
Peak-f_T (GHz)	131	120	121	128

Table 1. Key electrical parametric summary for various process conditions chosen.

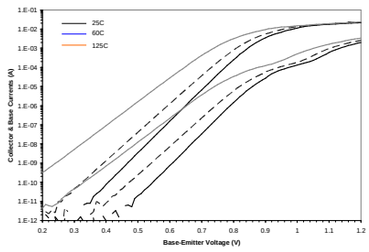

Figure 1. Gummel characteristics for HIHI condition at various temperatures. Ideal behavior is observed over several order magnitude in currents.

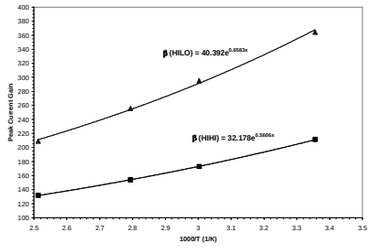

Figure 2. Temperature dependence of peak current gain for HILO and HIHI conditions. Stronger temperature dependence is observed for HILO condition primarily due to collector current variation.

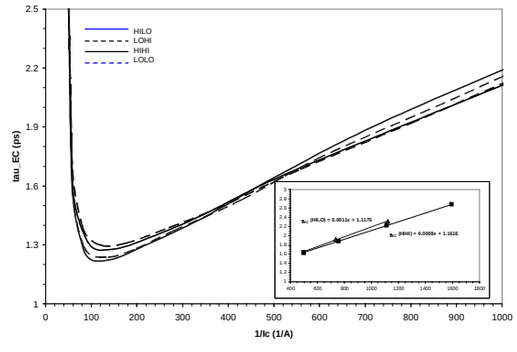

Figure 3. Collector-emitter delay shown as a function of 1/Ic for various process conditions. Inset shows that the HIHI improves C_{BE} by 18%.

References:

[1] G. Freeman et al., SiRF 2003, [2] B. Orner et al., BCTM 2003, [3] J. Rieh et al., IEDM 2002, [4] A. Joseph et al., BCTM 2001, [5] A. Joseph et al., ISTDM 2003