Enhanced 5V Complementary SiGe BiCMOS Technology by Separate NPN/PNP Emitter Formation

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Abstract

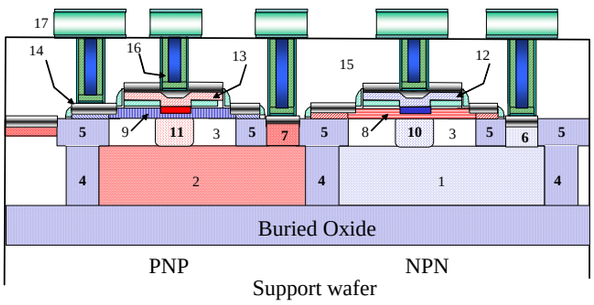
A method to enhance the PNP and NPN performance in a complementary 5V SiGe BiCMOS technology is described. By separately optimizing the base profiles and emitter interfaces, f_T of 27 GHz is obtained for both transistors while reducing the NPN noise and minimizing the impact on the remaining 5V parameters. Additional enhancements are the reduced thermal resistance by thinning down the SOI buried oxide thickness, the formation of a $CoSi_2$ Schottky-Barrier diode, and the reduction in the precision capacitor dielectric absorption.

Introduction

A complementary 5V SiGe BiCMOS process in production for high-speed analog applications was presented in [1]. In this technology, the base of the NPN and PNP are separately optimized but their emitter interfaces are formed simultaneously, limiting the flexibility in optimizing both transistors. The interface oxide (IFO) that is formed to improve the PNP gain increases the NPN gain, reducing BVceo. It also increases the NPN flicker noise. It was hence necessary to increase the NPN base boron concentration to reduce gain, however, at the cost of fT. This paper presents a method to separately form the NPN and PNP emitter interfaces, allowing the optimization of key parameters of both transistors. Other process enhancements are also described.

Process

The basic process is similar to that described in [1]. The major improvement is in the separate emitter process. Other enhancements are: a) thinner SOI buried oxide layer (BOX) to reduce thermal resistance and cost, b) reduced collector epitaxial thickness to further improve f_T, c) optimized base profiles, d) silicidation with $CoSi_2$ rather than $TiSi_2$ to form a Schottky Barrier Diode (SBD) e) reduced dielectric and interfaces trap density for precision capacitor. The completed bipolar transistors remain essentially the same as in [1] (Fig. 1).



1: N-buried layer; 2: P-buried layer; 3: Collector epitaxy 4: Deep trench; 5: STI; 6: NPN sinker; 7: PNP sinker; 8: NPN base; 9: PNP base; 10: NPN SIC; 11: PNP SIC; 12: NEMIT POLY; 13: PEMIT POLY; 14: $CoSi_2$; 15: BPSG; 16: Contact; 17: 1st metal (2nd-4th metal not shown).

Fig.1: Schematic of NPN and PNP transistors

The fabrication of CMOS and passive components is detailed in [1].

Starting material

The starting wafer is SOI, as described in [1]. The BOX thickness is, however, thinned-down from 0.4 μm to 0.145 μm to reduce thermal resistance and self-heating, particularly during operation at maximum power. The choice of BOX thickness is a trade-off between thermal resistance, maximum applied voltage, parasitic capacitance between collector and support wafer, and cost. Reducing the BOX thickness increases parasitic capacitance. This increase is particularly significant in PNP structures because of the accumulating applied voltage and workfunction difference between collector and p-type support wafer. The support wafer resistivity is increased to reduce the impact of thinner BOX on parasitic capacitance and also to improve the quality factor of passive components. The latter is especially important to RF applications.

Collector epitaxy

The minimum collector epitaxy thickness is primarily limited by the buried-layer up-diffusion, the SIC and base profiles, and their impact on transistor breakdown. Tighter control of the epitaxial film allowed the reduction of its nominal thickness, improving fT by 1-2 GHz while maintaining the minimum transistor breakdown of 5.5 V.

Base profiles

Separating the NPN and PNP emitter loops, increases the flexibility in optimizing both transistors. The NPN IFO thickness is considerably reduced from [1], eliminating the strong increase in gain and the necessity to increase the base Gummel number to compensate for this increase. The NPN base "dose" was hence reduced from [1] to re-establish the target gain. The PNP IFO process is kept essentially unchanged. The transistor gain is primarily determined by the IFO thickness, the Ge concentration at the emitter-base junction [2], and the base Gummel number. The Early voltage (V_A) is strongly impacted by the ratio of Ge concentration at the collector-base junction to that at the emitter-base junction [3,4]. By reducing the NPN emitter IFO and base "dose", the base-width is reduced and the electron mobility is increased. The Ge profile is re-adjusted to the new base boron profile.

The PNP IFO process is kept essentially unchanged from [1]. A tighter control of emitter patterning and "undercut" allows the reduction of base concentration at the surface, resulting in a narrower base. The Ge profile is re-adjusted to the new base arsenic profile.

Silicidation

The silicide is changed from $TiSi_2$ in [1] to $CoSi_2$, primarily to form a Schottky-Barrier Diode (SBD), but also to improve the continuity of narrow, silicided polysilicon lines. The SBD is formed between cobalt-silicide and CMOS NWELL. The barrier height of $CoSi_2$ over NWELL is approximately 80 meV higher than $TiSi_2$, making it more suitable for specific applications. The SBD series resistance is reduced by placing the NPN collector sinker and N-buried layer (NBL), and the CMOS source/drain in the cathode path.

The precision capacitor is formed between TiN and silicide, as in [1]. The deposition conditions of oxide dielectric and its interfaces with TiN and $CoSi_2$ are modified to reduce the trap density within the dielectric and its interfaces, reducing transient shifts in capacitance. This effect is also known as "dielectric absorption" [5].

Separate emitter formation

The separate emitter modules begin with a stack of insulators into which NPN emitter windows are patterned over the base. A very thin IFO is formed followed by depositing, implanting and patterning the NPN emitter polysilicon (Fig. 2).

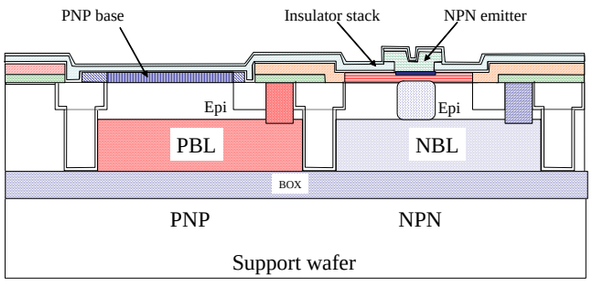


Fig.2: NPN emitter patterning, insulator deposition

One of the critical steps is the formation of PNP emitters with patterned NPN emitters in place. Another stack of insulators that act as etch-stops is first deposited into which the PNP emitter windows are patterned. A special PNP IFO is formed followed by depositing, implanting and patterning the PNP emitter polysilicon (Fig. 3).

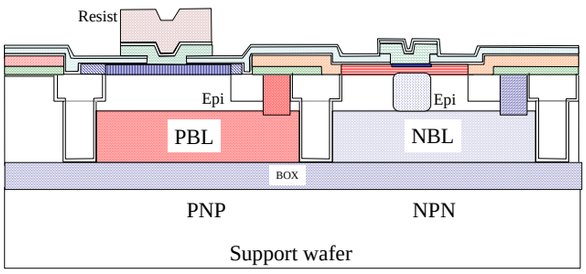


Fig.3: PNP emitter patterning with NPN in place

Results

With the new process scheme, considerable improvements in bipolar performance and noise are achieved. In addition, the thermal resistance is appreciably reduced, a Schottky-Barrier Diode with satisfactory parameters is obtained, and transient shifts in the precision capacitor are suppressed. CMOS and precision resistors are unchanged from [1].

Bipolars

Key bipolar results are given in Table I. NPN and PNP f_T plots are shown in Figs. 4, 5. For both transistors, the nominal f_T is increased from [1] by 8-10 GHz, while the limits on transistor gain, breakdown, and Early voltage are maintained. The main contributor to the increase in f_T is the reduced base dose and width in the new process flow.

The reduction in NPN IFO thickness considerably reduces noise, as shown in Fig. 6. The noise is reduced from [1] by approximately one order of magnitude. Characterizing and modeling the dependence of noise on IFO thickness is being pursued in a joint effort with [6].

Table I: Nominal NPN, PNP characteristics (25 °C)

Parameter	Unit	NPN	PNP
β		200	140
V_A	V	95	200
BV_{CEO}	V	6.4	5.9
f_{Tmax} (V_{CE}=5V)	GHz	27	27

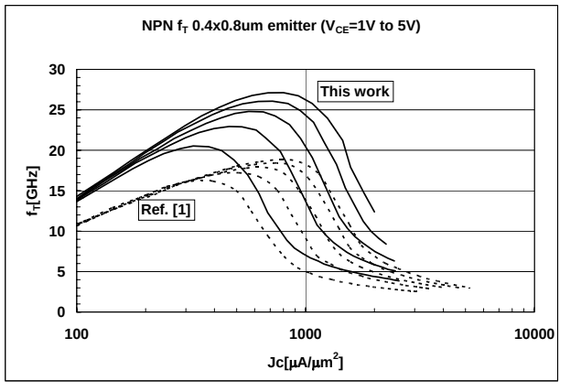


Fig. 4 NPN fT for Vce = 1-5V. AE = 0.4x0.8 μm^2

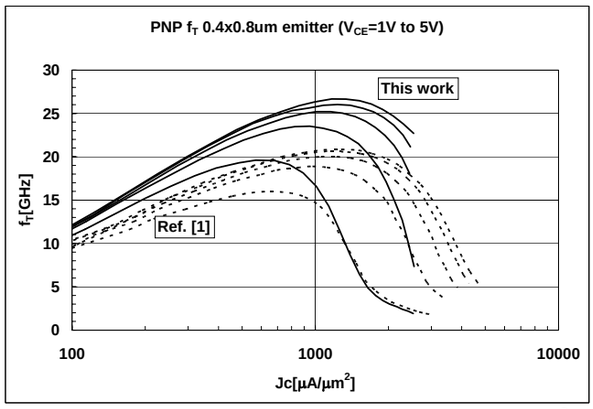


Fig. 5 PNP fT for Vce = -1 to -5V. AE = 0.4x0.8 μm^2

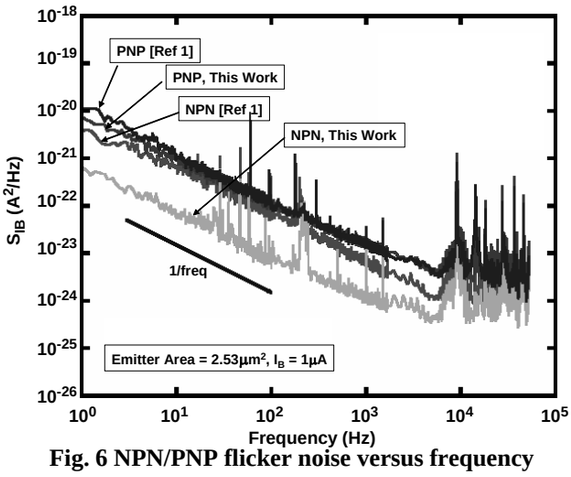


Fig. 6 NPN/PNP flicker noise versus frequency

Thermal resistance

Fig. 7 illustrates the bipolar structure indicating major heat dissipation paths. Because the thermal conductance is considerably lower in silicon dioxide than in single-crystal silicon (0.014 W/cm-K in SiO_2 versus 1.47 W/cm-K in Si), the effective thermal resistance is strongly affected by the BOX thickness. The insulator film compositions above the structure limit the heat dissipation upward and toward bond-pads. Lateral heat dissipation is limited by the effective deep trench thickness and sidewall area, and balanced by heat transfer from adjacent structures.

A simplified analytical spreading resistance model is developed to approximate the effective thermal resistance for DC conditions. The assumption is made that most of the heat dissipation occurs toward the support wafer of infinite dimensions compared to the size of the structure. The model predicts a reduction in thermal resistance by approximately 50%. More accurate 2D simulations place this value to 30-40%. This analysis is being pursued by [7].

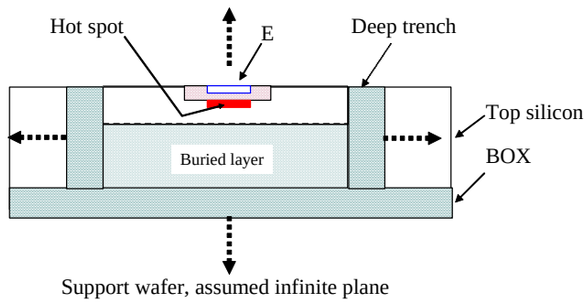


Fig. 7 Illustration of bipolar heat dissipation paths

The impact of reduced BOX thickness on self-heating is experimentally observed by tracing the base-emitter forward voltage as a function of collector reverse voltage for a fixed base current (Fig. 8). The drop of V_{be} with increased power dissipation is a measure of self-heating. An appreciable reduction in self-heating is found when the BOX thickness is reduced from 0.4 µm to 0.145 µm.

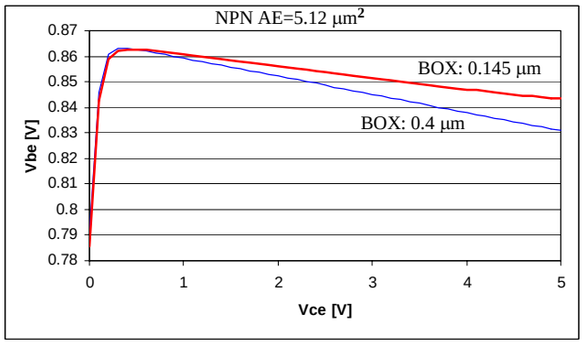


Fig. 8 V_{be} versus V_{ce} at constant I_B illustrating self-heat

Thermal resistance and self-heating are also important considerations for CMOS, passive components and temperature increase in adjacent structures.

Schottky-Barrier Diode

Table II summarizes key SBD parameters for an "unguarded" structure. The reverse leakage is typically reduced by placing a PMOS source/drain guard ring around the structure to reduce edge-field effects.

Table II: Key SBD parameters (25 °C)

Barrier height, ϕ	0.60	eV
Ideality factor	1.20	
Capacitance at 0 V reverse	2.0	fF/µm²
Reverse leakage at 3V	250	nA/µm²

Precision capacitor

Key capacitor parameters are given in Table III. One important property of precision capacitors is the transient drift caused by traps within the dielectric and at its interfaces. This effect is also known as "dielectric absorption" and manifests itself as a partial recovery of voltage across the capacitor when the terminals are instantaneously shorted. This drift causes errors in analog applications that are based on charging and discharging capacitors, such as sample-and-hold circuits [5]. The new process scheme reduces dielectric absorption from about 2500 ppm in [1] to < 100 ppm.

Table III: Key capacitor parameters (25 °C)

Capacitance per unit area	0.70	fF/µm²
Capacitance to support wafer	0.04	fF/µm²
Capacitance to body, fringe	0.04	fF/µm
Voltage coef, VCC linear 1 MHz	-4	ppm/V
Voltage coef, VCC quad 1 MHz	0.6	ppm/V²
Linear TCC	+10	ppm/°C
Quadratic TCC	0.03	ppm/°C²
Dielectric BV at 0.1 nA/µm²	> 40	V
Dielectric absorption, κ	< 100	ppm

Summary

By separately forming the NPN and PNP emitter interfaces and optimizing the base profiles in a complementary 5V SiGe BiCMOS process, a nominal fT of 27 GHz is achieved for both transistors. The NPN noise is reduced by one order of magnitude. In addition, thinning down the SOI BOX thickness reduces the thermal resistance and self-heating, further improving bipolar parameters. Finally, the reduction in dielectric trap density in precision capacitors and the formation of a $CoSi_2$ Schottky-Barrier extend the applicability of the process. Further enhancements are in progress to extend the technology to RF applications.

Acknowledgements

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References

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