Strained Ge MOSFET technology

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Strained Ge (ϵ-Ge) on relaxed $Si_{1-x}Ge_x$ possesses extremely high hole mobility[1] and can be used as a channel material for high-performance p-MOSFETs. In one configuration, referred to as a dual-channel heterostructure, the ϵ-Ge channel is epitaxially capped with strained Si (ϵ-Si) in order to allow the use of an SiO_2 gate dielectric. In an alternate configuration, a high-κ gate dielectric is deposited directly onto the ϵ-Ge, allowing surface-channel operation. We earlier reported on the optimization of dual-channel ϵ-Ge p-MOSFETs, demonstrating hole mobility enhancements over bulk Si as high as 10 times (Fig.1).[2,3] More recently, we reported surface-channel ϵ-Ge p-MOSFETs with an HfO_2/TaN gate stack exhibiting a 2× mobility enhancement over similarly processed bulk Si devices (Fig. 2).[4] In this paper, we review the current progress in both dual-channel and surface-channel ϵ-Ge p-MOSFETs. Some results on the integration of n-MOSFETs will also be presented.

Dual-channel heterostructures, where ϵ-Ge (or a Ge-rich SiGe alloy) is capped with Si, may be thought of as an extension to strained silicon technology. One of the motivations for exploring such structures was the relatively modest hole mobility enhancements typically observed in ϵ-Si p-MOSFETs.[5] In dual-channel heterostructures, the ϵ-Si surface layer allows the formation of a high-quality interface with a standard SiO_2 gate dielectric and can also serve as a high-mobility electron channel at the surface (type-II offset). The buried Ge layer forms a well for holes (type-I offset), and the compressive strain imparts a lower effective mass, in addition to splitting the valence band degeneracy. Since three heterogeneous materials (i.e. ϵ-Si, ϵ-Ge, and $Si_{1-x}Ge_x$) under different states of strain (tensile, compressive, and relaxed, respectively) coexist near the surface, the carrier mobilities can be drastically influenced by varying the layer thicknesses and in-plane lattice constant. In order to understand and optimize mobility in these material stacks, we fabricated MOSFETs on a wide variety of ϵ-Si/ϵ-Ge/$Si_{1-x}Ge_x$ heterostructures and measured their effective mobilities. We will present the key parameters for attaining high hole mobilities, as well as the techniques we have developed for the epitaxial growth of these heterostructures.

For surface-channel ϵ-Ge p-MOSFETs, the gate dielectric is formed on the ϵ-Ge layer itself. Following RTP nitridation in ammonia, a 5 nm HfO_2 layer is deposited by RT-CVD. The nitridation process forms a thin (~0.7 nm) Ge oxynitride layer, which was earlier shown to be necessary for attaining good C-V characteristics,[6] and the equivalent electrical oxide thickness (EOT) of the entire stack was found to be 1.6 nm. Compared to bulk Ge devices processed under similar conditions, the ϵ-Ge devices exhibited a 35% mobility enhancement. With further optimization, it is expected that considerably higher mobilities can be attained.

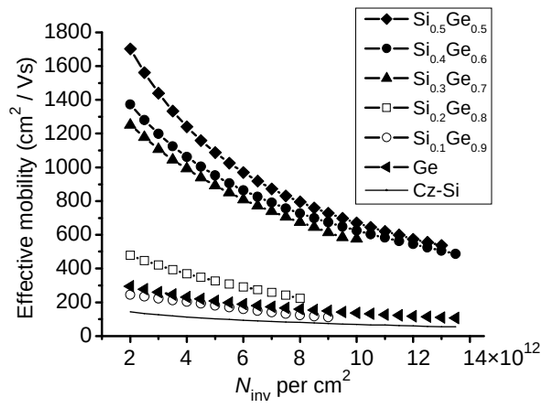

Fig. 1 Hole effective mobility vs N_{inv} of ϵ-Si/ϵ-Ge dual-channel heterostructures grown on $Si_{1-x}Ge_x$ with x = 0.5-1.0

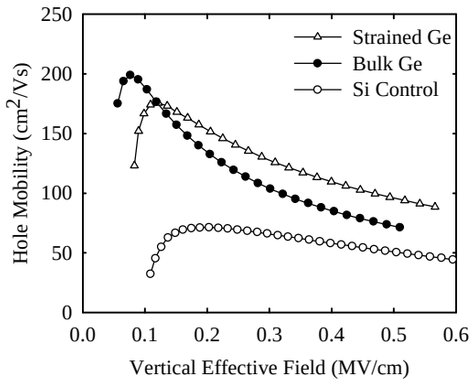

Fig. 2 Comparison of extracted mobility for surface-channel strained Ge, bulk Ge, and silicon control devices with HfO_2/TaN gate stacks. At high effective field, the strained Ge devices show a 35% increase in mobility compared to the bulk Ge devices.

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