Extraction of band offsets in Strained Si/Strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$ dual-channel enhanced mobility structures

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A dual-channel structure consisting of a thin (~3 nm) strained Si layer on strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$ (Fig. 1) has been shown to offer large enhancements in both electron and hole mobilities in a single epitaxial layer stack [1,2]. Mobility enhancements as large as 1.8x and 10x have been measured in n- and p-MOSFETs respectively [3]. It is essential to know the band structure in order to accurately model these devices. In particular the valence band offset, ΔE_V, between the strained Si and strained $Si_{1-y}Ge_y$ layers (Fig. 1) determines the degree of hole confinement in the $Si_{1-y}Ge_y$ layer. The positions of the conduction band edge in the strained Si and the valence band edge in the strained $Si_{1-y}Ge_y$ significantly impact the effective bandgap of the structure and can be used to tune the threshold voltage of both n- and p-MOSFETs for use with a single workfunction metal gate [4]. Theoretical predications of these band parameters are uncertain by ±100 meV [5,6]. In this work, for the first time, we extract these critical band parameters over a wide range of Ge composition and strain, using a combination of experiment and modeling. It is also shown that the appropriate density of states for the strained layers must be used in order to accurately model the capacitance-voltage (C-V) behavior.

Epitaxial layers were grown in an Applied Materials "Epi-Centura" system. The layer structure is illustrated in Fig. 1. High frequency C-V was measured and compared to simulations taking into account quantum corrections using the density gradient model in Dessis [7]. The valence band offset, ΔE_V was extracted from the analysis. As the bias is swept negative, hole accumulation occurs first in the strained $Si_{1-y}Ge_y$ layer. A plateau forms in the C-V curve, which is very sensitive to ΔE_V (Fig. 2).

The effective valence band density of states N_V decreases with strain and increasing Ge content [8]. N_V values calculated by the nonlocal empirical pseudopotential method from full-band Monte Carlo simulations [9] were used in the Dessis C-V simulations. Fig. 3 illustrates the improved C-V fitting obtained when the appropriate values are used for N_V in the strained Si and strained SiGe, and the impact on extracted oxide thickness and ΔE_V. Fig. 4 compares values of extracted ΔE_V for a more well studied structure, strained SiGe on relaxed Si. Using the full-band strained N_V values we obtain a slope of 101 meV/10% Ge for ΔE_V, and a corresponding value of 87 meV/10% Ge when the relaxed Si value is used for N_V. For strained Si on strained $Si_{1-y}Ge_y$, ΔE_V increases with both y and strain (Fig. 5). The sensitivity of V_t and subthreshold slope to both ΔE_V and N_V demonstrate the importance of using appropriate values for accurate modeling of these structures (Fig. 6).

In summary, MOS C-V analysis has been used to extract critical band parameters for strained Si/strained SiGe dual-channel structures. These parameters are essential for modeling such high mobility structures.

References:

[1] Leitz et al, *Appl. Phys. Lett*. 2001.
[2] Jung et al, *EDL*, 2003.
[3] Lee et al, *IEDM*, 2003.
[4] S. Yu et al, submitted to *EDL*.
[5] People, *J. Quant. Electronics*, 1986.
[6] Schaffler, *Semicond Sci. Technol.*, 1997.
[7] Ancona et al, *Phys. Rev.B,* 1989.
[8] Manku et al, *J. Appl. Phys.*, 1991.
[9] Rieger et al, *Phys. Rev.B,* 1993.
[10] Lang et al, *Appl. Phys. Lett*. 1985.
[11] King et al, *Trans. Electron Devices*, 1989.

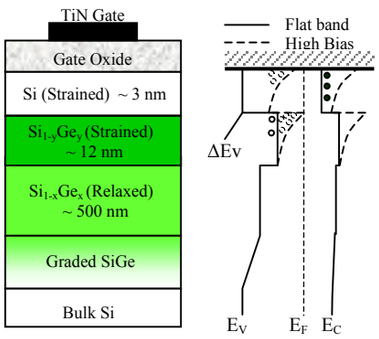


Fig. 1 Structure and band diagram for strained Si on strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$ (x<y) dual channel p-MOSFET. P-type doping used for capacitor structures.

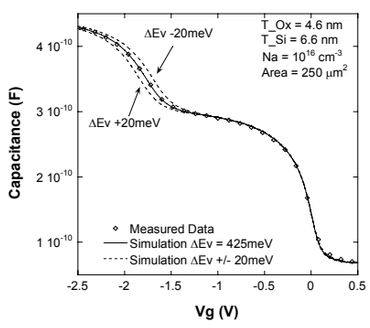
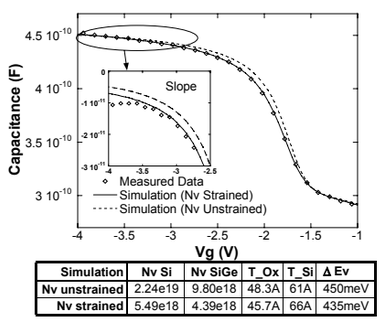


Fig. 2 ΔE_V extraction and sensitivity for strained Si, strained $Si_{0.4}Ge_{0.6}$ on a relaxed $Si_{0.7}Ge_{0.3}$ substrate. Measured data with simulation of ΔE_V =435meV ± 20meV.



Simulation	Nv Si	Nv SiGe	T_Ox	T_Si	Δ Ev
Nv unstrained	2.24e19	9.80e18	48.3A	61A	450meV
Nv strained	5.49e18	4.39e18	45.7A	66A	435meV

Fig. 3 Impact of N_V value on fitting of simulation to experimental results. Same structure as for Fig.2.

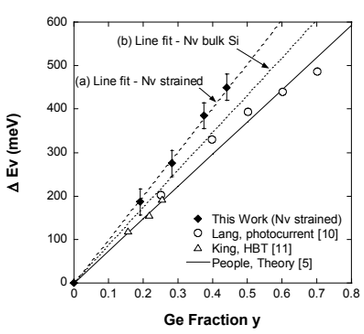


Fig. 4 ΔE_V for strained $Si_{1-y}Ge_y$ on unstrained Si. N_V values used for line fit (a) N_V (Strained $Si_{1-y}Ge_y$), and (b) N_V (Unstrained Si).

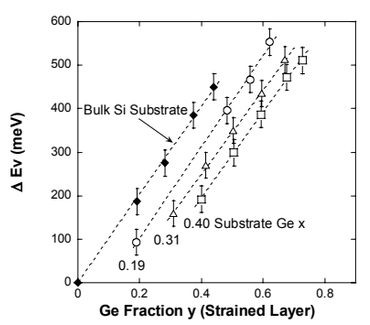


Fig. 5 Extracted ΔE_V for strained Si on strained $Si_{1-y}Ge_y$ on various relaxed $Si_{1-x}Ge_x$ substrates. Line fit gives slope of 105, 97, 99 meV/10%Ge in the strained $Si_{1-y}Ge_y$ for x of 0.19, 0.31 and 0.40 respectively.

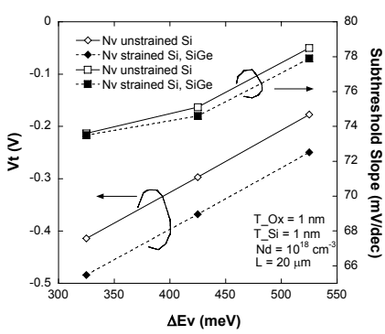


Fig. 6 Simulated V_t and subthreshold slope versus ΔE_V for dual channel p-MOSFET on relaxed $Si_{0.7}Ge_{0.3}$ substrate with N_V for unstrained Si and strained Si, $Si_{1-y}Ge_y$.