Anomalous behaviour of buried strained-Si channel Heterojunction FETs at low temperatures

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Low temperature behavior of strained-Si MOSFETs [1] and HFETs [2] generate an invaluable source of information on the physical processes, in particular confinement and scattering, in these devices. It has been shown for both Si MOSFETs [3] and strained-Si FETs [1,2] that reduced temperature increases the performance parameters, mainly due to increased carrier mobility. In this abstract we present the reduced temperature performance of strained-Si buried channel HFETs and discuss the physical principles behind the anomalous behavior.

Fig.1 give the layer structure of the Schottky gated HFET. The gate lengths of the devices are L_G = 100, 150, 250 and 500 nm. The total source-drain distance is fixed at L_{SD} = 2 µm. The gate width is W = 15 µm for all.

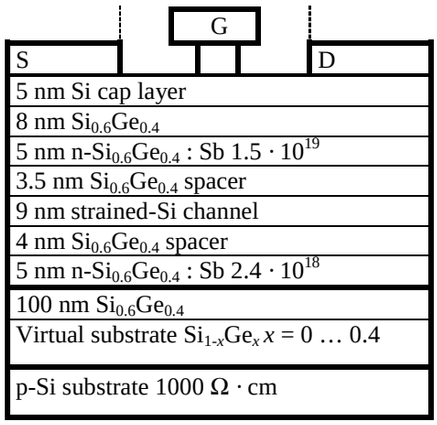

Fig.1: Cross-section of Schottky gated HFET.

An Agilent 4155B Semiconductor Parameter Analyzer and a CTI-Cryogenics closed-cycle He cryostat (10 – 300K) is used for the measurements.

The room temperature maximum low-field transconductance, g_{mmax} increases up to 61% at T = 10 K. A record value of 440mS/dec at only 0.35V V_{DS} is reached at 10K for the 100nm HFET. The sub-threshold slopes of all studied devices decrease to 14…19 mV/decade at T = 10 K, but remains higher than the theoretical curve. This is a feature apparent in all studied n-channel strained-Si FETs [1,2].

At T<40K the I_{DS}-V_{DS} characteristics in the triode region become highly non-linear. Since the ohmic contact implantations are degenerate, but the annealing temperature kept low, a small Schottky barrier exists at the source and drain contact, that is completely negligible in comparison with kT/q at room temperature, but becomes important at low T. This increases the switch-on voltage and decreases the switching speed, but since g_{mmax} lies at higher V_{DS} (in the triode region) where no Schottky behavior occurs, low power analogue performance is not impeded.

The substrate current is virtually independent of V_{GS} and L_G. Its temperature dependence is accurately described by $I_{SUB}^{T} = I_{SUB}^{0} \exp\left(-\frac{E(=0.71eV)}{2kT}\right)$, in qualitative agreement with the bandgap of SiGe.

Low temperature operation of the HFETs has already shown double peaked g_m curves as a function of gate voltage [4](fig.2), associated to parallel conductance.

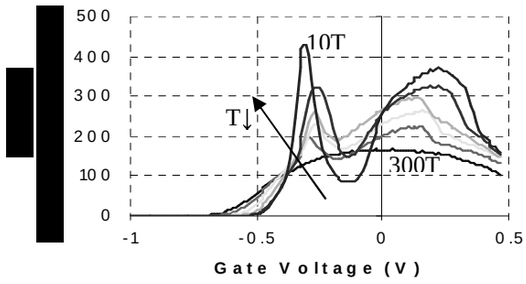

Fig.2: Anomalous behaviour of the HFET at low T, low V_{GS} and here demonstrated at V_{DS}=1V. (ΔT=60K)

Although simulations confirm this anomaly to first approximation, they cannot predict the relative sharpness of the peaks. We have found that the origin of the anomalous peak is due to self-biasing effects of the HFETs at reduced temperatures.

When measuring the HFET at low V_{GS} and low T, a kink effect in the current is observed as given in fig.3.

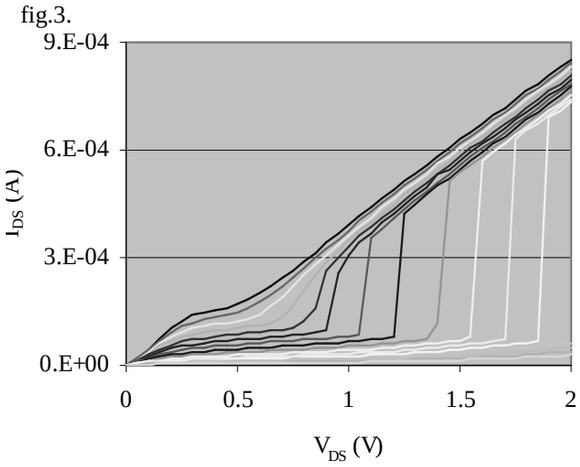

Fig.3: The kink effect measured in the I_{DS}-V_{DS} curves at 10K, L_G=0.5µm, V_{GS}=-0.45 → -0.3V, step: 0.01V.

The kink effect is explained by the fact that the high resistivity substrate becomes insulating, and becomes effectively self-biased. Impact ionization near the drain creates an excess current of electrons (to drain) and holes, which go partly to the substrate. This hole current biases the substrate at a positive voltage with respect to the source and causes a shift in threshold voltage, such that the device switches on [5]. Calculating g_m across the abrupt current steps, generates sharp peaks as those occurring in fig.2 at low V_{GS}. The higher lying g_m peak in fig.2 is the traditional one found in HEMT structures.

In conclusion, we have found dramatically improved low voltage behavior in HFETs at low temperatures. We have demonstrated that the double peaked transconductance curves of these devices at low temperature are a result of substrate self-biasing effects at low temperatures.

References:

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