

Titanium dioxide gate dielectric for strained-germanium heterolayers

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As the CMOS device downscaling reaches its fundamental limits, alternative techniques for device performance enhancement must be developed. Channel engineering using high-mobility Ge seems to be a potential option to improve the performance of the CMOS devices. Enhancements in carrier mobilities have been observed in Si/SiGe heterostructures leading to a number of novel device structures [1]. In this work, we report on the low temperature deposition of TiO₂ on strained-Ge layer and the electrical properties of the deposited films by using a metal-insulator-semiconductor (MIS) structure. The starting substrate was n-type Si (100) with resistivity 10-20 Ω-cm. Relaxed graded Si_{1-x}Ge_x buffers (x = 0.6) were then deposited by UHV compatible low pressure chemical vapor deposition using silane (SiH₄) and germane (GeH₄). Next, strained-Ge layers were deposited at 800°C (pressure ~ 0.092-0.150 Torr) and the total film thickness was 1-1.2 μm. Thin films of TiO₂ (high-k gate dielectric) were deposited at a low temperature (150°C) by plasma enhanced chemical vapor deposition (PECVD) using titanium tetrakis isopropoxide (TTIP), [Ti(OC₃H₇)₄] as an organometallic precursor. The thickness of the TiO₂ film was found to be ~140Å (EOT~33.4Å).

A TEM micrograph (Fig. 1) shows the complete heterostructure of strained-Ge layer. Fig. 2 shows that the Raman peaks are present at 290 cm⁻¹ and 400 cm⁻¹ and 465 cm⁻¹ wave numbers due to Ge-Ge, Si-Ge and Si-Si bonds, respectively. The high frequency (1 MHz) C-V and G-V characteristics of as-deposited TiO₂ films on strained-Si layer are shown in Fig. 3. The interface trap density (D_{it}) at midgap and fixed oxide charge density (Q_{f/q}) was calculated using Hill's single frequency approximation method [2]. The extracted values of D_{it} and Q_{f/q} are 5.14×10¹¹ eV⁻¹cm⁻² and 1.46×10¹² cm⁻² respectively. Fig. 4 shows the high frequency (400 kHz) C-V characteristics of the as-deposited sample before and after constant current stressing (2mA/cm²). It is observed that the C-V curves shift towards the negative voltage direction after stressing. This indicates the generation of positive charges in the dielectric. Fig. 5 shows the I-V characteristics before and after constant current stressing of 2mA/cm² for 100s and 325s. It is evident that there is no significant stress induced leakage current (SILC) in the sample, indicating no serious trap is generated by current stress. To obtain charge trapping behavior, the changes in gate voltage (ΔV_g) need to be studied. The changes in the gate voltage to maintain a constant current (2mA/cm²) injected through gate was studied. Positive gate voltage shift (Fig. 6) confirms that as-deposited sample exhibits electron trapping. In conclusion, electrical properties of TiO₂ films have been investigated. The stress induced leakage current is negligible, indicating a good reliability property of the deposited TiO₂ films on strained-Ge films.

[1] C. K. Maiti and G. A. Armstrong, "Applications of silicon-germanium heterostructure devices," Inst. of Physics Pub, UK, 2001.

[2] W. A. Hill and C. C. Coleman, Solid-State Electron., 23, pp. 987-93, 1980.

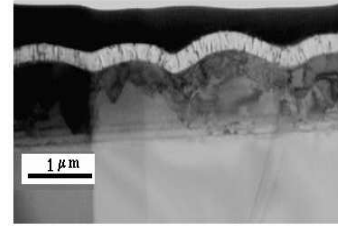


Fig. 1 Cross-sectional TEM image of strained-Ge layer.

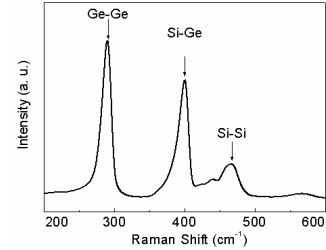


Fig. 2 Raman spectra of strained-Ge layer.

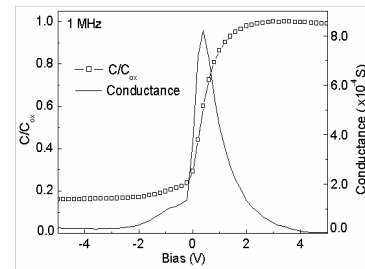


Fig. 3 High frequency (1MHz) C-V and G-V characteristics of as-deposited TiO₂ films on strained-Ge layer.

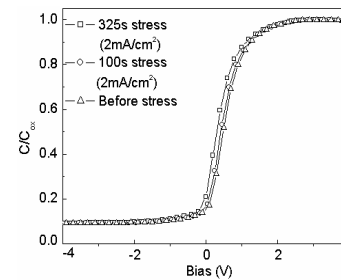


Fig. 4 C-V characteristics before and after constant current stressing (2mA/cm²).

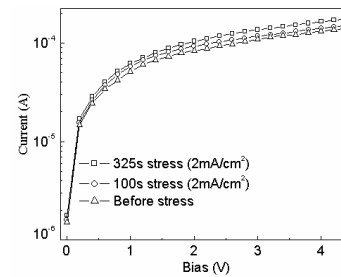


Fig. 5 I-V characteristics of TiO₂ films under constant current (2mA/cm²) stressing.

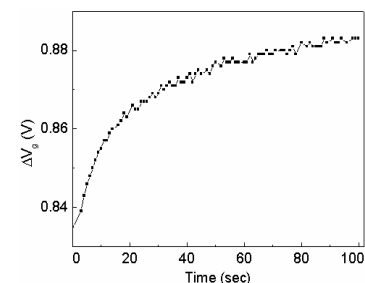


Fig. 6 Gate voltage shift vs. stress time for TiO₂ films on strained-Si layer under constant current stressing.