Abs. 1322, 206th Meeting, © 2004 The Electrochemical Society, Inc.

"Tri-layer heterostructure for improved PMOS enhancements preserved over a large processing temperature range"

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Hole mobility enhancements in P-type MOSFETs processed on strained Si heterostructures are typically small and dependent on the strain and the gate overdrive. These mobility enhancements reduce to zero at very high gate overdrives. A compressively strained $Si_{1-y}Ge_y$ layer on top of a relaxed $Si_{1-x}Ge_x$ layer (y>x) provides a high mobility channel for the holes. A Si capping layer on top of the compressively strained $Si_{1-y}Ge_y$ layer provides compatibility with conventional CMOS processing and a high quality interface with a standard SiO_2 gate dielectric. This structure, known as a dual channel heterostructure, provides a platform for fabricating both P-type and N-type MOSFETs, with very high hole and electron mobility enhancements over CZ-Si.

The hole mobility enhancements obtained on dual channel heterostructures are very dependent on the Ge concentration of the compressively strained $Si_{1-y}Ge_y$ layer and the relaxed $Si_{1-x}Ge_x$ layer. Out-diffusion of Ge from the compressively strained $Si_{1-y}Ge_y$ layer into the relaxed $Si_{1-x}Ge_x$ layer and the top Si cap reduces the Ge concentration in the compressively strained layer. This out-diffusion can occur during high temperature steps of the MOSFET processing such as gate oxidation or S/D activation. The reduction in the Ge concentration, and hence the strain in the compressively strained layer, leads to reduced hole mobilities.

It has earlier been observed that the diffusion coefficient for Ge interdiffusion in SiGe single crystals increases with increasing Ge concentration. The higher hole mobility structures have higher Ge concentration in the layers, and thus, are more susceptible to such out-diffusion. A tri-channel heterostructure is presented in which a tensilely strained Si layer is present below the compressively strained $Si_{1-y}Ge_y$ layer, which in turn is capped by a tensilely strained Si layer for SiO_2 compatibility. The underlying strained Si layer helps in reducing the Ge out-diffusion from the compressively strained layer during the high temperature processing steps. The hole mobility enhancements in the tri-channel heterostructures, are thus retained even after high temperature processing. The presence of an underlying strained Si layer also prevents the hole wavefunction from tunneling into the low mobility relaxed $Si_{1-x}Ge_x$ layer. Better confinement of the hole wavefunction in the high mobility compressively strained $Si_{1-y}Ge_y$ layer could be beneficial for the hole mobility.

Results for the hole mobility characteristics of tri-channel heterostructures will be compared with that of similar dual channel heterostructures without the underlying Si layer. A mathematical model for estimating the Ge out-diffusion in the strained dual channel and tri-layer heterostructures will also be presented. This model takes into account strain evolution of the layers due to interdiffusion as well as change in activation energy of diffusion because of strain. Some simulation results using the model will be compared against the experimentally observed concentration profiles.

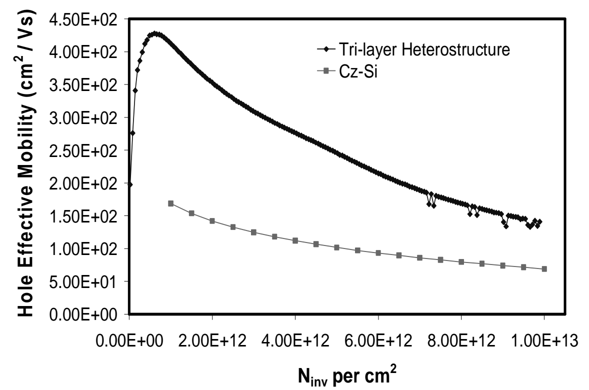

Figure 1 - Hole effective mobility vs N_{inv} obtained from a PMOS fabricated on a ε-Si|ε-$Si_{0.5}Ge_{0.5}$ |ε-Si structure grown on relaxed $Si_{0.80}Ge_{0.20}$.

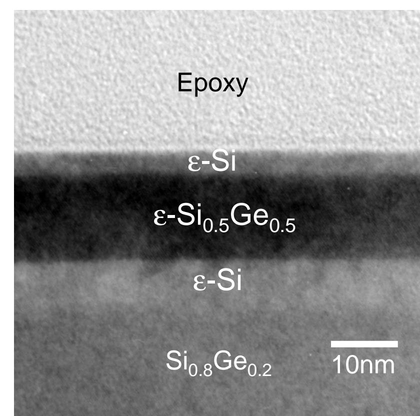

Figure 2 – Cross-Sectional TEM image of the tri-layer heterostructure.