SiGe MODFETs: Overview and issues for sub-100 nm gate-length scaling

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Introduction. SiGe MODFETs are attractive devices for future rf and mixed-signal communications applications, due to their greatly enhanced mobility compared to Si MOSFETs. However, MODFETs have been slow to keep pace with the tremendous advances in scaling technology that have allowed Si MOSFETs to maintain performance leadership, both for digital and analog applications. In order to fulfill their promise for enhanced performance, MODFETs must also be aggressively scaled, both laterally and vertically (1). In this paper, I will give an overview of SiGe MODFET technology and describe the materials issues for the future scalability of these devices.

MODFET overview. Tensile-strained Si on relaxed SiGe n-MODFETs produce electron mobilities about 4x higher than Si/SiO_2 inversion layers at a given carrier density, while compressive-strained $Si_{0.2}Ge_{0.8}$-channel (Ge-channel) p-MODFETs have mobility enhancements of ~ 6 (10). Recent demonstrations by IBM include 100 nm gate-length Ge-channel p-MODFETs with trans-conductance, g_m, of 488 mS/mm (2), and $Si_{0.2}Ge_{0.8}$-channel p-MODFETs with g_m = 377 mS/mm and f_{max} = 116 GHz (3). More recently, we have fabricated laterally-scaled Si/ $Si_{0.7}Ge_{0.3}$ n-MODFETs with L_g = 80 nm and source-to-drain spacing of only 300 nm. These devices have record f_{max} of 210 GHz (4), as shown in Fig. 1. However, gate-length scaling below 80 nm results in reduced voltage gain and higher off-state leakage current, indicating the need for improved scalability.

Challenges for MODFET scaling. Numerical simulations of scaled MODFET geometries indicate that quantum well depths ≤ 10 nm, as well as p-well doping and a buried insulator layer are necessary for effective scaling below L_g = 50 nm. For vertical scaling, we have developed a low-temperature UHV-CVD growth process to increase the transient incorporation rate of phosphorous in the supply layer (5). Using this process, $Si/Si_{0.7}Ge_{0.3}$ layer structures have been grown with quantum well depths of 10 nm and electron mobility and sheet density of 1800 cm^2/Vs and 2.1 x 10^{12} cm^{-2}, respectively. For p-well doping, implantation through the quantum well cannot be used as it results in dopant incorporation within the channel that can degrade the mobility. Therefore, we have developed a process where the SiGe buffer layer is implanted with boron, and then the n-MODFET layer structure is regrown on top. As shown in Fig. 2., devices using this improved design have reduced output conductance and off-state leakage compared to devices with no p-well doping (6). We have also demonstrated the growth of MODFET layers structures on thin SGOI substrates. One such layer structure, shown in Fig. 3, has total thickness of only 74 nm, while maintaining room temperature mobility of 1700 cm^2/Vs.

Acknowledgement. This work was supported by DARPA under SPAWAR contract N66001-00-C-8086.

References

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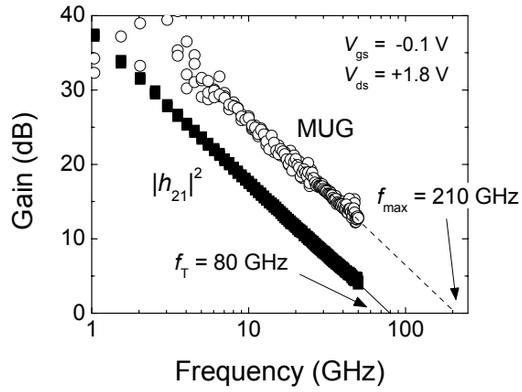

Fig. 1. Plot of $|h_{21}|^2$ and MUG vs. frequency for a $Si/Si_{0.7}Ge_{0.3}$ n-MODFET with f_T = 80 GHz and f_{max} = 210 GHz. The device has L_g = 80 nm, and L_{ds} = 300 nm and a total gate width of 20 μm.

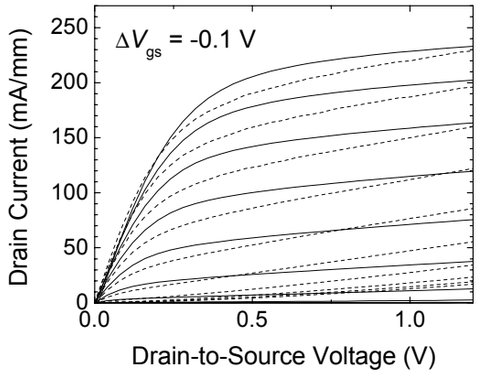

Fig. 2. Output characteristics for $Si/Si_{0.7}Ge_{0.3}$ n-MODFETs with (lines) and without (dashes) p-well doping. Both devices have L_g = 150 nm and L_{ds} = 300 nm. The MODFETs with p-well doping have 2x lower output conductance, and improved pinch off.

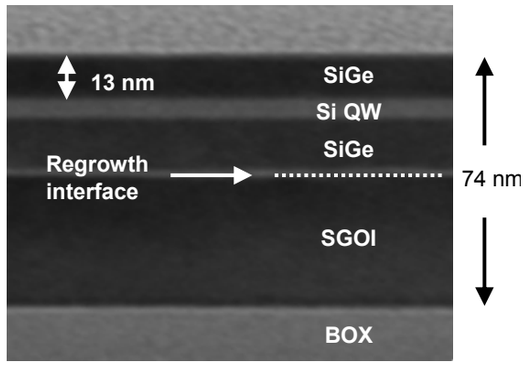

Fig. 3. Cross-sectional TEM micrograph of a $Si/Si_{0.7}Ge_{0.3}$ layer structure grown on a thin SGOI substrate. The initial and final SGOI thicknesses are 38 nm and 74 nm, respectively.