Ge Diffusion Effect on Low Frequency Noise in Ultra-thin Strained-SOI CMOS

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Due to high mobility, strained-Si MOSFETs are expected to be applied to RF analogue applications. There are, however, few investigations concerning noise in strained-Si MOSFETs, though low frequency noise characteristics are key issue in those applications. Recently, low frequency noise characteristics in strained-Si n-MOSFETs have been reported (1), where the low-frequency noise has been discussed from the viewpoint of dislocation and Ge diffusion, which must be suppressed because of mobility degradation (2). However, the relationship of Ge diffusion or dislocation to the low-frequency noise is still unclear. In this paper, the effect of Ge diffusion to the gate oxide on the low frequency noise characteristics in both n- and p-type strained-SOI MOSFETs is investigated. We have found that a larger number of inhomogeneous oxide traps are generated near the conduction band edge by Ge diffusion and fewer near the valence band edge, causing increase in the low frequency noise only in the n-MOSFETs.

Ultra-thin strained-SOI CMOS were fabricated by half-micron CMOS process on relaxed SiGe-on-insulator (SGOI) substrates with Ge content of 30% (2) produced by the Ge condensation technique (3). The thickness of ultra-thin strained-Si varied from 0 to 25 nm. The 8 nm thick gate oxide layers were formed by oxidation at 800C in O_2 and HCl gases. Maximum thermal budget in our process was RTA process of 1000C for 20 sec to form single S/D region. As a result, Ge atoms diffused into strained-Si layers by 4 nm, over which Ge concentration decreases from 10^{22} to 10^{19} /cm^3, from the strained-Si/relaxed SiGe interface, which was measured by SIMS (2). The chemical bonds in the gate oxide were analyzed by XPS. GeO peak was observed in the 7 nm thick strained-Si layer showing Ge atoms reach to the gate oxide/strained-Si interface (2).

Figure 1 shows electron and hole high field mobility as a function of strained-Si thickness. The mobility degradation in the strained-Si, thinner than 6.5 nm, is attributed to Ge alloy scattering caused by Ge diffusion into the strained-Si layer (4). Figure 2(a) shows the relationship between the drain current noise, Sid, in n- and p-MOSFETs and the strained-Si thickness. In the n-MOSFETs, the Sid rapidly increases with decreasing strained-Si thickness less than 5 nm after Ge atoms reach the gate oxide/strained-Si interface, while the Sid is almost constant in the p-MOSFETs. As shown in Fig. 2(b), the noise spectra in the n-MOSFETs deviate from 1/f shape and exhibit a hump as the strained-Si thickness decreases, while such deviation is observed little in the p-MOSFETs. If high-density traps, which can capture and emit carriers, locate in a certain depth range in the gate oxide, the noise in the frequency range, related to the time constants of those traps, increases and the noise spectrum has a hump. Therefore, Fig. 2 represents that a larger number of oxide traps are generated inhomogeneously in the depth direction inside the gate oxide near the conduction band edge by Ge diffusion and fewer near the valence band edge. It is also found in Fig. 3 that the negative oxide tapped charges, evaluated from the Vt shift, increase with decreasing strained-Si thickness less than 5 nm in the n-MOSFETs, while not in the p-MOSFETs, corresponding to the Sid dependence on strained-Si thickness in Fig. 2(a). This result means that the Vt shift is caused not by fixed oxide charge states but trapping states, which can change the charging condition depending on the Fermi level under the inversion condition. Therefore, the difference between n- and p-MOSFET can be explained by the difference in the relative location of Fermi level to the oxide trap level. These results do not contradict the results that oxide traps are generated dominantly near the conduction band edge by Ge diffusion, obtained from the noise characteristics.

In summary, we have investigated the effect of Ge diffusion to the gate oxide on the low frequency noise characteristics in both n- and p-type strained-SOI MOSFETs. It is found that a larger number of inhomogeneous oxide traps are generated near the conduction band edge by Ge diffusion and fewer near the valence band edge, causing increase in the low frequency noise only in the n-MOSFETs.

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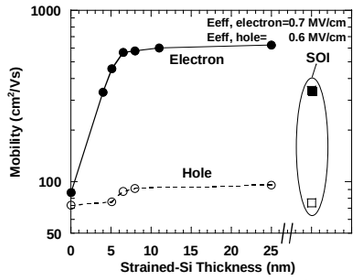

Fig. 1. Electron and hole mobility as a function of strained-Si thickness.

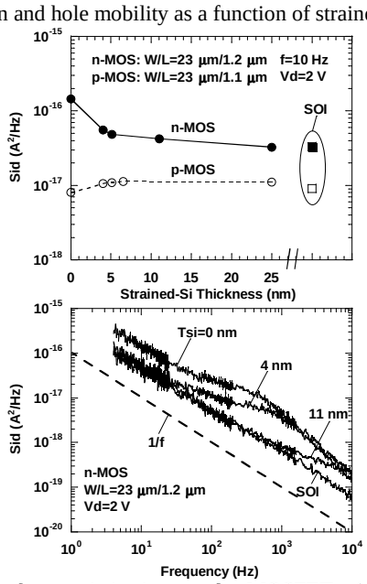

Fig. 2. Noise characteristics in n- and p-MOSFETs. (a)Dependence on strained-Si thickness, Tsi, and (b) noise spectra.

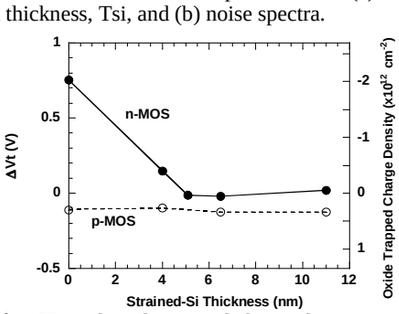

Fig. 3. Vt shift, ΔVt, and oxide trapped charge density as a function of strained-Si thickness in n- and p-MOSFETs.