Design, Fabrication and Operation of Sub-65nm Strained-Si/Si $_{1-x}$Ge$_x$ MOSFETS

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Abstract

As power supply voltage lowers with successive scaling, the non-scalability of threshold-voltage (V_T) and gate oxide (T_{ox}) (without the use of high-κ dielectric) to maintain low stand-by leakage is rapidly reducing the maximum gate overdrive factor, $C_{ox}(V_{dd}-V_T)$ [1]. Enhancing carrier mobility by biaxially-straining Si with relaxed SiGe virtual substrates [2] may provide a viable option to sustain the continual drive current increase. Though strained-Si (SSi) augmentation of conventional MOSFET seems minimally disruptive, the use of SiGe virtual substrate in CMOS devices introduces new process and device issues that need to be addressed in order to prove successful manufacturability. This paper highlights and discusses some of these issues.

Short-channel, 50nm and 60nm, CMOS devices featuring a 1.9nm nitrided oxide starting with a 13nm SSi cap on SiGe virtual substrates (25% Ge) have been fabricated (Fig.1). Devices with and without elevated source/drain (S/D) are processed to evaluate the effects of Ge segregation with cobalt silicidation. The elevated S/D are formed by selective epitaxial growth (SEG) of Si after nitride spacer formation. Due to dramatic dopant diffusion differences in Si and SiGe, extensive S/D and channel re-engineering is necessary to achieve optimized short-channel devices.

The electron mobility as a function of effective vertical field showed a 2x-enhancement with respect to the Si control devices (Fig. 2). On the other hand, the holes only enjoy a modest 20-25% increase in peak mobility and exhibit a strong effective-field dependence that diminishes any gain under moderately high vertical fields. By careful optimization of the S/D and halo doping, the 60nm n-channel SSi device demonstrates superior short-channel control, exhibiting a DIBL metric of only 30mV/V and an inverse substhreshold swing of 77mV/dec, while the equivalent Si device show a 3x larger DIBL (Fig. 3). The SSi device exhibits a 46% drive-current enhancement and a 20% increase in saturation Gm over the Si device at one-volt gate overdrive. Misfit dislocations at the SSi-SiGe heterointerface that arise from SSi relaxation can pose serious reliability problems [3]. Figure 4 shows the wide- and narrow-channel Id-Vg behavior of selected 60-nm SSi nMOSFETs. Many selected short-channel wide-width devices (L<100nm, W=10μm) exhibit subthreshold slope degradation that is only rarely observed in the narrow devices (W=0.2μm). As dopant diffusion from the source and drain can be further enhanced along the defect, creating a weak buried channel. Under higher gate bias, the steeper subthreshold slope for a surface channel is recovered (Fig. 4). Successful small-circuit operations have been demonstrated. Despite the lack of pMOSFET drive current enhancement, SSi ring-oscillator is 13% faster than the Si control. The SSi SRAM bit cell operates at a static noise margin of 140mV at V_{dd}=1.2V (Fig. 5).

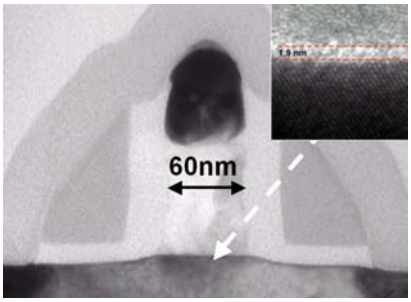

Fig. 1 Cross-sect. TEM of a 60nm strained-Si device with $CoSi_2$. Inset: High-resolution TEM of the 1.9nm nitrided SiO_2 SSi interface.

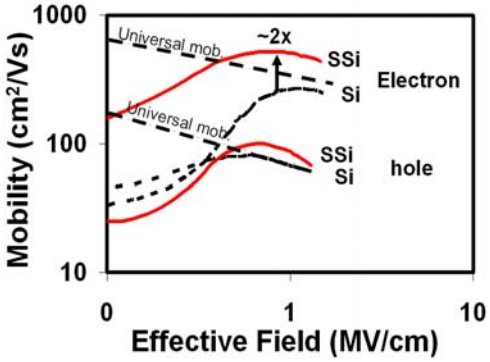

Fig.2 Electron and hole low-field mobility comparison for SSi and Si devices.

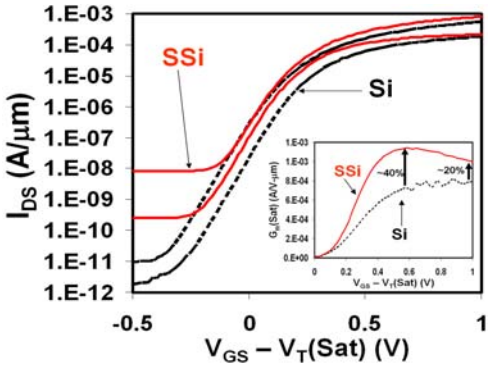

Fig. 3 Id-Vg curves for 60nm SSi and Si devices. Inset: Saturation transconductance at Vds=1.2V.

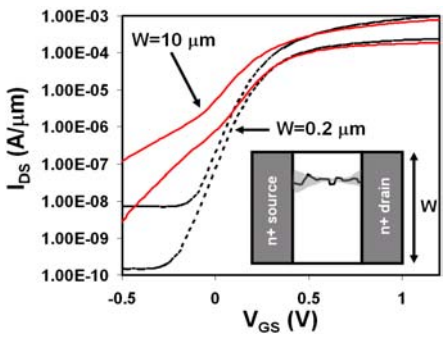

Fig.4 Id-Vg curves for wide and narrow SSi n-channel devices with Lgate=60nm. The Id-Vg at Vds=0.1V and 1.2V are plotted for each device.

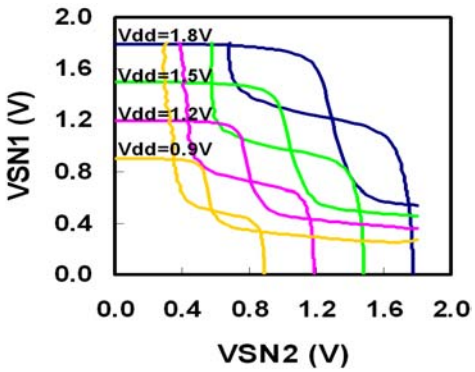

Fig.5 SSi SRAM bitcell "butterfly" curves

Acknowledgments

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