Optoelectronic Substrates by SiGen NanoTec™ - a General Layer-Transfer (LT) Approach

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New materials for optoelectronic and semiconductor applications are increasingly manufactured using layer-transfer (LT) methods. This paper reviews a unique LT approach – SiGen NanoTec™ process [1,2]. The paper presents data on two applications relevant to this topic: Germanium-on-Insulator (GeOI) and multi-layer-SOI wafers. 150 mm diameter GeOI substrates were manufactured and characterized for physical and chemical properties. Multi-layer-SOI are produced by repeating the LT process sequence with two and/or three stacked SOI layers on 200mm wafer substrates. The key to successfully producing these innovative optoelectronic starting materials are the plasma-activated bonding and room temperature cleaving of the various material layers. Additionally, a unique non-contact process, Epi Smoothing (ES), is used on as-cleaved substrates to achieve device layer quality surface roughness. ES also provides excellent layer uniformity. Both the GeOI and the multi-layer SOI wafers were evaluated for properties relevant to device fabrication using a variety of analytical techniques. Both materials were found suitable for initial device processing.

[1] IJ Malik et al, Spring 1999 MRS Symp. T Proc., MRS, 1999.
[2] IJ Malik at al, SSDM, Sendai, Aug. 2000.
[3] CJ Tracy et al, J. Electronic Materials, in press.

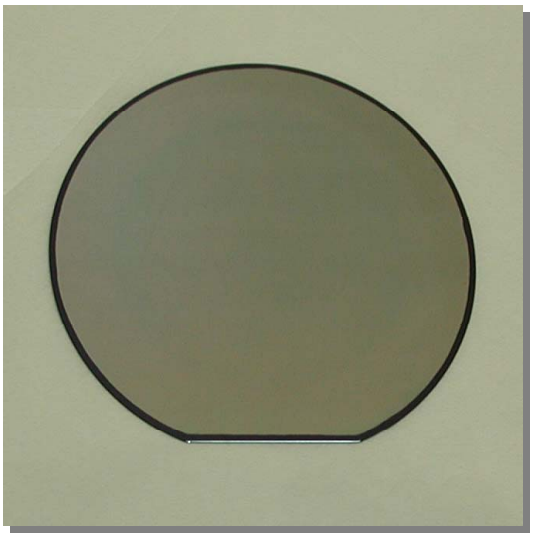

Fig. 1: A 150 mm diameter GeOI wafer manufactured by SiGen NanoTec™ LT process. Note the complete Ge layer transfer.