Low temperature SiGe process for defect-free epitaxy and smooth morphology

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Abstract

Low temperature SiGe process has been successfully developed to grow defect-free epitaxy and smooth morphology by RTCVD process. The effects of baking temperature, baking duration, H_2 pressure, seed layer thickness, were investigated to grow different SiGe epi layers on various active regions and SiGe poly films on STI. H_2 baking pressure plays a key role to remove oxygen-containing residue and improve discontinuity with low thermal budget from SEM & SIMS microanalysis results. A mechanism related with hydrogen desorption and reduction is proposed to explain this key effect.

Purpose and Experimental Procedure

SiGe epitaxy has been studied to implement for BICMOS devices due to higher current gain [1], and for CMOS devices due to mobility enhancement [2]. The quality of epi films would mainly determine the final electric performance of devices for these applications. Surface preparation by cleaning or baking processes plays a key role to grow epi films. H_2 baking process, which usually higher than 950°C, becomes more critical to cleaning efficiency during epi growth due to lower thermal budget as devices scaling down in advanced generations. In this work, a low temperature baking process for defect-free SiGe films was intended to develop for meeting the requirement of 0.18 μm BICMOS applications and beyond.

Si-Ge films (Ge conc. ranged from 8 to 16%) were pre-cleaned by HF last process, and grown SiGe epi on active areas with heavy-implanted doping in high speed (HS) devices and SiGe poly on shallow trench isolation (STI) regions for BICMOS application by RTCVD tool. Process parameters including baking temperature (950°C>A>B>C), H_2 baking pressure, Si seed layer thickness, were used to develop a robust defect-free SiGe epi process. Oxygen concentration was analyzed by SIMS analysis. Crystal defect and surface morphology of epi films were examined by SEM microanalysis.

Results and Discussion

Temperature v.s. Pressure	760 torr	Medium	Low
950°C	0	0	0
Temp. A	557	0	0
Temp. B	1730	415	0
Temp. C			1700

Table I Peak oxygen concentration at different conditions

Peak oxygen concentration of samples (counts/sec) at the interface of epi and substrate is listed in Table I. Fig. The oxygen concentration depth profile of samples is shown in Fig.1 and Fig. 2 after baking at temperature A (target temperature for thermal budge less than 5 minutes) and B respectively using different baking pressures. The higher baking temperature and the lower baking pressure are, the higher oxygen removing efficiency is for baking process to achieve defect-free epi layers. Additional advantage to reduce baking pressure is to improve surface morphology of SiGe poly on STI area in Fig. 3. Defect-free low temperature SiGe process with reduced H_2 baking pressure was successfully developed from these results.

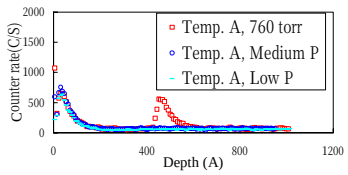

Fig. 1 Temperature A

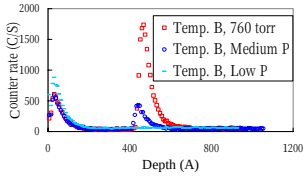

Fig. 2 Temperature B

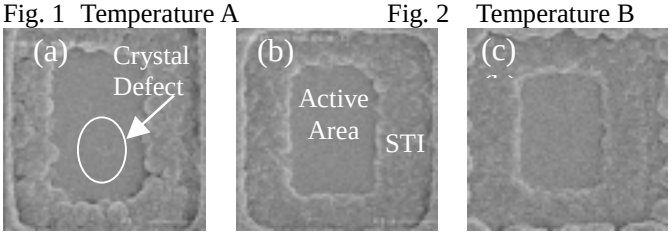

Fig.3 Surface morphology of SiGe films baked at Temp. A by, (a) 760 torr, (b) Medium pressure, (c) Low pressure.

Crystal defects were only found in the sample with active areas of HS device, enclosed by STI surrounding regions, in Fig. 4. It also indicates that crystal defect induced by oxygen-containing residue would be enhanced by heavy-doped implantation and STI. Thicker seed layer would improve surface morphology as well.

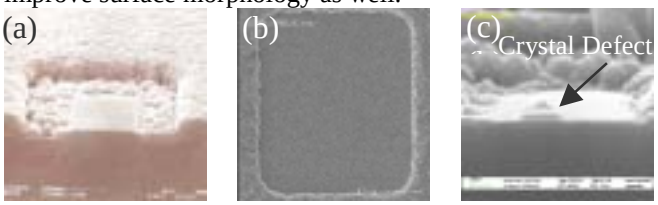

Fig. 4 Samples baked at 760 torr and Temp. A, (a) No implant with STI, (b) HS implant without STI, (c) HS implant with STI.

At high temperature, the desorption and reduction of H_2 are quite efficient to result in the defect-free epitaxy. Both H_2 effects degrade as temperature reduces. The reduce of H_2 pressure to decrease Si-H or O-H coverage on substrates becomes critical to reduce oxygen-containing residue especially for samples with heavy-doped implant.

Conclusion

Low temperature SiGe process using low baking pressure was successfully developed to effectively remove oxygen-containing residue for defect-free SiGe RTCVD process in 0.18 μm BICMOS applications and beyond.

References:

[1] D.L. Harame, et al., IEEE Trans. Elec. Device, **42 (3)**, p 455, 1995.
[2] K. Rim, et al., VLSI, p98, 2002.