Abs. 1344, 206th Meeting, © 2004 The Electrochemical Society, Inc.

A Novel, High Quality SiGe Graded Buffer Growth Process Using $GeCl_4$

Richard Westhoff, John Carlin, Matthew Erdtmann, Thomas Langdo, Christopher Leitz, Vicky Yang, Ken Petrocelli, Mayank Bulsara, E.A. Fitzgerald, and Christopher Vineis
AmberWave Systems Corp., 13 Garabedian Drive
Salem, NH 03079, rwesthoff@amberwave.com

Introduction

A relaxed SiGe virtual substrate (VS) forms the growth template for strained silicon MOSFETs. A high throughput SiGe graded layer process that maintains high quality is required for this technology platform. High quality (few dislocations and dislocation pileups, low surface roughness and particles) and economic (high growth and grade rate) graded layer metrics are difficult to attain simultaneously. Threading dislocation density, ρ_t, of graded layers increases with growth rate, $\mathbf{R_G}$, and grade rate, $\mathbf{R_{Gr}}$, and decreases exponentially with temperature, **T**, as described by the following equation[1]:

$$\rho_t \sim R_G * R_{Gr} * \exp(E_a/kT).$$

Where $\mathbf{E_a}$ is the activation energy for dislocation glide velocity and **k** is Boltzmann's constant. The increase of dislocation density with decreased temperature[1] and increased grade rate[2] is documented in the literature. The increase in dislocation density with increased growth rate has been observed experimentally. Higher temperature growth (>1000°C) is the most promising means to control dislocation density without sacrificing growth rate, which is required for a high throughput process. However, high temperature SiGe graded layer growth with GeH_4 (to ~900 °C) can cause gas phase nucleation and reactor coating issues that promote particle generation, resulting in lesser quality strained silicon wafers. Additionally, such processes require frequent reactor maintenance, limiting the economics of strained silicon wafer manufacturing. Here, we present a graded layer VS process using dichlorsilane (SiH_2Cl_2) and germanium tetrachloride ($GeCl_4$) with atmospheric pressure (AP) or reduced pressure (RP) chemical vapor deposition (CVD) to grow VS layers with low process time (10-15 min/wafer) and high material quality metrics.

Process Description

All epitaxial growth steps were done in an ASM Epsilon™ E2000 RPCVD system at AP or RP (80 Torr) on 200mm substrates. The SiGe VS process began with an etch with HCl to remove reactor coating, and wafers were loaded and baked 30 seconds at 1130°C to remove native oxide. Next the SiGe graded layer was grown using SiH_2Cl_2 (100-250sccm) and $GeCl_4$ (0-0.5g/min) at 1000-1100°C at rates of 0.4-1μm/min. The graded layer was either 1 or 2μm thick with an overall grading rate of 10 or 20% Ge/μm, and was grown in 1-4 minutes to a terminal composition of ~19% Ge. A 19% Ge cap layer was then grown to ~2μm thick in 2-4 minutes. Fig. 1 shows a comparison of the growth rates for GeH_4 and $GeCl_4$ processes utilized in this study.

Results

In contrast to SiGe VS growth with GeH_4 (at 875°C, (Fig. 2a), after the growth process with $GeCl_4$ (Fig. 2b), the reactor chamber was substantially free of deleterious coating. This result significantly improved reactor uptime and enabled the growth of low particle density VS layers. Layers were characterized using spectroscopic ellipsometry (SE); Fourier transform infrared spectroscopy (FTIR); secondary ion mass spectrometry (SIMS); x-ray diffraction (XRD); vapor phase decomposition inductively coupled plasma mass spectrometry (VPD-ICPMS); and etch pit density (EPD) for threading dislocation density (TDD) and dislocation pileup density (DPD), correlated with plan view transmission electron microscopy (PVTEM). The SiGe VS layers had excellent thickness (<± 3%) and Ge (<± 0.01 Ge mole fraction) uniformity (5 mm edge exclusion), highly repeatable SiGe grading profile, high relaxation (>96%), low metals contamination (<3E10 cm^{-2}), and low TDD and DPD (TDD<2E5 cm^{-2} and DPD<1 cm^{-1}). Note that TDD is measured as total threading dislocations per unit area, yielding an areal density, while DPD is measured as total pileup length per unit area, yielding a linear density. Recent modifications to the epitaxial process have enabled an improved SiGe VS that is substantially free of dislocation pileups (DPD <0.01 cm^{-1}) with essentially no impact on wafer throughput; results will be reported elsewhere. The reduction of reactor wall coating also enabled the process to produce VS wafers with low particle counts. Impurity analyses of SiGe layers grown using the highest available purity $GeCl_4$ indicated that its purity (for C, O, and metals) is as good or better than that of GeH_4.

In conclusion, the use of $GeCl_4$ as a Ge precursor has enabled fabrication of high quality SiGe VS layers. Despite a total epi thickness of 4-5 μm for this SiGe VS, the entire epitaxial process required less than 15 minutes, providing a very economic path for the high quality wafers required for strained Si CMOS.

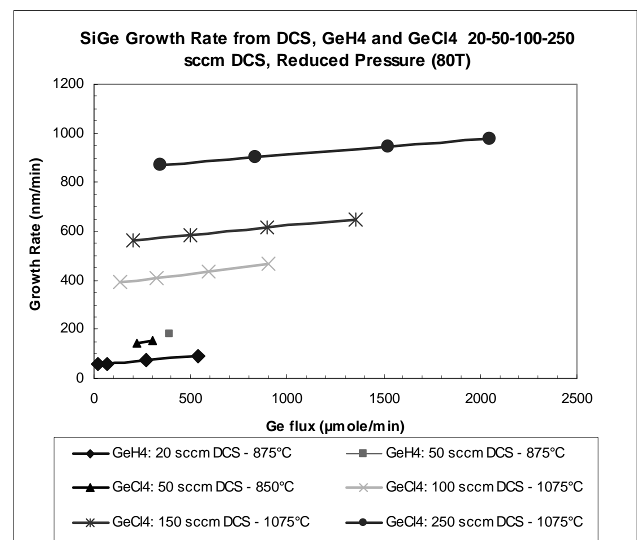


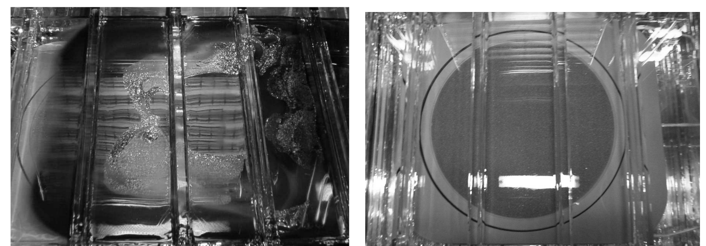
Fig. 1. SiGe growth rate versus source gas flow for growth with GeH_4 and $GeCl_4$.

(a) GeH_4 source gas (b) $GeCl_4$

Fig. 2. Reactor coating with (a) GeH_4 as Ge source, and (b) $GeCl_4$ as Ge source (RP conditions).

References

1. E.A. Fitzgerald, et al., Mat. Sci. Eng B67, 53-61, 1999



2. G. P. Watson, et al, J. Appl. Phys., 75 (1), 1994