Ge deep-submicron PMOS transistors with etched TaN metal gate on a High-K dielectric, fabricated in a 200mm prototyping line

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The need for electron and hole mobility enhancement and progress in high-k deposition techniques, lead in the past years to a renewed interest in Ge substrate MOSFETs. Until now however all the transistor data published in the literature are exclusively for long channel transistors [1],[2] and [3]. But, before Ge devices can be used for advanced circuits, many issues of the Ge processing and device properties have to be addressed by fabricating them in conventional deep sub micron silicon like process. In the first place, the mobility enhancement of Ge vs. Si, as observed in long channel transistors, has to be proven to result in a larger drive current for short channel transistors. Secondly, it must be possible to manufacture these Ge devices in a silicon-like semiconductor-manufacturing environment. Last but not least, the reliability and yield of the Ge based circuits, has to be sufficient to allow ULSI circuits. This work builds on the results presented by [1], [2] and [3] and extends them to deep sub micron pFETs on 200mm wafers with standard DUV lithography and direct metal gate etch. A 3-mask process flow, compatible with a Si-process, for fabricating deep sub micron Ge PMOS transistors with directly etched TaN metal gate and HfO_2 gate dielectric is presented for the first time and transistor device characteristics are analyzed. It is seen as a first step for the future exploration of the Ge based CMOS devices.

100mm and 200mm <100> 10 Ω.cm bulk Ge wafers were used, with specifications similar to those of Si device wafers. First, the HfO_2 deposition on a Ge surface was studied with Atomic-Layer CVD (ALCVD). In Fig. 1 the Hf growth curve as function of the ALCVD cycles and for different prepared Ge surfaces is shown. The steady growth rate is similar for Ge and Si substrates.

Also, capacitor and transistor structures were processed with a process flow, similar to silicon device structures. The gate stack consisted of a 10nm HfO_2 layer, with a metal gate of 10nm TaN thin film covered with a thick TiN layer. The HfO_2 deposition was performed with ALCVD at 300°C or Metal-Organic CVD (MOCVD) at 485ºC. The surface was pre-treated with a 600°C NH_3 anneal [4,5]. After standard DUV litho, the gate was dry etched with a specially developed metal etch process, producing physical gate lengths down to 0.15mm while stopping on HfO_2. In Fig. 2 a SEM picture shows the transistor structure made on Ge. Note the spacer formation to allow sub micron features.

In Fig. 3 the I_D-V_D characteristics of an 0.18µm Ge transistor with an HfO_2 layer are presented. This result shows the feasibility of a Ge transistor device with short gate lengths using a High-K deposited layer and a metal gate. Note for this channel length, the short channel effect, because more research is necessary for improved doping and activation in Ge processing.

References:
[1] Chui, C.O. et al., IEDM'02, p.437 (2002)
[2] Shang, H. net al., IEDM'02, p.441 (2002)
[3] Huang, C.H. et al., Symp. VLSI Techn., p.119, (2003)
[4] Bai, W.P. et al., VLSI'03, p.121
[5] Van Elshocht, S. et al., accepted for MRS spring meeting 2004

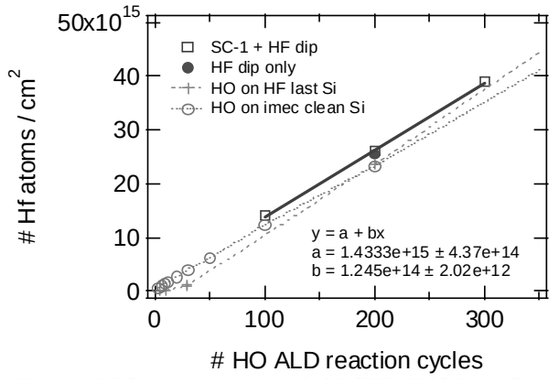

Fig. 1: RBS growth curve of ALCVD HfO2 on Ge with different surface treatments. As a reference the growth curve on Si is shown

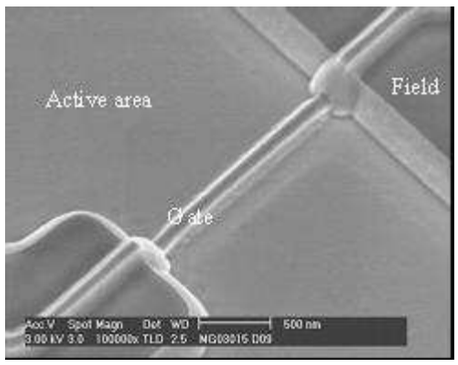

Fig. 2: SEM picture of the short-channel transistor structures made on Ge. Note the small gate feature (dry etched metal gate) and the spacer.

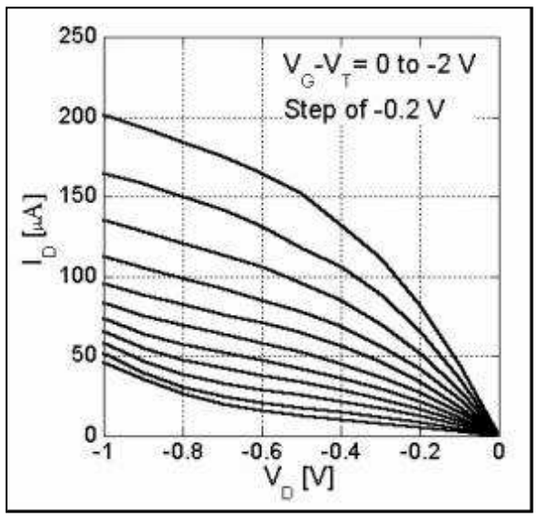

Fig. 3: Characteristics of a transistor made with a NH_3 pretreated 10nm MOCVD HfO_2 layer on Ge. Gate length is 180nm and gate width is 2 µm.