Strained Silicon on Relaxed SiGe made by Ion Implantation and Strain Transfer

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Introduction of tensile strain into the silicon channel of MOSFETs enhances the carrier mobility, the drain current at saturation and the speed of the transistors [1]. Presently, a key issue is the making of the strained silicon in high quality, preferentially on SiO_2. We have demonstrated that thin relaxed SiGe buffer layers can be made by H or He ion implantation and annealing [2]. When He ions are used, a defect band about 100- 200 nm below the SiGe/Si interface is formed. These defects initiate strain relaxation via misfit dislocations at the interface during annealing around 850°C. The surface roughness of the relaxed SiGe layers amounts to <0.5 nm. The threading dislocation density depends on the Ge content x and the layer thickness and is in the range of $7x10^5$ to $5x10^6$ cm^{-2} for x = 0.2 – 0.27. Recently, we have shown that reduced self-heating in strained Si MODFETs is observed when they are fabricated on thin SiGe buffers as compared to those on 4 µm thick buffers [3].

In this contribution we will show several examples and, in addition, strain build up in a thin silicon cap layer during relaxation of the SiGe layer. We used chemical vapor deposition (CVD) to grow the 150 nm $Si_{.74}Ge_{.26}$ buffers and the Si top layers on 6 and 8 inch Si(100) wafers. The thickness of the Si cap layer was varied between 0 and 30nm. All wafers were implanted with He ions with a dose of $7x10^{15}$ cm^{-2} and annealed in Ar at 850°C for 600s. The layers were investigated by RBS, ion channeling, ellipsometry, transmission electron microscopy (TEM) and AFM. The strain in the layers was measured with Raman spectroscopy using excitation at a wavelength of 415nm. If the thickness of the Si cap is below a critical thickness, threading dislocations glide from the SiGe layer into the cap layer and strain the silicon layer during annealing. Fully pseudomorphic, strained silicon on relaxed $Si_{.74}Ge_{.26}$ was obtained as evidenced by detailed cross-sectional TEM. For the investigated 150 nm $Si_{.74}Ge_{.26}$ buffers a critical thickness of about 8 nm was found. A TEM cross-section of such a structure is shown in Fig. 1. The strained silicon cap has a thickness of 8nm. No threading dislocations in the SiGe layer are visible in the cross-section. Strain contrast arising from the misfit dislocations at the SiGe-substrate interface are clearly visible. Deeper in the substrate residual damage from the He implantation remained. The efficiency of strain transfer will be discussed in dependence of the silicon cap layer thickness.

Producing the strained silicon directly by strain transfer has several advantages. First, only one epitaxial growth step is required to make a thin strained layer and second, optional overgrowth on silicon is much easier than on relaxed SiGe. Standard silicon clean and standard growth conditions can be applied.

Furthermore, we will discuss the use of heavier ions for the strain relaxation of the SiGe layers. First results will be presented and compared with He results. The advantage of using heavier ions is that the ion dose and thus the implantation time can be strongly reduced.

In summary, we will show that ion implantation and annealing of pseudomorphic SiGe layers is a CMOS compatible method for the production of strained silicon on relaxed SiGe. The excellent surface morphology allows wafer bonding without polishing. The use of strain transfer allows the formation of thin strained Si layers by only one growth step with a thickness (≈8nm) sufficient for ultra thin body SOI MOSFETs.

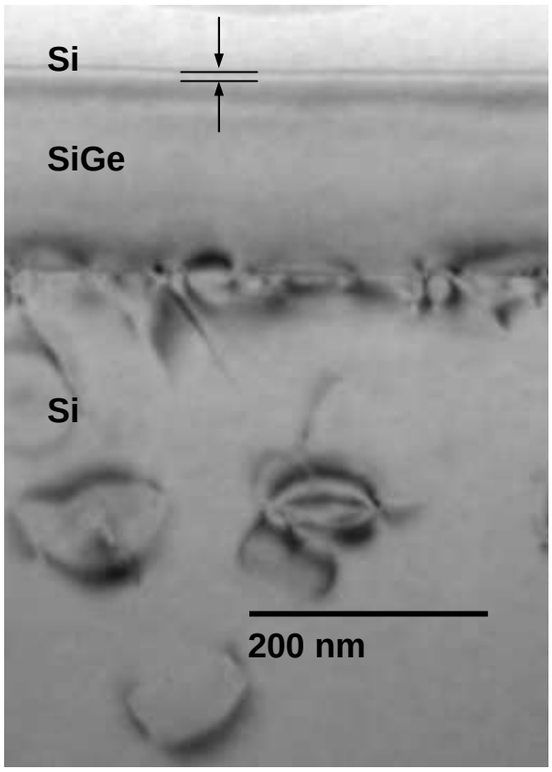

Fig. 1. Cross-section TEM micrograph of a relaxed 150 nm $Si_{.74}Ge_{.26}$ layer with an 8 nm strained silicon cap.

[1] K. Rim et al., Symposium on VLSI Technology Digest of Technical Papers p. 98 (2002).
[2] B. Holländer, St. Lenk, S. Mantl, H. Trinkaus, D. Kirch, M. Luysberg, T. Hackbarth, H.-J. Herzog, and P.F.P. Fichtner, Nucl. Instrum. Methods Phys. Res. B 175-177, 357 (2001).
[3] Th. Hackbart, H.-J. Herzog, K.-H. Hieber, U. König, S.Mantl, B. Holländer, St. Lenk, H. von Känel, M. Enciso, F. Aniel, and L. Giguerre, Proc.of ISDRS Conf 2003, Washington, Dec. 2003
[4] D. Buca, B. Holländer, H.Trinkaus, S. Mantl, R. Loo, M. Caymax and H. Schäfer, submitted to Phys. Rev. Lett.