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Selective epitaxy of Si and SiGe for advanced applications: possibilities and limitations

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Selective Epitaxial Growth (SEG) is a growth process in which deposition of epitaxial Si or SiGe occurs only on the bare Si surface inside windows in a patterned insulator-covered wafer. This unique feature of CVD has attracted considerable interest due to its potential for self-aligned processing of very advanced devices. Some important applications of SEG (both Si and SiGe) are i) the base layer stack in Heterojunction Bipolar Transistors in BiCMOS technology and ii) Raised Source/Drain areas on bulk Si as well as on Si on Insulator (SOI) wafers. We will touch as well on some other, more exploratory applications.

SEG has been shown for various deposition chemistries. These chemistries can be divided into two classes, i.e. with and without chlorine. Typically, unlimited SEG in chlorine-free ambience is only possible for temperatures above 1100 ºC. Below this temperature, unvariably nucleation of Si on the insulator surface followed by poly-Si deposition will occur after some limited time/thickness of selective deposition. Full selectivity at all temperatures has only been shown in chlorine-containing mixtures, e.g. SiH_4 + HCl or SiH_2Cl_2 (with or without HCl), in which the chlorine component is able to etch away possible nuclei from the insulator surface before they can reach a critical size. SEG has been studied since the early sixties of last century. Important progress however has been possible only since the advent of load-locked reduced pressure reactors with very low background oxygen and water contamination levels and ultra-clean gases. This allowed to avoid serious problems with quality degradation such as metal contamination by HCl and at the same time to reduce epi growth temperatures. Lower deposition temperatures can be very helpful in avoiding issues such as defects on the Si/SiO_2 interface and dopant redistribution, but can at the same time compromise layer quality.

There are several important problem areas for some of which solutions are already available but for others not yet. Among these are loading effects, facetting, selectivity loss, crystalline defects, excessive thermal budgets, limitations in doping, limited throughput (and therefore a high add-on cost) and others. We will discuss some of these, and indicate solutions that have been found, as well as areas where further work is needed.

A first problem area is loading effects: the growth rate (and therefore the thickness) is dependent on the dimensions and spacing of the windows, and on the Si/SiO_2 area ratio. This loading effect can also play on the composition of SiGe layers as well as on doping levels. Generally, SEG can show both micro-loading and macro-loading effects. Micro-loading plays on the dimension of the microscopic features inside an IC, and can involve both variations in growth from window to window, and non-uniform growth rate inside a window. It can be caused by local variations in gas phase precursor concentrations and by local variations in surface temperature. The most important parameter to play with for solving micro-loading is the deposition pressure. Macro-loading plays on the wafer scale, and can also be caused by varying gas phase concentrations ("depletion") as well as by thermal effects. Process parameters to solve this effect are pressure, temperature profiles, wafer rotation, gas flow and gas distribution. In brief, it is perfectly possible to tune SEG processes towards fully loading-free conditions.

A next one is the formation of crystalline facets on the edge of the Si layer near the border of the windows. Connected to these facets can be crystalline defects in the Si which grows over neighbouring insulator areas (ELO – epitaxial lateral overgrowth). The major factor controlling facet formation is the shape of the SiO_2 side walls. The presence of the any step in this side wall will cause Si overgrowth. In this way, the Si crystal will be allowed to grow into its natural habitus exhibiting the slower growing planes, i.e. (111) and (311), which show up as facets. Additionally, the temperature, growth rate and type of insulator can also influence the onset of facet formation. In general, also this problem can be solved satisfactorily, be it as part of a broader integration effort.

Although it is mentioned before that full selectivity is only possible in chlorine-based chemistries, full selectivity is therefore not always guaranteed, or can be difficult to be obtained. An important factor influencing selectivity is the insulator material (e.g., SiO_2 vs. Si_3N_4), the way it is made, and the previous processing and cleaning which have been applied on this insulator surface. Generally, SiO_2 exhibits better selectivity properties than Si_3N_4, and any defects, contamination or irregularities can induce Si nucleation. Also the cleanliness of the deposition environment is extremely important. Applications involving mainly Si_3N_4 covered fields can be subject to unexpected loss of selectivity which then is due to very minor flaws in the processing conditions. This can cause important problems, especially in manufacturing. In this respect, SiO_2 gives much less troubles and is to be preferred if the architecture allows it.

Finally, there is a number of less generally known problems. Not necessarily an SEG problem, but still closely connected to it, is the aspect of the pre-epi cleaning which needs to reveal the bare Si surface: the advanced applications which ask for SEG usually impose severe limitations to the allowable thermal budget. Specific cleaning schemes were needed. Furtheron, a very appealing application is Raised Source/Drain, which can be made with undoped Si in a first approach. Even more interesting however, especially for ultra-shallow junctions, is the possibility of in-situ doping. Here, we are facing limitations to the maximum active dopant concentration that can be reached. A last area that could be mentioned is the use of in-situ Si back etching with HCl, a technique that allows to recess the epitaxial layer e.g. to make it level with the surface of the surrounding areas. In this technique, there are restrictions to the ratio of vertical vs. horizontal etch rates, which can limit the application field of this technique. These issues will be discussed as well, time permitting.