Abs. 1382, 206th Meeting, © 2004 The Electrochemical Society, Inc.

Industrial Applications of Poly-Silicon-Germanium as Functional MEMS Material ^Tino Fuchs, ^Christina Leinenbach, ^Silvia Kronmueller, ^Franz Laermer, ^^Tudor Thomas, ^^Kenneth Robb, **Helmut Seidel and *Wilhelm Frey

 ^Robert Bosch GmbH, Robert-Bosch-Platz 1, D-70839 Gerlingen, Germany;
*Robert Bosch Corporation, 4009 Miranda Avenue, Palo Alto, CA 94304, USA
^^STS - Surface Technology Systems plc, Imperial Park, Newport, NP10 8UJ, UK
**Saarland University, Dept. of Micromechanics, Microfluidics/Microactuators, D-66123 Saarbrücken, Germany

Introduction

The number and diversity of micro electro mechanical systems (MEMS) that are used in industrial applications are continuously growing. In addition, there is an increasing demand for more and more complex systems. The main requirements for both new and existing applications are increased performance to allow for smaller units and/or better functionality, as well as lower manufacturing costs, enabling MEMS to eventually diversify from high-end applications into ubiquitous consumer goods. The introduction of modern integration techniques enlarges the versatility of MEMS manufacturing technologies, enabling future MEMS devices to face these challenges. The talk addresses SiGe MEMS as a versatile technology by highlighting both prospects and problems encountered from an industrial point of view.

Silicon-germanium (SiGe) MEMS is a new development in MEMS integration technology. The functional layer consisting of a silicon-germanium alloy is deposited at low temperatures and micro structured in IC-backend (i.e. after completion of the evaluation circuitry IC), allowing the MEMS structure to be vertically integrated on top of the active IC area.

IC and MEMS processes are completely separated and decoupled. Stacking MEMS over IC, this vertical backend integration concept enables multi-use of costly IC surface going along with reduced parasitics for high performance devices such as miniaturized accelerometers and gyroscopes. Scalability of this integrated process allows for reducing the chip size and for using the IC process to provide customized specifications 'on demand', providing for desired characteristics at minimized fabrication costs.

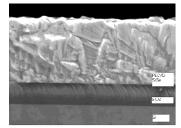
However, we are dealing with a new and basically unknown MEMS material. The temperature tolerance of the processed IC narrows the thermal budget available for SiGe backend processing; and a HF free sacrificial layer etching technique enables possible use of dielectric isolating oxide layers, but is a new process, too.

Experimental / Results

Potentially feasible deposition techniques include LPCVD, PECVD, and atmospheric epitaxy, which is addressed in a joint effort by Bosch and collaboration partners like UC Berkeley, as well as the SiGeM consortium consisting of Bosch GmbH, Philips, ASM, IMEC, and CNM. A commercial batch system for SiGe deposition (Centrotherm) with added PECVD option was installed at Bosch.

The machine allows for switching between two generators, 450kHz and 40kHz and includes the option for pulsed operation. The films can be doped n- or p-type insitu using gases like PH₃ and B_2H_6 , respectively. The deposition temperature can be adjusted between room temperature and 600°C at maximum. The maximum pressure is 2 Torr.

With these features SiGe films were deposited to determine important physical properties and first of all to optimize the stress and stress gradient. The Centrotherm batch device allows for SiGe deposition rates capable for a production line. The morphology of the SiGe layers measured by SEM, TEM, XRD, and AFM will be addressed in detail.



SEM micrograph of PEVCD SiGe

The chemical constitution is obtained by XPS. It is known that the stress gradient is strongly influenced by the grain structure. Stress gradient reduction for the deposited SiGe layers has been achieved by various techniques, like stacking multiple layers, using different types of seed layers or the removal of edge layers from freestanding beams after the release step.

In situ alloying of SiGe with other elements causes a variation in the crystal structure or inclusion of interstitial atoms. In that way the strain in the crystal lattice can be reduced.

In general it is possible to deposit polycrystalline SiGe on sacrificial oxide with different seed layers. The stress gradient changes with the variation in deposition parameters of the batch CVD-process.

Achnowledgements

The authors would like to thank Andrew Chambers, Technical Director of STS, Newport (UK) for providing the PECVD single wafer tool. Also we want to thank the staff of STS for the excellent technical support as well as many helpful discussions at STS. We are grateful to Christoph Duenn of the Bosch Sensor Process Technology Department, Reutlingen, Germany, for invaluable experimental support and discussions, Professors Tsu-Jae King and Roger Howe, as well as the SiGe-MEMS-Group at BSAC for their helpful discussions and experimental expertise, as well as the UC Berkeley MicroLab staff for continuous support.