Regular Paper Device Physics & Novel Structures

Fast recovery and low Vf characteristics on SiGe/Si/Si pin diodes

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In the power switching circuits, fast recovery diodes with the low on-state voltage drop (Vf) are necessary for the lower switching noise, the faster operation or the lower power dissipation. To achieve the fast operation, the suppression of the minority-carrier lifetime is effective by the gold diffusion or the irradiation of high-energy electron into the i-layer. This technique, however, sacrifices Vf according to the reduction of recovery time (Trr). So far, the fast recovery characteristics have been reported in the SiGe/Si/Si pin diodes [1], though the detailed Vf characteristics have not been demonstrated. Moreover, the mechanism has not been well known. In the present paper, we first show Vf-If characteristics and discuss the operation mechanism.

For the present experiment, we have fabricated SiGe/Si/Si pin diodes with the area of 2.2x2.2mm^2 in Yamagata University. The device schematic is shown in Fig.1. As a substrate, we utilized As-doped Si(100) wafers with the resistivity of 0.001Ωcm. In the beginning, we deposited a Si i-layer at the thickness of 20μm on the wafer. The Si layer is slightly doped with P atoms. The doping concentration is in the order of 10^{14}/cm^3. Then the SiGe layer was deposited on the wafer at the thickness of 0.4μm. The Ge content in the SiGe layer is in the range of 0～6%. The SiGe layer is doped with B at the level of 5～10×10^{17}/cm^3. The depositions of Si and SiGe here were performed by chemical vapor deposition (CVD). After the CVD, Al alloy layers were formed on both front- and backside surfaces of the wafer. Then we fabricated mesa structures on the front surface by the wet etching and the photolithography. The mesa structures were diced to each piece. The piece was covered with silicone gel to isolate itself to air. The diodes in the present work have the reverse voltage ratings of 320～370V with the appropriate surface treatment described elsewhere [2].

The recovery characteristics of the SiGe/Si/Si pin diodes are shown in the Fig. 2. The recovery time at the Ge content of 5.5% is lowered to the level of half of those in 3% and 0%. The recovery charge (Qrr) also decreases according to the Trr, which can be clearly seen in Fig. 3. The SiGe p-layer acts to decrease the stored carrier in the diode. What's interesting is little change in Vf characteristics as shown in Fig.4. It is highly possible that the present technique enables the faster switching operation regardless the Vf and Trr trade-off that is inherent in the conventional Si pin diodes with the lifetime control.

The stability in Vf suggests that the conductivity modulation is not lost by the lifetime reduction at all the area in the i-layer. The possible explanation for the short Trr and stable Vf is the selective reduction of lifetime at the SiGe/Si interface and/or the p-SiGe layer. The SiGe layer at 5.5% is in the relaxing condition when the thickness of SiGe is 0.4μm. The dislocation must decrease the lifetime there. It has been also reported elsewhere that the deposited SiGe exhibits two-order lower lifetime due to the oxygen impurity or SiC precipitates [3]. This is one of possible reasons for the reduction of lifetime. The reduced lifetime at the SiGe layer and/or SiGe/Si interface must enhance the diffusion current if the carrier recombination is finite at the metal and p-SiGe interface. If the diode current is stable, the increase of the diffusion current causes the reduction of minority carrier stored in the i-layer. Additionally we are considering another mechanism of carrier transport at the interface. The detailed analysis will be exhibited in the present symposium.

References

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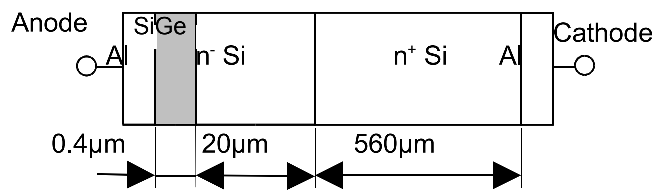

Fig.1 Schematic of the SiGe/Si/Si PIN diode

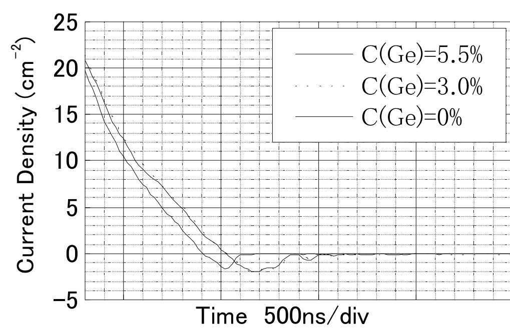

Fig.2 Recovery characteristics of the SiGe diodes

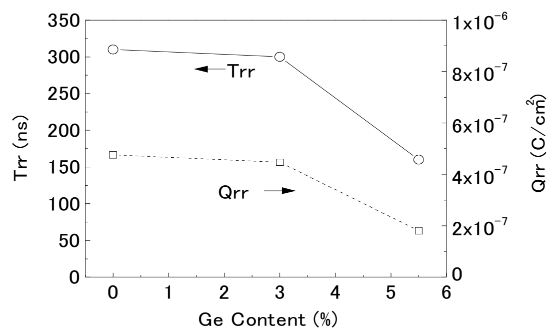

Fig.3 Trr and Qrr of the SiGe diodes

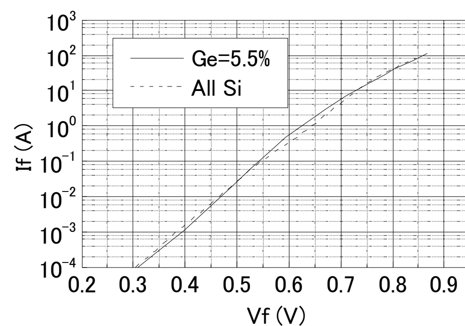

Fig.4 Vf-If characteristics of the SiGe diodes