Effects of Hydrogen Annealing on Heteroepitaxial-Ge layers on Si : Surface Roughness and Electrical Quality

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Recently germanium has emerged as a viable candidate to augment silicon for CMOS and optoelectronic applications [1-3]. However, for Ge to become main-stream, heterogeneous integration of crystalline Ge layers on Si must be achieved. This is not straightforward because of the large lattice mismatch (4%) between Ge and Si, which limits the quality of the heteroepitaxial growth. Such growth is associated with large density of defects and surface roughness, causing difficulties in process integration, such as wafer bonding for Ge-on-insulator (GOI). This can lead to degradation in device properties.

In this work we have studied the surface roughness of Ge films grown by CVD on Si. We grew 200 nm epitaxial germanium layers at 400 °C with reduced pressure of 10 Torr. It has been shown that hydrogen annealing significantly reduces surface roughness of SOI layers comparable to bulk Si wafer control [4]. Following from that previous work, five different hydrogen anneals were carried out for 1 hr immediately following the epitaxial growth, (600 °C, 700 °C, 725 °C, 763 °C, 825 °C), at a pressure of 80 Torr. Surface roughness was evaluated by using a 10 μm × 10 μm AFM scan.

In figure 1 (a)-(b) tilted high resolution SEM cross sections of an un-annealed sample along with the 825°C H_2 annealed sample clearly show a reduction in surface roughness. This effect can also be seen in the topographical AFM images of the samples shown in Figure 1 (c)-(d). In addition, direct plan-view TEM images confirmed the epi-Ge layer is crystalline but has crystal defects due to a 4% lattice mismatch. Figure 2 shows absolute value of RMS roughness (R_{rms}) and change in R_{rms} as a function of H_2 anneal temperature for five different anneals. Surface roughness reduction is clearly seen with an 88% reduction at 825 °C. The change of R_{rms} shows a peak at around 800°C. Further increase in the temperature no longer reduces R_{rms}. This surface smoothing effect is firstly observed in Ge. Inferred from the Si[4] and Pt[5] cases, the effect of attaching H to Ge during the hydrogen annealing, reduces the diffusion barrier for Ge. However, there appears to be an upper limit to the amount of diffusion barrier reduction. In the case of Ge it occurs around 800°C which corresponds to ~70 meV reduction of barrier height. The results indicate that Ge and Si [5] behave similarly when annealed in hydrogen.

The smoother Ge surface enables us to evaluate the electrical quality of the epi-Ge layer. MOS capacitors were fabricated using NH_3 grown GeO_xN_y as the gate dielectric with tungsten gate electrode over Ge epi-layer annealed in hydrogen at 825° C. Electrical quality of both the epi-Ge substrate and the GeO_xN_y/epi-Ge interface was examined using CV measurements. We deduced the CV hysteresis of these MOS capacitors, which is an indicator of the level of interface states (through interface charge trapping) that can eventually degrade the MOSFET mobility. Figure 3 presents bi-directional high frequency CV characteristics measured at 100 kHz and 1 MHz showing negligible hysteresis. From the 100 kHz sweep, however, two kinks are observed near inversion, suggesting the presence of a finite amount of interface states. They originated either at the GeO_xN_y/epi-Ge interface or in the epi-Ge layer. Further improvements in both the interface and epi-Ge layer are certainly required to perfect this material system for future Ge MOS device applications.

This hydrogen annealing technology may lead to subsequent bonding of Ge to Si/SiO_2 needed for the fabrication of GOI substrates using epitaxial Ge.

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References

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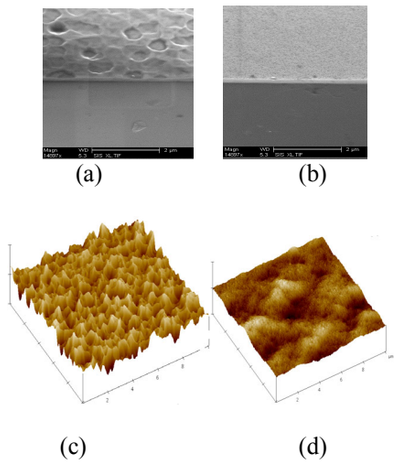

Figure 1. Cross section HR-SEM image of **(a)** No anneal **(b)** 825°C H_2 anneal; Surface AFM image of epi-Ge layer: *(10μm X 10μm)* **(c)**: No anneal, **(d)** 825°C H_2 anneal.

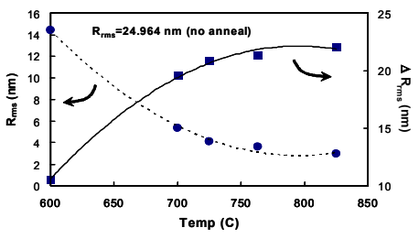

Figure 2 ***(left axis data)*** RMS of epi-Ge layers as a function of hydrogen annealing temp for 1hr measured by AFM. (10μm X 10μm)) ***(right axis solid)*** change in RMS (RMS (No anneal) – RMS (Anneal), vs TEMP *(RMS of the non-annealed sample if 24.94 (nm)* (fitted)

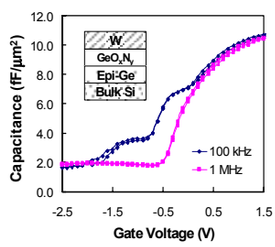

Figure 3. Bi-directional CV characteristics of epi-Ge MOS capacitors with GeO_xN_y gate dielectric and W gate electrode: 100 kHz and 1 MHz.

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