An Innovative Planarization Technology For Ultra High Frequency InP/InGaAs Heterojunction Bipolar Transistor (HBT) Manufacturing

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The increasing demand for ultrahigh frequency device from high-speed electronics industry has driven the advancement of III-V compound semiconductor research and development at a record clip due to its nature of high electron mobility. A great amount of approaches have been brought to the public on how to drive the frequency higher with conventional HBT architecture.[1]

An innovative planarization technology is presented in this paper to demonstrate how it flattens out the complex topography after mesa etch, which presents us a great beneficial platform for designer to scale down base size into sub-mircon region and ensuing process integration.[2]

As detailed through diagrams in Fig1, one layer of PECVD deposited silicon nitride (SiN) is coated on top of topography. Due to the high conformity of nitride step coverage, all the sidewalls of mesa and Ohmic metal stack are well covered by nitride. Then a thick layer of Bisbenocyclobutene (BCB) is spin-coated on top of SiN to make the whole surface flat (as shown in Fig1a). A specially developed BCB/SiN reactive ion etch (RIE) process is developed to etch through BCB layer into SiN layer until the surface of the base ohmic metal stack is exposed for the incoming interlayer connect metal (as shown in Fig1b). The key point of RIE process is to control etching condition at the point of etch rate selectivity of BCB over nitride to be around 1.0, which minimizes any uneven etching between BCB and nitride, and as a result, a flat surface from the top of the as-coated BCB is successfully retained.

Later in the process after base metal connect is finished, a similar planarization process is employed to expose emitter ohmic metal on a flat surface. As a result, the size limitation of emitter imposed by I-Line stepper on complex topography is avoided, and emitter geometry can be significantly scaled down. A sophisticated 4-layer metal interconnect process module can be easily built on top of flat surface. Fig2 shows an SEM cross-section of transistor built with this technology

Fig3 presents the etch rate relationships of both BCB and SiN with O_2 gas flow. RIE is used for this process development. Etching precursors include O_2 and SF_6. Obviously O_2 facilities the etching of polymer based BCB at the same time of limiting the etching of SiN while SF6 flow rate stays constant. A parallel etching between BCB and SiN can be achieved by adjusting etching selectivity appropriately.

This state-of-art planarization technique has successfully demonstrated superior RF performance on transistor with emitter size as small as 0.35um, with unit gain cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) of 290GHz and 426GHz, respectively.

References:

1. *J. C. Zolper, 2003 Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 25th Annual Technical Digest 2003. IEEE , 2003 Pages:3 – 6*
2. *T. Oka et al, IEEE Transactions on Electron Devices, vol. 45, no. 11, pp. 2276-2282, 1998.*

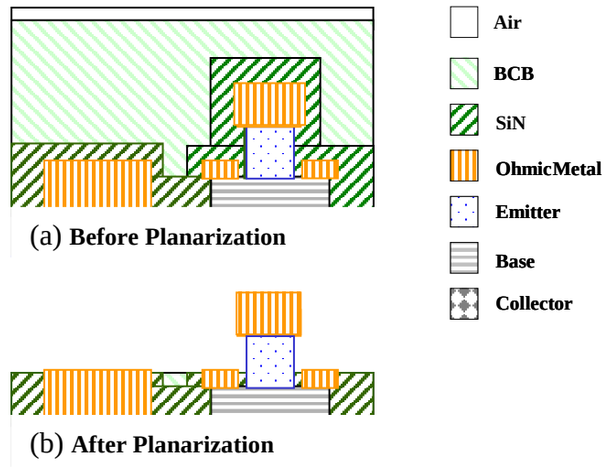

FIG.1. BCB/SiN Planarization Process Flow

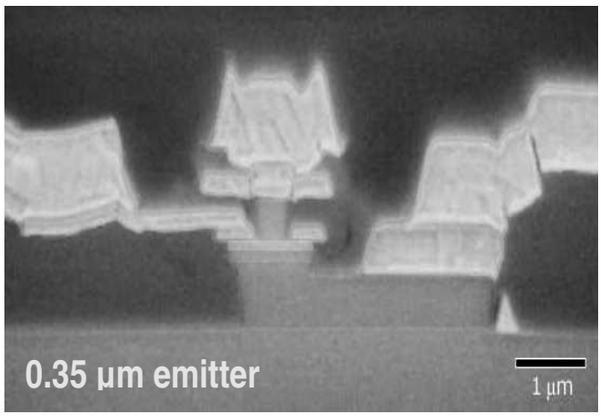

FIG.2. SEM Cross-section of a 0.35□m device

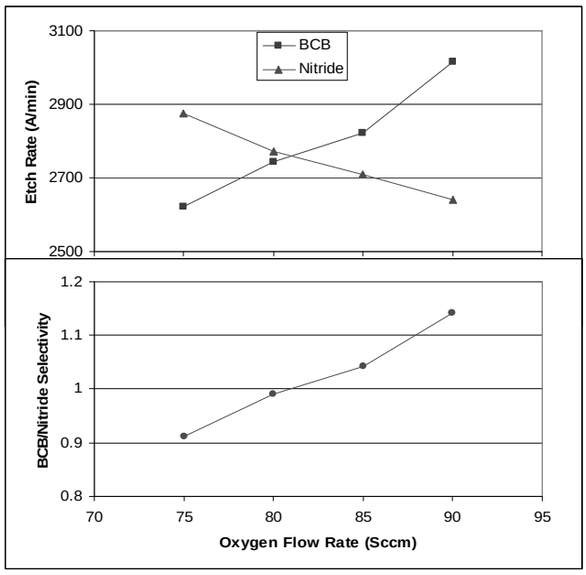

FIG. 3. BCB And Nitride Etch Rates And Selectivity vs O2 Flow Rate. Power=150w; Pressure=300mtorr; SF6=15sccm; Temperature=25C

Work supported by the DARPA TFAST program and by the US Office of Naval Research.

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