Planar Sub-Micron InP/InGaAs Heterojunction Bipolar Transistor

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Performance requirements for future high speed, low power, mixed-signal circuit applications have continued to push the development of InP double heterojunction bipolar transistor (DHBT) device design. Higher frequencies and greater levels of integration will be desirable in next generation architectures. To meet the demands for future high-speed electronics, we have developed a planarized HBT process that is compatible with high-yield advanced interconnect technology needed for the higher level of integration[1]. Along with developing a planar technology, device performance enhancements were also achieved via reduction of the base-collector junction capacitance (C_{BC})[2]. The device fabricated using this new process has achieved excellent RF characteristics, with unity gain cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) of 272 and 430 GHz, respectively.

The InP/InGaAs HBT is grown by solid source molecular beam epitaxy (MBE). Using the planarized fabrication process, the C_{BC} is reduced by minimizing the base-collector junction area. Fig. 1 shows the cross-section of a typical 0.7 µm device. An extrinsic base metal layer buried in dielectric eliminates the base surface area usually needed for the base via, therefore the base-collector junction area is minimized to only optimize base-contact resistance. Another advantage of the planarized process is that it allows device scaling using standard I-line stepper process by eliminating the need to align emitter vias. Device size down to 0.25 µm has being successfully demonstrated using this technology.

The Gummel plot, breakdown, and common emitter IV characteristics of a 0.7×8 µm^2 device are shown in Fig. 2. The current gain (β) is over 30, and the breakdown voltage (BV_{CEO}) is over 5 V. Similar DC characteristics are obtained for devices down to 0.25 µm. The RF performance for various device sizes is summarized in Table I. As shown in Table I, f_T and f_{MAX} of 272 and 430 GHz, respectively, are obtained for the 0.7×8 µm^2 device. The device RF performance peaks at a collector current density (J_C) of around 4.5 KA/cm^2. The C_{BC} value for the 0.7×8 µm^2 device is less than 13 fF. The f_T and f_{MAX} of a 0.25×10 µm^2 device is 205 and 292 GHz, respectively. The smaller devices have lower f_T and f_{MAX} values. This is probably due to the device design geometry that is less optimized for smaller devices, improved designs are needed to enhance the performance of the scaled down devices. Using this technology, we have demonstrated operational divider circuits with multiple-layers of interconnect, as shown in Fig. 3.

We have demonstrated a novel planar sub-micron InP/InGaAs HBT process that allows device scaling down to 0.25 µm using standard high throughput production equipment. Using this technology, high RF performance devices with f_T of 272 GHz and f_{MAX} of 430 GHz has been obtained, and high-speed circuits with compact multiple-layer metal interconnect integration were demonstrated.

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[1]J. C. Zolper, 2003 GaAs IC Symposium, 25th Annual Technical Digest. IEEE, 2003.
[2]A. Gutierrez-Aitken *et al.*, 1999 Electron Devices Meeting, IEDM Technical Digest.

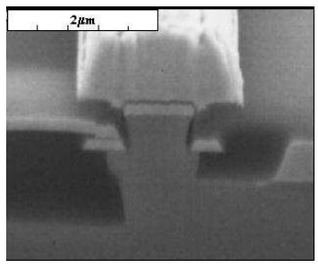

Fig. 1: Cross-section of a 0.7 µm device.

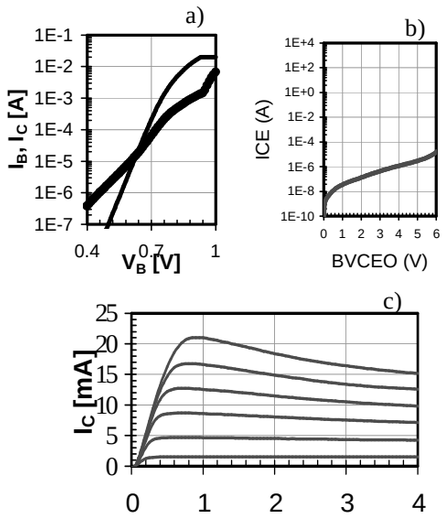

Fig. 2: (a) Gummel plot, (b) BV_{CEO} characteristics, and (c) Common-emitter IV of a 0.7×10 µm^2 device.

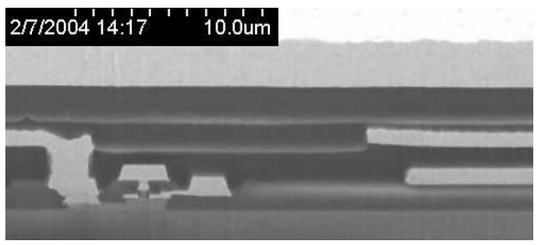

Fig. 3: Cross-section of the planar HBT with a 4 layer interconnect process.

Table I: RF Summary for various device sizes.

Device	f_T [GHz]	f_{MAX} [GHz]
0.7×8 µm^2	272	430
0.5×12 µm^2	262	503
0.25×10 µm^2	205	292