

TABLE OF CONTENTS

<i>Preface</i>	ix
<i>Conference Organization</i>	xi
Section I	1
MOSFET Gate Stack Engineering: Ultrathin Gate Dielectrics	
1.* Enabling Single-Wafer Process Technologies for Reliable Ultra-Thin Gate Dielectrics <i>G. Miner, G. Xing, H.S. Joo, E. Sanchez, Y.Yokota, C. Chen, D. Lopes, and A. Balakrishna</i>	3
2. Evaluation of Ultra-Thin Gate Oxides using Different Ambients in a Rapid Thermal Processing System <i>Y.B. Jia, J.Y. Choi, J. Schuur, J.H. Das, R. Sharangpani, and R.P.S. Thakur</i>	15
3. Dilute Steam Rapid Thermal Oxidation for 30 Å Gate Oxides <i>K.G. Reid, H. Tseng, R. Hegde, G. Miner, and G. Xing</i>	23
4. Preparation of Ultra-Thin Gate Oxides with annealing in Nitric Oxide <i>B. Froeschle, N. Sacher, and F. Glowacki</i>	31
5.* High-k Gate Stack for sub-0.1 μm CMOS Technology <i>G. Bai</i>	39
6.* Recent Developments in Ultrathin Nitride Gate Stack Prepared by In-Situ RTP Multiprocessing for CMOS ULSI <i>S.C. Song, B.Y. Kim, H.F. Luan, D.-L. Kwong, M. Gardner, J. Fulford, D. Wristers, J. Gelpey, and S. Marcus</i>	45
7.* Advanced Gate Dielectrics Synthesized by JVD <i>T.P. Ma</i>	57
8.* Integration of Alternative High-k Gate Dielectrics into Aggressively Scaled CMOS Si Devices: Chemical Bonding Constraints at Si-Dielectric Interfaces <i>G. Lucovsky</i>	69
9. Evaluation of Ultra-Thin Gate Evaluation of Ultra-Thin Gate Stack Dielectrics for 0.1 μm PMOSFETs <i>A. Srivastava, C.M. Osburn, K.F. Yee, H.H. Heinisch, E.M. Vogel, K.Z. Ahmed, Z. Wang, K. Min, B. Timberlake, C. Parker, J.J. Wortman, and J.R. Hauser</i>	81
10. Growth Kinetics and Modeling of Direct Oxynitride Growth with NO-O ₂ Gas Mixtures <i>R. Sharangpani, S.P. Tay, R. Thakur, S. Everist, J. Nelson, and P.M. Smith</i>	89
11. Interfacial Properties of Si-Si ₃ N ₄ Formed by Remote Plasma and Rapid Thermal Processing <i>H. Lazar, V. Misra, Z. Wang, M. Mulkarni, W. Li, M. Mahler, and J.R. Hauser</i>	95

* Invited paper

Section II	103
MOSFET Source/Drain Engineering: Ultrashallow Junctions	
12.* Shallow Junction Formation by Low Energy Implant and High Ramp-Up Rate RTA Process <i>S. Shishiguchi, A. Mineji, T.Y. Matsuda and H. Kitajima</i>	105
13. Spike Anneals in RTP : Kinetic Analysis <i>E.G. Seebauer</i>	117
14. Transient Enhanced Diffusion and Ostwald Ripening of Ion-Implantation Generated Defects in Silicon <i>N.E.B. Cowern, G. Mannino, F. Roozeboom, P.A. Stolk, H.G.A. Huizing, J.G.M. van Berkum, N.N. Toan, P.H. Woerlee, F. Cristiano, and A. Claverie</i>	125
15. Electrical Measurements of Annealed Boron Implants for Shallow Junctions <i>A.T. Fiory, K.K. Bourdelle, M.E. Lefrancois, D.M. Camm, and A. Agarwal</i>	133
16. Influence of Thermal Nitridation on the Diffusion of Arsenic during Rapid Thermal Annealing <i>W. Lerch, N.A. Stolwijk, S.D. Marcus, D.F. Downey, and M. Schäfer</i>	141
17.* Doping and Annealing Requirements to Satisfy the 100 nm Technology Node <i>D.F. Downey, S.B. Felch, and S.W. Falk</i>	151
18. Direct Correlation Between Defects and Thermal Stress in Rapid Thermal Processing <i>V. Parihar, S. Venkataraman, R. Singh, K.F. Poole, and R.P.S. Thakur</i>	163
19. Application of Excimer Laser Annealing in the Formation of Implanted Shallow Junctions <i>L.K. Nanver, E.J.G. Goudena, Q.W. Ren, M. van de Berg, R. Mallee, and J. Slabbekoorn</i>	171
20. Ultra-Shallow P+ -N Junctions for 50-70 nm CMOS Using Selectively Grown In-Situ Boron-Doped Silicon Films <i>I. Ban and M.C. Öztürk</i>	179
21. Shallow Junction Fabrication by Rapid Thermal Outdiffusion from Implanted Oxide <i>J. Schmitz, M. van Gestel, P.A. Stolk, Y.V. Ponomarev, F. Roozeboom, F.N. Cubaynes, J.G.M. van Berkum, W.M. van de Wijgert, P.C. Zalm, and P.H. Woerlee</i>	187
Section III	195
MOSFET Source/Drain Engineering: Metals and Silicides	
22.* RTP for Advanced Device Fabrication using Shallow, Elevated, and Silicided Junctions <i>C.M. Osburn</i>	197
23. Pre-Deposition Treatments for Selective Rapid Thermal Chemical Vapor Deposition of TiSi ₂ on Arsenic-Implanted Silicon Substrates <i>H. Fang, M.C. Öztürk, P.A. O'Neil, and E. Seebauer</i>	207

Section IV	215
MOSFET Source/Drain Engineering: Contacts	
24.* Junction Perimeter Leakage Considerations for the Integration of CoSi ₂ and Damascene W Local Interconnect in Dynamic Logic Compatible, Sub-0.25 μm CMOS Technologies <i>P.D. Agnello</i>	217
25. Influence of Rapid Thermal Ramp Rate on Phase Transformation of Titanium Silicides <i>Y.Z. Hu, S.P. Tay, J. Yang, R. Thakur, P.M. Smith, and G. Bailey</i>	229
26.* Low Resistivity Contacts to Ultra-Shallow Junctions in ULSI Devices <i>L.J. Chen, S.L. Cheng, and L.W. Cheng</i>	237
27. Attainment of Low Resistivity Polycide Films Using Rapid Thermal Annealing <i>H.A. Yoon, C. Chen, A. Singhal, D. Lopes, G. Miner, S. Hong, M. Yamazaki, and Y. Maeda</i>	249
28. Thermal Stability Improvement of Cobalt Disilicide Thin Films on (001)Si by High Temperature Sputtering Deposition <i>H.Y. Huang, L.J. Chen, W.F. Wu, and R.P. Yang</i>	257
Section V	263
Novel Applications	
29. ⁺ Rapid Thermal Processing of High Performance Dielectrics and Silicon Solar Cells <i>A. Rohatgi</i>	265
30. Poly-Si _{1-x} Ge _x Process Integration for Low Resistance Gate CMOS Technology <i>H. Takeuchi and T.-J. King</i>	277
31. Scanning Rapid Thermal Annealing Process for Low Temperature Poly-Silicon Thin Film Transistors <i>T.-K. Kim, G.-B. Kim, Y.-G. Yoon, C.-H. Kim, B.-I. Lee, and S.-K. Joo</i>	285
32. Enhanced Mobility in Buried SiGe Channel PMOS Fabricated using Rapid Thermal Processing <i>D.J. Tweet and S.T. Hsu</i>	291
33. Strain Relaxation of Si/Si _{1-x-y} Ge _x C _y /Si Quantum Wells Grown by RTCVD <i>M.H. Lee, Y.D. Tseng, C.W. Liu and M.Y. Chern</i>	299
Section VI	307
RTCVD and Epitaxy of Si and SiGe	
34.* Emissivity Effects in Low-Temperature Epitaxial Growth of Si and SiGe <i>W.B. de Boer and D. Terpstra</i>	309
35. Suppressed Phosphorus Autodoping in Silicon Epitaxy for Ultrasharp Phosphorus Profiles by Low Temperature Rapid Thermal Chemical Vapor Deposition <i>M. Carroll, M. Yang, and J.C. Sturm</i>	319

36. Comparative Study of Crystallinity and Surface Roughness of RTCVD versus LPCVD Deposited Polysilicon <i>J.W.H. Maes, C. Pomarede, M. Mansoori, C.W. Werkhoven, and I.J. Raaijmakers</i>	327
37. As Peaks in Si (100) Films Fabricated with Rapid Thermal Epitaxy <i>W.D. van Noort, L.K. Nanver, C.C.G. Visser, A. van de Boogaard, and J.W. Slotboom</i>	335
Section VII	343
Equipment & Temperature Issues and Modeling	
38.* Critical Considerations and Integration Issues in the Design of an RTP System <i>A. Gat, Z. Koren, P.J. Timans, and R.P.S. Thakur</i>	345
39.* Temperature Calibration in Microelectronic Manufacturing <i>P. Vandenabeele and W. Renken</i>	359
40. Passive and Active Pyrometry in RTP and RTCVD Systems <i>E.D. Glazman, A.E. Glazman, Z. Atzmon, H. Gilboa, E. Iskevitch, and A. Thon</i>	371
41. Temperature Measurement, Uniformity, and Control in a Furnace-Based Rapid Thermal Processing System <i>J. Hebb and A. Shajii</i>	375
42. Emissivity Compensated Wafer Temperature Measurement Using Intensity-Modulated Lamp Light <i>M. Hauf, H. Balthasar, C. Merkl, S. Müller, and C. Striebel</i>	383
43. Floating Wafer Reactor: RTP Based on Thermal Conductive Heat Transfer <i>V.I. Kuznetsov, S. Radelaar, and E.A.H. Granneman</i>	391
44. Dynamic Uniformity Control in a Rapid Thermal Processing System <i>K.S. Balakrishnan, S. Shooshtarian, N. Acharya, P.J. Timans, and R.P.S. Thakur</i>	399
45.* A Novel Full-Quartz Open Cluster Platform for Advanced Rapid Thermal Processing <i>R. Bremensdorfer, H. Walk, E. Merz, and S. Paul</i>	407
46. Modeling Chamber Radiation Effects on Radiometric Temperature Measurement in Rapid Thermal Processing <i>F. Rosa, Y.H. Zhou, Z.M. Zhang, D.P. DeWitt, and B.K. Tsai</i>	419
47. Emissivity of Bare and Coated Si Wafers: Theoretical Studies <i>B. Sopori, W. Chen, Y. Zhang, J. Madjdpour, and N.M. Ravindra</i>	427
48. An Advanced Radiation Model for Thermal Processing of Wafers <i>S. Mazumder and A. Kersch</i>	435

* *Invited paper*

Section VIII	443
Author Index and Key Word Index	
Author Index	445
Key Word Index	449