

TABLE OF CONTENTS

<i>Preface</i>	<i>iii</i>
<i>Conference organization</i>	<i>iv</i>
Section I	1
Advances in Short-Time Processing	
1. Rapid Thermal Processing and the Engineering of Intrinsic Point Defect Profiles and Silicon Materials Properties <i>R. Falster</i>	3
2.* The Process of Innovation in Batch Furnaces <i>A. Hasper, T. Claasen-Vujcic, and R. Noben</i>	11
3. Rapid Thermal Implant Annealing using Cold Wall and Hot Wall Systems <i>W.S. Yoo, T. Fukada, T. Setokubo, K. Aizawa, J. Yamamoto, and R. Komatsubara</i>	21
4. Extremely Rapid Thermal Processing Using an Intense Hot Gas Stream <i>L.D. Bollinger and J.D. Callahan</i>	29
5.* Thermal Technologies for Sub-100nm CMOS Scaling: Development Strategies <i>P. Meissner, A. Hegedus, J. Madok, R. Thakur and G. Miner</i>	37
6. Low Temperature Borophosphosilicate Glass (BPSG) Process for High Aspect Ratio Gap Fill <i>M. Belyansky, R. Conti, A. Upham, F. Liucci, C. Parks, K.-H. Lee and J. Strane</i>	47
7. Plasma and UV Assisted Rapidcuring TM of Low-K Materials <i>C. Waldfried, A. Margolis, O. Escorcica, Q. Han, R. Albano, and I. Berry</i>	53
8. Selective Oxidation of Silicon (100) versus Tungsten Surfaces by Steam in Hydrogen <i>Y. Liu and J. Hebb</i>	63

* *Invited paper*

Section II	71
Chemical Vapor Deposition in Short-Time Processing Systems	
9.* Manufacturability of SiGe:C and Si Epitaxy for Heterojunction Bipolar Transistors integrated in a BiCMOS Technology <i>B. Tillack, D. Knoll, Y. Yamamoto, B. Heinemann, K.E. Ehwald, W. Winkler, and H. Rücker</i>	73
10. Transient 3-D / 3-D Transport and Reactant-Wafer Interactions: Adsorption and Desorption <i>S.G. Webster, M.K. Gobbert, and T.S. Cale</i>	81
11. Single-Wafer Hot-Wall Rapid Thermal CVD of Silicon Nitride Films for Capacitor and Spacer Applications <i>Y. Senzaki, C. Barelli, J. Sisson, Y. Brichko, D. Teasdale, R. Herring, J.-U. Sachse, A. Morgenschweis, and J. Krujatz</i>	89
Section III	97
MOS Gate Stacks: High-K Dielectrics	
12.* Challenges and Opportunities in High-K Gate Dielectric Technology <i>M. Niwa, Y. Harada, K. Yamamoto, S. Hayashi, R. Mitsuhashi, K. Eriguchi, M. Kubota, Y. Hoshino, Y. Kido, and D.L. Kwong</i>	99
13. Stability of Advanced Gate Stack Devices <i>I. Kim, S.K. Han, and C.M. Osburn</i>	117
14.* High Temperature Stability of High-K Dielectrics: Thermal Processing and Kinetics <i>E.W.A. Young, J. Chen, V. Cosnier, P. Lysagh, J.W. Maes, F. Roozeboom, C. Zhao, R. Carter, O. Richard, and T. Conard</i>	125
15.* Molecular Beam Deposition of Alternate Gate Dielectrics for Si CMOS <i>N.A. Bojarczuk, S. Guha, V. Narayanan, and L.A. Ragnarsson</i>	137
16. Effect of Post Metallization Annealing for Alternative Gate Stack Devices <i>I. Kim, S.K. Han, and C.M. Osburn</i>	145
17. In-line Electrical Metrology for High-K Gate Dielectrics Deposited by Atomic Layer Chemical Vapor Deposition <i>H. De Witte, S. Passefort, W. Besling, J.W.H. Maes, K. Eason, E. Young and M. Heyns</i>	153

* *Invited paper*

Section IV	161
MOS Gate Stacks: Atomic Layer Deposition of High-K Dielectrics	
18.* Process Optimization in Atomic Layer Deposition of High-K Oxides for Advanced Gate Stack Engineering <i>A.R. Londergan, S. Ramanathan, K. Vu, S. Rassiga, R. Hiznay, J. Winkler, H. Velasco, L. Matthyse, T.E. Seidel, C.H. Ang, H.Y. Yu, and M.F. Li</i>	163
19. Nucleation and Growth of ALD HfO ₂ and ZrO ₂ Films, and the Effects of Post-Deposition Annealing on Electrical Properties <i>M.L. Green, T. Conard, B. Brijs, M.-Y. Ho, G.D. Wilk, P.I. Räisänen, T. Sorsch and W. Vandervorst</i>	177
20. Atomic Layer Deposition of ZrO ₂ Thin Films: Study of Growth Kinetics and Dielectric Behaviour <i>A.U. Mane, M.S. Dharmaparakash, A. Chakraborty, V. Venkataraman and S.A. Shivashankar</i>	189
Section V	197
MOS Gate Stacks: MOCVD of High-K Dielectrics	
21.* Novel HfSiON Gate Dielectric for Advanced CMOS Devices <i>L. Colombo, M.R. Visokay, J.J. Chambers, A.L.P. Rotondaro, A. Shanware, M.J. Bevan, H. Bu, and L. Tsung</i>	199
22. Effect of HfO ₂ Deposition on Interfacial Layer Thickness and Roughness <i>F. Chen, R. Smith, S.A. Campbell, and W.L. Gladfelter</i>	207
23. Hf Cross-Contamination in RTCVD System and its Effect on Gate Oxide Integrity <i>J. Jeon, B. Vermeire, H. Parks, S. Raghavan and B. Ogle</i>	215
Section VI	223
MOS Gate Stacks: Alternative Gate Electrode Materials	
24.* NMOS Gate Electrode Selection Process for Advanced Silicon Devices <i>V. Misra, G. Heuss, Y.-S. Suh, H. Zhong, and J.-H. Lee</i>	225
25. Chemical Vapor Deposition of Novel Precursors for Advanced Capacitor Electrodes <i>J. Peck, C.A. Hoover, J.D. Atwood, D.C. Hoth, S. Consiglio, F. Papadatos, and E. Eisenbraun</i>	235

* *Invited paper*

Section VII	243
RTP Equipment: Temperature and Process Control	
26. Reflectance and Transmittance Measurements in a Mock-Up Rapid Thermal Processing Chamber <i>Y.J. Shen, Q.Z. Zhu, Z.M. Zhang, and P.J. Timans</i>	245
27. Correlation between Hot Plate Emissivity and Wafer Temperature at Low Temperatures <i>T. Murakami, T. Fukada, and W.S. Yoo</i>	253
28.* Pattern-Induced Effects in RTP: Still a Hidden World in Production? <i>Z. Nényei, J. Niess, S. Buschbaum, K. Meyer, W. Dietl, R. Berger, S. Miethaner, H. Gruber, R. Wahlich and S. Chamberlain</i>	261
29. Wafer Emissivity Effects on Light Pipe Radiometry in RTP Tools <i>K.G. Kreider, D.H. Chen, D.P. DeWitt, W.A. Kimes, C.W. Meyer, and B.K. Tsai</i>	273
30. Emissivity Dependence of Spike Annealing in Levitor and Lamp-Based Heating Systems <i>E.H.A. Granneman, C. Laviron, A. Halimaoui, R. El Farhane, V.I. Kuznetsov, X. Pages, R. Grisel, and H. Terhorst</i>	281
31.* Wafer Processing in an RTX™ RTP Chamber with Device Side Emissivity Measurement and Temperature Control <i>I. Mahawili, S.J. Lineberry, and A.J. Davio</i>	289
32. Cutting-Edge Temperature Measurement and Control over a Wide Range of Process Temperatures in a 300 mm Hot-Wall RTP System <i>J. Willis and J. Hebb</i>	301
Section VIII	311
Advanced Junctions by Ion Implantation and Thermal Annealing	
33.* Advanced Annealing for Sub-130 nm Junction Formation <i>J.C. Gelpy, K. Elliott, D. Camm, S. McCoy, J. Ross, D.F. Downey, and E.A. Arevalo</i>	313
34. Solutions for Ultra-Shallow Junction - Improvements in Spike Annealing <i>B. Ramachandran, R. Boas, and S. Ramamurthy</i>	325
35. Stability of Ultra-Shallow Junctions Formed by 0.2 keV Boron Implantation and Spike Annealing <i>L. Shao, X. Wang, J. Bennett, L. Larsen, I. Rusakova, H. Chen, J. Liu, and W.-K. Chu</i>	333

* *Invited paper*

36.*	Non-Destructive Thermo-Probe Measurements on Annealed Ultra-Shallow Junction Samples <i>S. Cherekdjan, L. Nicolaidis, and M. Bakshi</i>	339
37.	Point Defect Engineering and its Application in Shallow Junction Formation <i>L. Shao, J.R. Liu, P.E. Thompson, X.M. Wang, I. Rusakova, H. Chen, and W.-K. Chu</i>	351
38.	Measurement of Fermi Pinning at Si-SiO ₂ Interfaces: Implications for TED Spike Anneals <i>K. Dev and E.G. Seebauer</i>	357
39.	Measurement of Nonthermal Illumination-Enhanced Diffusion in Silicon <i>M.Y.L. Jung and E.G. Seebauer</i>	363
	Section IX	369
	Alternative CMOS Source Drain Junction Technologies	
40.	A Study of Boron Diffusion from Selectively Grown Epitaxial Silicon-Germanium into Silicon During Rapid Thermal Annealing <i>T.H. Yang, E.Y. Chang, K.M. Chen, C.H. Chien, H.J. Huang, T.Y. Yang, and C.Y. Chang</i>	371
41.	Ultra-Shallow Junctions in Si _{1-x} Ge _x Formed by Molecular-Beam Epitaxy <i>P.E. Thompson and J. Bennett</i>	381
42.*	Ultra Shallow Junctions for Sub 0.1 Micron Technologies and Beyond <i>M.M. Mansoori, A. Jain, D.E. Mercer, L. Robertson, and P. Kohli</i>	389
43.	Effects of Cl ₂ on In-Situ Boron Doped Si _{1-x} Ge _x Alloys <i>N. Pesovic and M. C. Öztürk</i>	407
44.*	Laser Annealing for Ultra-Shallow Junction Formation in Advanced CMOS <i>R. Surdeanu, Y.V. Ponomarev, R. Cerutti, B.J. Pawlak, L.K. Nanver, I. Hoflijk, P.A. Stolk, C.J.J. Dachs, M.A. Verheijen, M. Kaiser, M.J.P. Hopstaken, J.G.M. van Berkum, F. Roozeboom, R. Lindsay</i>	413

* *Invited paper*

Section X	427
New Contact Technologies for Advanced CMOS	
45.* Challenges for Integration of Source-Drain Contacts into Emerging Future Generation CMOS Devices <i>R.A. Roy</i>	429
46.* Rapid Thermal Silicidation in Silicon-Germanium and SOI Devices <i>L.J. Chen, W.W. Wu, C.H. Liu, T.F. Chiang, S.L. Cheng and S.W. Lee</i>	441
47.* <i>In Situ</i> Monitoring of Thin Film Reactions During Rapid Thermal Annealing: Nickel Silicide Formation <i>C. Lavoie, R. Purtell, C. Coia, C. Detavernier, P. Desjardins, J. Jordan-Sweet, C. Cabral, Jr., F.M. d'Heurle, and J.M.E. Harper.</i>	455
Section XI	469
Author Index and Key Word Index	
Author Index	471
Key Word Index	475

* *Invited paper*