

TABLE OF CONTENTS

PREFACE	iii
<u>VOLUME 1</u>	
<u>CHAPTER 1 -- PLENARY SESSION: ITRS UPDATE AND GLOBAL CONSORTIA</u>	1
INTRODUCTORY REMARKS - ITRS UPDATE AND GLOBAL CONSORTIA H. R. Huff, L. Fabry, and S. Kishino	3
INVITED: THE 2002 INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS) P. Gargini	5
INVITED: REALIZING THE FUTURE FOR THE SEMICONDUCTOR INDUSTRY-MEETING THE CHALLENGES OF PROCESS, DESIGN, AND BUSINESS C. M. Melliar-Smith and C. R. Helms	20
INVITED: ESTABLISHMENT OF A DEVICE PROCESS PLATFORM FOR REALIZING A LEADING-EDGE SYSTEM-ON-A-CHIP A. Morino	38
INVITED: IMEC'S RESEARCH PROGRAM AND THE ITRS CHALLENGES G. J. Declerck	52
INVITED: FOUNDRY TECHNOLOGY IN SOC ERA S.Y. Chiang	67
INVITED: MIRAI PROJECT M. Hirose	82
INVITED: CHINA'S SEMICONDUCTOR INDUSTRY AND THE GLOBAL IC ENVIRONMENT H. Tu	97

INVITED: WAYS OF COOPERATION IN THE FIELD OF THE SILICON TECHNOLOGY M. Brillouët	111
LONG-TERM PRODUCTIVITY MECHANISMS OF THE SEMICONDUCTOR INDUSTRY R. Goodall, D. Fandel, A. Allan, P. Landler and H. R. Huff	125
<u>CHAPTER TWO -- SILICON MATERIALS: 300 mm</u>	145
INTRODUCTORY REMARKS - SILICON MATERIALS: 300 mm W. von Ammon and T. Shigematsu	147
INVITED: CONTROL OF POINT DEFECTS, IMPURITIES, AND EXTENDED DEFECTS IN CZ Si: THE ORIGINAL/ONGOING SILICON NANOSCALE ENGINEERING DEFECT SCIENCE G. A. Rozgonyi	149
INVITED: SUPER SILICON INITIATIVE AND FUTURE LARGE WAFER SIZE DIAMETERS M. Kuramoto	163
INVITED: 300 MM SUBSTRATE REQUIREMENTS FOR ADVANCED DRAM TECHNOLOGIES H. Dietrich, C. Kupfer, J. Martin and F. Katzwinkel	176
GROWTH OF 300 mm SILICON SINGLE CRYSTALS IN A 24" HOT ZONE H. Tu, X. Dai, Z. Wu, G. Zhang, J. Wang, F. Fang, Q. Zhou and Q. Xiao	182
STUDY ON GEOMETRY, SURFACE DAMAGE AND RAPID THERMAL ANNEALING OF 300 mm AS-CUT SILICON WAFERS G. Zhang, B. Liu, J. Zhao, W. Chen, J. Wang, Q. Zhou and H. Tu	189
ARGON-ANNEALED 300 mm WAFERS COMPLEMENTING PP- EPITAXIAL LAYERS T. Müller, W. Siebert, K. Messmann, R. Wahlich, P. Krottenthaler R. Hölzl, A. Ikari and W. von Ammon	194

<u>CHAPTER THREE -- SILICON MATERIALS: GENERIC ISSUES</u>	207
INTRODUCTORY REMARKS - SILICON MATERIALS: GENERIC ISSUES W. von Ammon and T. Shigematsu	209
INVITED: THERMOPHYSICAL PROPERTIES OF INTRINSIC POINT DEFECTS IN CRYSTALLINE SILICON T. Sinno	212
DEFECTS IN SILICON CRYSTALS AND THEIR IMPACT ON TRENCH CAPACITOR DRAM DEVICE CHARACTERISTICS E. Dornberger, D. Temmler and W. von Ammon	227
FRACTIONAL CONTRIBUTION IN Si SELF-DIFFUSION: DOPANT CONCENTRATION AND TEMPERATURE DEPENDENCE ON Si SELF-DIFFUSION MECHANISM Y. Nakabayashi, H. I. Osman, K. Toyonaga, K. Yokota, S. Matsumoto, J. Murota, K. Wada and T. Abe	241
EFFECT OF VACANCY DOUBLE ACCEPTOR LEVEL ON Si SELF DIFFUSION UNDER HEAVY DOPING CONDITION H. I. Osman, Y. Nakabayashi, S. Tomohisa, K. Toyonaga, S. Matsumoto, J. Murota, K. Wada and T. Abe	248
WAFERS WITH LOW LPD AND REDUCED HAZE PREPARED BY SHORT ANNEALING PROCESS J. L. Vasat, A. D. Stefanescu, T. Torack and R. Orizio	254
OXIDATION-INDUCED STACKING FAULTS IN NITROGEN DOPED CZOCHRALSKI SILICON D. Yang, J. Chu, X. Ma, L. Li and D. Que	273
IMPACT OF NITROGEN DOPING IN SILICON ONTO GATE OXIDE INTEGRITY A. Huber, M. Kapser, J. Grabmeier, U. Lambert, W. v. Ammon and R. Pech	280

ATOMIC-LAYER DOPING OF N IN Si EPITAXIAL GROWTH ON Si(100) AND ITS THERMAL STABILITY Y. Jeong, M. Sakuraba, T. Matsuura and J. Murota	287
A TECHNIQUE FOR DELINEATING DEFECTS IN SILICON L. Mule'Stagno	297
GROWTH TECHNOLOGY FOR 200 mm ANTIMONY HEAVILY DOPED SILICON SINGLE CRYSTALS Q. Zhou, F. Qin, J. Zhou, F. Fang, J. Wang and H. Tu	307
SILICON EPITAXY AND PARTICLE DYNAMICS: A THEORETICAL AND EXPERIMENTAL STUDY S. Kommu	311
<u>CHAPTER 4 -- ALTERNATIVE MATERIALS AND IC PROCESS TECHNOLOGIES</u>	323
INTRODUCTORY REMARKS -- ALTERNATIVE MATERIALS AND IC PROCESS TECHNOLOGIES H. Iwai and W. Maszara	325
INVITED: ELECTRONIC DIVISION AWARD ADDRESS: SOI TECHNOLOGY: THE FUTURE WILL NOT SCALE DOWN S. Cristoloveanu	328
INVITED: SiGeC DEVICE APPLICATIONS H. J. Osten	342
INVITED: NiSi SALICIDE FOR SUB-100nm CMOS Q. Xiang	354
INVITED: CURRENT AND FUTURE HIGH-K CAPACITOR TECHNOLOGY FOR DRAM APPLICATIONS K. Hieda	362
RARE EARTH METAL OXIDES FOR HIGH-K GATE INSULATOR S. Ohmi, S. Akama, A. Kikuchi, I. Kashiwagi, C. Ohshima, J. Taguchi, H. Yamamoto, K. Sato, M. Takeda, H. Ishiwara and H. Iwai	376

ELECTRONIC STRUCTURE OF NON-CRYSTALLINE HIGH-K TRANSITION METAL AND RARE EARTH OXIDES AND THEIR SILICATE AND ALUMINATE ALLOYS	388
Y. Zhang, G. Lucovsky, G. B. Rayner, G. Appel, H. Ade and J. L. Whitten	
INTERPRETATION OF NON-LINEAR SHIFTS IN XPS/AES FEATURES IN NON-CRYSTALLINE ZIRCONIUM SILICATE ALLOYS	413
G. B. Rayner, Jr., D. Kang, M. Schultz, K. Mai and G. Lucovsky	
INTERFACE REACTIONS DURING OXYGEN PLASMA ASSISTED CHEMICAL VAPOR DEPOSITION OF YTTRIUM OXIDE ON SILICON	429
D. Niu, R. W. Ashcraft, S. Stemmer and G. N. Parsons	
STUDY OF DIFFUSIVITY AND ELECTRICAL PROPERTIES OF Zr AND Hf IN SILICON	440
O. F. Vyvenko, R. Sachdeva, A. A. Istratov, R. Armitage, E. R. Weber, P. N. K. Deenapanray, C. Jagadish, Y. Gao and H. R. Huff	
<u>VOLUME 2</u>	
<u>CHAPTER 5 -- PROCESS MODELING</u>	453
INTRODUCTORY REMARKS -- PROCESS MODELING	455
P. Mertens and H. Richter	
INVITED: PHYSICAL MODELS OF ULTRA-THIN OXIDE RELIABILITY AND IMPLICATIONS FOR CMOS CIRCUITS	458
J. H. Stathis	
INVITED: LOW VOLTAGE GATE DIELECTRIC RELIABILITY	465
B. E. Weir, M. A. Alam, P. J. Silverman and Y. Ma	
INVITED: ELECTRIC STRESS-INDUCED DEGRADATION OF THIN OXIDE LAYERS AND ITS IMPACT ON DEVICE RELIABILITY	475
R. Degraeve, B. Kaczer, Ph. Roussel and G. Groeseneken	

<p>INVITED: SIMULATION OF CRYSTAL PULLING AND COMPARISON TO EXPERIMENTAL ANALYSIS OF THE CZ-PROCESS G. Müller, O. Gräbner and D. Vizman</p>	489
<p>GROWN-IN MICRODEFECT DISTRIBUTION IN DOPED SILICON CRYSTALS G. Borionetti, D. Gambaro, M. Porrini and V. V. Voronkov</p>	505
<p>CALCULATION OF SIZE DISTRIBUTION OF VOID DEFECT IN CZOCHRALSKI SILICON M. Akatsuka, M. Okui, S. Umeno and K. Sueoka</p>	517
<p>MODELLING OF CRYSTAL ORIGINATED PARTICLES AND THEIR IMPACT ON GATE OXIDE INTEGRITY T. Bearda, P. W. Mertens, P. H. Woerlee, H. Wallinga, R. Schmolke and M. Heyns</p>	528
<p>COMPUTER SIMULATION FOR MORPHOLOGY, SIZE AND DENSITY OF OXIDE PRECIPITATES IN CZOCHRALSKI SILICON K. Sueoka, M. Akatsuka, M. Okui and H. Katahama</p>	540
<p>SIMULATION OF THE POINT DEFECT DIFFUSION AND GROWTH CONDITION FOR DEFECT FREE CZ SILICON CRYSTAL K. Nakamura, T. Saishoji and J. Tomioka</p>	554
<p>MODELING OF SiGe EPITAXIAL GROWTH IN A WIDE RANGE OF GROWTH CONDITIONS A. Segal, A. P. Sid'ko, S. Yu. Karpov and Yu. N. Makarov</p>	567
<p>INVITED: UNIFIED THEORY OF THERMAL SILICON OXIDE GROWTH M. Uematsu, H. Kageshima and K. Shiraishi</p>	578
<p>INVITED: CHARACTERIZATION OF THE MECHANICAL STRESS MOS TECHNOLOGY INDUCED DURING SILICIDATION IN SUB- 0.25 μm MOS TECHNOLOGY A. Steegen</p>	592

INVITED: GETTERING EFFICIENCIES AND THEIR DEPENDENCE ON MATERIAL PARAMETERS AND THERMAL PROCESS: HOW CAN THIS BE MODELED? R. Hoelzl, M. Blietz, L. Fabry and R. Schmolke	608
MODELING OF COMPETITIVE GETTERING BETWEEN DEVICES AND GETTERING SITES A. A. Istratov, W. Huber and E. R. Weber	626
DETERMINATION OF MINIMUM OXYGEN PRECIPITATE GROWTH CONDITIONS FOR GETTERING OF COPPER AND NICKEL M. Seacrist, M. Stinson, J. Libbert, R. Standley and J. Binns	638
EFFECTIVE INTRINSIC GETTERING FOR 200 mm AND 300 mm P/P- WAFERS IN LOW THERMAL BUDGET 0.13 μm ADVANCED CMOS LOGIC PROCESS M. J. Binns, S. Bertolini, R. Wise, D. J. Myers and T. A. McKenna	647
BULK MICRO DEFECTS OF P/P- EPITAXIAL SILICON WITH WAFERS WITH NITROGEN DOPED SUBSTRATES AND THEIR GETTERING BEHAVIOR R. Schmolke, M. Blietz, R. Hölzl, D. Menzel and H. Bender	658
FIRST PRINCIPLE CALCULATIONS FOR NITROGEN- VACANCY RELATED DEFECTS IN NITROGEN DOPED SILICON; STRUCTURE, ENERGETICS AND THERMAL STABILITY A. Karoui, F. S. Karoui, G. A. Rozgonyi, M. Hourai and K. Sueoka	670
THE CONTROL OF BORON AUTO-DOPING DURING DEVICE PROCESSING FOR P/P+ EPI WAFERS WITH NO BACK-SURFACE OXIDE SEAL M. J. Binns, S. Kommu, M. R. Seacrist, R. W. Standley, R. Wise, D. J. Myers, D. Tisserand and D. Doyle	682

IMPACT OF STATE-OF-THE-ART Cz SUBSTRATES ON THE CURRENT-VOLTAGE CHARACTERISTICS OF SHALLOW p-n JUNCTIONS A. Poyai, E. Simoen, C. Claeys, A. Huber, D. Gräf and E. Gaubas	694
<u>CHAPTER 6 -- PROCESS INTEGRATION</u>	
INTRODUCTORY REMARKS - PROCESS INTEGRATION P. Tobin and S. Deleonibus	707
INVITED: INVENTION OF STACKED CAPACITOR DRAM CELL M. Koyanagi	711
INVITED: CMOS TECHNOLOGY ROADMAP APPROACHING UP HILL SPECIALS T. Skotnicki and F. Boeuf	720
INVITED: THE HIGH K CHALLENGES IN CMOS ADVANCED GATE DIELECTRIC PROCESS INTEGRATION E. WA Young	735
INTEGRATION ISSUES OF POLYSILICON WITH HIGH K DIELECTRICS DEPOSITED BY ATOMIC LAYER CHEMICAL VAPOR DEPOSITION W. Tsai, J. Chen, R. Carter, E. Cartier, J. Kluth, O. Richard, M. Claes Y. M. Lin, H. Nohira, T. Conard, M. Caymax, E. Young, W. Vandervorst, S. DeGendt, M. Heyns, Y. Manabe, J. W. Maes, Z. M. Rittersma, W. Besling and F. Roozeboom	747
INVITED: A NEW JUNCTION TECHNOLOGY BASED ON SELECTIVE CVD OF SiGe ALLOYS FOR CMOS TECHNOLOGY NODES BEYOND 30 nm M. C. Öztürk, N. Pesovic, J. Liu, H. Mo, I. Kang and S. Gannavaram	761
AVOIDING FURNACE SLIP IN THE ERA OF SHALLOW TRENCH ISOLATION A. E. Stephens	774

EFFECTIVE INTRINSIC GETTERING OF COPPER DURING A SUB-QUARTER MICRON CMOS PROCESS K-M. Bae, J-R. Kim, Y-K. Hong, S-I. So, S-C. Lee, S-S. Kim, S-W. Ha, C-G. Koh, S-H. Pyi and D-M. Lee	786
DAMASCENE METAL GATE FOR 70 nm CMOS PROCESS B. Guillaumot, F. Ducroquet, T. Ernst, G. Guegan, C. Galon, C. Renard, B. Prévitali, M. Rivoire, M. E. Nier, S. Tedesco, T. Fargeot, H. Achard and S. Deleonibus	793
EFFECT OF WAFER BACKSIDE CLEAN PROCESS ON THE ULSI LITHOGRAPHY N. Balasubramanian, M-M. Roy, Pauline H. G. and F. P. Dow	803
<u>CHAPTER 7 -- INTEGRATED METROLOGY AND DIAGNOSTICS</u>	811
INTRODUCTORY REMARKS - INTEGRATED METROLOGY AND DIAGNOSTICS A. C. Diebold and H. Koyama	813
INVITED: CHARACTERIZATION OF SOI WAFERS BY PHOTOLUMINESCENCE M. Tajima and S. Ibuka	815
CHARACTERIZATION OF SOI WAFERS BY CROSS-SECTIONAL SCANNING PROBE MICROSCOPY T. Uchihashi, Y. Ishizuka, H. Yoshida and S. Kishino	829
INVITED: DEFECT MANAGEMENT AND YIELD ENHANCEMENT FOR THE SEMICONDUCTOR INDUSTRY M. H. Bennett	839
INVITED: INTEGRATED METROLOGY AND ADVANCED PROCESS CONTROL IN SEMICONDUCTOR MANUFACTURING A. P. Shanmugasundram, M. Sarfaty, A. Schwarm and J. Paik	850

EVALUATION TECHNOLOGY FOR TIME-DEPENDENT ORGANIC CONTAMINATION ON SILICON WAFER SURFACES H. Habuka, S. Ishiwari and H. Kato	863
INVITED: MEASUREMENT OF NITROGEN CONCENTRATION IN CZ SILICON N. Inoue, K. Shingu and K. Masumoto	875
EXPERIMENTAL METHOD TO DETERMINE AN ACCEPTABLE CONCENTRATION OF IRON IMPURITY IN HOT ZONE STRUCTURAL COMPONENTS H. Sreedharamurthy, M. Seacrist, H. Holder and M. Banan	889
EFFECT OF OXIDE THICKNESS ON DIELECTRIC BREAKDOWN INDUCED BY SURFACE COP K. Yamabe, Y. Shimada, M. Piao, T. Yamazaki, T. Otsuki R. Takeda, Y. Ohta, S. Jimbo and M. Watanabe	898
MICROROUGHNESS ANALYSIS OF SILICON WAFERS USING ULTRAVIOLET RAMAN MICROSCOPY J. Wang, H. Tu, B. Liu, Q. Zhou and W. Zhu	906
THE BEHAVIOUR OF OXYGEN IN OXYGENATED N-TYPE HIGH-RESISTIVITY FLOAT-ZONE SILICON E. Simoen, C. Claeys, R. Job, A. G. Ulyashin, W. R. Fahrner, G. Tonelli, O. Degryse and P. Clauws	912
<u>CHAPTER 8 -- ULTIMATE SILICON AND END-OF-ROADMAP DEVICES</u>	925
INTRODUCTIORY REMARKS -- ULTIMATE SILICON AND END-OF- ROADMAP S. Hillenius and S. Ishihara	927
INVITED: 50 nm VERTICAL REPLACEMENT-GATE (VRG) nMOSFETS WITH ALD HfO ₂ GATE DIELECTRICS J. M. Hergenrother, T. Nigam, G. D. Wilk, F. P. Klemens, D. Monroe, T. W. Sorsch, B. Busch, M. L. Green, D. A. Muller, P. M. Voyles, J. L., Grazul, E. J. Shero, M. E. Givens, C. Pomarede, M. Mazanec and C. Werkhoven	929

INVITED: ELECTRICAL PROPERTIES OF NANOMETER-SCALE MOSFETS H. Kawaura and T. Sakamoto	943
INTERBAND TUNNELING-BASED ULSI-COMPATIBLE SILICON DEVICES A. Zaslavsky, D. Mariolle, S. Deleonibus, D. Fraboulet, S. Luryi, J. Liu, C. Aydin, M. Mastrapasqua, C. A. King and R. W. Johnson	956
INVITED: SILICON SINGLE-ELECTRON TRANSISTORS AND THEIR APPLICATIONS TO LOGIC CIRCUITS Y. Takahashi, Y. Ono, A. Fujiwara and H. Inokawa	968
INVITED: SINGLE-ELECTRON AND NANOSCOPIC DEVICE EVOLUTION F. Kreupl	979
INVITED: BOTTOM-UP APPROACH IN Si TECHNOLOGY BASED ON SURFACE STRUCTURE DESIGN T. Ogino, Y. Homma, Y. Kobayashi, H. Hibino, K. Prabhakaran, K. Sumitomo, H. Omi, D. Bottomley, A. Kaneko and F. Ling	992

APPENDICES

APPENDIX 1 - AN ELECTRONICS DIVISION RETROSPECTIVE -- AND FUTURE OPPORTUNITIES IN THE TWENTY-FIRST CENTURY H. R. Huff	1005
APPENDIX 2 - AUTHOR INDEX	1059
APPENDIX 3 - SUBJECT INDEX	1063