

## TABLE OF CONTENTS

|  |            |
|--|------------|
| <i>Preface</i>   | <i>iii</i> |
| <i>Conference organization</i>   | <i>iv</i>  |
| <b>Section I</b>   | <b>1</b>   |
| <b>Ultra-Shallow Source/Drain Junctions</b>  |            |
| 1 Ultra-Shallow Junction Implant Anneal Using Xenon Arc Flash Lamps<br><i>W.S. Yoo and K. Kang</i>   | 3          |
| 2 Fundamental Issues in Millisecond Annealing<br><i>N. Acharya and P.J. Timans</i>   | 11         |
| 3 Radiative Properties of Silicon Considering Surface Imperfections and Chamber Effects<br><i>Z.M. Zhang and H.J. Lee (Invited Paper)</i>  | 19         |
| 4 Optimization of Pre-Amorphization and Dopant Implant Conditions for Advanced Annealing<br><i>S.B. Felch, H. Graoui and A. Mayur</i>  | 31         |
| 5 Application of Ultra-rapid Thermal Annealing for Electrical Activation for Next Generation MOSFETs<br><i>K. Suguro, T. Ito, K. Nishinohara, K. Matsuo, T. Iinuma, H. Itokawa and Y. Kawase (Invited Paper)</i>                       | 39         |
| 6 Defect Behavior and Control in Advanced CMOS Process Technologies<br><i>C. Claeys and E. Simoen (Electronic Division Medal Award Paper)</i>  | 50         |
| 7 Influence of Surface Chemistry on Ultrashallow Junction Formation<br><i>K. Dev and E.G. Seebauer</i>   | 66         |
| 8 Sub-30 nm Abrupt Junction Formation in Strained Si/Si <sub>1-x</sub> Ge <sub>x</sub> CMOS Device<br><i>K.L. Lee, F. Cardone, P. Saunders, P. Kozlowski, P. Ronsheim, H. Zhu, J. Li, J. Chu, K. Chan and M. Jeong (Invited Paper)</i> | 71         |
| 9 Stability of Shallow Junctions: Issue and Solution<br><i>L. Shao, P.E. Thompson, X.M. Wang, H. Chen, J.R. Liu, and W.-K. Chu</i>   | 82         |

|    |  |     |
|----|--|-----|
| 10 | Solid Phase Epitaxy- Activation and Deactivation of Boron in Ultra-Shallow Junctions<br><i>W. Lerch, S. Paul, J. Niess, F. Cristiano, Y. Lamrani, P. Calvo, N. Cherkashin, D.F. Downey and E.A. Arevalo (Invited Paper)</i>                | 90  |
| 11 | Ultra Shallow p <sup>+</sup> /n Junctions Fabricated by Plasma Doping and All Solid State Laser Annealing<br><i>K. Tsutsui, Y. Sasaki, C.-G. Jin, H. Tamura, B. Mizuno, R. Higaki, T. Sato, K. Majima, S.-I. Ohmi and H. Iwai</i>          | 106 |
| 12 | Structure and Dynamics of Si Interstitials at Si(001) and Si(001)/SiO <sub>2</sub><br><i>T.A. Kirichenko, D. Yu, S.K. Banerjee and G.S. Hwang</i>  | 112 |
| 13 | Interaction between Interstitials and Arsenic-Vacancy Complexes in Crystalline Silicon<br><i>S. A. Harrison, T. F. Edgar and G. S. Hwang</i>   | 120 |
| 14 | Gate-Source /Drain Extension Overlap Control with Angled Implants: TCAD Modeling Study<br><i>S. Thirupapuliyur, A. Al-Bayati, A. Jain and A. Mayur</i>   | 127 |
| 15 | Significant Improvement in Device Performance of Advanced Dynamic Random Access Memory by Hot Wall-Based Single Wafer Rapid Thermal Annealing<br><i>T. Setokubo, E. Nakano, K. Aizawa, H. Miyoshi, J. Yamamoto, T. Fukada and W.S. Yoo</i> | 135 |
| 16 | Integration of Low and High Temperature Junction Anneals for 45 nm CMOS<br><i>R. Lindsay, B. Pawlak, K. Henson, A. Satta, S. Severi, A. Lauwers, R. Surdeanu, S. McCoy, J. Gelpey, X. Pages and K. Maex (Invited Paper)</i>                | 145 |
|    | <b>Section II</b>  | 157 |
|    | <b>Silicide Contacts to Ultra-Shallow Junctions</b>  |     |
| 17 | Nickel SALICIDE Technology for Sub-100 nm CMOS Devices<br><i>J.P. Lu, D. Miles, A. Li-Fatou, Y.Q. Xu, J. Zhao, A. Gurba, A. Griffin, Jr., B. Hornug, M. Hewson, T. Grider, D. Mercer and C. Montgomery (Invited Paper)</i>                 | 159 |
| 18 | The Effect of Ramp Rate - Short Process Time and Partial Reactions on Cobalt and Nickel Silicide Formation<br><i>X. Pagès, K. van der Jeugd, V. Kuznetsov, E. Granneman, A. Lauwers and R. Lindsay</i>                                     | 174 |

|  |  |     |
|--|--|-----|
| 19   | Formation and Characterization of NiSi-Silicided n <sup>+</sup> -p Shallow Junctions Using Implantation Through Silicide and Low Temperature Furnace Annealing<br><i>C.-C. Wang and M.-C. Chen</i>   | 183 |
| 20   | Optimized Nickel Silicide Formation Process for High Performance Sub-65nm CMOS Nodes<br><i>B. Froment and V. Carron</i>  | 191 |
| <b>Section III</b>   |  | 203 |
| <b>Advanced Gate Stacks I: Oxynitrides and Polysilicon Gate Electrodes</b> |  |     |
| 21   | Reduced Poly-Si Gate Depletion Effect by Pulsed Excimer Laser Annealing<br><i>H.Y. Wong, H. Takeuchi, T.-J. King, M. Ameen and A. Agarwal (Invited Paper)</i>  | 205 |
| 22   | Ultra-Thin Silicon Oxynitride Gate-Dielectric Made by ECR Plasmas<br><i>G.A. Manera, J.A. Diniz, I. Doi and J.W. Swart</i>   | 216 |
| 23   | Characterization of Silicon Nitride Films for the Thin Film Transistor Gate Dielectric<br><i>S. Abbasi, H. Abu-Safe, H. Naseem and W. Brown</i>  | 222 |
| 24   | Laser Anneal Technology for Enhancement of Poly-Silicon Dopant Activation<br><i>Y. Ma, K.Z. Ahmed, K.L. Cunningham, C.S. Olsen, T.Y.B. Leung, R.C. Mcintosh, A.J. Mayur, H. Liang, M. Yam, M. Castle, S. Muthukrishnan, P.M. Liu, M. Foad, G.E. Miner and G.S. Higashi</i>       | 230 |
| 25   | Further Optimization of Plasma Nitridation of Ultra-thin Oxides for 65 nm Node MOSFETs<br><i>P.A. Kraus, T.C. Chua, A. Rothschild, F.N. Cubaynes, A. Veloso, S. Mertens, L. Date, T.M. Bauer, K.Z. Ahmed, J. Campbell, F. Nouri, J. Cruse, R. Schreutelkamp and M. Schaekers</i> | 236 |
| 26   | Enhancement of Manufacturability in Polycrystalline Silicon Process by Using Disilane Precursor at 65nm CMOS Technology<br><i>Y. Chen, H. Bu, K. Cunningham, B. Spicer and S. Wang</i>   | 244 |

|  |     |
|--|-----|
| <b>Section IV</b>  | 253 |
| <b>Advanced Gate Stacks II: High-k Gate Dielectrics and Metal Gate Electrodes</b>  |     |
| 27 Band Alignment Issues in Metal/Dielectric Stacks: A Combined Photoemission and Inverse Photoemission Study of the HfO <sub>2</sub> /Pt and HfO <sub>2</sub> /Hf Systems<br><i>S. Sayan, R.A. Bartynski, J. Robertson, J.S. Suehle, E. Vogel, N.V. Nguyen, J. Ehrstein, J.J. Kopanski, S. Suzer, M. B. Holl and E. Garfunkel (Invited Paper)</i> | 255 |
| 28 A Novel Atomic Layer Deposition Process to Deposit Hafnium Silicate Thin Films<br><i>Y. Senzaki, M. Park, L. Bartholomew, and H. Chatham</i>  | 264 |
| 29 Recent Progress in Gate Dielectric Scaling<br><i>G. Higashi, P. Kraus, T.C. Chua, C. Olsen, K. Ahmed, F. Nouri, S.S. Kher, R. Sharangpani, P. Deaton, E.J. Ulloa, G. Tevatia and P.K. Narwankar (Invited Paper)</i>   | 271 |
| 30 Hafnium Titanate as a High-k Gate Insulator<br><i>F. Chen, M. Li, V. Afanasev, W. Gladfelter, and S. Campbell</i>   | 278 |
| 31 Electrical Characterization of HfO <sub>x</sub> N <sub>y</sub> Gate Dielectric with Different Nitrogen Concentration Profiles Formed by Rapid Thermal Annealing<br><i>C.-L. Cheng, K.-S. Chang-Liao and T.-K. Wang</i>  | 286 |
| 32 Low-Frequency Noise Characterization in HfAlO <sub>x</sub> /SiO <sub>2</sub> n-MOSFETs<br><i>T. Horikawa, N. Yasuda, W. Mizubayashi, K. Iwamoto, K. Tominaga, K. Akiyama, K. Yamamoto, H. Hisamatsu, H. Ota, T. Nabatame and A. Toriumi (Invited Paper)</i>   | 292 |
| 33 Effects of Impurities in Hafnium Dioxide<br><i>B. Xia, A. Stesmans, F. Chen, Z. Zhang, W.L. Gladfelter and S.A. Campbell</i>  | 304 |
| 34 Factors Influencing the Threshold Voltages of Metal Oxide CMOS Devices<br><i>C. Hobbs, L. Fonseca, S. Samavedam, J. Grant, V. Dhandapani, B. Taylor, L. Dip, D. Triyoso, D. Gilmer, J. Schaeffer, R. Hegde, H. Tseng, B. White, and P. Tobin (Invited Paper)</i>  | 313 |
| 35 Challenges in Integration of Metal Gate High-k Dielectrics Gate Stacks<br><i>W. Tsai, L-A. Ragnarrson, T. Schram, S. DeGendt, and M. Heyns (Invited Paper)</i>  | 321 |

|    |   |     |
|----|---|-----|
| 36 | Atomic Layer Deposition of Dielectrics and Electrodes for Embedded-DRAM Capacitor Cells in 90 nm Technology and Beyond<br><i>E. Gerritsen, N. Jourdan, M. Piazza, D. Fraboulet, F. Monsieur, J.F. Damlencourt, F. Martin, E. Mazaleyrat, K. Barla and G. Bartlett (Invited Paper)</i> | 328 |
| 37 | Fully Silicided Metal Gates for High Performance CMOS Technology -<br><i>W.P. Maszara (Invited Paper)</i>   | 341 |
| 38 | Silicon Precursors for Gate Dielectric and Electrode Applications<br><i>C.A. Hoover, S.H. Meiere, M.H. Litwin, J.P. Natwora, G.B. Piotrowski, D. Zhang and J. Peck</i>  | 354 |
| 39 | TiCl <sub>4</sub> as a Precursor in the TiN Deposition by ALD or PEALD<br><i>K.-E. Elers, J. Winkler and S. Marcus</i>  | 361 |
|    | <b>Section V</b>  | 369 |
|    | <b>New CMOS Technologies</b>  |     |
| 40 | Device and Substrate Design for Sub-10nm MOSFETs<br><i>M. Jeong, B. Doris, J. Kedzierski, Z. Ren, K. Rim, M. Yang, H. Shang and L. Chang (Invited Paper)</i>  | 371 |
| 41 | CMOS Optoelectronics<br><i>C.W. Liu and B.C. Hsu (Invited Paper)</i>  | 383 |
| 42 | Low Thermal Budget Ge MOS Technology<br><i>C.O. Chui and K. Saraswat (Invited Paper)</i>  | 396 |
| 43 | Strained Ge MOSFETs: Devices and Process Technology<br><i>A. Ritenour, M. Lee, N. Lu, W. Bai, S. Yu, E. Fitzgerald, D.L. Kwong and D. Antoniadis (Invited Paper)</i>  | 406 |
| 44 | Source-Drain Series Resistance: The Real Limiter to MOSFET Scaling<br><i>S.E. Thompson (Invited Paper)</i>  | 412 |
|    | <b>Author Index</b>   | 421 |
|    | <b>Subject Index</b>  | 425 |