PROCEEDINGS OF THE SYMPOSIUM ON

# HIGH VOLTAGE AND SMART POWER DEVICES

Edited by

Peter W. Shackle
North American Philips Corporation
Briarcliff Manor, New York

*ELECTRONICS AND DIELECTRICS AND INSULATION DIVISIONS*

Proceedings Volume 87-13

THE ELECTROCHEMICAL SOCIETY, INC., 10 South Main St., Pennington, NJ 08534-2896

File copy
Rec'd 9/22/87

PROCEEDINGS OF THE SYMPOSIUM ON

# HIGH VOLTAGE AND SMART POWER DEVICES

Edited by

Peter W. Shackle
North American Philips Corporation
Briarcliff Manor, New York

*ELECTRONICS AND DIELECTRICS AND INSULATION DIVISIONS*

Proceedings Volume 87-13

THE ELECTROCHEMICAL SOCIETY, INC., 10 South Main St., Pennington, NJ 08534-2896

Copyright 1987
by
The Electrochemical Society, Incorporated

***Papers contained herein may not be reprinted and may not be digested by publications other than those of The Electrochemical Society in excess of 1/6 of the material presented.***

Library of Congress Catalog Number: 87-82469
Printed in the United States of America

# HIGH VOLTAGE AND SMART POWER DEVICES

## PREFACE

Peter W. Shackle, Philips Laboratories

High voltage and smart power devices have been the subject of considerable activity over the last seven years. Advances have been made in the design, technology and applications to such a degree that that the resulting products are now a measurable and rapidly growing segment of the semiconductor industry.

In recognition of this growing importance, the Electrochemical Society sponsored a Symposium devoted entirely to high voltage and smart power devices at the 1987 Spring meeting held in Philadelphia. This volume documents the papers that were presented. The diverse nature of the papers presented in this Symposium reflect the multiple avenues along which the technology has evolved in response to the different application needs. The original discrete power device technologies remain as a backbone to the whole activity and were the subject of a complete session. Common to many of the structures used are the special techniques associated with high voltage and power devices, involving passivation, packaging and diagnostic methods. Papers on this special technology comprised another complete session. Chips which incorporate multiple isolated power devices on a single chip almost inevitably involve the use of lateral structures of some kind or another, and so a complete session was devoted to these devices.

In the various technologies which are being used to fabricate power integrated circuits, two distinct lines of progress are emerging - junction isolated chips and dielectric isolated chips. In many cases these two kinds of technology address different applications, in a few others they compete directly. For example automotive applications are mostly junction isolated while many telephony applications are dielectric isolated. Some companies are also developing technologies which are partially dielectrically isolated, achieving some of the advantages of each. In this symposium complete sessions were devoted to progress in junction isolated technology and to progress in dielectric isolated technology respectively. The competition between these twin avenues of progress promises to be considerable in the future.

## ACKNOWLEDGMENTS

The organization of the symposium recorded in the following pages was facilitated by the sponsorship of Siliconix inc, who contributed the editor's time along with mail, telephone and secretarial facilities.

A watchful committee helped to solicit papers and carried out numerous chores to make the whole event happen. Terry J. Riley of ATT Bell Labs ran the evening panel session, Steve Miles of Sprague Electric organized the publicity and Co-Chairman David Crees of Marconi managed European relations. Ayman Shibib of ATT Bell Labs ran the late news papers session, while other sessions were chaired by King Owyang of General Electric, Adrian Cogan of Siliconix, Vladimir Rumennik of Philips Laboratories and Jay Baliga of General Electric Labs. All the committee members contributed ideas and helped with refereeing papers.

Most important of all, I should like to thank the numerous authors who travelled from Japan, Sweden, Germany, Italy, Spain, South Africa and Europe and also from various parts of the USA. Their efforts literally made the symposium the worthwhile event that it was. In particular the Symposium was honored by the presence of the invited speakers, J. Tihanyi of Siemens, H. C. Becke and J. C. Gammel of ATT Bell Labs and Vladimir Rumennik of Philips Laboratories.

Finally it would not be proper to pass over the help and encouragement provided by the various ECS officials, in particular Pat Castro and Sam Broydo, and the professional staff of the ECS office in Pennington, especially Roque Calvo and Sarah Kilfoyle.

Peter W. Shackle,
Co-Chairman,
Symposium on High Voltage and Smart Power Devices.
May 1987

CONTENTS

Junction Isolated Power IC Technologies


| Page | |
|---|---|
| 11 | Invited Paper: "Smart High Side Switches for Automative Applications"<br>Dr. J. Tihanyi<br>Siemens AG |
| 20 | "Process and Device Considerations for the Design of an H-Bridge Motor Driver IC"<br>S. P. Robb, L. E. Terry, J. Sutor<br>Motorola |
| 31 | "Experimental and Numerical Analysis of the High Voltage Structures Implemented in the New Mixed Process Multipower BCD 250V"<br>C. Contiero, A. Andreini, P. Galbiati, C. Lombardi<br>SGS |
| 41 | "Modelling of CMOS Compatible High Voltage Device Structures"<br>Z. Parpia, C. Andre T. Salama and R. Hadaway<br>University of Toronto |
| 51 | "High Voltage Complementary Mosfet Technology for Flat Panel Display Driver ICs."<br>Takeaki Okabe, Kouzo Sakamoto, Masatoshi Kimura and Koichrou Satonaka.<br>Hitachi |
| 60 | "High Voltage CMOS: Devices and Applications"<br>William G. Meyer<br>AT&T Bell Laboratories |
| 68 | "A New Technology for Junction Isolated ICs"<br>Judy L. Sutor, Lewis E. Terry, Stephen P. Robb<br>Motorola |

CONTENTS - CONTINUED

Dielectric Isolated PIC Technologies


| Page | |
|---|---|
| 79 | "A Dielectrically Isolated Bipolar CMOS-DMOS (BCDMOS) Technology for High Voltage Applications"<br>C. A. Goodwin, M. A. Shibib, R. A. Furnanage, C. Y. Lu, P. C. Riffe, N. S. Tsai and J. L. Schmoyer<br>AT&T Bell Laboratories |
| 90 | "A 200V DI Process Which Provides IGT's, SCR's, High Speed Complimentary Low Voltage Bipolars, CMOS and Bipolar Logic Options."<br>James D. Beasom<br>Harris Semiconductor |
| 96 | "Dielectrically Isolated High Voltage Intelligent Power IC Technologies Composed of CMOS Logic and Lateral Power Thyristors."<br>Yoshita Sugawara and Tatsuo Shimura.<br>Hitachi |
| 106 | "The Effects of Plasma Enhanced Vapor Deposited Oxide on Leakage Current of Transistors for CMOS High Voltage IC"<br>Henry W. Chien, Franklin F. Lee and Timothy J. Herbst<br>Telmos. |
| 118 | "A High-Voltage Dual-Gate DMOS Structure (DGDMOS)"<br>C. N. Dunn, J. C. Gammel and M. A. Shibib<br>AT&T Bell Laboratories |
| 131 | "The Status of Isolation in High Voltage Integrated Circuits"<br>H. W. Becke and J. C. Gammel<br>AT&T Bell Laboratories |

CONTENTS - CONTINUED

Discrete High Voltage Devices


Page

150 "The MOS Controlled Thyristor (MCT) and Smart Power ICs"
V. A. K. Temple
General Electric

157 "The Accumulated Layer under the Gate Electrode in VDMOS Devices"
J. Rebollo, J. Millan and F. Serra-Mestres
CSIB-UAB (Spain)

166 "Area Partition of High Voltage Darlington Transistors Using a Graphical Saturation Model."
S. A. Smithies
NEERI (South Africa)

174 "A Novel Gate Structure to Set the Turn-on Current of a Fold Back Diode."
P. Schieke.
NEERI (South Africa)

187 "Anamolous Reduction in Blocking Voltage Capability of High Voltage Transistors Due to Selenium Contamination"
G. Dolny, L. Goodman, P. Robinson, C. Magee, L. Hewitt, E. Botnick, E. Tena, D. Burton
RCA

194 "The Effect of Platinum Diffusion and Annealing on Breakdown Voltages and Lifetimes of Boron and Aluminum Doped High Voltage Diodes."
A. V. Hayes, M. Livschultz, T. J. Knowles
UNISYS Corp.

206 "Investigation of Turn Off Behavior for the Design and Development of High Current GTO Thyristors."
M. Bakowski, K. Thorselius, F. Vojdani
ASEA (Sweden)

CONTENTS - CONTINUED

Technology for High Voltage Devices


| Page | |
|---|---|
| 218 | "The Modular Power SIP - An Innovative Packaging Technique for Smart Power Integrated Circuits"<br>Phil Davies and Barry Sheldon<br>IPS (Great Britain) |
| 226 | "Characteristics of Metal-insulator-SIPOS-Silicon Capacitors"<br>A. Mogro-Campero, S. A. Al-Marayati, M. F. Chang, J. L. Benjamin, and W. A. Kotas<br>General Electric |
| 232 | "Humidity Induced Structural Changes in SIPOS"<br>J. W. Osenbach and W. R. Knolle<br>AT&T Bell Laboratories |
| 241 | "Dielectric Isolation by Growth of Thick Silicon Films on Oxidized Silicon Wafers".<br>G. K. Celler and L. E. Trimble<br>AT&T Bell Laboratories |
| 250 | "Evaluation of High Voltage ICs by Corona Charging"<br>R. B. Comizzoli and J. W. Osenbach<br>AT&T Bell Laboratories |
| 262 | "Field Dependent Conductivity in Semi-Insulating Polycrystalline Silicon Films"<br>R. B. Comizzoli and R. L. Opila<br>AT&T Bell Laboratories |

CONTENTS - CONTINUED

Lateral High Voltage Devices


| Page | |
|---|---|
| 280 | "Complimentary LIGTs for Power IC Applications"<br>D. N. Pattanayak, T. P. Chow, B. J. Baliga and<br>M. S. Adler<br>General Electric |
| 290 | "Modeling and Optimization of Lateral High Voltage<br>IC Devices to Minimize 3D Effects"<br>H. Yilmaz<br>General Electric |
| 295 | "DC and Transient Analysis of Lateral Insulated Gate<br>Conductivity Modulated Transistors"<br>M. N. Darwish and M. A. Shibib<br>AT&T Bell Laboratories |
| 310 | "Influence of Device Structure on the Transient and<br>Steady State Characteristics of the LIGT."<br>S. Mukherjee, M. Amato and V. Rumennik<br>Philips Laboratories |
| 318 | "Two Dimensional Device Simulation of High Voltage<br>Lateral DMOSFETs"<br>R. W. Busse and R. K. Williams<br>Siliconix |

CONTENTS - CONTINUED

Late News Papers


Page

330 Physical Modeling of LIGT Structures for SPICE Simulation of Power Integrated Circuits.
R. J. McDonald, J. G. Fossum and Y. S. Kim
University of Florida
M. A. Shibib, AT&T Bell Laboratories

343 Magnetic Czochralski Silicon for Power Devices
F. A. Selim and L. B. Major
General Electric Company
G. F. Fiegl
Unisil Corporation

353 INDEX

# JUNCTION ISOLATED PIC TECHNOLOGY

## SESSION CHAIRMAN:

VLADIMIR RUMENNIK
PHILIPS LABS

Proceedings of The Electrochemical Society, PV 1987-13, 11-19 (1987)
DOI: 10.1149/198713.0011PV © The Electrochemical Society

# SMART HIGH SIDE SWITCHES FOR AUTOMOTIVE APPLICATIONS

J. Tihanyi

Siemens AG, UB B, WDH LH TE 1
Frankfurter Ring 152, 8000 München 46,
Germany

## ABSTRACT

The expanding use of microcomputer systems in automobiles has created a need for new types of "relays", requiring compatibility to VLSI circuits. A novel power IC technology has been developed integrating vertical power MOSFETs, high voltage CMOS, and 5V CMOS logic on a single chip.

The first products in this "Smart SIPMOS" technology (for applications under 50V) are high side switches which provide full protection against short circuit and overtemperature conditions, in addition to diagnostic functions. The switch inductive or capacitive loads, as well as incandescent lamps.

## INTRODUCTION

Electrical loads in automobiles are traditionally powered by high side switches, in order to reduce corrosion of the contacts. One terminal of the load is permanently attached to the negative (low) pole of the battery while the other makes contact with the positive (high) pole when the switch is activated.
In fig. 1 the well known relay activated reflector bulb driver is shown as a typical example of high side switching. The bulb current flows through the secondary circuit of the relay, which is protected by a fuse. The relay is activated by the relatively small primary current, which is delivered by the mechanical switch in the dashboard. The fuse provides protection in case of a short in the lamp circuit. This relay solution is simple and functional. It is hard to explain to the average automobile driver why we are working so diligently to replace this simple divice with complex and esoteric semiconductor circuits.

There are, however, many reasons for developing microelectronic power switches which outperform mechanical relays. One is the expected higher reliability of a monolithic switch with no moving parts. Another argument is that by using semiconductor circuitry, new innovations can be imagined which would be impossible for mechanical equipment. In any case, the prime motivation is the expanding use of microcomputers and VLSI circuits in the automobile for achieving better performance in all aspects: pollution control, reducing energy consumption, and last, but not least, comfort. Mechanical relays are not compatible with microcomputers and VLSI circuitry, consequently new power switches are needed which meet the requirements of the microcomputer age.
For over three years, our engineering staff has worked on developing microprocessor compatible advanced or "smart" switches for automotive applications. According to inputs from customers collected during this time, the ideal high side "smart" switch would have the following attributes:

* Inputs and diagnostic autput must be TTL/CMOS compatible
* Self protection functions must provide for short circuit, over-temperature, and over-voltage conditions (in addition, indication for improper polarity is also desired).
* Relatively slow switching speed to avoid FR influence.
* Functional voltage range spanning the interval from 4 to 50 volts.
* Switching capabilities for both lamps and solenoids.
* Capability for diagnostic functions to distinguish between open load and overload conditions.
* Operating temperature range between $-50^{o}C$ and $150^{o}C$ inclusive.
* Capability for suppressing voltage spikes due to wire inductances.
* Low $R_{ON}$ and standby current.
* Superior reliability.
* Low price.

## SMART SIPMOS TECHNOLOGY

In order to fulfill the requirements, a relatively simple technology has been developed for fabrication of the power switches. It was obvious that for the main switching device, only n-channel power MOSFETs could be considered. For voltages under 50V, they achieve the lowest $R_{ON}$ on of all electronic devices, including bipolar darlington transistors. It was also clear that, for logic functions, only CMOS techniques could be used, in order to obtain the smallest possible standby current. The technology developed allows the simultanious construction of vertical power MOSFETs and high and low voltage CMOS logic circuits, in addition to supporting devices such as Zener diodes and bipolar transistors. The basic structures of the technology are shown schematically in figues 2 through 5. The high voltage lateral p-channel MOSFET is shown in fig.2. It can operate up to 100V, with excellent DC characteristics. Figure 3 shows the high voltage lateral n-channel transistor. The low voltage logic, with its corresponding CMOS DC characteristics, is shown in fig. 4. The p-channel device exhibits relatively strong body effects, as the change in its body bias is equal to the positive voltage. The vertical power device $I_D$ ($U_D$) characteristics demonstrate adequate operation well beyond 50V. (fig. 5) All of the structures are fabricated simultaneously with a ten mask process. They are built on a simple epitaxial wafer, which is identical to the starting material of standard SIPMOS devices. The process techniques are those routinely used in polysilicon gate IC fabrication, i.e., ion implantation, plasma etching, sputtering, CVD-oxide and polysilicon deposition. The yield is also the same as the standard polysilicon gate process.

## BTS 412

The first product fabricated by the "smart" SIPMOS process is a 250 m$\Omega$ high side switch, the BTS 412. Its basic building blocks are shown in fig. 6. The power switch is a vertical device driven by a level shifter - charge pump combination, which delivers the required over-voltage to the gate of the output device. The switching speed is rather high (10 µs rise and fall times) despite the slow pumping action. The device contains a 5 volt CMOS logic circuit for managing the input and feedback information, delivering the status signals, and providing the built-in delay of 50 µs for the direct short circuit protection.

The low voltage CMOS logic is operates on an internal power supply. The device maintains its 60 µA standby current even at 150°C. The output device includes a Zener chain between drain and gate, which protects the autput against voltage spikes. The short circuit current is limited to about 20 amps, and the device will be switched off if the short circuit duration exceeds the predetermined delay time of about 50 µs. The temperature threshold is set to about 170°C. It would function even at 220°C, which means the safety margin for temperature sensing and protection is high enough for reliable operation.

## FURTHER DEVELOPMENTS

The first device provides all functional requirements, however it does not fulfill all of the different needs of the high side switchmarket. There are applications in which $R_{ON}$ must be as low as 20-40 m Ω. Other users need specialized logic functions, different types of status information, and other voltage levels for inductive current decay in solenoids. There is interest in devices with controllable current limiting levels, or with controllable switching speeds. This, in addition to other information, confirms the early prediction that the high side switch market would be oriented toward custom design. With this realization, our first step in the new designs was to raise the current carrying capability per unit chip area. Figure 7 shows the layout of one such development device.

## CONCLUSION

We have described a simple power IC technology, especially suited for high side switches in automotive applications. We hope it is flexible and inexpensive enough to address the various needs of the new, expanding automotive market. After the introduction of the first device, the BTS 412, further dedicated and standard products are now in development.

## ACKNOWLEDGEMENTS

The author would like to say thanks to all of the members of the SIPMOS team for their help and support, and to Mr. B. Cohen for revising the English text.

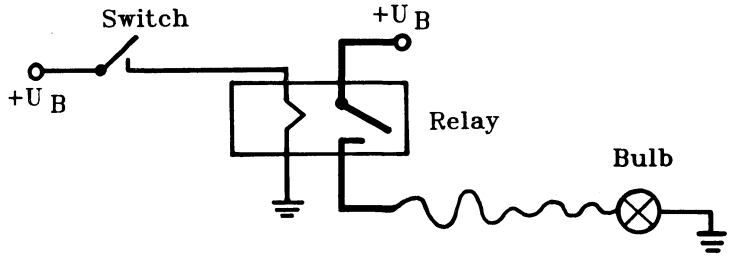



Fig. 1 Relay circuit for high side bulb switching

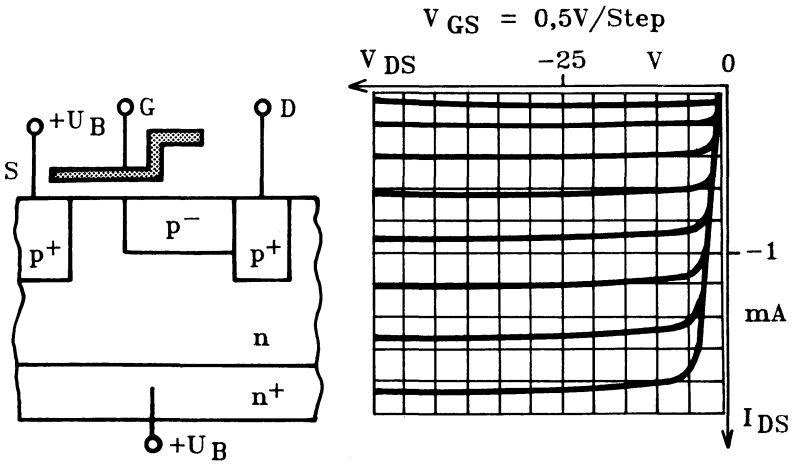



Fig. 2 Structure and DC characteristics of the lateral HV P-channel MOSFET (Test device)

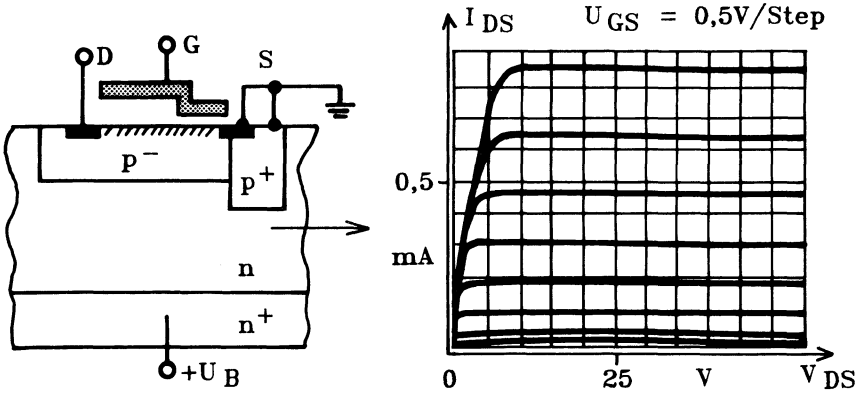



Fig. 3 Structure and DC characteristics of the lateral HV n-channel MOSFET (Test device)

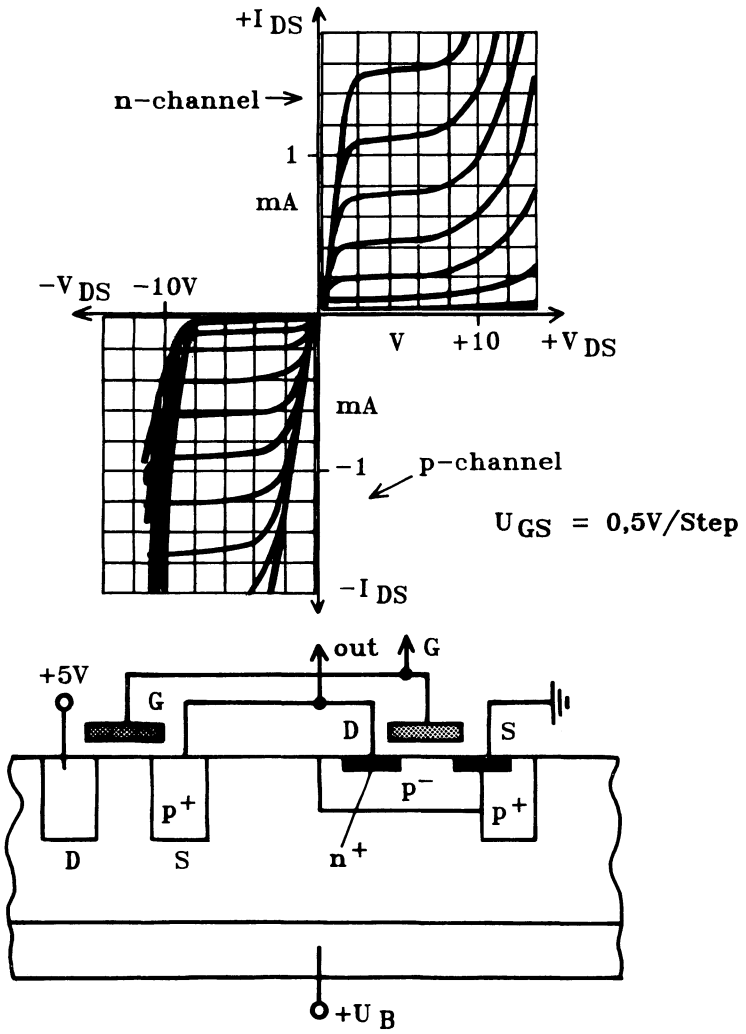



Fig. 4 Low voltage CMOS inverter and DC characteristics of the MOSFET's (Teststructure)

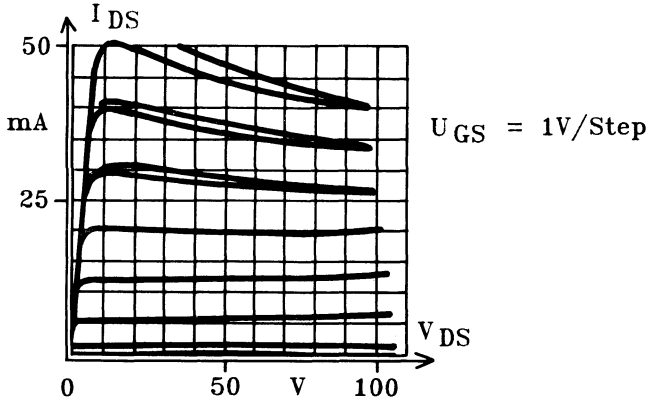



Fig. 5 DC characteristics of the vertical power switch (Test device)

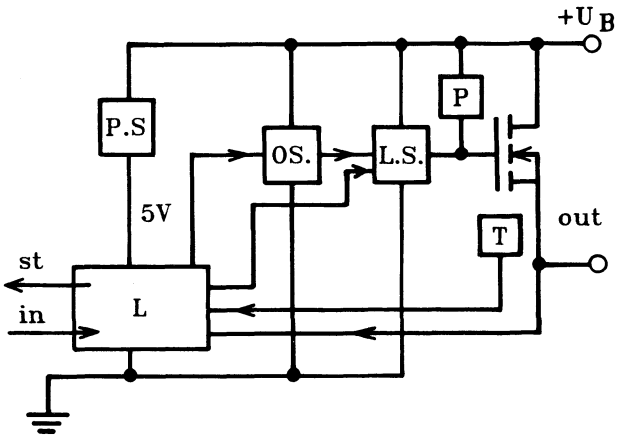



Fig. 6 Circuitry of the smart high side switch BTS 412

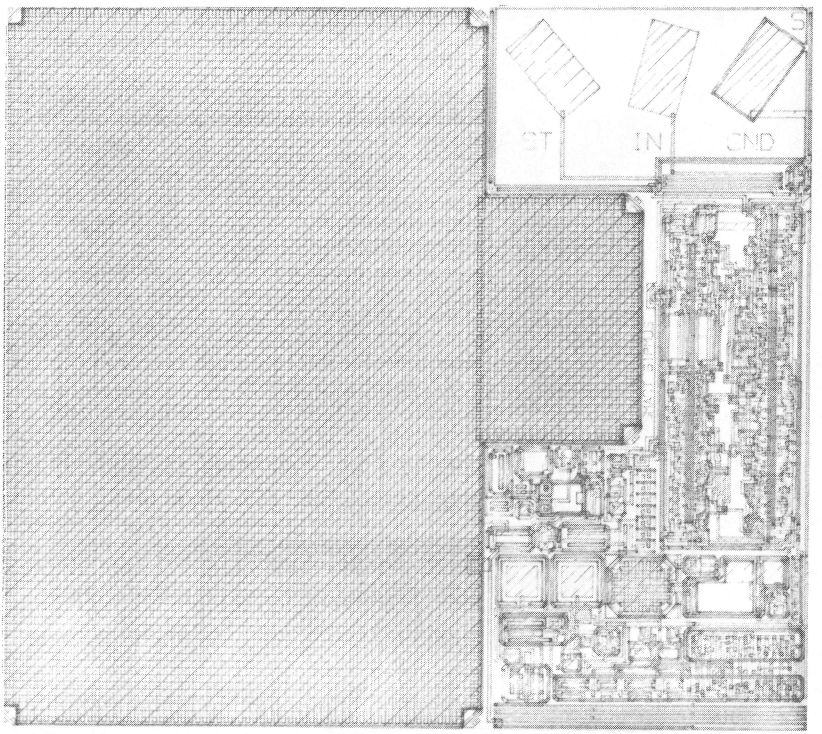



Fig. 7 Layout of an experimental device with low $R_{on}$

Proceedings of The Electrochemical Society, PV 1987-13, 20-30 (1987)
DOI: 10.1149/198713.0020PV © The Electrochemical Society

# PROCESS AND DEVICE CONSIDERATIONS FOR THE DESIGN OF A SMARTpower H-BRIDGE MOTOR DRIVER

Stephen P. Robb
Lewis E. Terry
Judith L. Sutor
David Okada

Motorola Inc.
5005 E. McDowell Rd.
Phoenix, Az. 85008

## ABSTRACT

This paper details the process and device design for a SMARTpower H-bridge motor driver which is ideal for battery-powered systems. In such a system the on-resistance of the power FETs is extremely important because of the limited voltage available for driving both the gates of the FETs and the load. Since the FET's are very low voltage, the channel resistance is a major contributor to on-resistance and so it is important to maximize channel width. Metallization resistance also becomes an important factor.

Different device geometries were modeled to determine which device had the lowest total $r_{DS(ON)}$. A test vehicle was built with the different geometries to confirm the results of the modeling. Finally, a circuit was designed and built utilizing four of the "optimum" devices in an H-bridge configuration.

## INTRODUCTION

One of the most important considerations in designing a power I.C. is the choice of the power device configuration. The voltage and current requirements of the system dictate whether the devices will be lateral, vertical, updrain, planar, etc. Once the type of power device is decided, a process can be designed to include the device(s) and the associated logic circuitry.

It is much easier to build a power I.C. for a specific system rather than try to design a generic circuit that will work well in many applications. Fortunately, for the circuit under consideration, the system requirements were clearly spelled out before the design began. Working under these constraints, it was possible to design power devices that were optimum for the application.

## SYSTEM CONSTRAINTS

Fig 1 illustrates the configuration of the H-bridge motor driver. The motor is driven forward when FETs 1 & 4 are turned on, and in reverse when FETs 2 & 3 are turned on. The system that the motor driver I.C. fits into is powered by a battery source ($V_{bat}$) which can vary from +2 to +7 volts. Charge pumping is utilized to provide the CMOS logic with a constant 5 volt rail, should the battery voltage fall below 5 volts.

Because of power dissipation limits, the sum of the on-resistance of an upper FET (FET 1 or 2) and a lower FET (FET 3 or 4) must be less than 0.5 ohms at a temperature of 125 C. Since the potential of the source of an upper transistor is near $V_{bat}$ when the motor is on, charge pumping must be used to drive the gates of the upper FET's above the upper rail. The effective gate drive for the upper FETs is then less so that they will have higher $r_{DS(ON)}$ than the lower FETs. The power devices have to be capable of 1 amp D.C. continuous operation and 3 amp transients. The $BV_{DSS}$ of the devices must be at least 15 volts.

## PROCESS FLOW

Process and device modeling was done to determine how to scale the junction depths, doping concentrations, gate oxide thickness and the poly width for the devices. Based on the simulation results, a process flow was developed and a test vehicle was laid out which included devices with different geometries and poly widths, but with the same active area.

The process used allows CMOS and bipolar small signal devices to be integrated on the same chip with power n-channel DMOS devices. The DMOS devices can be either vertical or lateral structures. The minimum geometry used in the circuit is 5 μM, while in the power device it is 3 μM.

A cross section of the process utilizing lateral power devices is shown in Fig 2a. The process starts with a p type substrate on which a layer of n epi is grown. A p-type isolation diffusion is done to separate the power devices from the control circuitry, and from each other. Next the p well for the n-channel MOS devices is implanted. Field oxidation is followed by active area definition, gate oxide and polysilicon for the gates. The p tub for the LDMOS power devices is then implanted, followed by the $p^+$ and $n^+$ diffusions which form the source-drains of the CMOS. Two-layer metal is used so that the circuit can utilize the thin metal required for fine line patterning while the power devices can use the thick metal required for high current capability.

The process is much the same for the vertical devices (Fig 2b) except an $n^+$ buried layer is used to minimize the $r_{DS}(ON)$ of the power devices. Also, a deep $n^+$ sinker is used to form a low resistance path from the buried layer to the drain contact.

## DEVICE MODELING

Several power device geometries were considered for the task and they are shown in Fig 3. Cross sections of the devices are also shown. The possibilities include a vertical DMOS device with a top drain contact (3a), a lateral DMOS device with a stripe geometry (3b), a lateral DMOS with a checkerboard layout where the sources and drains are on alternating squares (3c), and a lateral DMOS device with a cellular layout where the polysilicon resembles links in a chain (3d).

A first order approximation of $r_{DS}(ON)$ can be made by comparing the channel width per unit area (Z/A) available in the various layouts since, for low voltage, lateral devices the channel resistance will be the dominating component of $r_{DS}(ON)$. For the updrain vertical device the epi, buried layer, and sinker resistances become important. Fig 4 compares Z/A values for the lateral geometries as a function of source-to-drain spacing which could include a drift region for higher voltages. It appears at first glance that the checkerboard layout is the best for low voltage while the stripe geometry will be better for high voltage devices.

The devices were modeled for $r_{DS}(ON)$ using lumped components similar to what was done by Sun & Plummer.[1] In addition to the silicon, the model included the resistance of the front metal assuming 10 kA of Al-Si at 3 μΩ-cm. In the double metal process, the finely patterned metal (9 μM pitch) in the interior of the power device is 10 kA thick while the high-current, large metal runs from the interior of the device out to the bond pads are 60 kA thick. The thick metal runs minimize $r_{DS}(ON)$ and prevent electromigration of the metal.

A two-dimensional Poisson solution with the device simulator CANDE from Stanford indicated that the lateral devices could achieve 20 volts without any drift region between the gate electrode and the drain diffusion. So the modeling for the $r_{DS}(ON)$ of the lateral devices was done with the gate extended over the entire distance from source to drain so that the current path is through the low resistance accumulation region at the surface. This produces a device with very low $r_{DS}(ON)$.

In a vertical device there is only one drain stripe per several rows of source cells. The current flows down an n+ sinker, through a buried layer to the source cells. The number of source cells between drain stripes can be optimized for lowest $r_{DS}(ON)$.[2] In this case the optimum number of source cells between drain stripes was found to be 3 to 4.

Table 1 shows the $r_{DS}(ON)$ X Area products for the different geometries. The columns in the table show the resistance of the silicon, the resistance of the metal, and the total $r_{DS}(ON)$ X area product. Results are shown for both a 3 μM and a 5 μM process for the lateral devices. Both processes were done to determine the $r_{DS}(ON)$ penalty of the 5 μM process which is easier to manufacture and would have higher yield. The vertical device was done with a 9 μM polysilicon width which allows room for the lateral diffusion of the p-tube beneath it.

It is interesting to note that the model predicted the best device to be the "chain link" device of Fig 3d, even though this device did not have the best value for Z/A. In fact, if only the silicon is considered, the lowest $r_{DS}(ON)$ X A product is achieved for the checkerboard device. The advantage of the chain device is that it has less resistance in the front metal, a parameter which sometimes goes ignored. But in the case of these very low voltage devices, as much as 35% of the total $r_{DS}(ON)$ is in metallization, bond wires, and packaging.

## EXPERIMENTAL DATA

A test vehicle was built to verify the model numbers. Devices with the various geometries were included and laid out with 3 μM and 5 μM design rules.

The experimental results are summarized in column 4 of Table 1. As can be seen, the chain geometry device with 3 μM poly has the lowest $r_{DS}(ON)$. In this design the chain device is the best combination of large channel width and low metal resistance. If a large gate drive voltage were not available, the checkerboard device would be the best by virtue of its larger channel width.

The vertical flow device is not able to compete because the resistance in the epi is large compared to the resistance of the surface accumulation region in the lateral devices. At higher voltages (above 50 volts) vertical devices become attractive because lateral devices require large source-drain spacings to accommodate the associated drift regions which add considerable resistance.[3]

An H-bridge circuit was designed which used power devices with the chain link layout and 3 μM poly. The circuitry interfaces the H-bridge to logic levels and provides protection functions and drivers for the power devices. The power devices were scaled to obtain the required $r_{DS}(ON)$. The resulting chip size is 110 X 130 mils.

## CONCLUSIONS

The choice of power device for a power I.C. dictates what process will be used. Voltage and current constraints determine the type and geometry of the power device. In this application, lateral power devices with a unique "chain-link" layout were chosen because they provided the lowest total on-resistance. For this design, metal resistance and available gate drive became important considerations. Computer modeling of $r_{DS(ON)}$ and breakdown voltage was a very valuable tool in determining the optimum device geometry.


## ACKNOWLEDGEMENT

The authors would like to thank the people of the SRDL Pilot Line at Motorola Inc. for the fabrication of all of the devices used in this study.


## REFERENCES


1. S. Sun & J. Plummer, IEEE Trans. Elec. Devices, ED-27, NO. 2, 356, (1980)

2. A. Andreini, C. Contiero, P. Galbiati, IEEE Trans. Elec. Devices, ED-33, NO. 12, 2025, (1986)

3. M. Amato & V.Rumenik, IEDM Technical Digest, 736, (1985)

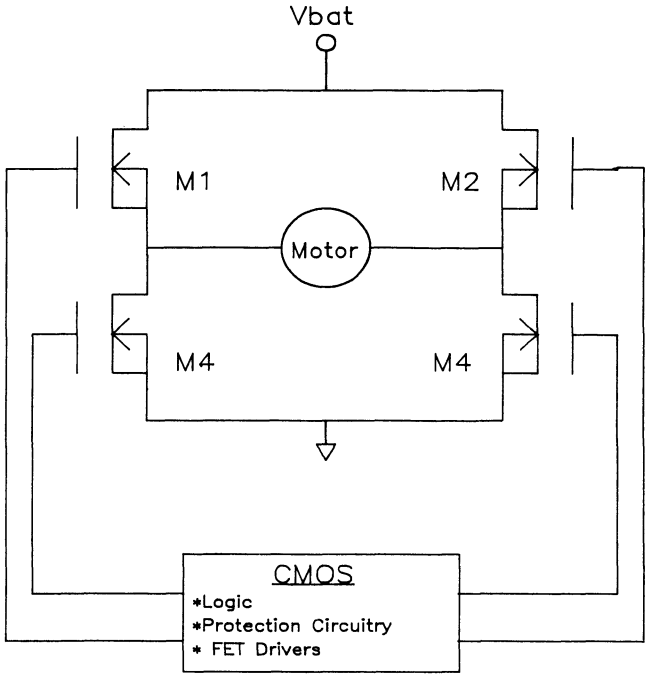



Fig 1: H—Bridge Motor Driver

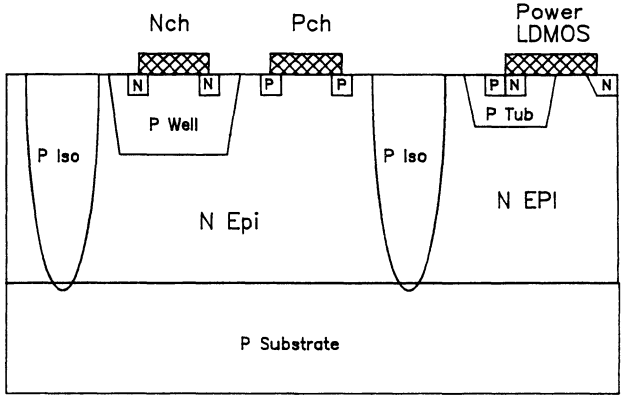



Fig 2a: Crossection of Process
For Lateral Devices

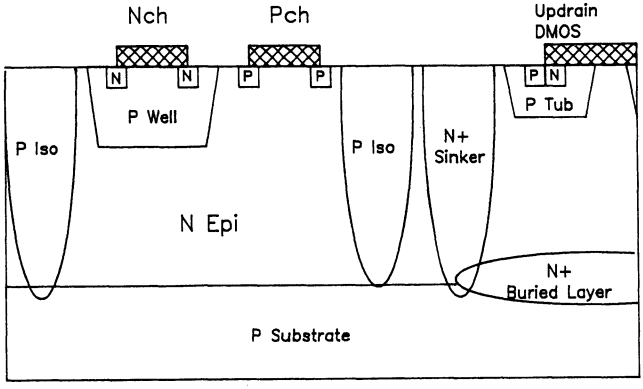



Fig 2b: Crossection of Process
For Updrain Devices

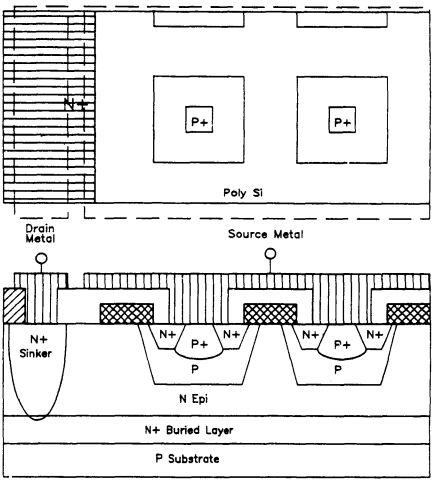



Fig 3a: Updrain Vertical DMOS

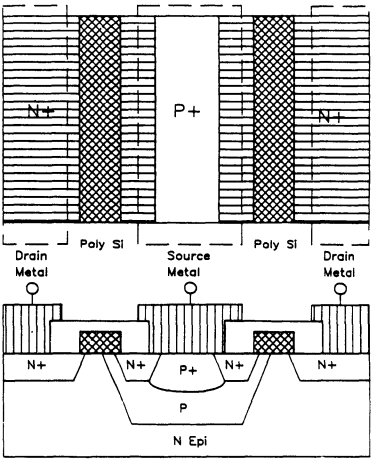



Fig 3b: LDMOS With Striped Layout

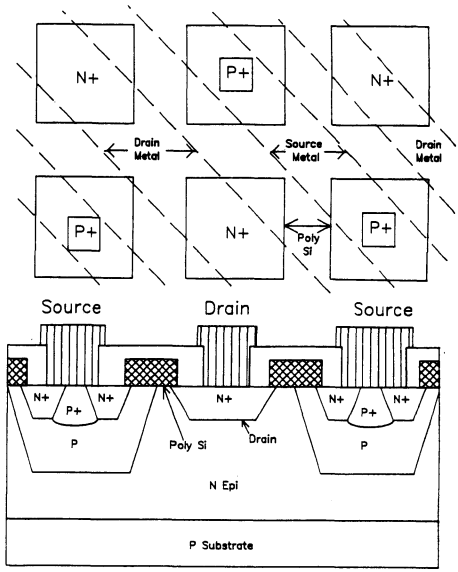



Fig 3c: LDMOS With Checked Layout

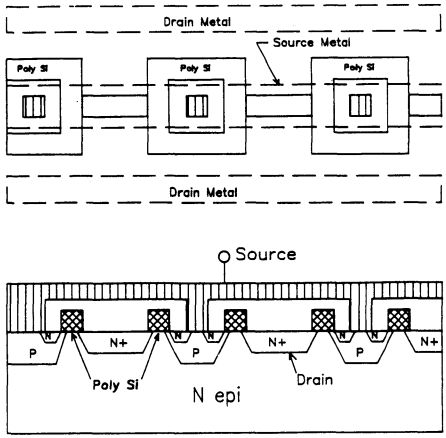



Fig 3d: LDMOS With Chain Layout

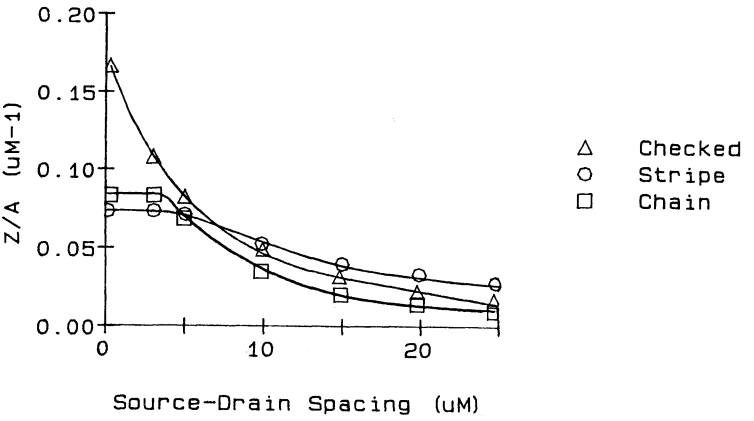



Fig 4: Channel Width/Unit Area

| Device | Model Silicon Only (ohm uM2) | Model Total (ohm uM2) | Measured (ohm UM2) |
|---|---|---|---|
| Chain (3 uM) | 9.90E4 | 1.17E5 | 1.3E5 |
| Chain (5 uM) | 1.97E5 | 2.13E5 | 2.0E5 |
| Stripe (3 uM) | 1.14E5 | 1.37E5 | 1.7E5 |
| Stripe (5 uM) | 1.92E5 | 2.13E5 | 2.8E5 |
| Checker (3 uM) | 7.85E4 | 1.30E5 | 1.6E5 |
| Updrain (3 uM) | 4.00E5 | 4.10E5 | 4.6E5 |

Table 1: On Resistance X Area Product For Various Devices

Proceedings of The Electrochemical Society, PV 1987-13, 31-40 (1987)
DOI: 10.1149/198713.0031PV © The Electrochemical Society

# EXPERIMENTAL AND NUMERICAL ANALYSIS OF THE HIGH VOLTAGE STRUCTURES IMPLEMENTED IN THE NEW MIXED PROCESS "MULTIPOWER BCD 250V"

C.Contiero A.Andreini P.Galbiati C.Lombardi
SGS Microelettronica SpA, Monolithic Microsystem Division
20019 Castelletto di Settimo Milanese MILAN ITALY

**ABSTRACT**

An evolution towards high voltage of a new integrated silicon gate mixed process has been developed. This technology, whose name is Multipower BCD 250, allows to integrate on a same chip bipolar linear, CMOS logic together with high voltage, high current DMOS and high voltage P-channel MOS devices that can sustain more than 250V.
The high voltage structures have been analyzed and dimensioned by using the 2-D device simulator HFIELDS.

## INTRODUCTION

It has been reported in previous works (1-4) that to develop integrated circuits that combine high power output stages and low voltage analog and digital signal processing the most popular approach is to use the DMOS silicon gate structure in an isolated scheme. In fact DMOS devices are preferred to bipolar devices because of their low input gate currents (that means simplified drive circuitry) their higher breakdown voltage, better SOAR and very fast switching speed. Besides they are technologically compatible with CMOS silicon gate devices.
To enter into the new and very interesting field of the "smart PIC" our strategy was to adopt the junction isolation technique, which is a well controlled process less costly to produce compared to the dielectric isolation technique (even in the high voltage case where a top-bottom approach is required), merged with the DMOS silicon gate process today in mass production for discrete power devices. From this marriage a very versatile technology called Multipower BCD has been developed. By using the dopant profiles involved in the DMOS structure and adding only a few extra steps, this technology allows to integrate at the same time a large group of basic devices (Bipolar, CMOS, DMOS) to build complex control sections and multiple high power vertical DMOS transistors to realize high performance PICs.
This technology is particularly suitable for all kinds of applications where neither the sources or drains of the power stages are necessarily connected to ground or together. The process has been successfully implemented in 60V and 100V ranges realizing many electrical applications (switched mode motor control, switched mode power supply, low and high side driver) (5-7).
This paper presents the 250V version of the Multipower BCD process (8). The rating at 250V is sufficient for some off-line switching supplies, lamp ballasts, solid state relays, motor controls and fluorescent display drivers.
A test pattern has been designed to evaluate the process feasibility, the low level CMOS and bipolar properties, a low leakage diode implementation and to investigate the best design of the high voltage structures (i.e. the N-channel vertical DMOS, the extended drain P-channel MOS and the metal line crossovers).

All the device design has been supported by simulation using the 2-D device analysis program HFIELDS (9) developed at the University of Bologna and IDAS (Interactive Device Analysis System) (10) developed in SGS.

**PROCESS AND DEVICE DESCRIPTION**

The architecture of the Multipower BCD 250V process is rather similar to the 60V version reported in a previous work (8). The main difference regards the junction isolation technique that is improved to provide high voltage blocking capability by the top-bottom sinker and isolation approach (11) (fig.1). In fact, owing to the thick (25-μm) epitaxial layer required to spread the junction depletion layers, it is useful to follow this scheme to reduce the high temperature processing times which are responsible for the buried layer out diffusion and the isolation and drain sinker sizes (fig.1).
The key structure of the process is the high voltage DMOS (BVdss>250V) in vertical configuration with the drain contact brought to the surface via an N+ buried layer and N+ sinker diffusion.
The fabrication sequence starts on (100) 30-ohm*cm P-type substrate in which buried layers of antimony, phosphorus and boron are selectively implanted. After epitaxial growth of a 25-μm, 11-ohm*cm N- layer, P-well regions are applied by masked implantation and standard P+ isolations and N+ sinkers are diffused. The P-well regions are designed to realize self isolated N-ch. MOS for CMOS devices but they also serve as a base region for a first type of NPN transistor (NPN1) with high gain ($\beta$=200) and as a medium doped region to better control the maximum electric field at the drain of the HV P-ch. MOS. To improve the high voltage performance of the process the 1-μm thermal field oxide is covered with 1.5-μm CVD oxide and the active areas are patterned after a high dose, low energy implant to obtain tapered oxide profiles. This step is very important to realize high efficiency field plates in DMOS structures and allows to improve step coverage.
The fabrication sequence continues following the DMOS silicon gate process. The high doped P+ regions, which are selectively introduced in the middle of the DMOS cells to kill the gain of the parasitic NPN structure, serve also to form the emitter/collector of lateral PNP, channel stops in CMOS N-ch. FET and contact regions in the NPN base and P-ch. MOS.
The polysilicon gate of the DMOS forms also self aligned gates (over a 850-Å gate oxide), field plates, interconnections, channel stops and electric shields. The boron doped body regions (Rs~600-ohm/sq), calibrated for a DMOS channel length of about 1.7-μm and a threshold voltage of about 3-V, act also as the source/drain for self aligned CMOS P-ch. FET and as the base for a second type NPN transistor (NPN2) with low, but very constant and reproducible gain ($\beta$=35). Arsenic doped DMOS source is employed for CMOS N-ch. FET source/drain, NPN bipolar emitters and low resistance contacts. Before these N+ regions are implanted and driven, a lightly boron doped layer is implanted for drain extensions to increase the avalanche breakdown voltage of the HV P-ch. MOS transistors. Finally after 1-μm PSG deposition and reflow, the wafers are contact etched, metallized and passivated with plasma nitride.
The total number of masking steps is 14 and a 4-μm linewidth and 1-μm alignement tolerance process is used.

## BIPOLARS, CMOS AND LOW LEAKAGE DIODE

Bipolar devices are only employed for low voltage operations where their higher transconductance, low offset and low noise offer better performance in high precision stages while CMOS devices, thanks to their high packing density (~450 transistors/mm2 N- and P- ch. mixed) and low power consumption, are mainly employed in logic and switching functions. A mixture of both can profitably be used in special analog design (signal amplifier, voltage reference). As regards immunity to latch-up, the CMOS has taken advantage of the combination of the low shunt resistance of the N+ buried layer and the P+ ring around the P-well regions. In table 1 some electrical characteristics of the low voltage signal components are reported.
If to the 14-mask process an extra mask is added to implant an optional phosphorus doped buried layer, the top-bottom sinker and isolation approach allows the integration of an isolated high voltage low leakage diode (LLD) (fig.2). This diode structure is useful as a free wheeling diode in inductive load driving. The gain of the parasitic substrate PNP associated with this diode is very low; in this way the current losses towards the substrate are about four order of magnitude lower compared to a traditional base-collector diode (fig.3) reducing the problems of power dissipation and the undesired parasitic NPN action in between adiacent epi islands. The structure shown in fig.2 integrated in the process has given a blocking voltage capability of 290-V.

## HIGH VOLTAGE DEVICE DESIGN

N-channel Vertical DMOS

For applications that necessitate at the same time high voltage capability, medium currents (of the order of a few amperes) and flexibility in the output stages to realize for example low side, high side and push-pull configurations, the power DMOS devices must be integrated in a vertical scheme bringing the drain contact to the surface via an N+ buried layer and a deep N+ diffusion. The tradeoff among the maximum breakdown requirement for the body/drain junction, the minimum drift region contribution to the on resistance and the maximum epitaxial layer thickness available with the top-bottom technique, sets the resistivity and thickness of the N- epitaxial layer.
Fixed the epitaxial layer parameters ($\rho$=11-ohm*cm, th=25-µm), the breakdown of the DMOS body/drain junction, can occur between the inside cells (12) or at the edge of the outside cells. To improve the breakdown value at the edge, a field plate termination is used. From the computer analysis made for different combination of oxide thickness, field plate extension and spacing towards the drain sinker, it follows that a simple biplanar polysilicon field plate laying over the gate oxide and over a field oxide thinner of about 2-µm is not suitable to sustain a 300-V reverse voltage. In fact a high surface electric field, more than 2.5*10E5-V/cm, is induced at the edge of the field plate (13) that is not a reliable condition.
A triplanar structure, realized connecting the two oxides with a very low angle ($\alpha$=20°) and extending the source metal beyond the polysilicon field plate edge over an increased oxide thickness (field oxide + PSG), can reliably sustain the maximum 300-V applied voltage (fig.4). In fig.5 is reported the surface

electric field at point Q as a function of the angle to outline the importance of this scheme. In fact the high electric field arising in that point, when the angle is wide, causes electron injection in the oxide, causing walk-out of the breakdown value. Test devices designed with the two different edge terminations have shown that the change of the field oxide thickness from 2.5-μm to 1.5-μm affects only the blocking voltage capability of the biplanar structure lowering the value from 300-V to 270-V, while the triplanar structure is not quite affected allowing a breakdown voltage of about 315-V. However the thicker oxide is necessary to reduce the effects of the electric fields induced on the silicon surface by the high voltage metal interconnections.

To investigate the effect of the spacing (s) between the cells on the breakdown voltage (13), in fig.6 is reported the relationship between the computer simulated electric field at the junction curvature and the parameter s for fixed gate oxide thickness and epi layer specification. From the nearly constant behaviour of the electric field it follows that the field plate action of the gate electrode is effective over a wide range of spacings s between the cells without limiting the blocking voltage capability of the whole structure.

When the vertical DMOS is in an integrated scheme the maximum breakdown voltage requirement must not be limited by other effects. Then to avoid a low breakdown induced by the junction curvature of the N+ buried layer towards the P substrate, the bottom sinker is placed to increase the radius of curvature of the N+/P junction. As regards the parasitic MOS channels induced between active areas and junction isolation by the metal interconnections, a polysilicon shield is used as a channel stop. The same trick is employed to avoid electric field crowding effects due to metallization overlap on the isolation and drain sinker diffusions. The experimental analysis of the test devices designed to investigate these problems has revealed that the VDMOS blocking voltage capability is not limited by the integrated scheme.

The integrated VDMOS layout configuration has been chosen according to a mathematical model (14) that provides the product Ron*Area as a function of the physical and geometrical parameters involved in the structure taking into account the extra contributes to the Ron introduced by the buried layer and sinker diffusion. Using the symbols shown in fig.7, the product Ron*Area has the follwing expression:

$$R_{on}{}^{*}Area = [\frac{R_c}{N} + \frac{1}{12} R_{bl} N + \frac{1}{12} R_{bl} \frac{2Y}{l} + \frac{R_{sink}}{l X_{sink}}] \times l(N l + X_{sink} + 2Y)$$

where:

Rc is the on resistance of the DMOS cell;

Rbl is the N+ buried layer sheet resistance;

Rsink is the N+ sinker resistance per unit area;

l is the cell pitch = Xcell + d, where Xcell is the DMOS cell window and d is the spacing between two DMOS cells;

Xsink is the N+ sinker window width;

N is the number of cells between two drain sinker contacts;

Y is the distance between the edge of sinker window and half spacing of the outer cell (this value includes the extension of the junction edge termination).

In fig.8 some Ron*Area behaviours are reported as a function of DMOS gate width (d) and number of cells (N) between two drain sinker contacts. The cell used to realize power test devices was a 15-μm*15-μm square with round corners to avoid excessively high fields close to the MOS channel area when high Vds are applied. The gate width (d) was chosen equal to 15-μm, that corresponds to s = 10-μm, to minimize the Ron*Area product. Test vehicles designed placing 11 cells between two drain sinker contacts have given a Ron*Area equal to 5.2*10E-2-ohm*cm2, in good agreement with the calculated value shown in fig.8.

High voltage P-channel MOS

A complementary P-type HV MOS device is very useful to easily drive the high voltage DMOS. The HV P-ch. MOS uses an implanted extended drain to increase the maximum breakdown voltage of the body/drain junction by allowing the depletion region to spread mainly into the lightly doped drain instead of into the channel region. The drain extension also gives less Early effect. Its extension length (Lde) and doping level controls the maximum electric field at the drain but, at the same time, introduces a series resistance into the device. The 2-D computer program HFIELDS has provided a correlation among these parameters giving the design rules of many test structures for an experimental check with the aim of achieving a 300-V blocking capability.The first design step was to find the optimum implanted charge Qp for a drain extension length which does not limit the breakdown voltage. The second step was to minimize the drain extension and the MOS channel length to avoid severe performance degradation.

By the numerical analysis of the breakdown voltage versus Qp (fig.9) of the structure reported in the same plot, it was found that only a small Qp variation (less than about 15% of 3.0*10E12-cm-2) are allowed if the maximum blocking voltage capability is to be guaranteed.

A more reliable drain extension configuration is obtained introducing a second medium doped region and overlapping the source metal on the gate extending over a part of the drain region (square in fig.10). This second region does not cost any extra mask because it is realized with the dopant profile that is used as P-well in CMOS N-ch. FET. Although this junction has a profile not optimized for this purpose, its higher radius of curvature and lower doping level lowers the maximum electric field at the high doped contact region. The source metal extended over and beyond the polysilicon gate acts as a field plate reducing the crowding field effect at the gate-drain overlap region due to the thin gate oxide. Experimental and numerical results of breakdown voltage versus Qp (fig.10) show that this second kind of drain region allows a wider range of Qp variation, exhibiting more uniform distribution of the electric field in the whole structure. For Qp>3.0*10E12-cm-2 the calculated breakdown voltage is dependent on the value of the fixed oxide charge (Qf), because the breakdown occurs at the surface. The Qf value of 5.0*10E11-cm-2 at which there is a good agreement between experimental and calculated breakdown voltage values is a fitting value that corrects those surface effects (surface states, surface scattering and charge injection) not taken into account in the calculation of the ionization integrals (15).

In the dose range from 1.0 to 3.0*10E12-cm-2 the optimum value for the drain extension length is Lde = 30-μm (fig.10).

The tradeoff between the maximum breakdown and minimum Ron*Z (Z=channel width)

values (fig.11) is achieved with an implant dose of 2.5*10E12-cm-2.

In table 2 are summarized the typical high voltage device data.

## CONCLUSION

The junction isolated mixed process, described in this paper, allows to integrate LV components, HV P-ch. MOS and HV vertical DMOS suitable for low side, high side and push pull circuitry configurations. An extra mask allows the implementation of a HV low leakage diode. The optimum device parameter tradeoff has been obtained through device simulation and process tests.
A triplanar field plate for the HV vertical DMOS and a double doped drain extension for the HV P-ch. MOS were chosen as junction edge terminations.

## ACKNOWLEDGMENTS

We wish to thank L.Zullino for her support in device simulation, G.Siepe for test measurements and U.Mastromatteo for his contribution in the preparation of the samples and for his helpful discussions.

## REFERENCES

(1) Siliconix, Electronic Design, pp. 37-38, Feb.9, 1984

(2) E.G.Wildi, J.P.Walden and M.S.Adler, "A 500-V/25-A half-bridge IC with on-chip control logic", ISSCC Tech.Dig., pp.266-267, Feb. 1985

(3) P.G.Blanken and P.van der Zee, "An integrated 8-MHz video output amplifier", IEEE Trans.Cons.Electron., vol.CE-31, no.3, pp.109-118, 1985

(4) R.S.Wrathall, "The design of a high power solid state automotive switch in CMOS-VDMOS technology", 16th PESC Tech.Dig., pp.229-233, June 1985

(5) C.Cini, C.Diazzi and D.Rossi, "A new high frequency, high efficiency mixed technology motor driver IC", ESSCIRC, Delft, Sept. 1986

(6) C.Cini, C.Diazzi, D.Rossi and S.Storti, "High side monolithic switch in Multipower BCD technology", Electronica 86, Munich, Nov. 1986

(7) C.Cini, C.Diazzi and D.Rossi, "High frequency high current monolithic switching regulator in Bipolar CMOS DMOS mixed technology", PCI Munich, June 1986

(8) A.Andreini, C.Contiero and P.Galbiati, "A new integrated silicon gate technology combining Bipolar linear, CMOS logic and DMOS power parts, IEEE Trans.Electron.Dev., vol.ED-33, no.12, Dec. 1986

(9) G.Baccarani, R.Guerrieri, P.Ciampolini and M.Rudan, "HFIELDS: a highly flexible 2-D semiconductor device analysis program", Proc.of NASECODE IV, pp.3-12, Dublin, June 1985

(10) C.Lombardi, M.Vanzi and E.Torri, "IDAS: an interactive device analysis environment", Proc.of NASECODE IV, pp.384-389, Dublin, June 1985

(11) F.Bertotti, V.Borghese and B.Murari, "Video stages IC implemented with new rugged junction isolation technology", IEEE Trans.Cons.Electron., vol.CE-27, no.3, pp.295-303, Aug. 1981

(12) M.N.Darwish, K.Board, "Optimization of breakdown voltage and on resistai of VDMOS transistors", IEEE Trans.Electron.Dev., vol.ED-31, no.12, Dec.
(13) F.Conti, M.Conti, "Surface breakdown in silicon planar diodes equipped with field plate", Sol.State Electron., vol.15, pp.93-105, 1972
(14) S.C.Sun, J.D.Plummer, "Modeling of the on resistance of LDMOS, VDMOS and VMOS power transistors", IEEE Trans.Electron.Dev., vol.ED-27, no.2, Feb. 1980
(15) R.Van Overstraeten, H.De Man, "Measurement of the ionization rates in diffused silicon P-N junctions", Sol.State Electron., vol.13, pp.583-60 1970

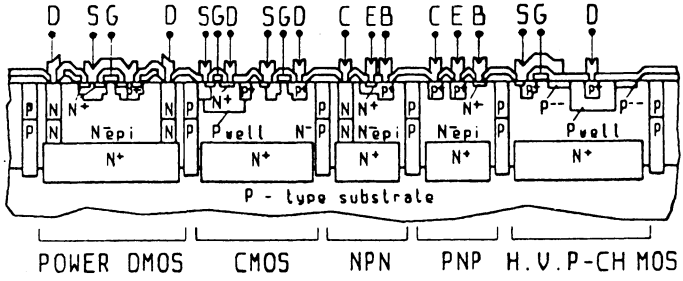



fig.1 Cross section of Multipower BCD 250-V technology

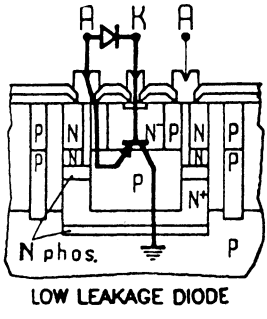



fig.2 LLD and parasitic PNP

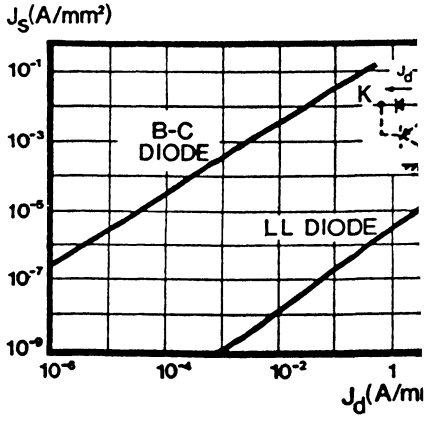



fig.3 Comparison of current lost towards the substrate of the parasit PNP for LLD and conventional base collectoe diode

## Table 1

SIGNAL DEVICES

| | $h_{FE}$ | $LV_{ceo}$ (V) | $BV_{cbo}$ (V) | $BV_{ebo}$ (V) |
|---|---|---|---|---|
| NPN1 (•) | 200 | 75 | 180 | 18 |
| NPN2 (•) | 35 | 120 | 130 | 8 |
| LPNP (L=18u) | 60 | 80 | 150 | 190 |

(•) NPN1: P-well base, NPN2: DMOS P-body base

| | | $V_{th}$ (V) | $BV_{dss}$ (V) | $g_m/Z$ (S/cm) $V_{gs}$=10V, $V_{ds}$=5V | $R_{on}\cdot Z$ (Ω·cm) $V_{gs}$=10V, $V_{ds}$=0.1V | $T_{delay}$ (nsec) fan out=1 |
|---|---|---|---|---|---|---|
| CMOS | N-ch | 1.0 | 18 | 0.16 | 1.9 | 24 at $V_{dd}$=5V |
| | P-ch | 1.2 | 20 | $5\cdot10^{-4}$ | 24 | 10 at $V_{dd}$=10V |

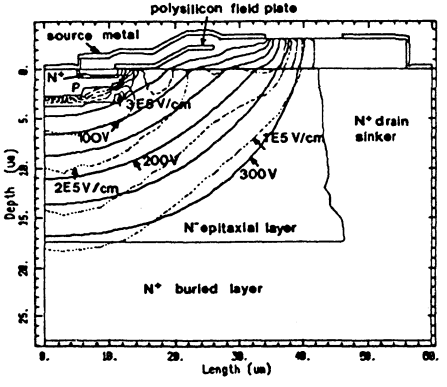



fig.4 Cross section of the triplanar field plate

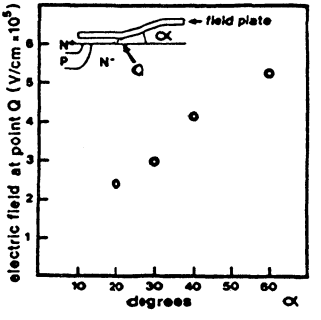



fig.5 Relationship between electric field at point Q and angle α

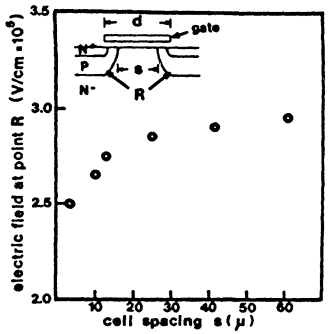



fig.6 Relationship between electric field at point R and cell spacing (s)

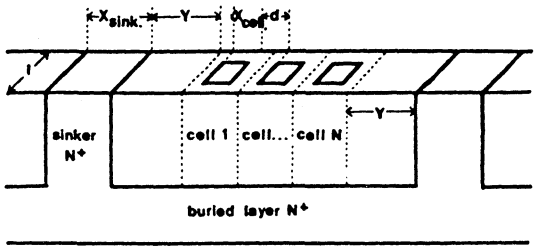



fig.7 Model of the integrated VDMOS for the Ron*Area calculation

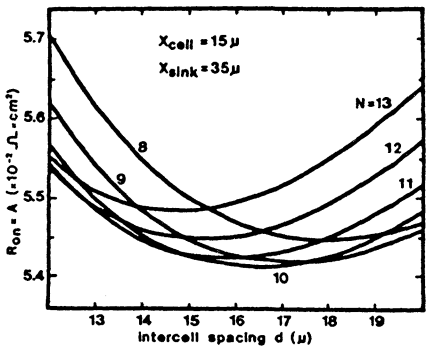



fig.8 Theoretical Ron*Area as a function of DMOS gate width (d) and number of cells (N) between two drain sinker contacts

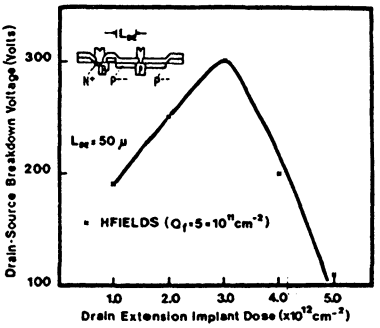



fig.9 Theoretical HV P-ch. MOS BVdss versus drain extension implanted charge Qp

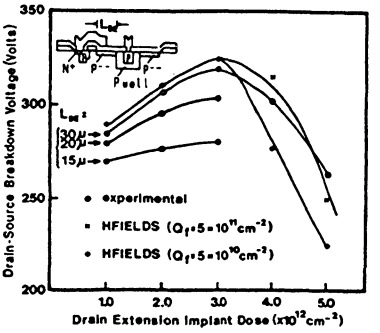



fig.10 Theoretical and measured BVdss as a function of implanted charge Qp and drain extension length Lde for the improved HV P-ch. MOS structure

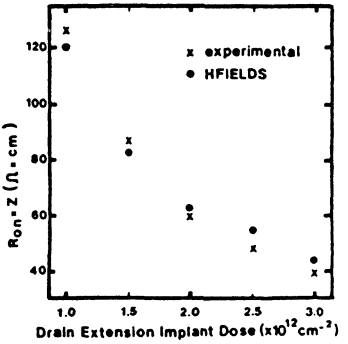



fig.11 HV P-ch. MOS Ron*Z product versus drain extension implant dose

**Table 2** HIGH VOLTAGE DEVICES

| | $V_{th}$ (V) | $BV_{dss}$ (V) | $g_m/Z$ (S/cm) $V_{gs}$=10V, $V_{ds}$=5V | $R_{on}\cdot Z$ (Ω·cm) $V_{gs}$=10V, $V_{ds}$=0.1V | $R_{on}\cdot Area$ (Ω·cm$^2$) $V_{gs}$=10V, $V_{ds}$=0.1V |
|---|---|---|---|---|---|
| P-ch MOS | 1.2 | 320 | 0.037 | 44 | |
| N-ch DMOS | 3 | 315 | 0.11 | | $5.2\cdot10^{-2}$ |

Proceedings of The Electrochemical Society, PV 1987-13, 41-50 (1987)
DOI: 10.1149/198713.0041PV © The Electrochemical Society

# MODELLING OF CMOS COMPATIBLE HIGH VOLTAGE DEVICE STRUCTURES

Z. Parpia, C. Andre .T. Salama,
Department of Electrical Engineering,
University of Toronto,
Toronto, Ontario, Canada. M5S 1A4

and R. Hadaway
Northern Telecom Electronics,
Nepean, Ontario, Canada. K2H 8V4

## ABSTRACT

The implementation and modelling of high voltage MOS transistors in a standard CMOS technology is described. High voltage n- and p- channel transistors, with breakdown voltages of 50 V and 180 V respectively, have been fabricated. Two dimensional device simulations are used to provide supporting evidence for the development of a simple SPICE compatible model, consisting of conventional MOSFETs and JFETS, which can be used to simulate the behaviour of these high voltage devices. The accuracy of the model is verified by comparison with experimental results.

## 1. INTRODUCTION

In high voltage integrated circuits (HVICs), it is imperative that high and low voltage transistors be fabricated on the same chip. Because of the unique requirements of the high voltage transistors, HVICs are typically fabricated using a specialized technology. However, considerable savings in cost and development time can be achieved if an existing low voltage technology can be used to fabricate HVICs. Several approaches aimed at integrating high voltage transistors in existing NMOS [1-3], bipolar [4], and CMOS [5, 6] technologies, have been proposed. However, these approaches all require additional processing steps resulting in reduced accessibility and additional expense.

In this study, high voltage transistor structures fabricated using a standard CMOS technology, without any additional processing steps, are presented. Using information derived from two-dimensional simulations and experimental results, SPICE models for the devices are developed and verified.

## 2. DEVICE STRUCTURE

The cross-sections of the CMOS compatible n- and p-channel extended drain transistors are shown in Figs. 1(a) and (b) respectively. In both transistors, the highly doped drain contact diffusion is separated from the channel by a lightly doped drift region. This region serves to reduce the electric field at the gate/drain interface, resulting in higher breakdown voltages. The n-guard implant is used as the n-channel device drift region, while the p-well forms the p-channel device drift region. In both

cases, part of the source metal extends over the polysilicon gate and overlaps the drift region, acting as a field plate to reduce the electric field intensity near the gate edge and increase the drain breakdown voltage.

The high voltage transistors have structures similar to those of their low voltage counterparts, in that the n-channel device is fabricated inside a p-well and the p-channel transistor is formed in the n-substrate. The gate electrodes of both devices are self aligned with respect to their sources, but not with respect to the drift regions. As a result, the gate electrode overlaps that region.

The n-channel transistor is isolated from the rest of the chip by the p-well it is fabricated within. The p-well also allows the n-channel source to be referenced at high voltages below the substrate potential. The p-channel drain is isolated by the reverse biased p-well/n-substrate junction, thus allowing it to swing to high negative voltages relative to the substrate voltage. Therefore, in applications where the high voltage supply is negative with respect to the substrate (which is typically at the logic power supply level), no extra processing steps are required to provide isolation between the high voltage devices and the rest of the chip. This is typically the case in telecommunication applications where -48 V battery voltages are used.

## 3. EXPERIMENTAL RESULTS

The n- and p-channel high voltage transistors were fabricated using a 5 $\mu$m analog/digital CMOS process.* Since no process changes were required to implement these devices, the performance of the low voltage CMOS devices was not affected.

The I-V characteristics of the n- and p-channel transistors, with drawn channel lengths of 5$\mu$m and 11$\mu$m respectively, are shown on Figs. 2(a) and (b) respectively. The breakdown voltage of the n-channel transistor (at $V_G = 0$) is 50 V, while the corresponding breakdown voltage of the p-channel transistor is 180 V.

In the case of the n-channel transistor, the breakdown voltage is reduced, at gate voltages greater than zero. The breakdown characteristics are similar to those obtained in short-channel MOSFETs and as shown by Hsu et al [7] this breakdown is caused by the turn on of the extrinsic bipolar transistor in parallel with the MOSFET. The rapid increase in the drain current, at drain voltages lower than the avalanche breakdown voltage, is due to the weak avalanche multiplication of the substrate current, which results in the turn on of the extrinsic bipolar in parallel with the MOSFET. is to increase the gate overlap over the drift region. The weak avalanche breakdown effect was not observed in the p-channel devices because of the much lower ionization rate of holes compared to electrons.

The high voltage transistor characteristics are summarized on Table I. The p-channel requires a longer channel length than the n-channel transistor because of the higher lateral diffusion of the p-well as well as higher channel length modulation effects in the saturation region. The much lower on-resistance and transconductance of

* In this process, the devices are fabricated on a 5 $\Omega$–cm n-type (100) silicon substrate. An ion implanted p-well is used for the fabrication of the low voltage n-channel transistors. Isolation between the devices is provided by a 1$\mu$m LOCOS field oxide. The process uses a 850 Å gate oxides and $n^+$ polysilicon gates. The magnitude of the threshold voltages for both n- and p-channel transistors is approximately 1 V.

the n-channel transistor, compared to the p-channel transistor, are due to the very low drift region concentration as well as the gate overlap over the drift region. As will be shown in the next section, the gate overlap can significantly affect the device behaviour.

## 4. DEVICE MODELLING

In this study, two dimensional simulations were carried out to investigate the high voltage behaviours of the fabricated devices. The main objective of these simulations was to gain insight into device operation as well as help in the generation of SPICE models for these devices. The numerical simulator used was PISCES-IIB, a two-dimensional simulator developed by Pinto et al [8]. Two dimensional solutions of the Poisson and continuity equations, for single carriers (electrons for the n-channel transistor and holes for the p-channel transistor) were obtained.

Figs. 3(a) and (b) show the depletion regions in the n- and p- channel transitors respectively, at various drain voltages. At low drain voltages, the extension of the depletion region into the drift layer is small, hence the drift layer operates like a resistor. As the drain voltage is increased, the depletion region in the drift layer under the source field plate, is modulated by the field plate as well as by the substrate potentials. At drain voltages $V_D$ = 6.5 V and $V_D$ = -30 V, for the n- and p-channel transistors respectively, the drift region under the field plate is completely depleted, as shown on Fig. 3. Thus, the behaviour of this setion of the drift region is similar to that of a JFET, with a pinchoff voltage equal to the voltage required to completely deplete this section.

As the drain voltage is further increased, the depletion region in the rest of the drift layer, which is modulated solely by the substrate potential, widens. As shown in Fig. 3, at drain voltages $V_D$ = 8.5 V and $V_D$ = -90 V in the n- and p- channel transistors respectively, the drift layer is completely depleted. Therefore, this section of the drift layer can also be modelled by a JFET, with a pinchoff voltage equal to the voltage required to completely deplete this section.

Fig. 4(a) shows an idealized cross-section of the extended drain transistor used in the model derivation. In order to simplify the analysis, the gate overlap over the drift region has been neglected. As shown by the two-dimensional simulations, the behaviour of the two drift regions resembles that of JFETs. Consequently, the drift region can be modelled by a series combination of two JFETS, as shown on Fig. 4(b). Here, JFET J1, with a pinchoff voltage $V_{P1}$ models the drift region under the source field plate, while JFET J2, with pinchoff voltage $V_{P2}$ models the rest of the drift layer. The MOSFET M1 models the channel under the gate electrode.

The operation of the extended drain transistor can be divided into the linear or triode region, where the drain current varies approximately linearly with the applied drain voltage, and the saturation region where the drain current is relatively indepedent of the drain voltage. The idealized output I-V characteristics are shown on Fig. 5. The various modes of operation shown on this diagram are listed in Table II and are identified by the letters A to F.

In the linear region (mode A operation), all three transistors operate in their respective triode regions. The overall device on-resistance is given as the sum of the individual on-resistances. In saturation, at low gate voltages (mode B operation), the

device operation is dominated by the MOS transistor M1. Consequently, the extended drain transistor current, in this mode, will be equivalent to that of it's low voltage counterpart. As the drain voltage is increased, most of the voltage is dropped across M1, causing channel length modulation and resulting in a finite output resistance in the I-V characteristics of Fig. 5. This is shown in the two-dimensional results, of Fig. 3, by a widening of the depletion region into the channel region.

As the drain voltage is further increased, the drift region under the source field plate pinches off, corresponding to the saturation of J1, resulting in mode C operation. Once this occurs, as shown in the simulation results of Fig. 3, further widening of the depletion region into the channel is small compared to the vertical extension. This results in less channel length modulation, hence lower output conductances. In circuit terms, the lower output conductance is the result of the cascode configuration of the equivalent circuit. Most of the applied drain voltage now appears across J1, effectively isolating the drift region near the gate electrode from further increase in the drain voltage. When the drain voltage exceeds $-V_{P2}$, JFET J2 saturates and now sustains most of the additional drain voltage, resulting in mode D operation and even lower output conductances.

At high gate voltages, J1 saturates before M1 (resulting in mode E operation). In contrast to operation in mode B, the transconductance in this region falls with increasing gate voltage. As a result the device current is no longer controlled by the gate electrode, but by the substrate controlled JFET J1. Hence, the drain current tends to saturate to a value determined by the drift region parameters. Thus, the JFET J1 is important in determining the maximum current handling capability of the extended drain transistor. The JFET J1 now sustains most of the applied drain voltage, until J2 saturates (which results in mode F operation).

When the drift region is shallow and lightly doped, as in the case of the n-channel transistor, the gate overlap can significantly affect the device behaviour. In this case, the MOS transistor (M1) of Fig. 4(b) has to be replaced by a series combination of two MOS transistors, M1 which models the channel region and M2 which models the gate overlap over the drift region (see Fig. 4(c)). Generally, the device characteristics in the MOS controlled regime are typically dominated by M2.

From the above analysis, it is clear that the pinchoff voltages of the two sections of the drift layer can play an important role in determining the overall device breakdown voltage. In the case of the n-channel transistor, due to the lightly doped nature of it's drift region, the source field plate has only a small effect on the pinchoff voltage. Consequently, most of the potential drop appears in the drift region not covered by the field plate. This is illustrated in Fig. 6(a), which shows the simulated off-state potential contours in the n-channel transistor. The potential contours become crowded near the $n^+$ drain, indicating high electric fields and causing avalanche breakdown to occur in that region, at relatively low drain voltages.

In the p-channel device, the drift region is relatively highly doped, and the source field plate significantly lowers the pinchoff voltage, resulting in more evenly spread potential contours across the drift region, as shown in Fig. 6(b). Most of the potential drop above $V_D$ = -90 V occurs across the drift layer beneath the source field plate. The potential drop below $V_D$ = -90 V appears across the rest of the drift region. Potential contour crowding near the $p^+$ drain begins to occur at $V_D \approx$ -180 V.

Hence, the p-channel drift region doping and depth correspond more closely to an optimized design than the n-channel drift region.

## 5. COMPARISON WITH EXPERIMENTAL RESULTS

In order to prove the validity of the extended drain transistor model derived in the previous sections, this model was implemented in the SPICE circuit simulation program. Using parameters extracted from the fabricated devices and from the compatible low voltage CMOS transistors, SPICE simulations of the extended drain transistor characteristics were carried out. The resulting simulated I-V characteristics for both devices are shown on Fig. 7. In the case of the n-channel transistor, the agreement between experimental and simulated characteristics is very good at low drain voltages ($\pm 5\%$ for $V_D < 20$ V). However, because of the weak avalanche breakdown effect at higher drain voltages, the discrepancy between simulation and experimental results is higher. In the case of the p-channel transistor, the matching is extremely good even at high voltages ($\pm 5\%$ for $V_D$ up to 100 V).

The n-channel device characteristics, at low gate voltages, were found to be dominated by the gate overlap transistor. This fact combined with the low drift pinchoff voltage, significantly reduced the saturation drain current of the device. On the other hand, in the p-channel transistor, the gate overlap transistor had virtually no effect on the device characteristics and could therefore by neglected in the simulations. As a result the p-channel transistor current in the saturation region is comparable to that of it's low voltage counterpart.

## 6. CONCLUSIONS

The feasibility of implementing high voltage transistors in a standard CMOS process, without process changes, has been investigated. High voltage n- and p-channel transistors, with breakdown voltages of 50 V and 180 V respectively have been fabricated. In addition, no extra processing steps are required to isolate these devices from the rest of the chip.

In order to simulate the performances of these transistors, a general model for the extended drain transistors was also presented. The main advantages of this model are that it is general enough to be applied to most extended drain as well as other high voltage structures (such as the lateral RESURF DMOS transistor) and can be used in conjunction with general purpose circuit simulators such as SPICE. The accuracy of the model was verified by it's ability to accurately simulate the behaviour of the fabricated high voltage transistors.

## ACKNOWLEDGEMENTS

The authors would like to thank Jose Mena and Stephen Wong for their contributions. This work was supported by Northern Telecom Electronics and the Natural Sciences and Engineering Research Council of Canada.

## REFERENCES

[1] T. Yamaguchi and S. Morimoto, "Process and device design of a 1000 V MOS IC," *IEEE Trans. Electron Devices*, vol. **ED-29**, pp. 1171-1178, 1982.

[2] R.S. Abbott, J.P. Ellul, R.A. Hadaway, and J.J. White, "High-Voltage N-Channel Metal-Oxide-Semiconductor Technology," *Can. J. Phys.*, vol. **63**, pp. 897-900, 1985.

[3] R. Martin, S. Buhler, and G. Lao, "850V NMOS Driver With Active Outputs," *IEDM Tech. Dig.*, pp. 266-269, 1984.

[4] A.W. Ludikhuize, "High voltage DMOS and PMOS in analog ICs," *Proc. Int. Electron Devices Meeting, Washington, D.C.*, pp. 81-84, 1982.

[5] W.G. Meyer, G.W. Dick, K.H. Olson, K.H. Lee, and J.A. Shimer, "Integrable High Voltage CMOS: Devices, Process Applications," *IEDM Tech. Dig.*, pp. 732-735, 1985.

[6] G.M. Dolny, O.H. Schade Jr., B. Goldsmith, and L.A. Goodman, "Enhanced CMOS for Analog-Digital Power IC Applications," *IEEE Trans. Electron Devices*, vol. **ED-33**, pp. 1985-1991, Dec. 1986.

[7] F-C. Hsu, R.S. Muller, and C. Hu, "A Simplified Model of Short-Channel MOSFET Characteristics in the Breakdown Mode," *IEEE Trans. Electron Devices*, vol. **ED-30**, pp. 571-576, 1983.

[8] M.R. Pinto, C.S. Rafferty, H.R. Yeager, and R.W. Dutton, "PISCES-IIB," *Stanford Electronics Lab., Dept. of Electrical Eng., Stanford Univ.*, 1985.

**TABLE I: DEVICE CHARACTERISTICS**

| Parameter | Transistor | |
|---|---|---|
| | n-channel | p-channel |
| $L_{eff}$ ($\mu$m) | 4.2 | 7.5 |
| $W_{eff}$ ($\mu$m) | 120 | 120 |
| $V_T$ (V) | 1.01 V | -1.01 V |
| $R^*_{ON}$ (k$\Omega$) | 5.58 | 1.92 |
| BV (V) | 50 | 180 |
| $g_m$(max) (A/V) | $4.3\times10^{-5}$ | $7.7\times10^{-4}$ |

*measured at $V_{GS}=\pm10$ V, $V_{DS}=\pm0.1$ V

**TABLE II: DEVICE OPERATING MODES**

| M1 | J1 | J2 | MODE | | REGION |
|---|---|---|---|---|---|
| TRIODE | TRIODE | TRIODE | A | | Linear |
| SAT. | TRIODE | TRIODE | B | MOS Control | Saturation |
| SAT. | SAT. | TRIODE | C | | |
| SAT. | SAT. | SAT. | D | | |
| TRIODE | SAT. | TRIODE | E | JFET Control | |
| TRIODE | SAT. | SAT. | F | | |

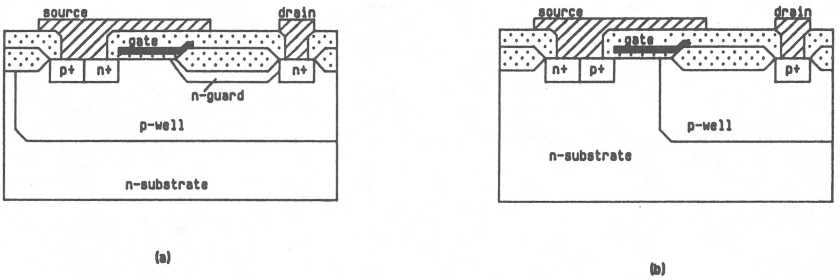



Fig. 1 High voltage transistor cross-sections
(a) n-channel extended drain transistor
(b) p-channel extended drain transistor

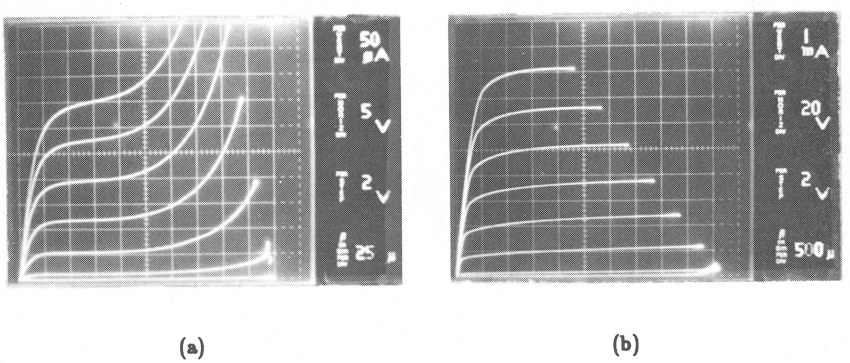



Fig. 2 I-V characteristics of fabricated transistors
(a) n-channel transistor
(b) p-channel transistor

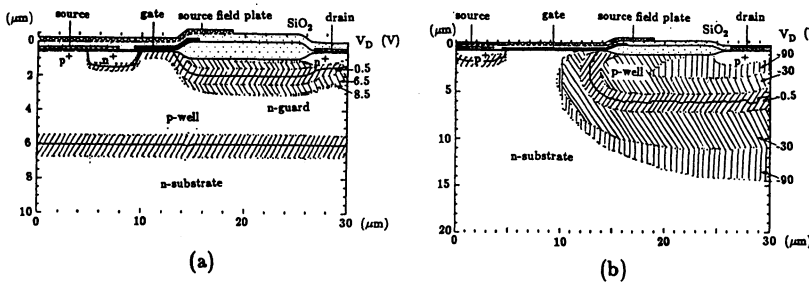



Fig. 3 Depletion regions at various drain voltages
(a) n-channel transistor
(b) p-channel transistor

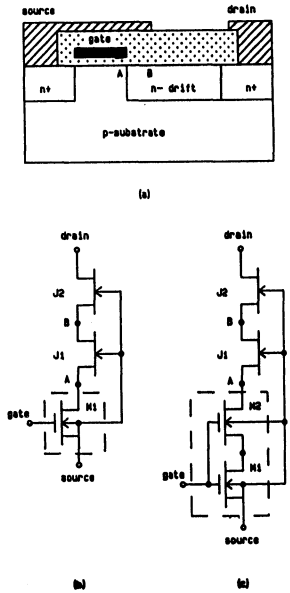



Fig. 4 Extended drain transistor models
(a) simplified device cross-section
(b) equivalent circuit neglecting gate overlap
(c) equivalent circuit including gate overlap

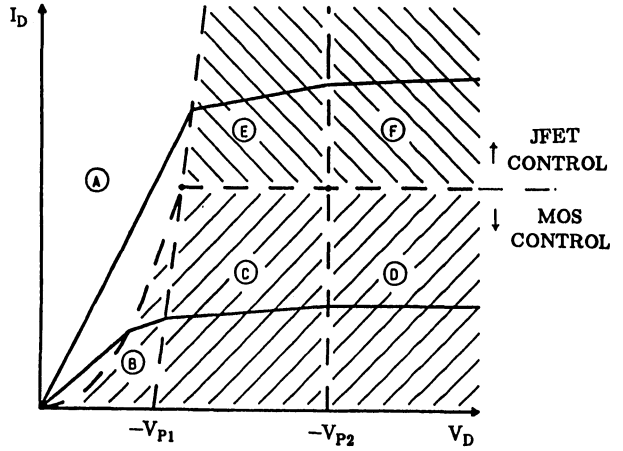



Fig. 5 Theoretical I-V characteristics of the extended drain transistor, showing the various modes of operation

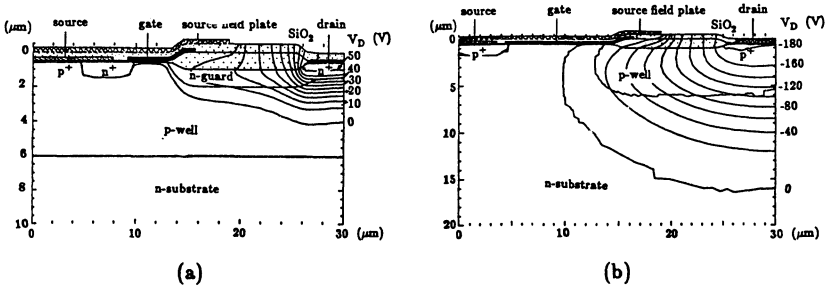
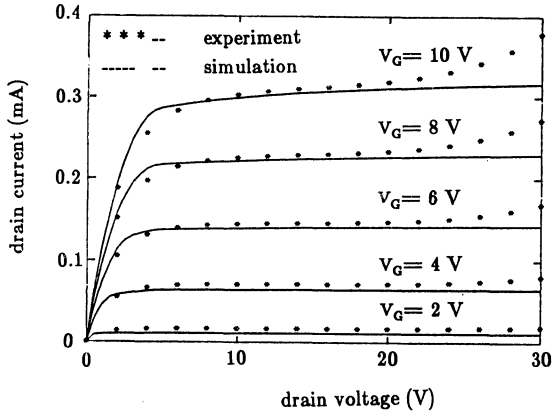
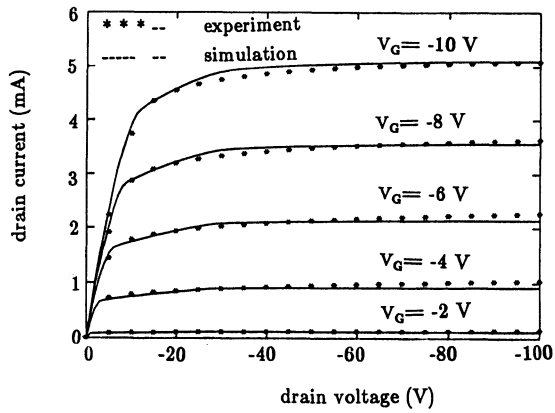



Fig. 6 Off-state potential contours
(a) n-channel transistor
(b) p-channel transistor




(a)




(b)

Fig. 7 Simulated and Experimental I-V characteristics
(a) n-channel
(b) p-channel

Proceedings of The Electrochemical Society, PV 1987-13, 51-59 (1987)
DOI: 10.1149/198713.0051PV © The Electrochemical Society

# HIGH VOLTAGE COMPLEMENTARY MOSFET TECHNOLOGY FOR FLAT-PANEL DISPLAY DRIVER ICs

Takeaki OKABE, Kouzou SAKAMOTO, Masatoshi KIMURA and Koichiro SATONAKA*

Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo 185, Japan
*Takasaki Works, Hitachi, Ltd, Takasaki, Gunma 370-11, Japan

Abstract — This paper describes the complementary high-voltage MOSFETs for flat-panel display driver ICs. The fabrication process was based on Semi-Well Isolation and a standard poly-Si gate CMOS processes. As for high-voltage n-channel MOSFETs, LDMOS, VDMOS and BDL DMOS were discussed. For small current usage, LDMOS and BDL DMOS are suitable as a pull-down and a pull-up devices, respectively. A p-channel MOSFET for current source was realized introducing p+ island within offset drain region. Using these devices, an 8-output experimental driver IC, which can operate up to 300V, has been fabricated.

## INTRODUCTION

Recently, flat-panel displays such as plasma, EL or VFD have been extensively studied to provide low cost and full color displays competing with CRTs. Consequently, low cost electronic drivers are bound to play an important role in the flat display system.

Various kinds of high-voltage devices and isolation structures have been already developed [1] - [3]. For flat-panel display drivers, voltage ranges from 30V for LCD to 300V for EL. In addition, a push-pull configuration is preferable from the standpoint of compact circuit design. To satisfy these requirements, an appropriate combination of devices and isolation structure is needed.

To provide a cost effective chip integrating logic with high-voltage devices, the CMOS/high-voltage MOSFETs approach seems to be the most appropriate one from the viewpoint of process complexity. Various types of high-voltage MOSFETs

have been realized and discussed earlier as discrete power devices [4], [5]. In an output circuit of a flat-panel display driver IC, a smaller current is used compared with a power device. Thus, discussion is needed on providing optimum devices to realize an effective driver IC.

In this paper, various types of high-voltage MOSFETs are discussed. A combination of devices to implement driver circuits in the cost-effective pn junction isolation structure is also considered. To show the validity of this approach, an 8-output experimental driver IC was realized.

## FABRICATION PROCESS and ISOLATION STRUCTURE

It is desirable that isolation occupies a minimum die area which means the usage of a thin epitaxial layer for shallow pn junction isolation diffusion. On the other hand, for high voltage devices, a thicker epitaxial layer is needed because the voltage is supported in the bulk of the semiconductor. To satisfy this requirement, Semi-Well Isolation(SWI) structure having two epi-layers of different thickness has been developed[1]. The cross-section of SWI is shown in Fig.1. The starting material is 30ohm-cm p-type silicon and the key steps are summarized as follows:

1) well formation for thick epi-layer;
2) n+ buried layer diffusion;
3) epi-layer growth of a 20ohm-cm n-layer;
4) leveling of the surface to adjust the thickness of the epi-layer;
5) p+ isolation and n+ contact diffusions.

The cross-sections after epi-growth and leveling process are shown in Fig.2. As seen from the figure, slight roughness exists near the well edge; however, the increment is rather small and causes little problem in the photolithographic process.

High-voltage MOSFETs are made in the thick and thin epi-layers, and CMOS logic is made in the thin epi-layer. The core of the fabrication sequence is a standard poly-silicon gate CMOS process. Two mask levels are introduced to integrate high-voltage n-channel and p-channel MOSFETs. Other process steps for high-voltage MOSFETs are commonly used with the CMOS process. For instance, an n-well for the

formation of low-voltage p-channel CMOS is used as the punch-through stopper and also as the Vth control of high-voltage PMOS.

## HIGH-VOLTAGE MOSFETs

As for high-voltage devices, three types of n-channel MOSFETs and a lateral PMOS are studied, as shown in Fig.3.

### A. N-channel MOSFETs

In a high-voltage MOSFET, as the greater part of the applied voltage is supported in the bulk, the basic structure has a high-resistive conducting layer in series with the MOS channel. Source-substrate connected Lateral DMOS(LDMOS), shown in Fig.3(a), is realized in the thin epi-layer without an n+ buried layer. The thin epi-layer acts as a pinch-resistor which sustains high voltage. Since current flows in the thin epi-layer laterally, a thinner epi-layer gives a larger on-resistance.

Vertical DMOS(VDMOS) is well known as a discrete power device. In a high-voltage IC, VDMOS has an additional n+ buried layer and a deep n+ contact diffusion. The spacing between the deep n+ diffusion and the p+ isolation is the same as the distance between the source and the drain. Since current flows vertically from the MOS channel formed near the gate edge, the on-resistance is affected by the spacing between the channels; wider spacing is preferable for the reduction of on-resistance, but the cell area becomes large.

Utilizing the whole bulk as the current path and reducing on-resistance, a lateral and vertical mixed structure, called BDL( Buried Drain Lateral structure) DMOS, was proposed and realized by the authors[6]. This structure has the same spacings between source and drain, and n+ drain diffusion and p+ isolation as those of VDMOS. However, the gate area becomes smaller, resulting in a smaller cell area.

For the usage of small output current, current handling capability of the three types of MOSFETs with single stripe layout are compared. The relation between current normalized by feature size and breakdown voltage is shown in Fig.4. LDMOS seems to be the most appropriate for compact output circuits, but this type can be used only as a pull-down device. As for a pull-up device, BDL or VDMOS must be used.

Typical characteristics of the fabricated MOSFETs are listed in Table 1. The breakdown voltages and threshold voltages are the same for three devices, while the current handling capability changes as mentioned above.

The above discussion is restricted to small current MOSFETs. A larger current power device must be realized by placing in parallel a number of unit structures, consequently, VDMOS seems to have superior current handling capability than the others for use in power IC.

B. P-channel MOSFET

To obtain a push-pull output circuit, a high-voltage p-channel device is also required. Lateral PMOS, as shown in Fig.3(d), is realized using a lightly doped offset drain and a gate field-plate. The offset length and doping are sensitive to voltage and on-resistance. These two characteristics are contradictory, and thus, a compromise is needed. Heavily doped n region under the gate, introduced to prevent punch-through breakdown, reduces the doping level of the offset region near the gate. Thus, a low pinch-off voltage for the field plated region is attained in spite of the heavy doping for the offset region. This lateral PMOS is suitable for large-current usage, but, it provides rather poor matching characteristics for a current mirror circuit because of its gradual current saturation around the pinch-off region. The gradual saturation is attributed to the light-doping of the offset region near the gate edge. Thus, the structure is modified introducing a p+ diffused island within the offset drain region, as shown in Fig.5. This modified device shows a low-voltage MOSFET in series with a lateral p-channel JFET. A fairly matched current source is easily provided utilizing a low-voltage MOSFET as a diode connected reference device, and a high-voltage modified device as an output device.

The breakdown voltage for two types of lateral p-channel MOSFETs as a function of offset region implanted ion dose is also shown in Fig.5. For the same offset length, a PMOS without the p+ island can attain higher voltage than that of a modified device. However, the longer offset region of the modified device can improve the breakdown voltage at larger ion-dose condition.

## LOGIC CMOS

As mentioned earlier, standard poly-silicon gate CMOS was fabricated in an n-well and a p-well formed on the thin epi-layer of SWI structure. To improve latch-up hardness, n+ buried layer is employed[2]. The electrical parameters of the fabricated CMOS are listed in Table 2.

## DRIVER CIRCUIT

An 8-output experimental driver IC for VFD was designed. To realize an output circuit capable of switching 250V across capacitive load, totem-pole circuit configuration was chosen, as shown in Fig.6. As for pull-up transistor M1 and pull-down transistor M2, BDL DMOS and source-substrate connected LDMOS were used, respectively, because of their compactness. As for current source output device M3, a modified PMOS was employed to match with low-voltage reference transistor M4. Current-voltage characteristics of high-voltage BDL DMOS(M1) and modified PMOS(M3) were shown in Fig. 7. A base-collector shorted bipolar transistor was used as diode D1 because the emitter-substrate capacitance is negligibly small and requires little charging current from M3. In this case, collector-substrate capacitance is added to the output terminal.

A shift register and latches are designed in CMOS to provide a high packing density and minimal power dissipation. The IC was realized using single aluminum metallization to attain low die cost, as shown in Fig.9.

Waveforms showing data input and delayed outputs are shown in Fig.8. This chip can operate up to 300V at a clock frequency greater than 10MHz. Switching times of the output circuit with 15pF of load including parasitic capacitances of measurement circuit, as a function of the pull-up transistor drive current are shown in Fig.10. This figure shows that for small capacitive load the rise time is determined by the charging time of the M1 gate node; in addition, fall time is determined by the discharge time of the parasitic capacitances added mainly at the output terminal. Switching times as a function of load capacitance values were shown in Fig.11. To switch a large load capacitance fast, the current capability of M2 and the bias current of M3 must be increased.

Typical characteristics of the experimental IC are listed in Table 3. Maximum clock frequency is 15MHz at Vcc1=5V. For 5MHz clock operation, logic dissipation power is only 3mW.

## CONCLUSION

High-voltage MOSFETs technology for flat-panel display driver ICs has been described and evaluated. These devices are fabricated in thick and thin epi-layers provided by Semi-Well Isolation technology. Utilizing these devices, an experimental IC chip was fabricated. This IC can operate at up to 300V of output voltage.

## ACKOWLEDGMENT

The authors wish to thank Dr. M. Nagata of the Central Research Laboratory and K. Hoya and T. Nishimura of Takasaki Works for their valuable discussions and support throughout this work.

## REFERENCES

[1] M. Kimura, et al., Proc. 16th Conf. on SSDM, Aug. 1984.
[2] K. Sakamoto,et al., Syp. on VLSI Tech. Digest of Tech. Papers, p.21, May 1986.
[3] B.A. Blanchard, SID82 Digest, p.258, 1982.
[4] T. Okabe, et al., IEEE Trans. on Electron Devices, vol.ED-27, p.334, Feb. 1980.
[5] S.C Sun, et al., IEEE Trans. on Electron Devices, vol.ED-27, p.356, Feb. 1980.
[6] K. Sakamoto, et al.,Papers of Tech. group on Transistors, IECE Japan, SSD85-23, July 1985

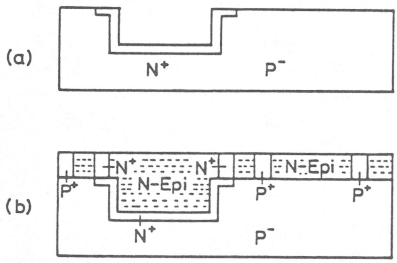



Fig.1.
Formation of pn junction isolated area.
(Semi-Well Isolation : SWI)

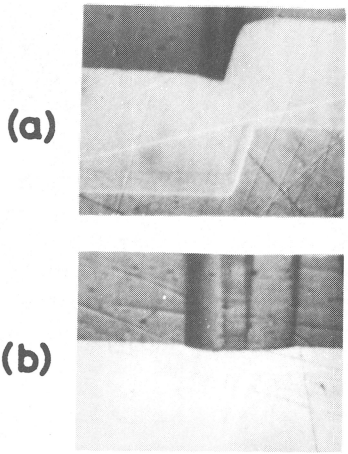



Fig.2.
Cross-sections of SWI steps :
(a) Epi growth. (b) Leveling.

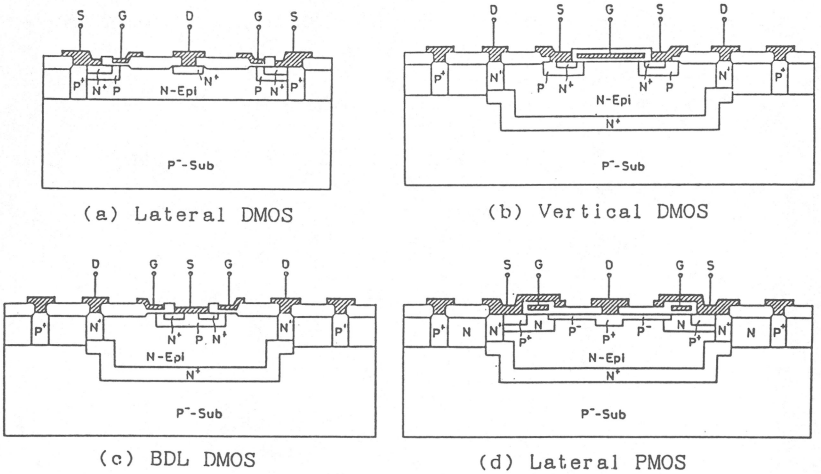



Fig.3 Cross-sections of various types of high-voltage MOSFETs.

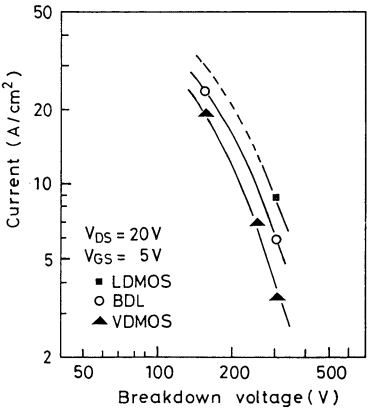



Fig.4.
Current handling capability as a function of breakdown voltage.

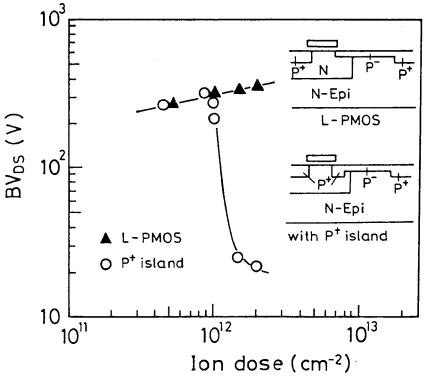



Fig.5.
Breakdown voltage as a function of offset region implant dose.

Table 1
High-voltage N-channel MOSFETs

| | LDMOS | VDMOS | BDL DMOS |
|---|---|---|---|
| $BV_{DS}$ (V) | 320 | 320 | 320 |
| $V_T$ (V) | 2 | 2 | 2 |
| Current ($A/cm^2$) | 8.6 | 3.5 | 5.8 |

Table 2 CMOS

| | N-ch | P-ch |
|---|---|---|
| $V_T$ | 1 V | 1 V |
| $g_m$ (W=200μm) | 2 mS | 1.2 mS |
| Gate delay | $t_{pd}$= 7 ns/gate ($V_{CC1}$= 5V) | |

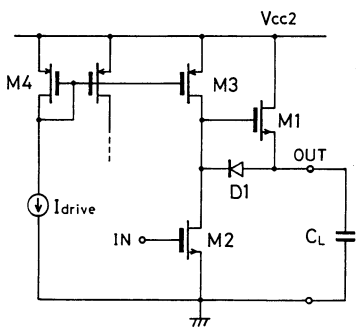



Fig.6.
Totem-pole push-pull output circuit.

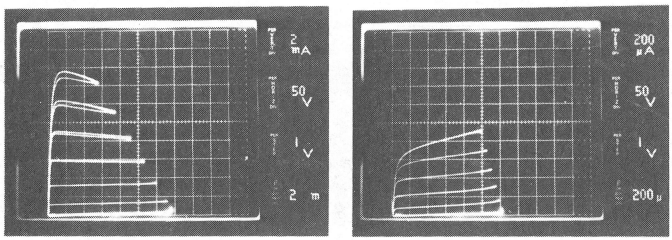



Fig.7. Current-voltage characteristics of the high-voltage MOSFETs.

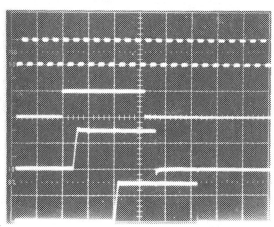



Fig.8. Waveforms of an experimental IC.

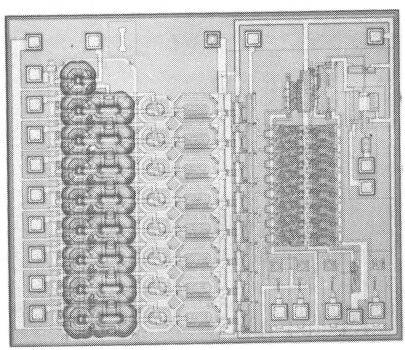


Fig.9. Chip photograph of an 8-output experimental IC.

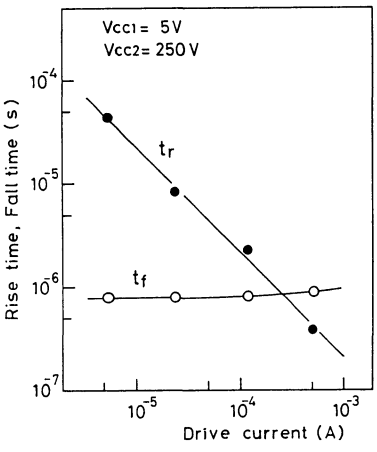



Table 3
Typical characteristics of fabricated IC

| | Value | Condition |
|---|---|---|
| Output voltage | 250 V | |
| Output current<br>Source<br>Sink | <br>10 mA<br>3 mA | $V_{cc2}$ = 200 V<br>$V_{OH}$ = 190 V<br>$V_{OL}$ = 5 V |
| Max. clock frequency | 15 MHz | $V_{cc1}$ = 5 V |
| Logic dissipation power | 3 mW | $V_{cc1}$ = 5 V<br>$f_{CL}$ = 5 MHz |
| Output<br>Rise time<br>Fall time | <br>3 μs<br>0.7 μs | $V_{cc2}$ = 250 V<br>$C_L$ = 15 pF |

Fig.10.
Switching performance of a push-pull output circuit with 15pF load.

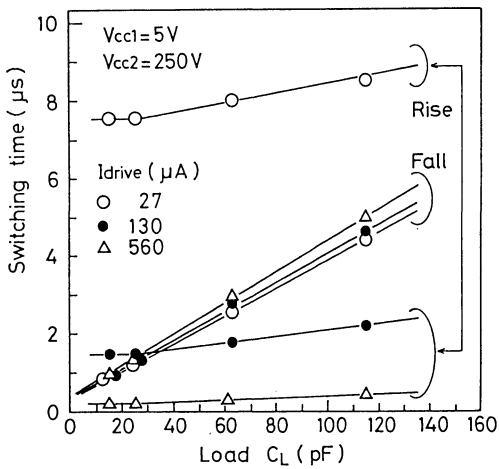



Fig.11. Switching times of the output circuit as a function of load capacitance.

Proceedings of The Electrochemical Society, PV 1987-13, 60-67 (1987)
DOI: 10.1149/198713.0060PV © The Electrochemical Society

# HIGH VOLTAGE CMOS: DEVICES AND APPLICATION

W. G. Meyer, G. W. Dick, K. H. Olson,
AT&T - Bell Laboratories
Reading, Pennsylvania 19612-3566

K. H. Lee and J. A. Shimer
AT&T-Bell Laboratories
Allentown, Pennsylvania 18103-1285

## ABSTRACT

A high voltage (HV) CMOS process has been developed. This process allows one to easily create junction isolated HVCMOS structures on the same chip with low voltage (LV) CMOS structures. The HV structures, which are realized in a 3.5μm CMOS technology were designed for and achieved 100V operation. The process allows for the isolation of LV and HV devices and circuits. The technology is suited for applications which require the marriage of LV analog and digital signal processing and control circuitry with HV output buffers and drivers.

## INTRODUCTION

A high voltage (HV) CMOS process has been developed which allows one to make junction isolated HVCMOS structures on the same chip with low voltage (LV) CMOS devices. The HV structures, which are realized by adding one additional photolithographic step to a LV 3.5μm twin tub, SORT (selective-oxidation-reduced-topology) process, were designed for and achieved 100 volt operation. The HVCMOS devices are lateral drift transistors which are built within P-Wells, across n-tub, p-tub boundaries. The P-Well allows one to fabricate individually isolated p- and n-channel HV MOSFETs as well as p- and n-channel LV MOSFETs.

## HIGH AND LOW VOLTAGE CMOS DEVICES

### High Voltage Devices

The complementary HV Devices (Figure 1) were realized by the addition of a P-Well to a twin tub 3.5μm CMOS process. This simple alteration to a standard process allows one to make individually, junction isolated n- and p-channel HV devices. The uniqueness of these devices lies in the way in which they are created. An already existing technology was used with the addition of only an isolation diffusion (P-Well), producing HV devices that are comparable to more complicated double-diffused structures. This was accomplished without affecting the

performance of the LV CMOS devices.

The devices, as depicted in Figure 1, are source-substrate connected structures which are built within P-Wells, across n-tub, p-tub boundaries utilizing degenerately doped polysilicon as the gate electrode.

Typical device I-V characteristics are pictured in Figure 2 for both the n- and p-channel devices. As is evident from Figure 2, both types of devices have a break-down voltage that is greater than 110V. A complete set of typical device characteristics and device operation limits are given in Table 1, for both HV and LV structures. One point to note from Table 1 and Figure 2, is the extremely small, almost zero, output conductance ($g_o$) of both the n- and p-channel HV devices.

A list of Ron (on resistance) as a function of device geometry is given in Table 2. The area resistance product for the HV n- and p-channel devices are $6.6x10^{-2}$ and $9.5x10^{-2}$ $cm^2\Omega$ respectively. These devices compare very favorably with n-channel vertical DMOS devices which have an area-resistance product of $6.7x10^{-2}cm^2\Omega$. (The areas are total area occupied by the device)

Low Voltage Devices

The P-Well, in the HVCMOS process, also serves as an isolation island for LV CMOS devices and circuits, allowing the low voltage circuitry to be isolated from the HV devices. Figure 3 shows some typical LV configurations.

The individual isolated n- and p-channel devices can be very important in analog design. With them we can have source-substrate connected devices that are not tied to either power supply rail. This is very desirable for operational amplifier input stages which need to have their source and substrate referenced to a voltage between the positive and negative power supply rails for proper operation. The isolated devices also afford us the capability of individually modifying the threshold voltage of specific devices by changing the source to substrate potential. This allows us to dynamically match thresholds on two or more devices.

## PROCESSING

The HV CMOS process achieves high voltage structures in the 3.5μm twin-tub, single poly, SORT technology (1) with minimal additions or changes to the process. The high voltage process requires nine mask levels:

P-Well
n-tub
GASAD
$V_t$ adjust
Poly
n+
window
metal
nitride

The processing sequence for a high voltage p-channel transistor is illustrated in Figure 4. The high voltage process requires n/n+ epitaxial material with a doping concentration of approximately $1x10^{14}cm^{-3}$. The first operation involves the creation of a P-Well with a surface concentration of $2x10^{15}cm^{-3}$ via a boron implant and drivein.

In the HVCMOS process, the p-tub implant sets the n-channel threshold voltage for both LV and HV devices. The n-tub implant sets the n-tub profile within the P-Well. A blanket boron chanstop sets the n- and p-tub field thresholds. The combination of tub doping and chanstop also controls the drain to source breakdown voltage of the HV devices.

The $V_T$ adjust is a boron implant which sets the p-channel transistor threshold voltages for both LV and HV devices. Processing from Poly to Nitride is the same as the 3.5μm twin-tub process.

## APPLICATION

The first HVCMOS circuit designed was a high voltage output driver. The driver is a non-inverting level shifter and is depicted schematically in Figure 5. The components of the cell are as follows:

1. M1 and M3 are HVCMOS PCH devices.
2. M2 and M4 are HVCMOS NCH devices.
3. R3 and R4 are p-tub diffused resistors.
4. D1 - zener diode with reverse bias breakdown of ~6.3V, therefore, two in series will clamp the gate-to-source voltage of M3 and M4 to ~12.6V.

The non-inverting level shifter works as follows: if the input (IN) is at potential V1 than the output (OUT) will be at potential V2, if IN is at potential G1, than OUT will be at potential G2. This non-inverting buffer has complete decoupling of bias supplies. It's only limitation is that G2 must be more negative than V1 and G1 must be more negative than V2.

The HV output driver was integrated with low voltage control logic (capable of reliably operating at 7MHz) to make an 8-bit driver circuit. The schematic for this circuit is shown in Figure 6. The circuit consist of an 8-bit shift register and two sets of control gates.

Oscillographs of the operation of one of the outputs of the 8-bit driver circuit are shown in Figure 7. The oscillographs depict operation with V2=100V and G2=OV and with V2=+5V and G2=-95V.

## CONCLUSIONS

We have succeeded in creating a HV CMOS process with 100V capability. The process allows us to effectively integrate low voltage and high voltage functions on the same piece of silicon without compromising the integrity of either.


## ACKNOWLEDGEMENTS

We would like to thank C. A. Bollinger and S. F. Shive for their help with wafer fabrication and final process definition and C. A. Goodwin and K. H. Oh for their support and advice during the course of the development.


## REFERENCES


[1] L. C. Parrillo, R. S. Payne, R. E. Davis, G. W. R. Reutlinger, T. L. Field, "Twin-Tub CMOS-A Technology for VLSI Circuits," IEDM paper 29.1, December 1980.


TABLE 1
HV and LV Device Characteristics[a]

| | HV | | LV | |
|---|---|---|---|---|
| | NCH | PCH | NCH | PCH |
| $gm(\frac{A}{V})$ | $4.0x10^{-6}$ | $1.3x10^{-6}$ | $4.2x10^{-6}$ | $1.2x10^{-6}$ |
| $g_o\ (\frac{A}{V})$ | $5.7x10^{-7}$ | $2.0x10^{-8}$ | $4.0x10^{-8}$ | $8x10^{-8}$ |
| $R_{on}(\Omega)$ | 8550 | 15270 | 4080 | 14900 |
| $V_T(V)$ | 0.8 | -0.8 | 0.8 | -0.8 |
| BV(V) | 135 | -135 | 22 | -27 |

a Device: L = 75μm W = 75μm
HV Drift Region = 10μm

| HV Operation Limits[b] |
|---|
| $V_{DS} \leq 100V$ |
| $V_{GD} \leq 100V$ |
| $V_{GS} \leq 12V$ |

b Wafer substrate must be held at highest positive potential, not to exceed 100V.

TABLE 2

On Resistance: Measured With $V_{GS} = 10_V$, $V_{DS} = 1V$

| HV-NCH $R_{on}(\Omega)$ | HV-PCH $R_{on}(\Omega)$ | Length(μm) Inversion | Drift | Width(μm) |
|---|---|---|---|---|
| 140 | 380 | 10 | 10 | 500 |
| 710 | 2000 | 10 | 10 | 100 |
| 1560 | 3600 | 10 | 10 | 50 |
| 1870 | 5700 | 15 | 10 | 50 |
| 2500 | 7460 | 20 | 10 | 50 |
| 4700 | 16400 | 50 | 10 | 50 |

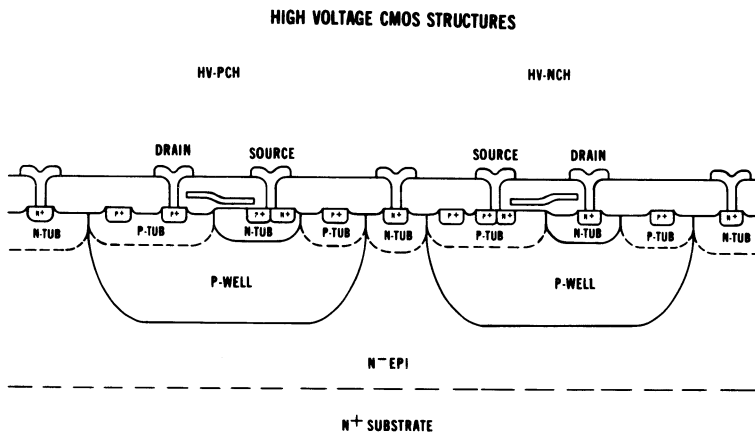
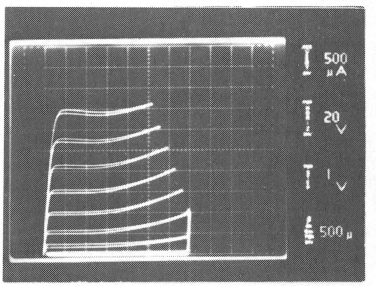
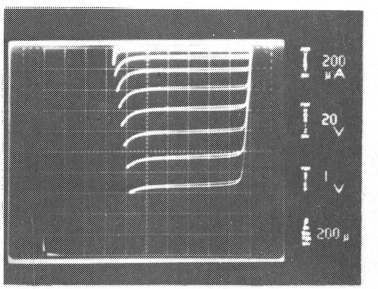



**FIGURE 1**




HV N-CHANNEL




HV P-CHANNEL

**FIGURE 2**

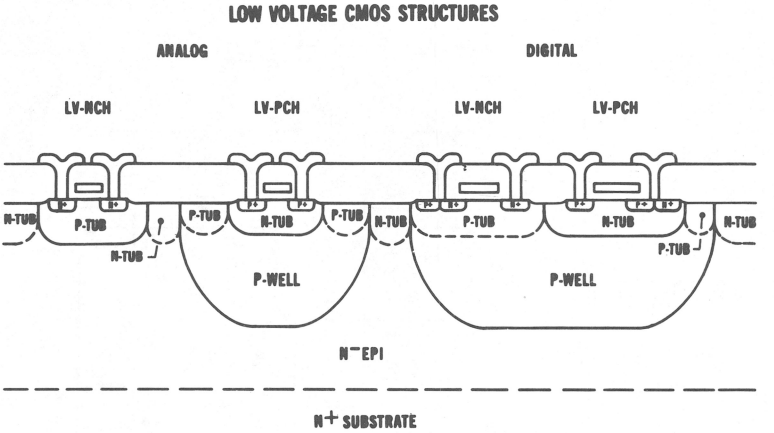



**FIGURE 3**

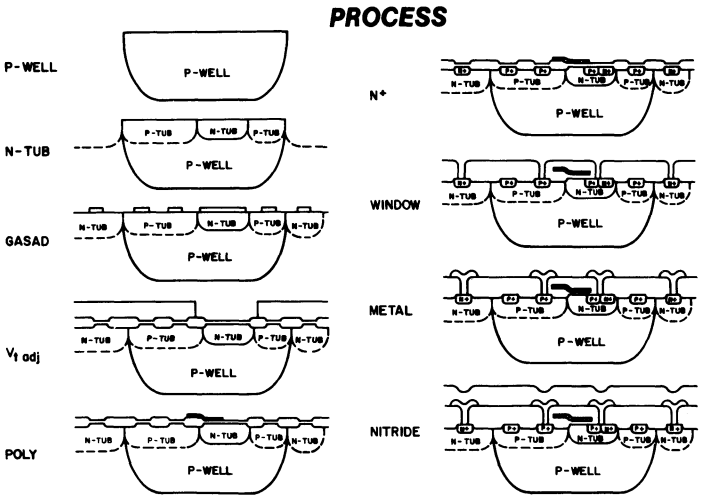



**FIGURE 4**

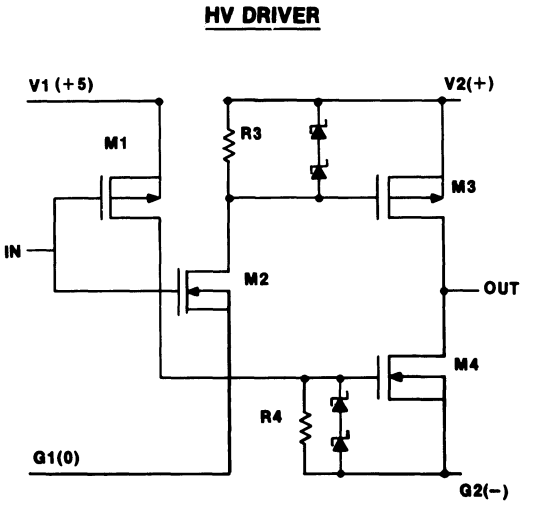



**FIGURE 5**

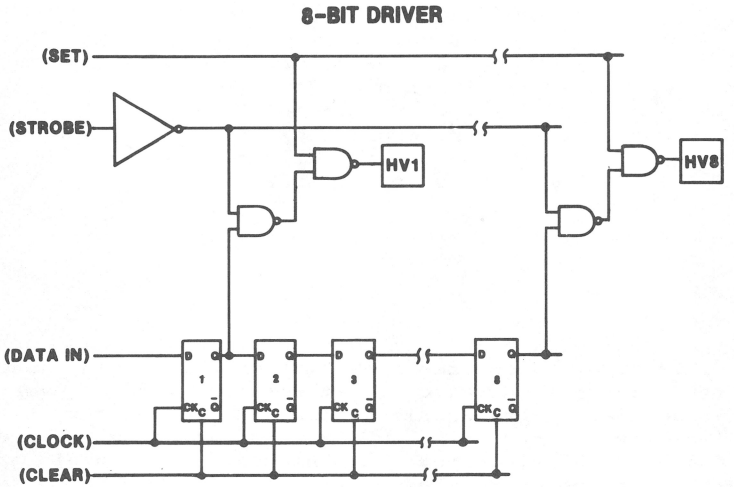



**FIGURE 6**

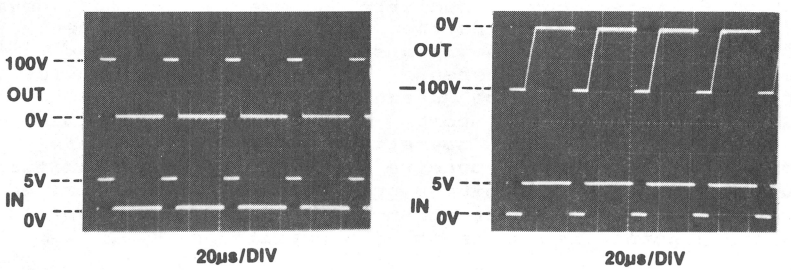



**FIGURE 7**

Proceedings of The Electrochemical Society, PV 1987-13, 68-76 (1987)
DOI: 10.1149/198713.0068PV © The Electrochemical Society

# NEW TECHNOLOGY FOR JUNCTION ISOLATED POWER ICs

Judy L. Sutor
Bernie Boland
Lewis E. Terry
Stephen P. Robb

Motorola Inc.
5005 E. McDowell Rd.
Phoenix, AZ 85008

## ABSTRACT

This paper describes a new method for forming junction isolated integrated circuit structures with a vertical output device. The technique uses etch and epitaxy to form the isolation structure. This paper compares the present technique with the new technique. Epitaxial growth conditions to optimize the pattern integrity are considered. The effect of the grind and polish step on the design rules is also considered. Finally, device data is presented using this technology to optimize the structure for both a high voltage and low voltage application.

## INTRODUCTION

There are many issues to consider when designing a power IC technology. Isolation scheme and output device structure will determine the maximum voltage, current, and operational bias constraints. For this reason, the technology of choice depends on the particular application for which it will be used. In terms of isolation, dielectric isolation imposes the fewest constraints for maximum voltage and operational bias constraints (1), however it is very expensive to produce. The traditional junction isolated structures are cheaper, but are limited in breakdown voltage, although methods have been reported to extend junction isolation to higher voltages (2).

The output device structure becomes an issue primarily when controlling high power. For such applications, the vertical output device offers substantial improvement over lateral devices. Since vertical structures use the back of the wafer as a contact, they are quite area efficient and the current flow is more uniform. This has draw backs as well. With the back of the wafer as the drain/collector

contact, vertical devices can only be used for applications with a single output or common drain type circuits. Yet for single output power applications, a higher voltage, junction isolated vertical output device structure would be quite useful.

## THE PRESENT TECHNOLOGY

Figure 1 shows the conventional process for achieving junction isolation with a vertical output device. The process begins with an n+ substrate with p epi grown on it. An n+ plug is diffused through the p epi in the power device section. Next, n epi is grown on top of this layer. A p+ isolation diffusion extends through the n epi down to the p epi layer, forming n type epi islands which are isolated from the vertical power device by reverse biased p-n junctions.

One limitation of this technology is that the voltage capability is limited by the maximum n epi thickness. The epi thickness is constrained by the ability to diffuse a p isolation through it. Also the resistivity of the n epi layer will affect parameters in the control circuitry as well as controlling the breakdown voltage of the power device. Therefore, either the control circuitry or the power device will be compromised.

The technology is limited even further by the fact that the p epi layer must be thin enough and high enough in resistivity that the n+ plug can diffuse through it. Yet with the high voltage contact on the back of the wafer, this is the layer which must support the voltage. Therefore if this layer becomes too thin the breakdown of the power device decreases.

## THE ETCH REFILL TECHNOLOGY

A better junction isolated process would offer separate epi thicknesses and resistivities in the control and power device regions with no constraint on the thickness of the layers.

The novel structure shown in figure 2a eliminates the limitations of the conventional process. The n epi in the control area is a separate layer from the n epi in the power device area. Thus the epi parameters can be chosen independently to optimize the performance of both sides.

The process for this structure involves the same number of masking steps and fewer epi runs than the conventional process. First a caustic etch is used to define a pedestal

where the power device will go. In a single epi run, n- epi is grown (resistivity chosen for the desired TMOS breakdown voltage, the thickness is determined by the desired BV plus grind back tolerance), the dopant is switched in the epi reactor and a p epi layer is grown, then the dopant is switched back to n for a final n epi layer.

The p layer serves as an isolation layer which wraps around the control area. The final n layer thickness and resistivity are chosen by control circuitry parameters. The last step is a grind and polish which leaves the desired structure as shown in figure 2b.

## ETCH REFILL PROCESS DEVELOPMENT

While the structure is straightforward, the processing is not simple. There are a number of conditions which can cause pattern distortion or crystal defects in the epitaxial layers. The pedestal is formed by a fairly deep etch so the pattern can distort during the caustic etch step. Corner compensation techniques similar to those used in DIC technologies can be used to maintain the pattern during this etch.

The epi growth conditions chosen can cause different types of pattern distortions. A high temperature, slow growth rate could be chosen to give the highest integrity of the epi layers and to cause the least pattern distortion on the top flat surface of the wafers. Figure 3 shows the top view of a grid pattern with high and lower temperature epi growth condition for the same epi growth rate. Clearly the pattern is maintained for the higher temperature epi.

Although these epi conditions give the highest pattern integrity on the surface of the wafer, a cross section reveals that the epi is not growing in the corners at the bottom of the pedestal. This could cause unpredictable breakdown problems since this is the blocking junction for the high voltage signal. This effect can also be a problem on the surface of the wafer if it is severe enough. Figure 5 shows an illustration of how pits can result in the corners of the isolated regions even after the grind and polish step when the epi is not growing uniformly.

On the other extreme, a lower temperature growth will fill in the corners at the bottom of the pedestal. But now the corners tend to fill faster than the sidewalls and the pattern rounds on the surface as shown in figure 5. This can make the devices difficult to align, and can force the design rules to leave unused space to account for the

isolation layer rounding. At these growth conditions the epitaxial layer is more susceptible to crystal defects as well. Therefore, the epi growth conditions must be chosen in a range where both of these extremes can be minimized.

The grind and polish is also a critical step since it defines the final epi layer thicknesses in this process. To maintain the proper final thicknesses, it is necessary to know the original thickness of the wafer, and the exact thicknesses of the grown epi layers. From this information the target polish stop is determined. Polishing techniques have been mastered to the point that the tolerance is as low as ±5 μM from the target and across the wafer.

## TECHNOLOGY ADVANTAGES

The advantages of this technology are numerous. Since the p epi wraps around the control area, the isolation step can be dropped. The isolation epi can be designed to sustain higher voltages. This can help avoid latch problems as well as giving higher breakdown voltages.

The leakage of the isolation junction must be low for power ICs to truly isolate the power device from the low voltage section. The high and low voltage sections operate at such different current densities that the leakage in the power device is on the order of the operating current in the control area. If the isolation junction leaks, it can seriously impact the operation of the control circuit. Figure 6 shows the current across the isolation junction when the back of the wafer is swept to 100V.

The etch refill technology is very flexible. It can be used for any application which could be optimized by using separate thickness and resistivity in the control and power areas. The technology has been demonstrated for both high and low voltage applications. If the application will tolerate lower breakdown voltage for the power device, that epi layer can be made thinner and lower resistivity in the vertical area to improve the on resistance with no change in the isolated control area. A low voltage part has been fabricated which had identical control circuitry as that fabricated on the n+ plug material with up to 40% reduction in on resistance and an acceptable breakdown for the application.

The etch-refill technology was developed primarily for high voltage applications. Although it is junction isolated, it does not have the thickness constraints that the conventional technology has. This technique has been used to make 350V low side switch circuits with Motorola's SMART-

power II biCMOS/TMOS process (3). The conventional technology yielded 100V BVdss while the etch refill TMOS BVdss was 350V. This higher breakdown is achieved with no compromise to the control circuitry.

## CONCLUSIONS

The technology described offers an easily integrated vertical power device with junction isolated control circuitry. The material can be made with minimum pattern distortion and epitaxial layer defects if the epi growth conditions are chosen properly. This technology has been demonstrated to be useful for both high and low voltage applications. It has been used to build a 350V low side switch circuit which achieves only 100V in the standard process. This technology could be used to benefit any process where separate epi layers could optimize the power and control sections of the circuit.

## REFERENCES


(1) V. Rumennik, "Power Devices are in the Chips," IEEE Spectrum, pp. 42-48:July 1985.

(2) F. Bertotti, C. Cini, "High Voltage IC Technologies and Products," Powertechnics Magazine, pp. 19-22:Jan. 1986.

(3) J.Sutor, B.Boland, S.Robb, L.Terry, "A Novel Isolation Structure for SMARTpower ICs," IEDM Tech. Dig., pp. 214-217:Dec. 1986.

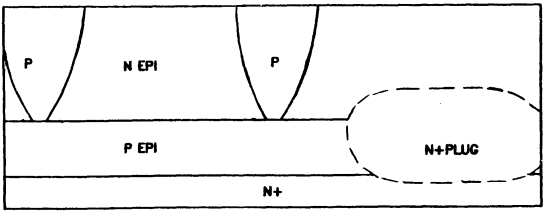
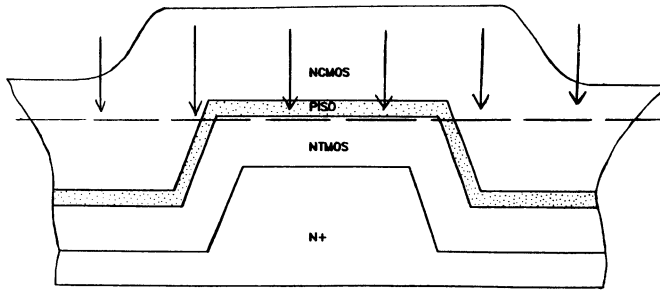




Figure 1. The conventional process




1. FORM PEDESTAL FOR POWER DEVICE
2. GROW NTMOS, PISO, NCMOS IN SINGLE REACTOR RUN
3. GRIND AND POLISH TO NTMOS EPI SURFACE

Figure 2a. The etch refill process.

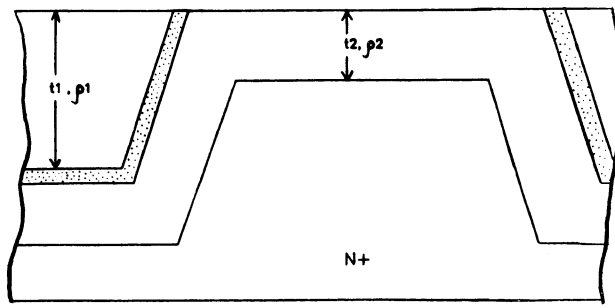
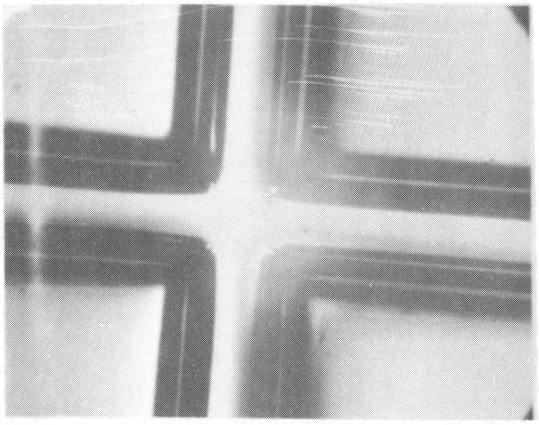
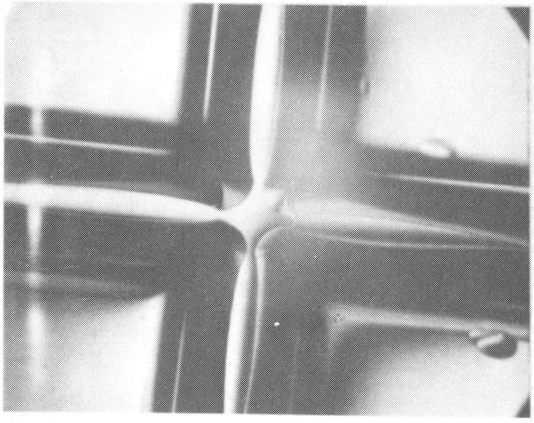



Figure 2b. The final structure.



High temperature
growth



Lower temperature
growth

Figure 3. High temperature and lower temperature epitaxy for the same growth rate.

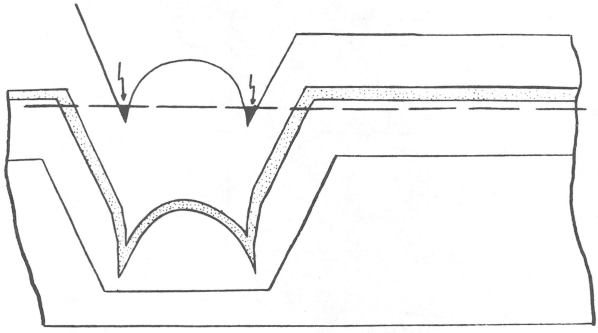


Figure 4. Illustration of cross-sectional view of epi growth on pedestal for high temperature condition.

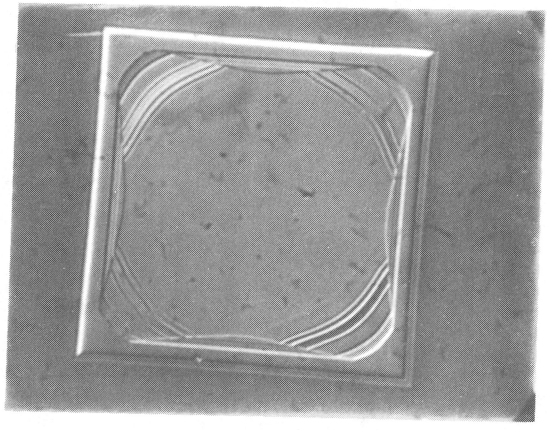


Figure 5. Epitaxy rounds the corners for low temperature conditions.

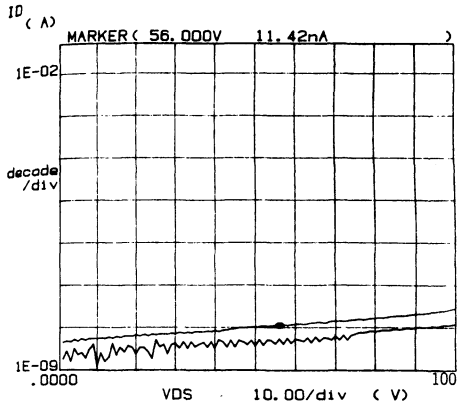



Figure 6. Leakage current across the isolation junction.

# DIELECTRIC ISOLATED PIC TECHNOLOGY

## SESSION CHAIRMAN:

M. AYMAN SHIBIB
AT&T BELL LABORATORIES

Proceedings of The Electrochemical Society, PV 1987-13, 79-89 (1987)
DOI: 10.1149/198713.0079PV © The Electrochemical Society

# A DIELECTRICALLY ISOLATED BIPOLAR-CMOS-DMOS (BCDMOS) TECHNOLOGY FOR HIGH VOLTAGE APPLICATIONS

C. A. Goodwin, M. A. Shibib, R. A. Furnanage,
C. Y. Lu, P. C. Riffe, N. S. Tsai and J. L. Schmoyer*

AT&T Bell Laboratories/*Technology Systems
2525 North 12th Street
Reading, PA 19612-3566

*ABSTRACT*

We have developed a versatile new technology that provides the capability to integrate low voltage devices on the same chip with high voltage components (>400V, bipolar and DMOS). The new technology combines bipolar, DMOS and CMOS processing steps that are compatible with dielectric isolation to provide a wide variety of bipolar and MOS devices on the same chip. Use of dielectric isolation insures >1000V dc isolation between adjacent components. We will discuss salient features of the wafer process, the types of devices available in BCDMOS and examples of high voltage ICs in manufacture.

## *INTRODUCTION*

The driving forces to combine maximum functionality with minimum cost for high voltage/power applications have led to the development of a number of new, promising technologies. The diverse applications for these technologies include display drivers, motor controllers, telecommunications switches, relays and interface chips (1-5).

This paper describes the approach taken at AT&T to address these circuit needs by providing a mixed low and high voltage capability on the same Si integrated circuit. We have chosen to exploit a well proven-in, cost effective Dielectric Isolation (DI) technique that was used originally for gated-diode-crosspoint (GDX) ICs (4, 5). The DI method constructs "wafers" that contain many tubs of single crystal Si (6), isolated to >1000V from each other via $SiO_2$ and in which a wide variety of different types of devices can be built.

To form the device structures we have developed a technology termed BCDMOS that can integrate a number of robust, high voltage devices such as SCRs and DMOSs that are capable of handling high voltage, fast dV/dt and current surges present in driver applications and communication systems and equipment. At the same time, we have strived to minimize costs to the systems designer by providing low voltage components such as JFETs and CMOS transistors on the same chip. The use of dielectric isolation allows great flexibility of IC design and layout. We can integrate any number of different circuit building blocks, each of which may

range in complexity from a single diode to a multi-hundred-cell DMOS transistor to a large CMOS logic array. If adjacent devices do not need to be high-voltage isolated (such as a CMOS array), they are placed in one larger DI tub to minimize chip size. In essence, DI gives the designer the ability to "glue" together an assemblage of miniature "Integrated Circuits" (bipolar or CMOS) on the same chip while still maintaining electrical isolation and freedom from parasitic interactions.

The remainder of this paper describes the BCDMOS technology in some detail. The structure and characteristics of the primary component devices are discussed and some examples of HVICs now in production will be given.

*FEATURES OF BCDMOS PROCESS*

During the development of BCDMOS, compatibility with dielectric isolation for ease of transfer to manufacturing has been stressed in the design of the process and components. The technology is modularized so that if process steps used to fabricate certain devices are not needed, they may be removed from the process, without impact on other components.

The wafer fabrication process begins with an adaptation of the Dielectric Isolation method discussed in Reference 6. After V-grooves, n+-wraparound layers and isolation oxide have been formed on high quality CZ-grown starting wafers, a thick layer of polycrystalline Si is deposited. The single crystal portion of the wafer is then thinned by backgrinding and polishing until individual tubs are formed. By using the DI technique each device or each sub-circuit group can be fabricated in its own "tub" of single crystalline silicon (6, 7). Since all devices or groups of devices are isolated from each other to > 1000V by a thick layer of oxide, diverse device types may be fabricated and interconnected thus allowing great flexibility for the designer.

After the dielectrically isolated wafers with the DI tubs have been fabricated for a specific circuit, the BCDMOS process is used to fabricate bipolar, CMOS and DMOS devices on the same chip. The core process utilizes single level poly, single-level metal, self-aligned poly gates, ion implantation and dry etching of windows to form an optimized poly gate N-channel vertical DMOS transistor; other process steps have been added to provide additional device structures such as JFETs but care was taken to avoid deleterious effects on the basic DMOS devices.

The key steps and mask levels of the BCDMOS process sequence are described in Table I. Cross sections of the DMOS and CMOS transistors at various stages of the process are depicted in Figures 1A, B and C. The JFET and the bipolar devices formed at the same time as the MOS devices are shown in Figures 2 and 3. Also, the BCDMOS process provides an SCR, high and low voltage diodes, resistors and capacitors (see Table II).

A simple, but important, circuit element that is heavily utilized by our designers is a high sheet resistance poly-Si resistor. This element allows improved layout flexibility and packing density because it can be placed between DI tubs thereby using otherwise wasted space.

The final portion of the process sequence, from phosphorus-doped oxide deposition through plasma nitride window etching is similar to that of our 3μm CMOS technology (8). The structure of the DMOS device after metal patterning is shown in Figure 4.

The BCDMOS technology was proven in for manufacture using fairly conservative 8μm design rules. This approach was taken to insure adequate photolithographic definition tolerances in view of difficulties expected from non-flat DI wafers and the significant surface topography associated with the DI tub walls as well as the high-voltage structures themselves. Experience over many hundreds of production lots has shown that such problems are quite surmountable. Because of this and the fact that in the BCDMOS technology we employ "VLSI-like" methods for pattern definition, we are working on quickly evolving toward finer design rules.

In addition to the production-ready components discussed previously, we have also fabricated and are evaluating lateral "resurf"-based high voltage MOSFETs (9) and Insulated Gate Bipolar-Transistors (IGBT) (10-12). Results on these promising devices will be reported separately.

## *DEVICE CHARACTERISTICS AND PROCESS PARAMETER OPTIMIZATION*

### (1) Bipolar Junction Transistors

The BCDMOS technology provides a variety of NPN and lateral PNP transistors. The emitters of all NPN transistors are formed by the heavily doped Source-N diffusion which is primarily designed for the source/drain of the NMOS and the source of the DMOS devices. Maximum emitter efficiency is achieved since the Source-N level is the shallowest heavily doped n+ layer in the BCDMOS technology. The arsenic doped wrap-around layer is used as the buried layer collector and the n-substrate is used as the collector drift region in order to sustain high voltage. Three different npn transistors are available each with a different base doping corresponding to the Tub-P, Deep-P or Body-P implantations. These variations produce BJTs with a variety of different current gains (6-400) and breakdown voltages (180-300V). A Body-P base vertical npn transistor is shown in Figure 2.

The emitters of all pnp transistors are formed by using the source/drain implantation of the PMOS devices (Shallow-P+) since this is the shallowest, most highly doped p+ diffused layer available. The collectors of the pnp can be formed by either a Tub-P or a Deep-P implantation to obtain different breakdown voltage ratings. Appropriately designed field plates on the surface of the lateral pnp

collector reduce the local high surface electrical fields and improve the breakdown voltage.

(2) Junction Diodes:

By choosing different combinations of n-type and p-type implantations for cathodes and anodes, a variety of pn junctions can be formed. Avalanche diodes having breakdown voltages in the 10 ~ 30V range are available for voltage reference and/or gate-oxide protection. High voltage blocking diodes and photodiodes are also available.

(3) Junction Field Effect Transistors:

The BCDMOS technology provides p-channel junction field effect transistors using two optional mask levels: Channel-P and Gate-N. The structure of a typical JFET in this technology is shown in Figure-3. The normally-on p-channel JFET transistor is important for many applications in telecommunication integrated circuits. The Channel-P and Gate-N ion-implantation parameters were selected so that after later heat treatments, a highly reproducible pinch-off voltage of about 2 volts is obtained. The drain breakdown voltage (65V) is determined by the avalanche breakdown of the gate-to-channel junction. Due to fairly low doping concentration in the p-channel and the smaller ionization rate of holes, the excess gate current (13) of the JFET is very small.

(4) PNPN - GTO/SCR

Four layer pnpn devices are also available in this technology by combining the structures of the vertical npn transistor and the lateral pnp transistor as shown in Figure-2. The devices function as switches to block high voltage when in the blocking state and to conduct high current with low voltage drop in the forward conduction state. The Gate Turn-Off (GTO) device is one of several thyristor devices that can be fabricated using this technology. The GTO can block more than 265 volts in both directions by the use of lightly p-type doped diffusions surrounding the anode p-type junction and the p-type base of the vertical npn, as indicated in Figure 2. The effect is to reduce the high electric field caused by junction curvature of the two p-type junctions. This combined light and heavy diffusion structure is essential to meet the breakdown voltage requirement while maintaining satisfactory turn-off characteristics for the GTO.

(5) CMOS Transistors:

The low voltage CMOS devices are usually used in the circuitry controlling high voltage devices in BCDMOS integrated circuits. The structures of the NMOS and PMOS devices are shown in Figure 1C. The NMOS is built in a p-tub and the PMOS is built in the n- substrate. The choice of doping concentration of the n-substrate is usually determined by the breakdown voltage requirement of the high voltage DMOS transistor. The gate oxide thickness of the CMOS is also chosen to be the same as that of the DMOS (1000Å) for the sake of processing simplicity.

Therefore, the threshold voltage and transconductance of the PMOS devices cannot be independently chosen but are coupled to that of the DMOS devices. Due to the very lightly doped channel region, the scaling of the PMOS device is somewhat limited by punch-through. Guard rings (not shown) are used extensively to prevent field inversion and latchup within DI tubs containing CMOS circuitry.

(6) DMOS Transistors:

The structure of the vertical DMOS device is shown in Figure-4. The Body-P dose was adjusted to obtain a DMOS threshold voltage of ~2V. The use of carefully designed poly field plates as well as junction termination extension techniques (14, 15) allows us to achieve a breakdown voltage of 300V for 8 ohm-cm substrates. The doping profile of the Deep-P plug in the DMOS structure is also important for achieving maximum breakdown voltage.

For a DMOS device with 180 cells, the on-state resistance at a gate voltage of 7 volts is about 12 ohms. The major parts of this resistance are associated with the n- substrate and the wraparound layer.

(7) DGDMOS Switch

A Dual Gate DMOS (DGDMOS) device is formed by merging two DMOS transistors which share a common drain as shown in Figure-5 (14, 18, 19). Note that the DGDMOS is built in one oxide-isolated silicon tub. These devices were designed to meet the requirements of three operating modes: (a) to block 265 volts in both directions in the off state when the gate is connected to the source; (b) to provide linearly increasing current with voltage up to 100 mA in the low conductivity, but "on" state; and (c) to handle up to 10A, 1 millisecond surges in the thyristor mode. This is accomplished by switching from the low conductivity state (linear) to the high conductivity state (thyristor). More details on the operation of the DGDMOS devices are given in the accompanying paper (14) and in Reference 19.

(8) High-value Polysilicon Resistors and Diffused Resistors:

The high-value polysilicon resistors provided in the BCDMOS technology have a sheet resistance of 20 Kohms/square. The I-V characteristics of the polysilicon resistor are well modeled by a grain-boundary trapping model (16). However, the resistivity of polysilicon films is rather process sensitive, thus tight control in film structures (17) and cross contamination (16) need to be addressed in order to obtain reproducible resistors.

It should be noted that the temperature coefficient of resistance of a polysilicon resistor is negative and is a function of temperature and applied bias. The resistance value of the polysilicon resistor in the BCDMOS technology decreases by 26% for temperature increasing from 25°C to 75°C; however, its linearity is not deteriorated for applied fields up to 4 KV/cm.

Well-controlled ion-implanted resistors can be formed in DI tubs yielding various resistivities from 2 ohms/square to 4 Kohm/square.

(9) Capacitors:

The low voltage capacitor is fabricated by using an n+ diffusion-gate oxide-poly structure. High voltage capacitors (>500V) are formed with a sandwich-type structure using N+ diffusion and metal as the bottom and top plates and the heavily doped polysilicon film as the center plate. The dielectric between the n+-Si and the polysilicon film is a thick field oxide and that between polysilicon and metal is a composite film consisting of P-glass, nitride, and oxide.

## *HVICs FABRICATED IN THE BDCMOS TECHNOLOGY*

The BCDMOS process has provided us with the means to develop a variety of proprietary parts for internal switching applications and also several commercially available HVICs (2). The latter include a Telephone Interface Circuit, an Ink-Jet Driver chip, a Gate Array/Driver chip (Figure 6) and a Multipurpose Solid State Relay. Details of the operation of these circuits will be discussed elsewhere (2).

## *CONCLUSIONS*

We have developed a new, versatile, powerful technology termed BCDMOS that allows integration of high voltage and low voltage devices into a single dielectrically isolated chip. The flexibility provided by the DI approach and the wide variety of available devices insure that this technology is well-suited for a diverse range of circuit applications. The high degree of manufacturability provided by this rugged, conservatively-designed process results in high yields and high quality to the customer.

## *ACKNOWLEDGEMENTS*

The authors would like to thank the numerous past and present members of the HVIC development team who have contributed to the success of this technology. You know who you are -- thanks.

## *REFERENCES*

[1] H. W. Becke, 1985 IEEE IEDM Tech. Dig. 724 (1985).

[2] M. A. Banak, J. C. Gammel, M. L. Embree, D. M. Pietruszynski, A. Ortiz-Conde, R. A. Furnanage, R. E. Carey and B. A. Mangieri, "High Voltage Custom ICs Using BCDMOS Technology", submitted to Custom Integrated Circuits Conference, May, 1987.

[3] V. Rumennik, IEEE Spectrum Mag., 42, July (1985).

[4] J. S. Mayo, Scientific American, p. 59, October (1986).

[5] H. T. Weston, H. W. Becke, J. E. Bethold, J. C. Gammel, A. R. Hartman, J. E. Kohl, M. A. Shibib, R. K. Smith, Y. H. Wong, IEDM Technical Digest, p. 85, 1982.

[6] K. E. Bean and W. R. Runyan, J. Electrochem Soc., Vol. 124, 5C, 1977.

[7] P. W. Shackle, Integrated Circuits, March/April, 19 (1984).

[8] L. C. Parillo, R. S. Payne, R. E. Davis, G. W. Reutlinger and R. L. Field, IEEE Tech. Dig. IEDM, 1980, p.752.

[9] J. A. Appels and H. M. J. Vaes, 1979 IEEE IEDM Techn. Digest, 238 (1979).

[10] H. W. Becke and C. F. Weatley, U. S. Patent 4,363,073 (1982).

[11] J. P. Russel, A. M. Goodman, L. A. Goodman, and J. M. Neilson, IEEE Electron Device Letter, Vol. EDL-4, 63 (1983)

[12] B. J. Baliga, M. S. Adler, R. P. Love, P. V. Gray, and N. D. Zommer, IEEE Trans Electron Devices,Vol. ED-31, 821 (1984).

[13] D. L. Mo, Proc. IEEE (Lett), Vol. 58, 1166 (1970).

[14] C. N. Dunn, J. C. Gammel and M. A. Shibib, this Symposium (1987).

[15] A. S. Grove, O. Leistiko and W. W. Hooper, IEEE Trans. Electron Devices. Vol. 13, 157 (1967).

[16] N. C. Lu, L. Gerzberg, C. Y. Lu and J. D. Meindl, IEEE Trans. Electron Devices, Vol. ED-28, 818 (1981).

[17] N. C. Lu, C.Y. Lu, M. K. Lee, C. C. Shih, C. W. Wang, W. Reuter, and T. T. Sheng, J. Electrochem. Society, Vol. 131, 897 (1984).

[18] J. D. Plummer and B. W. Scharf, IEEE Transactions on Electron Devices, Vol. ED-27, 380 (1980).

[19] C. Y. Lu, N. S. Tsai, C. N. Dunn, P. C. Riffe, M. A. Shibib, R. A. Furnanage and C. A. Goodwin, submitted to IEEE Transactions on Elec. Devices.

TABLE I-BCDMOS PROCESS SEQUENCE

1. Initial Oxidation.
2. Deep-N level to form drain contact for vertical devices.
3. P-tub level for CMOS [Figure 1(a)].
4. Deep-P level for DMOS and pnp collector.
5. Thin oxide level to form active regions by etching field oxide.
6. LPCVD polysilicon deposition and patterning using dry etching. [Figure 1(b)]
7. Body-P level for DMOS and npn base.
8. Shallow-P+ level for PMOS and pnp emitter.
9. Source-N level for NMOS and DMOS source region [Figure 1(c)] and npn emitter.
10. JFET P-channel level. (optional)
11. JFET N-gate level. (optional)
12. LPCVD phosphorus-doped oxide deposition and flow
13. Window opening using RIE, Al-Cu metallization, and final plasma nitride passivation.

PRODUCTION-READY

TABLE II - COMPONENT DEVICES PROVIDED BY BCDMOS

| DEVICE | MAIN ATTRIBUTE** | OTHER CHARACTERISTICS |
|---|---|---|
| BIPOLAR | | |
| SCR | 300V (BVCAO) | HANDLES 15A PULSES, 1A DC |
| GTO | 300V (BVCSAO) | |
| PNP* | 280V (BVCBO) | hFE=35 (IB=10UA, VCE=1V) |
| NPN* | 180V or 300V (BVCBO) | hFE=120 or 400 (IB=10UA, VCE=1V) |
| DIODES | >300V (10UA) | |
| AVAL. DIODES | 8, 13, 26V | |
| PHOTODIODES | 150V | |
| UNIPOLAR | | |
| JFET | 60V (BVG-DS) | P-CHANNEL, VPINCH=1.6V |
| DMOS FET | 200-400V (BVDS) | ONE TO 400 CELLS, VT=2.4V |
| DUAL GATE DMOS | BIDIRECTIONAL, ±260V | BUILT-IN SCR; (10A PULSE, 1A DC) |
| HVPMOS | 300V (BVDS) | VT=-1.2V |
| CMOS NMOS | 20V (BVDS) | VT= 1.2V |
| CMOS PMOS | 30V (BVDS) | VT=-1.2V |
| PASSIVE ELEMENTS | | |
| DIFFUSED R'S | 2-4Kohm/sq | |
| POLY R'S | >10 Kohm/sq | ISOLATED, NEGATIVE Tc |
| CAPACITORS | 300V MAX | LOW C/UNIT AREA |
| | 20V MAX | HIGH C/UNIT AREA |

* LOW-VOLTAGE VERSIONS AVAILABLE

** BREAKDOWN VOLTAGE OF SOME HV DEVICES DEPENDS ON TUB RESISTIVITY.

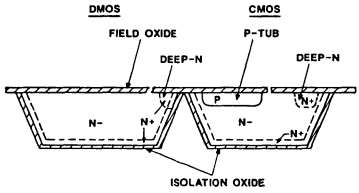



FIGURE 1A - CROSS SECTIONS AFTER P-TUB STEP

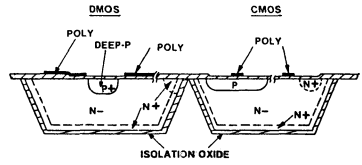



FIGURE 1B - CROSS SECTIONS AFTER POLY-SI PATTERNING

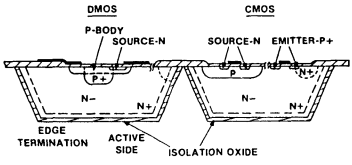



FIGURE 1C - CROSS SECTIONS AFTER SOURCE-N

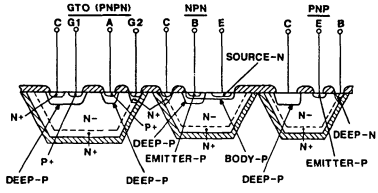



FIGURE 2 - CROSS SECTIONS OF BIPOLAR DEVICES AFTER SOURCE-N

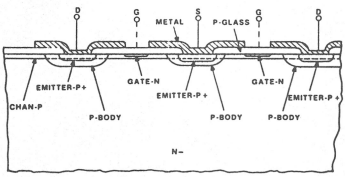



FIGURE 3 – CROSS SECTION OF JFET AFTER METAL PATTERNING

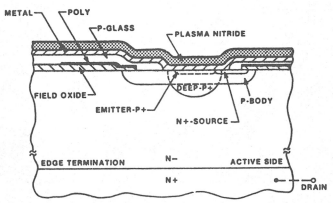



FIGURE 4 – FINAL STRUCTURE OF DMOS TRANSISTOR

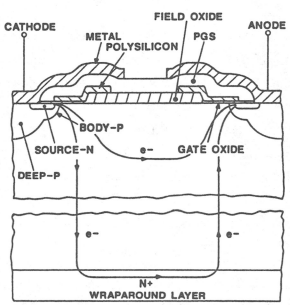



FIGURE 5 – A DGDMOS DEVICE IS FORMED BY MERGING TWO DMOS TRANSISTORS SHARING A COMMON DRAIN

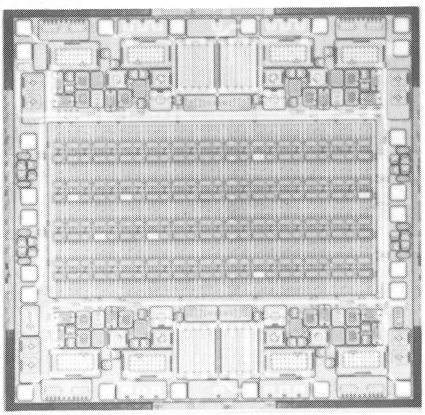


FIGURE 6 – CHIP PHOTO OF GATE ARRAY/DRIVER IC

Proceedings of The Electrochemical Society, PV 1987-13, 90-95 (1987)
DOI: 10.1149/198713.0090PV © The Electrochemical Society

# A 200V DI PROCESS WHICH PROVIDES IGT'S, SCR'S HIGH SPEED COMPLIMENTARY LOW VOLTAGE BIPOLARS, CMOS AND BIPOLAR LOGIC OPTIONS

J.D. BEASOM

HARRIS SEMICONDUCTOR
P.O. BOX 883
MELBOURNE, FL 32901

## ABSTRACT

A process which provides both high and low voltage complementary bipolar and complementary MOS devices is discribed. Dielectric isolation is used to isolate all device types. Process simplicity is achieved by multiple use of all diffusions including using the same PN junction as the high voltage junction for all high voltage devices. Basic electrical characteristics of all devices are presented. Dependence of lateral DMOS parameters on geometry factors is presented. Current density capabilities of various types of high voltage devices are compared. Compatible logic implementations are described.

## INTRODUCTION

Previously reported high voltage processes have not offered a full spectrum of device performance. Some have been MOS based processes (1,2) with low performance bipolars if any while others have been bipolar based with no MOS devices (3). Some of the previously reported processes (4) constrain the terminal voltage of the power device in the process thus limiting application. Few processes accommodate conductivity modulated devices which can handle approximately ten times the current density of unmodulated high voltage devices thus providing a significant area reduction for high voltage power devices.

The process reported in this paper overcomes the limitations of previous processes. It provides complimentary MOS and bipolar devices for full flexibility in low voltage design. High voltage bipolar and MOS devices of both polarities are available. SCR's and N channel IGT's are available as high voltage conductivity modulated devices. All devices are fully isolated with no restriction on terminal voltages.

## PROCESS DESCRIPTION

Component isolation is accomplished by use of dielectric isolation which provides a number of benefits. Greater than 500 volts can be applied between any two islands. Separation between isolated devices can be less than 25 microns which is significantly

smaller than the space required by alternative methods (5). DI, unlike JI, completely blocks minority carrier flow to the substrate thus allowing unrestricted use of conductivity modulated devices such as IGT's and SCR's.

The isolated islands are N type 5 ohm cm 20 microns thick. Selective N+ buried layers are used.

The various devices which the process provides are formed in the isolated islands by a sequence of five diffusions followed by thin oxide patterning and oxidation, poly silicon deposition and patterning, P drift region formation, reflowed oxide deposition, contacts, inter connect and passivation. The diffusions are: P-, N base, P base, P+ and N+.

## LOW VOLTAGE DEVICE STRUCTURES

The low voltage NPN is formed in a buried layer island from the P base and N+ diffusions. The P+ diffusion is used for base contact. Base depth is about 2 microns.

The low voltage vertical PNP is formed in an isolated P- region which is its collector. The N base and P+ diffusions form base and emitter. N+ is used for base contact. Base depth is about 2 microns.

Low voltage PMOS devices are built in an N island while low voltage NMOS devices are built in a P- well region. Both device types may be formed in a single dielectricly isolated island with individual devices self isolated from one another in the usual way. Alternatively P channel and N channel devices may be formed in separate DI islands which provides total elimination of latchup.

NMOS drains and sources may be made from either N+ or N base which provides higher breakdown due to double diffused drain profile. Likewise, the PMOS drains and souces may be made from either P+ or P base. Because all of these diffusions are made before gate poly is formed, the devices are not self aligned.

## HIGH VOLTAGE DEVICE STRUCTURES

High voltage NPN's are made using P- as base and N+ as emitter. This structure exploits the high voltage capability of the deep graded P- to N island junction to achieve maximum base collector breakdown voltage. The same junction is used as the high voltage junction in all other high voltage device types.

High voltage PNP's are lateral devices. They are made from P- as collector and P+ as emitter. The emitter is formed in an N base punch through shield to achieve minimum base width for a given breakdown voltage (6).

High voltage SCR's are made with the usual merged vertical NPN, lateral PNP configuration using the NPN and PNP structures described above. When reverse blocking is required, the emitter punch through

shield is eliminated, P- is added to the anode to boost junction breakdown and anode to cathode gate spacing is increased to avoid punchthrough.

High voltage PMOS devices are lateral structures with P- drains and P+ sources. The drain is offset from the gate to avoid gate bias induced drain-body breakdown reduction. The drain is extended to the gate edge by a P- drift region implant made after gate delineation and masked by field oxide and gate poly.

High voltage NMOS devices may be either vertical or lateral DMOS structures. In either case the N- island is drain and the P- diffusion is body with N+ used as source and drain contact. These structures can be converted to conductivity modulated IGT's by replacing the ohmic N+ drain contact by a minority carrier injecting P+ diffusion.

## DEVICE CHARACTERISTICS

Key bipolar device parameters are presented in Table 1. The excellent $f_T$ of the low voltage bipolars is a result of their shallow vertical structure together with the low parasitic capacitance of dielectric isolation. The HV lateral PNP has a base width which yields a 200V breakdown; wider base widths yield breakdowns of 250V. The $f_T$ of the HV PNP is about three times that of a conventional 50V lateral PNP which illustrates the performance improvement which can be achieved with the improved structure used to build it.

Basic MOS characteristics are presented in Table 2.

The HV NMOS $V_T$ may be adjusted by mask design, unlike a conventional DMOS, because source to body space is set by mask design rather than by self aligned lateral diffusion difference. The variation of threshold and breakdown with mask design for a lateral N channel DMOS are presented in Table 3. Breakdowns are not recorded for the 2 and 4 micron devices because other geometry variations affected the breakdowns of the devices from which that data was taken.

Table 4 presents data illustrating the effect of thin oxide overlap of P- on breakdown voltage of the lateral N channel DMOS.

The high current densities which can be achieved by conductivity modulating high voltage devices are illustrated by the data in Table 5. All devices have at least 200V breakdowns and all are characterized at 2.5V across the device. Because current must flow laterally through the high voltage blocking region, the device currents have been normalized to the width of the high voltage region through which they flow to provide a meaningful basis for comparison among the different device types.

The MOS devices are operating at Vgs of 20V. At this bias, the channel resistance is small compared to drift region resistance.

The lateral IGT is also biased with Vgs of 20V. At this bias and 2.5V across the device, it is approximately at its holding

current. The relatively low latching current density is due, in part, to a non-optimum geometry device with a long source which increases the value of the pinched P- resistor beneath the source through which collected anode hole current flows.

The PNP, which has HFE of 10, is operated at a forced beta of 5 to provide about the same base overdrive as the high beta NPN has at its forced beta of 10.

The bilateral blocking SCR has twice the lateral PNP base-width of the forward blocking SCR. That difference is the major cause for the difference in current densities between the two devices.

## LOGIC

A variety of logic implementations are possible in the process. The low voltage CMOS devices may be placed in a single island and used to implement any CMOS logic form. Alternatively PMOS devices may be placed in one island and NMOS devices in another to provide absolute immunity to latchup. The low voltage bipolar devices may be used to implement any of a wide range of different logic circuits. Very high speed may be obtained by use of one of the nonsaturating current steering schemes as a result of the high $f_T$ of the bipolar devices.

## REFERENCES


1. E.J. Wildi, T.P. Chow, M.S. Adler, M.E. Cornell and G.C. Pifer, "New High Voltage IC Technology, 1984 IEDM Technical Digest, pp. 262-265.
2. R.A. Blanchard and R.K. Williams, "D/CMOS Technology: Smartpower Processes That Solve Different Circuit Design Problem", Electro/86, 13/1.
3. Y. Sugawara, K. Miyata and M. Okamura, "350V Analog-Digital Compatable Power IC Technologies", 1985 IEDM Technical Digest, pp. 728-731.
4. R.K. Frank and D.L. Zaremba, "Junction Isolated Power IC's", Electro/86, 13/5.
5. H.W. Becke, "Approaches To Isolation In High Voltage Integrated Circuits", 1985 IEDM Technical Digest, pp. 724-727.
6. J.D. Beasom, "A High Performance High Voltage Lateral PNP Structure", 1983 IEDM Technical Digest, pp. 424-427.

TABLE 1

Bipolar Device Characteristics

| Device Parameter | LVNPN | LVPNP | HVNPN | HVPNP |
|---|---|---|---|---|
| HFE | 250 | 150 | 100 | 10 |
| BVCES (V) | 80 | 45 | 220 | 200 |
| $f_T$(MHZ) | 600 | 300 | 75 | 15 |

TABLE 2

MOS Device Characteristics

| Device Parameter | LVNMOS | LVPMOS | HVNMOS | HVPMOS |
|---|---|---|---|---|
| $V_T$ (V) | 1.5 | 1.5 | 0.8 | 1.5 |
| BVdss (V) | 35 | 35 | 250 | 250 |

TABLE 3

Dependence of Lateral NMOS Threshold and Breakdown Voltage on Drawn Source to Body Space

| Source to Body Space (microns) | $V_T$ (V) | BVdss (V) |
|---|---|---|
| 0 | 0.47 | 63 |
| 1 | 0.57 | 116 |
| 2 | 0.74 | - |
| 4 | 1.0 | - |
| 6 | 1.1 | 136 |
| 8 | 1.3 | 136 |

TABLE 4

Dependence of Lateral
NMOS Breakdown on Drawn Thin Oxide Overlap of P-

| Thin Oxide to P- Space (microns) | BVdss (V) |
|---|---|
| 2 | 246 |
| 6 | 205 |
| 10 | 158 |

TABLE 5

Current Density Capability
of Various 200V Components at $V_F$=2.5V

| Component | Current Density A/cm | IC/IB or Vgs in V |
|---|---|---|
| PMOS | 0.05 | 20 |
| Lateral NMOS | 0.26 | 20 |
| PNP | 0.082 | 5 |
| NPN | 0.44 | 10 |
| Lateral IGT | 0.47 | 20 |
| Forward and Reverse SCR | 21 | |
| Foreward Blocking SCR | 43 | |

Proceedings of The Electrochemical Society, PV 1987-13, 96-105 (1987)
DOI: 10.1149/198713.0096PV © The Electrochemical Society

# DIELECTRICALLY ISOLATED HIGH VOLTAGE INTELLIGENT POWER IC'S COMPOSED OF CMOS LOGICS AND LATERAL POWER THYRISTORS

Yoshitaka Sugawara+ and Tatsuo Shimura

Hitachi Research Laboratory+ and Hitachi Works of Hitachi Ltd.
Hitachi, Ibaraki, Japan

## Abstract

A combination technology of dielectric isolation, CMOS logics and power thyristors is investigated to develop intelligent power IC's. A large current power IC for solenoid drives ( 50 V, 1.5 A/channel, 12 channels ), a high voltage power IC for flat panel displays ( 250 V, ±40 mA/channel, 34 channels ), and a floating-operated linear switch array for telecommunication uses (450 V, 100mA/switch, 4 switches ) are developed with the combination technology. Its superior characteristics such as compactness, low power dissipation and high noise immunity are confirmed by the performance of the fabricated power IC's.

## § 1. Introduction

To ensure electronic equipment which are more efficient, compacter and more reliable, monolithic high voltage intelligent power IC's are desirable and a number of them have been developed recently (1-3). In these power IC's, many logic circuits must be integrated for realization of high intelligence, and high voltage/large current output devices must be integrated for realization of large output power. This results in a large IC chip area and then, high cost.

By increasing the logic density, the chip area can be reduced and both low power dissipation and high speed can be achieved, but noise immunity decreases. On the other hand, larger output power devices generate a larger surge voltage and a larger surge current. Therefore, the noise immunity of the power IC becomes very low.

In order to solve these problems and realize an intelligent power IC, a combination technology of dielectric isolation, CMOS logics and lateral power thyristors has been investigated. Its advantages were verified through development of compact intelligent power IC's.

## § 2. Combination Technology for Compact Intelligent Power IC's

Although several kinds of integration methods, such as self-isolation (4), pn junction isolation (5) and dielectric isolation (6), have been developed for power IC's, dielectric isolation is superior to the others for several reasons. The first reason is complete isolation. Since the devices in the power IC's are surrounded by a dielectric film, electric interference between the output power devices and the logic circuits is completely eliminated. The second reason is compact chip size. In the case of $p^+$ n junction isolation, the width of the isolation area must be larger than the total width of the $p^+$ diffusion layer for isolation and the depletion layer around the $p^+$ n junction. Therefore, the width of the isolation area becomes larger with increasing applied voltage. The isolation area of dielectric isolation, however, is independent of the depletion layer width and is only dependent on the matching accuracy of the dielectrically isolated substrate. In the case of an EPIC (Epitaxial Passivated IC) method (6), the width of the isolation area is easily reduced to less than 5 $\mu$m (7), which is narrower than that of the pn junction isolation when the applied voltage is high. Figure 1 compares typical transistor cell sizes. The cell of the EPIC becomes smaller than that of the pn junction isolation at an applied voltage of more than 30 V. The third reason is a negligible dependence of isolation leakage current on temperature. Output power devices generate a lot of heat, which locally increases the IC's temperature. Leakage current of the pn junction doubles approximately every 11 ℃ and reaches a few microamperes at 300 ℃ (8). Leakage of this order hinders accurate operation of the linear circuits, and generates increasing static power dissipation and latch up actions of the CMOS logics. Therefore, we have chosen the EPIC method as a better integration approach to power IC's.

CMOS logic has also been selected because of its low power dissipation, high speed and large noise margin. The thyristor family, i.e. thyristors, gate turn-off thyristors, Triac etc., has been chosen because of its high current capacity per unit area as compared with transistors, MOSFET's and IGBT's. While their operation speed is not very fast, it is satisfactory for most conventional power equipment. Since output power devices occupy a lot of the area in the power IC, the thyristor family is the most suitable for realization of compact power IC's.

According to the above reasons, the combination technology of dielectric isolation, CMOS logics and thyristors was selected and utilized for the development of compact intelligent power IC's.

## § 3. CMOS Logic / Thyristor Output Large Current Power IC for Solenoid Drive

A compact, large current IC ( 50 V, 1.5 A/channel ) has been investigated for the solenoid drive of step motors and wire dot printers. Figure 2 shows a block diagram of a 12 channel driver IC developed for the wire dot printer, which is composed of gate turn-off thyristors for 12-wire dots, a turn-off circuit of the thyristors, a thermal shut-down circuit, a 12-bit static shift registor and a 12-bit latch circuit. Since the shift registor is integrated in the driver IC, the IC can be controlled by serial signals and the number of signal lines needed can be reduced to a few. Therefore, the IC can be set in the printer head and the printer can be made more compactly. The thermal shut-down circuit operates at 115 ℃ and prevents the driver IC from thermal damage by limiting the current.

Figure 3 shows a photomicrograph of the driver IC. For easy wiring, the thyristors are laid out on the chip circumference and CMOS logics are laid out at its center. Although the output current per one thyristor is large ( 1.5 A ), its cell size is small ( 270 $\mu$m x 450 $\mu$m ) because of its large current capacity per unit area. Thus, a driver IC with large power dissipation of 11 W at 70 ℃ is realized in a small chip.

To prevent CMOS logics from latching up, p MOSFET's and n MOSFET's are integrated in the different islands from each other and CMOS logics are formed by connecting these MOSFET's with a metal layer as shown in Figure 4. Thus, high noise immunity is realized in spite of a large surge current. In the case of driver IC's fabricated with pn junction isolation, not only the logic circuits, but also undriven thyristors latch up and the driver ICs cannot be provided for practical use, because the potential of the p substrate is the most negative and a large output current flows through the p substrate, therefore, a potential distribution is generated in the p substrate.

The combination technology enables realization of a practical, large current power IC of more than a few amperes with high noise immunity and good temperature proof.

## § 4. CMOS Logic / Thyristor Output High Voltage Power IC for Flat Panel Display

Compact high voltage power IC's of the 250 V class have been investigated for flat panel displays such as plasma and electro-

luminescent displays. Figure 5 shows a block diagram of a developed 34 channel raw driver IC intended for electroluminescent displays. The IC includes 34 high voltage push-pull outputs of a breakdown voltage of more than 300 V, 34 control logics and a 34- bit shift registor. Each output stage consists of a push-up gate turn-off thyristor and a pull-down npn transistor. Since the thyristor is anode-fired, a level shift circuit which is used for driving the pull-up device in the conventional high voltage push-pull circuit (9) is not necessary. As compared with the push-pull circuits composed of MOSFET's or bipolar transistors, the IC chip size can be reduced since the thyristor has a high current capacity per unit area and the drive power dissipation can also be reduced, since the thyristor has a self-holding function for the on-state.

Figure 6 shows a photomicrograph of the raw driver IC for electro-luminescent displays. The chip is very compact in spite of integrating 34 channel push-pull outputs, which is the smallest one yet reported as shown in Figure 7 (9-15). The shift resistor and the control logic are composed of 3 $\mu$m poly Si gate CMOS FET's, for which the fabricating process is the same as that of a conventional LSI.

A maximum shift resistor clock frequency of more than 30 MHz is realized at a supply voltage of 5 V. Main features of the raw driver IC are : output voltage, 250 V; output current, $\pm$ 40 mA; clock frequency, 0.25 MHz; power dissipation, 0.4 mW. Since every raw line is operated at 50 Hz, high speed is not essential for the logic circuit.

The same technology has also been applied to the design of column driver IC's and a 32-bit column driver IC has been developed. The chip size is the smallest reported for 32-bit column driver IC's (9-15). The IC has a 32-bit latch circuit, in addition to the circuits of the raw driver IC, and it has a high clock frequency of 6 MHz in spite of a high output current of $\pm$ 10 mA.

The combination technology enables fabrication of multi channel driver IC's of more than 64 channels as a result of the low power dissipation, high density and high clock frequency which are achieved.

## §5. CMOS Logic / BIMOS Output High Voltage IC for Telecommunication Uses

Since devices in the dielectrically isolated power IC's are isolated by the dielectric film from each other, interference between devices that is generated by current noise or voltage noise through

the isolation and substrate does not occur. But, the IC's are not always free from interference between logics and output power devices which occurs from the inteconnections between them. In particular, switches for subscriber line interface circuits in telecommunications uses must be driven under a floating bias condition by a constant low supply voltage and they must be isolated electrically from the control logics. A capacitor coupling technology (16) is suitable for this because it can be realized on an IC chip.

Figure 8 shows a block diagram of a unit circuit for a linear switching IC which is developed for telecommunications uses. The IC includes a thyristor, a bilateral MOSFET, CMOS control logics, capacitors for isolation, a protection circuit against over currents, and diode bridges which generate a dc bias current for switching off the thyristor and a dc bias voltage for switching on the MOSFET. Only the MOSFET is operated in the small current region and the thyristor is operated in the large current region, therefore, both linear output characteristics at small current region and the low power dissipation at large current are realized simultaneously.

Since control logics are electrically isolated from the thyristor and the MOSFET by the capacitors, floating operation is possible. Namely, when the potential of the thyristor's cathode and MOSFET's drain is in the region from $-500$ V to $+500$ V, both the thyristor and MOSFET can be driven by a power supply of 5 V. It is difficult to realize floating operation by IC's isolated with a pn junction.

Figure 9 shows a photomicrograph of the linear switching IC integrating four unit circuits shown in Figure 8. The main specifications of the IC are the following: breakdown voltage, 450 V; output current, 100 mA; interruptable current, 2 A; crossover distortion, $\leqq$ 40 dB. Although the IC satisfies the requirements for practical use, it is driven by only pulse signals and cannot be driven by dc signals.

To realize operation by both pulse and dc signals, a COGMOS thyristor ( Complementary Gated MOS thyristor ) has been developed (17). Figures 10 and 11 show its equivalent circuit and structure, respectively. The COGMOS thyristor is composed of six elements, such as pnp and npn transistors, p and n channel MOSFET's and two diodes. The COGMOS thyristor and its drive circuit are isolated by the gate oxides of the p and n channel MOSFET's. When an input signal is given at the control terminal C, the supply voltage Vs is applied to the gate electrodes of the MOSFET's Q3 and Q4. Under a forward bias condition, the thyristor is triggered by the p channel

MOSFET Q3 when the potential Vk of its cathode electrode K is higher than that of the drive circuit Vs, and it is triggered by the n channel MOSFET Q4 when the potential VA of its anode electrode A is lower than that of the drive circuit. Thus, the COGMOS thyristor can be driven under the floating bias condition by the drive circuit with a constant low supply voltage Vs. A high bidirectional blocking voltage ( $\geqq \pm 350$ V ) is achieved by prevention of MOS gate electrification with the short diodes D1 and D2, and the combined technique of junction termination extension and a field plate.
Both low triggering MOS gate voltage ( $\sim 5$ V ) and high isolation voltage ( $>500$ V ) are achieved by the structure optimization of the self-aligned vertical n channel MOSFET and the lateral p channel MOSFET with the double offset gates. By using the COGMOS thyristor, the chip area of the linear IC shown in Figure 9 can be reduced further.

## § 6. Summary

To develop compact and practical intelligent power IC's integrating logics, control circuits and high voltage/large current output devices, a combination technology of dielectric isolation, CMOS logics and power thyristors was investigated.

It was difficult to realize a multi channel large current power IC (50 V, 1.5 A/channel, 12 channel), with the pn junction isolation method due to uncontrollable latch up actions of the logics and output power devices, but the IC was realized easily and compactly with the combination technology. Multi channel high voltage power IC's for flat panel displays (250 V, $\pm 40$ mA/channel, 34 channels) were also realized in a smaller chip area than that of IC's developed with other technologies. A compact linear switch array for telecommunications uses was developed, which integrates the control CMOS logic isolated electrically from the BiCMOS output power devices.

It also appeared possible to reduce the chip area by using the COGMOS thyristor. The switch array and the COGMOS thyristor could realize floating bias operation which was difficult for IC's fabricated with the pn junction isolation.

The superior characteristics of the combination technology such as compactness and high noise immunity, were confirmed through the fabricated powerIC's.

## ACKNOWLEDGMENTS

The authors wish to thank Drs. Y. Kawamoto, M. Okamura and T. Kariya, and Messers. K. Miyata, K. Nagata, T. Yatsuo and N. Monma for their continuous encouragement and guidance. Appreciation is also expressed to members of the IC Design and Fabrication Groups.

## REFERENCES

1) Y. Sugawara, K. Miyata and M. Okamura : IEDM Technical Digest, p.728, 1985.
2) B. G. Bynum and D. L. Cave : ISSCC Digest of Technical Papers, p.290, 1984.
3) I. Wacyk, M. Amato and V. Rumennick : ISSCC Digest of Technical Papers, p.16, 1986.
4) H. Wakaumi, T. Suzuki, M. Saito and H. Sakuma : IEDM Technical Digest, p.416, 1983.
5) I. Imaizumi, M. Kimura, M. Yoshimura and F.Inoue : IEEE Trans. Consumer Electron., vol. CE−26, p.368 Aug. 1980.
6) D. Mc Williams, C. Fa, G. Larchian and O. Maxwell : J. Electro−chem. Soc., vol. 111, p.153, 1964.
7) F. Ohira, T. Karaki and J. Watanabe : Extended Abstructs of Electrochem. Soc., Spring Meeting, vol.84−1, p.178, 1984.
8) J. D. Beasom : Technical Report of Harris Semiconductor, 16/2, 1980.
9) G. Remmerie, B. D. Ceulaer et. al. : IEEE Solid State Circuit, p.793, 1985.
10) R. A. Martin, S. A. Buhler and G. Lao : IEDM Technical Digest, p.266, 1984.
11) M. Saito, H. Wakaumi, T. Aizawa and H. Sakuma : National Convention Record, No.193, 1985, The Institute of Electronic and Communication Engineers of Japan.
12) T.Okabe, M. Kimura, I. Simizu, Y. Nagai and K. Hoya : ISSCC Digest of Technical Paper, p.100, 1986.
13) K. Fujii, Y. Torimaru, K. Nakagawa, T. Fujimoto and Y. Aoki : ISSCC Digest of Technical Paper, p.46, 1981.
14) S. A. Buhler, D.L. Heald, R.R. Ronen, T. Gannon and P. Elkins : IEDM Technical Digest, p.259, 1981.
15) T. Nakagawa, T. Ashida, H. Takeuchi and K. Fujii : IEDM Technical Digest, p.72, 1982.
16) W.H.A.Mattheus : ISSCC Digest of Tech. Paper, p.238, 1981.
17) Y.Sugawara : IEDM Technical Digest, p.111, 1986.

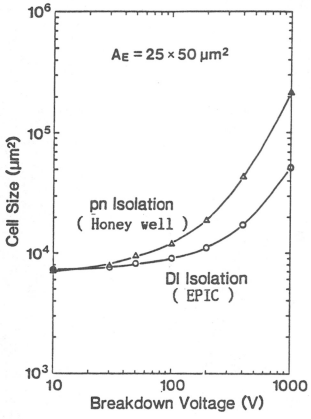



Fig.1. Comparison of typical transistor cell sizes.

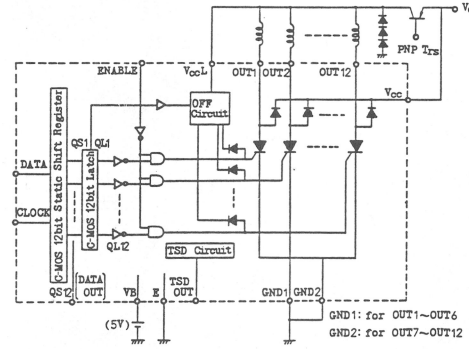



Fig.2. Block diagram of a 12 channel driver IC for solenoide drive.

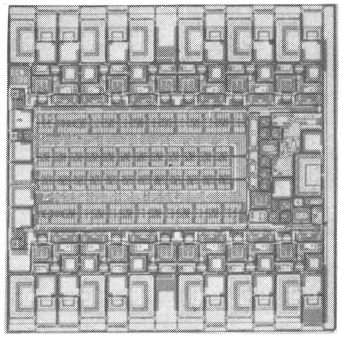


Fig.3. Photomicrograph of the 12 channel driver IC.

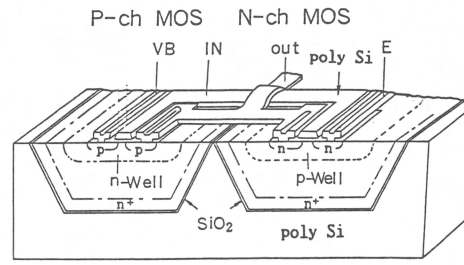



Fig.4. Structure of CMOS logics.

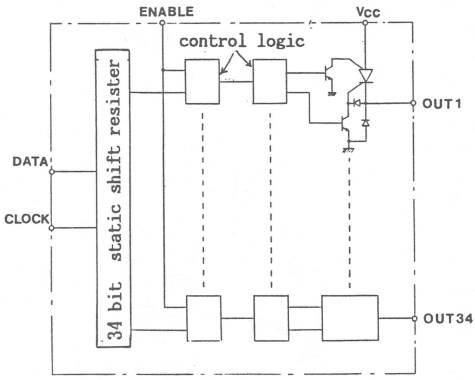



Fig.5. Block diagram of a 34 channel raw driver IC for flat panel displays.

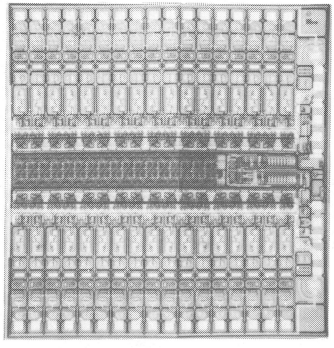


Fig.6. Photomicrograph of the 34 channel raw driver IC.

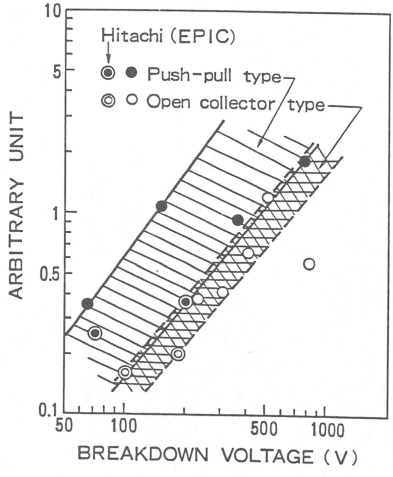



Fig.7. Chip size per a channel of driver IC's for flat panel diplays.

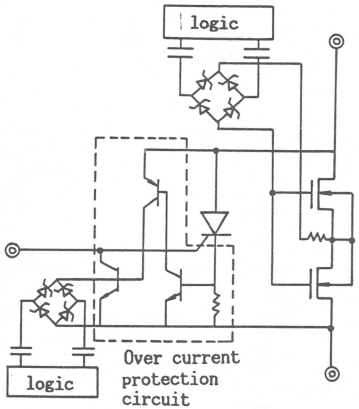



Fig.8. Block diagram per a unit of the linear switching IC for telecommunication uses.

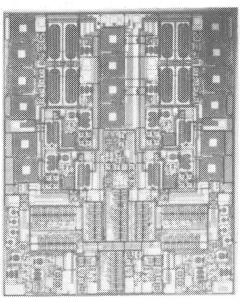


Fig.9. Photomicrograph of the linear switching IC.

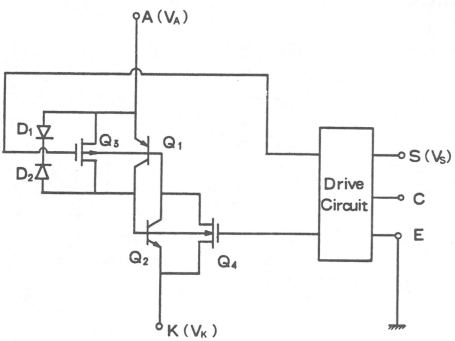



Fig.10. Equivalent circuit of a COGMOS thyristor.

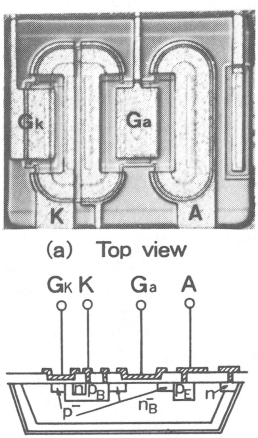



Fig.11. Structure of a COGMOS thyristor.

Proceedings of The Electrochemical Society, PV 1987-13, 106-117 (1987)
DOI: 10.1149/198713.0106PV © The Electrochemical Society

# THE EFFECT OF PECVD OXIDE ON THE THRESHOLD VOLTAGE AND LEAKAGE CURRENT OF TRANSISTORS FOR CMOS HIGH VOLTAGE INTEGRATED CIRCUITS

Henry W. Chien, Franklin F. Lee and Timothy J. Herbst
Telmos Inc. Sunnyvale, California.

## ABSTRACT

Plasma Enhanced Chemical Vapor Deposited (PECVD) oxide, which is used as an intermediate passivation layer for devices, has two effects on CMOS High Voltage Integrated Circuits (HVIC) utilizing the dielectric isolation (DI) technique. First, the leakage current of high voltage devices is significantly improved by PECVD oxide; secondly, the radiation damage caused by plasma during oxide deposition introduces threshold voltage shifts on both N- and P- channel MOSFET's in the low voltage logic sections. An optimized composite layer of PECVD and LPCVD oxide is developed to fully utilize the annealing effects of PECVD oxide and yet completely eliminate the threshold voltage shifts.

## I. INTRODUCTION

For device versatility and area efficiency, DI provides the best isolation solution for HVIC's (1). However, the technology to fabricate DI wafers is still in the development stage. The quality of DI wafers in terms of defects and cleanliness can not compare with conventional single crystal wafers. Stacking faults and defects introduced by the DI process manifest themselves electrically as high leakage current and low breakdown voltage.

The commonly known process techniques to reduce leakage current in devices such as backside damage and intrinsic gettering are not effective for transistors with DI substrates. Because the silicon tubs, into which the devices are built, are isolated from the polysilicon substrate by a thick layer of oxide, defects cannot be gettered through this thick oxide. An alternate way to reduce leakage current is to render the defects and surface states electrically inactive by passivating the devices with atomic hydrogen from the front side of the wafers. PECVD oxide is known to have a high concentration of atomic hydrogen. Experimental results clearly indicate that the PECVD oxide used as an intermediate passivation layer for HVIC with DI substrates significantly reduce the leakage current and improve device yield.

## II. PROCESS AND DEVICES OF CMOS HIGH VOLTAGE IC'S

All the IC's or devices reported in this paper were fabricated into dielectrically isolated wafers with N-type single crystal silicon islands.

The depth of the islands is optimized to meet the device breakdown voltage requirement of 500 volts.

The first step of the process is to pattern and implant the P-well and N-well, then drive in each well to 6 um with the same temperature cycle. One micron-thick field oxide was grown and the active device channel and source/drain regions were patterned and defined. An undoped 1.5 um-thick oxide was deposited on the field regions of the high voltage devices. The gate oxide regions were defined and etched down to silicon, followed by a 100 nm-thick gate oxide. Polysilicon for gate electrodes and field plates were then deposited, heavily doped with phosphorous, and patterned. The N+ and P+ contact regions, self-aligned to the gate polysilicon, was implanted and annealed. An intermediate passivation layer of oxide (IPOL) was deposited.

The IPOL is a layer of oxide to insulate metal from polysilicon. There are two different techniques to deposit oxide; the most common technique is Low Pressure Chemical Vapor Deposition (LPCVD), another one is PECVD. The basic chemical reaction for both techniques are the same. However plasma is formed during the PECVD process, the reaction needs less energy and the deposition temperature is lower compared to the LPCVD technique.

The experiments are designed to investigate the effects of PECVD oxide. Both LPCVD and PECVD deposited oxide are doped with 8% phosphorus. A composite layer with PECVD on top of LPCVD and with varying LPCVD thickness was employed. The total thickness of deposited IPOL is 3 um. After the IPOL was deposited, the oxide was densified and flowed in a steam ambient. Only the high voltage devices need 3 um of oxide in the field regions to alleviate the high electric field. The low voltage section, all contact regions, and the gate/source areas of high voltage VDMOSFET's are masked and etched down to 1 um. The cross sectional view after etch down is shown in Figure 1.

A high voltage IC with a die size of 67,000 square mils was chosen for this experiment. It is composed of 120 high voltage N- and P- channel transistors for level shifting functions and 16 large N-channel VDMOSFET's for output drivers. Twenty percent of the die area comprises the low voltage CMOS logic control section. Extremely low leakage current for all 16 output high voltage transistors is required. The leakage current limit for each transistor is 10 nA at a drain voltage of 450 volts. Therefore, high leakage current becomes the major yield limiting factor for this HVIC.

## III. CHARACTERISTICS OF LEAKAGE CURRENT

The leakage current of high voltage transistors occur sporadically from transistor to transistor, die to die, and wafer to wafer. The magnitude of leakage current also varies over several orders of magnitude; from nA to as large as uA. It is also observed that leakage current depends

on several factors including temperature, biasing configuration of the transistor, drain voltage and the post-metalization alloy process.

The high leakage current will occur in each of the following devices; VDMOS FETs, NPN bipolar transistors and IGT transistors. One of the major leakage failure modes is like "channel-type." The leakage current is saturated at a very low drain (or collector) voltage; typically less than 2 volts. Once the current is saturated, the current is constant with drain voltage until the drain voltage reaches the breakdown voltage of the device namely 500 volts.

All the bipolar NPN transistors and VDMOS FET's show that the leakage current is a strong function of temperature. Figure 2a shows the dependence of leakage current on temperature for a normal and leaky VDMOS FET. The normal transistor leakage current at 50°C is 0.4 nA and increases to 60 nA at 125°C. The leaky transistor leakage current at room temperature is 40 nA and increases to 500 nA at 125°C.

From the curve of temperature versus logarithm of current for the normal transistor, the slope of the curve is approximately equal to Eg/2kT, Eg is the energy band gap of silicon. This implies that the defects, which are recombination centers for leakage current, are at the middle of the band gap. The slope of the curve for the leaky transistor is less than Eg/2kT and its current is less temperature dependent.

From Figure 2b, it is interesting to note that a kink in the current versus drain voltage for a normal transistor occurs at a temperature of 100°C and increases as the temperature is increased at 125°C. The kink is also observed for the leaky transistor at room temperature. The current kink at a drain voltage around 30 volts implies that a cluster of defects, which are located at the edge of the depletion region, are activated and contribute to the abrupt increase in leakage current.

After metal masking and etching, the wafers are alloyed at 450°C in forming gas for 30 minutes. Figure 3 shows the change in leakage current before and after alloy. There are two types of transistors in terms of the leakage current change. One type of transistor (Figure 3a) shows that the leakage current decreases after alloy. The other type of transistor (Figure 3b), shows that the leakage current increases significantly after alloy, i.e. the leakage current is less than 3 nA before alloy and increases to 150 nA after alloy.

For an NPN bipolar transistor, the terminals of the emitter (N+), base (P-well) and collector (N- substrate) can be separately accessed. Different biasing configurations of the NPN bipolar transistors are investigated to locate the source of leakage current. It was found that the junction between the emitter and base or the junction between the base and collector does not have leakage current at room temperature. However, once three terminals form a close loop, the leakage appears. In

other words, if the emitter is shorted to the base, the leakage current appears as the voltage applied to the collector. Another configuration shows the same result, if the collector is shorted to the base, the leakage current appears as the voltage applied to the emitter.

Since the leakage current is dependent on the biasing configuration, it seems that the defects form a conduction pipe through which electrons leak from the emitter to the collector. The defects can be generated during the process steps to fabricate the devices (3) or to prepare the DI wafers (2).

## IV. PECVD OXIDE ON THRESHOLD VOLTAGE SHIFT OF MOSFETS

The normal threshold voltage is 1.2 volts for low-voltage N-channel and -2.5 volts for P-channel transistors. Without LPCVD buffered oxide, the N-channel transistor, especially for short channel transistors, shows excessive current at a drain voltage below the threshold voltage. Figure 4 shows the Ids (drain current) as a function of drain/gate voltage for transistors with different channel lengths. If the channel length is 10 um or more, no excessive current is observed in the subthreshold region. For transistors with a channel length of 5 um and 6 um, the devices show soft turn-on characteristics. The excessive current in the subthreshold region increases as the channel length of the devices decrease. This Ids vs Vds characteristic in the subthreshold region is similar to the punchthrough phenomena of regular short channel transistors.

Since the long channel device has normal Ids-Vds characteristics, it indicates that the damage caused by plasma can be impeded by the polysilicon gate electrodes. However, the damage caused by plasma at the edges of the polysilicon gate electrodes can propagate into the channel region under the gate. The transistor with a channel length of 6 um still has excessive leakage current in the subthreshold region. This implies that the damage can propagate as far as 3 um from each side of the electrodes.

Figure 5 schematically illustrates the effects of plasma induced damage on both N- and P-channel transistors with different channel lengths. For N-channel transistors, if the channel is long enough, such that the major center region of the channnel is not affected by the damage, then the threshold voltage and subthreshold conduction will behave like normal. If the damage propagates through most or through the whole channel region of the transistor, the threshold voltage is a function of position along the channel, and the potential barrier at the center could be very narrow; therefore, short channel behavior for Ids vs. Vds is expected for those transistors. The effects of plasma on P-channel transistors is different. The threshold voltage is a function of position along the channel too, but for holes, the peak of the potential barrier is at the edge of the electrodes. The peak potential barrier also is the measured threshold voltage of the transistor, because the current must flow through the peak

potential barrier. Therefore all P-channel transistors with different channel lengths have the same threshold voltage.

The damage induced by plasma on devices can be greatly alleviated by depositing a buffer layer of LPCVD oxide between the devices and PECVD oxide. The threshold voltage shift, which is an indication of the extent of the damage, is a strong function of the thickness of this buffer LPCVD oxide. Figure 6 shows the dependence of threshold voltage on the thickness of the buffer layer; (a) for N-channel transistors and (b) for P-channel transistors. The channel length for both types of transistors is 5 um. As the thickness of the buffer layer increases to 8,000 A, the threshold voltage of both types of transistors is restored back to the normal value. Without the buffer layer, the shift in threshold voltage is -0.5 volts for N-channel and -2.5 volts for P-channel transistors. The difference in threshold voltage shift between N- and P-channel transistors could be attributed to the smeared short channel potential barrier for N-channel transistors.

From the threshold voltage shift of P-channel transistors and gate oxide thickness, the plasma induced positive charge density at the $Si\text{-}SiO_2$ interface is estimated to be $5.1 \times 10^{11}$ $cm^{-2}$. Figure 4 shows the distance of damage propagation into the channel region under the gate electrodes. The minimum channel length of N-channel transistors which do not have excessive current in the subthreshold conduction region will increase as the thickness of the buffer layer decreases. The threshold voltage of all field transistors are shifted by plasma also. Figure 7 shows the threshold voltage of metal field transistors as a function of thickness of the buffer LPCVD oxide layer.

The real mechanisms of the plasma caused threshold voltage shift needs further investigation, but there are two possible mechanisms: first, the energetic particles and radicals in the plasma bombard the $Si\text{-}SiO_2$ interface, causing damage and inducing charges. Second, the charges are due to silicon dangling bonds at the $Si\text{-}SiO_2$ interface, which could be the result of the drift of Si ions and oxygen ions or their vacancies under the high electric field in the oxide during plasma deposition.

## V. PECVD OXIDE ON LEAKAGE CURRENT OF HIGH VOLTAGE TRANSISTORS

Experimental results consistently show that the PECVD oxide, either directly deposited on devices or with various thicknesses of LPCVD buffer oxide, has a great impact on leakage current of high voltage transistors and the wafer sort yield. Figure 8 shows the leakage current distribution for transistors from different wafers within the same lot, however, the only different process step is that half of the lot has PECVD oxide and the other half has LPCVD oxide as the intermediate passivation oxide. For the transistors with LPCVD oxide, the distribution of leakage

current has a wide range, from 0.4 nA to as high as 700 nA. Almost thirty percent (12 out of 40) of the transistors fail at the 10 nA criteria. On the other hand, for transistors with PECVD oxide, the distribution of leakage current is very tight, from 0.4 nA to 30 nA. Only 2.5% (1 out of 40) of the transistors fail at the 10nA criteria. Compared to the transistors with LPCVD oxide, the PECVD oxide improves the leakage current by one order of magnitude.

Figure 9 shows the distribution of wafers vs. the number of die on each wafer which fail at the leakage current test. For wafers with LPCVD oxide, the number of die failures can be as high as 67. The average number of failures is 52 die per wafer. For wafers with PECVD oxide, the average number of failures is 10 die per wafer.

Hydrogen passivation is used as a method to improve the transistor properties of MOSFET's fabricated in fine-grain LPCVD polysilicon (4). The annealing effects of PECVD oxide on the leakage current of transistors is similar to the applications in transistors on LPCVD polysilicon substrates. The high concentration of atomic hydrogen, typically greater than $10^{22}$ $cm^{-3}$, in the deposited PECVD oxide, acts as an ideal diffusion source for atomic hydrogen. Those active species of atomic hydrogen will migrate and diffuse through the field oxide and into the silicon substrate, passivating the defects, surface-states, and traps which are created during the high temperature fabrication process steps or the DI substrate preparation steps. Consequently, those defects become electrically inactive and reduce the leakage current significantly.

## VI. DISSCUSSIONS AND CONCLUSIONS

An optimized composite layer of LPCVD and PECVD oxide for HVIC's was developed to reduce the leakage current of high voltage transistors, improve the yield of devices and eliminate the radiation damage caused by plasma. Thus PECVD oxide passivation provides a fundamental solution to the weakness of DI material which is inherently susceptible to defects and insensitive to conventional established gettering process techniques.

## VII. ACKNOWLEDGEMENTS:

The authors would like to thank their colleagues: B.Weir, P. Shackle, F. Gonzalez, P. Mhaskar, C. Hodges and T. Arrieta for many useful discussions, S. Babino and L. Wright for process assistance. In addition, we also gratefully acknowledge Professor J. Plummer of Stanford University for helpful discussions.

## REFERENCES


(1) H.W. Becke, "Approaches to isolation in high voltage integrated circuits", in IEDM Tech. Dig., abstract 30.1, PP. 724-727, 1985.

(2) Y. Sugawara, K. Miyata and M. Okamura, "350 V analog-digital compatible power IC technologies," in IEDM Tech. Dig., abstract 30.2 PP. 728-731, 1985.

(3) M.A. Shibib and C.B. Ziemer, "Observation and analysis of negative resistance in the forward I-V characteristics of dielectrically isolated high-voltage gated diode switches," IEEE Trans. Electron Devices, VOL. ED-33, No. 7, PP. 1062-1065, July 1986.

(4) T.I. Kamins and P.J. Marcoux, "Hydrogenation of transistors fabricated in polysilicon-silicon films," IEEE Electron Device Lett., Vol. EDL-1, PP. 159, 1980.



* Frank F. Lee : Siliconix Inc., Timothy J. Herbst: Siemens.

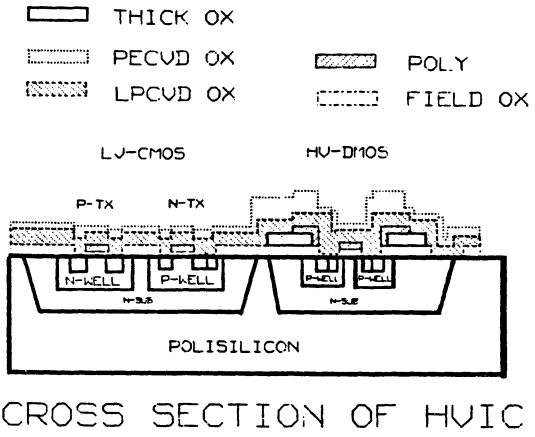



Figure 1 : Cross sectional view of CMOS high voltage IC's.

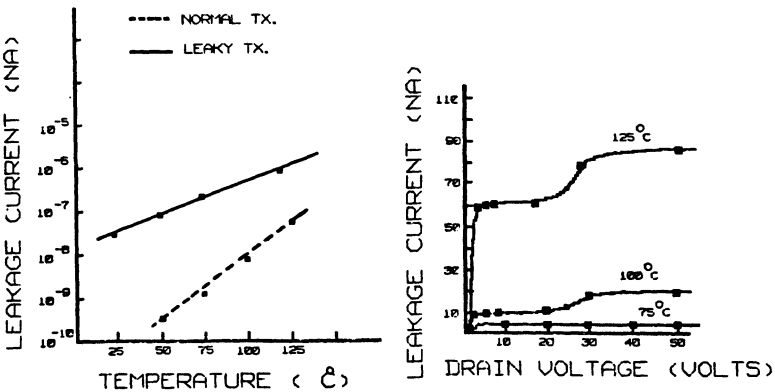



Figure 2 : Leakage current vs. temperature

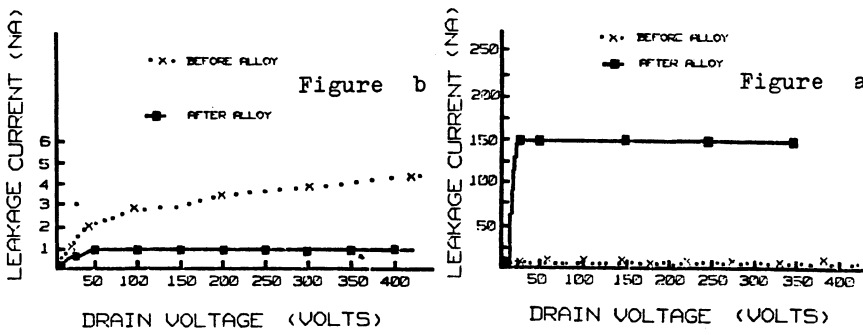



Figure 3 : The effects of alloy process on leakage current.

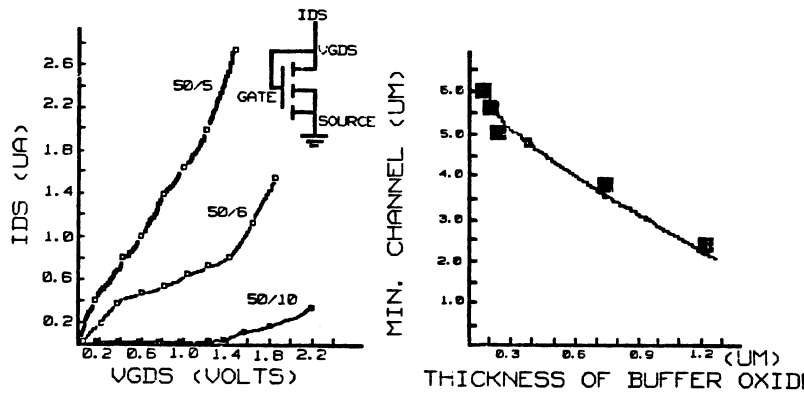



Figure 4 : Threshold voltage shift vs. channel length

Figure 6 b.

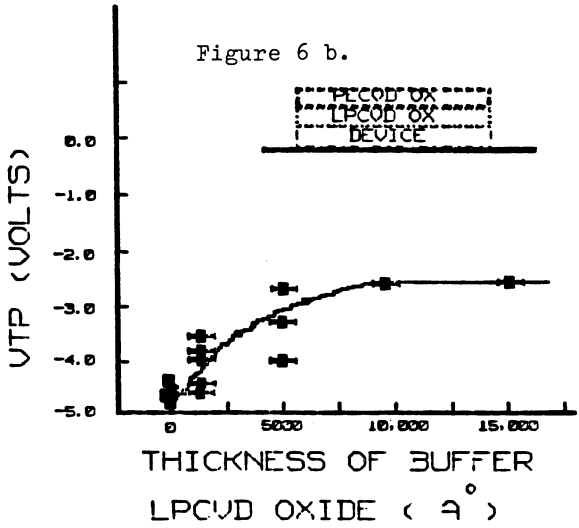



Figure 6 a.

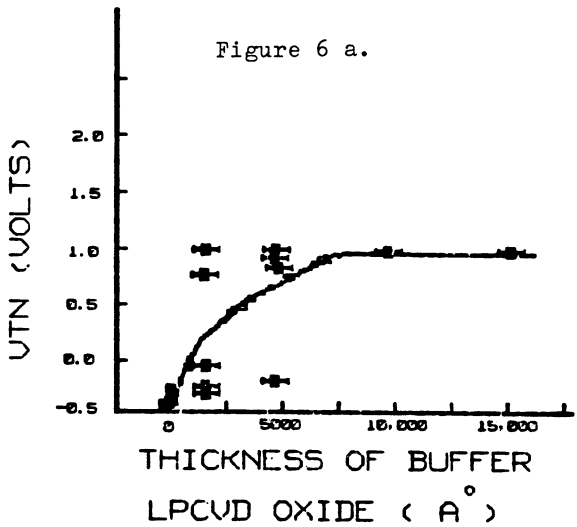



Figure 6 : Threshold voltage for low voltage MOSFET's vs. buffer oxide thickness

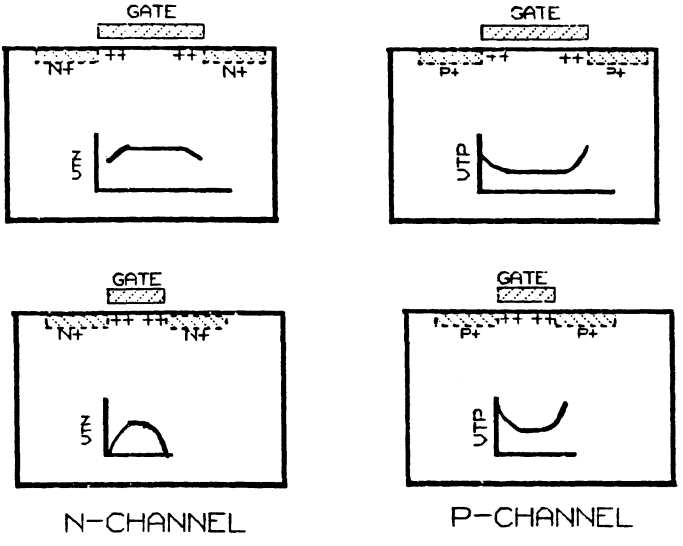



Figure 5 : Plasma damage vs. channel potential

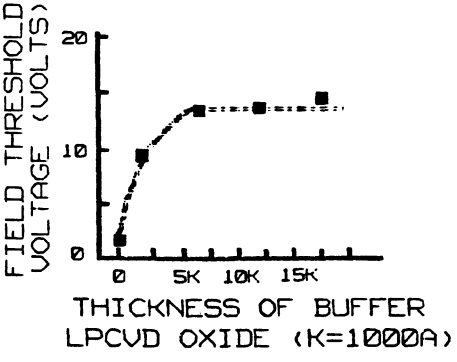



Figure 7 : Metal field threshold voltage vs. buffer oxide thickness

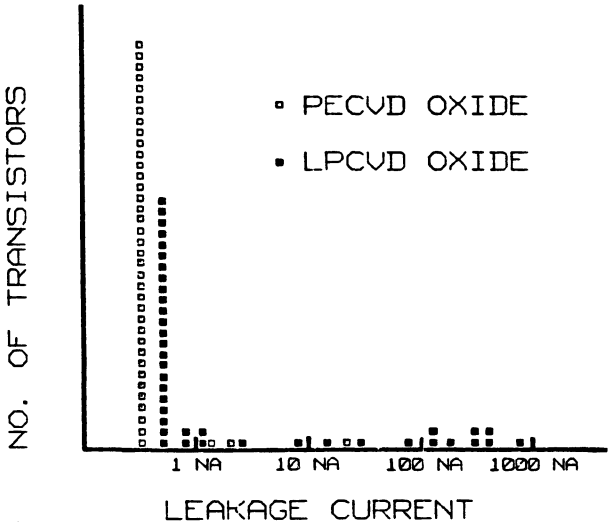



Figure 8 : Leakage current distribution for VDMOS FET's

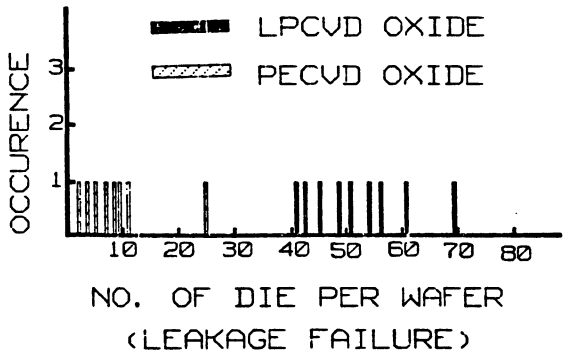



Figure 9 : Leakage failure distribution for wafers

Proceedings of The Electrochemical Society, PV 1987-13, 118-130 (1987)
DOI: 10.1149/198713.0118PV © The Electrochemical Society

# A HIGH-VOLTAGE DUAL-GATE DMOS STRUCTURE (DGDMOS)

C. N. Dunn, J. C. Gammel and M. A. Shibib

AT&T Bell Laboratories
2525 North 12th Street
Reading, PA 19612-3566

*ABSTRACT*

This paper describes the DGDMOS, a MOS gated bidirectional switching device. The structure is similar to a TRIMOS except it has separate gate contacts and a cellular array has been used to emphasize the linear DMOS characteristics.

Dielectric Isolation and Bipolar-CMOS-DMOS technology are utilized to design DGDMOS structures. The optimization of these structures to achieve a desired performance with respect to on-resistance, breakdown voltage, current break, current handling and surge capability will be discussed.

*SUMMARY*

This paper describes a DMOS gated bidirectional switching device that we call the DGDMOS. The structure incorporates two n-channel DMOS transistors in a single region with a common drain. The structure is similar to a TRIMOS described by Plummer and Scharf [1,2], but differs in its operational characteristics in that separate gate contacts are used to allow high voltage operation while using 1000 Å gate oxides and also a cellular array [3-5] has been used to emphasize the linear characteristic through the origin. Junction Termination Extension techniques [6-9] and field plates are used to obtain the desired voltage capability. The structure provides a linear characteristic through the origin in the on-state, high blocking voltage in the off-state, DC current break, and an ability to switch into a non-destructive thyristor mode in the presence of overvoltage or over current transients.

Dielectric Isolation (DI) and Bipolar-MOS (BCDMOS) technology [10,11] are used to design several compatible structures that provide a foundation for integration of high-voltage devices in a circuit. The DGDMOS is a key device in this technology, particularly in telecommunication applications. A floating feed and a current feed control circuit for the DGDMOS demonstrate the ease of control when using the DGDMOS.

The optimization of these DGDMOS structures to achieve a desired performance with respect to on-resistance [3-5,12,13], current handling and surge capability,

breakdown voltage and the ability to break DC current involves the tradeoff of interrelated parameters. For a 280 volt device that has a 10 ohm linear region for ± 100 mA we have found 8 ohm-cm material, 45 micron deep tubs and an overall size (including isolation) of 2.75 $mm^2$ to be adequate. The structure has an equivalent 280 active cells in each DMOS portion and a design Ron-Area product of 35 mohm-$cm^2$ for the active cells. Buried layer resistance and spatial allowances for source to source breakdown voltage are responsible for the remainder of the resistance. When the source-gate voltage is brought to zero ($V_{gs}$ = 0V) this device can interrupt 300 mA DC. The DGDMOS is also capable of withstanding current surges exceeding 10 Amperes as might be seen from a lightning transient.

## *INTRODUCTION*

In many telecommunications applications it is desirable to have a high-voltage bilateral switch-like function that provides a high OFF and a low ON impedance, is capable of being self protecting in the case of transient over voltage or current and is controlled by low-voltage circuitry. Such a device is the DGDMOS that uses two DMOS structures in a common DI tub.

When one looks at the possible ways of using a DMOS structure as a switch and requires that the device be bilateral there are two ways to hook up the structures. These are Source-to-Source with the Drains as the terminals or Common Drain with the Sources as the terminals. Of course there are many tradeoffs between these two alternatives and each has some distinct advantages. One advantage with the common drain approach is the fact that with the DI technology such a structure requires only one tub. Also this configuration has the parasitics of a thyristor and consequently it is possible to provide self protection under some of the typical stress conditions encountered in telecommunication applications.

Both devices have been used for several applications [11,14,15] and the intent of this paper is to document the salient points of the common drain device. In this paper we will discuss the current-voltage characteristic, equivalent circuit, cell array design, resistance calculations, control circuits, current break, surge and breakdown voltage capability of the DGDMOS.

## *CURRENT-VOLTAGE CHARACTERISTIC*

The coupling of the equivalent circuit and the current-voltage characteristics in the ON-STATE are essential to the understanding of the DGDMOS. This device has the same parasitic devices and characteristic regions as the TRIMOS described by Scharf and Plummer [1,2] and encompasses the IGBT [16] and COMFET [17] equivalent circuits as well. Each of these devices is optimized to accomplish a particular task and emphasizes different elements in the equivalent circuit by either enhancing or reducing the importance of that element. There are three distinct regions of behavior for the common drain mode ON-STATE operation. Referring

to Figure 1, they are (a) the linear region, (b) the IGBT (COMFET) region where the lateral anode is injecting holes and thus conductivity modulating the tub and finally, (c) the thyristor region where the combined current gain of the npn and pnp of the device has reached one and turned on the thyristor so that the gate no longer has control of the current flow. For the DGDMOS we are describing, we focus predominantly on the region of linear behavior where the voltage drop across the switch is less than 1.4 V. During surge conditions the "TRIMOS" (thyristor mode) will be used as a protective mode to carry large currents at the associated limited voltages.

In the OFF-STATE the DGDMOS shows the characteristics of a diode with low leakage current [11] up to the voltage where avalanche occurs. With sufficient avalanche current the device goes into the thyristor mode and must be protected by a series element (i.e., a 100 ohm resistor can be incorporated to limit a 10 μsec x 1000 μsec 1000 volt lightning pulse to 10 A).

*EQUIVALENT CIRCUIT*

An equivalent circuit for the DGDMOS is shown in Figure 2. The circuit consists of two DMOS transistors shunted by two npn and two pnp transistors connected in such a way that they can exhibit back-to-back thyristor behavior. Two emitter short resistors (base under emitter lateral resistors) are also necessary for the thyristor action. For the TRIMOS device the gates G1 and G2 are tied together and the values of $R_p$ are exaggerated to turn on the thyristor in the device operation [1,2]. For the IGBT device the shorting resistor is minimized to reduce the possibility of encountering the thyristor mode [13,18-22] and finally tying G2 to S2 creates a p-type anode needed in a lateral IGBT.

The equivalent circuit of the linear ON-STATE DGDMOS is shown in Figure 2b and consists of two back to back diodes each shunted by a resistor of half the series resistance of the switch. This circuit can be arrived at by assuming that S2 is positive and that p2 acts as a forward-biased diode into the N-well. There are only reverse junctions for the resulting current to flow out of the circuit except through the DMOS channel. In the OFF-STATE the DGDMOS is essentially two back-to-back high voltage diodes. The thyristor state is illustrated as follows; (a) take S2 sufficiently positive to inject holes from transistor p2, (b) collect these holes in the base of transistor n1 where, (c) they pass through the parasitic resistor $R_{p1}$. When the voltage drop across $R_{p1}$ exceeds 0.7 volts, transistor n1 turns on and a regenerative process takes place which completes the thyristor turn on. The resultant voltage drop across the switch is that of the thyristor.

More elaborate computer models of these circuits have been developed to include the parasitic capacitances and to simulate the MOS [23] and SCR [24] behavior of the device.

*CELL DESIGN AND ARRAY*

It has been shown in several papers that the cell design is the preferred way to construct a DMOS device [4,5,13]. The cells consist of two parts. The first component is the body and source region and the second component is the body to body spacing. Figure 3 shows the cross section of an edge cell in the body and source region and illustrates both the junction termination extension used for the edge termination [6-9] and the active DMOS structure. The body to body spacing is dictated by the tub resistivity, tub depth, and body and source dimensions. Selection of the body to body dimension of the cell will be discussed in the next section. The photo resist design rules and the diffusions that will be in the cell dictate the minimum source and body dimensions of the cell. This is because it is generally accepted that the body dimension of a DMOS should be as small as possible to achieve minimum resistance.

*RESISTANCE*

In this section we discuss the resistance of a DGDMOS structure. As has been previously discussed, the DGDMOS is two DMOS devices in the same tub. Also it has been established that each DMOS is a collection of individual cells and these can be characterized by an Area times Resistance product that represents the cell design [3-5,13]. $R_{on}$ x Area calculations have been made that represent cell geometries similar to those used in these devices using techniques that have been published [4,5,12]. A representative curve from this set is shown in Figure 4. These calculations are based on a square cell and the current distribution from the accumulation region has been calculated in two ways with the curves illustrating the small difference obtained. It has been our experience that this type modeling gives results in good agreement with actual devices. There are several components that comprise the resistance of these devices. In Figure 5 an illustration of the major resistance components is given. For example, the inversion layer and accumulation layers each contribute about 6% to the cell resistance with the JFET region contributing 18% and the tub showing 50% with the remaining 20% in the cell below the level where the spreading at 45 degrees has stopped. This latter resistance can be reduced by either controlling the tub thickness or allowing some punch through of the depletion region into the wraparound layer [25] with the attendant lowering of breakdown voltage capability. Finally beneath all this the resistance of the wraparound layer has to be considered.

Figure 6 shows the grid of cells that represent one DGDMOS device. This grid includes a substantial periphery to maintain a safe current density in the edge cells during surge conditions and adequate area to maintain the linear characteristic during normal operation. To calculate the total switch resistance it is necessary to build a network of resistors starting with this topological grid and including the wraparound layer resistance that will exist from finger to finger. Such a network is shown in Figure 7. From this it is possible to obtain the expected resistance (see

Figure 8) for a four finger interdigitated DGDMOS. For the resistance calculations used in this work it has been assumed that the current path is vertical to the wraparound layer and then across to the next finger and back up. This does not then allow for any lateral dispersion of the current. Considering the width of the fingers and the depth of the tubs, it is felt that this approximation is reasonable. Consequently these calculations are upper bounds for resistance. Analytical expressions can be differentiated to obtain the optimum length and width for each finger.

*CONTROL CIRCUITS*

In this section we explain the two representative control circuits that have been used to drive these DGDMOS devices. They are the floating feed and the current feed shown in Figure 9. The floating feed circuit is useful in those cases where there is a significant voltage differential between the switch and the control circuitry. Charge pumping [1,26] and optical-coupling [14,15] are two possible ways of providing the voltage to drive the floating feed bias circuit. The DMOS devices shown are used to direct current back to the supply, provide a voltage reference point for the DGDMOS and provide voltage isolation across the switch. The principal function of the JFET is to provide a low resistance connection between the gate and source of the DMOS structures when the switch is in the OFF-STATE. The JFET devices are also used to provide more useful voltage to the gates of the DMOS and DGDMOS devices by pinching off at a few uA ($V_p$ = 2V) [10] and consequently the JFET and resistor provide a voltage splitter with most of the voltage appearing source to drain on the JFET. The diodes are used for current steering, to block high voltage and because of this voltage blocking ability it is possible to use the same 1000 Å gate oxide thickness used in some CMOS processes. Consequently, the DMOS gate voltage is compatible with the low voltage control circuitry. With minor changes it is possible to use the floating feed circuitry to stack DGDMOS devices in series to provide switches with multiples of the intrinsic DI tub capability. Thus, by providing proper device and metal spacings this control circuitry is capable of controlling switches to 1000 volts.

Current feed circuitry is used in those cases where a direct return path to the current source is available through the DGDMOS switch load or supply circuitry. Possible current sources could be derived from either CMOS or Bipolar circuits. A simple one is using a pnp in a current mirror configuration. The diodes, resistors and JFETs are used in this circuit just as they were in the floating feed circuit.

*CURRENT BREAK AND SURGE*

One of the attributes of the DGDMOS device is that while it is operating in either the linear DMOS (all majority current) or the lightly conductivity modulated mode it is easy to break the current merely by turning off the MOS channel. Thus, exercise of the gate voltage will break substantial dc currents. Here the arguments

are the same as for the IGBT were efforts are made to avoid the latch into the thyristor mode (i.e., minimize the pnp gain, keep the emitter short as efficient as possible and maintain the npn at a low gain) [13,18-22]. Consequently as long as one can exercise gate control of the device (until the device goes into the thyristor mode) it is possible to interrupt the current. We have found that until these devices are conducting currents more than three times the current level at the onset of conductivity modulation there is no problem breaking current. (The high body doping and the low gain of the lateral pnp cooperate to maintain the minority carrier concentration below the level necessary to establish the regenerative conductivity modulation.)

Obviously connected with the current break capability limit is the ability to withstand a surge of current by switching into the thyristor mode of operation. Qualitatively, holes injected at the anode (Figure 10) reach the cathode and are collected and flow through the body-P under the Source-N to the common source/body (cathode) contact. The associated voltage drop can turn on the npn transistor of the DMOS and subsequently saturate the tub. This sequence is capable of regeneration and triggering the thyristor mode of operation. Since the process requires the collection of holes at the cathode, most of the regeneration process will take place along the periphery of the cellular array in a predominately lateral action. To simultaneously satisfy on-resistance and surge capability requires a careful trade-off of area ($R_{on}$) and periphery (surge). Figure 11 shows the distribution of ON-Voltage (operating voltage of a DGDMOS during surge) measured for the devices. Figure 12 shows the on state voltage-time characteristic of these same devices as they respond to a 9 Ampere surge.

The devices are measured for their dc current interruption capability and their ability to withstand the required surge for their respective applications.

*BREAKDOWN VOLTAGE*

Breakdown voltage for these devices is determined by a combination of factors. First it is necessary to review the breakdown voltage versus doping density curves that have been published [6,12,27,28]. Next the impact of design specific conditions such as radii of curvature, spacing separations unique to the design or doping profiles must be considered [29]. Selection of the minimum tub resistivity and tub depth to provide adequate breakdown voltage also takes into consideration the process variations expected. In Figure 13 a plot of breakdown voltage versus tub depth for 10 ohm-cm material is shown and illustrates the uniformity of breakdown voltage versus tub depth attained with a test structure similar to the DGDMOS designs that are being discussed in this paper. The junction extension edge termination [6-9] moves the breakdown voltage away from the edge and thus eliminates the walk out behavior typical of edge breakdown [30]. Also satisfied are the design requirements of optimal field plate design established by Conti and Conti (i.e., a thin oxide near the junction and a thick oxide at the field plate termination

edge) [31].

On the inside edge of the cell (Figure 3) the depletion edge will move into the body P diffusion. The lightly doped drain of this DMOS [11] and the higher doping profile of the body at the source edge will reduce the spread of the depletion region into the channel region.

*CONCLUSIONS*

In this paper we have described a device structure that is compatible with our DI-BCDMOS technology and can simultaneously satisfy several telecommunication needs. For example, low voltage control of a high voltage switch and a switch that can withstand the possibility of high current or voltage. Structurally, the DGDMOS is similar to a TRIMOS or a IGBT except that the DGDMOS is optimized via geometry and process variations for low MOS gate voltage, bidirectional linear current conduction and also to provide the ability to withstand a surge of current. In addition these structures are shown to have high-voltage blocking capability in the OFF-State and they have the ability to break dc currents while operating in the ON-State of more than three times the current level at the onset of conductivity modulation.

The control circuit techniques are compatible with other applications and are relatively simple to use and implement.

*ACKNOWLEDGEMENTS*

The authors would like to acknowledge the support and encouragement of T.J. Riley and the earlier efforts of G.K. Chang, A.M. Gottlieb, L.H. Fry, A.R. Hartman, J.E. Kohl and H.T. Weston in the design and construction of the DGDMOS structure. The participation of D.P. Chabinec, M.C. Dolly, C.A. Goodwin, M.L. Embree, R.A. Furnanage, M.P. Hammer, J.J. Joseph, R.F. Lee, C.Y. Lu, W.F. MacPherson, B.A. Mangieri, L. Pagano, P.C. Riffe, J.L. Schmoyer, N.S. Tsai, P.K. Tse and C.B. Ziemer in turning these devices into robust devices is also greatly appreciated.

*REFERENCES*

[1] J. D. Plummer and B. W. Scharf, "Insulated-Gate Planar Thyristors: 1-Structure and Basic Operation", IEEE ED-27, February 1980.

[2] B. W. Scharf and J. D. Plummer, "Insulated-Gate Planar Thyristors: 2-Quantitative Modeling", IEEE ED-27, February 1980.

[3] P. L. Hower, T. M. S. Heng and C. Huang, "Optimum Design of Power MOSFET's", IEDM 83

[4] Chenming Hu, Min-Hwa Chi and V. M. Patel, "Optimum Design of Power MOSFET's", IEEE ED31 December 1984.

[5] K. Board, D. J. Byrne and M. S. Towers, "The Optimization of On-Resistance in Vertical DMOS Power Devices with Linear and Hexagonal Surface Geometries", IEEE ED-31, January 1984.

[6] B. J. Baliga, "High-Voltage Device Termination Techniques, a Comparative View", IEE P Vol 129, October 1982.

[7] V. A. K. Temple and W. Tantraporn, "Junction Termination Extension for Near-Ideal Breakdown Voltage in p-n Junctions", IEEE ED-33 October 1986.

[8] S. Ahmad and J. Akhtar, "A Proposed Planar Junction Structure With Near-Ideal Breakdown Characteristics", IEEE EDL-6, September 1985.

[9] S. Georgescu, T. Dunca, D. Sdrulla and I. Ghita, "Planar Termination for High-Voltage p-n Junctions", Solid-State El., Vol29, No.10, 1986.

[10] C. A. Goodwin, et al., "A Dielectrically Isolated Bipolar-CMOS-DMOS (BCDMOS) Technology for High Voltage Applications", ECS, May 1987, Proceedings of High-Voltage Symposium.

[11] C. Y. Lu, et al., "An Analog/Digital BCDMOS Technology With Dielectric Isolation - Devices and Processes", to be published

[12] S. C. Sun and J.D. Plummer, "Modeling of the On-Resistance of LDMOS, VDMOS, and VMOS Power Transistors", IEEE, ED-27, February 1980.

[13] M. H. Chi and C. Hu, "Some Issues of Power MOSFET's", 1982 IEEE PESC

[14] J. C. Gammel, "High Voltage Solid State Relays for Telecommunications", ELECTRO/85 Proceedings, April 85

[15] M. A. Banak, et al., "High Voltage Custom IC's Using BCDMOS Technology", Custom IC Conference Proceedings, May 1987.

[16] B. J. Baliga, et al., "The Insulated Gate Rectifier", IEDM 1982.

[17] J. P. Russel, et al., "The COMFET - A New High Conductance MOS-Gated Device", IEEE EDL-4, 1983.

[18] B. J. Baliga, "Analysis of Insulated Gate Transistor Turn-Off Characteristics", IEEE EDL-6 1985.

[19] H. Yilmaz, "Cell Geometry Effect on IGT Latch-Up", IEEE EDL-6, 1985.

[20] B. J. Baliga, et al., "Suppressing Latchup in Insulated Gate Transistors", IEEE EDL-5, 1984.

[21] Chenming Hu and Min-Hwa Chi, "Second Breakdown of Vertical Power MOSFET's", IEEE ED-29, August 1982.

[22] L. A. Goodman, "Recent Advances in Discrete Power Transistors", IEDM 1984.

[23] M. N. Darwish, "Study of the Quasi-Saturation Effect in VDMOS Transistors", IEEE ED-33, 1986.

[24] J. J. Joseph, unpublished work

[25] S. K. Ghandhi, SEMICONDUCTOR POWER DEVICES, New York, Wiley, 1977.

[26] G. Remmerie and L. Van Den Bossche, "10 ohm 370 volt High Voltage Switches for Line Circuit Application", IEEE SC-19, June 1984.

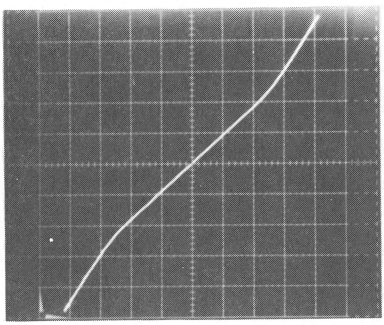
[27] D. R Decker and C. N. Dunn, "Temperature Dependence of Carrier Ionization Rates and Saturated Velocities in Silicon", Jour. of Electronic Metals, Vol4, No3, 1975.

[28] M. S. Adler, "A Comparison Between BIMOS Device Types", IEEE ED-33, February 1986

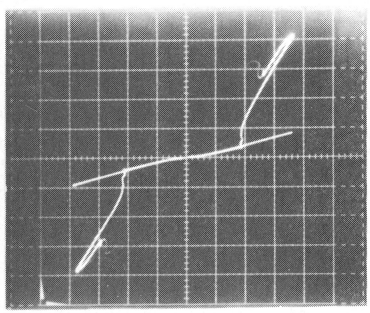
[29] M. D. Pocha, J.D. Plummer and J.D. Meindl, "Tradeoff Between Threshold and Breakdown in High-Voltage Double-Diffused MOS Transistors", IEEE ED-25, November 1978.

[30] J. F. Verwey, et al., "Drift of the Breakdown Voltage in p-n Junctions in Silicon (Walkout)", Solid-State Electronics, Vol 20, 1977.

[31] F. Conti and M. Conti, "Surface Breakdown in Silicon Planar Diodes Equipped with Field Plates", Solid-State Electronics, Vol 15, 1972.



(a) LINEAR-50mA PER VERTICAL DIV. 500mV PER HORIZONTAL DIV.



(b) CONDUCTIVITY MODULATED & THYRISTOR-500mA PER VERTICAL DIV. 2V PER HORIZONTAL DIV.

FIGURE 1 CURRENT VOLTAGE CHARACTERISTICS

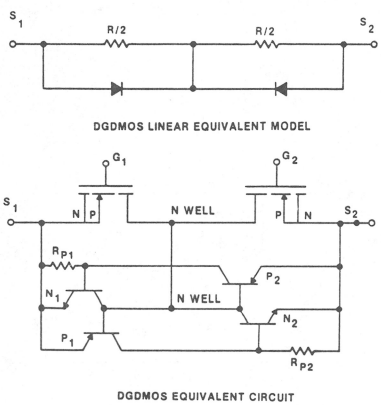



FIGURE 2 EQUIVALENT CIRCUITS FOR DGDMOS

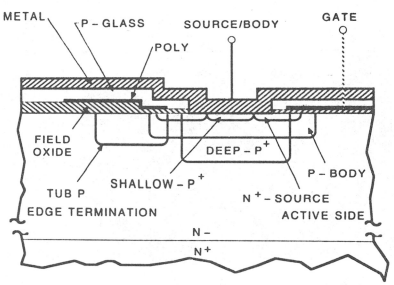



FIGURE 3 CROSS SECTION OF A DGDMOS EDGE CELL

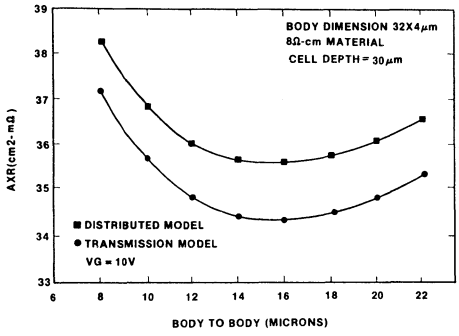



FIGURE 4 AREA X RESISTANCE PRODUCT VS BODY SPACING

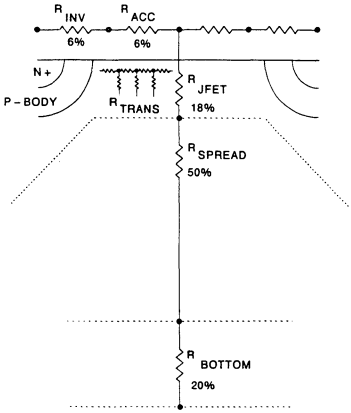



FIGURE 5 RESISTANCE DISTRIBUTION FOR TYPICAL CELL-250 V DESIGN

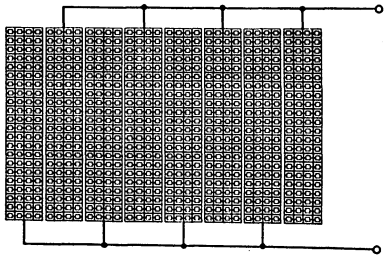


FIGURE 6 SURFACE TOPOLOGY OF 4-FINGER DGDMOS

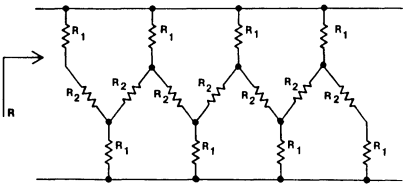



FIGURE 7 RESISTOR ARRAY OF 4-FINGER DGDMOS INCLUDING BURIED LAYER

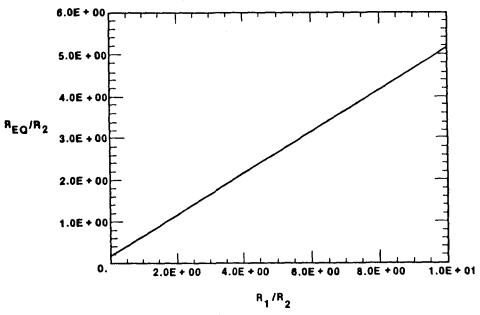



FIGURE 8 RESISTANCE OF 4-FINGER DGDMOS VS FINGER AND BURIED LAYER RESISTANCE

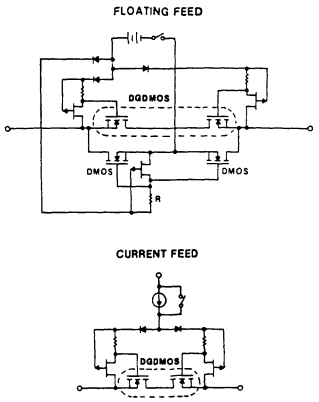



FIGURE 9 CONTROL CIRCUITS FOR DGDMOS

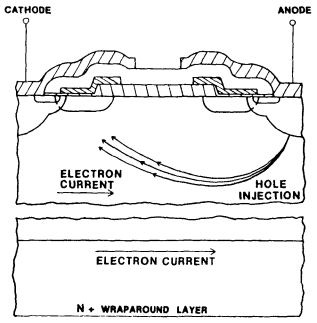



FIGURE 10 HOLE AND ELECTRON CURRENT IN DGDMOS

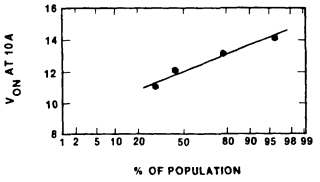



FIGURE 11 DISTRIBUTION OF ON-VOLTAGE FOR DGDMOS DURING 10 X 1000μS-10A SURGE

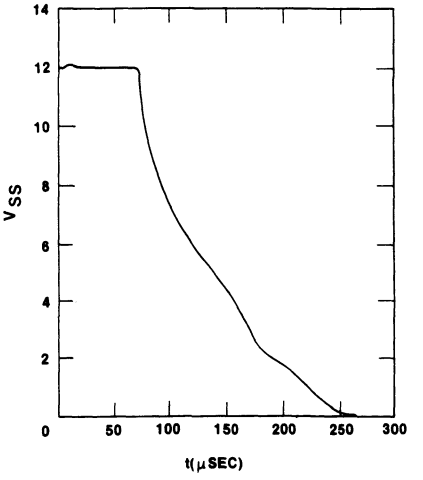



FIGURE 12 DEVICE RESPONSE TO 9AMP SURGE

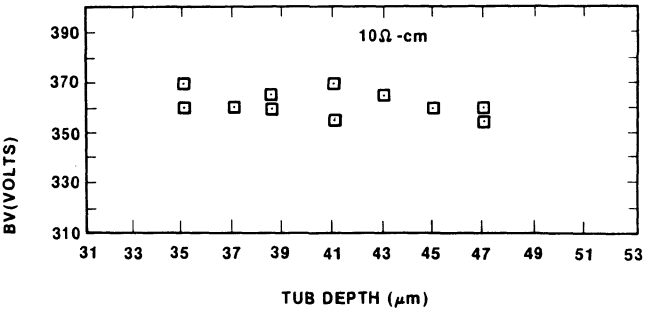



FIGURE 13 BREAKDOWN VOLTAGE VS TUB DEPTH FOR DGDMOS

Proceedings of The Electrochemical Society, PV 1987-13, 131-146 (1987)
DOI: 10.1149/198713.0131PV © The Electrochemical Society

# THE STATUS OF ISOLATION IN HIGH VOLTAGE INTEGRATED CIRCUITS

Hans W. Becke
AT&T Bell Laboratories
600 Mountain Avenue
Murray Hill, NJ 07974-2070

John C. Gammel
AT&T Bell Laboratories
2525 North 12th Street
Reading, PA 19612-3566

Abstract

This paper reviews high voltage integrated circuits, their isolation methods, and device features. Conventional Junction Isolation can be used for voltage requirements > 200 volts if special upward-downward diffusions are employed or if the RESURF principle is applied. Self Isolation is limited to common source arrays. Dielectric Isolation is most versatile and area efficient. MOS-Bipolar combination devices, complementary design, and on-chip logic are the trends in HVICs.

## INTRODUCTION

Semiconductor applications requiring high blocking voltages and high power densities are generally still using discrete devices assembled on PC-boards, modern surface mount (SOT) techniques included. Also, thick film and thin film techniques are applied for making passive components and interconnections to form hybrid circuits with semiconductor chips on ceramic substrates.

The evolution in semiconductor technology together with new developments in high voltage devices have made it feasible to integrate high voltage and high power circuits containing control, level shift functions, and logic into monolithic chips.

A list of major application areas with their voltage requirements is given in Table 1.[1]

| Applications | Voltage Requirement |
|---|---|
| Display Drivers-Plasma | 160 V AC, 320 P-P |
| Telecommunications | ≈500 V (also 325 V) |
| Regulators | Full Range |
| Switch Mode Power Supplies | 300-1000 V |
| Protection Circuits | Full Range |
| Motor Controllers | 400-800 V |
| Inverters | 300-600 V (1000 V) |
| Ultrasonic Imaging | 200 V |
| Electrostatic Printers | 500-600 V |
| Luminescent Displays | 250-300 V |
| Automotive Electronics | 50 V, 20 A |
| TV Deflection Circuits | 1000-1500 V |
| Multivoltage Chips - | |
| Control of Power Devices | 5 V Logic & |
| Logic/Level Shift | HVIC |

Table 1 - Major Applications and Voltage Requirements for High Voltage ICs[1]

One of the foremost problems for realization of HV ICs is to find a satisfactory solution for the isolation of components and subcircuit sections. The isolation techniques fall into three major categories: a) Junction isolation where for high

voltage applications components must be isolated by relatively deep diffusion; b) Self isolation where high voltage components share a common connection; and c) Dielectric Isolation where components are typically isolated from each other by an oxide wall.

Before discussing these isolation techniques we will briefly discuss junction termination techniques as this impacts the device thickness for a given breakdown voltage and this, in turn, affects the space required for the isolation barrier.

## JUNCTION TERMINATION TECHNIQUES

The conventional approach to achieving high breakdown voltages is the use of deep diffusions on lightly doped substrate material.[19] Deep diffusion is required to minimize surface breakdown due to sharp junction radius of curvature. In high voltage integrated circuits this has the disadvantage of increasing the overall device thickness requirement and the space required to isolate the high voltage devices.

One technique for improving breakdown voltage is Junction Termination Extension or JTE. With this method the junction is surrounded by a lightly doped diffusion which depletes rapidly and reduces the surface fields. This allows the realization of nearly ideal parallel plane breakdown voltage relatively shallow junctions.

A possibility to further extend the voltage range while minimizing the device thickness required is offered by using the "RESURF" principle.[2] Figure 2 shows the basic idea. A (thin) layer (N) is placed on top of a high resistivity substrate of opposite conductivity ($P^-$). The thin (N) layer is then surrounded by an opposite conductivity diffusion (P) which contacts the substrate.

For a substrate concentration of 3E14 when the total charge per $cm^2$ in the N-region between the $N^+$ and $P^+$ contact $Q_{tot} = \int N(x)\,dx > 1.2$ E12, then the top layer is only partially depleted and surface limited breakdown will occur (Figure 2a); for $\int N(x)\,dx < 1.2$ E12, the top layer is completely depleted before the critical field is reached and full bulk breakdown is obtained (Figure 2b).

Since the (two-dimensional) charge distribution in the RESURF layer is arbitrary, epitaxial growth, ion implantation, and concentration variations along the surface can be used to obtain optimized high voltage structures.

This allows high voltage devices to be built in relatively thin layers. While JI is depicted in Figure 2 these same concepts can be used with DI and for the termination of any lateral high voltage device structure.

## JUNCTION ISOLATION (JI)

### Standard Junction Isolation (JI)

For the conventional JI the active device layer is usually grown on an epitaxial substrate of opposite conductivity type. Deep isolation diffusions electrically separate devices, and high concentration buried layers reduce the bulk series resistance as shown at the top of Figure 1. This method is useful, in general, to voltages of 60 volts[3], in the extreme up to 150 volts. An improvement in voltage capability is achieved for thick epi-layers if the isolation diffusion is composed of an up-diffusion from a buried layer and a surface diffusion as shown at the bottom of Figure 1. Voltages capabilities of 400 volts have been reported for this modification.[4],[5]

The "RESURF" principle has been applied to high voltage JI devices at up to 1200V as illustrated in Figure 3 for the case of lateral NPN transistor.[6],[7] Using "RESURF" JI circuits containing logic, level shift functions, and high voltage drivers (350-500 V) for direct control of output devices in motor controls and power supplies, have been developed.[8]

While the area required for isolation in a JI technology is considerable, this may not be a disadvantage when integrating large power devices or large sections of low voltage circuitry which only need one isolation barrier to the high voltage circuitry.

A special class of JI devices (or circuits) are those consisting of one high voltage vertical transistor with integrated low voltage circuitry. In this case the low voltage circuitry can be built into the base of a high voltage bipolar transistor or body of a high voltage MOS transistor and no extra isolation diffusions are required. This approach is often referred to as the "Smart Power" technology.[9],[10]

### Self Isolation

In some IC applications individual devices share a common terminal and do not need to be fully isolated from each other. In this case the devices can be considered to be self-isolated. Self Isolation (SI) for HV ICs can, for example, be employed for an array of output MOS devices having a common source the gates being driven by integrated CMOS logic. Figure 4 is an example for 400 volt output devices, the application being used in a 200 volt plasma display with 2MHz bandwidth.[11]

## DIELECTRIC ISOLATION

Coventional DI is a method by which single x-tal islands (tubs) are embedded in a polysilicon substrate, dielectrically isolated by an insulator, generally silicon dioxide. The typical sequence of the substrate fabrications is illustrated in Figure 5.

This approach is the most versatile. Virtually all components existing as discrete devices can be integrated in this form. It is possible to use bipolar and MOS technology on the same chip; also, complementary functions are feasible. Bidirectional switch arrays with integrated controls having 600 volt capabilities are already being mass produced.[12] GTO-thyristors are integrated with other bipolar components for use as a cross-point arrays in telecommunication circuits.[13],[14] Recently, high voltage custom ICs with mixed high voltage/low voltage capability have been reported.[15],[16]

Also, other Dielectric Isolation techniques such as Silicon Direct Bonding SDB[17],[18] and Lateral Epitaxial Overgrowth (e) have been investigated. Using these techniques, it may be possible to go to larger diameter wafers (150 mm instead of the 100 mm commonly used at present) with improved uniformity.

## COMPARISON OF JI WITH DI

Because DI requires a certain amount of preprocessing for generating the substrate, a higher cost may be expected for this approach over JI. Nevertheless, the advantages of DI are:

1. Parasitic multi-junction structures do not exist between components and undesirable latch-up conditions or substrate injection are eliminated. Also, the dielectric layer can easily provide > 1000 V isolation; and a wrap-around layer as shown in Figure 5d [also see Figure 6] will allow positive or negative potentials on the substrate without affecting leakage current and breakdown voltage of the component.

2. A much denser packing of components will result in substantial area savings. Figure 6 explains this fact for the example of two NPN-transistors. The schematic at the top shows that for JI a distance $D \sim 0.1\ (BV)^{7/6}$ is required.[19] Thus, for 400 volt devices the distance D~110 microns. For DI this distance is independent of the breakdown voltage and 10 microns is a rather easily attainable value, determined from process tolerances. Component separations as small as D~5 microns have been reported if a precision process for depth control is employed.[20]

## A CONDUCTIVITY MODULATED MOS THYRISTOR (THYMOS)

Recently, MOS-Bipolar combination devices[21],[22],[23] are gaining more and more importance; in general, the lateral version of them being particularly suitable for use in HV ICs. These devices feature a voltage controlled input (MOS-gate) for ease of drive and have a bipolar output, whereby means of conductivity modulation a low resistance is achieved.

Thus, a very efficient high voltage switch, capable of operating at high power densities, is available. A schematic cross section of such a device in DI is depicted in Figure 7.

For operation between Terminal T1 and T4 as output with T2-T1 as input, the conventional DMOS behavior is obtained. When the output is taken between T1 and T3, the device will operate in several modes. In the non-regenerative region (below latch-up), the device is an IGBT (also known as COMFET[24],[25], IGT[26],[27] or GEMFET[28]; beyond latch-up the device operates as a MOS-gated Thyristor.[29],[30],[31]

Figure 8 shows the MOS-mode, the device On-resistance being about 30 Ohms per 1 cm of source width (gate width). This value is reduced to 2.5 Ohms per 1 cm cathode width for the IGBT mode as shown in Figure 8b. Latch-up occurs at a cathode current density of $J=1000A/cm^2$. Figure 8c is the VI-characteristic for the thyristor mode with 10 V gate drive applied (10 steps, IV/step). The On voltage for a cathode current density of $3300A/cm^2$ is 2.0 volts. Figure 8d represents a multiple exposure of the VI-curve taken from the "On" state to the "Off" condition for DC without gate drive.

## APPLICATION EXAMPLES

In this section we will describe two HVICs in production at AT&T that use Dielectric Isolation. These devices were fabricated using the second generation BCDMOS process.[15],[16]

The first example is a gate array with 250 volt output drivers (LA500 Gate Array/Driver). This IC was developed to provide rapid prototype of high and low side switches selectable by an on-chip CMOS interface (see Figure 9). The center portion of this IC has 120 gates of 20 V CMOS logic. This layout used conservative (7μm) design rules. The use of standard cells and 5μm design rules would allow for about 500 gates in the same area. The periphery of this IC has large DMOS transistors for output drivers, small DMOS and PMOS transistors for level shifting and pre-drivers and an assortment of bipolar transistors, CMOS transistors, resistors, and diodes for interfacing and analog functions. A device library for the Gate Array/Driver appears in Table 2.

## HIGH VOLTAGE DEVICES

| Device | BV | $R_{ON}$ (Ohms) | $V^{TH}$ |
|---|---|---|---|
| 8-Large DMOS | 275V | 50 | 2.4V |
| 8-Small DMOS | 275V | 1.4k | 2.4V |
| 4-Large PMOS | 300V | .69k | -1.25V |
| 4-Small PMOS | 300V | 14.3k | -1.25V |

## BIPOLAR DEVICES

| Device | BV | Beta |
|---|---|---|
| 4-NPNs | $90V_{CEO}$<br>$250V_{CBO}$ | 300 at 200μA |
| 4-PNPs | $60V_{CEO}$<br>$200V_{CBO}$ | 60 at 30μA |
| 4-Blocking Diodes | 310V | -- |
| 16-13 Volt Zeners | 12.9V | -- |
| 16-26 Volt Zeners | 25.6V | -- |

## LOW VOLTAGE CMOS DEVICES

| Device | BV | $V_{TH}$ | Z/L |
|---|---|---|---|
| 240-Logic NMOS | 28V | 1.25V | 11 |
| 240-Logic PMOS | 32V | -1.25V | 11 |
| 12-Peripheral NMOS | 26V | 1.25V | 13 |
| 12-Peripheral PMOS | 26V | -1.25V | 40 |

RESISTORS (TCR –4800ppm°C)

8-5k, 10, 1.6 Meg.
4-20k, 25k, 40k, 100k, 360k

Table 2 - Device Library for the High Voltage Gate Array Driver

The second example is the LH1056 350V optically controlled solid state relay. In this device a pair of 350V DMOS transistors is controlled by a photodiode stack and a JFET pre-driver. A simple current limit scheme using a small current sense resistor and NPN feedback allows this typically 32Ω switch to survive during lightening surges. The negative temperature coefficient of the current limit and photo-diode stack output disables turn-on above 150°C, thus affording further protection against overloads. This device in particular benefited from the DI process by eliminating all interaction between the 27 photodiodes and the rest of the devices. A chip photo for this device is shown in Figure 10.

## CONCLUSIONS

This paper is an update of a 1985 talk on the same subject.[32] Since that time Junction Isolation in the 200-300V region has been shown to be practical in many applications. Progress in Dielectric Isolation has also continued at a rapid pace with mixed high voltage/low voltage ICs. Dielectric Isolation has proved its value in allowing the rapid development of high voltage ICs free from unwanted parasitics, substrate injection and latch-up. High Voltage ICs continue to be an area of considerable growth in the fields of power electronics and telecommunications.

## Acknowledgments

The authors would like to thank Messrs. T. J. Riley and S. M. Sze for their support and encouragement. Special thanks to J. G. Mena for his help in assembling some of the additional reference material. We would also like to thank our colleagues Messrs. K. Miyata (Hitatchi), R. Roop (Motorola), P. Shackle (Siliconix), R. Sittig (Siemens), E. Stupp (Philips), and E. Wildi (GE) for their input.

## REFERENCES


1. A. R. Hartman, "Summary of Discussion on High Voltage Integrated Circuits"; 1980 IEEE Power Semiconductor Devices Workshop, December 1980, pp. 11.
2. J. A. Appels and H. M. J. Vaes, "High Voltage, Thin Layer Devices (RESURF Devices)"; 1979 IEDM Conf. Digest, December 1979, pp. 238-241.
3. Siliconix-Electronic Design, February 1984.
4. SGS Semiconductor - Integrated Circuits, March/April 1984.
5. A. Ludiknize, "A Versatile 250/300V IC Process for Analog and Switching Applications"; IEEE TED ED 33, pp. 2008, December 1986.
6. E. E. Wildi e. al., "500V BIMOS Technology and Its Applications"; Electro/85, 24/2, April 1985.
7. M. F. Chang et. al., "Advanced 1200V HVIC Technology"; 1986 IEDM Technical Digest, pp. 230-233, December 1986.
8. M. S. Adler et. al., "The Evolution of Power Device Technology"; IEEE Trans. ED, pp. 1570-1591, see Figure 26, pp. 1584, November 1984.
9. S. Lytle et. al., "Power BIMOS - A Versatile IC Technology for Switching and Regulations Applications"; Cust. Integrated Ckt. Conference, pp. 51-56, 1984.
10. J. L. Sutor et. al., "A Novel Isolation Structure for SMART power ICs"; 1986 IEDM Technical Digest, pp. 214-216, December, 1986.
11. H. Wakaumi et. al., "Highly Reliable 16 Output High Voltage NMOS/CMOS Logic IC with Shielded Source Structure"; 1983 IEDM, pp. 416-420, December 1983.
12. H. T. Weston et. al., "Monolithic High Voltage Gated Diode Crosspoint Array IC"; 1982 IEDM Digest, pp. 85-88, December 1982.
13. T. Kusaka et. al., "A High Voltage Dielectric Isolated Thyristor Crosspoint Array"; NEC Research and Development, 57, pp. 39-45, April 1980.
14. Tatsuya Kamei, "High Voltage Integrated Circuits for Telecommunications"; 1981 IEDM Digest, pp. 294, December 1981.
15. M. A. Banak et. al., "High Voltage Custom ICs Using BCDMOS Technology"; CICC/87.

16. C. A. Goodwin and M. A. Shibib, "A Dielectrically Isolated Bipolar, CMOS-DMOS Technology (BCDMOS) for High Voltage Applications"; Symposium on High Voltage and Smart Power Devices, May 10-15, 1987.

17. Hiromichi Ohashi et. al., "Improved Dielectrically Isolated Device Integration by Silicon-Wafer Direct Bonding (SDB) Technique"; 1986 IEDM Conf. Digest, December 1986, pp. 210-213.

18. Y. Ohata, T. Izunita, "Intelligent Power Switch"; CICC/87.

19. Ghandhi, "Semiconductor Power Devices"; John Wiley & Sons, 1977.

20. F. Ohira et. al., "Extended Abstracts of the Electrochemical Society"; Spring Meeting, Volume 85-1, pp. 178, 1984.

21. R. Jayaraman et. al., "Comparison of High Voltage Devices for Power Integrated Circuits"; IEDM Tech. Digest, pp.258-261, 1984.

22. D. N. Pattanayak et. al., "n-Channel Lateral Insulated Gate Transistors: Part I - Steady-State Characteristics"; IEEE Trans. Electron Devices, ED 33, pp. 1956-1963, December 1986.

23. Z. Paspia, J. G. Mena, and C. A. T. Salama, "A Novel CMOS-Compatible High Voltage Transistor Structure"; IEEE Trans. Electron Devices, ED 33, pp. 1948-1952, December 1986.

24. H. W. Becke, C. F. Wheatley, "Power MOSFET with an Anode Injection"; U.S. Patent 4,364,073, Issued December 14, 1982.

25. J. P. Russel et. al., "The COMFET - A New High Conductance MOS - Gated Device"; ED Letters, EDL4, pp. 63-64, 1983.

26. B. J. Baliga et. al., "The Insulated Gate Rectifier (IGR): A New Power Switching Device"; 1984 IEDM Conference Digest, pp. 264-267, December 14, 1982.

27. B. J. Baliga et. al., "Insulated Gate Transistor: A New Three-Terminal MOS-Controlled Bipolar Power Device"; IEEE Trans. ED, pp. 821-828, June 1984.

28. K. Gauen, "Power MOSFET Variant Excels at High Loads"; Electronic Design, pp. 103-110, April 1984.

29. J. D. Plummer, B. W. Scharf, "Insulated Gate Planar Thyristors: I and II"; IEEE Trans ED, pp. 380-394, February 1980.

30. J. Tihanyi, "Integrated Power Devices"; 1982 IEDM Conference Digest, pp. 6-10, December 1982.

31. A. Pshaesnich, "The MOS-SCR, A New Thyristor Technology"; Motorola Eng. Bulletin, ED-103, 1982.

32. H. W. Becke, "Approaches to Isolation in High Voltage Integrated Circuits"; 1986 IEDM Technical Digest, pp. 724-727, December 1986.

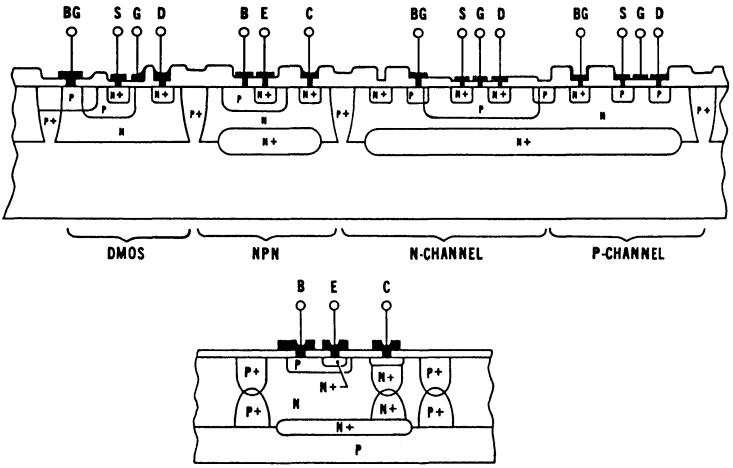



FIGURE 1 – EXAMPLE FOR CONVENTIONAL JI
TOP: 60-90 VOLT CAPABILITY [2]
BOTTOM: 200-400 VOLT CAPABILITY [3].

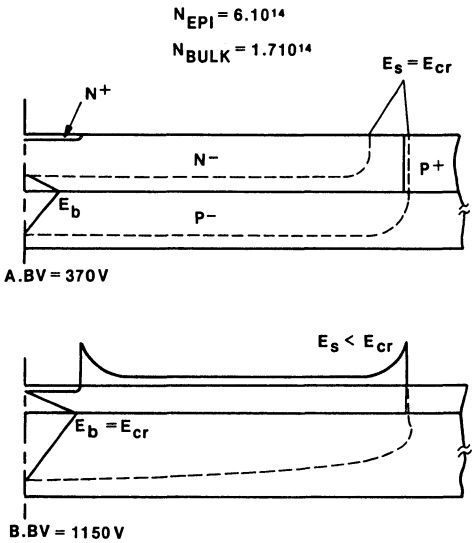



FIGURE 2 – RESURF PRINCIPLE [4]. A - SURFACE LIMITED BREAKDOWN B - BULK BREAKDOWN.

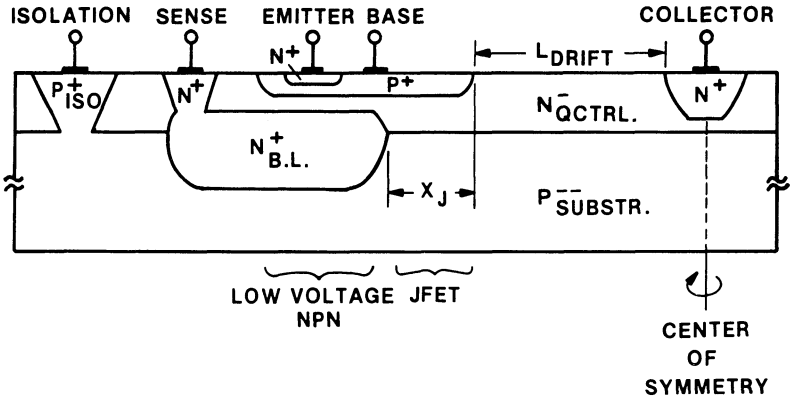



FIGURE 3 – HIGH VOLTAGE LATERAL NPN TRANSISTOR DEVICE STRUCTURE SHOWING LOW VOLTAGE NPN AND HIGH VOLTAGE JFET PORTIONS OF THIS COMPOSITE DEVICE [5].

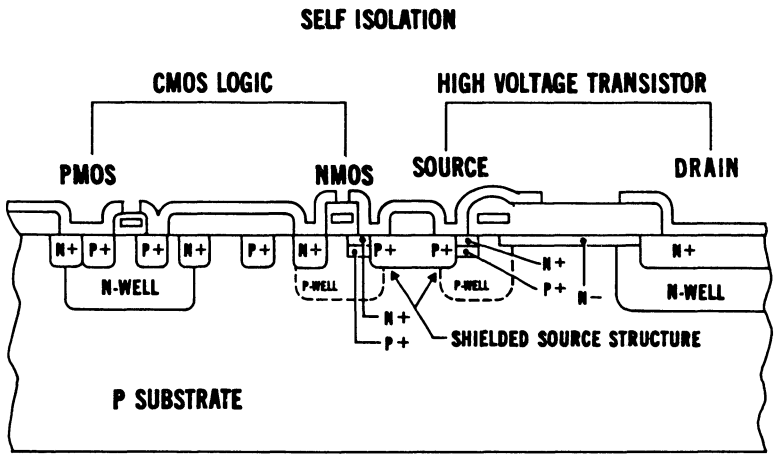



FIGURE 4 – ISOLATED DRAIN–COMMON SOURCE HIGH VOLTAGE NMOS WITH INTEGRATED CMOS LOGIC [8].

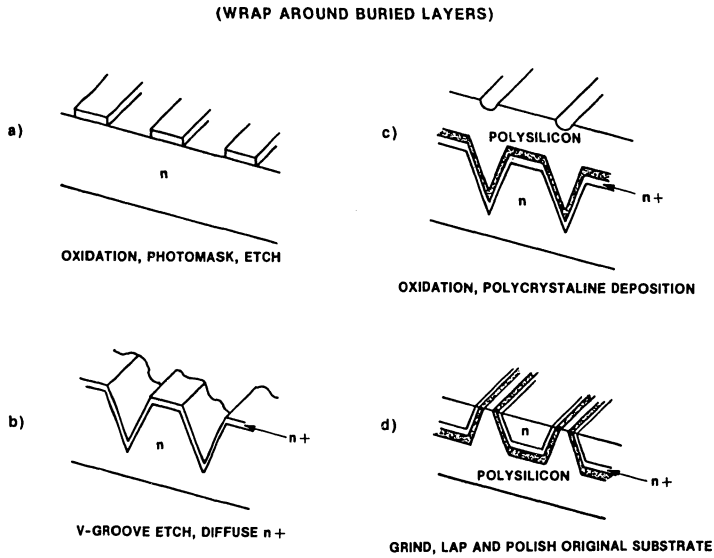



FIGURE 5 – MAIN PROCESS STEPS IN FABRICATION OF A SUBSTRATE FOR HIGH VOLTAGE DIELECTRICALLY ISOLATED IC'S.

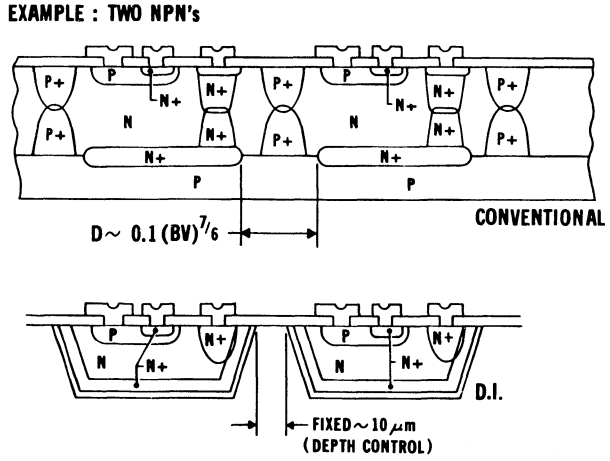



FIGURE 6 – COMPARISON OF SPACE REQUIRED BETWEEN ADJACENT DEVICES FOR JI (TOP) AND DI (BOTTOM).

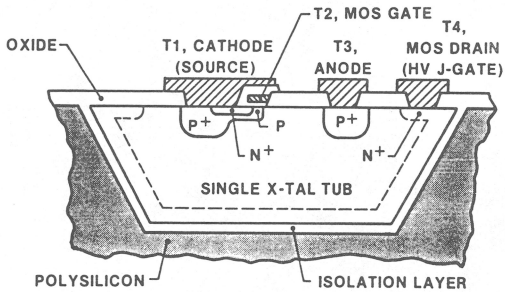



FIGURE 7 – SCHEMATIC CROSS SECTION OF A LATERAL THYRISTOR-MOS COMBINATION DEVICE (THYMOS).

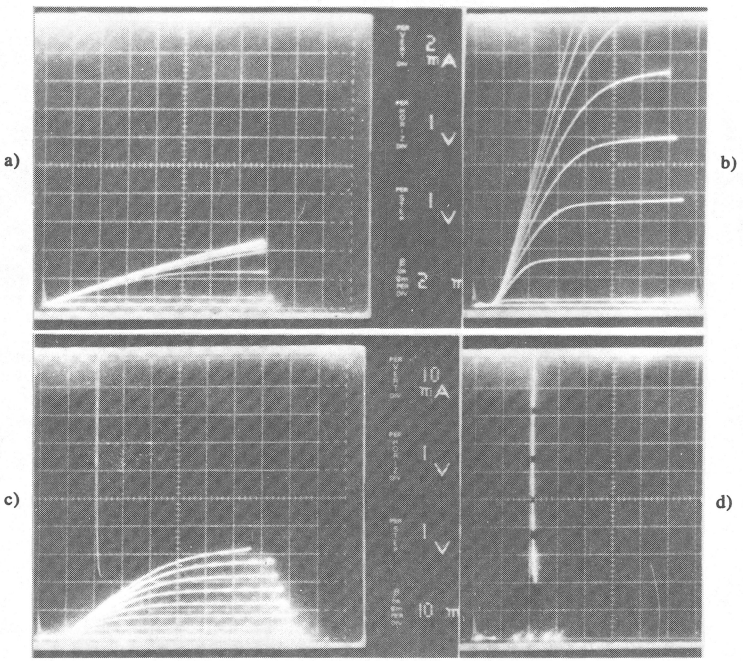



FIGURE 8 – THYRISTER-MOS COMBINATION DEVICE (THYMOS).
a) MOS MODE; b) COMFET MODE; c) GATE-DRIVEN IV-CHARACTERISTICS (1V/STEP, 10 STEPS)
d) IV-CHARACTERISTIC WITHOUT GATE DRIVE (MULTIPLE EXPOSURES FORM "ON" TO "OFF" STATE)
CATHODE CURRENT DENSITY $J = 1000 A/cm^2$ @ $I_A = 30mA$.

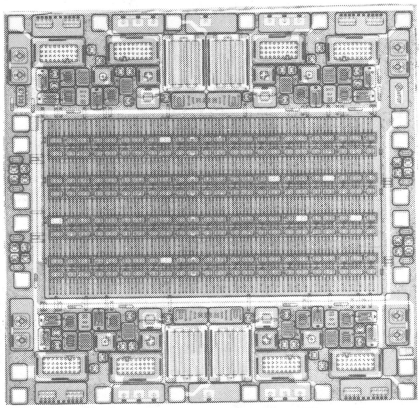


FIGURE 9 – CHIP PHOTO OF LA 500 GATE ARRAY/DRIVER.

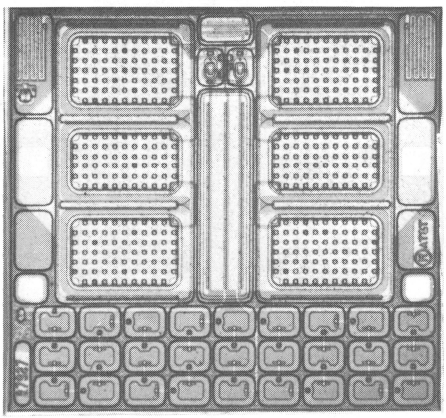


FIGURE 10 – CHIP PHOTO OF LH 1056 SOLID STATE RELAY.

# DISCRETE HIGH VOLTAGE DEVICES

## SESSION CHAIRMAN:

ADRIAN COGAN
SILICONIX

Proceedings of The Electrochemical Society, PV 1987-13, 150-156 (1987)
DOI: 10.1149/198713.0150PV © The Electrochemical Society

# The MOS Controlled Thyristor (MCT) and Smart Power IC's*

V.A.K. Temple
General Electric Research and Development Center
1 River Road
Schenectady, NY 12301

* This work was partly done with EPRI funding.

INTRODUCTION: There are several ways to combine MOS and thyristor elemets to form advanced devices. Recently, both GE [1,2] and Siemens [3] have desribed anew device termed the "MOS GTO" by Siemens and the MCT, a more inclusive name, by GE. The key element of the device is the MOS device located accross the upper emitter-base junction of the vertical thyristor element which, when turned on, shorts out the upper emitter and quenches the thyristor internal positive feedback, thus allowing it to turn off. Figure 1 shows the basic unit cell structure on the right along with an equivalent circuit diagram on the left. Looking at the equivalent circuit it is clear that, when on, the FET will be able to divert an upper base current given by the on-state emitter-base forward drop divided by the FET path resistance. Peak controllable current is approximately

$$Ioff = 2\ Vj/(Al*Rfet) \qquad (1)$$

where Vj is the on-state emitter-base junction drop, Al is the current gain of the lower transistor contained in the thyristor structure and Rfet is the FET resistance. Typically 1000 to 2000 A/cm2 can be turned off at room temperature[1-3] with 20 volts applied to the MOS gate. The largest turn-off current density reported has been 6000A/cm2 [1], while the largest reported current turned off has been 200A [3] at room temperature with a resistive load.

Device turn on is simply accomplished by including an appropriate density of IGT-like cells to initiate turn-on. This means that one gate polarity (This single gate electrode which is pulsed one polarity for turn-on and the other for turn-off.

In the following sections we will describe MCT operation, concentrating on forward drop and turn-off capability as affected by temperatures from room to 300C and by load ranging from resistive to 20mH inductive. In addition, one section will be devoted to high frequency operation.

FORWARD DROP: Figure 2 shows a forward drop comparison of a number of power devices that can be turned off with moderate gate drive energy. Clearly the thyristor based device is much more highly modulated than any of the other devices

which results in a 50-fold higher current density at 2V forward drop than the next best device. Figure 3 shows that this drop is less than a volt at 100A/cn2 for devices electron irradiated to increase switching speed.

TURN-OFF PERFORMANCE: Figure 4 shows turn-off waveforms in an SOA (Safe Operating Area) experiment on a 400 cell device. It was found that we could turn-off about 100A/cm2, unsnubbered, with a 20mH inductive load into a clamp voltage of 400V. This 200C result shows that the MCT has an inherently higher SOA than one would expect of a power transistor, an IGT or a GTO. Modelling and experiments, to be more completely described in another paper, show this to be due to the more uniform MCT current flow and its essentially plane and uniform forward blocking junction. Other tests showed that essentially the same current could be turned off with a 5mH load as with a 25 ohm load in 200C, unsnubbered turn-off tests. The explanation for this behaviour is that the latched MCT condition is broken before the device voltage starts to rise appreciably.

Figure 5 plots turn-off capability vs. off-FET gate voltage for a 10000 cell MCT. About 100 A/cm2 could be turned off at 200C with 20 volts on the MCT gate. Appreciable current could still be turned off at 250 and 300C. Life tests were performed at 200C and 250C, as shown in the figure, in which the MCT was turned off, unsnubbered, with a 20mH load to a 400V clamp level. Finally, four 100 mil devices were successfully operated in parallel to increase current capability by nearly a factor of 4. Parallelling of 30 such devices is being done at this time and wil be reported shortly.

The 100 A/cm2 turned off at 200C is not a limit of the MCT but rather the first results of a 25 micron cell size DMOS-based FET process which is already being optimized to have shorter channel length and higher density. Even the device structures of this paper, while termed MCT's, would more accurately be desribed as C-MCT's (complementary MCT's) since we wanted the FET diverted current to be electron for its two times higher FET channel mobility. It is felt that a 2 to 3-fold increase in 200C turn-off rating is achievable without pushing DMOS process capability.

HIGH FREQUENCY OPERATION: The 7 or 8 microsecond turn-off shown in Figure 4 was for a non-irradiated MCT wafer. Figure 6, however, shows 100kHz operation at 200C and turning off 100A/cm2 in a 100 cell MCT that had been electron irradiated to 4 megarad/cm2. Several dynamic MCT advantages can be seen. Turn-on delay and turn-on current risetime are very fast. The MCT reaches its final on-state voltage without a long and lossy plasma spreading phase. Essentially di/dt capability is no longer a device limitation as it was in the thyristor.

It should also be obvious that MCT dv/dt capability is also essentially unlimited, since with the off-FET's activated the thyristor structure is very heavily shorted (every half mil, for example). This high short density explains the MCT's very high temperature capability, at least in part, but does not explain why the MOS structure is so rugged with respect to temperature. This result we attribute to the fact that the built-in MCT off-FET is located entirely within the neutral region of the device and never sees a larger source to drain potential than the forward bias of the emitter-base junction. Moreover, the FET carries an extremely low average current and even during turn-off it carries less than half of the device current.

The turn-off current fall in Figure 6 leads indicates a 1.5 microsecond, recombination time limited turn-off time for this 4 Megarad electron irradiated device, inferring about a .75 microsecond turn-off time for the 8 Megarad case. However, fastest turnoff times were seen with proton dosed MCT's, the advantage of protons lying in the fact that recombination centers can be put where they can be most effective [6]. Figure 10 compares 400 cell MCT's from the same wafer half of which were protected from a 1e13/cm2 dose of 2.13 Mev protons. Evidently turn-off time has been reduced to several hundred nanoseconds. This turn-off is exceptional and indicates that efficient line voltage circuits employing MCT's could operate at megahertz frequencies.

MCT DRIVER CHIP SPECIFICATION: The ideal MCT driver chip is very similar to that of an IGT except that a second gate voltage supply (at comparatively low energy) is needed. An ideal chip should generate whatever power supply levels it needs from the MCT anode-cathode, monitor MCT current, voltage and temperature and use this data along with optical or logic level input from a master control to gate the MCT using high speed switches on the IC. An HVIC would be ideal but an IC with some 20V capability could be made to work (i.e. for -8V to turn on and +12 to turn off).

SUMMARY: Recently a new class of power devices has been described that is based on an optimal combination of MOSFET and thyristor structures. In this paper we show that devices of this type have greatly increased capabilities. For example, we have fabricated 700 volt devices with .2 microsecond turn-off time, operating to 300 degrees Celcius with a forward drop of less than one volt while retaining the MOS advantage of low energy gate control. Such devices should have enormous impact on smart power systems and circuits.

REFERENCES:
1) V.A.K.Temple "MOS-Controlled Thyristors" 1984 IEDM Technical Digest
2) V.A.K. Temple, "The MCT, a New Class of Power Devices", IEEE Trans on Electon Devices, ED-33, p. 1609 (1986)
3) M. Stoisiek and H. Strack, "The MOS-GTO, a Thyristor with MOS-Controlled Emitter Shorts" IEDM Technical Digest (1985)
4) V.A.K. Temple and D.N. Pattanayak, "Forward Voltage Characteristics of the MCT", IEEE Trans. on Electron Devices (in review)
5) A. Herlet, "The Forward Characteristics of Silicon Power Rectifiers at High Current Densities", Solid State Electron., V11, p. 717 (1968)
6) V.A.K. Temple and F.W. Holroyd, "Improved Trade-off Between Turn-off Time and Forward Drop", IEEE Trans. on Electron Devices ED-30, p.782 (1983)

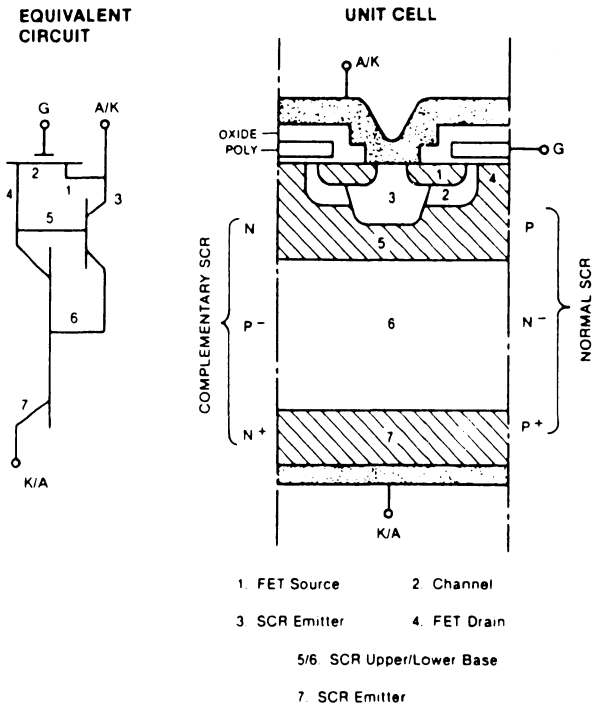



Figure 1. Left: Circuit schematic of a typical MCT unit cell. Right: Cross section. To turn off the MCT the FET is turned on to unlatch the thyristor structure.

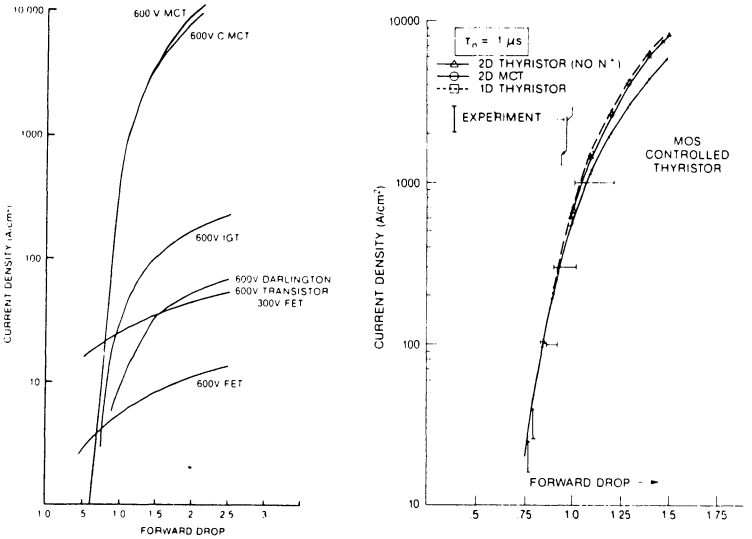



Figure 2. Left: Forward drop comparison of 600V power devices. Right: Experimental vs. 2-D modelled MCT forward drop.

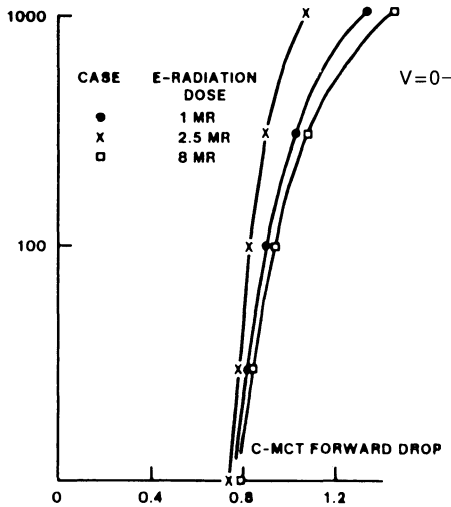



Figure 3. MCT forward drop vs. electron radiation dose.

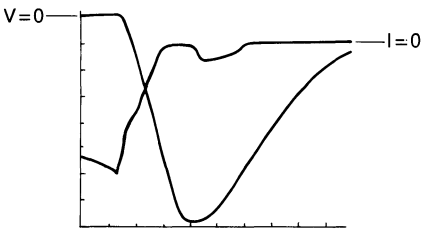



Figure 4. MCT SOA test. 20mH load, 200C, unsnubbered, 400 cell MCT. 50mA/div, 50V/div, 5us/div.

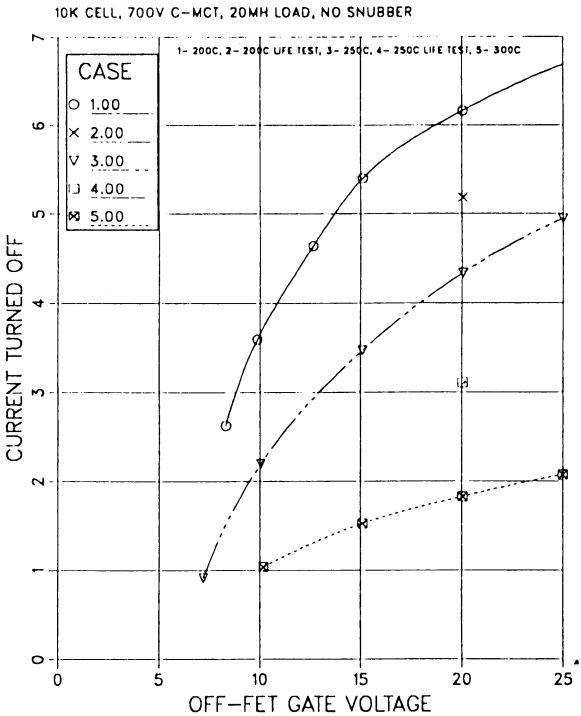



Figure 5.
10000 cell MCT turn-off as a function of gate voltage and temperature, unsnubbered with a 20 mH load.

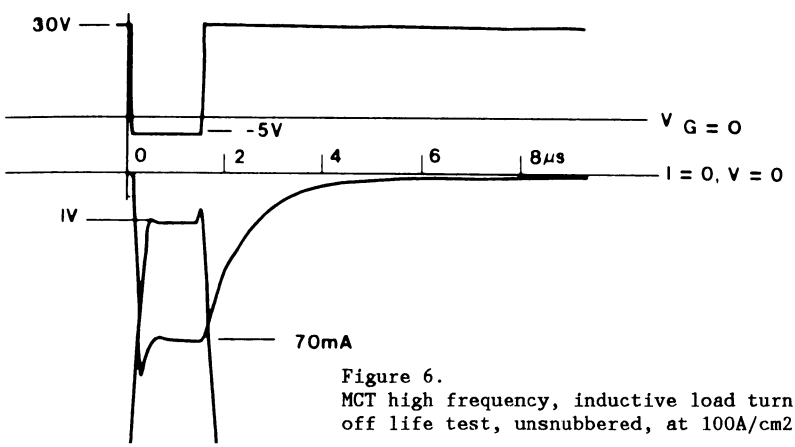



Figure 6.
MCT high frequency, inductive load turn-off life test, unsnubbered, at 100A/cm2.

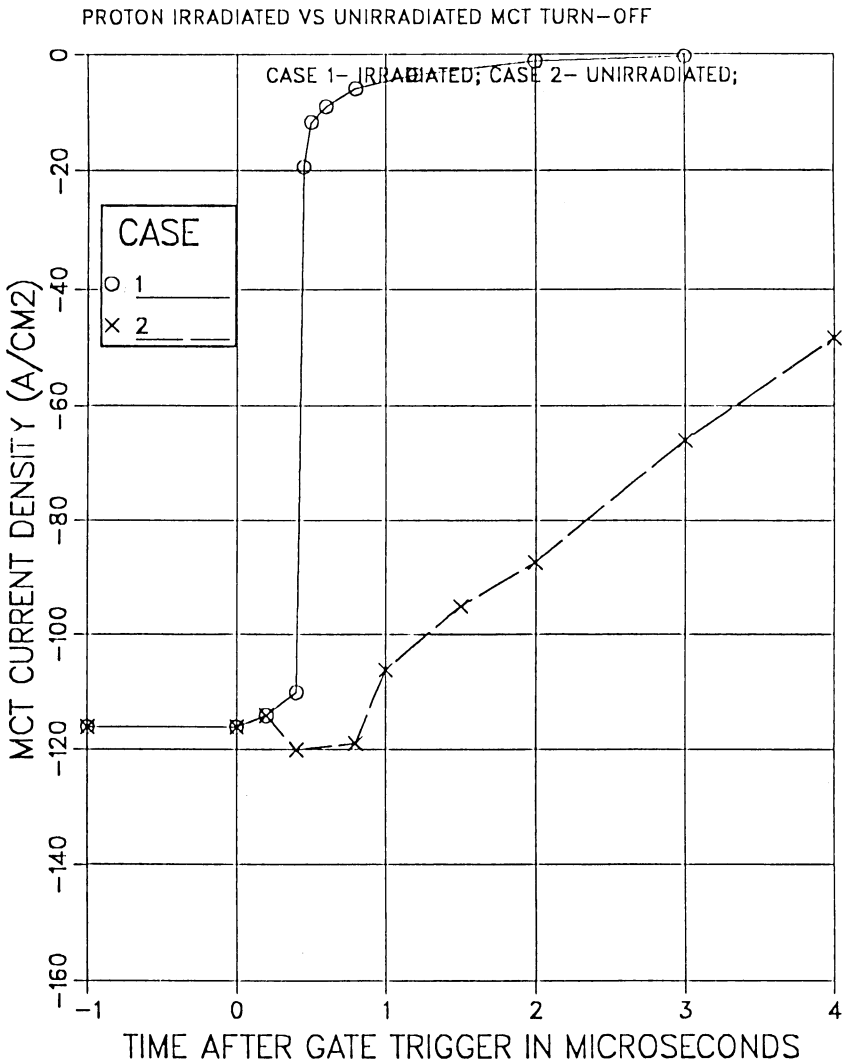



Figure 7. Turn-off comparison of unirradiated and proton irradiated 400 cell MCT's. Proton dose was 1e13/cm2 at 2.13 Mev.

Proceedings of The Electrochemical Society, PV 1987-13, 157-165 (1987)
DOI: 10.1149/198713.0157PV © The Electrochemical Society

# THE ACCUMULATED LAYER UNDER THE GATE ELECTRODE IN VDMOS DEVICES

J. Rebollo, J. Millán and F. Serra-Mestres.

Centro Nacional de Microelectrónica, CSIC-UAB. Bellaterra. Barcelona. Spain.

A model for the access resistance of high and low voltage VDMOS devices is proposed in this work. It is based on surface resistance and bulk conductance differential elements to account for the change of the current direction in the epitaxial layer. Rectangular or trapezoidal access resistance can be assumed depending on the voltage-handling capability of the device. The surface resistance elements correspond to the accumulated layer under the gate electrode and the bulk conductance elements depend on the current pinching between neighbouring cells. The oxide thickness between cells influences on the $I_D(V_D)$ characteristics through the accumulated layer resistance, this effect being more remarkable for low voltage VDMOS devices.

## 1. INTRODUCTION

Technological advances together with new structures achieved in the 70's have made possible an increase of voltage, current and power-handling capabilities of MOS devices. Power MOS technology has followed two main lines: new power MOS devices and the integration in the same chip of power devices as well as a low voltage control logic (PIC's).

Amongst the most important types of power MOS devices available on the market we should mention the VDMOS since it is the most widely used as a discrete device. These devices are formed by the parallel association of a multitude of short-channelled MOS transistors -in order to increase its current capability- and by a lightly doped epitaxial layer which extends from the channel itsef up to the drain contact; this epitaxial layer determines the voltage capability of the device. Consequently, a VDMOS device can be considered as a short-channelled MOS transistor in series with an epitaxial resistance depending on the device bias.

It is widely considered that the VDMOS epitaxial resistance has three main components (1, 2): a.- the accumulated layer resistance at the epilayer surface under the gate electrode, b.- the JFET resistance between neighbouring cells and c.- the bulk epilayer resistance that accounts for the current spreading in the semiconductor bulk.

The significance of the above-mentioned resistance components depends on the device voltage capability. Particularly, for very high voltage devices, the last component is the most important and the accumulated layer resistance could be neglected in a first approach. However, one of the main peculiarities of the VDMOS devices is its bidimensional nature, in the sense that current changes its direction along the accumulated surface under the gate electrode (3); the carrier flow comes out of the MOS channel horizontally changing to vertical at the drain contact, reason why this accumulated layer together with the rest of the epitaxial layer should be considered as distributed.

The change of current direction depends on the accumulated surface charge -and, therefore, on the oxide thickness between neighbouring cells- as well as on the doping level of the epitaxial layer. In the model we propose this change of current direction will be taken into account by means of a simple model twice one-dimensional, in terms of an access resistance which extends from the epilayer surface down to the p-well depth and characterized by surface resistance and bulk conductance differential elements.

The aim of this work is to show the influence of this distributed resistance on the $I_D(V_D)$ characteristics for VDMOS devices with different voltage-handling capabilities.

## 2. MODEL

We shall consider interdigitated VDMOS structures, a cross section is shown in figure 1 . As it is well known, current is pinched as it passes through neighbouring cells, this pinching depending on the device voltage-handling capability. The depletion layer width can be neglected for low voltage devices. On the other hand, the depletion layers between neighbouring cells strongly compress the current in high voltage devices. Accordingly, we shall differentiate the low case from that of high voltage.

## 2.1. LOW VOLTAGE DEVICE

According to what has been exposed above, we shall consider that the epitaxial resistance is made of a rectangular distributed access resistance up to the p-well depth and a trapezoidal component with a 45° angle for the current spreading in the semiconductor bulk (1). We assume that the base of the access resistance is at an equipotential, $V_1$, and that the current flows uniformly from it to the drain contact. Thus, the $I_D(V_D)$ characteristics can be obtained by considering the MOS transistor in series with this epitaxial resistance.

We have supposed the access resistance as formed by differential elements of surface resistance, dR, and of bulk conductance, dg, as it is shown in figure 2(a). The equations that govern the behaviour of this resistance are:

$$V_1 - V(x) = dI(x)/dg \qquad /1/$$

and

$$dV(x) = - I(x)\, dR \qquad /2/$$

where I(x) and V(x) are the current and voltage at the accumulated surface and the dR and dg elements are given by:

$$dR = \frac{dx}{Z\, \mu_A\, C_{OXA}\, (V_G - V_{FB} - V(x))} \qquad /3/$$

and

$$dg = \frac{Z\, dx}{\int h} \qquad /4/$$

2Z being the effective channel width, $\mu_A$ the accumulated layer mobility -supposed to be independent from x-, $C_{OXA}$ the capacitance per unit area of the oxide between neighbouring cells, $\int$ the epitaxial layer resistivity and h the p-well depth.

In previous $R_{ON}$ analysis (4, 5) the surface resistance elements, dR, were considered independent from x for a given gate voltage. We also assume this approximation neglecting the influence of the voltage drop along the accumulated surface on expression /3/, substituting V(x) by the voltage at the channel edge, $V_x$. Consequently, from equations /1/ and /2/, the access resistance is:

$$R_A = \frac{\int h\, A}{2\, Z\, th(AL/2)} \qquad /5/$$

where L is the cell spacing and A is given by:

$$A = \left(\int h\, \mu_A\, C_{oxA}\, (V_G - V_{FB} - V_x)\right)^{-1/2} \qquad /6/$$

The validity of this approximation can be justified comparing the former solution with the one obtained when V(x) is included in dR. Under this last condition, the following differential equation for the current distribution I(x) is deduced:

$$\frac{d^2I(x)}{dx^2} + B\,\frac{dI(x)}{dx} = C\, I(x) \qquad /7/$$

where B and C are given by:

$$B = \frac{(V_G - V_{FB} - V_1)\, Z}{\int h} \qquad /8/$$

and

$$C = \frac{Z}{\int^2 h^2\, \mu_A\, C_{oxA}} \qquad /9/$$

This differential equation for the surface current distribution must be numerically solved. Considering the adequate boundary conditions:

$$I = \begin{cases} -I_D/2 & \text{at } x = 0 \\ 0 & \text{at } x = L/2 \end{cases} \qquad /10/$$

the value of the equipotential $V_1$, which determines the access resistance, can be obtained. Discrepancies less than 1% are observed comparing the two calculated values of $R_A$.

## 2.2. HIGH VOLTAGE DEVICE

As already stated, current between neighbouring cells is compressed by their depletion layers. In this case, the epitaxial resistance includes an access resistance as previously, but of trapezoidal shape, a tube resistance

that accounts for the current pinching and a trapezoidal or trapezoidal/rectangular component (6, 7).

This last resistance component has been characterized in the same way as in the low voltage case. Besides, this resitance will be trapezoidal/rectangular or solely trapezoidal depending on the epitaxial thickness and on the p-well width.

The tube resistance is the most critical component, its length being established by assuming a zero lateral depletion layer of the cylindrical p-well/n-epilayer junction at the tube bottom (6). An effective curvature radius of this junction equal to 75% of the p-well depth has been considered to account for the two-dimensional effect of lateral diffusion.

Similarly to the previous case, the distributed access resistance has been also modelled by the surface resistance and the bulk conductance differential elements as it is shown in figure 2(b). As distinct from the low voltage case, the conductance differential elements are functions of the $\beta_\infty$ angle, which determines the current pinching in the epitaxial layer. Equations /1/ and /2/ again describe the access resistance behaviour but, aiming at an expression for the conductance differential elements, we shall impose the condition that the parallel association of all these conductance elements must express a $\beta_\infty$ angle trapezoidal resistance when neglecting the surface resistance elements.

Each dg element has a characteristic $\beta(x)$ angle and, by assuming a linear variation of tg $\beta(x)$ together with the boundary conditions:

$$\operatorname{tg}\beta(x) = \begin{cases} \operatorname{tg}\beta_\infty & \text{at } x = 0 \\ 0 & \text{at } x = L/2 \end{cases} \qquad /11/$$

we obtain

$$dg = \frac{2 Z \operatorname{tg}\beta_\infty \, dx}{\int^{L} \ln \dfrac{L}{L - 2h \operatorname{tg}\beta_\infty}} \qquad /12/$$

In this way, one yields to the same expression as in the low voltage case for the access resitance, where A is now given by:

$$A = \left[ \frac{2 \operatorname{tg} \beta_c}{\int_{L - 2 h \operatorname{tg} \beta_c}^{L} L \ln \frac{L}{L - 2 h \operatorname{tg} \beta_c} \mu_a C_{oxa} (V_G - V_{FB} - V_x)} \right]^{1/2} \quad /13/$$

Therefore, the access resistance is a function of the $\beta_c$ angle, $R_a(\beta_c)$, and the equipotential $V_1$ can be obtained taking into account the cylindrical shape of the p-well/n-epilayer junction:

$$V_1(\beta_c) - V_x = R_a(\beta_c)\ I_D \quad /14/$$

and the $I_D(V_D)$ characteristic is obtained considering the rest of the epitaxial resistance components.

## 3. RESULTS AND DISCUSSION

Applications fields of power MOS devices are expanding to higher frequencies ranges. In order to decrease the large Miller capacitance that causes a low cut-off frequency, devices with two different oxide thicknesses, such as the STGMOSFET (8), has been fabricated. This structure has a thin channel oxide and a thicker one on the epitaxial layer between cells. This last oxide layer reduces the surface charge induced by the gate voltage, resulting in an accumulated resistance increase.

Obviously, it is not possible to show the influence of the oxide thickness when the surface accumulated resistance is neglected. The obtained results for a high voltage VDMOS device are plotted on figure 3, in which the trapezoidal resitance has been considered as distributed, as well as neglecting the accumulated surface. The differencies between both sets of curves show the influence of the voltage drop accross the accumulated surface that accounts for a greater value of the equipotential $V_1$ that if one does not consider the accumulated surface, modulating the other epitaxial resistance components. The $I_D(V_D)$ characteristics for different oxide thicknesses between cells are also shown.

However, the influence of the oxide thickness between cells on the $I_D(V_D)$ characteristics is greater for lower voltage capability devices since the access resistance is less dependent on the induced surface charge as the epilayer doping increases and the resistance percentage corresponding to the access component also decreases. The

$I_D(V_D)$ characteristics of a low voltage VDMOS device, with different oxide thickness between cells, are shown in figure 4. Let us remark the strong dependence of the oxide thickness on the $I_D(V_D)$ characteristics for this device.

Moreover, surface current distributions are shown in figure 5. We can see that these distributions are rather uniform for high voltage devices but they are strongly dependent on the oxide thickness between cells for the low voltage ones.

We can conclude that a quasi-analythical model has been proposed to obtain the $I_D(V_D)$ characteristics for VDMOS devices, emphasizing the trapezoidal access resistance in high voltage devices, which permits to show the accumulated surface effect and, consequently, the influence of the oxide thickness between cells.

## REFERENCES


(1).- C. Hu, M. Chi and V. M. Patel. IEEE Trans. Electron. Dev., **ED-31**, 1693 (1984).

(2).- P. L. Hower and M. J. Geisler. IEEE Trans. Electron. Dev.,**ED-28**, 1098 (1981).

(3).- S. C. Sun and J. D. Plummer. IEEE Trans. Electron. Dev., **ED-27**, 356 (1980).

(4).- T. Phan Pham. Thèse de 3ème Cycle. Toulouse. France (1982).

(5).- K. Board, D. J. Byrne and M. S. Towers. IEEE Trans. Electron. Dev., **ED-31**, 75 (1984).

(6).- J. Rebollo, E. Figueras, J. Millán, E. Lora-Tamayo and F. Serra-Mestres. Solid State Electronics, **30**, 177 (1987).

(7).- J. L. Sanchez, M. Gharbi, H. Tranduc and P. Rossel. IEE Proc., **132**, 42 (1985).

(8).- D. Ueda, H. Takagi and G. Kano. IEEE Trans. Electron. Dev., **ED-31**, 416 (1984).

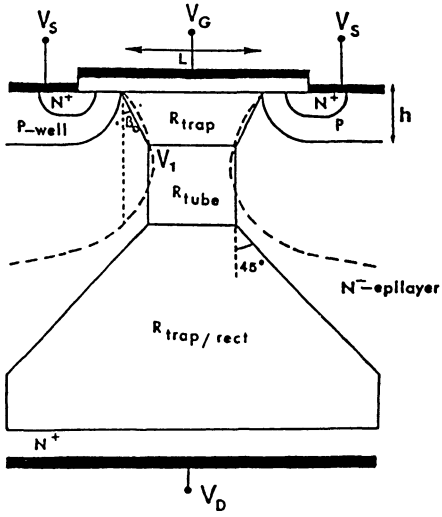



Fig. 1. Cross-section of the VDMOS structure.

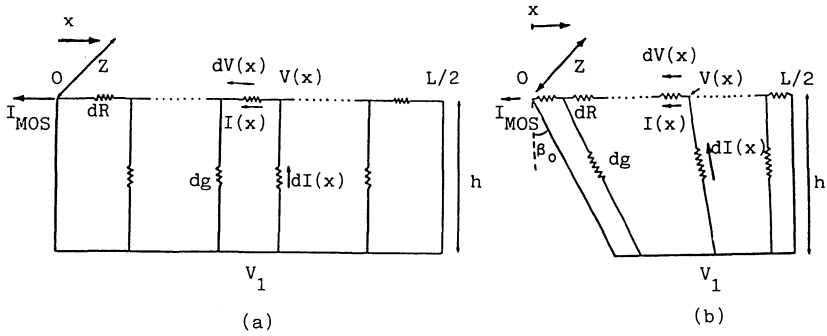



Fig. 2. Diagram of the distributed access resitance.
(a) Low voltage case. (b) High voltage case.

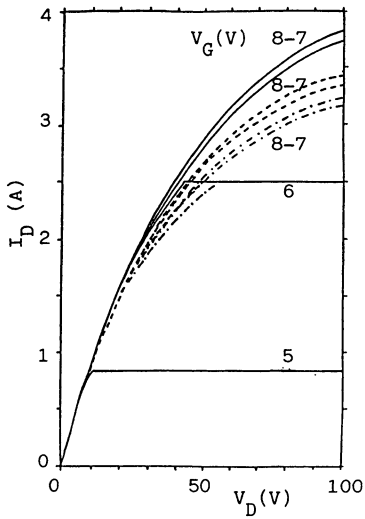



Fig. 3. I-V characteristics:
—— without accumulated resistance.
--- with trapezoidal access resistance ($d_{ox}$= 1800 Å).
-.- with $d_{ox}$= 9000 Å.
Parameters: $N_D$= $5.5*10^{13}$ $cm^{-3}$, h=5 μm, L=22.5 μm.,Channel length =1.5 μm., epitaxial thickness= 120 μm., Z=22.5 cm.

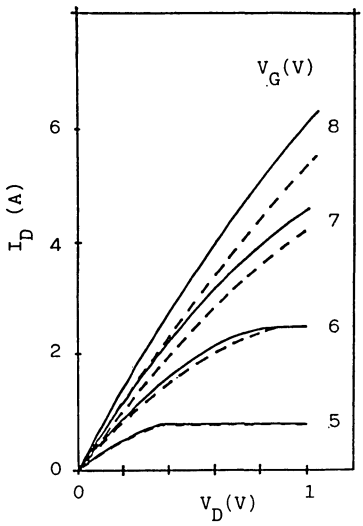
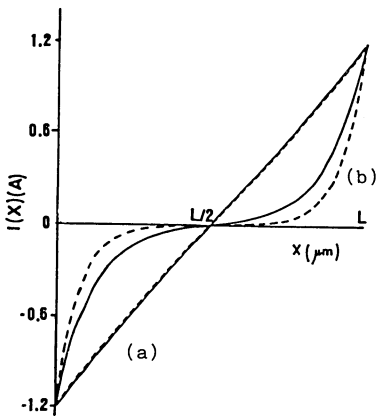



Fig. 4. I-V characteristics:
—— $d_{ox}$= 1800 Å.
--- $d_{ox}$= 9000 Å.
Parameters: $N_D$=$3.8*10^{15}$ $cm^{-3}$, epitaxial thickness=10 μm.

Fig. 5. Surface current distributions
(a) High voltage case.
(b) Low voltage case.
—— $d_{ox}$= 1800 Å.
--- $d_{ox}$= 9000 Å.



Proceedings of The Electrochemical Society, PV 1987-13, 166-173 (1987)
DOI: 10.1149/198713.0166PV © The Electrochemical Society

# AREA PARTITION OF HIGH-VOLTAGE DARLINGTON TRANSISTORS USING A GRAPHICAL SATURATION MODEL

**S A Smithies**

*National Electrical Engineering Research Institute*
*P O Box 395, Pretoria, South Africa*

## Abstract

A graphical model to quantify gain reduction in bipolar transistors due to both high-injection and quasi-saturation is described. The model was applied to the area partitioning of a high-voltage two-stage Darlington transistor to optimize the design in terms of the operating conditions and process limits. In maximizing high-current gain at low collector-emitter voltages, the effect of quasi-saturation was shown to necessitate the use of a small area ratio of six between the output and driver stages. The value of area ratio used also markedly affects the magnitude of the effect of quasi-saturation on gain, and it is shown that devices requiring an optimized linear operation region will have a much larger area ratio requirement than a device for which optimum high current saturation performance is required.

## Introduction

In the design of a high-voltage, medium-power two-stage Darlington transistor to be used in a dial buffer circuit in a loop disconnect telephone, it was essential that the active area be minimized in order to meet the cost target. As good saturation performance was essential in this application, for known worst-case operating conditions, it was necessary to model gain reduction in each of the two stages, resulting from both quasi-saturation and high-injection effects.

Kurata [1] has described a numerical modeling technique that includes two-region saturation effects, but this required considerable physical data for the transistor that was not readily available at the time. An approximation method similar to that proposed by Wheatley and Einthoven [2] for proportioning the areas in multi-stage Darlington transistors was desired. This approximation required five constants that could be measured directly from a transistor of known geometrical properties.

The technique described below makes use of a graphical saturation model, adapted from Smithies and Poole [3], and uses normal bipolar transistor modeling equations. It is a straight-line graphical approximation for the three regions in which the transistor operates, viz. saturation, quasi-saturation and Early-voltage control. It is simple to apply and requires only two parameters in addition to those normally used for D.C. modeling in the simulation program SPICE.

## The graphical saturation model

The three-region model is shown in Figure 1.

*Region 1.* - This is the true saturation region and the modified Ebers and Moll model [4] may be used to compute collector current here. For the purposes of the design of this Darlington transistor, great accuracy was not required in this region as both the driver and output stages would be operating in quasi-saturation at the given operating points. In order to minimize computing times a straight-line approximation for the saturation region was used and was found to be an acceptable approximation. In this case transistor conduction commences [5] at an applied collector-emitter voltage $V_{CE}$ of

$$V_{CE} = kT/q \times \ln(1/\alpha_R) \qquad (1)$$

where k is Boltzmann's constant, T is the absolute temperature, q is electronic charge and $\alpha_R$ is the inverse alpha of the transistor.

For the straight-line approximation, a linear increase in collector current with increasing collector-emitter voltage takes place from zero collector current. This continues up to the point of transition from region 1 (saturation) to region 2, quasi-saturation, and takes place at a collector-emitter voltage that may be approximated by :

$$V_{CE} = V_{CO} + R_S \times h_{FE1} \times I_B \qquad (2)$$

where $V_{CO}$ is a constant threshold voltage (typically 0.2 V), RS is the saturation resistance to approximate the effects of extrinsic resistance and $h_{FE1}$ is the transistor gain at the transition to region 2.

*Region 2.* - In this region the gain is reduced by quasi-saturation effects. Examples of charge distribution in this mode of operation are given by Kurata [6].

In his analysis of two-region saturation Hower [7] has shown that at the transition from region 1 to region 2

$$h_{FE2}/h_{FE1} - 1 = m \times I_C \qquad (3)$$

where, referring to Figure 1, $I_C$ is the collector current, $h_{FE1}$ is the current gain at the transition from saturation to quasi-saturation, $h_{FE2}$ is the current gain at the transition from quasi-saturation to normal transistor operation, and m is a device-specific constant.

Equation 1 may be rewritten as

$$h_{FE1}/h_{FE2} = 1/(1 + I_C/I_{QS}) \qquad (4)$$

where, for the purposes of this analysis, $I_{QS}$ is termed the quasi-saturation current and is the threshold current above which the variation of gain with collector-emitter voltage is governed primarily by quasi-saturation effects. $I_{QS}$ is measured at a collector-emitter voltage at the point of transition from saturation to quasi-saturation. In practice, due to the smooth rounded transition between saruration and quasi-saturation, a slightly higher value of collector-emitter voltage is used.

*Region 3.* - Here normal current-limiting transistor operation has been achieved, and the Early voltage concept may be applied to compute collector current as a function of collector-emitter voltage [8].

Transition from region 2 to region 3 occurs at a collector-emitter voltage

$$V_{CE} = R_C \times I_C$$

where $R_C$ is the passive-resistance of the collector region of the transistor, and, as seen in Figure 1, may be estimated from a family of collector current curves of a transistor, and $I_C$ is the collector current.

At high collector currents the gain also decreases, owing to emitter current crowding, and may be computed using the relationship [9]

$$h_{FE2}/h_{FE(pk)} = 1/(1 + I_C/I_K) \qquad (5)$$

where $I_C$ and $h_{FE2}$ are as above, and $h_{FE(pk)}$ represents the peak gain of the transistor in the normal operating region and is measured in conditions where saturation, quasi-saturation and high-injection effects are minimal. $I_K$ is known as the knee current and is the threshold current above which gain reduces owing to high injection effects.

An important difference from the practice in SPICE modeling is that the knee current $I_K$ is not measured at zero applied collector-base voltage as this would give a measure for the quasi-saturation current $I_{QS}$, but at an applied collector voltage greater than $R_C \times I_C$.

It may be of interest to note that in measurements on a number of power transistors, it has been found that a better approximation for gain reduction due to high-injection effects could be achieved by using an equation of the form

$$\ln(h_{FE2}) = D \times \ln(I_C) + C \qquad (6)$$

where D and C are device constants. The value of $h_{FE2}$ falls below $h_{FE(pk)}$ for values of collector current above the knee current $I_K$.

## Temperature effects

The effects of temperature on the parameters $R_C$, $h_{FE(pk)}$, $I_K$, and $I_{QS}$ were compensated for by using an exponential equation demonstrated by Martinelli et al. [10].

$$P_T = P_0 \times L \times \exp(-Ea/kT)$$

where $P_0$ is the value of the parameter $R_C$, etc. at room temperature, $P_T$ is the parameter value at the operating temperature T, L is a constant, k is Boltzmann's constant, and Ea is a characteristic activation energy for that particular parameter. Good agreement with measured values of the parameters was observed over the range 25 to 125 °C.

## Computer program

The flow diagram of the program to calculate the gain of a Darlington transistor using the graphical model is shown in Figure 2. Equations 1, 2, 4, and 5 (or 6) are used to calculate the collector current as a function of base current and collector-emitter voltage. The usual SPICE parameters of Early voltage, VA, knee current $I_K$ and peak gain $h_{FE(pk)}$, complemented by values of $R_C$ and $I_{QS}$, are used. A scaling factor N, relating the active areas of the output and driver stages, and termed the area ratio, is used to compute the values of $R_C$, $I_{QS}$ and $I_K$ for the driver stage.

## Results

*Darlington gain as a function of collector current.* - For the condition of fixed collector-emitter voltage ($V_{CE}$ = 3 V) the base current to the model was increased in steps and Darlington gain was computed as a function of collector current. The solid line in Figure 3 shows this characteristic for a Darlington transistor with VA = 1 000 V, $I_K$ = 0.3 A, $R_C$ = 100 , $I_{QS}$ = 60 mA, $h_{FE(pk)}$ = 60 and

$V_{CE}$ = 3 V. The area of the output stage was 0.6 $mm^2$, and the area of the driver stage 0.1 $mm^2$, i.e. an area ratio of N = 6. The regions of operation are: AB = both stages in region 3; BC = output stage in region 2; CD = driver in region 2; DE = output stage above $I_K$ and beyond E both stages are above their respective $I_K$ values.

To show the dependence of saturation performance on the area ratio N, the total area of the device was kept constant and resulted, when using values of N = 1 and N = 25 for the area ratio, in the broken curves in Figure 3. The inferences are that extended linear operation (both stages in region 3) may be obtained for large values of N and that the best saturation performance at high currents is obtained with low values of N.

*Gain integral as a function of area ratio.* - To assess the effect of the area ratio N on the saturation performance of a Darlington transistor, the area under the curves for each value of N in Figure 3 was used as a figure of merit and termed the gain integral (GI). The GI was computed as a function of area ratio N, with constant total Darlington area and a collector-emitter voltage of 3 V. Figure 4 shows that in the device described above the peak (normalized) GI occurs at N = 5 for $V_{CE}$ = 3 V.

*Area ratio as a function of collector-emitter voltage.* - Figure 5 shows the optimum value of N, computed as above, as a function of $V_{CE}$. It may be seen that low values of N will give better overall saturation performance for a given silicon area. As $V_{CE}$ is increased, the effects of quasi-saturation are reduced and larger values of N are acceptable.

## Conclusion

The graphical saturation model has been shown to be a useful and convenient tool in optimizing the area partition of a two-stage Darlington transistor for low-frequency applications. Other variations in the application of the model have included the calculation of the optimum value of area ratio N at a fixed collector-emitter voltage as a function of gain $h_{FE(pk)}$.

In the application of the model to A.C. circuit analysis, the sharp transition between regions 1 and 2 as well as regions 2 and 3 can give rise to high-order harmonics. Numerical smoothing has been used to minimize the effect. A distributed equivalent circuit [3] has similarly been used to smooth the transition between regions, and SPICE analysis of this equivalent circuit has enabled high-frequency effects to be approximated.

## References


1. M Kurata, "Numerical Analysis for Semiconductor Devices," pp. 75-112, Lexington Books, Lexington MA (1982).

2. C F Wheatley and Willem G Einthoven, "On the proportioning of chip area for multistage Darlington power transistors," IEEE Trans. Electron Devices, ED-23, no. 8, pp. 870-878 (1976).

3. S A Smithies and K F Poole, "A graphical model for two-region saturation in bipolar transistors and its implementation in the modeling program SPICE," IEEE j Solid State Circuits, to be published (April 1987).

4. I E Getreu, "Modeling the bipolar transistor," p. 27 and pp. 144-145, Elsevier Scientific Publishing Co., New York (1978).

5. Ibid. p. 22.

6. M Kurata, "Numerical Analysis for Semiconductor Devices." p. 104, Lexington Books, Lexington MA (1982).

7. P L Hower, "Application of charge-control model to high-voltage power transistors," IEEE Trans. Electron Devices, Vol. ED-23, p. 866, Equation 11 (1976).

8. I E Getreu, "Modeling the bipolar transistor," p. 45, Elsevier Scientific Publishing Co., New York (1978).

9. Ibid. p. 119, equation 2.193.

10. R U Martinelli, C F Wheatley, and K A Sassaman, "A study of forward second-breakdown in silicon transistors using the unit cell concept," Section 18.7, pp. 504-507, International Electron Devices Meeting, Digest of Technical Papers, San Francisco (1982).

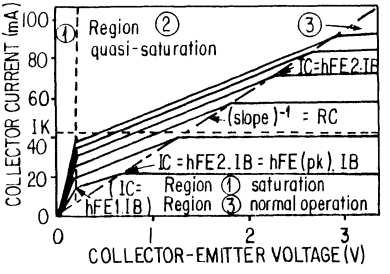



*Figure 1.* A linear graphical approximation for two-region saturation, showing three regions of operation of the transistor. Region 1 represents true saturation, region 2 represents quasi-saturation, and region 3, normal operation with Early-voltage control.

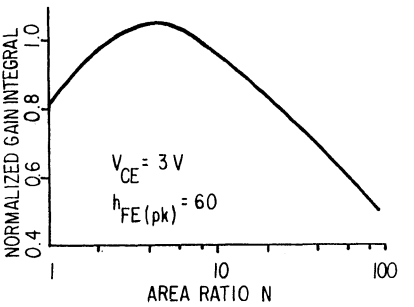



*Figure 4.* The gain integral of a Darlington as a function of area ratio N with collector-emitter voltage $V_{CE}$ = 3 V and peak gain $h_{FE(pk)}$ = 60. The optimum value of area ratio N is approximately 6 for $V_{CE}$ = 3 V.

*Figure 2* may be found on the next page.

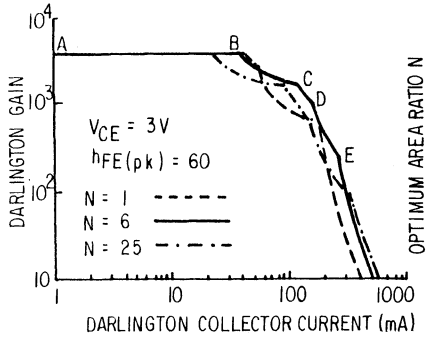



*Figure 3.* Darlington transistor gain as a function of collector current at $V_{CE}$ = 3 V for area ratios of 1, 6 and 25.

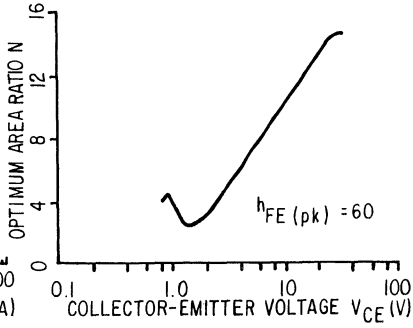



*Figure 5.* The optimum value of area ratio is shown as as a function of collector-emitter voltage for $h_{FE(pk)}$ = 60.

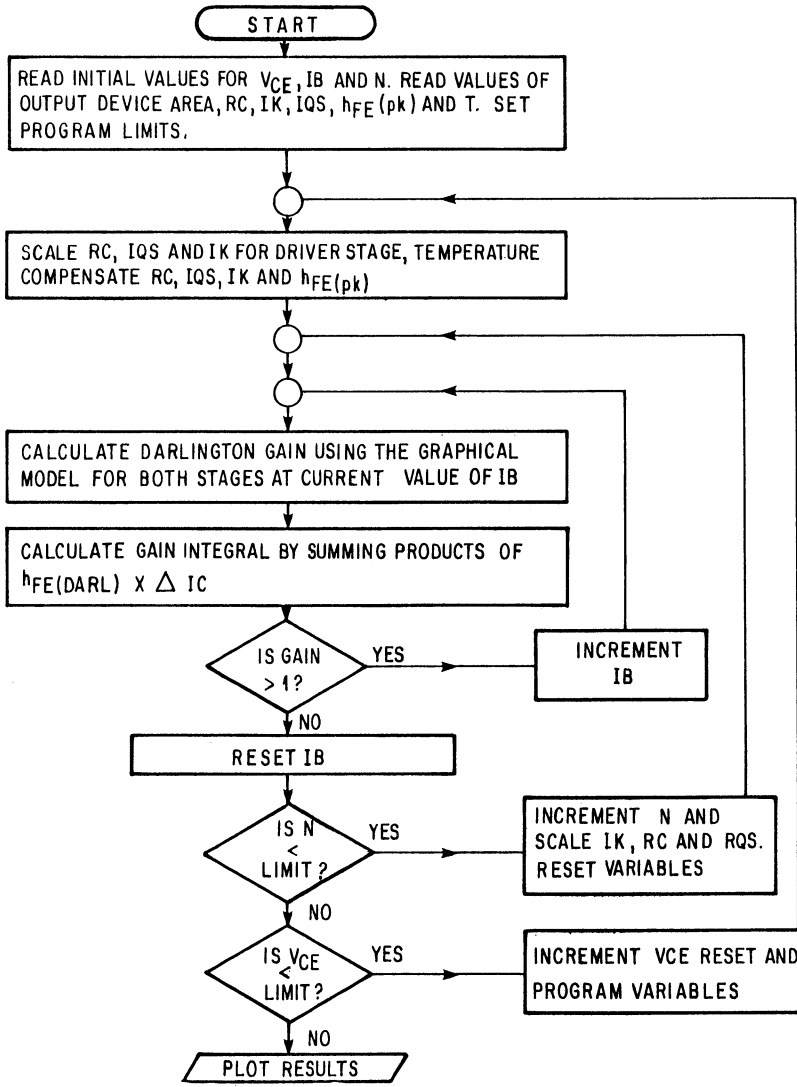



*Figure 2.* The flow diagram of the program to compute Darlington transistor characteristics using the graphical model in Figure 1.

Proceedings of The Electrochemical Society, PV 1987-13, 174-186 (1987)
DOI: 10.1149/198713.0174PV © The Electrochemical Society

# A NOVEL GATE STRUCTURE TO SET THE TURN-ON CURRENT OF A FOLDBACK DIODE

P Schieke

National Electrical Engineering Research Institute
P O Box 395, Pretoria 0001, Republic of South Africa.

## ABSTRACT

The turn-on current characteristics of a foldback diode were investigated using a number of different test structures which included special external gate structures with various densities. The variation of the turn-on current associated with these geometrical changes was investigated. A novel gate structure to control the turn-on current was also evaluated. With this gate structure it was possible to control the turn-on current precisely. The turn-on current was simulated using a circuit extraction program which provided a facility for the inclusion of process parameter variations.

## INTRODUCTION

The foldback diode (FBD) is a two-terminal device developed, in this instance, for use as secondary surge protection in a telephone application. The basic protection circuit which will be used in dual-tone multi-frequency (DTMF) signalling telephones, is shown in Figure 1. Primary protection is afforded by a 350 V, 10 kA gas-arrester. The FBD is then used to arrest surges of lower than 350 V.

## DESCRIPTION OF THE FOLDBACK DIODE

The characteristics of the foldback diode are shown in Figure 2, important parameters being the zener voltage, the turn-on current and voltage, the holding current and the saturation voltage at a given current. The subject of this investigation is the setting of the turn-on current because of its particular importance in this application.

The equivalent circuit for the FBD is shown in Figure 3. The value of the zener diode connected between the anode and the gate of the FBD determines the zener voltage of the FBD. The value of the resistor situated between the gate and the cathode of the thyristor, R(gc), determines the turn-on current of the FBD.

The value of this resistor R(gc), and thus the turn-on current, is determined by the geometries of both the cathode-short structure [1-6] and the proposed gate structure. The cathode-short structure on the other hand, determines the holding current and the rise-time immunity of the FBD. [1,2,4,6]

## TURN-ON CURRENT DETERMINATION

Turn-on current of the FBD is normally only a function of the geometry of the cathode-short structure [6]. In order to assess the influence of geometrical factors on the turn-on current, different cathode-short structures were designed and fabricated. The different structures that were used for these measurements, are shown in Figure 4. The distance x is the distance between the edge of the cathode and the first cathode-shorts, as is shown in Figure 5.

The results of the turn-on current measurements as a function of the distance x, are recorded in Table 1. The results are also presented as a graph in Figure 6.

TABLE 1

THE TURN-ON CURRENT OF CATHODE-SHORT STRUCTURES AS A FUNCTION OF THE DISTANCE x.

| DEVICE | DISTANCE x (um) | Ito (mA) |
|---|---|---|
| CS1 | 4 | 273 |
| CS2 | 35 | 91 |
| CS3 | 42 | 63 |
| CS4 | 42 | 71 |
| CS5 | 47 | 66 |
| CS6 | 84 | 52 |

It was found that a variation in the density of the cathode-shorts, had only a very small influence on the turn-on current, as can be seen from the measurements of the turn-on current of CS3 (low density cathode-shorts) and CS4 (higher density cathode-shorts). The turn-on current for the cathode-short structure with the higher density of cathode-shorts was only 11% higher than for the structure with a low density of cathode shorts.

As far as the cathode-short structure is concerned, the main

determinant of the turn-on current is thus the distance x.

In order to determine the turn-on current accurately as well as to set it at a high enough level, an additional gate structure was included around the cathode-short structure, in the basic FBD architecture.

The layouts of the test structures which were used for determining the effect of the gate structure on the turn-on current may be seen in Figure 7. In the center of these test structures the cathode-short structures are visible, whilst the gate structures are situated around the cathodes. Three different gate structures were evaluated. These were a high density, a medium density and a low density gate structure.

The gate structure acts as a resistor R(gs) between the gate and the cathode and is connected in parallel with the gate-cathode resistor R(gcs) provided by the cathode-short structure. The combination of these two resistances then forms the equivalent gate-cathode resistance R(gc) of the FBD.

$$R(gc) = [1/R(gs) + 1/R(gcs)]^{-1} \quad (1)$$

The turn-on current is then approximately:

$$I(\text{turn-on}) = 0{,}65 \; / \; R(gc) \quad (2)$$

## RESULTS

The measured values of the turn-on current of these test structures are listed in Tables 2 and 3. (CS = Cathode-short structure, GS = Gate structure)

TABLE 2

THE TURN-ON CURRENT OF ONE TYPE OF CATHODE-SHORT STRUCTURE WITH THREE DIFFERENT SURROUNDING GATE STRUCTURES

| DEVICE | CATHODE-SHORT | GATE STRUCTURE | Ito (mA) |
|---|---|---|---|
| GS1 | CS4 | High density | 582 |
| GS2 | CS4 | Medium density | 119 |
| GS3 | CS4 | Low density | 64 |

TABLE 3

THE TURN-ON CURRENT OF FIVE TYPES OF CATHODE-SHORT STRUCTURES WITH ONE SURROUNDING GATE STRUCTURE TYPE

| DEVICE | CATHODE-SHORT | GATE STRUCTURE | Ito (mA) |
|---|---|---|---|
| GS1 | CS4 | High density | 582 |
| GS4 | CS1 | High density | 712 |
| GS5 | CS5 | High density | 588 |
| GS6 | CS3 | High density | 581 |
| GS7 | CS6 | High density | 570 |

The following conclusions can now be formulated from these measurements:

1. With the inclusion of the gate structure, the turn-on current was, as expected, higher than in the case where only the cathode-short structure was used. The turn-on current was varied by changing the geometry of the gate structure.

2. Both the gate structure and the cathode-short structure plays a role in determining the turn-on current.

3. The higher the density of the gate structure, the bigger role it plays in determining the turn-on current of the structure.

The addition of the gate structure thus made it possible to adjust the turn-on current of the FBD precisely, with little effect on the holding current.

## SIMULATION

In order to simulate the turn-on current of the different structures, a circuit extraction program [7] was used to extract the value of the resistance R(gc) from the layouts of these structures.

This program was designed to extract all the circuit information from a computer layout of a bipolar integrated circuit. The inputs to the program are the layout and process specification files. The outputs of the program are a circuit diagram, a netlist for SPICE and an error report.

The name of the circuit extraction program is NEXT1. It has been written in VAX FORTRAN for VAX computers. A VT100 type terminal is used for interaction with the computer.

In NEXT1 two libraries with subroutines are used, one called EXTRACT, with routines directly relevant to the circuit extraction process, and the other called CADUTIL, with routines of a more general nature.

NEXT1 works in conjunction with the GAELIC suite of layout programs as well as with the SPICE circuit simulator.

An overview of the general program flow follows:

1. After the layout and process parameters have been specified, the first step is to reconstruct the circuit. During this phase, the layout is examined, components and connections are recognized and errors are recorded. Outputs available after this step are: an error report, a SPICE netlist and a circuit diagram, the latter two without component values. The outputs can be examined and the designer can, at this stage, make decisions on the correctness of the layout. Any errors on the layout should be corrected and reconstruction of the circuit must be repeated before continuing.

2. The second step is to extract the parameters. During this phase, every component recognized previously, will be examined and the relevant values calculated. Outputs available after this step are: an updated error report, a circuit diagram and a SPICE netlist. The component values are now included in both. Once again, the outputs can be examined for any errors. If any resulting changes are made on the layout, the whole procedure should be repeated, starting again with circuit reconstruction.

The resistance R(gc) was determined by the program and thus the turn-on current of a specific structure could be calculated. The extracted values of R(gc), the measured values of the turn-on current, as well as the calculated values of the turn-on current are shown in Table 4. The turn-on current was calculated using equation (2).

TABLE 4

A COMPARISON BETWEEN THE CALCULATED AND THE MEASURED VALUES OF TURN-ON CURRENT.

| DEVICE | R(gc) (ohm) | Ito (mA) (calculated) | Ito (mA) (measured) | Difference (%) |
|---|---|---|---|---|
| CS1 | 2,22 | 293 | 273 | 7,5 |
| CS2 | 6,73 | 97 | 91 | 6,1 |
| CS3 | 9,84 | 66 | 63 | 4,9 |
| CS4 | 9,28 | 70 | 71 | 1,4 |
| CS5 | 9,82 | 66 | 66 | 0 |
| CS6 | 12,60 | 52 | 51 | 1,9 |
| Of interest: | | | | |
| GS1 | 1,09 | 596 | 582 | 2,4 |
| GS2 | 5,12 | 128 | 119 | 7,9 |
| GS3 | 10,40 | 62 | 64 | 2,7 |
| GS4 | 0,99 | 657 | 712 | 8,4 |
| GS5 | 1,09 | 596 | 588 | 1,3 |
| GS6 | 1,09 | 596 | 581 | 2,6 |
| GS7 | 1,10 | 591 | 570 | 3,6 |

It is thus shown that the calculated values of the turn-on current corresponds with the measured values to within $\pm$ 10%, which is of the same magnitude as the spread in pinch resistance for the structures.

## CONCLUSION

By using the proposed gate structure, the turn-on current of the FBD can be set to a specified value which is higher than, but largely independent of the value of the holding current, when only a cathode-short structure is used.

By using the circuit extraction program, the turn-on current can be accurately simulated from the layout of the device. Considerable savings in both time and cost are realized when compared to the iteration process of design and production in order to optimize the desired turn-on current.

## REFERENCES


1. *Aldrich R W, Holonyak N, "Two-terminal Asymmetrical and Symmetrical Silicon Negative Resistance Switches," Journal of Applied Physics, Vol. 30, No. 11, November 1959, pp. 1819-1824.*

2. *Gentry F E et al, "Bidirectional Triode P-N-P-N Switches," Proceedings of the IEEE, April 1965, pp. 355-369.*

3. *Chu C K, "Geometry of Thyristor Cathode Shunts," IEEE Transactions on Electron Devices, Vol. ED-17, No. 9, September 1970, pp. 687-690.*

4. *Raderecht P S, "A Review of the 'shorted emitter' Principle as Applied to p-n-p-n Silicon Controlled Rectifiers," International Journal of Electronics, Vol. 31, No. 6, 1971, pp. 541-564.*

5. *Hartman K, "Improvement of Thyristor Turn-on by Calculation of the Gate-Cathode Characteristic before Injection," IEEE Transactions on Electron Devices, Vol. ED-23, No. 8, August 1976, pp. 912-917.*

6. *Munoz-Yague A, Leturq P, "Optimum Design of Thyristor Gate-Emitter Geometry," IEEE Transactions on Electron Devices, Vol. ED-23, No. 8, August 1976, pp. 917-924.*

7. *Kemp A J, "NEXT1 - A Rudimentary Program for the Extraction of the Equivalent Circuit from Mask Layout Data," NEERI Internal Report, I ELEK 264, November 1986.*

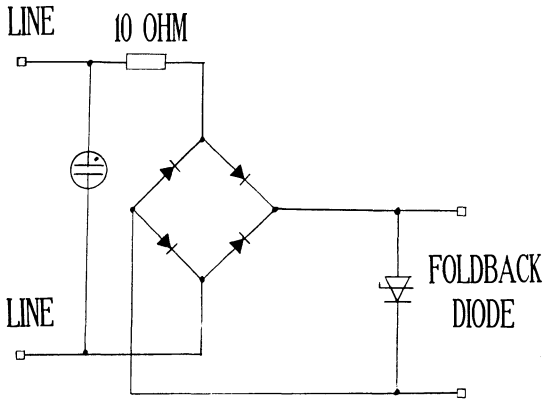



FIGURE 1 *The basic protection circuit used in DTMF telephones.*

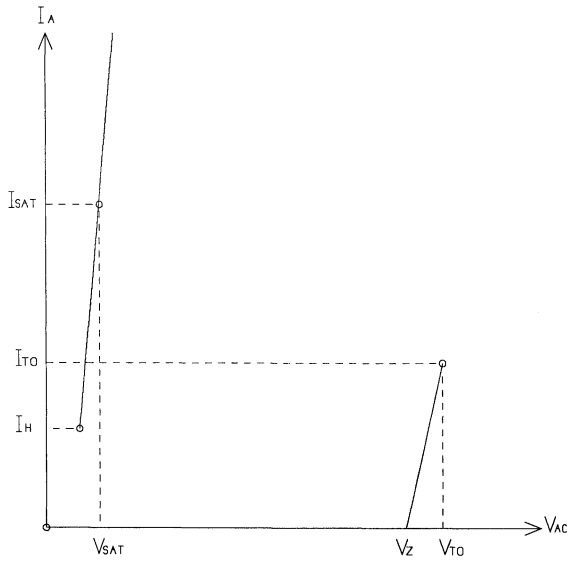



FIGURE 2 *Characteristics of the foldback diode.*

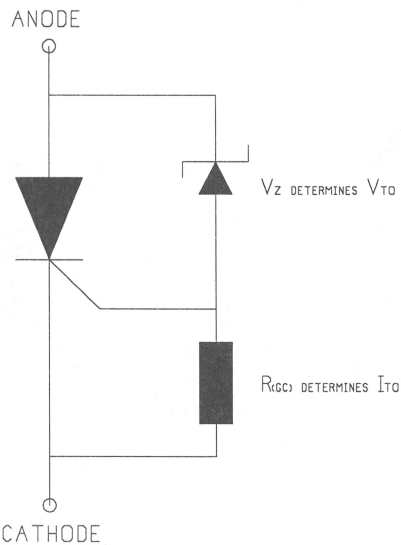



**FIGURE 3** *Equivalent circuit for the foldback diode.*

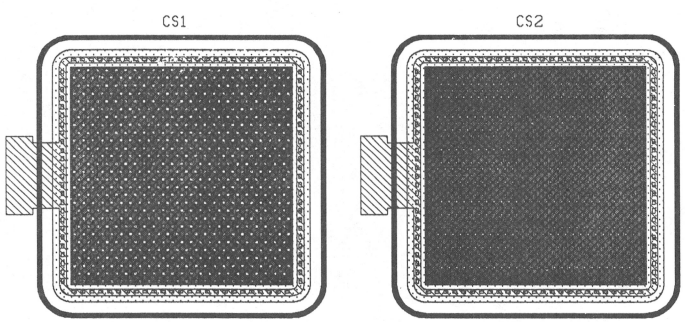



**FIGURE 4** *The layouts of different cathode-short stuctures used for measurements of turn-on current.*

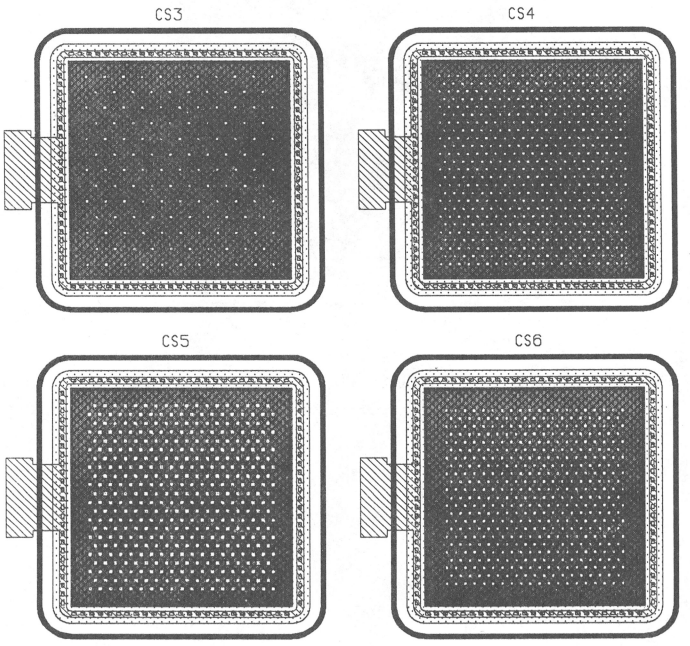



FIGURE 4 (Continued) *The layouts of different cathode-short stuctures used for measurements of turn-on current.*

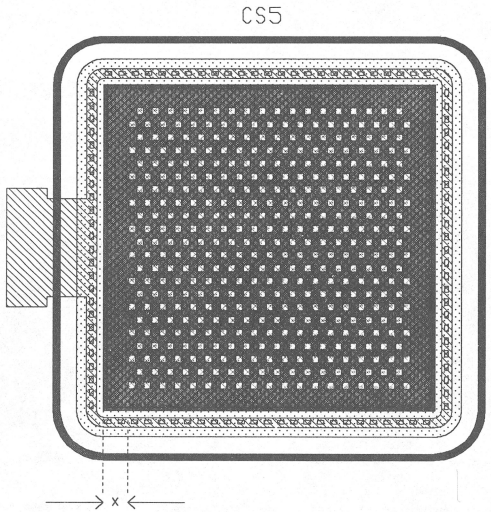



**FIGURE 5** *One of the cathode-short test structures with the distance x indicated between the edge of the cathode and the first cathode-shorts.*

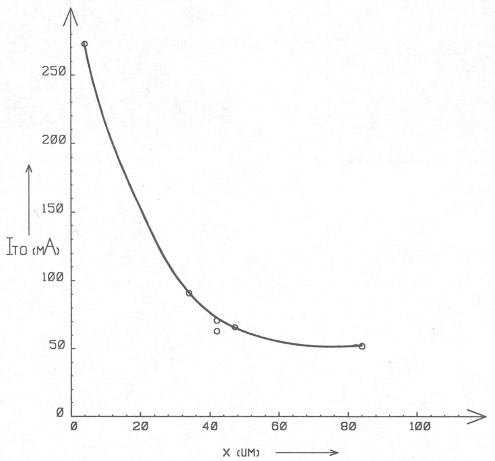



**FIGURE 6** *A graph of the turn-on current of the cathode-short test structures as a function of the distance x.*

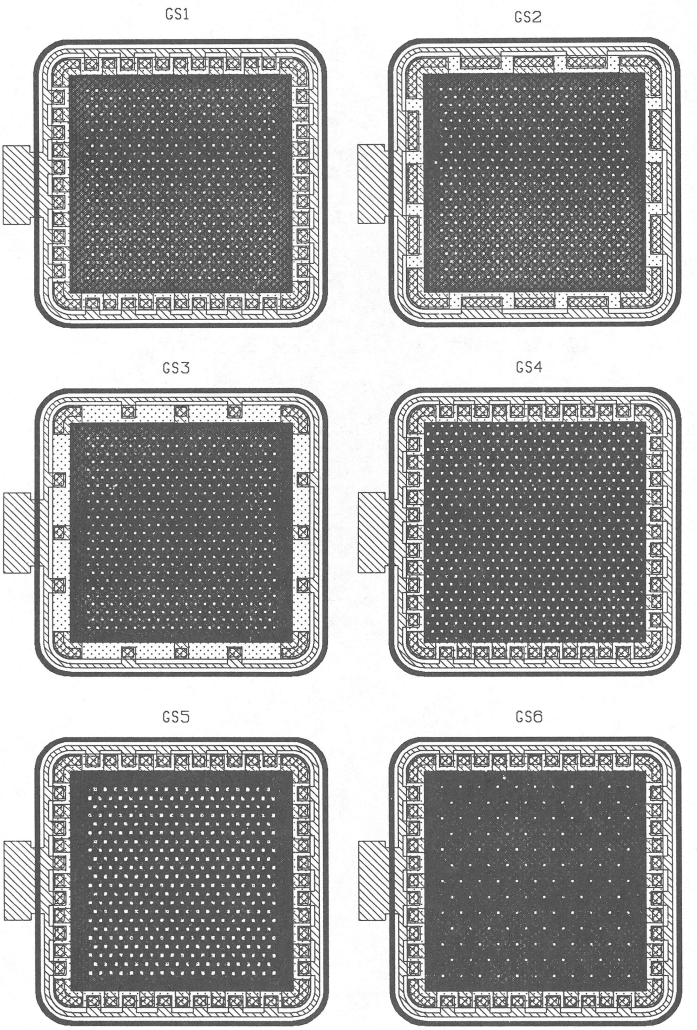



**FIGURE 7** *The layouts of different test stuctures used for determining the effect of the gate structure on the turn-on current. Different gate and cathode-short structures were used.*

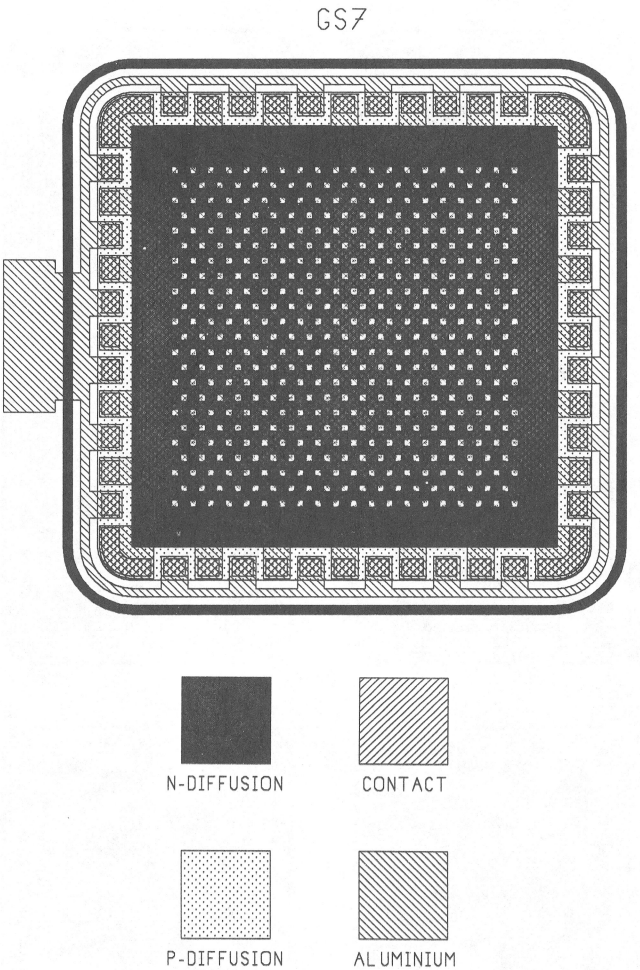



**FIGURE 7** (Continued) *The layouts of different test stuctures used for determining the effect of the gate structure on the turn-on current. Different gate and cathode-short structures were used.*

Proceedings of The Electrochemical Society, PV 1987-13, 187-193 (1987)
DOI: 10.1149/198713.0187PV © The Electrochemical Society

# ANOMALOUS REDUCTION IN BLOCKING CAPABILITY IN HIGH VOLTAGE TRANSISTORS DUE TO SELENIUM CONTAMINATION

G. M. Dolny, R. U. Martinelli, L. A. Goodman,
P. H. Robinson, C. W. Magee, L. R. Hewitt, E. M. Botnick

David Sarnoff Research Center
Princeton, N. J. 08540-0432

E. Teno, D. Burton

RCA Solid State Division
Mountaintop, Pa. 18707-2819

## ABSTRACT

An anomalous contamination mechanism in high-voltage silicon devices is presented. Down conversion of epitaxial layer resistivity and the associated reduction in device reverse blocking capability were observed under various process conditions. Capacitance spectroscopy, Rutherford Backscattering Spectrometry (RBS), electrical spreading resistance and voltage breakdown measurements were used to characterize the contaminating species. This analysis showed that the problem was caused by trace levels of selenium introduced during a wafer cleaning step.

## INTRODUCTION

A variety of failure mechanisms associated with the reverse blocking capability of high voltage devices has been reported in the literature. These include junction walkout due to electron trapping in the oxide (1), interface trap density increases due to the breakage of bonds near an avalanching junction (2), and reduction of epitaxial resistivity due to activation of oxygen thermal donors (3). Recently we have observed a new failure mechanism attributable to selenium contamination during a wafer cleaning step which led to decreased resistivity and thus reduced blocking capability of lightly doped N-type epitaxial layers. This paper describes the nature of the contamination, its physical and electrical characterisitics and the experimental methodology employed in its identifiction and elimination.

## DEVICE STRUCTURE

The transistors investigated in this study were double-diffused, epitaxial collector, N-P-N bipolar power transistors. The p-type boron bases were formed by ion implantation followed by diffusion while the

phosphorus emitters were diffused using standard process techniques. Fig. 1 shows typical impurity profiles for a device used in this study as derived from two point spreading resistance measurements. The emitter-base junction is 6μm deep and the collector-base junction is 10.3μm deep resulting in a base width of 4.3μm.

The epitaxial layer specifications are shown in Fig. 2. The region adjacent to the collector-base junction is the most lightly doped and supports the largest percentage of the collector-base reverse bias voltage. This region essentially determines the breakdown voltage. The regions adjacent to the $N^+$ substrate form a more heavily doped buffer layer. This buffer layer significantly improves the device's immunity to second breakdown but supports only a small fraction of the reverse bias voltage.

## PROBLEM DESCRIPTION

An anomalous failure mechanism was observed during the manufacture of bipolar power transistors with the physical structure described above. Device types designed for collector-base breakdown voltage ($BV_{cbo}$) at 1mA in the 900-1200 volt range exhibited low yields at wafer probe due to reduced blocking voltages. The failures were limited to devices with high resistivity (>40Ω-cm) N-type epitaxial material. Typically the failed devices exhibited $BV_{cbo}$ in the range of 500-700 volts. The yield problem was manifest as a 100% failure of apparently random lots and could not be correlated to a particular piece of process equipment.

## ELECTRICAL CHARACTERISTICS

Fig. 3 compares the collector-base reverse characteristics of normal and failed devices. The normal device (Fig. 3A) exhibits $BV_{cbo}$ of 1040 volts which is reduced to 590 volts (Fig. 3B) for the failed unit. In both cases the pre-breakdown collector-base leakage current is in the submicroampere range. These low leakage currents and sharp breakdown characteristics indicate that the $BV_{cbo}$ failures are not attributable to excess leakage current originating from heavy metal contamination and that the junctions are undergoing avalanche breakdown at an anomalously low voltage.

A possible explanation of these observations is an increase in base dopant concentration or a decrease in junction penetration originating from improper diffusion or ion implanation processing. This possibility was eliminated when sheet resistance measurements, junction penetration measurements, and spreading resistance profiles showed no observable differences in the base profiles between normal and failed devices.

A second possible explanation for the reduction in blocking capability is a decrease in the epitaxial layer resistivity from the specified value. Fig. 4 presents a two point spreading resistance profile of a typical epitaxial wafer used in this study prior to any high temperature processing steps. The measured resistivity and thickness of

the collector region are 47Ω-cm. and 50μm respectively. This combination results in a calculated breakdown voltage well in excess of 1000 volts. Comparison with Fig. 2 shows the epi structure is within the desired specification.

Fig. 5 shows the spreading resistance profile of a wafer from the same epi run as the one of Fig. 4 after base implant and diffusion. The base was formed using a 100 KeV, 5E14 atom/$cm^2$ boron implant followed by a 6 hour 1200° C diffusion. This diffusion was the initial high temperature processing step. The spreading resistance plot clearly shows a reduction in epi layer resistivity from the initial 47Ω-cm to approximately 15Ω-cm after the base diffusion. This resistivity decrease is responsible for the reduced breakdown voltage.

Thermal activation of oxygen donor states (3-5) is known to cause decreases in the resistivity of lightly doped epitaxial layers. This was investigated as a potential explanation for the observed reduction in the breakdown voltage by means of secondary ion mass spectroscopy (SIMS), infrared spectroscopy, and transmission electron microscope comparisons between normal and failed devices. These comparisons showed no difference in the oxygen content between the normal and failed samples. Additionally, the problem was independent of the reactor used to grow the epi layer as well as the substrate vendor. Finally, raw epi wafers that were subjected to only the base thermal cycle with no intermediate processing steps failed to show the resistivity down conversion. On this basis oxygen thermal donors were eliminated as a possible source of the problem.

A series of split-lot experiments was performed to investigate the possibility of wafer contamination during the prediffusion processing. Through these experiments it was determined that the reduction in the epitaxial layer resistivity was caused by a fast diffusing N-type dopant which was introduced during a wafer cleaning step, possibly through the degradation of rubber o-ring materials used in a wet chemical cleaning station. From electrical resistivity measurements the concentration of the contaminant after diffusion was computed to be in the range of $10^{14}$ atoms/$cm^3$ which is below the detection limits of available bulk analytic techniques.

In order to identify the contaminating specie Rutherford Backscattering Spectrometry (RBS) was utilized on wafers processed through the suspect cleaning step in order to concentrate the contaminant on the wafer surface. Prior to subsequent diffusions the wafer surfaces were analyzed using RBS. The RBS spectrum of Fig. 6 clearly shows the presence of selenium on the surface of the contaminated samples. Integration of the area under the Se peak shows an areal density of 1.9E13 Se atoms/$cm^2$ (approximately 1/100 of a monolayer). For the uncontaminated samples no Se was found to a detection limit of 5E11 $cm^{-2}$. Further analysis showed a correlation between areal density of Se detected and resistivity reduction of the epi layers.

Based on this information a series of experiments was performed to determine the electrical characteristics of selenium doped silicon.

N-type silicon wafers with the epitaxial structure shown in Fig. 2 were ion implanted with Se at doses ranging from 1E12 to 1E14 $cm^{-2}$. Isochronal diffusions followed by spreading resistance measurements were used to determine the diffusion coefficient of Se in Si as a function of temperature. These data are plotted in Fig. 7 along with the diffusion coefficients of other known fast diffusers in silicon. From these data it is clear that Se diffuses fast enough to penetrate a 50μm epi layer during the 6 hour 1200° base diffusion as shown in Fig. 5. In addition, these data were compared to diffusion coefficient measurements made on the chemically contaminated samples, and there was excellent agreement between the two measurements.

Fig. 8 shows the deep level energy spectrum of the Se doped Si. The peaks in the spectrum correspond to three levels in the upper half of the bandgap: $E_c$ -0.21 eV, $E_c$ -0.34 eV, $E_c$ -0.56 eV. The levels of $E_c$ -0.34 eV and $E_c$ -0.56 eV have been associated with substitutional sites, while the $E_c$ -0.19 eV level is associated with a $Se_2$ molecule (6) or interactions between Se and a shallow acceptor (7).

## CONCLUSIONS

Selenium contamination has been identified with a failure mechanism in power semiconductor devices. Selenium has been shown to be a fast diffusing N-type dopant capable of lowering the resistivity and hence the breakdown voltage of thick, lightly doped epitaxial layers used in high voltage transistor designs. A possible source of the Se contamination is the degradation of rubber O-ring materials used in wet chemical cleaning stations.

## REFERENCES


1.) J. F. Schenck, Proc. 6th Annual Reliability Physics Symposium, pp. 31-39 (1967)
2.) J. F. Verwey, Solid State Electronics, 14, 775 (1971)
3.) O. Heimrich and E. Sirtl, Semiconductor Silicon, 626-636 (1977)
4.) P. Rava, H. C. Gatos, and J. Lagowski, Semiconductor Silicon, pp. 232 (1981)
5.) A. Komamori,App. Phys. Lett., vol. 34, pp. 287-291 (1979)
6.) E. Astrova, I. Bol'Shakov, A. Lebeder, and O. Mikhno, Sov. Phys. Semiconductors, 19, 371-373 (1985)
7.) H. G. Grimmies, E. Jonzin, B. Skarstam, J. Appl. Phys., 51, 3740 (1980)

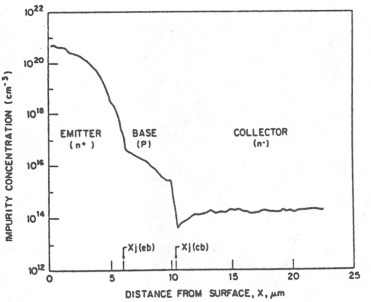



Fig. 1 Two Point Spreading Resistance Plot of Diffused Profiles

EPI STRUCTURE N-/N/N+

| LAYER | MICRONS | OHM-CM | CONDUCTIVITY |
|---|---|---|---|
| T1 | 8.0 – 13.0 | 2.0 – 4.0 | N |
| T2 | 20.0 – 25.0 | 8.0 – 15.0 | N |
| T3 | 45.0 – 65.0 | 45.0 – 65.0 | N |

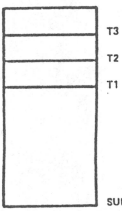



Fig. 2 Epitaxial Layer Specifications

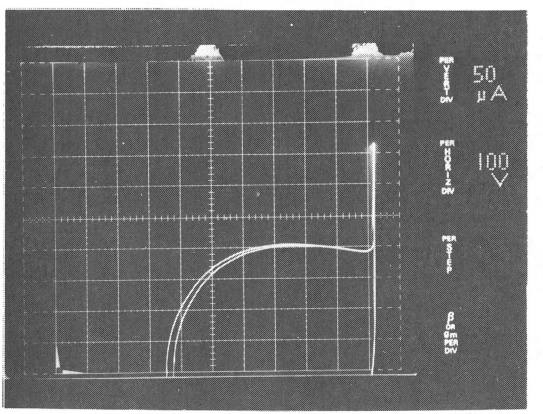



Fig. 3A Normal Device Collector-Base Reverse Characteristics

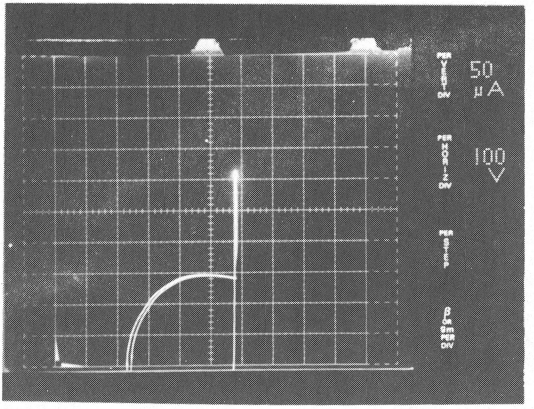



Fig. 3b Failed Device Collector-Base Reverse Characteristics

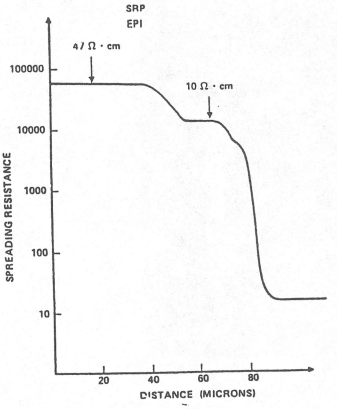



Fig. 4 Spreading Resistance Profile Post Epi Deposition

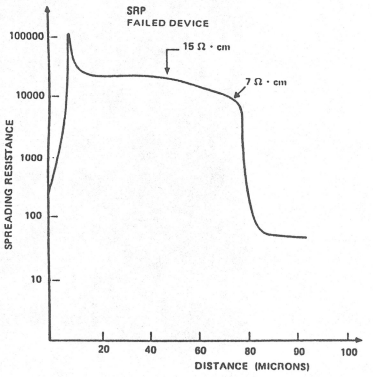



Fig. 5 Spreading Resistance Profile Post Base Diffusion

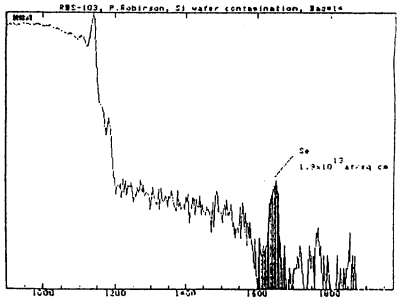



Fig. 6 RBS Spectrum of Contaminated Wafer

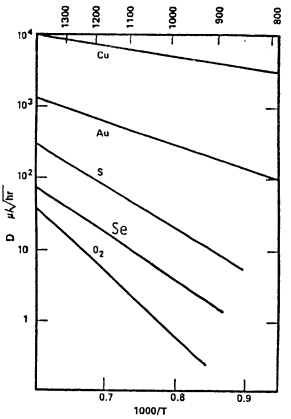



Fig. 7 Diffusion Coefficients of Fast Diffusers in Silicon

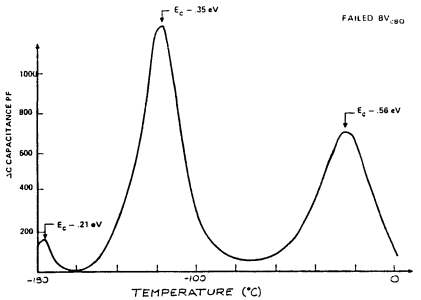



Fig. 8 DLTS Spectrum of Se in Si

Proceedings of The Electrochemical Society, PV 1987-13, 194-205 (1987)
DOI: 10.1149/198713.0194PV © The Electrochemical Society

# THE EFFECT OF PLATINUM DIFFUSION AND ANNEALING ON THE BREAKDOWN VOLTAGE AND LIFETIMES OF BORON AND ALUMINUM DOPED HIGH VOLTAGE DIODES

A.V. Hayes, *M. Livschultz, and *T.J. Knowles

Unisys Defense Systems
M.S./EV Great Neck, N.Y. 11020

*Zenith Electronics Corp.
1000 Milwaukee Ave.
Glenview, IL 60025

The effects of Pt doping and post-Pt annealing on the Breakdown Voltages (BVs) and Reverse Recovery Times (Trrs) of High Voltage diodes were studied for a range of initial n-type base resistivities and diffusion conditions. Relative concentrations of Pt acceptors ($N_A(Pt)$) and shallow donors ($N_D$) were varied from $N_D >> N_A(Pt)$ to $N_A(Pt) > N_D$. For $N_D >> N_A(Pt)$ recovery times of Pt-doped diodes are well known to be inversely related to Pt diffusion temperatures. Failure of this relationship was noted at significant compensation levels; a minimum in recovery time was observed which is ascribed to depopulation of the active recombination site. Results indicate that the energy level of this center lies in the upper half of the silicon bandgap. Evidence for an annealing-induced acceptor state in Pt:Si is found by heat treatment of the Pt-doped diodes at 735C.

## INTRODUCTION

Platinum is an important dopant for control of lifetime in silicon devices (1,2,3). Despite numerous studies of Pt-doped Si, there is confusion regarding the number of deep levels in silicon which may be attributed to Pt or Pt complexes (4-9). It is widely agreed that in cases where the Pt concentration is small compared to the density of shallow dopants, the dominant electrically active Pt defect, commonly designated as $Pt_I$, gives rise to either an acceptor level at about Ec-0.25 eV in n-type silicon or a donor at Ev+0.30 eV in p-type silicon. These levels have been observed in numerous studies.

However a number of authors have reported evidence of other Pt sites associated with different energy levels, especially in the case of n-type silicon which has been overcompensated to p-type by Pt doping (7,10). In addition, heat treatment of Pt:Si at 700-800C has been observed to cause some unusual effects probably associated with Pt complex formation (10-14). An acceptor level located approximately

0.4 eV above the valence band has been reported in a number of studies (4,7,10,12,13,15) and has been associated with a defect identified in an ESR spectrum as the $Pt_{II}$ site. Although normally present in low concentration, this impurity has been implicated as an important recombination center in Pt-doped silicon (16).

In this report we discuss the effects of Pt doping on the breakdown voltage and reverse recovery times of fast, high voltage $p^+nn^+$ diodes. Since these devices require Pt doping of near-intrinsic silicon in the base region they should be expected to be sensitive to $Pt_{II}$ type defects. A range of resistivites sufficient to attain overcompensation was selected. We also studied the effect of annealing at 735C for 2 hr. on device performance. Two diode pn diffusions with different proportions of aluminum and boron at the $p^+n$ junction were examined. Spreading Resistance Profiles (SRPs) were obtained for selected samples.

## EXPERIMENTAL DETAILS

$P^+nn^+$ diodes were fabricated from 10 mil thick <111> orientation unpolished Float Zone phosphorous n-type silicon wafers of 8-37 Ohm-cm resistivity supplied by S.E.H., Inc.. Type A diodes were fabricated with Filmtronics' A1B120A spin-on boron and aluminum source whereas Type AB diodes employed A1B120A together with a Filmtronics B15 boron preform. A Filmtronics P40X phosphorous preform was used as the n-type source in both cases. The p- and n-type dopants were co-diffused at 1250C for 32 hr. The resulting $p^+n$ junction depth was about 70 microns, and the diode n-base width was about 100 microns. Platinum was incorporated into the samples by spin-coating Emulsitone Platinum-silica-film on the p-side and diffusing in nitrogen at 900-960C for 1.3 to 15 hr. The wafers were loaded and unloaded from the diffusion tube at a rate of 2 in./min. They were then etched to remove excess platinum and seperated in halves. One half of each wafer was annealed by heating at 735C for 2 hrs.

The partial wafers were Ni/Au plated for ohmic contacts and diced into 0.090"x0.090" chips. Single chip diodes were junction-etched and coated, mounted on leadframes and measured for breakdown voltage (BV) at 10 microamps reverse current on a Tektronix 576 curve tracer. Reverse recovery times were measured at $I_F$= 2 mA, $I_R$= 5mA and 80% recovery on the oscilloscope. Spreading resistance analyses of sample diodes were performed by Solecon Laboratories, San Jose, CA.

## EXPERIMENTAL RESULTS AND ANALYSIS

The major difference between Type A and Type AB diodes as determined from spreading resistance analysis of the devices without Pt is that in both cases there is a "shoulder" in the $p^+n$ junction profile typical of deeply diffused devices incorporating aluminum, but

the effect is much more pronounced for the Type A diode because it was diffused with a relatively higher concentration aluminum source. As a consequence, the base width of the Type A diode is significantly narrower (80 microns vs. 150 microns for the Type AB diode).

Carrier Concentration

A spreading resistance analysis was performed for the 37 Ohm-cm Type A and other selected diode structures. The well-known effects of platinum diffusion in n-type silicon, compensation of shallow level donors by Pt acceptors and conversion of n- to p-type at relatively high doping levels, were observed for our Pt-doped n-base diodes.

We have observed that annealing Pt doped samples at 735C, in general, further compensates the n-type base and enhances the conversion of n-type to p-type, presumably by introduction of additional acceptors which are probably not the same $Pt_I$ acceptor state dominant in lightly doped n-type Si. We also have found that annealing of p-type base regions, which were converted from n-type by Pt diffusion, at 735C for 2 hr. decreased the base resistivity, again presumably due to the introduction of these annealing-induced acceptor states.

In order to provide a quantitative measure of the compensation effects observed, we assume that Pt does not alter carrier mobility at these low concentrations and measure the difference in the net carrier concentration due to Pt diffusion. The results are summarized in Table I. Also listed is the predicted compensation point, in resistivity units, which corresponds to the minimum initial n-type resistivity which would be converted to p-type by the given Pt treatment. Analysis shows that the "compensation level," i.e. the ratio of Pt acceptor concentration to the native donor concentration, varies under our experimental conditions from "lightly compensated" to fully "converted" to p-type.

From the Pt-related acceptor density data in Table I, we observe that 900C Pt diffusion for any resistivity up to 37 Ohm-cm or diffusion of 8 Ohm-cm resistivity at any temperature, time combination up to 960C, 15 hr. could be considered "lightly compensated" in our experimental matrix. On the other hand, diffusion at 950-960C can "convert" 27-37 Ohm-cm silicon and annealing of samples diffused at these temperatures can overcompensate resistivity levels down to 15 Ohm-cm.

Breakdown Voltages

The main parameters determining diode breakdown voltage are the base resistivity, the width of the intrinsic base region and, for deep diffused junctions, the junction gradient (1). In the lightly compensated regime none of these parameters is significantly affected and therefore BVs are nearly independent of Pt concentration. Examining Figures 1 and 2, which show the effect of Pt diffusion on the BVs of Type A and AB diodes, respectively, we see that this is the case for

the 8 Ohm-cm material for all Pt conditions tested and for 15-27 Ohm-cm silicon doped at 900-910C.

It is also shown in Figures 1 and 2 that from 910 to 920C for 15-27 Ohm-cm there is an increase in BV for both Type A and Type AB diodes. This can be attributed to increased base resistivity due to compensation of the n-base region by Pt acceptors. An additional effect of compensation is to decrease the junction gradient, which also increases BV, especially for high base resistivity Type A diodes.

Again referring to Figures 1-2, the dramatic drop in BV from 900 to 920C for 37 Ohm-cm material is ascribed to conversion of the n-base to p-type.

To summarize, the effect of Pt doping is insignificant in the lightly compensated regime, increases the BV for the case of partial compensation, and dramatically degrades the blocking capability of the overcompensated diode. This is also clear from Figures 3 and 4, which show the influence of Pt doping on the BV vs. resistivity plots for diodes Type A and AB: the 900-910C diffusions replicate the no Pt Type A diode and are classified as "lightly compensating" even in 37 Ohm-cm material, whereas Type A diodes treated to 920C, 15 hr., 960C, 1.3 hr. or 950C, 2 hr. have greatly reduced BVs in 37 Ohm-cm silicon due to heavy overcompensation. In the case of diode Type AB, devices diffused at 950 and 960C only are overcompensated.

The effect of Pt diffusion parameters on the breakdown voltage of annealed Pt doped silicon is shown in Figures 5 and 6 and the influence of Pt doping on BV vs. resistivity is displayed in Figures 7 and 8 for diode types A and AB, respectively. These results are qualitatively similar to those obtained with the unannealed samples in the corresponding Figures 1-4. Annealing generally increases the number of acceptor sites but not to the extent that the boundaries between lightly and partially compensated regimes are much affected. The greatest effect is on borderline cases between partial and overcompensation. For the Type AB diodes degradation in 950 and 960C diffused and annealed diodes is found for 21 Ohm-cm and 37 Ohm-cm material whereas this was the case only for 37 Ohm-cm in the unannealed samples. The general result of annealing on BV is to enhance the effects seen in as-doped samples: for the partially compensated case, the BVs are enhanced by annealing and in the overcompensated regime the BVs are further degraded by annealing. For the Type AB diode there is an intermediate range where annealing appears to have little effect on BV, e.g. 21-37 Ohm-cm material doped at 900-920C.

Reverse Recovery Time: Effect of Pt Diffusion

Reverse recovery measurements for "lightly compensated" 8-21 Ohm-cm, 900-950C diffused Type A diodes reveal the expected inverse dependence of lifetime on Pt diffusion temperature, as shown in Table II (upper lefthand corner). However, at higher levels of compensation

the behavior is more complex: for samples with an initial resistivity of 27-31 Ohm-cm little difference in Trr is observed between 900 and 920C (15 hr.) diffusions and the average recovery times for diodes diffused at 960C for 15 hr. are actually higher. In fact even for 8 Ohm-cm material the average Trr of diodes doped at 960C for 15 hr. is higher than for devices doped at 920C for 15 hr. or for only 1.3 hr. at 960C (top row of Table II). For an initial base resistivity of 37 Ohm-cm (bottom row of Table II), the average recovery time is found to increase from 900 to 910C, then decrease from 920 to 960C. Spreading resistance analysis has determined that this "anomolous" decrease in Trr at high compensation levels corresponds to conversion of the device to a fully compensated $p^+pn^+$ diode. Considerable variation in the data is noted for the partially overcompensated samples, as indicated by the large reported standard deviations. Data for the Type AB diode, shown in Table III, are consistent with these results but show less variation.

To summarize, we have observed a limit on the reduction of the reverse recovery time of $p^+nn^+$ diodes by Pt doping which occurs when the concentration of Pt acceptors significantly begin to compensate the n-type native carrier concentration. As conversion to p-type is approached Trr values are higher for devices with higher Pt concentrations. Once total conversion is reached however, the resistivity of the p-base diode is decreased and the Trr is seen to decrease as well.

These results indicate that the lifetime controlling level is located in the upper half of the band gap in "lightly doped" Si: compensation of the n-type base lowers the Fermi level causing a thermal depopulation of charged recombination centers and a net decrease in density of recombination centers even though the total Pt concentration may increase. This explaination is consistent with the results of Miller, et. al. (5) who report that the Pt-I acceptor at Ec-0.23 eV is the lifetime controlling level in lightly doped Pt:Si and who have discussed the sensitivity of the lifetime of the $Pt_I$ center to statistical occupation factors.

Another possible cause of depopulation of the recombination center at higher diffusion temperatures and higher compensation levels is redistribution of Pt impurities; in particular, the $Pt_{II}$ acceptor has been reported to be present in high concentration in this regime (7). However, if the Pt-II level, located at about Ev+0.4 eV, is the dominant recombination center in lightly doped silicon, as reported by Lisiak and Milnes (16), there would be no reason to expect an increased Trr in moderately compensated Si since essentially all of the $Pt_{II}$ acceptors are ionized; in the case of diffusions under conditions of heavy compensation we would expect a decrease in Trr as the relative proportion of the $Pt_{II}$ sites is supposed to be greater.

Reverse Recovery Time: Effect of Annealing

The effect of annealing at 735C for 2 hr. on diode recovery

times of Pt doped samples is found in Table II for the Type A diode. Annealing of "lightly doped" samples increases their lifetime. A modest increase or no effect is found in partially compensated samples. A decrease in $T_{rr}$ is found for the overcompensated samples. Spreading resistance analysis shows that the samples which have significantly decreased recovery times after annealing are overcompensated p-base diodes.

Annealing of Type AB diodes, as shown in Table III, has no effect on the lifetime of "lightly compensated" devices and increases the lifetime of partially compensated diodes. Again in the highly overcompensated regime, a sample was found which showed a decrease in Trr after annealing and again spreading resistance analysis identified that it had been fully converted to p-type in the base region by Pt diffusion.

It is notable that for the "lightly compensated" diodes which show increases in lifetime upon annealing we do not observe any change in breakdown voltage. This confirms that the compensation of these devices is practically insignificant and does not account for the increase in lifetime. Instead, we suggest that what is happening in this case is conversion of active recombination sites to annealing-induced acceptor states.

## SUMMARY AND DISCUSSION

The effects of platinum diffusion on the breakdown voltage and reverse recovery time of $p^+nn^+$ diodes at low compensation levels were found to conform to standard expectations, i.e., BV increases due to compensation of the n-type base by Pt acceptors, and Trrs are lower for diodes doped at higher temperatures. However a minimum reverse recovery time is reached as the Pt doping levels approach the initial base carrier concentration. This is ascribed to depopulation of the active recombination center. Although $Pt_{II}$ sites may be present, especially at high compensation levels, the evidence indicates that they do not play a role in the recombination kinetics of lightly doped samples.

We have documented increased recovery rates in heavily overcompensated diodes which have been converted to $p^+pn^+$, perhaps due to recombination by neutral acceptor recombination centers. BVs are severely degraded in the overcompensated regime.

Our investigation of the effect of post-Pt annealing at 735C on Pt doped Si diodes reveals an annealing-induced acceptor defect. Formation of this defect has complex and nonuniform effects on the carrier concentration profile. However, in general, it increases the base resistivity of the n-base diodes and converts n- to p-type. Breakdown voltages are seen to increase upon annealing for moderately doped

diodes and decrease for devices which are overcompensated by the treatment. Reverse recovery times are increased except for p-base diodes which have been overcompensated by Pt diffusion, which have lower Trrs after annealing.

These observations are consistent with the reports of heat treatment of Pt-doped Si by other authors (11,12). The origin of this annealing-induced acceptor state is not clear. From the decrease in reverse recovery rate in lightly compensated diodes which we observed, the report by Saito, et. al. (11) of a decrease in substitutional Pt and release of vacancies, and other observations of the deactivation of certain electrical properties (13,14) upon heat treatment, the evidence indicates that conversion of partially ionized $Pt_I$ sites to some sort of charged Pt acceptor complex occurs. This complex may be a combination of Pt with other impurities, such as phosphorous (6). Another possibility is an interstitial $Pt^-$-Pt pair. It should be noted that several authors have reported that the effect of heat treatment is reversible by reheating at diffusion temperatures. Also, heat treatment has been associated with the appearance of an acceptor level at about $E_V$ + 0.4 eV (10), which suggests that it is the same site as the $Pt_{II}$ complex. Our data supports this idea: we have found that the annealing-induced acceptor state can convert n- to p-type and decrease the base resistivity of $p^+pn^+$ diodes and therefore probably lies in the lower half of the bandgap.

## REFERENCES


1. S.K. Ghandi, "Semiconductor Power Devices," p. 293, John Wiley, N.Y., 1977.
2. S.D. Brotherton and P. Bradley, Solid State Elec., 25, 119 (1982).
3. M.D. Miller, IEEE Trans. Electron Devices, ED-23, 1279 (1976).
4. S. Braun and H.G. Grimmeiss, J. Appl. Phys., 48, 3883 (1977).
5. M. Miller, H. Schade, and C.D. Nuese, J. Appl. Phys., 47, 2569 (1976).
6. A.O. Evwaraye and E. Sun, J. Appl. Phys., 47, 3172 (1976).
7. K.P. Lisiak and A.G. Milnes, Solid State Elec., 18, 533 (1975).
8. P.M. Sandow, M. Das, and J. Stach, J. Elec. Mater., 7, 686 (1978).
9. S.D. Brotherton, P. Bradley, and J. Bicknell, J. Appl. Phys. 50, 3396 (1979).
10. S.A. Azimov, L.I. Islamov, and N.A. Sultanov, Sov. Phys. Semicond., 8, 758 (1974).
11. R. Saito, M. Mommo, and M. Naito, J. Electrochem. Soc., 132, 225 (1985).
12. M. Akhmedova, A. Lebedev, and Sh. Makhkamov, Sov. Phys. Semicond., 9, 861 (1976).
13. Y.A. Zibuts, et. al., Sov. Phys.-Solid State, 8, 2041 (1967).
14. K.D. Glinchuk and N.M. Litovchenko, Sov. Phys.-Solid State, 6, 2963 (1965).
15. H. Carchano and C. Jund, Solid State Elec., 13, 83 (1970).
16. K.P. Lisiak and A.G. Milnes, J. Appl. Phys., 46, 5229 (1975).

TABLE I

Effect of Platinum Doping and Annealing on Carrier Concentration in Diode Base Region[1]

| Pt Diffusion Temp. | 900C | 920C | 960C | 960C | 950C |
|---|---|---|---|---|---|
| Pt Diffusion Time | 15 hr. | 15 hr. | 15 hr. | 1.3 hr. | 2 hr. |
| Conc. of Diffused Pt Acceptors | $2.5 \times 10^{13}$ | $1.1 \times 10^{14}$ | $2.0 \times 10^{14}$ | $1.9 \times 10^{14}$ | $1.6 \times 10^{14}$ |
| Expected Post-Pt Compensation Point (Ohm-cm) | 185 | 42 | 23 | 24 | 29 |
| Conc. of Annealed-In Pt Acceptors | $5.0 \times 10^{12}$ | $5.0 \times 10^{13}$ | $1.6 \times 10^{14}$ | $1.0 \times 10^{14}$ | $1.0 \times 10^{14}$ |
| Total Conc. Pt Acceptors | $3.0 \times 10^{13}$ | $1.6 \times 10^{14}$ | $3.6 \times 10^{14}$ | $2.9 \times 10^{14}$ | $2.6 \times 10^{14}$ |
| Expected Post-Anneal Compensation Point (Ohm-cm) | 154 | 29 | 12.9 | 16 | 18 |

[1]Data obtained from SRP Analyses of Type A Diodes with 37 Ohm-cm Initial Base Resistivity.

TABLE II

Reverse Recovery Times for Type A Diodes Doped with Pt for Various Temperature & Time Schedules Vs. Initial Base Resistivity

| Initial Resistivity (Ohm-cm) | Reverse Recovery Times[1] (ns) | | | | | |
|---|---|---|---|---|---|---|
| | Platinum Diffusion Temperature, Time | | | | | |
| | 900C 15hr. | 910C 15hr. | 920C 15hr. | 950C 2hr. | 960C 1.3hr. | 960C 15hr. |
| 8, As-Doped | 247 (47) | 259 (23) | 120 (12) | 132 (8) | 135 (8) | 150 (15) |
| 8, Annealed | 260 (70) | 343 (67) | 125 (12) | 125 (6) | 135 (8) | 145 (15) |
| 15, As-Doped | 357 (71) | 344 (28) | 140 (14) | 134 (2) | 190 (19) | 200 (20) |
| 15, Annealed | 439 (81) | 551(108) | 140 (13) | 139 (7) | 155 (16) | 140 (13) |
| 18, As-Doped | 290 (18) | 288 (22) | 147 (15) | 149 (11) | 175 (18) | 220 (30) |
| 18, Annealed | 382 (52) | 362 (48) | 150 (15) | 189 (38) | 215 (21) | 125 (13) |
| 21, As-Doped | 287 (16) | 362 (41) | 150 (15) | 161 (9) | 180 (18) | 250 (25) |
| 21, Annealed | 337 (13) | 351 (45) | 155 (15) | 157 (50) | 178 (18) | 130 (10) |
| 27, As-Doped | 198 (19) | 222 (25) | 190 (16) | 176 (15) | 165 (16) | 250 (25) |
| 27, Annealed | 223 (30) | 267 (14) | 214 (32) | 163 (8) | 240 (25) | 130 (12) |
| 31, As-Doped | 179 (13) | 189 (14) | 180 (18) | 166 (8) | 170 (17) | 220 (22) |
| 31, Annealed | 208 (21) | 198 (13) | 178 (15) | 179 (26) | 185 (19) | 140 (12) |
| 37, As-Doped | 260 (43) | 320 (33) | 355 (45) | 267 (49) | 240 (40) | 220 (22) |
| 37, Annealed | 299 (53) | 422 (43) | 210 (80) | 147 (37) | 200 (19) | 140 (14) |

[1]Average (Standard Deviation) of 10 samples.

TABLE III

Reverse Recovery Times for Type AB Diodes Doped with Pt for Various Temperature & Time Schedules Vs. Initial Base Resistivity

| Initial Resistivity (Ohm-cm) | Reverse Recovery Times[1] (ns) | | | | |
|---|---|---|---|---|---|
| | Platinum Diffusion Temperature, Time | | | | |
| | 900C 15hr. | 920C 15hr. | 950C 2hr. | 960C 1.3hr. | 960C 15hr. |
| 8, As-Doped | 178 (23) | 138 (3) | 150 (11) | ---- | 150 (15) |
| 8, Annealed | 168 (26) | 136 (2) | 151 (6) | ---- | 149 (15) |
| 15, As-Doped | 346 (40) | 166 (3) | 151 (14) | ---- | 170 (20) |
| 15, Annealed | 464 (22) | 162 (4) | 161 (11) | ---- | 210 (20) |
| 18, As-Doped | 340 (40) | 178 (3) | ---- | 185 (10) | ---- |
| 18, Annealed | 1030(99) | 183 (4) | ---- | 200 (10) | ---- |
| 21, As-Doped | 511 (36) | 190 (5) | 165 (9) | 195 (10) | ---- |
| 21, Annealed | 749(150) | 193 (4) | 240 (20) | 240 (10) | ---- |
| 27, As-Doped | 337 (53) | ---- | ---- | ---- | ---- |
| 27, Annealed | 466 (42) | ---- | ---- | ---- | ---- |
| 37, As-Doped | 213 (6) | 255 (10) | ---- | 300 (10) | ---- |
| 37, Annealed | 252 (8) | 255 (10) | ---- | 135 (10) | ---- |

[1]Average (Standard Deviation) of 10 samples.

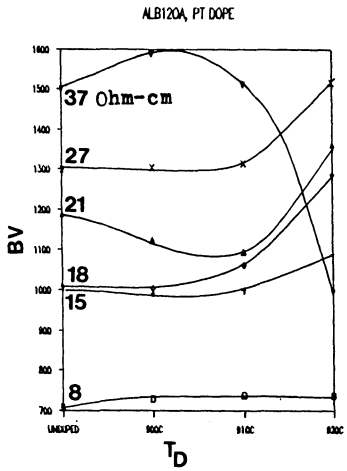



Fig. 1. Breakdown Voltage (BV) Vs. Pt Diffusion Temperature ($T_D$) for Type A Diodes.

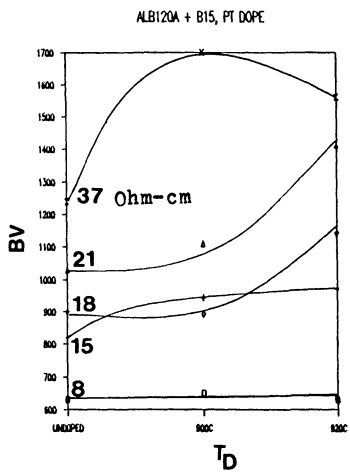



Fig. 2. Breakdown Voltage (BV) Vs. Pt Diffusion Temperature ($T_D$) for Type AB Diodes.

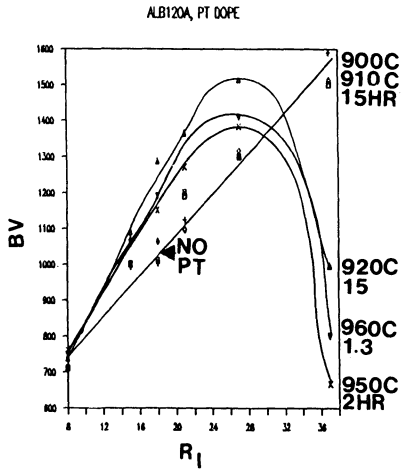



Fig. 3. Breakdown Voltage (BV) Vs. Initial Base Resistivity ($R_I$) for Pt-doped Type A Diodes.

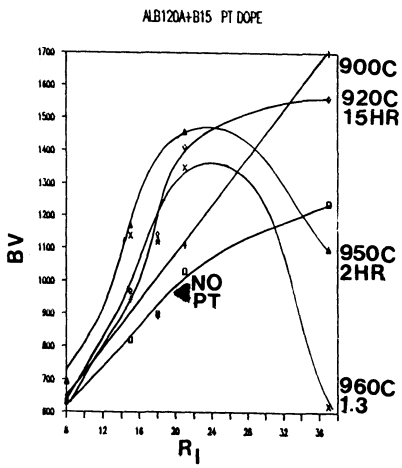



Fig. 4. Breakdown Voltage (BV) Vs. Initial Base Resistivity ($R_I$) for Pt-doped Type AB Diodes.

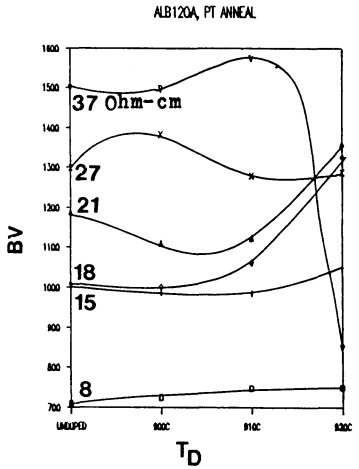



Fig. 5. Breakdown Voltage (BV) Vs. Pt Diffusion Temperature ($T_D$) for Annealed Type A Diodes.

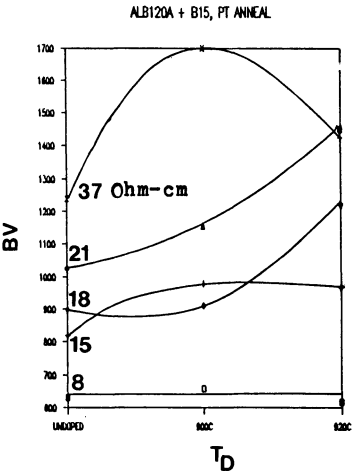



Fig. 6. Breakdown Voltage (BV) Vs. Pt Diffusion Temperature ($T_D$) for Annealed Type AB Diodes.

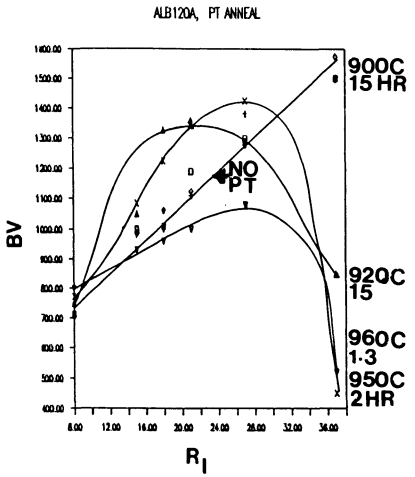



Fig. 7. Breakdown Voltage (BV) Vs. Initial Base Resistivity ($R_I$) for Pt-doped and Annealed Type A Diodes.

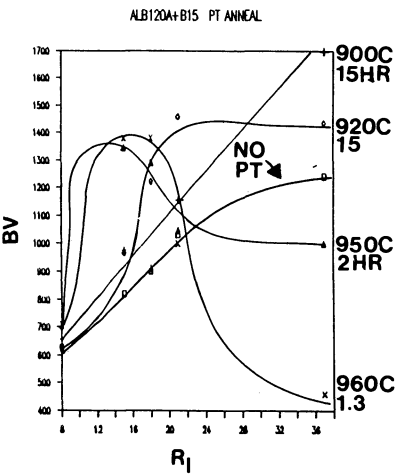



Fig. 8. Breakdown Voltage (BV) Vs. Initial Base Resistivity ($R_I$) for Pt-doped and Annealed Type AB Diodes.

Proceedings of The Electrochemical Society, PV 1987-13, 206-215 (1987)
DOI: 10.1149/198713.0206PV © The Electrochemical Society

# INVESTIGATION OF THE TURN-OFF BEHAVIOUR FOR THE DESIGN AND DEVELOPMENT OF HIGH CURRENT GTO THYRISTORS

M. Bakowski*, K. Thorselius**, F. Vojdani*.

* ASEA DRIVES, Semiconductor Component Development, Västerås, Sweden.
** Presently at BOFORS AEROTRONICS, Stockholm, Sweden

## ABSTRACT

Understanding of the turn-off behaviour of parallel connection of multitude of elementary thyristor units constituting the GTO (Gate Turn Off) thyristor is of primary importance for the development of the GTO thyristors with high current and voltage ratings. The maximum turn-off current was measured on test structures with emitter length, emitter width and gate contact width varying from 2 to 6 mm, 150 to 350 $\mu$m and 100 to 500 $\mu$m, respectively. The emitters had both constant and varied width and number of emitters was from 1 to 14. The uneven current load sharing between emitters explains following findings: The nonlinear dependence of the maximum turn-off current on the number of emitters connected in parallel and deviation from theoretically predicted inverse proportionality between maximum turn-off current and emitter width which is shown to hold for single emitter. The influence of the lateral voltage drop in the gate metallization on the maximum turn-off current is demonstrated and results agree well with two-dimensional computer calculations of current flow and potential distribution.

## INTRODUCTION

Since E Wolley published his analytical model of uniform turn-off process about 20 years ago (1) there have been an ever increasing need for the understanding of the role played by the geometrical arrangement of the emitters and gate contact and nonuniformities due to the starting material and process. The importance of improvement in uniformity of the turn-off behaviour is accentuated by the constant demand for GTOs with higher current control capability which requires components with increased area and number of elementary units. However, due to the complexity of the problem a satisfactory theoretical model including all the relevant mechanisms is still lacking and the approach has been mainly experimental.

The most important findings of several of such empirical studies are summarized below. The point of reference is Wolley's model according to which the maximum turn-off current is directly proportional to the emitter length, $l_E$, and inversely proportional to the emitter width, $b_E$. It is also proportional to the number of identical emitters, $n_E$, or total emitter area, $A_E$.

First of all the turn-off process in a single emitter was found to be nonuniform. Plasma is shown to break into several narrow, localized channels before being extinguished, instead of following the rectangular shape of the emitter and forming a narrow stripe along the emitter's center line (2),(3). This causes the maximum turn-off current to decrease instead of increasing as the emitter length is increased above a certain value; the value of about 3 mm has been reported (3). The maximum turn-off current increases as the emitter width is decreased but the dependence is either weaker and/or current value is lower than predicted by Wolley (2), (3), (4). Secondly, measurements performed on test structures consisting of several emitters show a dependence of maximum turn-off current on emitter width similar to single emitter structures (5), (6), however, the deviation from the predicted values is greater. The dependence of maximum turn-off current on the number of individual emitters is nonlinear and of the type $\sqrt{A_E}$ (4), (6) or log $A_E$ (5), where $A_E$ is total emitter area. The mechanisms responsible for those observations are connected with nonuniformities in the impurity concentration distribution, the minority carrier life time distribution and crystal defects distributions and with the lateral voltage drop in gate metallization. All of these factors influence current load sharing between elementary emitters.

Assuming a uniform turn-off process and totally identical emitters (process and material homogenity) and no lateral voltage drop in the gate metallization would give today's GTOs about 20 times higher nonrepetitive current turn-off capability.

## EXPERIMENT AND RESULTS

Test structures have total emitter area equal to 0.04 $cm^2$ or 0.08 $cm^2$ and consist of 3 to 14 identical emitters arranged in parallel. Measurements were done at anode d.c. voltage $V_a$ = 500 V and dV/dt was kept at about 500 V/$\mu$s by adjusting snubber capacitance. In this way switching losses could be kept reasonably constant with the variation of the turn-off current level. All measurements were done at a frequency of about 1 Hz and at room temperature.

In Fig. 1 typical results of the maximum nonrepetitive turn-off current density versus the width of the emitters are shown for one of the investigated technological process and silicon quality alternatives. The values shown are both for single emitters and test structures with $A_E$ = 0.04 $cm^2$. The analytical expression based on Wolley's model is shown in the insert and calculated for comparison. The $R_p$ is p-base sheet resistance, $V_{bE}$ is breakdown voltage of emitter junction and is relation between the anode current being turned off and the maximum gate current necessary to accomplish that.

The dependence of maximum turn-off current on the length of the emitter, for single emitters, is identical in character to the one reported in (3). The maximum value of turn-off current is diminishing with increasing emitter length for $l_E > 2.5$ mm (not shown). The behaviour is explained by the nonuniform character of turn-off process (the "spotty" turn-off) (2), (3).

In Fig. 2, a typical behaviour of the maximum nonrepetitive turn-off current, $I_{ATOM}$, with increasing number of emitters is shown. Data fit well a $I_{ATOM} \sim \sqrt{A_E}$ dependence.

In Fig. 3, the results of nonrepetitive maximum turn-off current density versus the gate metal width between emitters, are shown. The purpose of this investigation was to study the influence of the lateral voltage drop in the gate metallization during turn-off. Results of 2D-calculations of resistive voltage drop in the gate metallization, being a solution to heat transport equation

$$\Delta\Psi = -\frac{Q}{\sigma_{Al}}$$

where Q is volume density of current sources and $\sigma_{Al}$ is conductivity, are summarized in Fig. 4. Computations were performed with the program system "ACE" (8). Curves (1) are the numerical (.) and the analytical (+) solution for the case of $n_E = \infty$. The analytical solution is given by

$$V = \frac{j_o \cdot l_E^2 \cdot \varrho_{Al}}{\Delta_{Al}}$$

where $j_o$ is gate current density per length unit of emitter periphery, $l_E$ is length of the emitters, $\varrho_{Al}$ is sheet resistivity of the gate metallization and $\Delta_{Al}$ is width of the aluminium contact between emitters. The measured value of $\varrho_{Al}$ is 2.7 m$\Omega/\square$.

Curve ② is a numerical solution for the case of limited number of emitters, $n_E = 3$, as shown in the insert. Gate current density values $j_o$, for both ① and ② are about 20 A/cm.

Curve ③ finally is a numerical solution with proper $j_o$ values, about 5 A/cm, taken from measurements.

In Fig. 5 position of the destruction sites for test structure with 3 emitters are shown. Emitters are 5.5 mm long and 250/um wide and the spacing between them is 500/um. Two cases of current extraction are shown. First, with the gate contacted on one side of the structure and second, with the gate contacted on both sides of the structure.

In Fig. 6 current and voltage waveforms at the instant of destruction are shown for the test structure of Fig. 5 with gate contact on one side of it. The figure illustrates also measurement conditions.

In Fig. 7 the test structure with the emitter dimensions identical to the one of Fig. 5 but with reduced spacing between the emitters is shown. The spacing is 200/um.

In Fig. 8 the destruction site for the test structure with 10 emitters is shown. The emitters are about 3 mm long and 250/um wide.

Finally, in Figs 9 to 12 results of computer calculations of the potential distribution and current flow for the structures of Fig. 5 and Fig. 7 are presented.

## DISCUSSION OF THE RESULTS

It is obvious that all of experimental observations are in some way related to the nonuniformities. These nonuniformities are responsible for the distribution in I(V) characteristics over the population of elementary units and consequently also for the uneven current distribution between them. The uneven current load sharing leads in turn to the distribution in the turn-off time, because the units conducting more current take longer time to turn-off. Two mechanisms are believed to operate. At first, assuming a perfect electrical isolation between elements corresponding to the parallel connection of discret components, as soon as some of the units turn off, the remaining ones will obtain an increased current load in accordance to the I(V) distribution at this point in time (3), (6), (7). Secondly, in real device, the elementary thyristor units communicate with each other through p-base and n-base resistances

depending on the spacing between them. The closest neighbours to the units turning off get, therefore, an additional share of current during the last stage of the turn-off process. As the impedance in the unit turning off increases, the current seeks its way to the neighbouring unit with the lowest impedance. The combined result of the above is that GTO turn-off failure most often occurs in one single element, the last one to be turned off, and additionally to that in a localised channel within that element, as discussed earlier.

The $j_{ATOM}$ values for single emitters, in Fig. 1, follow well the predicted dependence for uniform turn-off. The predicted values are, however, higher by a factor 1.25.

The $j_{ATOM}$ values for multielement structures follow the model for $b_E > 250/um$, however, the predicted values are higher by a factor 1.8. The generally lower and decreasing values of $j_{ATOM}$ as the $A_E$ is increased are believed to be consistent with the both mechanisms described above. The strong deviation from the behaviour predicted by model at $b_E < 250/um$ is explained with the help of Fig. 2. The nonlinear dependence of $j_{ATOM}$ on $A_E$ indicative of uneven current load sharing (6) is much more pronounced for small $b_E$ values. The possible explanation being that wider emitters have better ability of averaging the effect of existing nonuniformities equalizing in this way the current load sharing between themselves.

A plot of $I_{ATOM}$ as a function of the $n_E$ for the analyzed structures shows the following: the test structure with separation between emitters $s = 500/um$ shows the most linear behaviour among the three structures while the structure with $s = 100/um$ shows the most nonlinear. That suggests that one of the dominating mechanisms responsible for the results of Fig. 3 is the current communication between the units through base resistances which should be strongest for the structure with closest spaced emitters, $s = 100/um$, while the structure with $s = 500/um$ can be regarded as consisting of almost isolated, noncommunicating emitters.

Finally, what concerns the problem of lateral voltage drop and results shown in Figs. 3, 5 and 7-12 the conclusion is that the lateral voltage drop in gate metallization is the most important factor determining the site of destruction. A very good agreement is obtained between the calculated and actual location of the destruction spot. The destruction occurring always in the area where the lateral voltage drop has its maximum value. However, as seen in Fig. 8, in a structure where potential distribution along the emitter is the same for all the emitters (the case of $n \rightarrow \infty$) the destruction occurs in the weakest member of the emitter family but still most likely in the area of maximum lateral voltage drop values (Fig. 8).

## CONCLUSIONS

Some of the results of extensive experimental study involving hundreds of test structures and the same amount of 400 A, 2 kV GTO thyristors are presented here. The main objective of the presentation is to discuss and identify mechanisms and factors determining the current turn-off capability of GTOs. The mechanisms discussed here are:

a) nonuniform character of the turn-off process in a single elementary thyristor limiting the optimum emitter length to about 2.5-3.0 mm.

b) uneven current load sharing between different emitters responsible for nonlinear dependence of the total turn-off current on the number of emitters connected in parallel. The increase of separation between the fingers (resistive ballasting) is shown to reduce the effect and a separation of more than 500 $\mu$m is needed to "disconnect" the emitters in the actual case.

c) lateral voltage drop in the gate metallization. The treatment of the problem is presented and the results show it to be the most important factor which determines the location of destruction spot.

d) Finally the turn-off current is shown to increase with reduced emitter width and shows an optimum between 150 and 250 $\mu$m for the structures with equal total emitter area.

In the final design the choice of the optimum emitter width, lenth and emitter-gate geometry is guided in addition to turn-off behaviour also by the turn-on behaviour, forward voltage drop and thermal considerations.

## REFERENCES


1. E.D. Wolley, "Gate turn-off in p-n-p-n devices", IEEE Trans. Electron Devices, vol. ED-13, No. 7, pp 590-597, 1966.

2. H. Ohashi and A. Nakagawa, "A study on GTO turn-off failure mechanism", IEEE Conf. Rec., IEDM 81, pp 414-417, 1981.

3. M. Azuma, M. Kurata and H. Ohashi, "Design Consideration for high power GTOs", Jap. J. Appl. Ph., vol. 20, suppl. 20-1, pp 93-98, 1981.

4. T. Nagano, H. Fukui, T. Yatsuo and M. Okamura, "A snubber-less GTO", IEEEConf. Rec., PESC'82, pp 383-387, 1982.

5. A. Tada, T. Miyajima, H. Hagino and M. Ishido, "Electrical characteristics of a high voltage high power gate turn-off thyristor", IPEC-Tokyo'83, pp 54-64, 1983.

6. O. Hashimoto, H. Kirihata, M. Watanabe, A. Nishirera and S. Tagami, "Turn-on and turn-off characteristics of a 4.5 kV 3 000 A Gate turn-off thyristor", IEEE Conf. Rec., IAS85, pp 876-881, 1985.

7. T.C. New, W.D. Frobenius, T.J. Desmond and D.R. Hamilton, "High power gate-controlled switch", IEEE Trans. Electron Devices, vol. ED-17, No. 9, 1970.

8. ACE (Advanced Computing Environment) User Guide, ASEA RESEARCH & INNOVATION, Dept. KZEB.

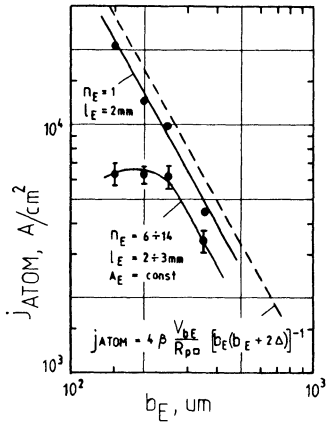



Fig. 1 Maximum turn-off current density, vs emitter width.

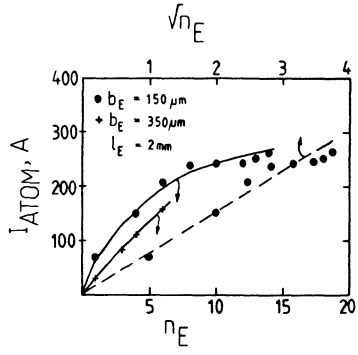



Fig. 2 Maximum turn-off current vs number of emitters.

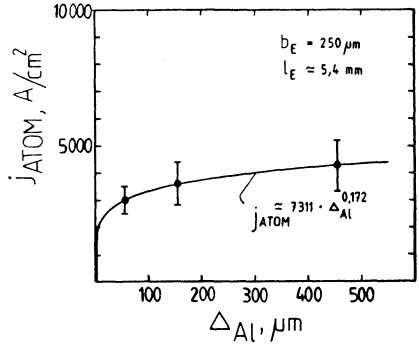



Fig. 3 Maximum turn-off current density vs gate metal width, $\Delta_{Al}$, between emitters.

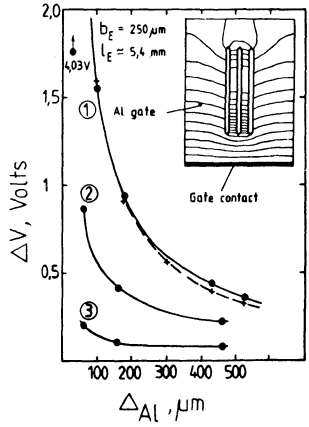



Fig. 4 Calculated lateral voltage drop in the gate metalization for 3 different cases explained in the text.

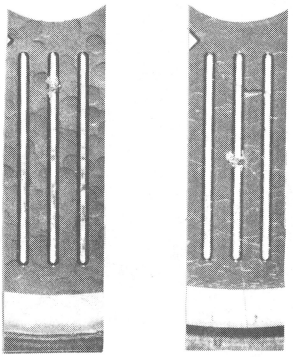


Fig. 5 Location of destruction sites for a structure with 3 emitters. The gate was contacted on one side (left), both sides (right).

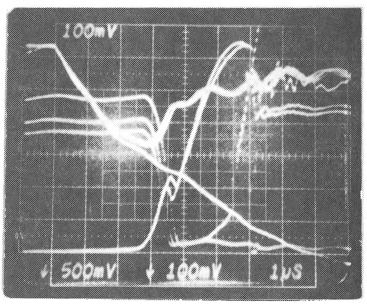



Fig. 6 Current and voltage waveforms for the structure of Fig. 5 (left). Anode current 50 A/div, anode voltage 100 V/div, gate current 10 A/div and time scale 1 µs/div.

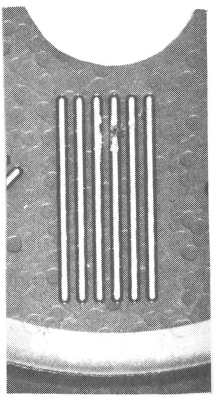


Fig. 7 Location of the destruction site for a structure with 6 emitters separated by 200 µm.

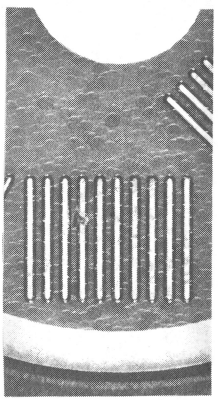


Fig. 8 Location of the destruction sites for a structure with 10 emitters.

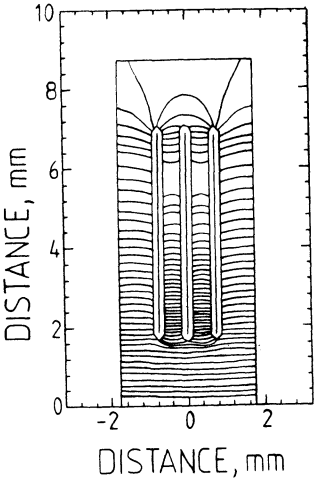



Fig. 9 2-D potential distribution for the structure of Fig. 5 (left). Equipotential lines are about 2.5 mV apart. The gate current is according to Fig. 6.

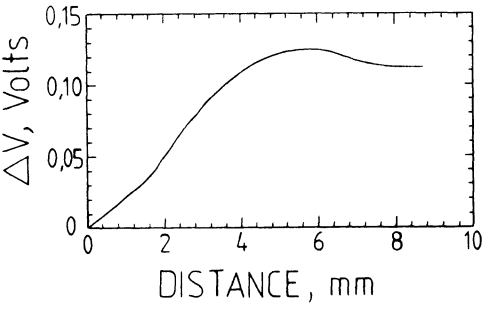



Fig. 10 Potential distribution along a line between the emitters and parallel to them for the solution of Fig. 9.

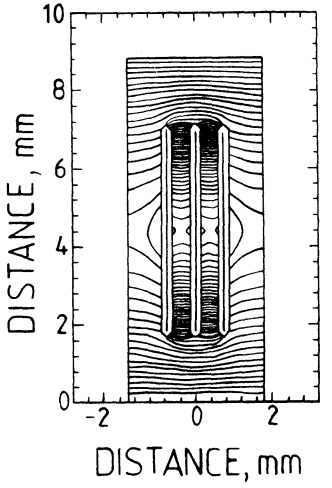



Fig. 11 2-D potential distribution for the structure of Fig. 5 (right).

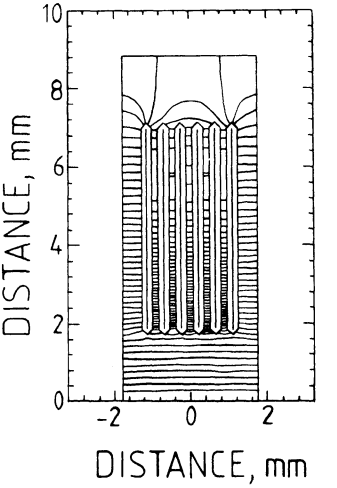



Fig. 12 2-D potential distribution for the structure of Fig. 7.

# TECHNOLOGY FOR HIGH VOLTAGE DEVICES

## SESSION CHAIRMAN:

DAVID CRESS
MARCONI LABS

Proceedings of The Electrochemical Society, PV 1987-13, 218-225 (1987)
DOI: 10.1149/198713.0218PV © The Electrochemical Society

# THE MODULAR POWER SIP
# AN INNOVATIVE PACKAGING TECHNIQUE
# FOR SMARTPOWER INTEGRATED CIRCUITS

PHIL DAVIES, BARRY SHELDON AND RICHARD RODRIGUES

INTEGRATED POWER SEMICONDUCTORS LIMITED

SCOTLAND, EH54 7BW

## INTRODUCTION

Power electronic system manufacturers are joining the general electronic industry in the requirement for higher levels of system integration, coupled with increasing sophistication in control techniques with lower costs.

Microprocessor based controllers and gate arrays are two examples of how mainstream integrated circuit companies are addressing some of the requirements in the digital control areas.

However, the task of interfacing the electronic systems to electromechanical loads still remains. It is to this area that system designers are turning their attention with the need for direct interfacing between intelligent control and power to maximise the performance to cost ratio of the complete system design. Semiconductor manufacturers are currently addressing these requirements with SMARTPOWER integrated circuits.

SMARTPOWER has become a generic term for a wide range of products and technologies all of which implement the function of interfacing logic circuits to power loads.

The development of SMARTPOWER IC's is currently one of the most exciting and dynamic sectors of the semiconductor industry, driven by large projected growth figures in several market areas.

This power integrated circuit development must however be closely followed by developments in package technology, an aspect which has been somewhat neglected by many semiconductor manufacturers. New packaging techniques are necessary to allow the successful development of complex monolithic SMARTPOWER devices. Complex SMARTPOWER designs rely heavily on a power package style which offers adequate thermal characteristics, high lead counts, configurable leadframe design, both internally and externally, and from the uses point of view a style that allows for easy handling and assembly.

Integrated Power Semiconductors has developed the Modular Power SIP (MODSIP), an innovative technique for SMARTPOWER IC packaging which addresses these requirements in a single modular design.

## PACKAGE ARCHITECTURE

The MODSIP design is based on a family concept of power SIP's (single in line package). The package consists of a two piece assembly, examples of one set of piece parts is shown in figure 1, and has been designed to provide eight standard heatsink sections with the leadframe being tailor made to suit the requirements of the system designer - external leadframe construction and Integrated Powers IC designs - internal leadframe construction in terms of lead count, pitch, width and configuration.

The family of MODSIP packages have been designed in eight widths ranging from 0.6 to 2.0 inches. The side profile, figure 2, remains dimensionally constant however for the full package range, thus providing the modular design.

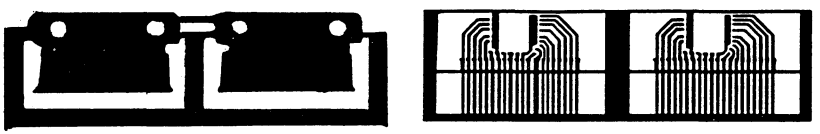


FIGURE 1

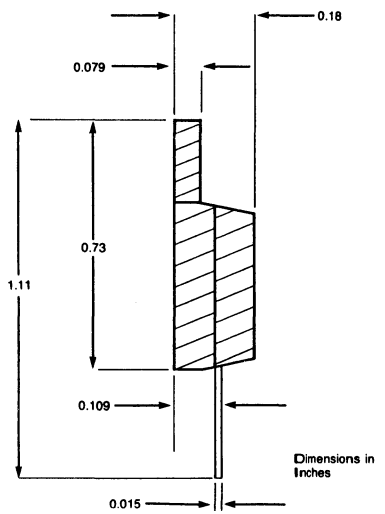



FIGURE 2

The options available with this packaging technique are summarised in table 1.

| MODULAR POWER SIPS | LENGTH | PIN COUNT 0.1 PITCH | PIN COUNT 0.05 PITCH | LEAD WIDTH | LEAD FRAME & PITCH | STAND OFF HEIGHT |
|---|---|---|---|---|---|---|
| | 0.6 | 4—6 | 8—11 | 0.02 STD OPTIONS AVAILABLE | CAN BE CUSTOMISED | 0.06 STD OPTIONS AVAILABLE |
| | 0.8 | 7—8 | 12—15 | 0.02 STD OPTIONS AVAILABLE | CAN BE CUSTOMISED | 0.06 STD OPTIONS AVAILABLE |
| | 1.0 | 9—10 | 16—19 | 0.02 STD OPTIONS AVAILABLE | CAN BE CUSTOMISED | 0.06 STD OPTIONS AVAILABLE |
| | 1.2 | 11—12 | 20—23 | 0.02 STD OPTIONS AVAILABLE | CAN BE CUSTOMISED | 0.06 STD OPTIONS AVAILABLE |
| | 1.4 | 13—14 | 24—27 | 0.02 STD OPTIONS AVAILABLE | CAN BE CUSTOMISED | 0.06 STD OPTIONS AVAILABLE |
| | 1.6 | 15—16 | 28—31 | 0.02 STD OPTIONS AVAILABLE | CAN BE CUSTOMISED | 0.06 STD OPTIONS AVAILABLE |
| | 1.8 | 17—18 | 32—35 | 0.02 STD OPTIONS AVAILABLE | CAN BE CUSTOMISED | 0.06 STD OPTIONS AVAILABLE |
| | 2.0 | 19—20 | 36—39 | 0.02 STD OPTIONS AVAILABLE | CAN BE CUSTOMISED | 0.06 STD OPTIONS AVAILABLE |

Further flexibility in package choice is provided by the variation in external lead configuration options and are highlighted in figure 3.

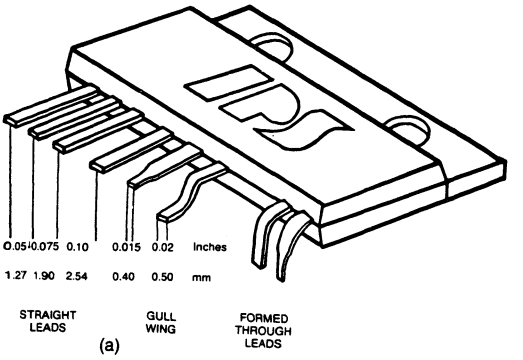



FIGURE 3

The modular design of the MODSIP considerably simplifies and reduces the assembly tooling equipment necessary for package construction and by standardising on the side profile also simplifies the tooling for pick and place machines in high volume PCB assembly.

The heatsink sections of the package are made with high thermal conductivity oxygen free copper which provides an excellent power dissipation medium. Typical junction to case thermal resistances for a 40,000 mil$^2$ SMARTPOWER die are of order of 1.5 to 2$^{O}$C/W.

Leadframe design flexibility both internal and external offers a number of important benefits to SMARTPOWER integrated circuit design and to the end user.

LEADFRAME DESIGN FLEXIBILITY BENEFITS

SMARTPOWER devices incorporating multiple output power stages and complex control circuitry rely heavily on package construction, thermal performance and flexibility to achieve their desired design objectives.

The package must be capable of efficiently dissipating the heat generated by the power stages for reliable performance and from a device design perspective must be flexible in its leadframe construction and wire bond placement.

An IC designer when in the layout stage of a chip design must give careful consideration to the thermal gradient set up across the device by the power dissipation in the output stage. It is these thermal gradients which can significantly effect the performance and reliability of the device assuming good thermal management techniques have been employed in the system design.

The IC layout must also cater for bond pad location which is usually complicated by a restricted leadframe construction.

This restricted leadframe design generally results in an IC layout having heavy metal tracks across the device to carry power to the output stage from the supply and to the load. This is further complicated by devices requiring multiple output power stages.

An example of such an IC is the IP3M05, 3 phase brushless DC motor SMARTPOWER IC shown in figure 4.

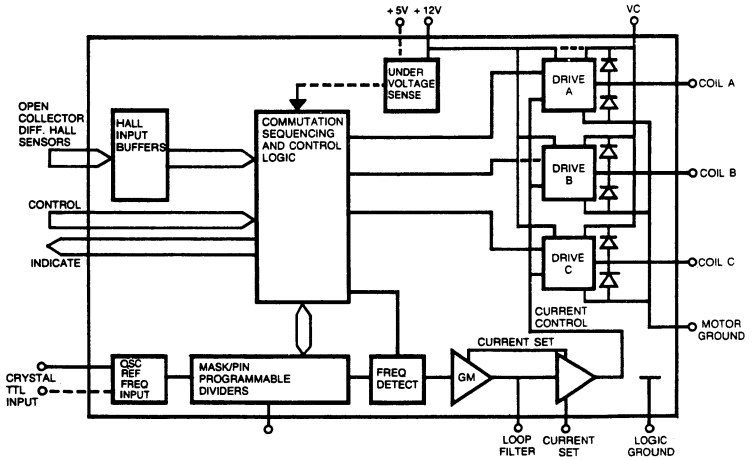



FIGURE 4

The device features a full three phase power bridge commutation and sequencing logic and a complex servo loop for accurate velocity control of motor speed. The IP3MO5 is also a semi custom ASIC device due to a number of mask programmable options offered with the basic chip design. The configurability of the MODSIP and this SMARTPOWER device provide a very adaptable design solution for various applications.

This design flexibility is made possible by having an ASIC packaging technique which can be designed to suit almost any standard, semi-custom or custom IC requirements.

## THE ROLE OF THE MODSIP IN FUTURE SMARTPOWER DEVELOPMENT

Within the SMARTPOWER arena Integrated Power's primary technology emphasis is based on devices with multiple high VA power elements integrated with analogue control and logic.

The key technology thrusts to enable the full development of such monolithic products will be in the areas of power stage and control circuit technology, packaging and semi-custom/custom ASIC design capabilities.

Combining multiple power elements with complex analogue control and logic circuitry in a single integrated circuit presents many challenges. Voltage and current handling capability of the power stage technology must be maximised requiring the optimisation of processes and power structures. Developments in the analogue control

and logic will have to follow the same advances as those made in small small signal integrated circuits. Developments such as advances from MSI to LSI technology providing a move away from component level integration such as gates and transistors to more sophisticated electronic controls such as PLA's (programmable logic arrays) and standard cells. Higher levels of integration such as VLSI technology will eventually be implemented to provide even higher device intelligence. To achieve price and performance advantages in competitive markets many manufacturers are turning to custom SMARTPOWER IC designs. Protection against possible system copying by competitors is also a major consideration.

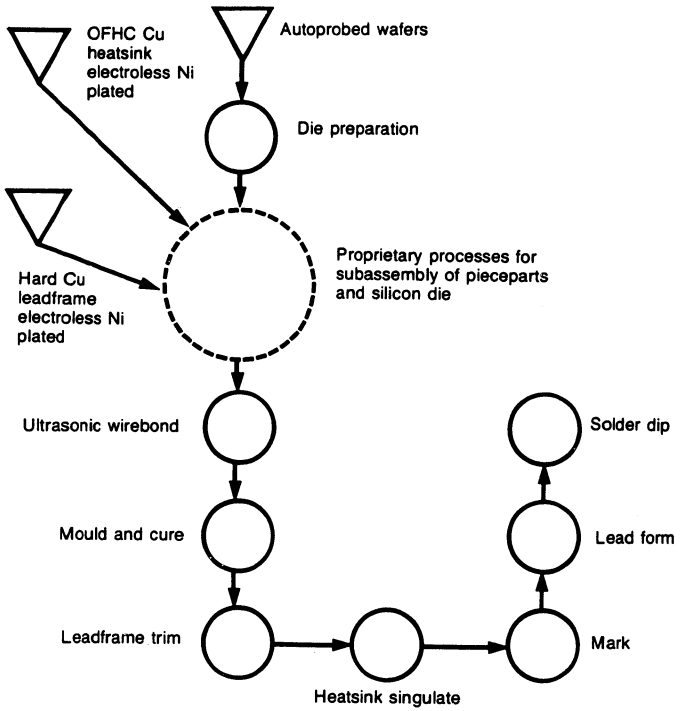
The MODSIP will play a vital role in the development of such SMARTPOWER devices. The package offers benefits to low voltage high current designs as well as high voltage and medium current level products by the flexibility of its design.

Variations in pin spacings for high voltage products can easily be accommodated for while thicker heavier pins can be designed to handle high currents.

The high pin count offered lends itself well to complex control and logic SMARTPOWER designs incorporating PLA's D A converters and various other data conversion and conditioning circuitry.

The internal leadframe flexibility will provide optimised SMARTPOWER device layouts due to the fact that the IC designer also designs the leadframe construction. The MODSIP is also a power package having excellent power dissipation properties.

MANUFACTURING AND PROCESS FLOW




CONCLUSION

The majority of requests made by systems designers for the package style of power IC's or SMARTPOWER products are either surface mount or plastic DIL devices. For low power IC's these package types are available, but supplying these packages for power products is not realistic because semiconductor manufacturers have been unable to shrink the watt.

The package styles are requested mainly for the reason of ease of handling and assembly.

The MODSIP packages fill the gap in this particular technology area in a package style which is thermally efficient and in a format that

allows simple and fast assembly techniques.

The flexibility in lead count, width, pitch and configuration allows the system designer to choose a package style to fit his system requirements rather than have to design his system around a package.

From a SMARTPOWER IC design perspective the flexibility in leadframe design gives a number of important benefits to today's SMARTPOWER products and will impact on an even greater scale, future complex monolithic or multiple chip devices.

Proceedings of The Electrochemical Society, PV 1987-13, 226-231 (1987)
DOI: 10.1149/198713.0226PV © The Electrochemical Society

# CHARACTERISTICS OF METAL/INSULATOR/SIPOS/SILICON CAPACITORS

A. Mogro-Campero and S.A. Al-Marayati
General Electric Research and Development Center
Schenectady, NY 12301

M.F. Chang and J.L. Benjamin
General Electric Power Electronics Semiconductor Department
Research Triangle Park, NC 27709

and

W.A. Kotas
Physics Department, State University of New York at Albany
Albany, NY 12222

Oxygen-doped polysilicon (SIPOS) with about 20 atomic percent oxygen was used in this study of the characteristics of metal/insulator/ SIPOS/Si capacitors. Capacitance at a given frequency is constant as a function of ramped voltage as long as minority carriers are available. Capacitance decreases from the insulator capacitance at low frequencies (less than about 100 Hz) to an insulator/SIPOS/Si capacitance at high frequencies (greater than about 100 kHz). The high frequency capacitance includes a region of depleted Si for the low doped n-type samples used. The duration of the capacitance transient produced by a voltage step towards depletion was studied as a function of temperature. The results show that the transient duration is determined by the minority carrier generation rate, so that it is limited by carrier availability.

## INTRODUCTION

Oxygen-doped polysilicon is known as SIPOS; it has been used as a passivant in high voltage applications since its inception a decade ago (1,2). Higher breakdown voltages of diodes were obtained with SIPOS, since the finite current through it relieves the surface electric field (1), but transient effects were not considered. In this paper, we investigate some characteristics of the metal/insulator/ SIPOS/Si capacitor which bear on transient response. It has been shown that this capacitance deviates from a constant value if the applied voltage is increased so that the electric field across the insulator is close to its breakdown field, and its conductivity becomes significant compared to that of the SIPOS (3). We explore further characteristics of the metal/insulator/SIPOS/Si capacitor by capacitance-voltage, capacitance-frequency, and capacitance transient measurements.

## EXPERIMENTAL PROCEDURE

Capacitors were built on n-type (100) silicon of about 20 ohm cm. 500 nm of SIPOS of about 20 atomic % oxygen was put on by chemical vapor deposition using silane and nitrous oxide at about 600 °C, and annealed at 900 °C for 30 min. An insulating bilayer of 50 nm of silicon nitride and 100 nm of silicon dioxide was deposited next and densified for 30 min at 900 °C. The thicknesses given are nominal values; variations occurred from run to run, resulting in variations in the absolute value of capacitance. Aluminum dots of 1 mm diameter were evaporated to complete the structure. The backs of the wafers had been previously implanted with phosphorus to ensure a highly doped contact to the backside aluminum. The last step was sintering at 465 °C for 30 min in forming gas.

## RESULTS

Capacitance as a function of frequency is shown in Fig.1. The transition from a low value at high frequencies to a high value at low frequencies can be understood by the simplest equivalent circuit model: the insulator capacitance $C_i$ in series with the parallel combination of the SIPOS capacitance $C_s$ and resistance $R_s$. By comparing the capacitive reactance $(\omega C_s)^{-1}$ with the resistance $R_s$, one concludes that for $\omega << (R_s C_s)^{-1}$, the net capacitance $C = C_i$, whereas for $\omega >> (R_s C_s)^{-1}$, the capacitance should decrease to $(1/C) = (1/C_i) + (1/C_s)$.

The frequency $\omega = (R_s C_s)^{-1}$ at which the capacitive reactance equals the resistance is a fundamental parameter of SIPOS, since $R_s C_s = \rho\varepsilon$, i.e., the product of resistivity and dielectric constant. The time constant $\rho\varepsilon$ is the dielectric relaxation time. The product of low field resistivity (2) and $\varepsilon$ obtained by interpolation between the values for silicon dioxide and silicon is 84 μs, or $\omega$ = 12 kHz. In Fig. 1, the corresponding frequency is 2 kHz, and the capacitance is about half way between its high and low frequency limit. Charges are not able to respond to changes in voltage at times much shorter than the relaxation time (4). Since at high electric fields (greater than about $10^5$ V $cm^{-1}$) the resistivity of SIPOS decreases exponentially with electric field (5), much lower relaxation times are possible.

Based on a relaxation time approach, an alternate interpretation of Fig. 1 is that at high frequencies only charges in the Si are able to respond to the a.c. voltage, so that the equivalent capacitor plate separation is at least as wide as the combined thicknesses of the insulator and SIPOS. At low frequencies, charges are able to penetrate and move within the SIPOS in response to the a.c. voltage so that the equivalent capacitor plate separation decreases.

For the sample in Fig. 1, a normalized capacitance of 3 corresponds to the insulator capacitance, so that given sufficient time,

charges will migrate to the SIPOS/insulator interface. It is more difficult to make a comparison between the expected and observed high frequency limit of the capacitance, since it involves the SIPOS dielectric constant which is not known precisely and an unspecified possible depletion layer in the silicon. The expected capacitance for no depleted Si was deduced as follows: some of the samples processed simultaneously had an additional thermally grown layer of Si dioxide of 28 nm, grown before SIPOS deposition. The capacitance at 1 MHz in accumulation for these samples was 97 pF, compared to 61 pF (independent of d.c. voltage in the sampled interval of ± 100 V) for the usual capacitors without the intervening oxide. Since the dielectric constant for silicon dioxide is well known, based on the 97 pF measurement, the effect of the 28 nm of oxide can be excluded, with a resulting value of 107 pF. The difference between the measured value of 61 pF and the computed 107 pF is attributable to about 500 nm of depleted Si.

The transient response of the capacitors was probed by applying a negative voltage step (Fig. 2). The capacitance decreases as the electric field penetrates into the Si to produce deep depletion. For the sample in Fig. 2 it takes 15 ms for the capacitance to return to its steady state value. This time interval is defined as the capacitance transient time, $t_F$; it is a function of voltage so that a standard voltage step of 0 to -100 V was used in this study. The behavior in Fig. 2 is analogous to the capacitance transient in an MOS capacitor, where electric field penetration into the depletion region is screened by minority carriers in the inversion region. In the present case, because of the finite conductivity of SIPOS, minority carriers can penetrate it allowing steady state conditions to be reestablished in the Si. Thus, it can be postulated that $t_F$ is proportional to the carrier generation rate.

The temperature dependence of the minority carrier generation rate is dominated by that of the intrinsic carrier concentration. The capacitance transient time is indeed observed to follow an inverse relationship with intrinsic carrier concentration (Fig. 3). This supports the conclusion that the limiting factor determining the duration of the capacitance transient is minority carrier availability.

## SUMMARY AND CONCLUSIONS

The characteristics of metal/insulator/SIPOS/Si capacitors were investigated. Capacitance vs. voltage is constant at a given frequency as long as minority carriers are available. This behavior contrasts with the variable C vs. V curves observed when no insulator is present, i.e., in metal/SIPOS/Si capacitors (6). Capacitance decreases from the insulator capacitance at less than about 100 Hz to an insulator/SIPOS/Si capacitance at greater than about 100 kHz. This behavior can be understood by a simple equivalent circuit or by

considering the dielectric relaxation time of SIPOS. A capacitance transient can be observed at 1 MHz in response to a voltage step towards depletion. The duration of the transient can be decreased by increasing the minority carrier generation rate. This was shown by the temperature dependence of the transient. Thus, the duration of the capacitance transient appears to be limited by carrier availability.

## REFERENCES


1. T. Matsushita, T. Aoki, T. Otsu, H. Yamoto, H. Hayashi, M. Okayama, and Y. Kawana, Japan. J. Appl. Phys. Suppl. 15, 35, 1976.

2. H. Mochizuki, T. Aoki, H. Yamoto, M. Okayama, M. Abe, and T. Ando, Japan J. Appl. Phys. Suppl. 15, 41, 1976.

3. D.W. Tong, D.M. Taylor, and S.J. Rzad, ECS Extended Abstracts 83-1, 660, 1983.

4. E.H. Nicollian and J.R. Brews, MOS Physics and Technology (Wiley, New York, 1982), p. 101.

5. M.L. Tarng, J. Appl. Phys. 49, 4069, 1978.

6. D.W. Tong, J.L. Benjamin, and W.R. Van Dell, IEEE Trans. Electron Dev. ED-33, 779, 1986.

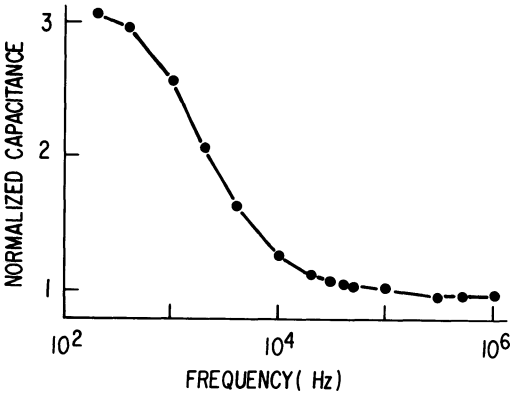



Fig. 1. Capacitance normalized to its value at 1 MHz vs. frequency; d.c. voltage was 0 V, but the curve was invariant to values in the probed range of ± 100 V.

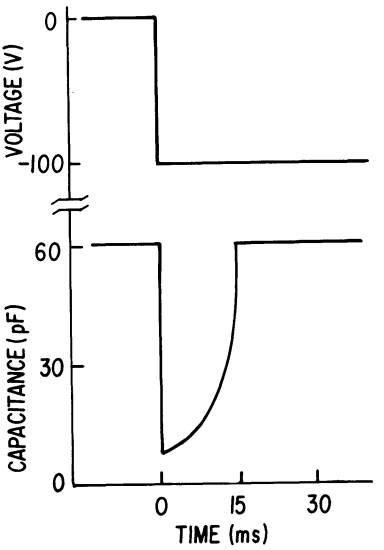



Fig. 2. Voltage step applied to the capacitor, and the resulting capacitance transient at 1 MHz.

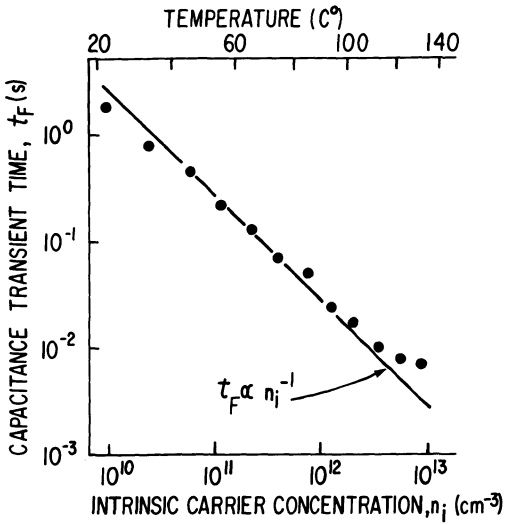



**Fig. 3. Capacitance transient time vs. intrinsic carrier concentration.**

Proceedings of The Electrochemical Society, PV 1987-13, 232-240 (1987)
DOI: 10.1149/198713.0232PV © The Electrochemical Society

# Humidity Induced Structural Changes in SIPOS

J. W. Osenbach
AT&T - Bell Laboratories
2525 North 12th Street
Reading, Pennsylvania

W. R. Knolle
AT&T - Bell Laboratories
555 Union Boulevard
Allentown, Pennsylvania 18103

High oxygen content (35 atomic % oxygen) SIPOS films were found to react with water vapor. Films which were exposed to 85° C/ 85% relative humidity appeared to have more $SiO_2$ character than those films not exposed. Also films treated at 85° / 85% relative humidity prior to 800 or 900° C nitrogen anneal appeared to have more $SiO_2$ character than those films which did not see the 85° C/ 85% relative humidity treatment prior to the anneal. These results show that the properties of SIPOS films can be significantly altered when they are exposed to a humid ambient before they are annealed at high temperatures. An 800° C or 900° C anneal stabilizes the SIPOS film so that no changes are observed after an 85° C/ 85% relative humidity treatment.

## *INTRODUCTION*

Semi-insulating polycrystalline oxygen-doped silicon (SIPOS) films have been used as passivation layers for silicon electronic devices[1,2] and as an integral part of nonvolatile memory devices.[3] Such films are produced by the reactive deposition from $SiH_4$ and $N_2O$. Both the chemical and physical properties of these films can be controlled by the deposition rate and the gas flow ratio of $SiH_4$ to $N_2O$[4]. Even though these films have been studied quite extensively, relatively little is known about the reactivity of SIPOS films with water vapor. Since SIPOS films can be exposed to humidity during the IC processing sequence as well as after the IC is packaged, it is important to know the stability of SIPOS in humid environments.

The present study was undertaken to determine the stability of high oxygen content (35 atomic %) films in an 85° C, 85% relative humidity environment. This humidity condition was chosen because it is a standard accelerated-aging condition which is used by semiconductor manufacturers to qualify incoming or outgoing non-hermetically sealed silicon devices.

## *EXPERIMENTAL PROCEDURE*

SIPOS films approximately 5000Å thick were deposited in a hot wall LPCVD reactor operated at 640° C and 0.24 torr. The gases used were $SiH_4$ and $N_2O$ at flow rates of 16 and 63 SCCM respectively. The oxygen content of the films was determined using the gravimetric method.[5] All of the films used in this study were deposited in one run and had an oxygen content of 35%± 2%. The films were deposited on 100mm p-type Si substrates that were polished on both sides to reduce infrared transmission losses.

As-deposited films were annealed in an 85° C, 85% relative humidity (RH) ambient for 48 hours. The as-deposited and as-deposited-humidity treated films were further annealed at 800° C or 900° C for 2 hours in nitrogen. Infrared spectroscopy was used to determine the structure of the films. The four wavenumber resolution infrared transmission spectra were obtained on a Nicolet 20SX Fourier transform infrared spectrometer (FTIR). The bare Si substrate spectrum was subtracted from the SIPOS on Si spectrum to give the SIPOS spectrum.

## *RESULTS*

Figures 1 and 2 show the infrared spectrum of an as-deposited SIPOS film on Si (a) for wave numbers between 400-1300 $cm^{-1}$ and 1930-4000 $cm^{-1}$, respectively. Also shown are the Si substrate (b) and the difference spectrum (c) (i.e., the SIPOS film spectrum). There are three peaks of interest in the spectrum of SIPOS; a weak absorption at 870 $cm^{-1}$ due to an Si-O interaction, a strong absorption at 1056$cm^{-1}$ due to an Si-O interaction and a weak peak at 2270$cm^{-1}$ due to an Si-H interaction. A small peak is observed at 3600 $cm^{-1}$ which is due to an Si-OH group. We believe this group was formed during the deposition. No peak is observed in the spectrum around 800$cm^{-1}$ which would be present in the infrared spectrum of $SiO_2$.[5] It should be noted that this spectrum was taken less than 24 hours after the film was deposited.

The spectrum of the as-deposited film before and after a 48 hour 85° C/ 85% RH treatment is shown in Figures 3 and 4. Also shown is the difference spectrum. The difference spectrum has been expanded to fill the plot. The absorbance ordinate only pertains to the original spectra. Figure 3 is the spectrum between 700$cm^{-1}$ and 1330$cm^{-1}$ and Figure 4 is the spectrum between 1930$cm^{-1}$ and 4000$cm^{-1}$. It is clear from the difference spectrum that the two spectra are different. The position of the strong absorption shifts after the treatment from 1056$cm^{-1}$ to 1063$cm^{-1}$. The width of this peak (full width at half height) decreases from 150$cm^{-1}$ to 140$cm^{-1}$. The maximum absorbance and the area of the strong peak increase after the humidity treatment. The peak area increases from 133$cm^{-1}$ to 140$cm^{-1}$. Furthermore, the areas of the 2270$cm^{-1}$ and the 870$cm^{-1}$ peak decrease from 0.14$cm^{-1}$ to 0.078$cm^{-1}$ and

$0.594cm^{-1}$ to $0.233cm^{-1}$ respectively after the film was treated for 48 hours in an 85° C/ 85% RH treatment. A weak peak at $800cm^{-1}$ is present in the humidity-treated films whereas it is not present in the non-treated film. These data are given in Table 1. The difference spectrum shows a small peak forming at $1230cm^{-1}$ and $910cm^{-1}$. These peaks are due to $SiO_2$ bonds. The absorption between $1150cm^{-1}$ and $950cm-1$ that resembles a first derivative in the difference spectrum is the type of absorption expected when the difference is taken of two peaks that are shifted slightly in frequency.

Figure 5 shows the spectrum of a film which was humidity treated (48 hours and 85° C/ 85% RH), then annealed for 2 hours at 800° C. Also show is the spectrum of a film which did not see the humidity treatment but had the 2 hour 800° C anneal and the difference spectrum. Only the spectrum between $700cm^{-1}$ and $1600cm^{-1}$ is shown. There are no absorption peaks in the spectrum at higher frequencies in these high temperature annealed films. Similarly, Figure 6 shows the spectrum of two films which saw a 900° C 2 hour anneal in nitrogen and the difference spectrum. One of the films was pre-treated in 85° C/ 85% RH for 48 hours the other was not.

The peak position of the strong absorption occurs at a higher frequency for the films which were humidity treated and annealed at high temperatures than for those films which were not humidity treated. Also the area of the strong peak and its maximum absorbance is higher for the humidity treated film than for the film which saw only a high temperature anneal. The width of this strong peak is also smaller for the humidity treated films. The $870cm^{-1}$ peak is not present in either of the humidity treated films, whereas it is visible in the non-humidity treated films. The position, area, and maximum absorption of the strong absorption peak are greater for the humidity treated films than for the non-humidity treated films. Finally, the $800cm^{-1}$ peak is also better defined in the spectrum of the humidity-treated films than in the non-treated films. The changes in the film are not due to a thin surface layer of $SiO_2$. The films were placed in a BHF solution for 1 minute to etch any surface oxide and no difference in the spectrum was observed.

## *DISCUSSION*

Humidity treatments at 85° C/ 85% RH of 35 atomic% SIPOS films caused the structure, as seen by infrared spectroscopy, to change. The width of the strong absorption peak is narrower for the humidity treated film than for the non-treated film. This suggests that the film has more structure. Also, this peak shifts to higher frequency. The intensity of the $2270cm^{-1}$ and $870cm^{-1}$ peaks decrease after humidity treatment. Similar changes are observed in the infrared spectra of $SiO_2$ and SIPOS films after high temperature anneals.[4,6,7] The changes in the spectrum of $SiO_2$ have been interpreted as being due to a

relaxation of the bond strain[6]. In SIPOS these changes have been interpreted as being due to a restructuring of the film by the reduction of some of the SiO groups into Si-Si groups and the oxidation of other SiO group into $SiO_2$ groups. SIPOS is thought to become a three dimensional array of interpenetrating phases of $SiO_2$ and Si after it is annealed at high temperatures. We believe that the changes in the infrared spectrum of the humidity-treated films are due to a similar restructuring of the SIPOS film.

An increase in the absorption intensity and peak area indicate that a slight amount of oxygen had been introduced into the film when it was exposed to 85°/85% RH. This combined with the fact that the Si-H bond intensity decreases in the spectrum of the humidity treated films suggests that a reaction of the form

$$ZH_2O+SiO_XH_Y \rightarrow SiO_XH_Y(OH)_Z+\frac{Z}{2}H_2 \rightarrow SiO_{X+Z}+(Z+\frac{Y}{2})H_2\uparrow$$

takes place when the SIPOS film is exposed to water vapor. We suspect that the high reactivity of these high oxygen content films with water vapor is due to the large amount of porosity (i.e., high surface area) present in the as-deposited films.

The reaction of the SIPOS film with water vapor also affects the structure of films which are annealed at high temperatures. after they are exposed to humidity. Films treated in a 85° C/ 85% RH ambient before they are annealed at high temperature look like they have received a higher temperature anneal. This suggests that the final structure of SIPOS films is critically dependent upon both low and high temperature processing steps.

Since the electrical properties of SIPOS films depend upon its structure,[8,9] the electrical characteristics of devices which use SIPOS could be influenced by extended exposure of unannealed films to a humid ambient. This in turn could lead to poor yields on devices which do not progress through the manufacturing line quickly.

Although we have not observed any structural rearrangement of films containing less than 30 atomic % oxygen when they are exposed to a humid ambient[10], we believe there is a surface reaction between SIPOS and water in these films. This reaction could lead to a structural rearrangement, due to a small increase in the oxygen content of the film, when they are later annealed at high temperatures. And, this could create high leakage currents in films which are not properly processed or sealed.

## *CONCLUSION*

High oxygen content films (35 atomic% oxygen) react with water vapor at 85° C. The reaction leads to a restructuring of the film. This reaction affects

the films properties even after the film is exposed to subsequent high-temperature post-deposition anneals. Films which are exposed to an 85° C/ 85% RH ambient prior to a high temperature anneal appear as if they have been annealed at higher temperatures.

Since this restructuring can have profound affects on the electrical characteristic of the film, films which proceed quickly through the manufacturing line could produce high quality devices while those processed more slowly could produce poor quality devices even though the stoichiometry and the subsequent high temperature processing of these films are identical.

*ACKNOWLEDGMENTS*

We thank D. S. Bingaman of AT&T Technologies for depositing the films.

REFERENCES

[1] T. Matsushita, T. Aoki, T. Otsu, H. Yamoto, H. Hayashi, M. Okayama, and Y. Kawana, "Semi Insulating Polycrystalline Silicon (SIPOS) Passivation Technology," Jpn J. Appl. Phys. 15, 35 (1976).

[2] H. Mochizuki, T. Aoki, H. Yamoto, M. Okayama, M. Abe, T. Amdo, Semi-Insulating Polycrystalline- Silicon (SIPOS) Films Applied to MOS Integrated Circuits, Jpn. J Appl. Phys., 15, 41 (1976).

[3] D. J. DiMaria, D. W. Dong, "High Current Injection into $SiO_2$ from Si rich $SiO_2$ films and Experimental Applications", J. Appl. Phys. 51, 2722 (1980).

[4] H. R. Maxwell, and W. R. Knolle, "Densification of SIPOS", J. Electrochem Soc., 128, 576 (1981).

[5] H. R. Maxwell, Jr., and W. R. Knolle, "A Simple Procedure for Measuring Oxygen Content in SIPOS Films," in "Semiconductor Characterization Techniques," P. A. Barnes and G. A. Rozgony, Editors, p 180, The Electrochemical Society Softbound Proceedings Series, Princeton, N. J. (1978).

[6] W. A. Pliskin, "Comparison of the Properties of Dielectric Films Deposited by Vapor Method," J. Vac. Sci. Technol., 14, 1064 (1977).

[7] M. Nakamura, Y. Mochizuki, and K. Usami, "Infrared Spectrum, and X-Ray Diffraction Studies of Silicon Oxide Films Formed from $SiH_4$ and $N_2O$ Chemical Vapor deposition", J. Electrochem. Soc., 132, 482, (1985).

[8] J. H. Thomas, III and A. M. Goodman, "AES and XPS Studies of Semi-Insulating Polycrystalline Silicon (SIPOS) Layers", J. Electrochem, Soc., 126, 1766 (1979).

[9] A. M. Goodman, Physics of Semiconductors Institute of Physics Conference Series No. 43, (1979), p. 805.

[10] J. W. Osenbach, W. R. Knolle, unpublished results.

TABLE I Infrared Characterization

| | 85°C/85% RH | Nitrogen Anneal | | Position of strong | Area of Strong | Area of 870 | Area of 2270 |
|---|---|---|---|---|---|---|---|
| film | 48hr | 800°C | 900°C | peak ($cm^{-1}$) | Peak ($cm^{-1}$) | Peak ($cm^{-1}$) | Peak ($cm^{-1}$) |
| 1 | no | no | no | 1056 | 133 | 0.14 | 0.594 |
| 2 | yes | no | no | 1063 | 140 | 0.078 | 0.233 |
| 3 | no | yes | no | 1073 | 154 | - | - |
| 4 | no | no | yes | 1086 | 165 | - | - |
| 5 | yes | yes | no | 1077 | 158 | - | - |
| 6 | yes | no | yes | 1087 | 173 | - | - |

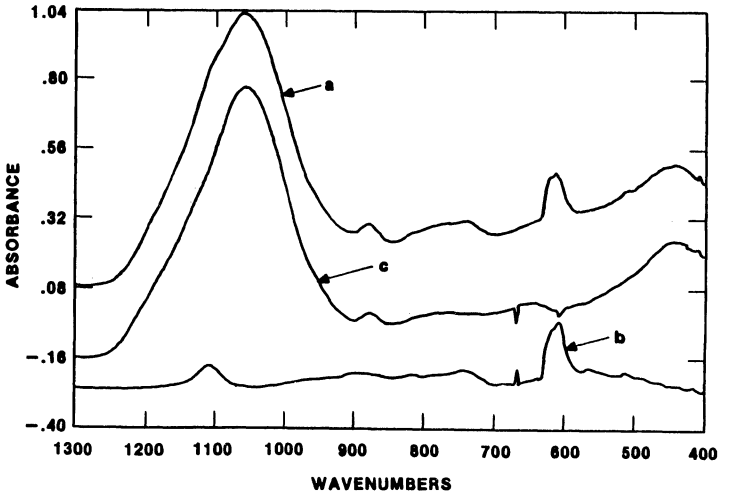



Figure 1: Infrared spectrum between 400 and 1300cm$^{-1}$ of as-deposited SIPOS a) SIPOS+Si, b) Si, c) SIPOS.

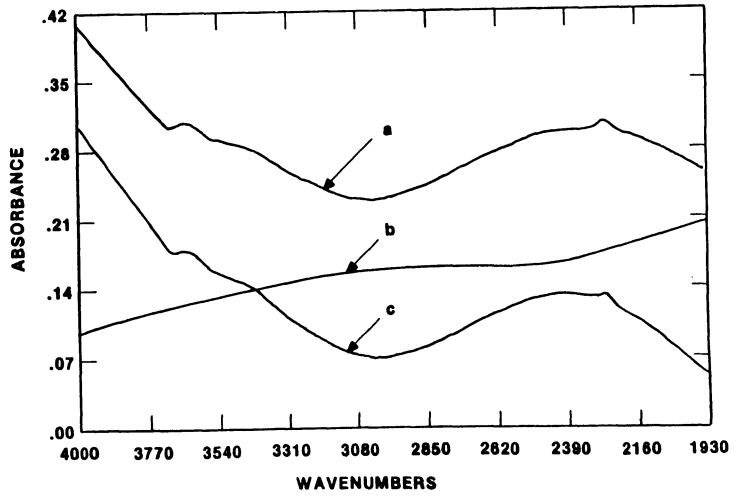



Figure 2: Infrared spectrum between 1930 and 4000cm$^{-1}$ of as-deposited SIPOS a) SIPOS+Si b) Si, c) SIPOS.

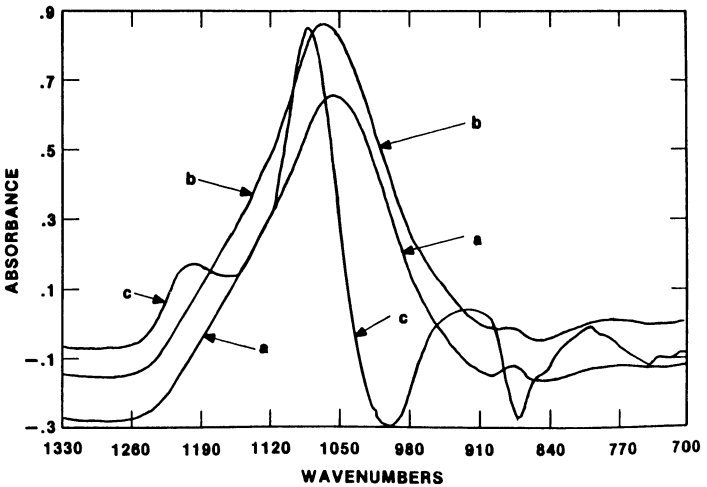



Figure 3: Comparison of the infrared spectrum between 700 and 1330cm$^{-1}$ of SIPOS before (a) and after (b) a 48hr treatment at 85° C/85% RH. Also shown is the difference spectrum (c).

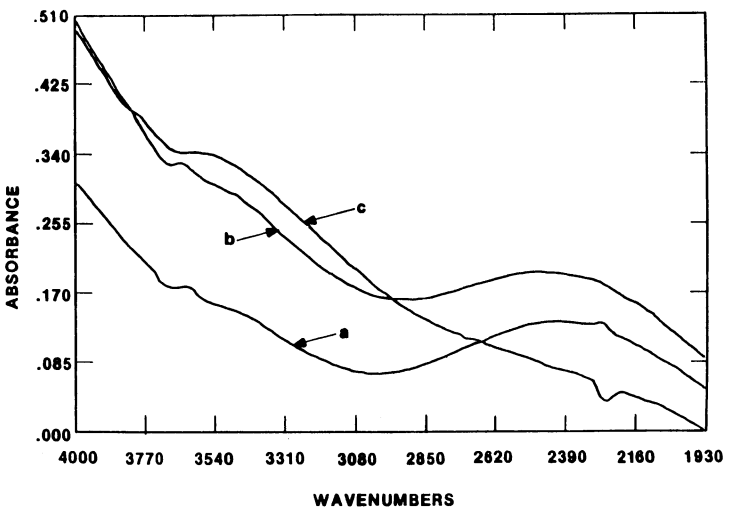



Figure 4: Comparison of the infrared spectrum between 1930 and 4000cm$^{-1}$ of SIPOS before (a) and after (b) a 48 hour treatment at 85° C/ 85% RH. Also shown is the difference spectrum.

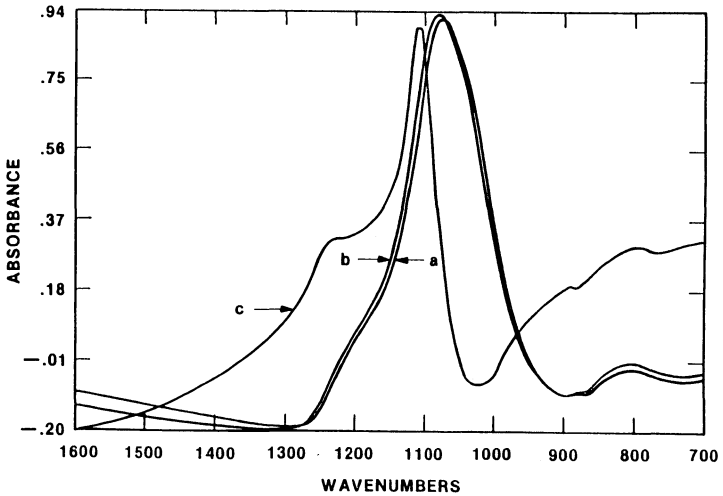



Figure 5: Comparison of the infrared spectrum of SIPOS. a) annealed at 800° C in nitrogen for 2 hours b) treatment at 85° C/ 85% RH for 48 hours then 800° C in nitrogen for 2 hours. Also shown is the difference spectrum.

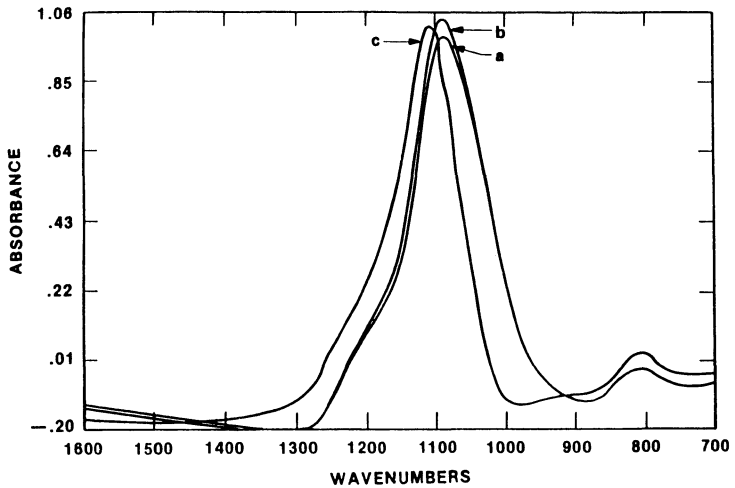



Figure 6: Comparison of the infrared spectrum of SIPOS a) annealed at 900° C in nitrogen for 2 hours b) treatment at 85° C/ 85% RH for 48 hours and then at 900° C in nitrogen for 2 hours c) difference spectrum.

Proceedings of The Electrochemical Society, PV 1987-13, 241-249 (1987)
DOI: 10.1149/198713.0241PV © The Electrochemical Society

# DIELECTRIC ISOLATION BY GROWTH OF THICK SILICON FILMS ON OXIDIZED Si WAFERS

G. K. Celler and L. E. Trimble
AT&T Bell Laboratories
Murray Hill, NJ 07974

## ABSTRACT

We review formation of single crystalline thick Si films dielectrically isolated from single crystalline substrates. This contrasts with conventional Dielectric Isolation (DI) technology, where the substrates are polycrystalline. The process of Lateral Epitaxial Growth over Oxide (LEGO) depends on seeded crystallization from the melt of 10 to 100 μm thick polycrystalline Si layers deposited on oxidized (100) Si wafers. The completed wafers have excellent structural and electrical properties.

## INTRODUCTION

Dielectric Isolation (DI) technology for high voltage and power devices was developed over twenty years ago [1] and has not changed much since then. The basic process consists of the following steps: formation of V-grooves of ~50μm depth by anisotropic etching, growth of thick thermal oxide, CVD deposition of ~500μm of polysilicon to form a new mechanical support or "handle", and removal of 90% of the original high quality crystalline substrate by mechanical means. The DI process, although expensive and difficult to control and automate, is still the only commercial method for obtaining dielectrically isolated thick silicon films on $SiO_2$.

We have developed a simpler method of forming thick dielectrically isolated single crystalline Si films on *single crystalline Si substrates* [2,3]. This method of Lateral Epitaxial Growth over Oxide (LEGO) relies on melting and controlled recrystallization of 10 to 100μm thick polysilicon films.

## GROWTH OF CRYSTALLINE Si FILMS ON OXIDE

The wafer preparation starts by growing 1-4μm of thermal oxide on 4-inch (100) Si wafers. A pattern of narrow parallel slits is then defined and etched in the oxide. The slits are aligned with the <110> crystallographic direction of Si and are spaced 3 to 5 mm apart to coincide with chip separation regions. A layer of polysilicon is uniformly deposited over the entire wafers in a conventional epitaxial reactor, followed by a capping layer of 2μm thick LPCVD $SiO_2$ needed to contain liquid silicon.

Wafers are placed on quartz pins in a lamp furnace, between an array of high intensity tungsten-halogen lamps and a water cooled metal base, as shown schematically in Fig. 1. The heating sequence and the corresponding temperatures are shown in Fig. 2. Power to the lamps is ramped up in a linear fashion until the wafer surface reaches the melting temperature. We have established before [4] that in order to melt silicon layers thicker than 1μm it is necessary to reach a considerably higher incident power density than the threshold value for superficial melting $P_{TH}$. Between the melt threshold and the threshold for deep melting $P_{DM}$, the surface of silicon is only partially molten and the system is under steady state conditions. This region of an intrinsic temperature stability stems from the increased reflectivity of molten Si compared to that of the solid Si, which reduces the coupling of energy flux into the wafer. To minimize the total time that the Si film on the $SiO_2$ is molten, the power is ramped quickly, in about 2 sec, from the melt threshold to a value that is slightly above the level required for deep melting. The difference $P\text{-}P_{DM}$ determines the velocity at which the melt front propagates into the wafer [5].

To obtain a single crystalline film the entire polysilicon region has to be melted to eliminate any sources of random regrowth. It was determined experimentally that for the best crystallization, the melt front should propagate only slightly into the Si substrate at the openings in the $SiO_2$. Deeper melting of the substrate causes distortions of the isolation oxide and an excessive redistribution of liquid silicon. Fortunately, it is possible to detect *in situ* the moment when the melt front traversing the thickness of the polysilicon film, reaches the isolation oxide. Single crystalline Si with a low defect density and passivated by an oxide contains few nuclei for melting. As a result the crystalline Si substrate can superheat by several degrees before it starts melting [6,7]. The superheating spike of 5-7°C is easily detected by a pyrometer monitoring the wafer temperature and indicates that the entire polysilicon has been melted. This signal activates the crystallization sequence. Typically, the power is dropped abruptly below the deep melt threshold $P_{DM}$ to reverse the direction of motion of the solid-liquid interface. The subsequent rate of cooling determines the velocity of the crystallization front.

The windows in the $SiO_2$ not only act as seeds for epitaxial crystallization, but also produce lateral thermal gradients necessary to grow epitaxial Si in the entire region between the seeding windows [2,7]. After crystallization there are no grain boundaries or subboundaries left in the film, and the dislocation density is about $5\times10^3$ $cm^{-2}$. In Fig. 3, a cross section of the wafer shows a region between two seeding windows. Dislocations are concentrated precisely in the center between two seeds, where two crystallization fronts meet. The crystalline quality over the rest of the area is excellent, as shown in Fig. 4. Since there is some mass transport during crystallization, as can be seen in Fig. 3, the wafer surface requires planarization before further processing.

Sidewall isolation can be achieved in three different ways, as shown in Fig. 5. The first configuration requires crystallization of non-planar films over Si substrates

with deep wells etched in them. We have obtained single crystalline films in such structures [3], but processing is more difficult than in the case of planar films. The other two approaches start with planar films, in which either vertical or V-shaped grooves are etched and the walls are then oxidized.

## FORMATION OF BURIED HIGH CONDUCTIVITY LAYER

Since many device designs in dielectrically isolated structures require a buried conductive layer adjacent to the isolation oxide, we have developed a unique method of doping silicon near the buried $SiO_2$/Si interface after recrystallization. The conventional method of forming the buried $n^+$ region in DI wafers relies on doping of Si from the surface, followed by oxidation to obtain what will eventually become the buried oxide. Since our films are melted, they can only be doped after resolidification, otherwise the dopants would redistribute rapidly in the molten phase. To avoid such redistribution, arsenic is implanted into the $SiO_2$ before deposition of the polysilicon overlayer. There it remains, essentially immobile during the entire processing sequence, since the diffusivity of high concentration As in the $SiO_2$ is $<10^{-14}$ $cm^2$/sec at 1400°C and the recrystallization cycle lasts about 2 min. After recrystallization the arsenic is outdiffused into Si next to the oxide, forming the desired buried conductive layer. However, it is difficult to achieve a low resistivity buried layer by diffusion alone, since at high concentrations As in $SiO_2$ is essentially immobile. We have discovered a much more efficient way of moving As out of $SiO_2$ and into Si, based on thermomigration of As-rich droplets in a temperature gradient [8]. When As is implanted into $SiO_2$ at a dose above $3 \times 10^{15}$ $cm^{-2}$ and the oxide is heated in the inert ambient, As precipitates into spherical inclusions which are stationary under isothermal conditions but drift toward the heat source if $\nabla T$ is present. By these means we can move the entire distribution of implanted As in one direction, toward the heat source, as illustrated in Fig. 6, until it reaches Si and conventional diffusion takes over. The drift in a thermal gradient is accomplished in the same lamp furnace that is used for melting and recrystallization. For this process however, the power is kept at or below the lower threshold $P_{TH}$, so that one face of the wafer is at 1300 to 1412°C and the other is lower by about 7°C. At 1400°C this provides a $\nabla T$ of 0.14°C/μm, sufficient to move the As at a rate of 2300 Å/h. In Fig. 7, two sets of curves are shown which demonstrate the influence of a temperature gradient on the formation of a conductive layer. The entire wafer processing sequence is shown schematically in Fig. 8.

## DEVICE PROCESSING

Electrical properties of the recrystallized thick films approach closely those of bulk Si. Undoped single crystalline films with resistivity of 40Ωcm have an electron drift mobility of 1400 $cm^2$/Vsec, minority carrier lifetime >5μsec, and a density of deep traps below $10^{11}$ $cm^{-3}$. Test devices prepared by twin tub 3.5μm CMOS process

perform as well in recrystallized wafers as in conventional DI or bulk epi Si wafers. Threshold voltages, transconductance, and leakage currents in the MOSFETs made in the recrystallized wafers match closely those in bulk Si. Yields of the recrystallized and DI wafers are similar but somewhat lower than in bulk epi wafers. Apart from the local undulations of the film thickness (see Fig. 3), which are removed by lapping and polishing, the wafers are flat to within 20μm across four inch diameter. Two views of a processed device wafer are shown in Fig. 9.

## SUMMARY

We have described the LEGO process for forming dielectrically isolated single crystalline thick Si films on single crystalline substrates. This method eliminates the polysilicon "handle" and the associated wafer warpage problems, reduces by a factor of ten the thickness of deposited polysilicon, and minimizes mechanical silicon removal. Wafers can be recrystallized rapidly in a lamp furnace, with throughputs up to 30 wafers/hour. Crystallization is well controlled and reproducible for planar films. In such films grooves must be etched to obtain lateral isolation. Crystallization of nonplanar films to obtain completely isolated crystalline Si tubs, similar to those in the conventional DI process, is possible but less reliable. Buried conductive layers can be obtained by releasing As dopant from the isolation oxide into Si, using a temperature gradient for more effective outdiffusion. Test devices demonstrate that the recrystallization method can compete with DI in performance and yield.

## ACKNOWLEDGMENTS

The results described in this paper would not be possible without active participation of many colleagues from AT&T Bell Laboratories facilities in Reading and Allentown, PA, and Murray Hill, NJ. We are especially grateful to R. P. Anand, R. A. Clapper, R. Lindner, D. J. Lischner, C. Y. Lu, R. L. MaSaitis, W. G. Meyer, B. W. Miller, L. Pfeiffer, McD Robinson, P. K. Roy, D. G. Schimmel, J. C. C. Tsai, L. O. Wilson, and K. W. West. The support of R. L. Batdorf, H. Basseches, A. Heller, and T. J. Riley is also appreciated.

## REFERENCES


[1] K. E. Bean and W. R. Runyan, J. Electrochem. Soc. **124,** 5C (1977).

[2] G. K. Celler, McD. Robinson, and D. J. Lischner, Appl. Phys. Lett. **42,** 99 (1983).

[3] G. K. Celler, McD. Robinson, L. E. Trimble, and D. J. Lischner, J. Electrochem. Soc. **132,** 211 (1985).

[4] G. K. Celler, L. E. Trimble, and L. O. Wilson, Mater. Res. Soc. Symp. Proc. **35,** 635 (1985).

[5] L. O. Wilson, G. K. Celler, and L. E. Trimble, J. Electrochem. Soc. **133,** 383 (1986).

[6] G. K. Celler, K. A. Jackson, L. E. Trimble, McD. Robinson, and D. J. Lischner, Mater. Res. Soc. Symp. Proc. **23,** 409 (1984).

[7] L. O. Wilson, and G. K. Celler, J. Electrochem. Soc. **132,** 2749 (1985).

[8] G. K. Celler, L. E. Trimble, K. W. West, L. Pfeiffer, and T. T. Sheng, Appl. Phys. Lett. **50,** 664 (1987).

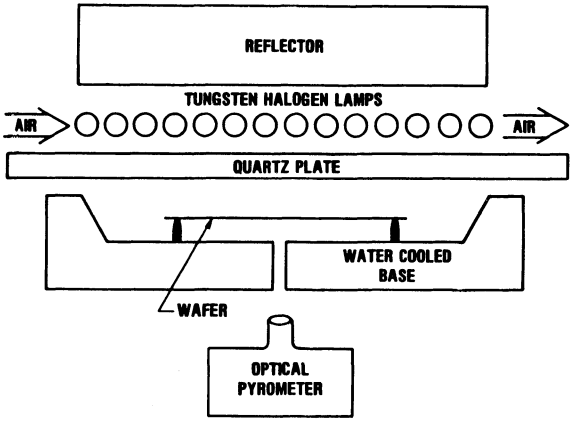



Fig. 1. A schematic view of the lamp furnace for controlled melting and recrystallization of silicon.

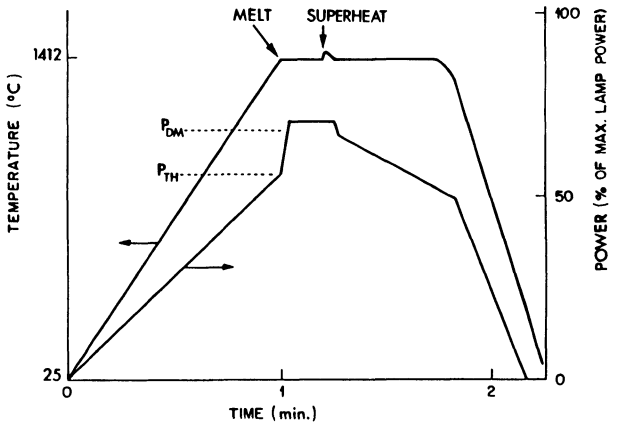



Fig. 2. Typical profiles of lamp power output and of Si wafer temperature vs. time.

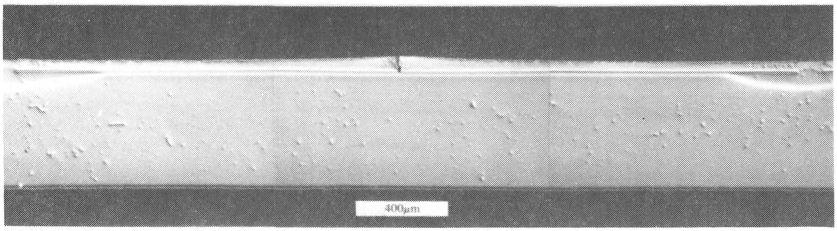



Fig. 3. Cross section of recrystallized Si film between two seed windows in the $SiO_2$, at far left and right. Dislocations, delineated chemically, are localized in a narrow collision region in the center.

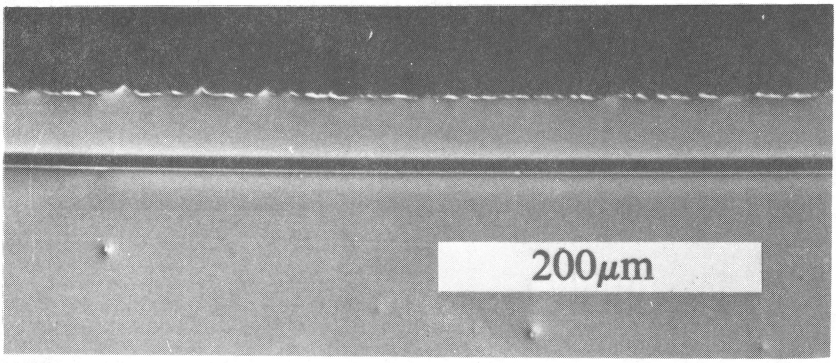



Fig. 4. Detailed view of the recrystallized Si film, the silicon substrate, and the isolation oxide.

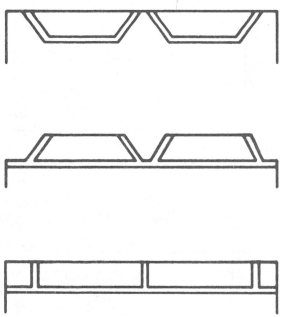


Fig. 5. Different schemes for sidewall isolation.

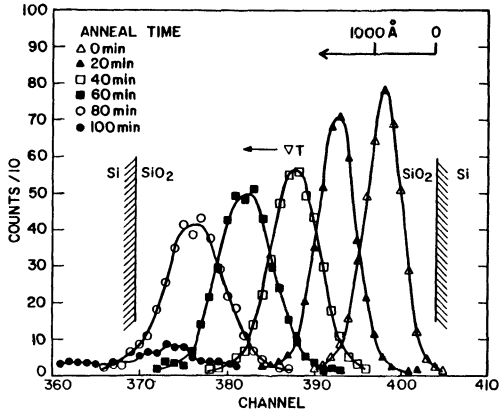



Fig. 6. Motion of the implanted arsenic peak inside the $SiO_2$ in a temperature gradient [8].

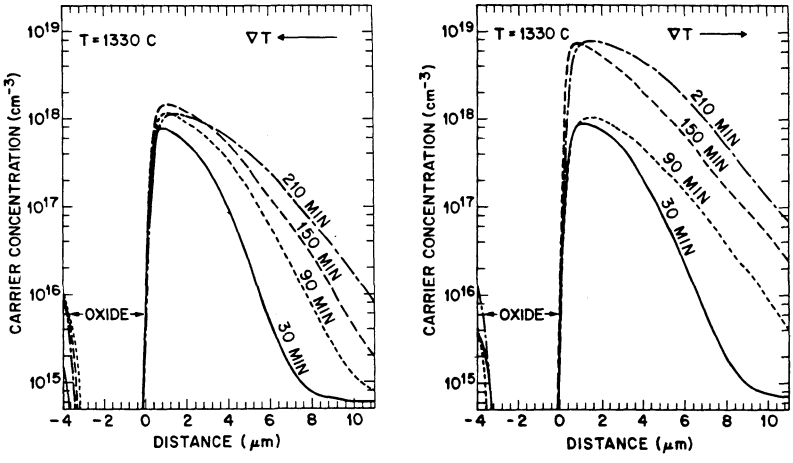



Fig. 7. Formation of a buried $n^+$ region in Si adjacent to the isolation oxide. $3\times10^{15}$ As/cm$^2$ was implanted at 100 keV into 4 μm thick oxide, of LPCVD oxide. the amount of As that outdiffuses from the $SiO_2$ depends strongly on the direction of the temperature gradient.

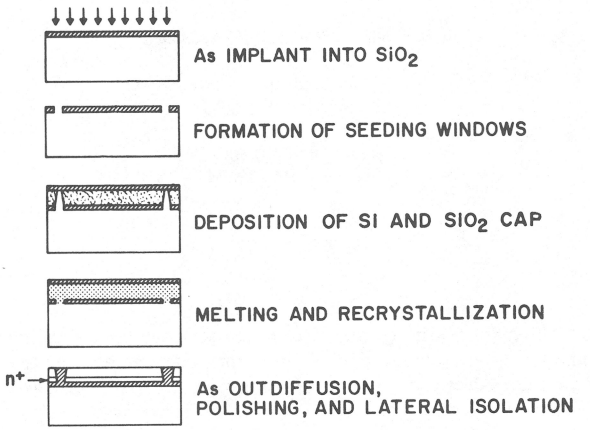



Fig. 8. Processing steps required to form a dielectrically isolated Si film with a buried $n^+$ region adjacent to the isolation oxide.

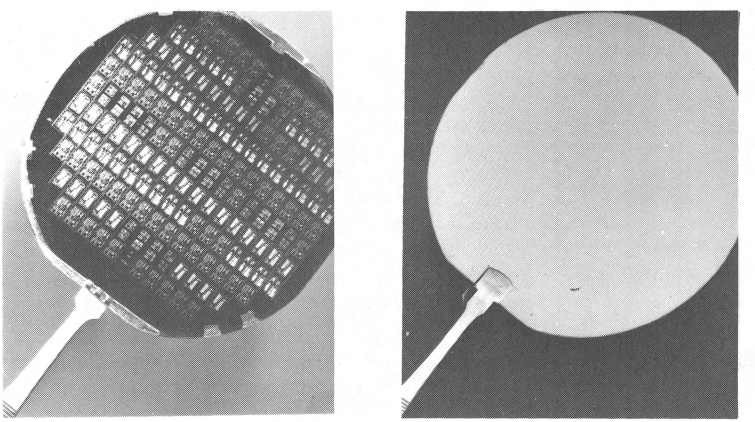


Fig. 9. Front and back views of recrystallized LEGO wafers with 3.5μm CMOS circuits.

Proceedings of The Electrochemical Society, PV 1987-13, 250-261 (1987)
DOI: 10.1149/198713.0250PV © The Electrochemical Society

# Evaluation of High Voltage ICs by Corona Charging

*R. B. Comizzoli* and J. W. Osenbach***

*AT&T Bell Laboratories
Murray Hill, NJ 07974

**AT&T Bell Laboratories
Reading, PA 19604

*ABSTRACT*

Many high voltage integrated circuits are sensitive to surface ions. The accumulation of net charge due to these ions over certain regions of the device results in decreased breakdown voltage or increased leakage current. The deliberate deposition of surface ions on a device from an atmospheric pressure discharge can be used to determine the surface ion sensitivity of devices. This technique is described and is shown to be useful in evaluating device designs and process variations and in failure analysis. The effects on surface ion sensitivity of variations in dielectrically-isolated tub depth, of field plate dimension, and of length of field-grading diffusions have been examined using this method. Three examples of the use of this technique for failure analysis are also presented.

## 1. Introduction

A useful electrical method for assessing the susceptibility of high voltage components and integrated circuits to surface-ion-induced breakdown voltage degradation has been described (1). The technique employs an atmospheric pressure, high voltage discharge (corona discharge) to generate and deposit gaseous ions upon the insulating surfaces of a device. The method is not destructive, as will be discussed below. Indeed, numerous useful applications for corona discharges have been developed in the areas of device passivation, defect detection, and insulator physics as well as for high voltage integrated circuit (HVIC) analysis(1).

The advantages of a rapid evaluation of the susceptibility of a HVIC to surface ion effects arise from the fact that surface ion failure modes are difficult to assess quantitatively. The charge density required for device failure is approximately $1 \times 10^{12}$ electronic charges/cm$^2$, which is below the normal sensitivity of most surface analytical methods. In addition, only a few monolayers of water are needed on the surface for the ions to be mobile. These surface ion effects(2-9) can lead to either reduced breakdown voltage or increased leakage current in both high voltage discrete devices and HVICs. The motion of surface ions laterally over the chip surface is a common means for this propagation, as shown in Figure 1. Here the surface ions cause the surface potential of the

insulator to approach that of some metallized portion of the chip. This is likely to occur when the surface ions are in contact with the metal at a location such as a bond pad or a pinhole or crack in the overlaying passivation layer. The vector addition of the applied electric field in the silicon and the electric field due to the insulator surface potential may lead to a total electric field that exceeds the silicon breakdown potential, as shown in Figure 1.

The minimization of such effects can be accomplished by several means. The electric field in the silicon can be reduced by increasing the distance between junctions, for example. This increases the device on-resistance, however, unless the device size is increased. Metal field plating and shielding can be provided to achieve a defined safe potential on the chip surface. Insulator thickness can also be increased to reduce the effect of the surface ion potential on the electric field in the silicon below. However, the compromises in favor of chip area and performance that must be made dictate that surface ion effects remain a significant failure mode in many high voltage devices. In addition, the presence of an insulator defect, such as a pinhole, can locally decrease the distance of the surface ions from the silicon and missing metal can reduce the effectiveness of field plates. Both effects can lead to surface ion induced failures in devices designed to be immune to such problems. Further, computer-based device design and simulation techniques do not normally take into account the possible presence of electrical charges on insulator surfaces. For all these reasons, it is useful to have a method that assesses device behavior in the presence of surface charges. In this report, we review the corona discharge procedure, present a simple model that relates the corona-deposited ion effects to failures induced by surface ionic charge drift, and describe application of the method to various aspects of HVIC technology. Our purpose is to illustrate the use of the corona technique for HVIC analysis, not to discuss in detail the results of the analysis as applied to designing and manufacturing HVICs.

## 2. Corona Method and Surface Charging Properties

In this section we briefly describe general properties of a corona discharge, the technique used for depositing ions on devices, and the effect of the sample geometry on the charge deposition. A more complete discussion is available in reference 1 and in the literature cited therein.

The corona is a high voltage discharge, maintained at atmospheric pressure, which both generates ions and provides the electrical field to move the ions to the surface of interest. For the present application the corona source may be either a plane array of fine wires or a single sharp point or multiple points. The wire array is useful for charging large areas, such as a device wafer, while a single point may be used for charging a single IC or component.

During operation, a DC potential of about 6,000 to 10,000V of either polarity is applied to the wires. Ions are generated in a narrow region very close to the electrode where a faint glow may be observed in a darkened room. For a negative potential on the wire or point, positive ions bombard the wire while free electrons are quickly captured by ambient molecules to form negative ions. The negative ions follow the field lines to regions of higher potential, namely the substrate, which is usually at ground potential. For a positive

potential on the corona source, electrons are attracted to the electrode and the positive ions follow the field lines to the substrate. Typically, several seconds are required to charge an insulating surface to a saturation surface potential.

The onset of corona is noted as a sharp increase in current from the high voltage electrode to the grounded electrode. The potential at which this occurs, called the starting potential, is a function of atmospheric conditions and the electrode geometry. For typical sharp points (radius of about 25 $\mu$m) and wires, the starting potential is about 3,000 to 4,000V at 760mm Hg. To achieve more uniform and constant corona current, systems are often operated at 6,000 to 10,000V. Below the starting potential the current to the electrode is usually less than 1 pA. At corona onset, the current increases by about six orders of magnitude to several microamperes. Sparking does not occur since the corona starting potential, at one atmosphere is well below the breakdown potential of the ambient ($\sim$30KV/cm) for the typical electrode spacing of several centimeters.

Above the corona starting potential a current of several microamps flows between the electrodes. Since air and other gases at atmospheric pressure are good insulators, the ion current carriers form a space charge between the electrodes. Thus, the current is proportional to the voltage squared, as is usually observed for space charge limited currents in gaseous or solid insulators. The flow of ions from the corona electrode results in a mass transfer detected by the observer as the "corona wind".

Since the current is carried in an insulating medium (air or other gas at one atmosphere) the impedance of the corona is very large. This large impedance is a great advantage when applying surface charges to electrically delicate thin insulators as found in semiconductor components or integrated circuits. The characteristic corona impedance prevents destructive currents from flowing through the thin insulators. In addition, the gaseous contact formed by a corona discharge to an insulator eliminates the requirement for a highly conducting surface contact, such as a metal plate. The corona ions have, therefore, a very low lateral conductivity on the insulator surfaces. This, too, prevents the flow of damaging currents. This non-destructive nature of the corona charging process applied to very sensitive devices (CMOS ICs) has been conclusively established(10).

In applying charge from a corona source to the insulating surfaces of a device it is necessary to consider the sample geometry and other factors. For monolithic IC wafers a plane array of wires spaced about 3 cm from the wafer, as shown schematically in Fig. 2a, will provide uniform charging of the wafer. The wafer substrate must be grounded. Relative motion of the wires in the plane of the wires relative to the wafer will enhance the charging uniformity(10). Since all metal on each device is connected to the substrate by a reverse or forward biased junction or ohmic contact, the metal is essentially grounded since the corona impedance is very large. For a packaged device, the chip surface must be exposed to the corona ions with all package leads grounded. Here, it is convenient to use a point source at about 3 cm from the chip surface, as shown in Figure 2b. The high voltage is applied to the corona electrode for about 10 seconds. Ions of sign given by the applied potential are generated and drift to the device surface where they deposit on insulator surfaces. To prevent the charge on the insulator surface from leaking away, the process is performed in dry ambient. Usually, relative humidity below 30% is sufficient. A device parameter of interest, breakdown voltage for example, is measured before and immediately after the charging process in the dry ambient.

The procedure is similar for dielectrically isolated (DI) devices; however, for DI wafers special precautions may be necessary since much of the metal is not connected to the substrate. Thus, it is usually necessary to charge one IC in a wafer at a time while the bond pads of the IC are connected to ground and all other ICs are shielded by a conductor mask.

The sample geometry normally limits the surface potential of the insulators on the IC when charged by the corona ions. The relevant geometry consists of the IC bonding pads and the surrounding grounded region, consisting of the bare silicon grid regions on a wafer or the grounded bond wires, cavity bottom, and bond lands of a packaged device. The close proximity of these grounded regions limits the maximum surface potential of the insulator regions. As ions accumulate on the insulator surfaces, the potential increases until a sufficient lateral electric field exists to deflect arriving ions to the grounded conductor areas. The maximum surface potential is a function of the chip dimension. For a square geometry, the relation between maximum surface potential and chip area has been determined(10). For insulator thickness such that the insulator breakdown potential is greater than the potential maximum set by ion deflection, the insulator potential is determined by ion deflection and for this reason is approximately constant across the chip surface(2). For most HVICs the insulator breakdown potential is greater than the ion deflection potential and calibration curves can be developed that relate the insulator potential to the device geometry. However, for thin insulators or very large circuits, leakage through the insulator may determine the surface potential. In either case, the chip surface potential can be determined approximately by measurement using a non-contacting feedback electrostatic voltmeter(10). Other parameters that determine the surface potential are corona electrode to sample spacing and corona potential(10). Ideally, the corona parameters should be adjusted to charge the device surface to a potential which equals the maximum potential difference normally applied to the device, and the effect on the device of both positive and negative ions should be determined.

Various techniques exist for removing the ionic charge from the chip surface. These include exposure to high humidity ambient, rinsing in ionic liquids, exposure to light of sufficient energy to generate photocarriers in the insulator, and baking at elevated temperature. The last method is usually preferred since it relaxes not only surface charge but also interface charges that may have been introduced by the corona charging process.

### 3. Effect of Surface Charge on Breakdown Voltage

The corona charge deposited on the device surface adds a perpendicular electric field at the silicon surface to the horizontal electric field due to the potential applied to the device. When all the metal regions and the substrate are grounded and the surface potential on the device is limited by ion deflection, the potential on the chip surface is approximately constant with position, but the charge on the surface will vary in proportion to the local capacitance, as shown in Figure 3. The perpendicular electric field at the silicon surface at any point can be calculated from the surface potential after corona charge deposition and the dielectric constants and thicknesses of the insulators above the silicon. The surface potential is known approximately from calibration curves or by measurement, as previously described.

When bias is applied to the device in the presence of the corona-deposited charge, a horizontal field $E_A$ is vectorially added to the perpendicular electric field $E_S$, in the silicon, as shown in Figure 3. The vector sum of these fields, $E_R$, is given by

$$E_R = (E_A^2 + E_S^2)^{1/2} .$$

The vector sum $E_R$ cannot exceed the breakdown potential of the silicon. In the absence of the field $E_S$ due to surface ions, the horizontal field $E_A$ due to the applied potential is limited to the silicon breakdown potential. Thus, the decrease resulting from surface ions in the maximum $E_A$ is given by

$$\Delta E_A = E_o - (E_o^2 - E_S^2)^{1/2},$$

where $E_o$ is the breakdown field value for the silicon. In principle, the field in the silicon due to surface ions, $E_S$, can be evaluated by applying Gauss' Law at the silicon-insulator interface. In practice, however, it is difficult to estimate the electric field in the insulator adjacent to the silicon since the insulator regions of HVICs are generally composed of several layers of different materials with widely varying conductivities and, therefore, the occurrence of unknown amounts of interface charge complicate the calculations. This problem, in fact, makes the inclusion of insulator surface charges in device design and modelling very difficult.

## 4. Some Applications of Corona Charging

### 4.1 Design Verification

The corona discharge method has been useful in studying the susceptibility of high voltage device design features to surface ion effects. Those aspects that have received the greatest attention are field plate dimension (distance from edge of opening in diffusion mask to edge of field plate in metal mask) and the effect of the depth of dielectrically isolated single crystal tubs on field plate requirements. As described previously(1), the reduction in breakdown voltage due to negative corona charging was determined as a function of field plate dimension. The results, shown in Fig. 4, permit optimization of the field plate dimension consistent with surface ion immunity and device area limitations. The depth of the dielectrically-isolated single crystal silicon tubs that are used in certain high voltage circuits determine diffusion times of certain device features. The resultant changes in lateral diffusion, in turn, may alter the effectiveness of a given field plate design. The corona discharge method was applied to determine the surface ion sensitivity of different tub depths. As shown in Table 1, the corona charge method using negative charge indicated definite differences related to tub depth for a given field plate design.

On some HVICs, an additional diffusion is used to provide a potential grading region. Increasing the length of this region by mask modification or by diffusion time will decrease the sensitivity of the device to surface ions, at the expense, however, of device area. Thus, it is important to choose the potential grading diffusion length precisely and corona charging with negative ions was used to determine the surface ion sensitivity of different potential grading diffusion profiles. As previously described for tub depth variation, corona

charging with negative ions resulted in breakdown voltage changes that were a function of the length of the potential grading, as shown in Table 2. The optimum length for acceptable surface ion sensitivity was chosen in this manner.

The breakdown voltage of a device observed after corona charging with negative ions is generally constant with time and does not exhibit walkout (a gradual increase in breakdown voltage due to charge injection into the oxide from the avalanche region). Thus, for a given device type and lot, the breakdown voltage values after negative corona charging have quite low scatter. Deviations from the mean value are in the direction of lower breakdown voltage and are often found to be related to dielectric or passivation defects. With positive corona charging, however, walkout is usually observed and it may be somewhat more difficult to determine the breakdown voltage precisely. The correlation of walkout with positive surface charge is related to the much greater injection efficiency into oxide of electrons as compared to holes.

### 4.2 Failure Analysis

Corona charging has proven useful in various failure analysis problems. In one case, special test ICs based on diffused MOS transistors were subjected to temperature-humidity-bias aging. After aging, several failures due to reduced breakdown voltage were found that were bake recoverable. A surface ion mechanism was not suspected initially since the test circuit design had been shown to be surface ion immune by corona charging. However, deposition of corona charge on the failed and recovered test samples did induce breakdown voltage reduction. Inspection revealed that localized corrosion had removed a portion of the aluminum field plate rendering the device sensitive to surface ions.

In another case, production devices were subjected to high temperature-bias aging. After aging, several failures were found due to high leakage currents. Initially, surface ions were suspected since failed devices recovered when annealed at room temperature for a few days. Two of these failures will be discussed. For each device, the section of the chip that caused the failure was determined by bench testing. The devices were then annealed at room temperature for a few days after which they were retested. They had recovered after this anneal. The devices were then subjected to both positive and negative corona charge. In each case negative corona charge created the same leakage failure mode as was observed after high temperature-bias aging. For both devices, the failure occurred in the same section as in the high temperature-bias stress test.

Visual inspection revealed local defects in both devices. Device A had a pinhole in the passivation layer next to a high voltage connection (Figure 5). During high temperature aging, negative ions accumulated at this defect because of Coulomb attraction between the positive metal connection and the negative surface ions. The negative ions that were attracted to this defect generated a vertical extrinsic field in the silicon, leading to reduced breakdown voltage as described above.

Device B had a hole in the oxide dielectric layer close to a high voltage connection (Figure 6). One of the low voltage bond pads is close to this defect. It was concluded that negative surface ions drifted out over the chip from the low voltage bond pad towards the high voltage line during aging. When the ions reached the local region of thin or missing

oxide, the electric field in the high voltage region of the silicon increased to the breakdown limit by the closer than normal approach of the surface ions.

## 5. Conclusion

A simple method for evaluating the effect of surface ions on HVICs has been described. The method involves the deposition of either positive or negative ions onto the surface of the device via a corona discharge. Several examples of its use in evaluating dielectrically isolated device designs have been discussed. Results have been presented that show that the length of the field plate, the tub depth, and the potential grading diffusion length have a significant effect on the sensitivity of the device to surface charges. Its usefulness as a failure mode analysis tool has also been discussed. It has been used to reveal that localized corrosion of the field plate on diffused MOS transistors render the device sensitive to surface charge as can passivation and oxide defects. Finally, a model has been presented that quantitatively shows how surface charges affect the breakdown voltage of HVICs.

## REFERENCES


1. R. B. Comizzoli, J. Electrochem. Soc., *134*, 424 (1987).
2. M. M. Atalla, A. R. Bray, and R. Lindner, Proc. IEE, *106*, 1130 (1959).
3. W. Shockley, H. J. Queisser, and W. W. Hooper, Phys. Rev. Letters, *11*, 489 (1963).
4. W. Shockley, W. W. Hooper, H. J. Queisser, and W. Schroen, Surface Sci., *2*, 277 (1964).
5. E. D. Metz, RADC Series in Reliability, Phys. Failure in Electronics, *2*, 163 (1964).
6. G. L. Schnable, E. S. Schlegel, and R. S. Keen, RADC Series in Reliability, Phys. Failure in Electronics, *3*, 108 (1965).
7. E. S. Schlegel, G. L. Schnable, R. F. Schwarz, and J. P. Spratt, IEEE Trans. Electron Devices, *ED-15*, 973 (1968).
8. E. S. Schlegel, R. S. Keen, and G. L. Schnable, 8th Ann. Proc. Reliab. Phys., 9 (1971).
9. W. Schroen, 11th Ann. Proc. Reliab. Phys., 117 (1973).
10. R. B.Comizzoli, J. Electrochem. Soc., *124*, 1087 (1977).

**Table 1**

| Tub Depth | Percent Decrease in Breakdown Voltage due to Corona Charging |
|---|---|
| D | 46 ± 2% |
| 1.2D | 60 ± 2% |

**Table 2**

| Relative Length of Potential Grading Diffusion | Per Cent Change in Breakdown Voltage due to Corona Charging |
|---|---|
| 0.8 L | − 30 ± 3 |
| 1.0 L | − 20 ± 2 |
| 1.5 L | + 5 ± 1 |

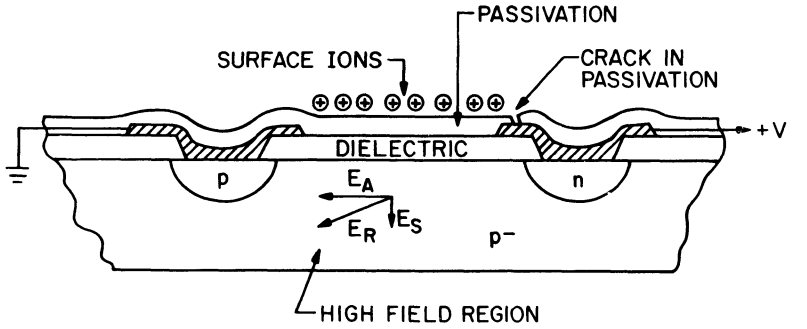



Fig. 1. Cross-section of high voltage diode showing ions which bias passivation surface to +V potential. The electric field of the surface ions, $E_S$, adds vectorially to the applied electric field $E_A$, giving a resultant field $E_R$, which may equal the breakdown field.

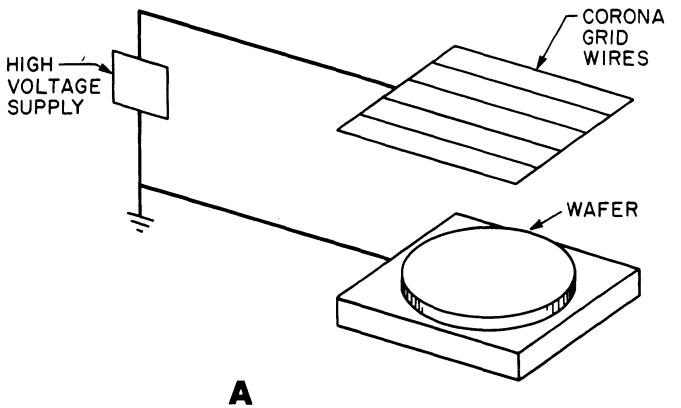
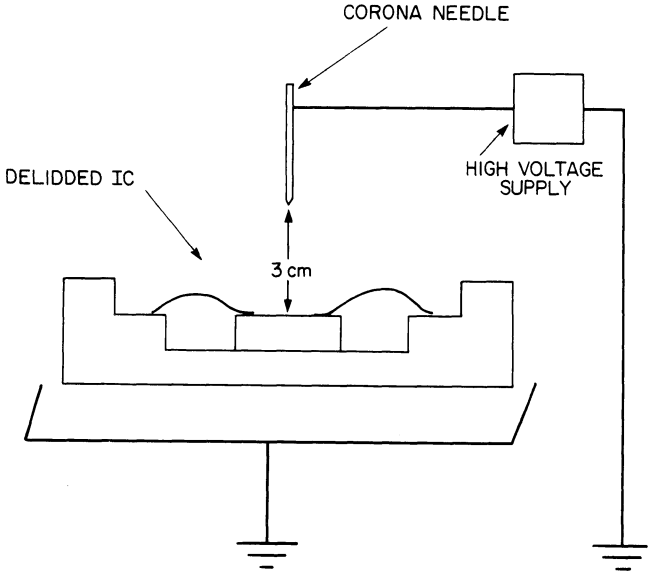



Fig. 2. Schematic arrangement for corona charging of: (a) a wafer using a plane array of wires; and (b) a delidded device using a single sharp point.




**2B**

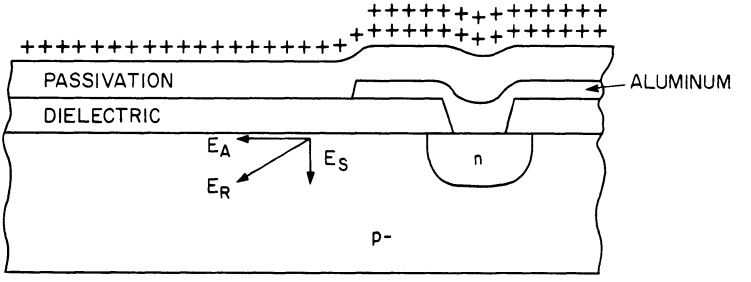



Fig. 3. Cross-section of a region of a device after positive ions have been deposited by corona charging. The ion density is greater over regions of high capacitance. Also shown is the vector addition of the applied electric field, $E_A$, and the perpendicular field, $E_S$, due to the surface charge.

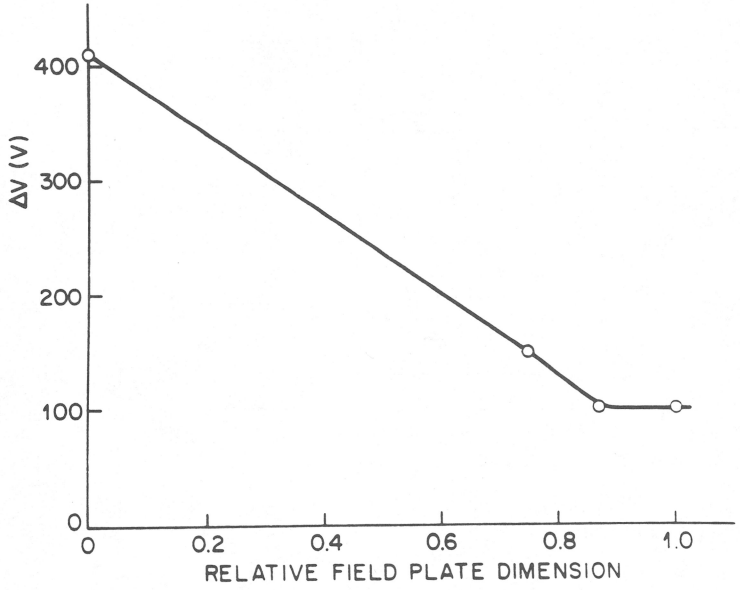



Fig. 4. The decrease in breakdown voltage, ΔV, due to deposited corona ions as a function of the relative field plate dimension for a high voltage test structure.

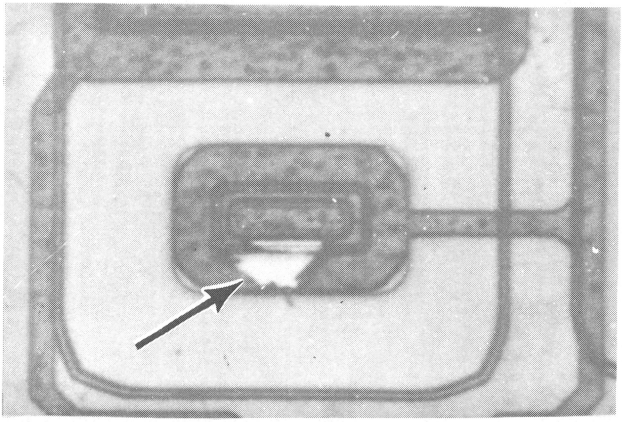


Fig. 5. Micrograph of device A showing pinhole in passivation layer over failing region of IC.

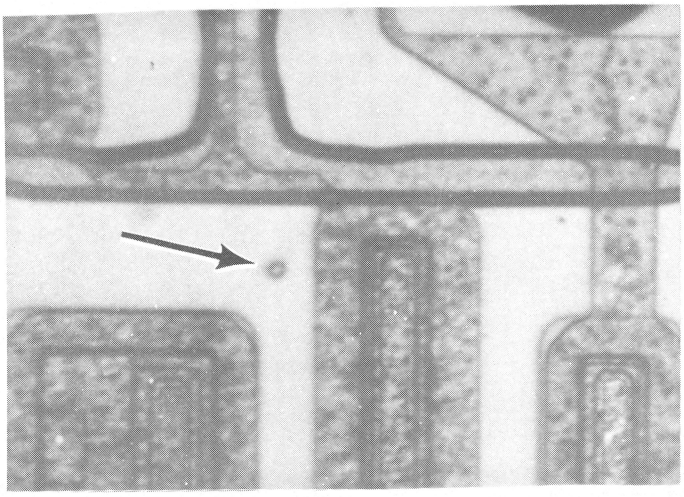


Fig. 6. Micrograph of device B showing defect in dielectric layer over failing region of IC.

Proceedings of The Electrochemical Society, PV 1987-13, 262-278 (1987)
DOI: 10.1149/198713.0262PV © The Electrochemical Society

# Field Dependent Conductivity in Semi-insulating Polycrystalline Silicon Films

*R. B. Comizzoli and R. L. Opila*

AT&T Bell Laboratories
Murray Hill, New Jersey 07974

*ABSTRACT*

A model based on Frenkel generation of carriers is presented to describe the electrical conductivity of semi-insulating polycrystalline silicon (SIPOS) films. This model considers both the electrical potential applied to the SIPOS and the potential due to the substrate. Potential screening by charge at the $SiO_2$ - SIPOS interface is related to location-dependent variations in the electrical potential distribution. The electrical potential as a function of position in the SIPOS film was measured with a scanning Auger microprobe and was found to be consistent with the model.

## 1. Introduction

Semi-insulating polycrystalline silicon (SIPOS) films have been used for passivation of various types of silicon devices. The SIPOS films in these applications act as a field-terminating layer, which prevents or reduces field-induced changes in the silicon charge density(1). SIPOS films have been used directly on the silicon for IC passivation(2-3) and for high voltage component passivation(4). SIPOS films above $SiO_2$ have also been proposed as a resistive voltage grading layer on high voltage discrete devices(5) and as a terminating layer for the field induced by surface ions on high voltage integrated circuits(6).

A critical consideration in applying such resistive films to ICs, and particularly high voltage ICs, is the additional device leakage current resulting from conduction through the film. Additionally, the SIPOS conductivity depends on electric field and can increase dramatically due to the substrate-induced field across the SIPOS(6-7). For example, the current in the SIPOS can change by four orders of magnitude when the silicon potential below the SIPOS changes by 250 V(7).

A brief summary of the substrate voltage effect on SIPOS conductivity follows. A more detailed discussion is contained in reference 7. A cross-section of a test structure in Fig. 1 shows a SIPOS film deposited over $SiO_2$ on a silicon wafer. Electrical contact is made to the SIPOS by a pair of parallel metal lines. Overlying the SIPOS there may be a layer of plasma-deposited silicon nitride passivation (SINCAP), but this is not shown in the figure. With a constant voltage $V_T$ applied between the metal lines, a large variation in current through the SIPOS is produced by changes in the substrate voltage. The change in SIPOS conductivity depends approximately exponentially on the square root of the electric field impressed in the SIPOS by the substrate potential difference with respect to the SIPOS(7). In the present work we studied the potential profiles in SIPOS between biased electrodes as a function of the vertical field induced by the substrate potential in order to develop a better understanding of the electrical conduction process at high fields in the SIPOS film.

## 2. Experimental

### 2.1 Sample Fabrication and Mounting

SIPOS films of 5000 Å ± 1000 Å thickness containing 17 atomic percent oxygen(8) were studied. Film deposition and annealing have been described previously(7). The sample is a parallel triple track of titanium-gold, with an electrode spacing of 18 $\mu$m and a line width of 10 $\mu$m, evaporated on 0.5 $\mu$m of SIPOS that is deposited on 1.2 $\mu$m of $SiO_2$ thermally grown on Si. No passivation layer was applied over the metallization. In cross-section, the structure is as shown in Fig. 1. After wafer sawing, the test devices were mounted in a chip carrier package and wire bonded.

To make the potential measurements, it was necessary to apply voltages to the device inside a scanning Auger microprobe (SAM). This was done as shown in Fig. 2, and the sample leads, insulated by glass tubing, were connected to vacuum feedthroughs. Electrical connections were made as shown in Fig. 1.

### 2.2 Analysis Method

The electrical potential of the SIPOS as a function of position was determined by measuring the energy shift of the Auger electrons, as previously described for silicon and aluminum(9-10). In Auger spectroscopy, a core hole is created in an atom by the energetic incident electron beam; the hole is filled by an electron from a higher atomic orbital and energy is conserved by the emission of another electron. The kinetic energy of the emitted Auger electron is characteristic of that specific transition. If the detector is grounded, the measured kinetic energy of the Auger electron will be shifted by the value of the electrical potential at the point of emission from the sample. Thus, the electrical potential of a point can be determined by measuring the change in the measured kinetic energy of a specific Auger transition.

The SAM is an ideal instrument for this measurement. Its small beam size, 0.5 $\mu$m in this case, allows the potential to be determined with high spatial resolution. In addition, spatial mapping of the Auger intensity can be performed. By programming the system to map the Auger intensity at the energy of a specific transition plus the value of a given potential, the equipotential line for that potential can be determined. For example, if a carbon Auger map were performed at a kinetic energy of 320 eV instead of the 270 eV observed for a grounded sample, the resultant map would be the equipotential line at −50 V. The incident electron beam should perturb the sample as little as possible. Thus a 3 kV electron beam was used to limit the extent of the volume excited and the number of charge carriers generated. A low incident electron beam current of 0.1 nA was used to limit the number of carriers generated and to avoid sample charging. Additional details on the technique have been described elsewhere(11).

### 2.3 Current-Voltage Measurements

Measurements of current through the SIPOS between two adjacent metal lines were made at constant line-to-line potential as a function of substrate voltage using a logarithmic picoammeter as shown schematically in Fig. 1. Line-to-line potential differences of 25 V to 300 V were applied, and the substrate potential was varied within the range ± 250 V, with the limitation that the potential difference between the substrate and the SIPOS contacts was not permitted to exceed about 300 V. In all cases, the leakage current through the $SiO_2$ film was negligible compared to the current between adjacent gold lines.

## 3. Results

### 3.1 Scanning Auger Microprobe

Auger spectra were taken of a region of SIPOS between a pair of tracks. One track was grounded, the other track was held at −250 volts, and the substrate voltage was varied from 0 to −250 volts. The shifts, V(x), in measured Auger energy of the Si (LVV, 90 eV), N(KLL, 380 eV), C(KLL, 270 eV) and O(KLL, 510 eV) peaks were determined for each value of substrate voltage, $V_S$. Good agreement, within a few percent, was found between the shifts for each Auger transition where the signal to noise ratio was sufficient. Once this agreement was determined, usually only the C (KLL) transition was used to determine the potential because its intensity was greatest. Adding +250 V to all of the applied potentials gave qualitatively similar results. Measurements were done to establish that an incident electron beam of 3 kV and a 0.1 nA current gave reproducible results from run to run and did not perturb the sample(11). Equipotential lines could be mapped as described in the previous section. Several series of equipotential lines for varying substrate voltages are shown in Fig. 3. The equipotential lines are not perfectly parallel to the tracks, and these variations were reproducible. The relative spacing of the lines and deviations from parallel will be discussed below.

### 3.2 Current-Voltage Characteristics

A typical I-V characteristic is shown in Fig. 4, where current is plotted as a function of substrate voltage, $V_S$, for a range of voltages, $V_T$, applied between the contacts. Note that for negative substrate voltage, the current increases approximately exponentially as the substrate voltage becomes more negative. For positive substrate voltage, the current is approximately constant. In some cases, the current increases slightly with more positive substrate voltage.

## 4. Discussion

### 4.1 Physical Description of Model

We propose here a physical model, based on field enhanced carrier release from localized states (Frenkel effect)(12), which explains, at least qualitatively, the substrate voltage dependence of current and the potential profile of the SIPOS surface as determined by the Auger microprobe. The nature of these localized states is not considered in this work. In the model, to be described in detail below, the total electric field generating the carriers via the Frenkel effect is given by the vector addition of two electric fields − one due to the substrate potential, $V_S$, and the other to the potential, $V_T$, applied between the two contacts to the SIPOS. Where the substrate is positive with respect to the SIPOS, a negative interface charge at the SIPOS − $SiO_2$ boundary terminates the electric field due to $V_S$ and no substrate potential effect on the conductivity is found. The Frenkel generated current is added to a current characterized by a constant conductivity (independent of electric field). This will be shown to agree with the current-voltage dependence found and can be related to a proposed model for SIPOS micro-structure. Each of the above aspects of the model will now be considered in greater detail.

### 4.2 Frenkel Carrier Generation

The barrier lowering in the Frenkel effect can be calculated for a simple one-dimensional model, as originally done(12). The potential energy of an electron trapped in a simple coulomb potential of a single point charge in an insulator or semiconductor in the presence of an applied uniform field E is

$$U = -e^2/4\pi\epsilon r - eEr\ .$$

The potential energy has a maximum at a distance $r_o$ from the point charge given by

$$r_o = (e/4\pi\epsilon E)^{1/2} , \tag{1}$$

where e is $1.6\times10^{-19}$ C and $\epsilon$ is the high frequency permittivity of the material. At the point $r_o$, the total energy of the electron with respect to the energy at an infinite distance is

$$U = e^2/4\pi\epsilon r_o + eEr_o . \tag{2}$$

If the zero energy level is taken to be at infinity in the absence of the uniform applied field E, then Eq. (2) represents the barrier lowering and is given by

$$U = (e^3E/\pi\epsilon)^{1/2} , \tag{3}$$

where we have substituted Eq. (1) into Eq. (2). The density n of free electrons originating from $N_T$ localized states per unit volume in the presence of an applied electric field is thus

$$n = N_T \exp(-U_o/kT) \exp[(e^3E/\pi\epsilon)^{1/2}/kT] ,$$

where $U_o$ is the energy of the localized state. The added conductivity $\sigma_F$ due to these n electrons is

$$\sigma_F = \sigma_o \exp[(e^3E/\pi\epsilon)^{1/2}/kT]$$

where $\sigma_o = n_o e\mu$, $\mu$ is the mobility, and $n_o = N_T \exp(-U_o/kT)$. If we add the conductivity $\sigma_F$ to the conductivity given by the free electrons of density N in the conduction band in the absence of an electric field we obtain for the total conductivity

$$\sigma = Ne\mu[1 + (n_o/N) \exp[(e^3E/\pi\epsilon)^{1/2}/kT]] . \tag{4}$$

The electric field in the SIPOS appearing in Eq. (4) is the magnitude of the vector addition of the fields due to the substrate potential, $V_S$, and the potential applied to the SIPOS contact, $V_T$. The field due to the substrate potential appears across both the $SiO_2$ and the SIPOS layers except where screening occurs as described below.

The effect of the substrate potential on the electric field in the SIPOS is a function of location in the SIPOS film. If we denote V(x) as the potential at the SIPOS surface as a function of distance, x, from the grounded electrode in a direction parallel to the substrate and perpendicular to the metallic contacts, then the potential drop, at position x, across the SIPOS thickness is given by

$$(1 + d_oK_S/d_SK_o)^{-1} [V(x) - V_S] , \tag{5}$$

where

$d_o$ = $SiO_2$ thickness (1.2 $\mu$m)
$d_S$ = SIPOS thickness (0.5 $\mu$m)
$K_o$ = $SiO_2$ static dielectric constant (3.8)
$K_S$ = SIPOS static dielectric constant ($\sim$ 6),

and the first factor in Eq. (5) is due to the capacitive division of the potential between the $SiO_2$ and the SIPOS. Defining E(x) as the electric field in the plane of the SIPOS, and assuming it is not a function of depth in the SIPOS layer, the total electric field at x in the SIPOS is

$$\{E^2(x) + (1 + d_oK_S/d_SK_o)^{-2} [V(x) - V_S]^2/d_S^2\}^{1/2} . \tag{6}$$

If expression (6) is substituted for E in Eq. (4) and numerical values for the physical constants and sample parameters are inserted, we obtain for the track to track current density j:

$$j = \sigma(x)E(x)$$

$$= Ne\mu E(x)\{1+(n_o/N)\exp 1.24\times10^{-2}[E^2(x)+1.6\times10^7[S(x)[V(x)-V_S]]^2]^{1/4}\}, \qquad (7)$$

in which $E(x) = -dV(x)/dx$, and we have used

$$e = 1.60\times10^{-19}\ C$$
$$k = 1.38\times10^{-23}\ J/^\circ K$$
$$T = 295^\circ K$$
$$\epsilon = 3.0\times10^{-13}\ F/cm,$$

where the value of $\epsilon$ is an estimate for the high frequency permittivity of our SIPOS film. The factor S(x), which varies from 0 to 1, we have inserted to account for potential screening in the SIPOS film.

The concept of potential screening is introduced to account for the non-symmetrical dependence of current on substrate voltage. Since the substrate voltage produces an increase in current only for negative values, some mechanism is required to shield the SIPOS film from the substrate potential when the substrate is positive with respect to the SIPOS. We postulate that a screening charge of electrons is formed at the SIPOS-$SiO_2$ interface for positive substrate potential with respect to the SIPOS. The supply of electrons is copious and thus no screening charge of holes is formed for the case where the substrate potential is negative with respect to the SIPOS potential. The screening is also a function of position x since, for a given V(x) in the SIPOS and a given $V_S$, $V_S$ will be greater than V(x) for some region of x, and smaller than V(x) for the other region of x. The parameter S(x) is defined to be unity for all x where $V_S < V(x)$. For x such that $V_S > V(x)$, S(x) has the value zero for the cases of total screening. We also introduce the concept of partial screening such that S(x) has a value greater than zero but less than unity for $V_S > V(x)$.

### 4.3 Solution for Current and V(x)

Since Eq. (7) is a transcendental differential equation, an analytical solution is not possible and a numerical solution was obtained. The first step in this procedure is to determine values for $Ne\mu$ and $n_o/N$. This was done by comparison with experimental results for current and for the SIPOS potential, V(x), measured by the SAM.

The quantity $N\mu$ can be determined from the current measured for low potentials applied between the two tracks and for substrate potentials that do not result in increased sample current. Thus, we select a condition $V_T = 25$ V and $V_S = 0$ for which a sample current $I = 1.9\times10^{-7}$ A was obtained, as shown in Fig. 4. In the region of $V_T = 25$ V, the current is approximately linear with $V_T$, and since there is little substrate potential dependence, field enhanced carrier generation does not occur. Thus, we can write

$$Ne\mu = I/Ewd = I\ell/Vwd ,$$

from which, by substitution of track length, $w = 0.2$ cm, SIPOS thickness, $d = 0.5\times10^{-4}$ cm, and track separation, $\ell = 18\times10^{-4}$ cm, we obtain

$$Ne\mu = 1.4\times10^{-6} \quad (\text{ohm-cm})^{-1} .$$

This value is the low field conductivity of the SIPOS film.

The ratio $n_o/N$ can be obtained from a measurement of the potential profile in a particular bias condition. As shown in Fig. 3, the SIPOS potential, V(x), is 40 V at $x_o = 7.6\times10^{-4}$ cm for $V_S=-250V$. Using a linear approximation for the electric field, $E(x_o) = 5.3\times10^4$ V/cm, substituting for $V(x_o)$ and $V_S$ in Eq. 7, and using the measured current of $1.6\times10^{-5}$ A for this bias condition, we obtain

$$n_o/N = 5.7\times10^{-6} .$$

Since all the constant factors are now specified, it is possible to obtain approximate solutions of Eq. 7 that specify V(x) by linear fitting procedures. After obtaining these solutions, they can be compared with the measured profiles of V(x) determined by the SAM. The fitting method has been described in detail.(11) This method allowed both j as a function of $V_S$ and the approximate shape of V(x) to be calculated without adjusting any variables. In Fig. 5(a), V is plotted as a function of x for $V_T=-250$ and $V_S = 0, -60, -125, -190$, and $-250$ with $S(x) = 1$ (no screening). The calculated current density, j, for $V_T = -250$ as a function of $V_S$ is also shown in Fig. 5(b) to be symmetric around $V_S = -125$ for the case of no screening. The experimental result from Fig. 4 is indicated by a dashed line.

The results shown in Fig. 6 were obtained with S(x) equal to 0.5 when $V < V_S$ and 1.0 when $V \geqslant V_S$. Here, the general shape of the calculated V(x) is in reasonable agreement with the data. The agreement between the derived and measured current densities is shown to be within a factor of 2 in Fig. 6(b). If screening is complete for $V < V_S$ and there is no screening elsewhere, the model predictions differ somewhat from the observations, as shown in Fig. 7. The V(x) curve in Fig. 7(a) (full screening for $V < V_S$) for $V_S = 0$ is linear. For the partial screening case shown in Fig. 6(a), the V(x) curve for $V_S = 0$ has a slight curvature and V(x) is more negative everywhere than the corresponding full screening case. This slight curvature can be seen in the data shown in Fig. 3. In the case of full screening, Fig. 7(b) shows the model prediction of a constant current density asymptote as $V_S$ becomes positive. On the other hand, the predicted current density in Fig. 6(b) increases slightly as $V_S$ becomes positive (i.e., where $V_S = 0$). This slight increase is evident in the data plotted in Fig. 4, especially for $V_T = -180$ V and $V_T = -25$ V. Thus, partial screening of the substrate potential appears to describe the results well.

It has been assumed that S(x) is independent of position when $V(x) < V_S$. However, S(x) will likely depend upon the number and depth of states that can accept electrons. Since trap states are known to exist at semiconductor-$SiO_2$ interfaces and their density of states can depend upon processing, it seems likely that there will be spatial variations in the density of trap states and, as a result, in the local screening function. Thus, regions where the equipotential lines are not parallel to the metal lines probably represent fluctuations in the local density of trap states. While local regions of effectively lower (or higher) conductivity will affect the observed j, the observed j will be an average (weighted to more conductive regions) of the entire track length. Sample to sample variations in screening have been implied in previous work on amorphous silicon(13). In that work, slow changes in current with time were observed, which we suggest are due to transient variation of the screening effect.

The same spatial variations in S(x) also explain the greater change of j with $V_S$ as predicted by the model compared to the data, as shown in Figs. 5(b), 6(b), 7(b). The particular locations chosen for potential profile measurements are statistically unlikely to be those regions where maximum currents are flowing. The ratio $n_o/N$ is derived from a V(x) curve determined at a particular location and does not reflect the average value of these parameters over the entire sample.

### 4.4 Comparison with Other Models

Another model, originally proposed by Cohen, Fritzsche, and Ovshinsky(14), has been used to describe the effect of transverse electric fields upon covalently bonded amorphous materials similar

to SIPOS (13,15-17). Briefly, this model assumes that the density of filled states and the density of unfilled states are symmetric about the Fermi energy ($\epsilon_F$). In addition, there is a gap of localized states centered around $\epsilon_F$. In the presence of a transverse electric field the delocalized states (bands) are bent. If the positive (negative) field is large enough to bend the bands below (above) the Fermi energy, electrons (holes) will fill the delocalized states and sample conductivity will increase. This model predicts low conductivity with small transverse fields and increasing currents with large transverse fields when the potential difference between electrodes is small. If the electrode potential difference is large, the conductivity should be low if the value of the substrate potential is between the electrode potentials. The conductivity will increase if the value of the substrate potential is either larger or smaller than that of both electrodes. In either case, the I-V curve should be approximately symmetric around the average of the electrode potentials (see Fig. 8a). Differences in the absolute values of the slopes of the arms of the I-V curves are then attributed to differences in electron and hole mobilities. In our samples, little increase in current was observed even at substrate voltages more than 100 V greater than the highest potential electrode (see Fig. 4).

Another consequence of the CFO model affects the shape of the V(x) curves. If $V_S$ is between the electrode potentials, there will exist a region where the delocalized states are not bent sufficiently to fill with carriers. In that region, the conductivity will be the lowest and, as a result, the electric field, E(x), (to maintain a constant j) will be the highest. This potential profile is sketched in Fig. 8(b). This behavior differs considerably from that observed in the present experiment.

On the basis of the shapes of the I-V and V(x) curves, it appears that our SIPOS films do not belong to the class of materials which display the CFO behavior. It should be pointed out, however, that by choosing appropriate electron and hole mobilities and an appropriate model for the densities of localized and delocalized states, the present data could be described by a CFO model. However, we prefer the proposed Frenkel model since it easily explains the observations and requires the derivation of only two parameters from the data, $n_o$ and N(18).

A symmetrical-Schottky-barrier (SSB) model has been previously proposed for SIPOS films(19). In that model the current is limited by a potential barrier between polysilicon grains, and by taking into account the grain morphology, good agreement between the SSB model and the current dependence on voltage and temperature was obtained. However, such a model cannot be used for our films since the SSB model predicts a decreasing slope for the I-V curve. In our data, the slope increases with voltage for both I-$V_T$ and I-$V_s$ characteristics. This difference in behavior may be related to the much lower oxygen content of the SSB SIPOS films(19).

### 4.5 Comparison with Higher Resistance SIPOS

In previous experiments(7) on aluminum contacted SIPOS films with an overlying plasma-deposited silicon nitride layer, it was found that the I-$V_s$ curves were approximately symmetric and that the minimum current was found at $V_S = V_T/2$. The data could be fit approximately by a simple Frenkel model which considered carrier generation only at the high field contact regions(7). Apparently, in the symmetric I-V SIPOS films the potential screening effect discussed above does not occur. This might be expected for a lower conductivity film in which electron and hole conductivities are approximately equal. The previous films with symmetric I-V curves did have conductivity lower than that of the present films by a factor of about 100 to 1000.

### 4.6 Suggested Physical Structure

In the present model we have *added* the Frenkel-effect contribution to a background current characterized by a constant conductivity. This is characteristic of a Frenkel effect in a semiconductor and can be distinguished from the same effect occurring in an insulator in which the background current can be neglected. In the former case, the substrate voltage produces a more limited change in total current than in the latter case. Thus, in the present data a change in current of about one order of magnitude was found, while, in the previous results(7) with more insulating films, the change in current was up to four orders of magnitude.

The additive nature of the Frenkel-generated current in the present model suggests a physical structure in which islands of insulator material are embedded in a semiconducting, continuous matrix. In such a system, a background current characterized by a constant conductivity flows through the matrix. At high fields, Frenkel generation of carriers in the insulating phase adds a current component that is field-dependent. A "mosaic" structure for SIPOS films formed in similar fashion to those of our study has been proposed(20). This proposed structure consists of a matrix of disordered silicon, which includes both Si microcrystals and particles of silicon oxide. The ohmic current would be expected to flow in the matrix region and in the silicon microcrystals, while the silicon oxide particles could provide a field-dependent conductivity via the Frenkel effect.

### 4.7 Reliability Implications

The field-dependence of the SIPOS conductivity requires care in the design of passivating structures for high-voltage devices. Since the electric field in the SIPOS due to the underlying silicon (substrate) potential increases the SIPOS conductivity, the potential profile across a SIPOS layer may not match the potential in the silicon below, when the silicon potential profile is linear or nearly linear. When the SIPOS to substrate potential difference is high, the conductivity will be higher than in those regions with lower potential difference. In the SIPOS region with higher conductivity, the electric field will necessarily be lower and the potential change will be more gradual, as found by the SAM profile measurements. In regions where the substrate potential is screened from the SIPOS, an almost linear potential profile may be expected.

The variations in potential screening found among various SIPOS regions on the sample surface imply that uniform passivation across a device surface may not be obtained. Thus, local increases in SIPOS leakage current or local variations in SIPOS potential profile may lead to device failure due to excessive leakage or to reduced breakdown voltage at a local site.

## 5. Conclusions

We have shown that the SAM can be used to measure the potential profile across semi-insulator structures. The conduction process in SIPOS films has been related to Frenkel generation of carriers, and this field-dependent process is additive to an ohmic current. The potential profiles obtained with the SAM are in reasonable agreement with those predicted by the model. The effects of potential screening by charge carriers at the $SiO_2$-SIPOS interface are discussed and related to variations in the potential profile depending on location.

**Acknowledgment**

The authors thank J. W. Osenbach for supplying the wafers, and the Murray Hill Wafer Separation Shop and the Murray Hill IC Packaging Shop for assembling the test devices. We also thank J. R. Mathews, H. R. Maxwell, Jr., and R. D. Plummer for useful discussions and J. D. Sinclair and G. W. Taylor for critical reading of the manuscript.

## REFERENCES

[1] R. D. Plummer, The Electrochemical Society Spring Meeting, May 1983, Extended Abstracts, Abstract No. 421, p. 659.

[2] T. Matsushita, T. Aoki, T. Otsu, H. Yamoto, H. Hayashi, M. Okayama, and Y. Kawana, Proc. 7th Conf. Solid State Devices, Tokyo, 1975. Suppl. to Japanese J. Appl. Phys. *15*, 35 (1976).

[3] H. Mochizuki, T. Aoki, H. Yamoto, M. Okayama, M. Abe, and T. Ando, Proc. 7th Conf. Solid State Devices, Tokyo, 1975. Suppl. to Japanese J. Appl. Phys. *15*, 41 (1976).

[4] R. Denning and J. White, RCA Technical Communication Reprint No. RE-24-5-11, originally published in RCA Engineer, 1979.

[5] F. A. Selim, IEEE Electron Device Letters *EDL-2*, 219 (1981).

[6] R. B. Comizzoli, unpublished.

[7] R. B. Comizzoli, Y. H. Wong, H. T. Weston, and J. E. Kohl, J. Electrochem. Soc. *133*, 1746 (1986).

[8] H. R. Maxwell, Jr. and W. R. Knolle in *Semiconductor Characterization Techniques,* P. A. Barnes and G. A. Rozgonyi, eds., The Electrochemical Society, p. 180 (1978).

[9] J. M. Patterson and M. C. Smith, Proc. of 1983 Int'l. Rel. Phys. Symp., p. 150 (1983).

[10] R. Pantel, F. Arnaud D'Avitaya, Ph. Ged, and D. Bois, Scanning Electron Microscopy 1982, II.

[11] R. B. Comizzoli and R. L. Opila, J. Appl. Phys. *61*, 261 (1987).

[12] J. Frenkel, Phys. Rev. *54*, 647 (1938).

[13] G. W. Neudeck and A. K. Malhotra, J. Appl. Phys. *46*, 2662 (1975).

[14] M. H. Cohen, H. Fritzsche, and S. R. Ovshinsky, Phys. Rev. Lett. *22*, 1065 (1969).

[15] D. F. Barbe, J. Vac. Sci. Technol. *8*, 102 (1972).

[16] A. K. Malhotra and G. W. Neudeck, Appl. Phys. Letters *24*, 557 (1974).

[17] M. Hamasaki, T. Adachi, S. Wakayama, and M. Kikuchi, Sol. St. Commun. *21*, 591 (1977).

[18] William of Ockham, *Dialogus* (1343).

[19] M. L. Tarng, J. Appl. Phys. *49*, 4069 (1978).

[20] M. Hamasaki, T. Adachi, S. Wakayama, and M. Kikuchi, J. Appl. Phys. *49*, 3987 (1978).

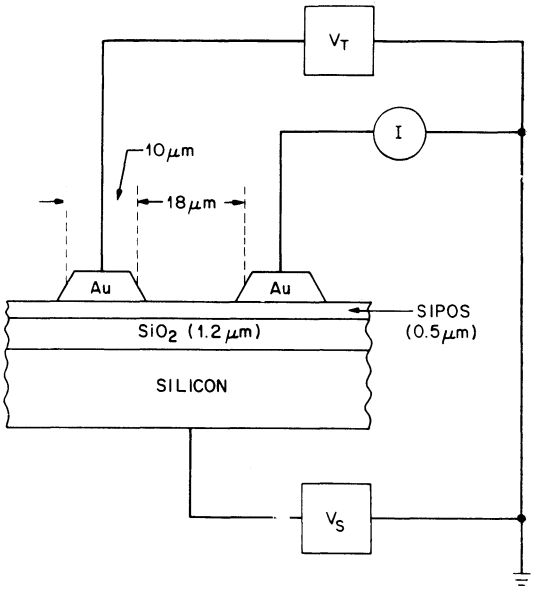



Fig. 1. Schematic cross-section of test device and of electrical connections.

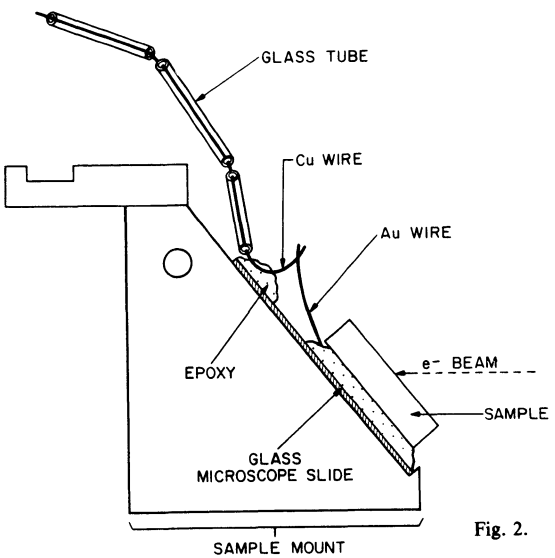



Fig. 2. Schematic of mounted sample.

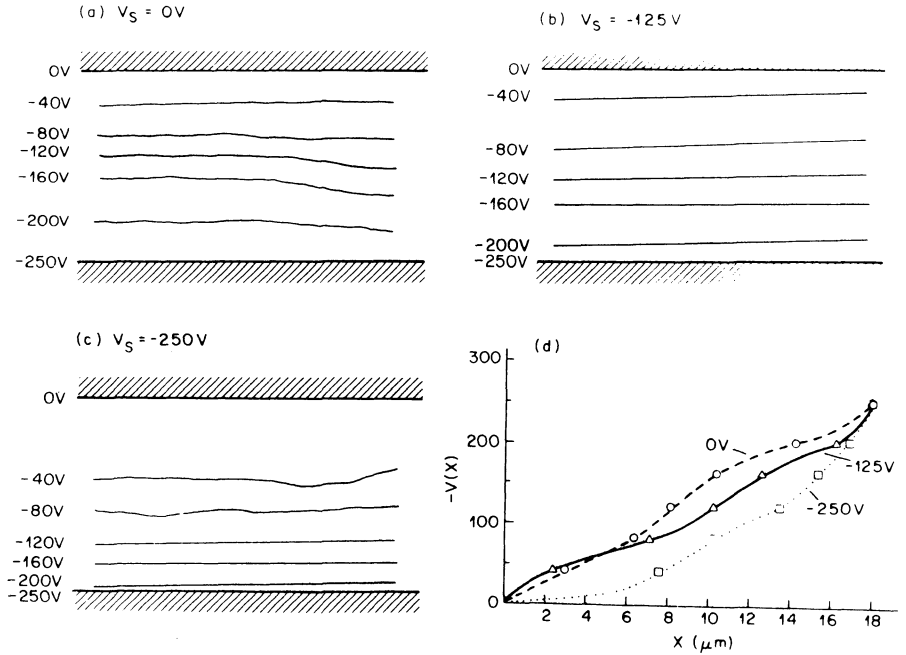



Fig. 3. Summary of equipotential lines for SIPOS sample determined from Auger maps for substrate voltages of 0, −125, and −250V in (a) through (c), respectively. Plot of measured surface voltage profile versus distance x from grounded electrode is shown in (d). Profile was taken at midpoint of region shown.

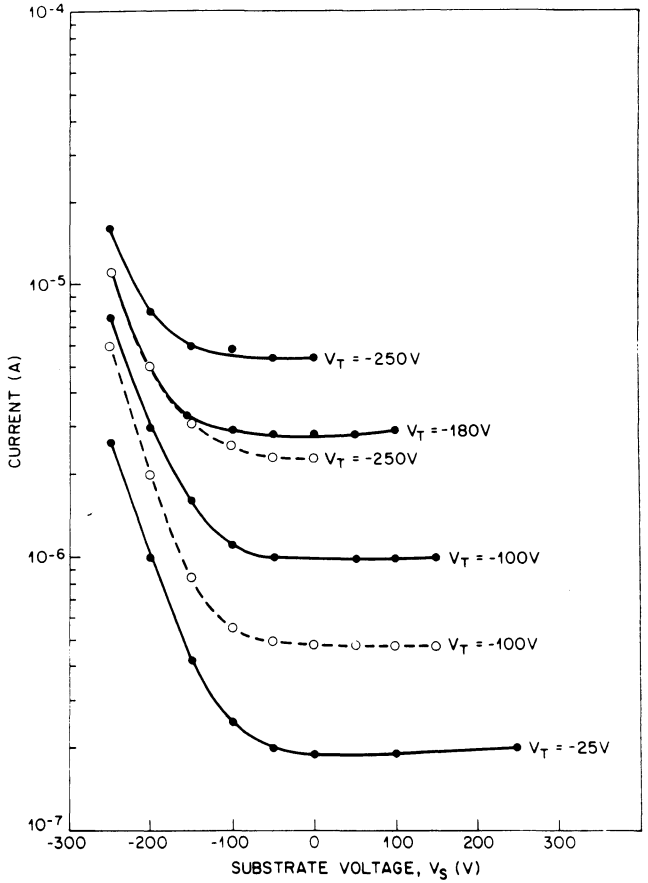



Fig. 4. Plot of current versus substrate voltage with $V_T$ as a parameter. Data is given for two samples distinguished by solid and dashed lines.

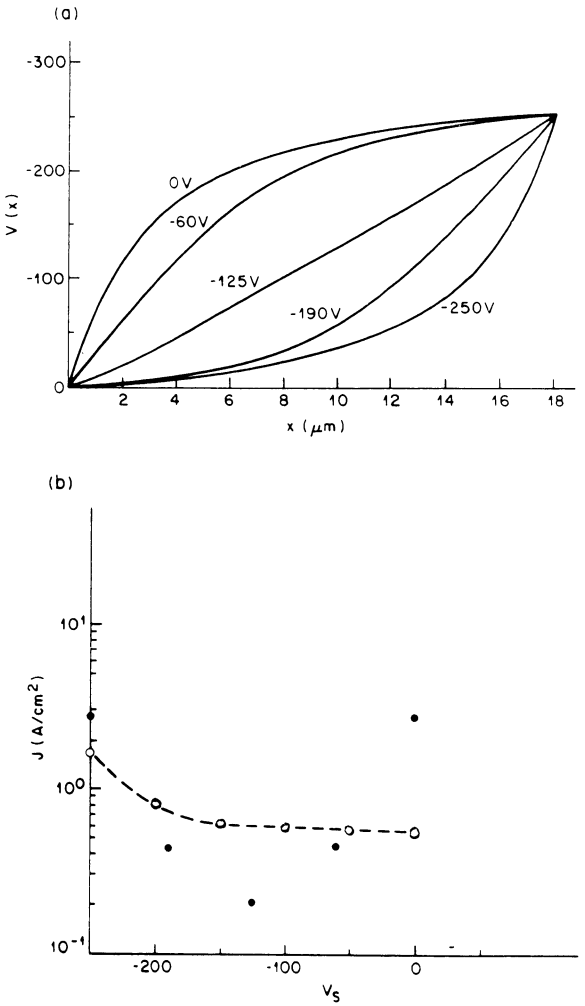



Fig. 5. Plot of calculated SIPOS voltage V(x) versus x in (a) for indicated values of $V_S$ with S(x) = 1 everywhere (no screening). Calculated current density is plotted versus $V_S$ as solid circles in (b), and measured current density is indicated by open circles.

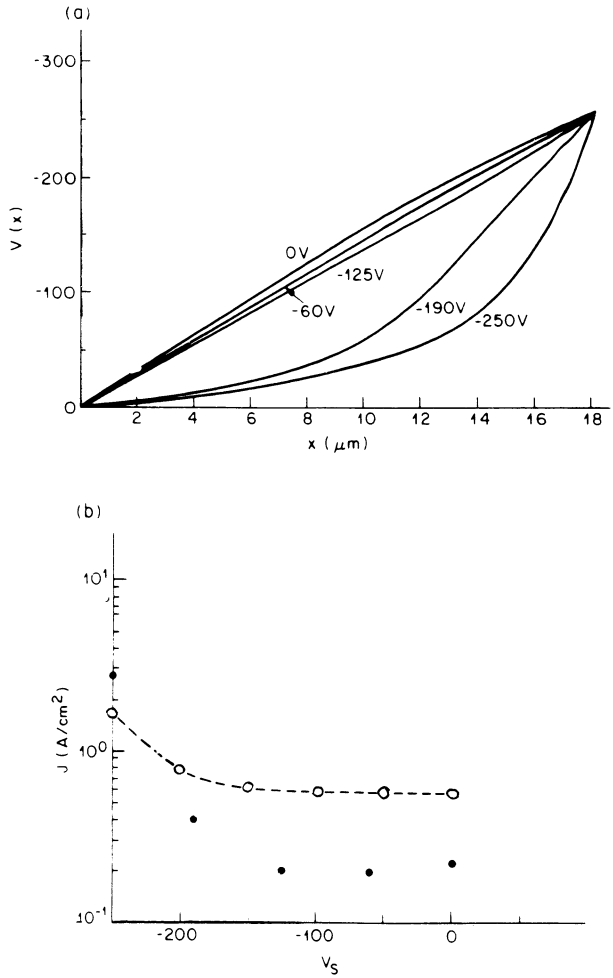



Fig. 6. Plot of calculated SIPOS voltage V(x) versus x in (a) for indicated values of $V_S$ with $S(x) = 0.5$ when $V(x) < V_S$ and $S(x) = 1$ elsewhere. Calculated current density is plotted versus $V_S$ as solid circles in (b), and measured current density is indicated by open circles.

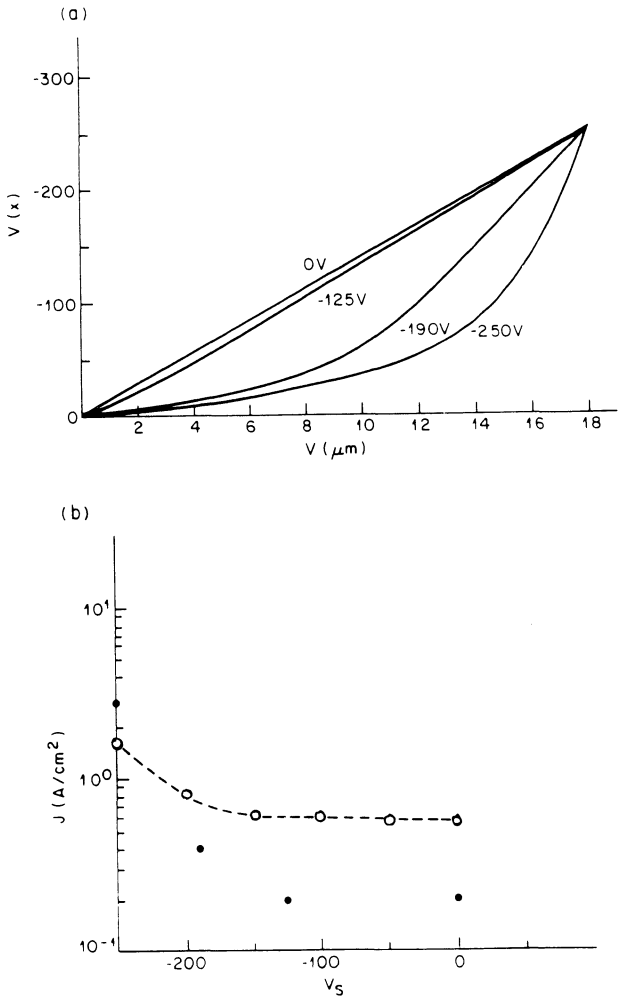



Fig. 7. Plot of calculated SIPOS voltage V(x) versus x in (a) for indicated values of $V_S$ with $S(x) = 0$ when $V(x) < V_S$ and $S(x) = 1$ elsewhere. Calculated current density is plotted versus $V_S$ as solid circles in (b), and measured current density is indicated by open circles.

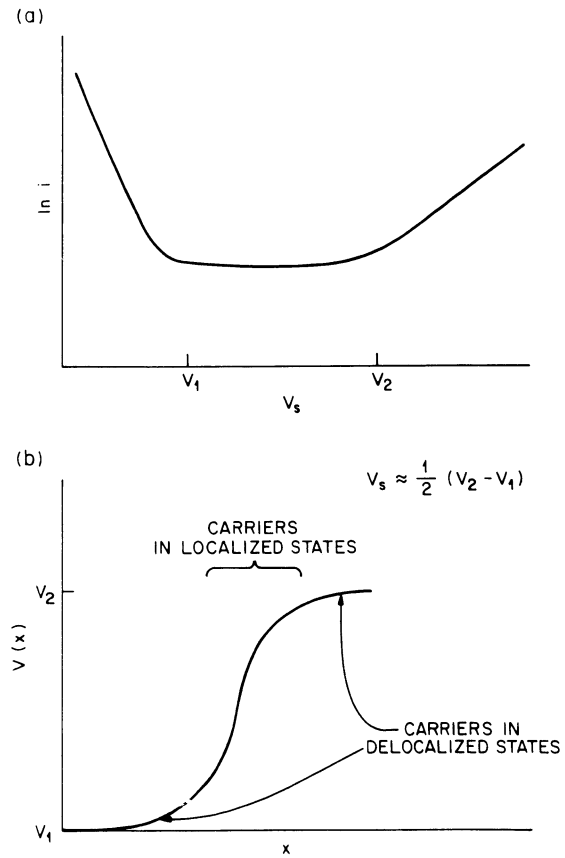



Fig. 8. Predicted current-voltage characteristic curve in (a) and voltage dependence on distance in (b) for the CFO model.

# LATERAL HIGH VOLTAGE DEVICES

## SESSION CHAIRMAN:

B. J. BALIGA
GENERAL ELECTRIC

Proceedings of The Electrochemical Society, PV 1987-13, 280-289 (1987)
DOI: 10.1149/198713.0280PV © The Electrochemical Society

# COMPLEMENTARY LIGTS FOR POWER IC APPLICATIONS

D.N. PATTANAYAK, T.P. CHOW, B.J. BALIGA AND M.S. ADLER

CORPORATE RESEARCH & DEVELOPMENT, GENERAL ELECTRIC COMPANY
SCHENECTADY, NEW YORK 12301

## ABSTRACT

The steady state and dynamic characteristics of Lateral Insulated Gate Transistors (LIGTs) are described theoretically and experimentally. The differences between N and P channel LIGTs are highlighted, and the suitability of LIGTs in power integrated circuitry is briefly discussed.

## INTRODUCTION

Complementary Lateral Insulated Gate Transistors (LIGTs)[1a-h] are attractive power switching devices for use in power IC applications due to their low forward drop and ease of integration. The latter is due to the fact that high voltage LIGTs can be fabricated using the RESURF principle in epitaxial layers and that the cathode, anode and gate terminals are accessible at the top of the wafer for easy interconnection to other high or low voltage devices. Device isolation can be accomplished either by junction isolation (JI) or by dielectric isolation (DI). LIGT is a complex semiconductor device that can be thought of as consisting of a lateral bipolar element and a MOS element, which is generally of the DMOS type. There is an inherent four-layer parasitic PNPN element that is normally in its off state as its emitter base junction is shunted at the surface. However, it can be triggered to its conducting state, resulting in a high current state of the device, at which point it acts like a lateral thyristor which can no longer be controlled by the MOS gate. In addition, there is a vertical bipolar element in LIGTs fabricated on junction isolated substrates, which allows substantial current to flow into the substrate which is generally tied to the cathode. This current component of the LIGT on JI is desirable as it does not take part in triggering the parasitic PNPN path; however, it brings in the possibility of lateral coupling between devices in a power IC environment.

Like vertical IGT/COMFETs[2], LIGTs are conductively modulated devices[3] and, thus, are relatively slow compared to the unipolar devices. The switching response of LIGTs reflects the compound nature of the LIGT device in that it consists of both MOS and bipolar junction transistor elements. While the MOS current dies off quickly, the current in the bipolar sections decays slowly exhibiting the characterstics of the turn off of an open base transistor, a storage

phase followed by a recombination phase. An interesting feature of LIGT is that it either consists of an N channel MOS and a PNP bipolar element, which is denoted as an N channel LIGT, or as a P channel MOS and an NPN bipolar element, which is denoted as the P channel LIGT. As will be shown later, because of this complementary composition complementary LIGTs have comparable forward drops. This is a desirable device attribute of LIGTs as complementary gate drive simplifies power IC design considerably.

In this paper, the basic device parameters, such as the avalanche breakdown voltage, forward drop, switching speed and latching current density for both N and P channel LIGTs, are discussed both theoretically, as well as experimentally. The numerical simulation results, as well as experimental results, are presented for a few typical LIGT structures with emphasis on the understanding of the steady state and dynamic behavior of LIGTs. The important results are summarized at the end.

## BREAKDOWN VOLTAGE

The off state of the LIGT can be analyzed effectively by ignoring the presence of the leakage currents and determining the electric field distributions. During the forward blocking state the anode base junction (J2 in Figure 1) is forward biased, and the voltage is supported by the junction (J1) consisting of the DMOS P base and the epitaxial N layer laterally and by the junction (J3) between the N layer and the substrate vertically. The charge in the N layer is chosen according to the RESURF principle[4], so that the surface fields are reduced and the breakdown occurs at the bulk junction. The field distributions prior to avalanche breakdown are shown in Figure 2. The peaks in the lateral electric field occur at the junction J1 (see Figure 2(a)) and at the gate electrode edges. The vertical field through the anode region is shown also in Figure 2(b). The breakdown, in this example, is occurng at the bulk rather than at the surface. It is clear from this example that a certain minimum thickness of the lightly doped substrate is needed to support the desired voltage and, similarly, a minimum lateral drift length. This defines the device geometry to a great extent for a given breakdown voltage design. The channel length can be made as small as possible, and we chose it to be about 2 to 3 microns. The anode region should be surrounded by a buffer layer to prevent vertical punchthrough between the substrate and the anode. There is a basic difference between the breakdown voltage of N and P channel LIGTs which stems from the asymmetry of the breakdown of the corresponding PNP and NPN bipolar transistor element. From a very simple analysis[5] it can be easily deduced that the ratio of the N and P channel LIGT breakdown due to the common emitter breakdown of the bipolar elements will be approximately given by

$$\text{VBCEO for NLIGT/VBCEO for PLIGT} = (\beta\text{NPN}/\beta\text{PNP})^{(\frac{1}{n})} \qquad [1]$$

where n is an adjustable parameter ranging from 1 to 5 for silicon. Since the right hand side of Eq. [1] is greater than 1, the breakdown of N LIGTs will be in general greater than the corresponding P LIGTs. This is borne out in practice. The breakdown voltage of N and P channel LIGTs fabricated on heavily doped epitaxial substrates is shown in Figure 3. The breakdown voltage of N LIGTs is about a factor of 1.4 times greater than the P LIGTs.

## STEADY STATE CHARACTERISTICS

The LIGT structure during its on state can be veiwed as a bipolar transistor whose base is being driven by a MOS channel. From a simple equivalent circuit it can be shown that the anode current Ina for an N channel LIGT on JI can be written as[1d]

$$Ina = Inmos * (1 + fln * \beta lp + (1 - fln) * \beta vp) \quad [2]$$

where fln denotes the fraction of base current feeding the lateral bipolar transistor whose current gain is denoted by $\beta$lp. The current gain of the vertical bipolar element is denoted by $\beta$vp, and Inmos denotes the N MOS channel current. In a similar fashion the anode current in a P channel LIGT is given by

$$Ipa = Ipmos * (1 + flp * \beta ln + (1 - flp) * \beta vn) \quad [3]$$

The various parameters in Eq. [3] are denoted in a corresponding way to those in Eq. [2]. On comparing Eqs. [2] and [3], it is clear that, since the PMOS channel current is smaller than the corresponding NMOS channel current and the current gain of NPN transistor is generally greater than that of PNP transistor, the forward drops of N and P channel LIGTs can be comparable to each other. In fact, as can be seen from the forward current voltage characteristics of simulated complementary LIGTs with buried layer, shown in Figure 4, the current handling capability of the P channel LIGT is better than that of N channel LIGTs. This analysis has been experimentally verified, as seen by the forward drop characteristics of complementary LIGTs fabricated on lightly doped epi on heavily doped substrates, as shown in Figure 5.

A substantial amount of current flows into the substrate in LIGTs on JI, especially on heavily doped substrates. The substrate current for both N and P channel devices fabricated on heavily doped substrates can be as high as 50 to 80% of the total device current. The percentage decreases with increase in current level, the percentage being higher for P channel than for N channel LIGTs. The substrate current can be reduced by employing a lightly doped substrate for which case the substrate current can be reduced by a factor of four to five from the values mentioned above. The substrate current is, thus, quite substantial and, for some power IC applications, it may be very undesirable. The substrate current can,

however, be totally eliminated by using DI substrates. In LIGTs on DI, the current conduction is exclusively lateral. The current flow paths of a simulated N channel LIGT structure on DI is shown in Figure 6 at a forward drop of 2.5 volts and gate drive of about 14 volts above channel threshold voltage. The current flow path shows the device current distribution from the anode to the cathode. In this example about 0.096 A/cm of current is flowing between any two adjacent lines. The current crowding at the anode and the channel is obvious. A significant amount of current is flowing in the P base and P+ region of the device. It is this hole current that forward biases the DMOS source junction at a sufficiently high current density, resulting in latchup. For this structure, latchup occurs at a current density of about $100A/cm^2$. The latch up in LIGT on DI can be supressed by including a buried layer, and simulation results confirm the effectiveness of a buried layer in combating latch up. However, in applications in which a common cathode is desired, it pays to have the substrate current component. Firstly it increases the total device current and, secondly, the substrate current does not participate in triggering latch up, as it does not flow through the DMOS P base region. As has been mentioned earlier, the current handling capability of LIGTs on DI will be lower than that of LIGTs on JI. This can be seen from the simulated I-V characteristics of LIGTs on JI and DI shown in Figure 7. In this example a buried layer is used to suppress latch up. Other effective ways exist to suppress latch up in LIGT; and several techniques, such as surface shorts, etc., are discussed in Reference (1d). In addition to forward drop, the switching speed of LIGTs is an important parameter, and the mechanism of conductivity modulation of the drift regions that lowers the forward drop increases the turn off time as the electron-hole plasma must now be removed before the current in the LIGT device ceases to flow. The turn off dynamics of complementary LIGTs are discussed next.

## TURN OFF DYNAMICS OF LIGT

The turn off dynamics of LIGTs are rather interesting, as they consist of several individual device elements, each having its own dynamics. Before describing experimental results, the results of computer simulation showing transient current and carrier distributions during device turnoff will be discussed to elucidate the LIGT turn off behavior, which will provide a basis for analyzing the experimental results. As is well known, the turn off dynamics are controlled by the external load circuit. In order to simplify computer simulation, the device turn off is achieved by first turning off the bias on the MOS gate, keeping the voltage across the anode fixed. This is not strictly true and we will, thus, have some errors in the initial phases of turn off. Once the gate voltage is turned off, the anode voltage is increased in a manner close to resistive turn off. The LIGT device structure is the one shown in Figure 1. The turn off waveform is shown in Figure 9. One can see the storage phase followed by an exponential decay phase. The high level lifetime used in this

simulation is several microseconds and clearly the turn off time is much shorter than the high level life time. A rather important phenomenon is the jump in the vertical bipolar current component during the initial MOS current drop following gate turn off. This is due to charge redistribution and transient increase in the bipolar current gain due to reduction in the base width. This is shown in Figure 8 where the electron concentration through the vertical PNP bipolar transistor is shown as a function of time and voltage. At the steady state just prior to gate turn off, the base collector junction is forward biased and the current induced base width is about 24 microns. The low current base width of this device is only 4 microns. This implies that the vertical bipolar transistor is in quasi-saturation and that the current through the device is essentially controlled by the external load resistor. The slight sloping in the current is due to increasing device resistance in time as more and more voltage is supported in the collector regions from which minority, as well as majority carriers, are removed. The reduction in the effective base width with time is clearly seen in Figure 9. The current in the device decreases due to back injection of the trapped majority carriers of the base; the time constant of the back injection process is roughly related to the transit time associated with the diffusion process of carriers from the base into the anode contact. Carriers are, of course, decaying by the recombination mechanism, but due to the fact that the base width is small compared to the ambipolar diffusion length, the characteristic time constant is determined more by diffusion rather than by recombination[6]. In Figure 10, the vertical electric field component is shown at time T=426 nanosecond when the device is in quasi-saturation and the field is supported in the collector region. After the quasi-saturation phase is over, the collector base junction supports voltage and the electric field peak moves to the collector base junction region. This electric field distribution appears similar to the one shown in Figure 2 where the current in the device is neglected as one would expect. In order to emphasize the two-dimensional nature of current flow in LIGT, the current flow lines for a P channel LIGT just before turn off and halfway through turnoff are shown in Figure 11. There is substantial current flow to the substrate during on state of the device, and the turn off of LIGT awaits the disappearance of this current component, as discussed earlier. The experimentally observed turnoff waveforms are shown in Figures 12(a-d). The turn off waveform in Figure 12(a) is for an N channel LIGT structure that is fabricated on lightly doped substrate. The effect of the large collector resistance is reflected in the large storage phase of about 2 microseconds. The jump in the substrate current is clearly seen. The current voltage turn off waveforms of the same LIGT structure fabricated upon epitaxial P-/P+ substrates is shown in Figure 12(b). The storage phase is much reduced to about 600 nanoseconds.

Several interesting observations are in order. Note the increase in the substrate current upon removal of gate voltage as discussed earlier. In Figure 12(c) the MOS and the lateral bipolar currents are

separate (by means of a special test device). The anode current waveform does not show the abrupt MOS current fall, as it is masked by the increase in the bipolar current components. Thus, caution must be observed in identifying the initial drop in the device current to the MOS channel current. Even the lateral current component that consists of the MOS channel current and the lateral bipolar current is masked by the jump in the lateral bipolar current, as can be inferred by looking at both Figures 12(b) and 12(c). The current voltage turnoff waveforms for a P channel LIGT with about 5% surface short[1d] shows similar features discussed already. The turnoff time is about 2 microseconds compared to the NLIGT turn off time of about 1 microsecond. This is related to longer transit time for holes compared to electrons. The turnoff times will in general be related to current levels and external circuit loading. Moreover, the turnoff times can be shortened by killing the lifetime of carriers through electron or protron irradiations, which will not be discussed here[7].

## CONCLUSION

The steady state behavior and dynamic characteristics of complementary LIGTs are presented with an emphasis on the basic understanding and suitability of LIGTs for power IC applications. The present generation of LIGTs show very favorable current handling capability due primarily to conductivity modulation, but for the same reason are rather slow. Both N and P channel LIGTs can carry about 100-150 A/cm$^2$ of current density at a forward drop of 2 volts and blocking voltages of about 400-500 volts. The switching speeds are in the range of 1-2 microseconds, which can be further reduced at the expense of increased forward drop through lifetime killing methods. The substrate current in these devices can cause potential problems in power IC applications, but this problem can be solved by fabricating LIGTs on dielectric substrate. The LIGT with structural and process enhancements has the potential of serving power IC as the lateral MOS structure has served the signal IC.

REFERENCES


1. a) M. Darwish and K. Board, Electron Lett, Vol.20, p. 520, 1984.
   b) R. Jayaraman, V. Rumennik, B. Singer and E.H. Stupp, IEDM Tech Dig., p. 258, 1984.
   c) D.N. Pattanayak and M.S. Adler, Proc. 43rd Annual Device Research Conference, Paper 6B5, June 1985.
   d) A. Robinson, D.N. Pattanayak, M.S. Adler, B.J. Baliga and E. Wildi, IEDM Tech Dig., p. 744, 1985.
   e) T.P. Chow, D.N. Pattanayak, B.J. Baliga and M.S. Adler, Device Research Conference, 1985.
   f) D.N. Pattanayak, A.L. Robinson, T.P. Chow, M.S. Adler, B.J. Baliga and E. Wildi, IEEE Trans. Electr. Dev. ED-30, p. 1956, 1986.
   g) P. Gough, M. Simpson and V. Rumennik, IEDM Tech. Dig. 1986, p. 218.
   h) J. Sin, C.A.T. Salama, L. Hoe, ibid, p. 222.

2. B.J. Baliga, M.S. Adler, P.V. Gray, R.P. Love and N. Zommer, IEDM Tech. Dig., 1982, p. 264; J.P. Russel, A.M. Goodman, L.A. Goodman and J.M. Neilson, IEEE EDL-4, p. 63, 1983.

3. See Reference 1(f) for detailed simulation results showing conductivity modulation in LIGT.

4. J.A. Appels and H.M.J. Vaes, IEDM Tech. Dig., 1979, p. 238; E.J. Wildi, P.V. Gray, T.P. Chow, and H-R Chang, IEDM Tech. Dig., 1982, p. 268.

5. R.M. Warner, Jr. and B.L. Grung, Transistors, Wiley-Interscience, New York, p. 565.

6. M. Byczkowski and J.R. Madigan, Journal of Appl. Phys., Vol. 28, 1957, p. 878.

7. To be published.

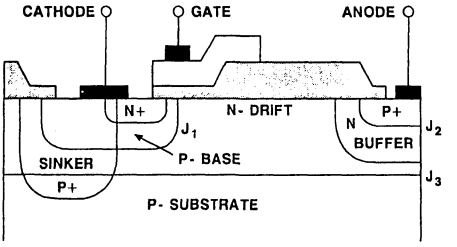



Figure 1. 2D schematic diagram of a lateral insulated gate structure.

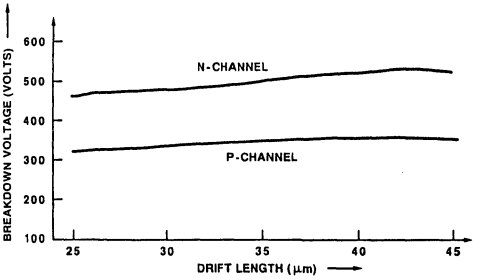



Figure 3. Breakdown voltage of N&P channel LIGTs.

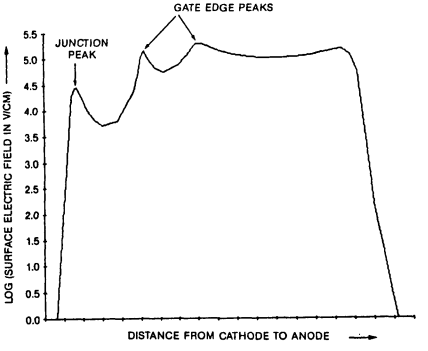



Figure 2a. Lateral surface electric field.

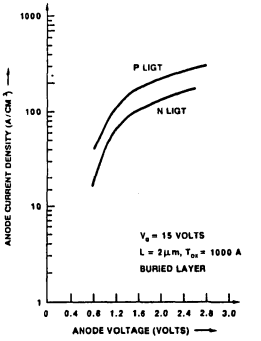



Figure 4. Comparison of N&P LIGT forward characteristics.

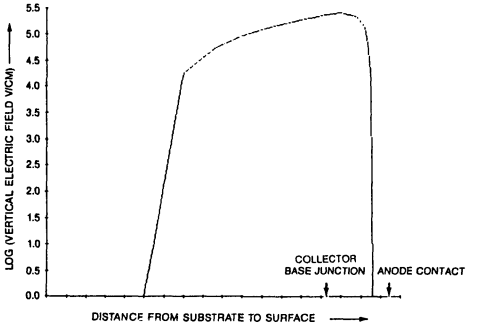



Figure 2b. Vertical electric field through anode region.

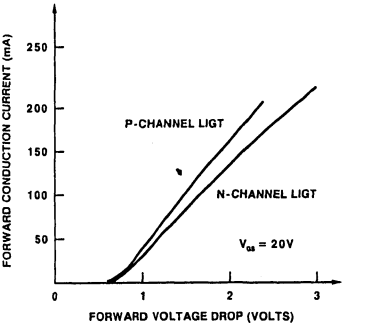



Figure 5. Forward drop characteristics of experimentally fabricated LIGTs.

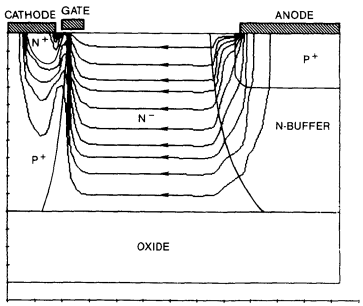



Figure 6. Current flow lines in LIGT on DI.

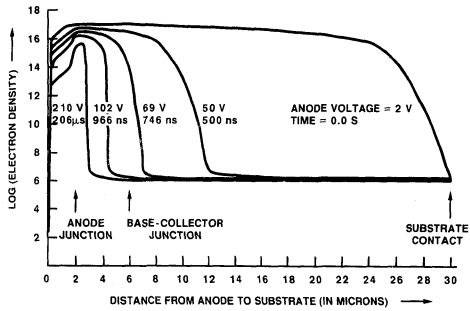



Figure 9. Transient base widening effect in LIGT.

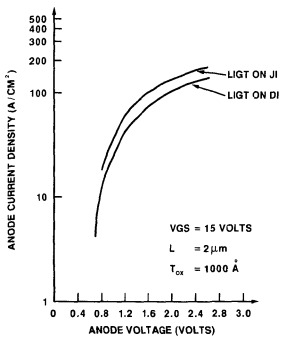



Figure 7. Current voltage characteristics of LIGT on JI & DI with buried layer.

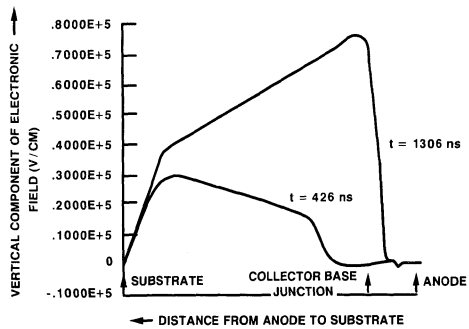



Figure 10. Shift of electric field peak with time in LIGT.

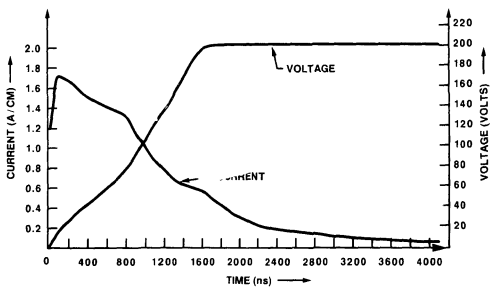



Figure 8. LIGT turn-off waveform (transient 2D simulation).

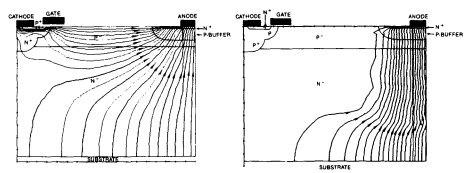



Figure 11a. Current flow lines prior to turn off inside a P-channel LIGT.

Figure 11b. Current flow lines at halfway point to device turn off inside P-channel LIGT on JI.

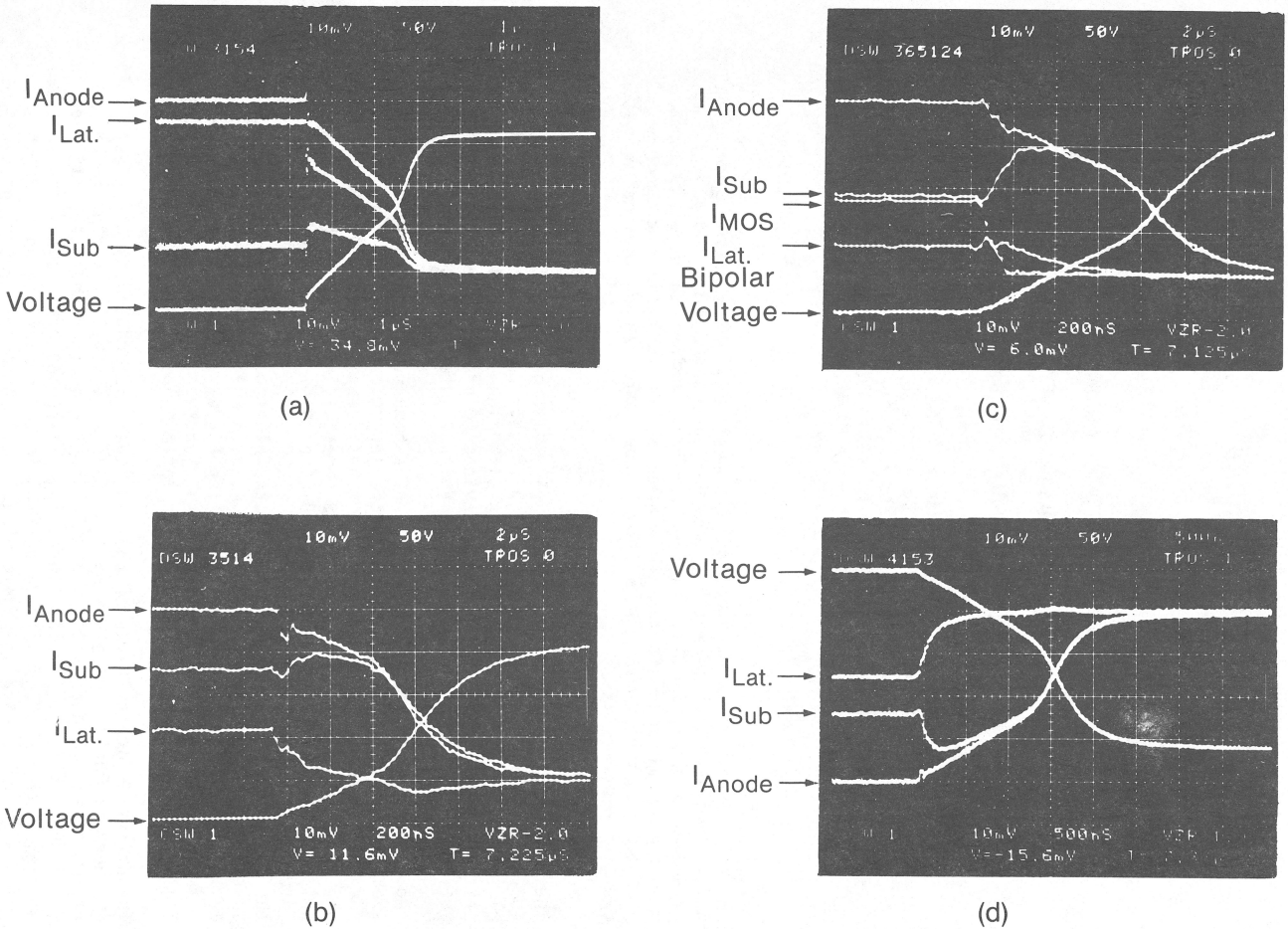



**Figure 12. Turn off wave forms of LIGTs.**

Proceedings of The Electrochemical Society, PV 1987-13, 290-294 (1987)
DOI: 10.1149/198713.0290PV © The Electrochemical Society

# MODELING AND OPTIMIZATION OF LATERAL HIGH VOLTAGE IC DEVICES TO MINIMIZE 3-D EFFECTS

Hamza Yilmaz
Research and Development Engineering
Semiconductor Business Division
General Electric Company
Research Triangle Park, NC 27709
(919) 549-3551

*Abstract: High Voltage blocking capability of the RESURF or Lateral Charge Control (LCC) devices are strongly junction curvature dependent. A new charge model has been developed to translate 3-D curvature effect into 2-d plane. Existing 2-D computer program in conjunction with this new model has been utilized to model and optimize the LCC devices for high voltage IC's. Theoretical predictions of this model are within 10% of the measured results.*

The Reduced Surface Fields (RESURF) [1], also called Lateral Charge Control (LCC) [2], technique has enabled high voltage IC's combining control electronics on the same silicon chip with high voltage driver devices. It is critical to optimize high voltage devices in order not to compromise the performance and density of the High Voltage Integrated Circuit (HVIC).

Two dimensional (2-D) cross-section of a high voltage lateral diode as an example is shown in Fig. 1. The drift length and impurity concentration in the substrate and in the drift region has been investigated 2-D analytically [1], experimentally [2], [3] and 2-D numerically [4], [5], [6]. However, prior studies have neglected the 3-D effects on the surface electric field (breakdown voltage capability) of the LCC device. As illustrated in Fig. 2, the curvature of the $n^+$-drain/collector electrode (3-D region) enhances the electric field at the $N^-n^+$ junction at both ends of the enclosed LCC device. Thus, breakdown voltage of the LCC devices optimized through 2-D simulation will be limited by the $n^-n^+$ junction curvature. The electric field enhancement factor, $F_C$ is calculated by using 3-D charge control model.

The effective drift length of the 3-D region is reduced by the electric field enhancement factor and given as $l_{eg} = l_C/F_C$. The drift length of the 3-D region of an LCC high voltage device, $l_{eg}$ is shorter than the drift length, $l_C$ of the 2-D drift region. Thus, $l_{eg}$ limits the breakdown voltage of the device. The 3-D LCC drift length, $l_{eg}$ in 2-D computer program [7] has been used to optimize high voltage device. The 3-D charge control predictions in conjunction with 2-D numerical simulation are within 10% of the experimental results as shown in Fig. 3.

The $n^-n^+$ junction curvature effects are reduced based on 3-D charge control model by i) larger $n^+$- radius as shown in Fig. 4 (a) and ii) longer drift length at both ends of the $n^-n^+$-junction as shown in Fig. 4(b). If $n^+$-radius is large, $l_{eq}$ is close to 2-D drift length, $l_c$. The required drift length of the 3-D region $l_c$ as a function of the drift length, and $n^-n^+$junction radius is calculated and shown in Fig. 5. The required $l_c$ increases with decreasing $n^-n^+$ junction radius.


[1] J.A. Appels and H.M.J. Vaes, "High-Voltage Thin Layer Devices (RESURF DEVICES)", Technical Digest 1979 IEDM, pp. 238-241.

[2] E.J. Wildi, P.V. Gray, T.P. Chow, H.R. Chang and M.E. Cornell, "Modeling and Process Implementation of Implanted RESURF Type Devices," Technical Digest 1982 IEDM, pp. 268-271.

[3] E.J. Wildi, T.P. Chow, M.S. Adler, M.E. Cornell and G.C. Pifer, "New High Voltage IC Technology," Technical Digest 1984 IEDM, pp. 262-265.

[4] S. Colak, B. Singer and E. Stupp, "Design of High-Density Power Lateral DMOS Transistors," Power Electronics Specialists Conference 1980, pp. 164-167.

[5] S. Colak, "Effects of Drift Region Parameters on the Static Properties of Power LDMOST," Trans. IEEE Electron Devices, Vol. ED-28, No. 12, December 1981, pp. 1455-1466.

[6] K. Board and M. Darwish, "LDMOS Transistors with Implanted and Deposited Surface Layers," IEE Proceedings-I, August 1985, pp. 177-180.

[7] M.S. Adler, V.A.K. Temple, A.P. Ferro, and R.C. Rustay, "Theoretical Bases for Field Calculations in Multi-Dimensional Reverse Biased Semiconductor Devices," Solid State Electronics, 25, 1982, pp. 1179-1186.

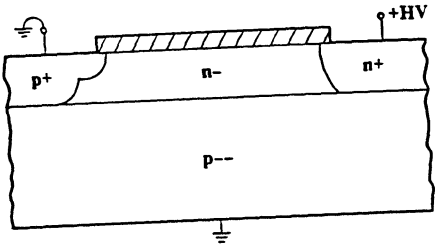



Figure 1 — 2-D cross-section of a high voltage LCC diode.

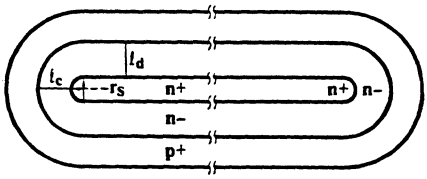



Figure 2 — Top view of a LCC HV diode showing 3-D n- n+ junction curvature at both ends of the n+- diffusion stripe.

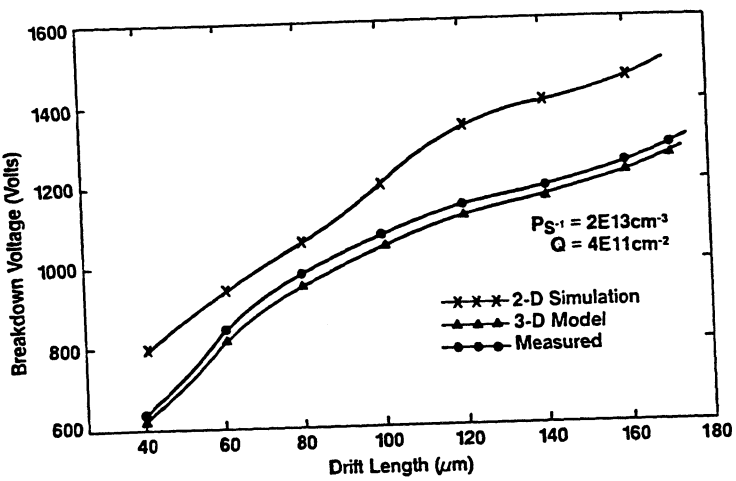



**Figure 3 — Breakdown voltage of a 1200V diode for HVIC as a function of the 2-D drift length. The measured results matches well with the 3-D model.**

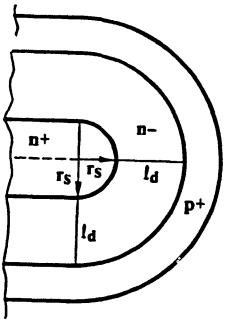



Figure 4(a) — LCC HV diode with larger n+- radius.

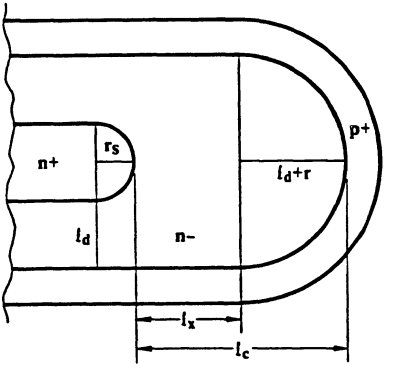



Figure 4(b) — LCC HV - diode with small n+- radius, but longer drift length at end of the n+- diffusion stripe.

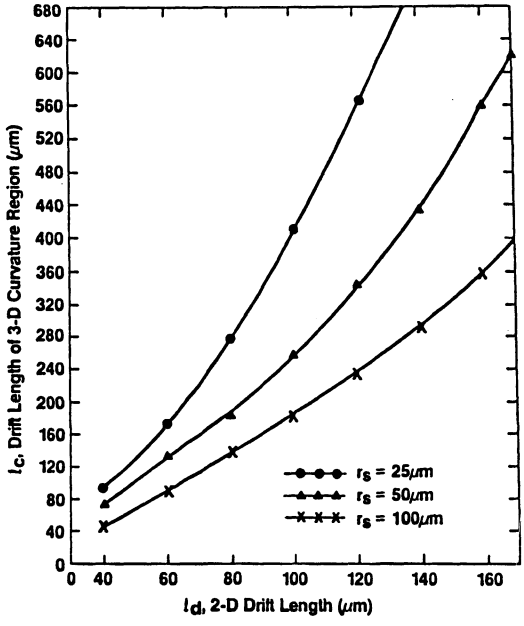



**Figure 5 — The calculated drift length of the 3-D curvature region as a function of the 2-D drift length and the radius of curvature of the enclosed n+ region.**

Proceedings of The Electrochemical Society, PV 1987-13, 295-309 (1987)
DOI: 10.1149/198713.0295PV © The Electrochemical Society

# DC AND TRANSIENT ANALYSIS OF LATERAL INSULATED GATE CONDUCTIVITY MODULATED TRANSISTORS

Mohamed N. Darwish and M. Ayman Shibib

AT&T Bell Laboratories
2525 North 12th Street
Reading, PA 19612-3566

*ABSTRACT*

Lateral Insulated Gate Bipolar Transistors (LIGBT) are power switching devices that can be easily integrated in silicon planar technologies (junction and dielectric isolation). Analysis of these devices require two-dimensional numerical solution of the underlying transport problem. DC and transient analyses are reported on lateral structures and in particular those using the "resurf" technique to optimize breakdown voltage and increase latch-up current level, at which gate control is lost. Results confirm that latch-up current increase is due to a vertical parasitic PNP action. Transient analysis is used to study both conventional and shorted anode devices during turn-off process. Experimental results are also reported on special test structures corroborating the theoretical results.

## *INTRODUCTION*

Recently there has been a growing interest in Lateral Insulated Gate Bipolar Transistors (LIGBT) [1-4]. LIGBT is a power switching device that can be easily integrated in both junction and dielectric isolation technologies. The device is therefore attractive for high voltage and power IC switching applications. It combines the desired features of MOS high input impedance, high breakdown voltage capability that can be optimized by the RESURF technique [5], and low on-resistance by conductivity modulating the drift region [6,7]. A schematic diagram of the basic device is shown in Figure(1-a). Since in such a structure the anode can be easily accessed from the surface, shorted anode devices can be easily fabricated in existing planar technologies [3] as can be seen in Figure(1-b). The device however can latch because of a parasitic p-n-p-n thyristor inherent in the structure thus the gate control is lost.

In this paper two-dimensional numerical simulations are presented and used to understand the device behavior at both on-state and during turn-off transient process for both conventional and shorted anode structures. These results provide the needed insight into the device operation. Furthermore, a more flexible model is presented for mixed mode device-circuit simulation. Experimental results of devices fabricated using dielectric isolation technology are also presented.

*DC CHARACTERISTICS*

In the on-state under steady state conduction the LIGBT(Figure 1-a) cathode and substrate electrodes are grounded and the anode electrode is connected through a load to a positive bias supply. When the gate voltage is higher than its threshold value, the MOS channel is inverted. The MOS electron current constitutes the base current of a lateral pnp transistor formed by the $p^+$ anode, the $n^-$ drift region and p well. As the anode $p^+/n^-$ junction turns on, it injects holes into the $n^-$ drift region and thus modulates its conductivity. The injected hole current can be divided into three components. The first component is the recombination current with the MOS electron current injected in the drift and anode regions. The second and third components are collected by the p well and $p^-$ substrate that form the collectors of lateral and vertical pnp transistors respectively.

Due to the complexity of the structures, two-dimensional numerical simulations are used to accurately analyze the device behavior. The basic semiconductor equations describing carrier transport in silicon are solved numerically using the computer programs ATLAS [8] and PADRE [9]. The relevant physical mechanisms such as different generation and recombination processes are taken into account.

In Figures 2 (a) and (b) the electron and hole concentrations in a LIGBT, designed to breakdown at 400 volts, are shown with gate voltage $V_G$=10V and anode voltage $V_A$=1.95V. The anode-drift region junction is heavily forward biased and the carrier concentrations in the drift region and part of the $p^-$ substrate are well in excess of the background doping. It is also noted that electron and hole concentrations in these regions are nearly equal. Thus, the drift region is conductivity modulated and a small voltage drop occurs on the device for a given current level. Figures 3 (a) and (b) show the electron and hole current vectors through the device under steady state conditions with $V_G$=10V and $V_A$=1.95V. Under such conditions the device under consideration has MOS electron current of 0.63 A/cm and anode current of 1.8 A/cm. The electron current flows horizontally through the channel and then spreads into the drift and $p^-$ substrate regions.

In addition to reducing the electric field and consequently the area of the device to achieve a high breakdown voltage, the $p^-$ substrate collects a large ratio of the hole current injected from the anode. Thus, turning on the $n^+$ (cathode)/ p well junction is avoided and higher latch-up current levels are achieved. The calculated different terminal currents versus the anode voltage are shown in Figure 5. The results show that latching current increases by about a factor of 4 due to the hole current collected by the $p^-$ substrate.

In shorted anode devices (Figure 1-b) the turn on voltage of the $p^+$ anode junction exceeds that of conventional LIGBT. Therefore, less conductivity modulation occurs and a higher forward voltage drop results across the device for a given current. However, the anode short results in a faster turn-off time as will be

discussed later. Figures 5 (a) and (b) show the electron and hole concentrations for the device shown in Figure 1(b) with $V_G$=10V and $V_A$=2.4V. The electron current vectors are shown in Figure 6(a). The flow of electron current under the $p^+$ anode along the junction region results in a voltage drop across the junction. This voltage drop is found to be higher at the anode corner away from the short, as can be seen from the distribution of the hole current vectors shown in Figure 6(b). Figure 6(b) indicates that hole current density varies considerably across the anode junction and that higher hole current is injected from the anode corner away from the center.

The calculated I-V characteristics of a LIGBT, shorted anode LIGBT and Lateral DMOS Transistor (LDMOST) are shown in Figure 7. LDMOST exhibits the conventional linear MOS transistor characteristics with a high on-resistance due to the drift region. LIGBT (Figure 1-a) shows the lowest on-resistance because of the heavy conductivity modulation of the drift region. However, LIGBT exhibits an offset voltage of approximately 0.7 volts before it starts full conduction. In shorted anode LIGBT the $n^-$ drift region conductivity is modulated but to a lesser extent to that of conventional LIGBT. The I-V characteristics of shorted anode LIGBT at low anode voltage (< 1.4 V) are similar to that of LDMOST. When the anode junction is forward biased current increases significantly. The turn on voltage can be controlled by device parameters such as the area of the short and the doping and thickness of the n buffer layer.

*TRANSIENT ANALYSIS*

In the following analysis, we will focus on the turn-off process in a device with a resistive load. For the device to turn-off, all the stored charge in the $n^-$, p well, $p^-$ substrate and $p^+$ anode regions must be removed. The computer program PADRE [9] is used to perform the time dependent simulations with an external load resistor between the DC voltage source and the device's anode.

In Figure (8) the calculated anode current $I_A$ , voltage $V_A$ and substrate current $I_S$ are plotted vs time during the turn off process. The gate voltage $V_G$ drops from 20 to 0 volts in 1.0 nsec. The carrier lifetimes $\tau_{po}$ and $\tau_{no}$ are taken equal to 0.1 μsec. The different phases of turn off current are shown. The sudden drop that results from cessation of the electron channel current followed by a slow decay (the current tail), which is due to excess carrier recombination is also shown. The tail part can be seen to have three phases. During the first phase both the $p^+$anode/$n^-$ drift region and $n^-/p^-$ substrate junctions are forward biased and the vertical pnp transistor is in saturation. The predominant recombination then occurs primarily in heavily doped regions which have short lifetimes, that is the anode, with the electrons stored in there recombining. Therefore, the anode current drops at a higher rate as it is controlled by the effective short lifetime in the anode. Following that, the current decay is governed by recombination in the conductivity-modulated lightly doped $n^-$ region. The decay there is slow because the ambipolar or high-injection lifetime is long. As the level of injected carriers

decrease below the doping level, the current decay then is dictated by the low-injection lifetime which is shorter than that of the high-injection case.

Figure (9) shows the electron current vectors slightly after the gate is turned off. Since a voltage drop develops across the $p^+$ well/$n^-$ drift region junction, a depletion layer starts to form and carriers are swept away from the junction. This causes the injection of carriers along the $p^+$ well/$n^-$ junction and a more uniform lateral electron current results in the drift region, when compared to the steady state case shown in Figure 3(a). However, the hole current distribution does not change significantly because little recombination occurs during this phase of the turn-off process.

Figure (10) shows the electron current vectors at t=0.3μsec. It is observed that the electron-hole plasma is now restricted to the area under the anode region. It is also noted that the vertical pnp transistor is about to come out of saturation. Figure (11) shows the holes current vectors at t=1.0 μsec. It is clear that the turn off current is almost completely determined by the lifetime of the holes in the floating base vertical pnp transistor which results in a slower decrease rate of the turn off anode current.

The different terminal current components of a shorted anode LIGBT during turn off are shown in Figure (12). Of particular interest are the various anode current phases during turn off [10]. Note that for the shorted anode case, Figure 12, the current decay shows very distinctly the high and low injection portions and a very small region for anode recombination because of the smaller anode area and the low back-injection of electrons in the anode especially near the short.

The gate turn-off time is a critical parameter. For fast gate turn off time, latch-up can be triggered by capacitive displacement currents. This dynamic latch-up is simulated using gate pulse falltime of 0.5 nsec. Figure (13) shows the electron current vectors for a shorted anode LIGBT just after gate turn-off. It is noted that the $n^+$ cathode/$p^+$ well junction is forward biased and electrons are injected from the $n^+$ cathode well below the surface.

The physical insight gained from full two-dimensional simulations enables us to simplify the analysis without sacrificing accuracy. This provides a more flexible analysis of the device in a relatively complex circuit environment. To achieve this, the program MEDUSA [11] is used. In MEDUSA the device is partioned into one dimensional segments, both lateral and vertical, that are coupled together by lumped elements (transportances). The DMOS transistor part of the device is simulated by a two-dimensional model. Figure 14 shows the anode current at on state and during turn off under resistive load conditions. The results agree reasonably well with that of full two-dimensional analysis.

*EXPERIMENTAL CORROBORATION*

Test devices of different LIGBT structures were fabricated using the dielectrically isolated Bipolar-CMOS-DMOS (BCDMOS) technology developed at AT&T Bell Laboratories [12]. The test devices were designed with separate access to the lateral anode and the drain of the DMOS that is contacted from the top via the $n^+$ wrap-around layer. The intent of the design was to analyze the structure in its DMOS and LIGBT modes of operation rather than to minimize device area.

The turn-off characteristics of one of these structures are shown in Figures 15 and 16. In Figure 15 the device is run in its DMOS mode with the anode floating, while in Figure 16, the device is run in its LIGBT mode with the drain floating. In both cases, the gate was triggered with a 10 V pulse and the anode was connected to a 20 V supply via a 1Kohm load resistor. The upper waveform in both cases is the voltage across the source to drain or anode, and the lower waveform represents the current measured with a current probe. Comparing the two current waveforms, it is clear that during turn-off the initial drop in current is similar in the two modes of operation. This represents the rapid fall in electron current via the channel of the DMOS immediately after the removal of the gate pulse. The tail in the current decay of Figure 16 is due to the excess holes injected by the anode. These holes are removed by recombination in the n-drift region and in the $n^+$ region.

The characteristic decay time of the current in the LIGBT mode is consistent with values of the hole lifetime in the $n^-$region. The voltage build-up across the source and drain or anode, as can be seen in the upper waveforms of Figures 15 and 16, occurs very rapidly with the current decay. The electrons, as verified by the simulations,are driven to the anode side where they maintain the forward bias at the anode until they recombine. Hence the shorting of the anode to the drain or $n^-$region allows the electrons to be removed faster than the recombination time,thus speeding-up the turn-off process.

*CONCLUSIONS*

In this paper, we have analyzed the DC and transient characteristics of lateral insulated gate bipolar transistors (LIGBT) using two-dimensional numerical simulations. The two-dimensional analyses allowed insight into device physics and optimization of device design. We focused on the turn-off characteristics of the LIGBTs and pointed out the role of the inherent PNP transistor of RESURF type devices. Also, the different phases of the terminals current and voltage/during turn-off have been analyzed. Furthermore, we demonstrated that use of a one-dimensional numerical simulation program, MEDUSA, is adequate for LIGBTs provided one chooses judiciously the one-dimensional segments. Finally,we presented experimental results on LIGBTs made in our dielectrically isolated BCDMOS technology using special test devices that allowed the operation of device in its DMOS and LIGBT modes. The turn-off current decay in the DMOS

and LIGBT modes was similar except for a tail due to the excess holes that are stored at the anode side and that have a slower decay time consistent with hole lifetime. As the simulations indicate,shorting the anode to the drain of the DMOS reduces the decay time by allowing the electrons to be removed at the short.

*ACKNOWLEDGEMENT*

The authors would like to thank H.W. Becke, John D'Arcy for helpful suggestions and C. A. Goodwin and T.J. Riley for their support and encouragement.

*REFERENCES*

[1] M. Darwish and K. Board "Lateral Resurfed COMFET" Electronics Letters, Vol. 20, No. 12, pp. 5119-5220, June 1984.

[2] D. Pattanyak and M. Adler "Analysiss Of Current Flow in Lateral Insulated Gate Transistors" Device Research Conference, pp. VIB-5, 1985, Boulder, CO.

[3] M. R. Simpson et al. " Analysis Of the Lateral Insulated Gate Transistor" IEDM Tech. Dig., pp. 740, 1985.

[4] D. Pattanyak et. al. "n-Channel Lateral Insulated Gate Transistors: Part I-Steady-State Characteristics", IEEE Trans. Electron Devices, Vol., Ed-33, pp. 1956, 1986.

[5] J. A. Apples and H. M. J Vaes "High Voltage Thin Layer Devices (RESURF)" IEDM Tech. Dig., pp. 238, 1979.

[6] H. W. Becke and C. F. Weatley, U. S. Patnet 4,363,073 (1982).

[7] B. J. Baliga et. al., "The Insulated Gate Rectifier (IGR): A New Power Switching Device," IEDM Techn. Dig., pp.264, 1982.

[8] J. D'Arcy "Two-Dimensional Semiconductor Simulator ATLAS" TM., to be published.

[9] M. R. Pinto and K.R. smith private communication.

[10] P. A. Gough, M.R. Simpson and V. Rumennik " Fast Switching Lateral Insulated Gate Transistor" IEDM Tech. Dig.,pp. 218,1986

[11] W. L. Engl, L. Laur and H.K. Dirks " MEDUSA a Simulator for Modular Circuits" IEEE Trans. on CAD,Vol. CAD-1,No.2,1982.

[12] C. A. Goodwin et al. " A Dielectrically Isolated BIPOLAR-CMOS-DMOS (BCDMOS) Technology for High Voltage Applications" this Symposium, 1987

FIGURE CAPTIONS

Figure 1: (a) Schematic diagram of a LIGBT, and
(b) LIGBT with shorted anode.

Figure 2: (a) Electron and
(b) Hole concentrations in LIGBT with $V_G$=10V and $V_A$=1.95V.

Figure 3: (a) Electron and
(b) Hole current vectors of LIGBT with $V_G$=10V and $V_A$=1.95V.

Figure 4: Anode ($I_A$), Cathod ($I_K$) and Substrate ($I_S$) terminal current of the device shown in Figure 3.

Figure 5: (a) Electorn and
(b) Hole concentrations in a shorted anode LIGBT with $V_G$=10V and $V_A$=2.4V.

Figure 6: (a) Electron
and (b) Hole current vectors in a shorted anode LIGBT with $V_G$=10V and $V_A$=2.4 V.

Figure 7: I-V characteristics of LIGBT, shorted anode LIGBT and LDMOST.

Figure 8: LIGBT anode current and voltage and substrate current during turn-off.

Figure 9: Electron current vectors of LIGBT during turn-off at t=1.2 nsec.

Figure 10: Electron current vectors of LIGBT during turn-off at t=0.3 μsec.

Figure 11: Hole current vectors of LIGBT during turn-off at t=1 μsec.

Figure 12: Shorted anode LIGBT anode current and voltage and substrate current during turn-off.

Figure 13: Dynamic latch-up in a shorted anode LIGBT t=0.5 nsec.

Figure 14: Calculated anode current at on-state and during turn-off using one-dimensional segments.

Figure 15: Waveform of a lateral device in the DMOS mode drain voltage (top) with 10V/div and drain current (bottom) with 8mA/div.

Figure 16: Waveform of a lateral device in the LIGBT mode, anode voltage (top) with 10V/div and anode current (bottom) with 8mA/div.

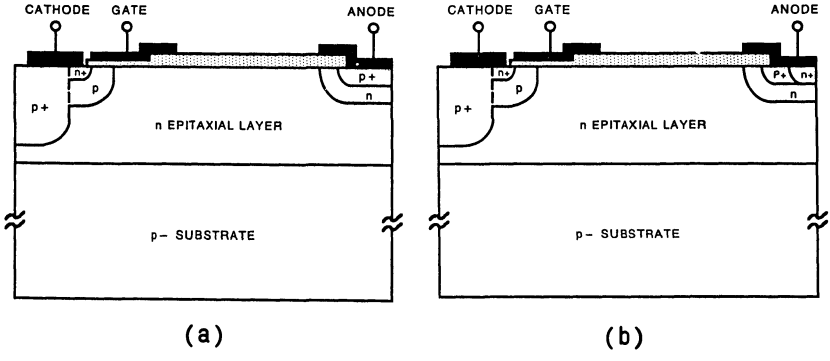



Figure 1: (a) Schematic diagram of a LIGBT, and
(b) LIGBT with shorted anode.

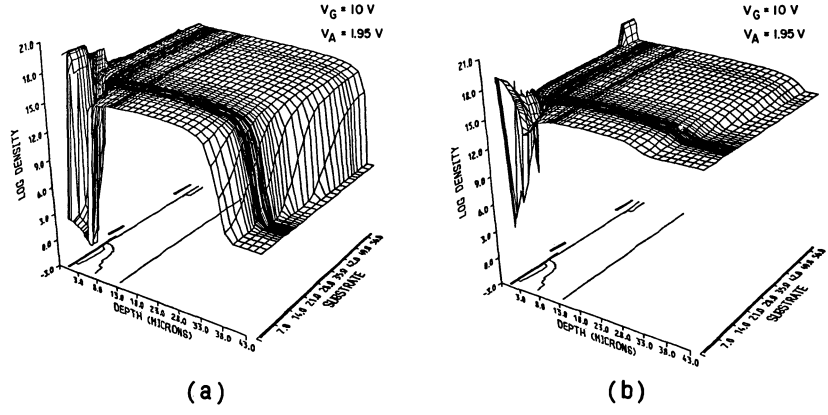



Figure 2: (a) Electron and
(b) Hole concentrations in LIGBT with $V_G$=10V and $V_A$=1.95V.

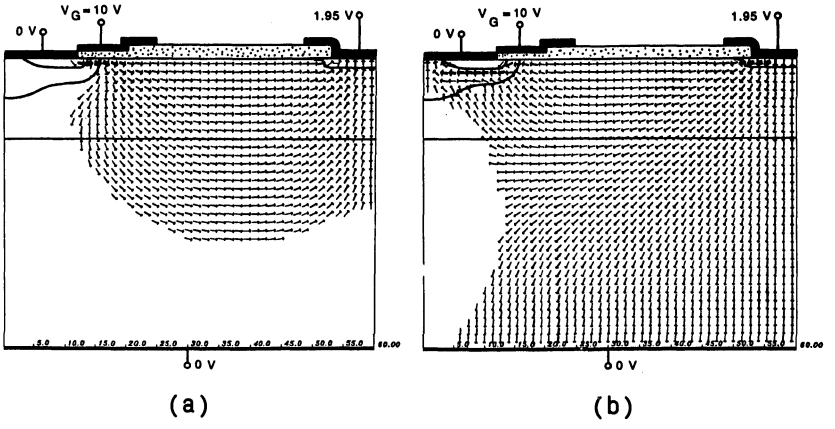



Figure 3: (a) Electron and
(b) Hole current vectors of LIGBT with $V_G$=10V and $V_A$=1.95V.

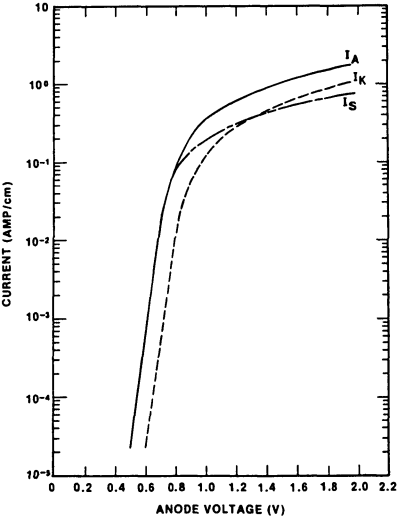



Figure 4: Anode ($I_A$), Cathode($I_K$) and Substrate ($I_S$) terminal current of the device shown in Figure 3.

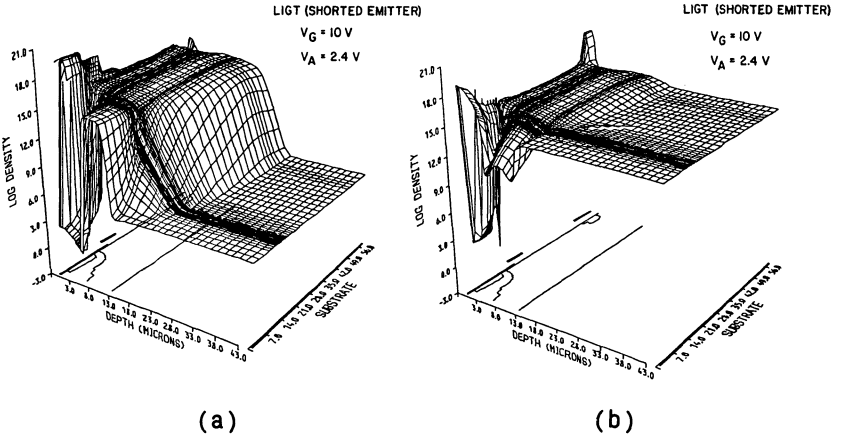



Figure 5: (a) Electorn and
(b) Hole concentrations in a shorted anode LIGBT with $V_G$=10V and $V_A$=2.4V.

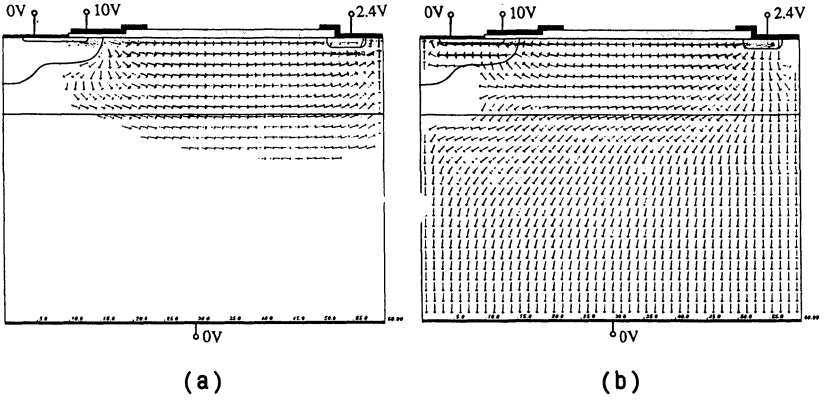



Figure 6: (a) Electron
and (b) Hole current vectors in a shorted anode LIGBT with $V_G$=10V and $V_A$=2.4 V.

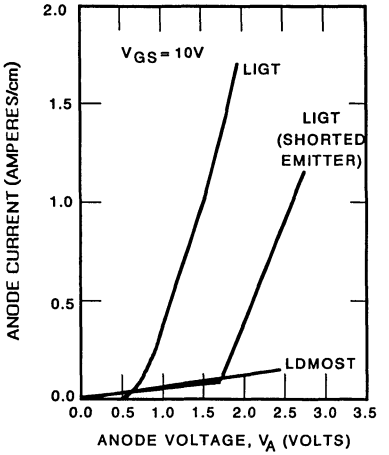



Figure 7: I-V characteristics of LIGBT, shorted anode LIGBT and LDMOST.

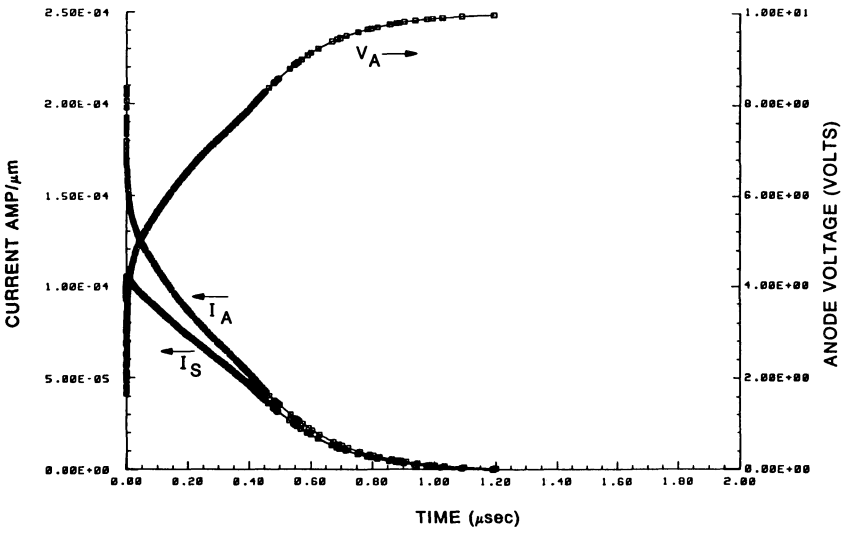



Figure 8: LIGBT anode current and voltage and substrate current during turn-off.

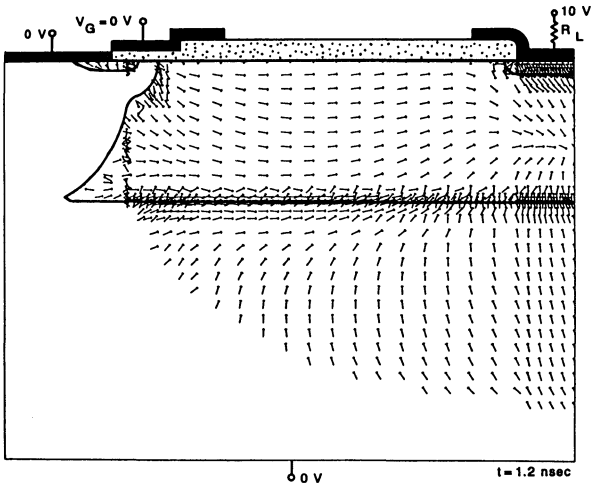



Figure 9: Electron current vectors of LIGBT during turn-off at t=1.2 nsec.

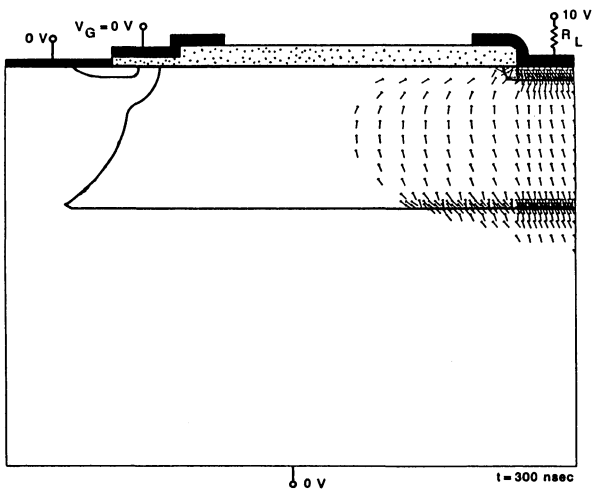



Figure 10: Electron current vectors of LIGBT during turn-off at t=0.3 μsec.

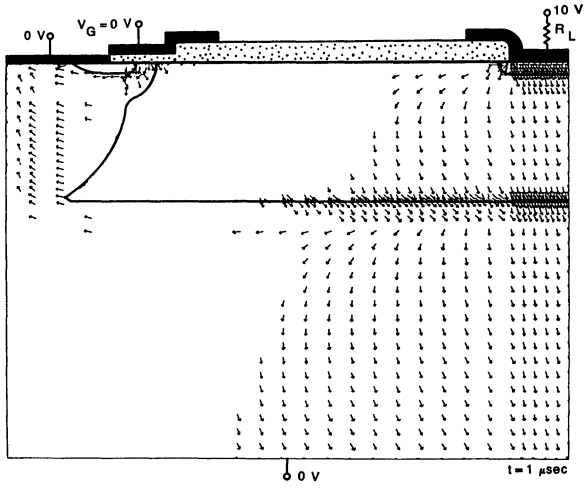



Figure 11: Hole current vectors of LIGBT during turn-off at t=1 μsec.

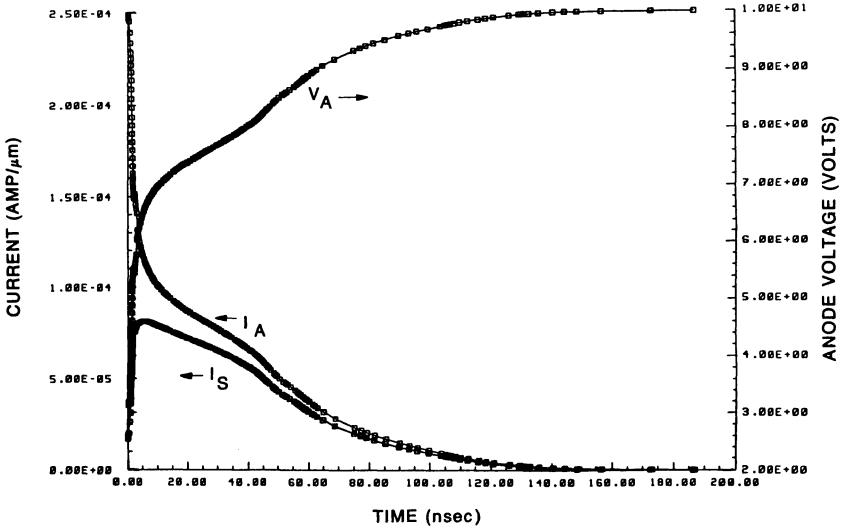



Figure 12: Shorted anode LIGBT anode current and voltage and substrate current during turn-off.

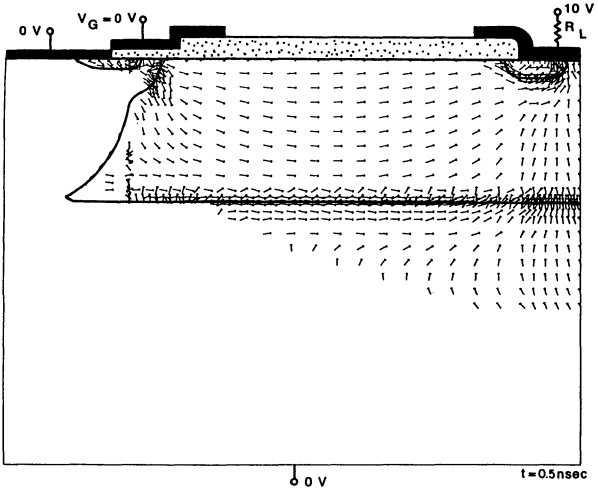



Figure 13: Dynamic latch-up in a shorted anode LIGBT t=0.5 nsec.

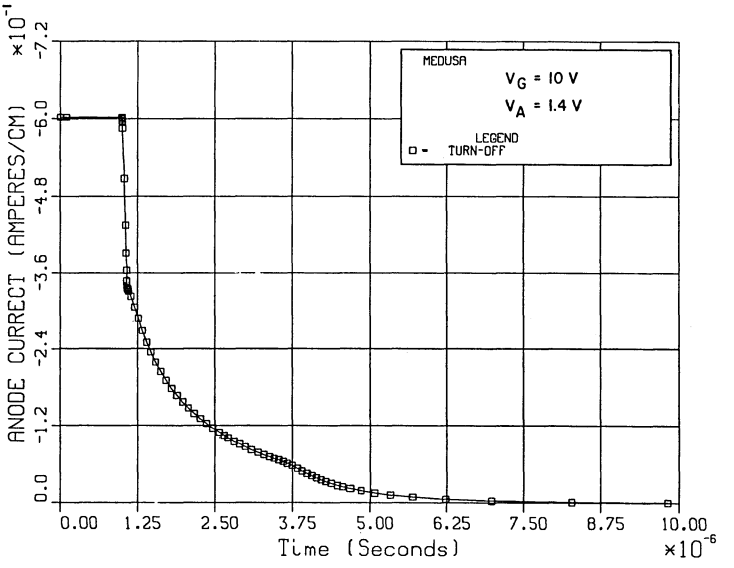



Figure 14: Calculated anode current at on-state and during turn-off using one-dimensional segments.

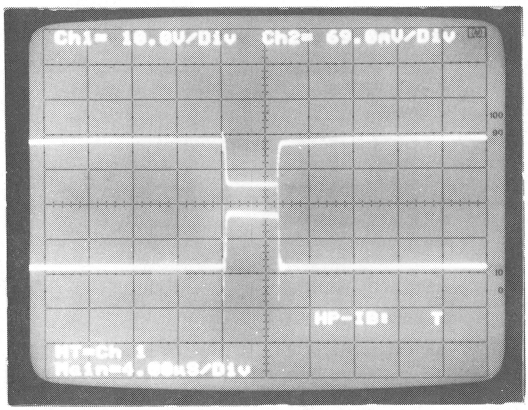



Figure 15: Waveform of a lateral device in the DMOS mode drain voltage (top) with 10V/div and drain current (bottom) with 8mA/div.

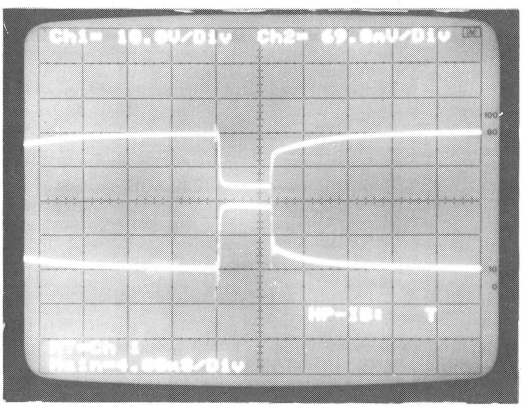



Figure 16: Waveform of a lateral device in the LIGBT mode, anode voltage (top) with 10V/div and anode current (bottom) with 8mA/div.

Proceedings of The Electrochemical Society, PV 1987-13, 310-317 (1987)
DOI: 10.1149/198713.0310PV © The Electrochemical Society

# Influence of Device Structure on the Transient and Steady State Characteristics of LIGT.

S. Mukherjee, M.Amato and V.Rumennik

Philips Laboratories,
North American Philips Corporation,
345 Scarborough Road,
Briarcliff Manor, NY 10510.

## ABSTRACT

The transient and steady state characteristics of the LIGT have been studied for several variations of the device structure and compared with that of LDMOS. The structural variations include combinations of n+ and p+ drain diffusions that clamp the drain junction as well as provide an effective resistive path for electron extraction at turn off. For the same breakdown voltage as LDMOS (500 volts) almost an order of magnitude reduction in ON resistance is observed in all the structures at high current. However, the switching turn OFF time is found to vary according to the efficiency of the minority carrier extraction process. The application of LIGT's in Power Integrated Circuits is also discussed.

## 1. INTRODUCTION

The Lateral Insulated Gate Transistor (LIGT)[1,2] has generated considerable interest in recent years primarily because of the reduced ON resistance that has been achieved in comparison with an LDMOST. In Power Integrated Circuit applications, where the trend is to increase the ratio of the area consumed by low voltage control circuitry to that of the power device, the LIGT promises substantially smaller die size. However, it is necessary to consider the switching delay or turn OFF time of the device together with the steady state ON resistance to determine the overall power loss in the chip. Furthermore, in Power Integrated Circuit applications it is necessary to determine the effect of the device operation on the peripheral circuitry and also the maximum current handling capability, limited by parasitic SCR latch-up.

In this paper the steady state and switching characteristics of the LIGT has been studied with a view to applications in Power Integrated

Circuits. It is seen that the device performance can be tailored to meet a specific requirement by using a modified anode structure.

## 2. DEVICE STRUCTURE

The structure of the conventional LIGT can be viewed as a modification of an LDMOS where the n+ drain diffusion is replaced by a p+ diffusion. This is shown in Figure-1 (a) & (b). A further variation is shown in Figure-1(c) where the drain junction consists of a combination of a p+ and n+ diffusion adjacent to each other. This structure can be viewed as a parallel combination of a conventional LIGT and an LDMOS. The performance characteristics of this device depends upon the sizes and spacing between the n+ and p+ diffusion.

## 3. DEVICE OPERATION

It is well known that in comparison with an LDMOS (Figure-1a) the conventional LIGT (Figure-1b) operates by injecting minority carriers in the drift region from a p-n junction at the drain end, thereby modulating the conductivity of the drift region and reducing the ON resistance. However, the storage time of the minority carriers results in increased turn OFF delay during switching. To minimize the turn OFF delay, it is possible to control the amount of minority carriers injected and/or provide an efficient conduction path for the carriers at turn OFF. Figure-1c shows a variations in the structure of the LIGT. Here an n+ diffusion is added to the drain end next to the p+ injector diffusion. The n+ diffusion provides a conductive path to electrons when the device is turned OFF at the gate, thereby reducing the turn OFF delay in comparison with the conventional LIGT(Figure-1b). Depending on the area of the n+ and p+ diffusions, this structure also helps to clamp the p+ injector at turn ON and reduce the amount of minority carriers injected into the drift region. By varying the separation between the n+ and p+ drain diffusions, additional control over the minority carrier injection can be achieved.

## 4. STEADY STATE CHARACTERISTICS

The devices shown in Figure-1 have all been fabricated on the same wafers using an all diffused process. The breakdown voltages of all the devices have been found to exceed 500 volts in agreement with designed values. The steady state IV characteristics are shown in Figure-2. At high currents the LIGT ON resistances are more than a factor of six lower than that of the LDMOS. The onset of the minority carrier injection is shown as a kink in the IV characteristics. LIGT1, shown in Figure-1c, is seen to exhibit a higher minority carrier onset voltage

compared to the conventional LIGT, and less minority carrier injection, implying clamping of the p-n junction bias as explained above. The advantage of this structure over the conventional LIGT is seen in the low current regime, prior to the onset of minority carrier injection, where the device operates like a LDMOST. The curve labeled LIGT2 in Figure-2 represents the same device as LIGT1 with increased separation between the n+ and p+ drain diffusions. In this device, the onset of the minority carrier injection is lowered, and the clamping of the p+ junction bias is reduced.

## 5. SWITCHING CHARACTERISTICS

The turn OFF delay characteristics of the devices are shown in Figure-3 as a function of on-state drain current. These characteristics were measured with a fixed load resistance on the drain and variable supply voltage (Vdd) to obtain different drain currents. In general the turn-off delay depends both upon the on-state current and off-state voltage (Vdd)[3]. In comparison with the other devices the conventional LIGT is seen to exhibit reduced turn-off delay with increasing drain current. This is caused by the increasing drain voltage which reduces the turn-off delay. In other words, in the conventional LIGT, the turn-off delay is a stronger function of the off-state voltage than the on-state current. Comparison of the switching delay and the IV characteristics (Figure-2 and 3) show that there is an inherent compromise between the onset of the minority carrier injection and the turn OFF delay. In a practical application the total power dissipation in the device will be determined by a combination of the steady state ON resistance and turn OFF delay. Therefore, the LIGT1 is expected to exhibit less power dissipation at moderately high frequencies in comparison with the conventional LIGT.

## 6. MINORITY CARRIERS IN THE SUBSTRATE

Another important consideration in the application of LIGTs in Power Integrated Circuits is the minority carriers injected into the substrate during the ON state. This sets a limit to the proximity of the low voltage control circuits (especially for CMOS) on the same chip. Figure-4 shows the collected minority carrier current at a distance of 100 microns from the device as a function of the drain current of the LIGT1. This current is seen to be about seven orders of magnitude lower than the drain current.

Finally, the latch-up currents of both the LIGTs have been found to exceed 250 Amps per square cm. at room temperature.

## 7. CONCLUSION

The steady-state and turn off characteristics of the Lateral Insulated Gate Transistor (LIGT) has been studied and it has been shown that variation of the anode configuration results in a trade-off between the on resistance and switching speed. In particular, with a clamped anode structure, the turn-off delay is reduced at the expense of increased on resistance. This trade-off can be optimized for a given application. Furthermore, in Power Integrated Circuit (PIC) applications, the effect of minority carrier substrate current on the operation of the peripheral circuits (particularly for CMOS) has been quantified.

Acknowledgments

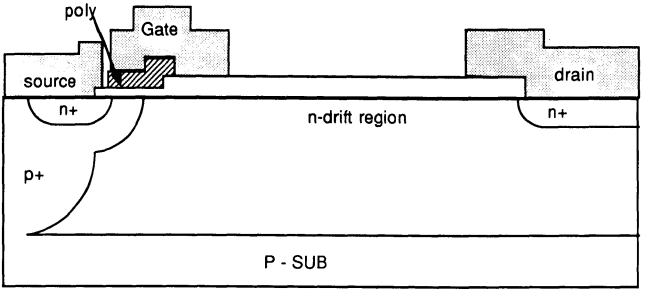
We would like to acknowledge P.Tsui and D.McArthur for wafer testing, M.Simpson for helpful discussions and the clean room staff for processing Silicon.

REFERENCES

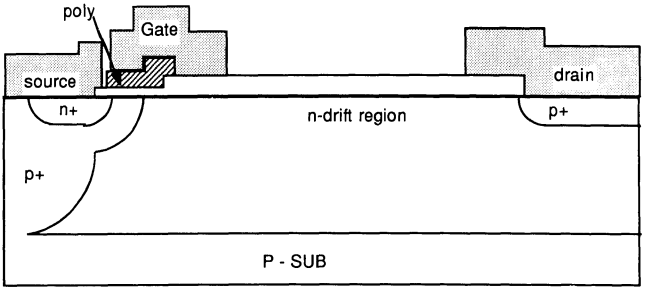
(1) M.Darwish and K.Board,"Lateral Resurfed COMFET",Electron. Lett.1984, 20,pp.519-520

(2) R.Jayaraman, V.Rumennik, B.Singer, and E.H.Stupp, "Comparison of High Voltage Devices for Power Integrated Circuits",IEDM Tech.Digest.,1984,pp.258-261.

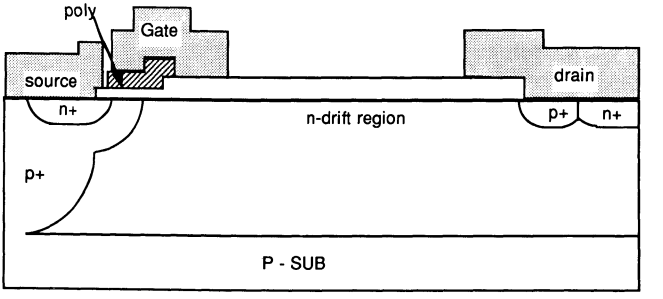
(3) To be published.




(a) LDMOST




(b) LIGT




(c) LIGT1

Figure-1. Cross-section of LDMOST, LIGT and modified LIGT.

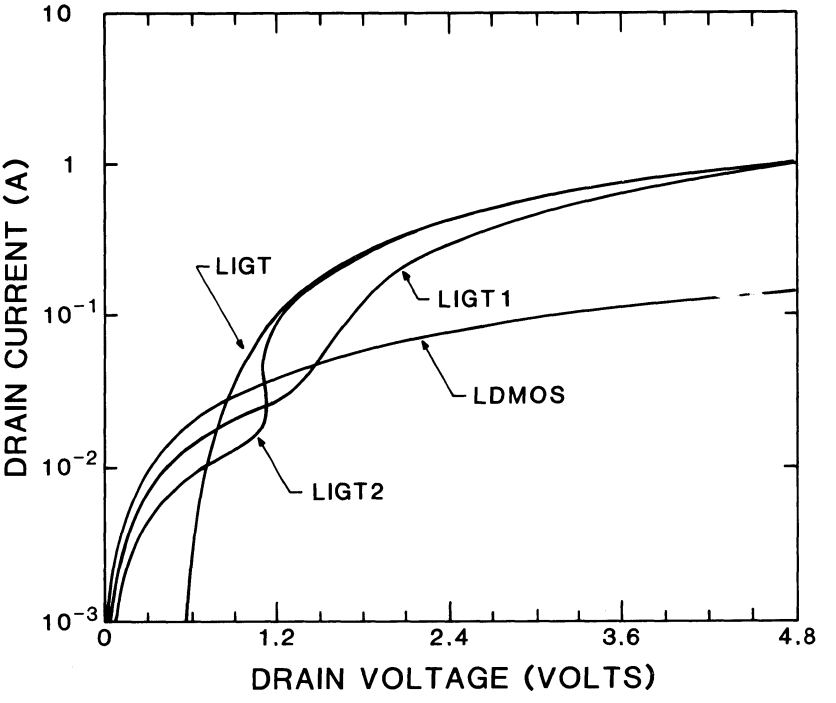



Figure-2. Steady state IV characteristics of LDMOST, LIGT and modified LIGT. All currents are normalized to the same area. Breakdown voltage of all devices exceed 500 volts.

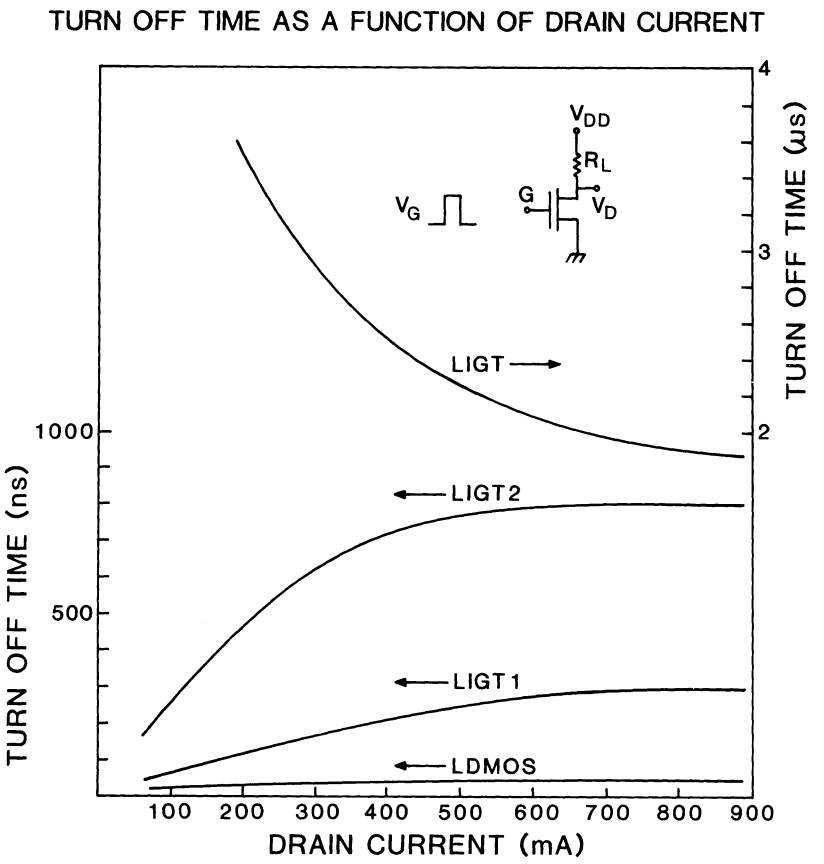



Figure-3. Turn off time vs maximum drain current for LDMOST, LIGT and modified LIGT.

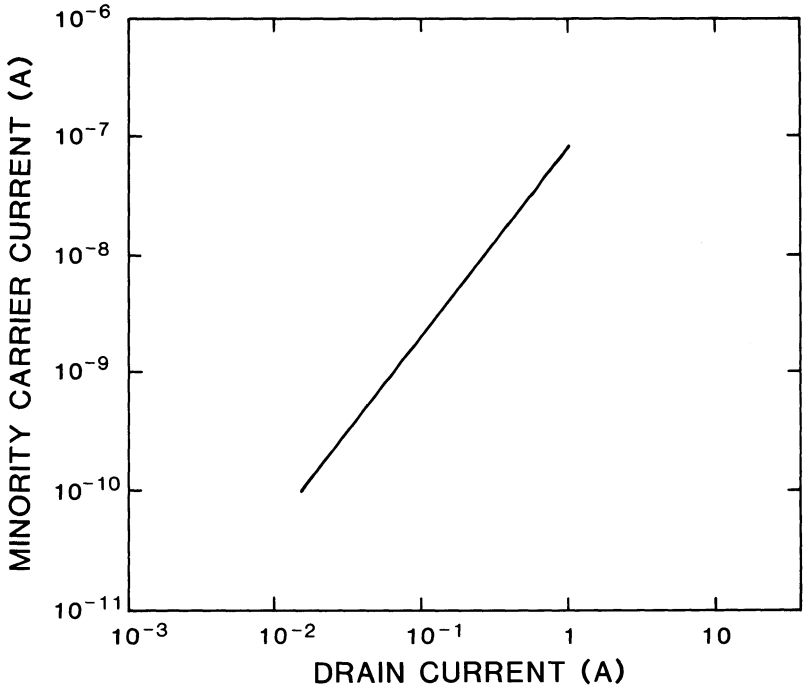



Figure-4. Minority carrier current collected 100 microns away from the device for LIGT1.

Proceedings of The Electrochemical Society, PV 1987-13, 318-327 (1987)
DOI: 10.1149/198713.0318PV © The Electrochemical Society

# TWO-DIMENSIONAL DEVICE SIMULATION OF HIGH-VOLTAGE LATERAL DMOSFETs

**Richard K. Williams, Francis X. Timmes, Robert W. Busse and Ion Kuan Siu**
*Siliconix, inc., 2201 Laurelwood Road, Santa Clara, California 95054*

## ABSTRACT

The I-V characteristics of a high-voltage LDD (lightly doped drain) lateral DMOS transistor have been simulated using the two-dimensional (2D) device simulator PISCES and compared to both measured and lumped-element device model results. A 1416-point nonuniform mesh was selected to maximize simulation accuracy in the channel and drift regions while minimizing computer run times. Simulation results show close agreement with measured values of device breakdown, normalized on-resistance and normalized saturation current as a function of the drift length, Ld. Device simulations of the LDD DMOS transistor in saturation indicate the collapse in transconductance observed at high-drain currents is due to parasitic JFET action of the lightly-doped drift region. This collapse was accurately modeled as a lumped-element JFET/MOSFET series combination subcircuit using parameter-extracted data in conjunction with a SUXES multiple-target optimization. Finally, the interrelationships of empirical, lumped-element and device simulation modeling techniques for device design and circuit simulation are discussed.

## INTRODUCTION

In the past several years, the application of high-voltage integrated circuits (HVICs) has increased. Previous development efforts have focused, primarily, on the process technology necessary to integrate high-voltage devices with low-voltage logic and control circuitry. To provide more complex functions, today's HVICs require higher levels of integration and more efficient use of available silicon real estate. This concern with area efficiency has provided an impetus for optimizing the design and layout of integrated high-voltage transistors through the use of computer simulations and device models.

One device common to many of today's HVICs is the lateral double-diffused transistor (LDMOS) using lateral-charge-control technology (1,2). The controlled-surface charge, whether implanted or provided by an epitaxial layer, is required to reduce the high surface-related electric fields which limit device breakdown. Consequently, the device is often referred to as a RESURF or lightly-doped-drain (LDD) transistor. Modeling the electrical characteristics of such a device requires that the behavior of a low-voltage MOSFET in series with a high-voltage drift region be described. The purpose of this work is to develop an accurate device model of an N-channel LDD lateral DMOSFET using the 2D device simulator PISCES and to correlate this information with a computationally convenient lumped-element device model. The work presented here concentrates on N-channel devices though a similar development could be described for P-channel LDD MOSFETs as well.

## DEVICE DESCRIPTION

Figure 1 illustrates the cross section of an N-channel LDD lateral DMOSFET. The device is composed of an N+ source and drain region with a lightly-doped N– drain extension self-aligned

to a polysilicon gate. Though the test devices fabricated used 1000A gate oxides, thicknesses between 500 and 2000A are common. The substrate is a high-resistivity p-type material (typically from 15 to several hundred Ω-cm) which facilitates high N+ drain-to-substrate avalanche voltages. The drift region, having an ion-implanted charge typically around 1E12 cm−2, varies in length, Ld, according to breakdown requirements. A lightly doped substrate requires the addition of a P-type body diffusion around the source to prevent punchthrough and maintain a positive threshold voltage, hence, the name double-diffused.

The device fabrication is compatible with an N-well CMOS process architecture allowing the integration of multiple high-voltage transistors with low-voltage logic. Since the N+ drains naturally form back-to-back diodes with the P-type substrate, the transistors are said to be "self-isolated."

## MODELING TECHNIQUES

To provide a basis for comparison between simulations and actual MOS transistors, an array of test devices was designed and fabricated. Devices include drift lengths ranging from zero to 37.5 μm. Data was taken using an integrated measurement system consisting of a VAX 11-780, an IEEE 488 bus, an HP 4145 semiconductor parameter analyzer, a switching matrix and other related hardware. Two distinct device modeling techniques were used to interpret the measured data, namely normalized device efficiencies and lumped-element subcircuit models. The electrical characteristics predicted by these simplified models are correlated to the PISCES simulation results described later in the paper.

In cases where only rudimentary "hand-calculations" are required, the test pattern provides electrical parameters (Rds, Id(sat), BV) that are normalized by the transistor's gate width (e.g., Rds•W and Id(sat)/W). The advantage of archiving statistical distributions of these electrical parameters is that manufacturing-related process variations are monitored and that initial IC device-size estimates use look-up tables. These electrical parameters were used to validate the initial mesh structure to be used in the 2D simulator prior to the detailed simulation.

It is well known that standard MOSFET circuit simulation models do not represent high-voltage LDMOS devices either structurally or electrically. To alleviate this problem, a subcircuit whose constituents are related to physical components of the LDD lateral DMOS transistor was developed. The subcircuit shown in Figure 2 models the transistor by a series combination of three devices, specifically

- a low-voltage enhancement-mode MOS transistor describing the double-diffused or P-body region of the device
- a low-voltage N-channel depletion-mode MOS transistor describing the gate region covering the P− substrate
- an N-channel JFET describing the resistance and current saturation of the N− drift resistor.

The subcircuit developed here is similar to the one for junction-isolated LDMOS transistors (3,4,5) except that the substrate does not form a pinch resistor with the depletion-mode device. A subcircuit for self-isolated LDD DMOS without the double-diffused region has also been proposed (6).

The multiple-target Levenberg-Marquardt algorithm in the enhanced SUXES (7) optimization program was used to extract a geometrically independent SPICE parameter vector for the

lumped-element LDD lateral DMOS. The model equations to be optimized are formulated by including the HSPICE circuit simulator (8) as a subroutine call in this enhanced version of SUXES. To our knowledge, this is this first time such a modeling technique has been employed for an LDD lateral DMOS parameter extraction, although similar efforts have been applied to discrete vertical DMOS structures (9). Scaling the JFET and both the enhancement- and the depletion-mode MOSFETs allows a single lumped-element model to simulate devices of varying poly gate (Lp) and drift lengths.

The lumped-element model was used with the 2D device simulation results to interpret the measured and simulated behavior of the LDMOS transistor. The predictive nature of the lumped-element subcircuit allows I-V characteristics to be generated for LDMOS devices scaled by W, Lp and Ld. This feature makes it particularly attractive in providing parameters for circuit design and simulation. The lumped-element subcircuit cannot predict the effect of processing parameters such as substrate doping on device electrical behavior. Moreover, the model development involves an extensive characterization of test devices. Future development will involve extracting parameters directly from PISCES device simulations.

The device simulator PISCES (10) simulates the electrical characteristics of a device from a 2D description of the device's nonplanar structure (cross section) and its impurity dopant profiles. The vertical dopant profiles were input into PISCES directly from SUPREM III (11) process simulations. These profiles were verified using a spreading resistance probe. The source/body vertical dopant profile, as shown in Figure 3, is extended into two dimensions by declaring the lateral diffusion width and a normalization factor to use as a multiplier for a Gaussian horizontal doping profile. For the devices simulated, a difference of two Gaussians was employed to form an effective channel region of 3 μm. This 2D transformation technique provides a possible source of error in the device simulation. Work is under way which uses the difference of two complementary error functions, or uses 2D process simulations to describe the lateral channel dopant profile.

The triangular element mesh structure used in PISCES to simulate an Ld = 12 μm lateral DMOS is shown in Figure 4. This mesh structure uses 1416 points, of which 400 are within the top 200A of the silicon surface for areas near the source-body channel junction. The mesh was chosen as the trade-off point between accuracy and CPU time.

Once the structure is defined, the Poisson's and majority carrier continuity equations are solved by a coupled solution method to find the static potential and carrier concentrations at the given electrode bias conditions. Impurity-concentration-dependent mobility was used in the simulation. Along the oxide-semiconductor interface, mobility becomes substantially lower than in the bulk due to surface scattering. The surface degradation factor g(surf) of 0.86 was chosen, thereby reducing mobility by a factor of g(surf) at the interface. Furthermore, electric-field-dependent velocity-saturation effects were included in the simulation. Finally, Auger and Shockley-Reed-Hall junction generation-recombination terms with equal hole and electron lifetimes of 2.5E–6 seconds were included.

Detailed PISCES simulations of high-voltage large-area devices is computationally intensive. However, the physical basis of PISCES allows examination of the LDD lateral DMOS internal depletion widths, equipotentials, field distributions, current-flow patterns and external I-V characteristics as the drift length, Ld, is varied. A properly gridded and calibrated 2D structure has the advantage of being a fully predictive model.

## RESULTS OF ANALYSIS

The DC drain characteristics are an excellent vehicle for displaying the results of the composite modeling effort. Figure 5 shows the measured (squares), lumped element (diamonds) and 2D device simulated (circles) drain current versus drain bias for three different gate drives of an Ld = 12 μm device. The maximum and root-mean-square error between the measured and PISCES simulated drain current is 8.6% and 2.1%, respectively. Similarly, a maximum error of 9.1% and an RMS error of 1.2% exists between the measured and lumped-element drain current values. Note that the collapse of the transconductance is well accounted for by both the PISCES simulation (pinching of the N- drift depletion region) and the optimized lumped-element subcircuit (threshold voltage of the JFET).

With the absence of an ionization integral in PISCES, the breakdown of the device is determined by examining the functional shape of the electric field along the silicon-oxide interface. A typical one-dimensional electric field distribution along the Si-SiO2 interface is shown in Figure 6 for the Ld = 12 μm device at drain-source biases of 75 V, 100 V, 125 V and 150 V. When the electric field at the interface exceeds the critical value of 4E5 V/cm for avalanche breakdown (12), the LDMOS is said to have "broken down."

With this definition, PISCES simulations indicate that the breakdown voltage of the device improves by about 10 to 12 V/μm of incremental drift length. Measured values of BVdss confirmed the PISCES predictions as shown in Figure 7. Breakdown in the lumped-element model is simulated by adding a reverse biased diode between the enhancement-mode MOS source node and the JFET drain node. Unless an Ld-dependent formula for BVdss is used, the sharp breakdown voltage of this diode is set to the measured breakdown eliminating the need for comparisons between lumped-element and measured data.

Figure 8 illustrates the drift length dependence of normalized on-resistance Rds•W (kΩ-cm) for an Lp = 12 μm LDD lateral DMOS transistor in the linear region of operation (Vds = 0.25 V). PISCES simulations show excellent agreement with both measured and lumped-element subcircuit resistances. The linear dependence of resistance on Ld is predicted by the lumped-element model when the JFET (symbolizing the drift region) is biased in the linear region. The slope of the Rds•W vs. Ld curve is equal to the sheet resistivity of the drift resistor Rs(N-) and is independent of gate bias. A least-squares fit of this data yields a slope of 5.2 kΩ/□ which was confirmed by Kelvin-probed (N-) resistor measurements and SRPs. The intercept of the curve corresponds to the low-voltage LDMOS resistance (a composite of the enhancement- and depletion-mode devices) and therefore depends on the gate drive, Vg.

For high drain voltages, the drain current of the LDD lateral DMOS transistor saturates (13). Figure 9 illustrates the drift length dependence of normalized saturation current Id(sat)/W for an Lp = 12 μm transistor at Vds = 25 V. The PISCES simulation shows excellent agreement with both measured and lumped-element values.

At low gate drives (e.g., Vgs = 5 V) the transistor saturation current is independent of drift length. Under such conditions the drift region behaves as a linear resistor and the current is limited by the low-voltage LDMOS device operating in its saturation region. At high gate drives (e.g., Vgs = 15 V), however, device operation is much different. With significant current flow, the drift resistor begins to drop a significant percentage of the applied voltage. Consequently, the two-sided depletion spreading in the drift region causes the parasitic JFET to pinch-off. When this occurs, the low-voltage LDMOS moves into the linear region and the current becomes entirely controlled by the saturation characteristics of the drift region. Thus, at high gate drives, the drain current is a function of drift length and charge, Qd.

To account for the current saturation effect of the drift region, the lumped-element model makes the assumption that the source of the JFET (a node internal to the LDD transistor itself) can be described to the circuit simulator as an external node with a distinct bias. The agreement to the measured characteristics validates this assumption. Our unique parameter extraction methodology was quite robust in obtaining an optimized vector for the LDD lateral DMOS subcircuit.

## SUMMARY

The agreement of PISCES device simulations with measured data and lumped-element subcircuit models confirms the accuracy and utility of a physically-based LDD lateral DMOS device model. Once a device grid structure is defined and numerical convergence is achieved, the predictive value of the model is useful in the optimization of transistor dopant profiles and topographies. Computer run times, however, were found to be extremely sensitive to the grid selection. In fact, a reduction in grid-point density from 1865 to 1411 reduced the CPU time by 30% with no corresponding reduction in simulation accuracy (to three significant places).

Table 1 compares the features of the device simulator with other device analysis techniques. Clearly, the predictive value and minimal degree of measurements required by PISCES are important attributes of the device simulator. Device simulators are computationally intensive and thereby inappropriate as subroutine calls in circuit simulators. In such cases, the lumped-element subcircuit model is best suited to provide accurate results for an entire range of device gate and drift lengths. For manufacturing trend analysis, however, the archival data base should be restricted to a few representative devices using look-up tables. This approach avoids the long measurement times required by parameter extraction routines used in lumped-element subcircuit models.

Only the combined application of all three techniques addresses the full range of device modeling requirements.

## CONCLUSIONS

The I-V characteristics of a high-voltage LDD (lightly doped drain) lateral DMOS transistor have been simulated using the 2D device simulator PISCES and compared to both measured and lumped-element device model results. Simulation results show close agreement with measured values of normalized on-resistance and normalized saturation current as a function of the drift length Ld.

Device simulations of the LDD MOS transistor in saturation indicate that the collapse in transconductance observed at high drain currents is due to parasitic JFET action of the lightly doped drift region. This collapse was accurately modeled as a lumped-element JFET/MOSFET series combination subcircuit using parameter-extracted data in conjunction with a SUXES multiple-target optimization. Simulations further confirm the lightly doped drift region behaves as a series linear resistance at lower drain currents. Due to the lack of ionization integrals in PISCES, breakdowns were estimated as the voltage at which the peak-electric field in the drift equals the critical electric field of silicon. The predicted dependence of breakdown on drift length of approximately 10 to 12 V/μm agrees well with measured breakdowns.

Finally, the interrelationship of empirical, lumped-element and device simulation modeling techniques for device design and circuit simulation was discussed. Future modeling efforts will

concentrate on the effects of the drift charge Qd, scaling of the poly gate length Lp and placement of field plates on the LDD lateral DMOS electrical characteristics.

## ACKNOWLEDGMENT

The authors wish to thank Sue Diehl and Craig Yappert for the many hours they dedicated to the preparation and layout of this manuscript.

## REFERENCES

1. R.A. Blanchard and R.K. Williams, "D/CMOS Technology: SMARTPOWER Processes that Solve Different Circuit Design Problems," ELECTRO/86 proc., paper 13/1, 1986.
2. E.J. Wildi, P.V. Gray, T.P. Chow, H.R. Chang, "Modelling and Process Implementation of Implanted Resurf Type Devices," IEDM Tech. Dig., p.p. 268-271, 1982.
3. H.R. Claessen and P. Van der Zee, "An Accurate DC Model for High-Voltage Lateral DMOS Transistors Suited for CACD," IEEE Trans. Electron Devices, Vol. ED-33, Dec. 1986.
4. S.C. Sun and J.D. Plummer, "Modeling of the On-Resistance of LDMOS, VDMOS and VMOS Power Transistors," IEEE Trans. Electron Devices, Vol. ED-27, no. 2, Feb. 1980.
5. M.D. Pocha and R.W. Dutton, "A Computer-Aided Design Model for High-Voltage Double-Diffused MOS (DMOS) transistors" IEEE Jrnl. of Solid State Circuits., Oct. 1976.
6. I. Yoshida, T. Masuhara, and M.Kubo, "Device Design of a Ion Implanted High Voltage MOSFET," Proc. Sixth Conf. Solid State Devices, 1974.
7. K. Doganis and D.L. Scharfetter, "General Optimization and Extraction of IC Device Model Parameters," IEEE Trans. Electron Devices, Sept. 1983.
8. L.W. Nagel, "SPICE 2: A Computer Program to Simulate Semiconductor Circuits", Memorandum No. ERL-M520, College of Engineering, University of California at Berkeley, May 1975.
9. F.X. Timmes, N. Maluf and D. Dodt, "Simulation of Power DMOS Devices," IEEE/IAS Conference Record. Denver, Oct. 1986.
10. M.R. Pinto, C.S. Rafferty, and R.W. Dutton, "PISCES-II: Poisson and Continuity Equation Solver," Stanford Electronics Lab. Tech. Report, Sept. 1984.
11. J.D. Plummer, et. al., "Process Simulators for Silicon VLSI and High Speed GaAs Devices," Integrated Circuits Lab, Stanford July 1986.
12. A.S. Grove, "Physics and Technology of Semiconductor Devices," (Wiley: New York, 1967).
13. S. Colak, "Effects of Drift Region Parameters on the Static Properties of Power LDMOST," IEEE Trans. Electron Devices, Vol. ED-28, no. 12, Dec. 1981.

Robert W. Busse is now employed by Siemens Components, PSD, Santa Clara, CA

PISCES and SUPREM-III were obtained from Technology Modelling Associates, Palo Alto, CA. SUXES and HSPICE were obtained from Meta-Software.Inc., Campbell, CA.

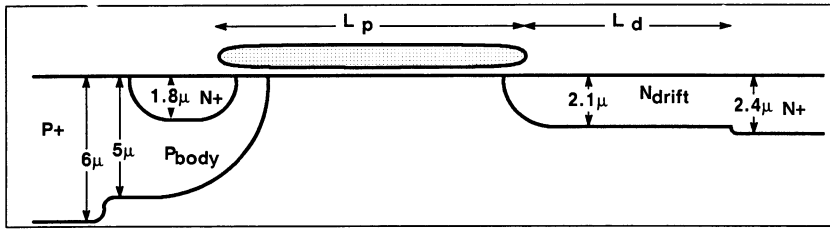



Figure 1: Cross Section of Self-Isolated High-Voltage N-DMOS

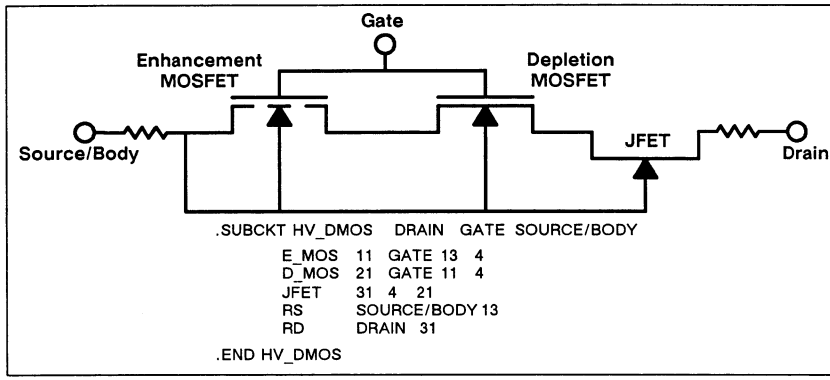



Figure 2: Topography and Net List
of Lateral HV DMOS Lumped-Element Model

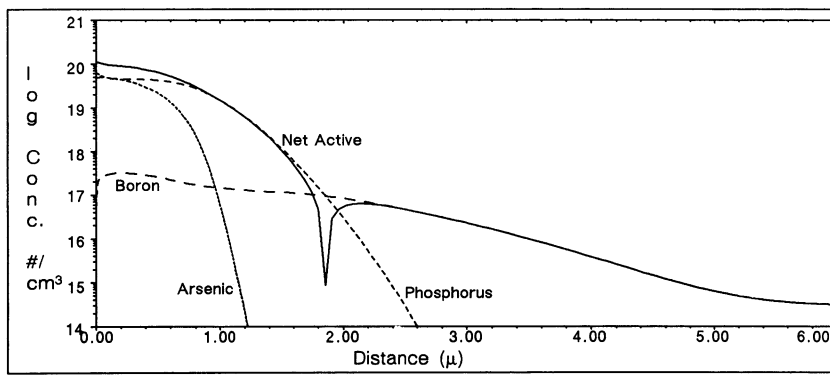



Figure 3: Source/Body Vertical Doping Profiles of HV LDD N-DMOS

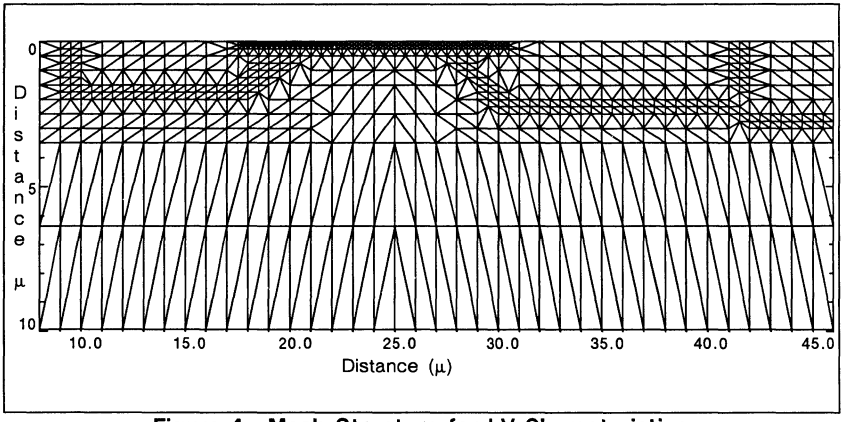



**Figure 4: Mesh Structure for I-V Characteristics**

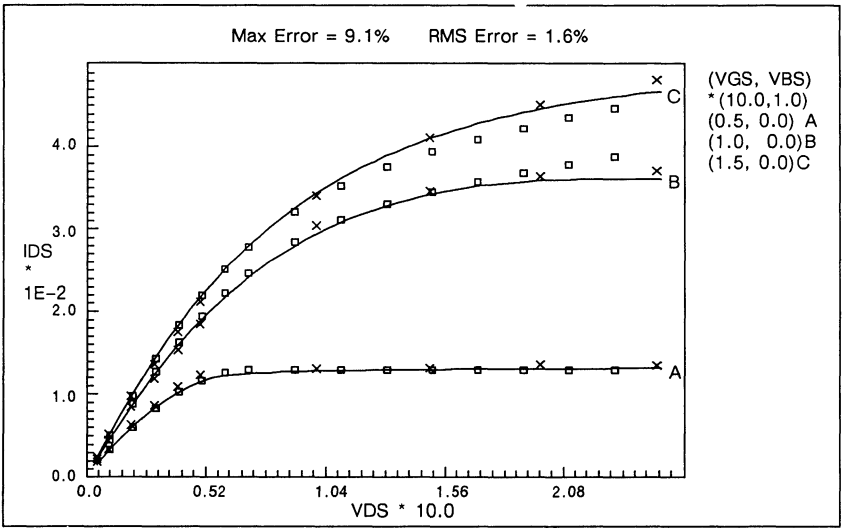



**Figure 5: Ld = 12μ Measured (Solid), Lumped (Square) and PISCES (X)**

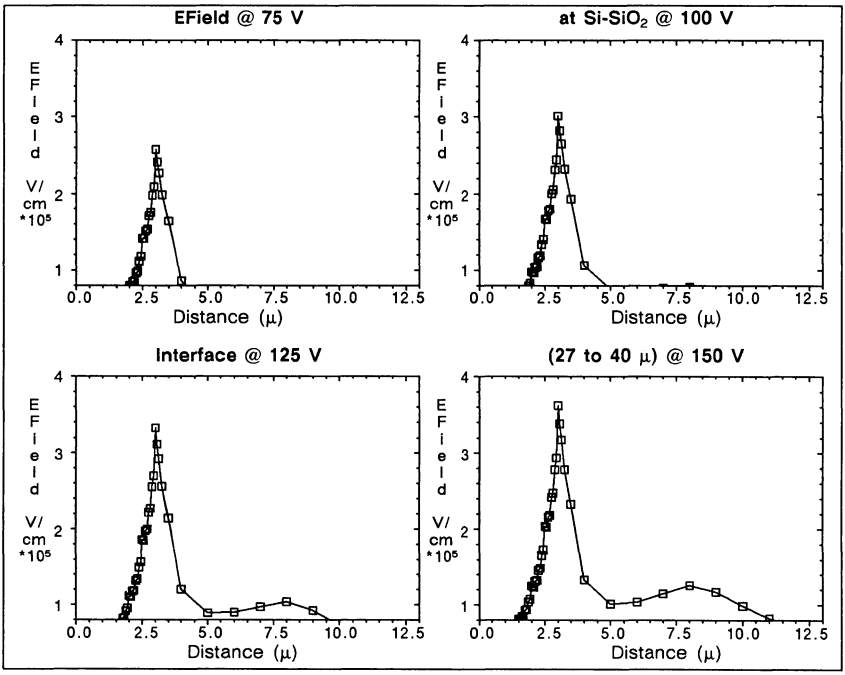



**Figure 6: PISCES Surface EField Plot**

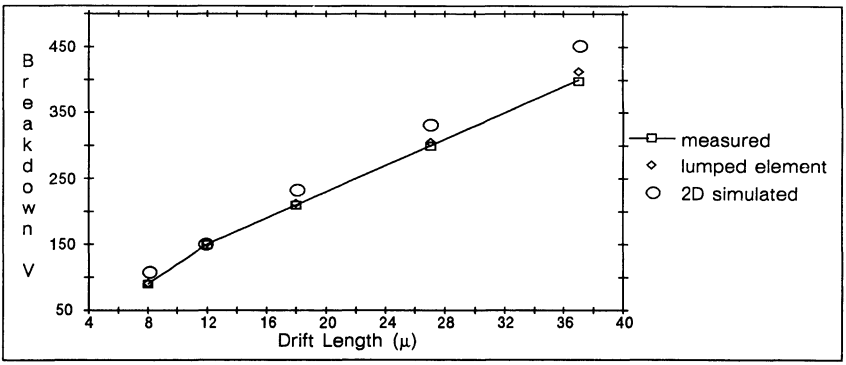



**Figure 7: Breakdown vs. Drift Length**

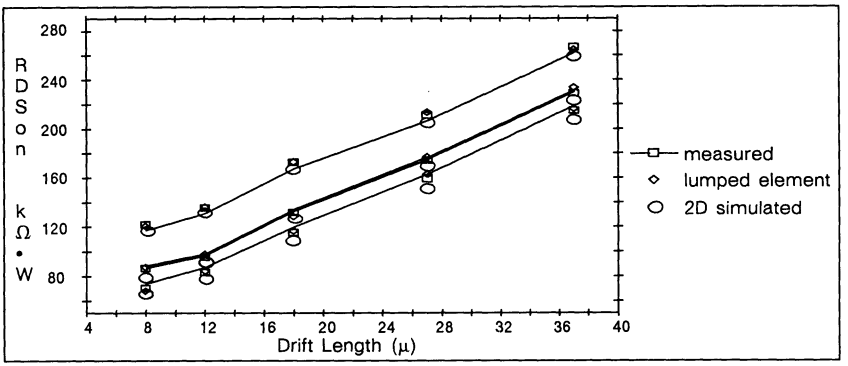



Figure 8: Normalized RDSon vs. Drift Length

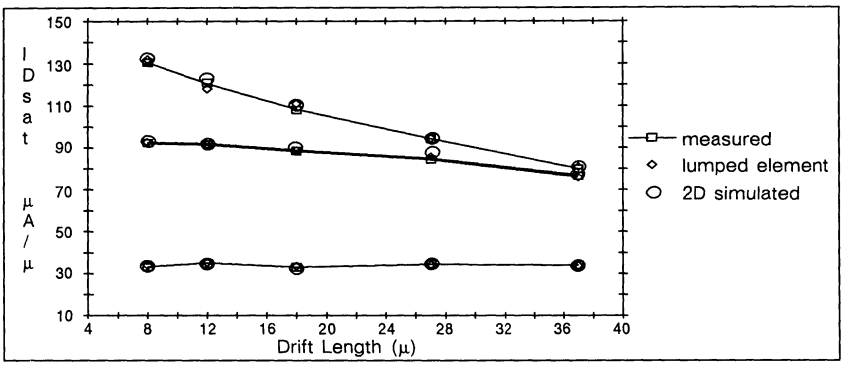



Figure 9: Normalized ID(sat) vs. Drift Length

| CONSIDERATION | MEASURED DATA LOOK-UP TABLES | LUMPED-ELEMENT SUBCIRCUIT | DEVICE SIMULATOR |
|---|---|---|---|
| basis | empirical | curve-fit | physical |
| predictive value | no | some | yes |
| measurement requirements | moderate | intensive | minimal |
| computational requirements | minimal | moderate | intensive |
| circuit simulator compatability | yes | yes | difficult |
| archive | on-going | periodic | as needed |

Table 1: Comparison of Modeling Techniques

# LATE NEWS PAPERS

## SESSION CHAIRMAN:

M. AYMAN SHIBIB
AT&T BELL LABORATORIES

Proceedings of The Electrochemical Society, PV 1987-13, 330-342 (1987)
DOI: 10.1149/198713.0330PV © The Electrochemical Society

# PHYSICAL MODELING OF LIGT STRUCTURES FOR SPICE SIMULATION OF POWER INTEGRATED CIRCUITS

R. J. McDonald, J. G. Fossum, M. A. Shibib*, and Y.-S. Kim

Department of Electrical Engineering
University of Florida
Gainesville, FL 32611

*AT&T Bell Laboratories
Reading, PA 19603

## ABSTRACT

To enable CAD of smart power integrated circuits, new physical models for lateral HV/P devices, in particular LIGT structures, are developed and implemented in SPICE. The models are charge-based, and, via regional partitioning, account for the unique features of HV/P devices unaccounted for in conventional equivalent-circuit models. The implementation of the models in the circuit simulator is flexible and allows these features (e.g., multidimensional carrier flow, conductivity modulation, latch-up, transcapacitance) to be simulated without having to sacrifice much physics through excessive empiricism. Numerical two-dimensional device simulations (with PISCES) and device measurements (of specially designed test structures) support the modeling methodology and the model parameter extraction.

## I. INTRODUCTION

To enable computer-aided design (CAD) of smart power integrated circuits (ICs), new models for high-voltage/power (HV/P) devices must be developed and implemented in circuit simulators, e.g., SPICE. The equivalent-circuit models currently built into SPICE do not properly represent HV/P devices having unique features such as multidimensional carrier flow, conductivity modulation, and latch-up.

We describe in this paper the development of new models for HV/P devices, in particular for lateral IGT (or COMFET) structures which are representative of the HV/P devices in smart power ICs. The models are physical, yet are implemented in SPICE, as we describe, through flexible techniques which do not require sacrificing physics by excessive empiricism. Thus the models can be used to aid optimal device (process) design as well as for CAD of HV/P ICs.

In the application of the modeling methodology to the LIGT, the device is regionally partitioned into three one-dimensional bipolar

transistors (BJTs) coupled to the DMOS transistor, yielding a quasi-two-dimensional model for the LIGT. The constituent device structures are represented by physical charge-based models in which currents and charges are related to junction voltages implicitly by sets of equations derived by solving the pertinent ambipolar transport problems. Charging currents in the transient model are represented by time-derivatives of the quasi-static charges, which implicitly (without capacitors) account for charge conservation and nonreciprocal transcapacitance.

The models are implemented in SPICE via user-defined controlled sources (UDCSs), which are FORTRAN subroutines accessed by the SPICE nodal analysis. The UDCSs define the systems of model equations, which are analytic but must be solved simultaneously and hence numerically. The solution of the equations is derived by the nodal analysis.

The LIGT model is supported by numerical two-dimensional device simulations with PISCES and test-device measurements, which also support the model parameter extraction. The PISCES simulations provide needed physical insight regarding, for example, current-crowding effects, and imply how the partitioning of the LIGT should be done to effectively account for coupling among the constituent devices. The test devices are specially designed lateral structures that allow experimental access to different regions of the LIGT, for different modes of operation, i.e., as a DMOS transistor, as an IGT, or as a "hybrid LIGT/DMOST" with the anode terminal shorted to the DMOST drain. This latter mode of operation depends on an internal voltage drop to forward-bias the anode junction and activate the IGT. The test structures were fabricated using a dielectric-isolation process which eliminates parasitic substrate effects. The utility of the flexible and physical modeling is emphasized by SPICE simulations of the LIGT which reflect the three possible active modes of operation. Furthermore, both static and dynamic latch-up can be simulated straightforwardly with the physical SPICE model.

## II. MODELING METHODOLOGY

We demonstrate the modeling methodology through an application to the LIGT structure illustrated in Fig. 1. The fabrication of this specially designed device is described in Sec. III. To develop a quasi-two-dimensional model, we partition the structure into one-dimensional constituent components. The basis for this partitioning rests upon physical insight gained from device measurements in the various modes of operation (PIN, DMOST, LIGT, LIGT/DMOST) and from device simulations using the two-dimensional simulator PISCES [1]. Subdividing a multidimensional structure into coupled one-dimensional devices is not uncommon, but in this case of HV/P devices the empiricism implied must be minimized through proper accounting for the underlying physics. The unique effects of significant back injection,

base-region conductivity modulation, and the associated low current gain in the BJT modules, which invalidates the commonly used SPICE Gummel-Poon model [2], necessitate new (more physical) models. We now exemplify our development of these new models, including description of a representative scheme for partitioning.

We first focus our attention on the low-gain pnp BJT constituent module. The low doping density in the wide $n^-$ base region implies that, under normal forward-mode operation, high injection will prevail throughout the base. Consequently, the base transport problem is described by the ambipolar transport equation with $p \simeq n$, the solution of which gives

$$n(x) \simeq p(x) = \frac{p(0)\sinh(\frac{W-x}{L_A})}{\sinh(\frac{W}{L_A})} \qquad (1)$$

where $p(0)$ is the hole density at the edge of the emitter-base ($p^+n^-$) junction space-charge region, $L_A$ is the ambipolar diffusion length, and $W$ is the voltage-dependent width of the quasi-neutral base, which we describe through the depletion approximation at the reverse-biased collector-base ($pn^-$) junction.

In contrast to the Gummel-Poon model [2], our (low-$\beta$) module accounts for, via (1), possibly substantial recombination in the base region. Furthermore it must account for possibly substantial recombination in the $p^+$ emitter region as well as a current-induced electric field in the conductivity-modulated base region which arises to support the quasi-neutrality. The integral of this electric field across the base region defines a voltage drop, $V_{epi}$, which causes the emitter-base junction voltage, $V_{JEB}$, to be less than the applied terminal voltage, $V_{EB}$:

$$V_{EB} = V_{JEB} + V_{epi} \quad . \qquad (2)$$

(We generically refer to the $n^-$ base region as also the epi region, even though it may not have been produced by epitaxial growth as in the case for our devices modeled in Sec. III.)

Using the quasi-equilibrium assumption, we express $p(0)$ and hence $V_{epi}$ in terms of $V_{JEB}$. For negligible recombination in the emitter-base junction space-charge region, the emitter current density, $J_E$, can be related to $p(0)$ following conventional pin-diode theory [3]:

$$J_E = \frac{b+1}{b}\{J_{N0}[\frac{p(0)}{n_i}]^2 - qD_A \frac{dp}{dx}\Big|_{x=0}\} \qquad (3)$$

where $D_A$ is the ambipolar diffusivity, b is the electron-hole mobility ratio in the base, and $J_{NO}$ is the saturation current density that defines the back injection of electrons into the quasi-neutral emitter region. The base current density, $J_B$, is the sum of the back injection current plus the integrated recombination current in the base region:

$$J_B = J_{NO}\left[\frac{p(0)}{n_i}\right]^2 + q\int_0^W \frac{p(x)}{\tau_H}\,dx \qquad (4)$$

where $\tau_H$ is the high-injection carrier lifetime. The collector current density, $J_C$, is expressed as $J_E - J_B$.

The transient modeling of the transistor is done using a charge-based method with the quasi-static approximation. The charges residing in the base ($Q_B$) and collector-base space-charge ($Q_{JC}$) regions are expressed as functions of the controlling nodal junction voltages, $V_{JEB}$ and $V_{JCB}$, and the charging currents are described as

$$\frac{dQ}{dt} = \sum_i \frac{dQ}{dV_i}\,\frac{dV_i}{dt} \quad . \qquad (5)$$

Note that in the general case the charges can depend on both $V_{JEB}$ and $V_{JCB}$, and hence (5) properly accounts for all significant transcapacitances as well as the (reciprocal) capacitances [4].

The charge-based low-β transistor module is implemented in SPICE via user-defined-control-sources (UDCSs) [4] in a novel manner which allows the circuit simulator to solve the nonlinear equations implied by (1)-(4). This is accomplished by using nonlinear UDCSs in which the controlling voltages are defined to be the junction voltages. The network representation of the pnp BJT module is shown in Fig. 2. Each element is a UDCS, which is simply a FORTRAN subroutine that describes the current (and the associated transconductance or transcapacitance) via the system of equations described above. The SPICE nodal analysis accesses the subroutines iteratively in the simulation process.

## III. APPLICATION/DEMONSTRATION

Test structures of LIGTs were fabricated using the dielectric-isolation (DI) BCDMOS technology [5] developed at AT&T Bell Laboratories. The LIGT is dielectrically isolated from the substrate and from other components to minimize parasitic effects, thus allowing access to the drain of the DMOST separately from the anode of the LIGT and making it easier to measure electrical parameters of the structure. This facilitates the demonstration of our modeling methodology, including the parameter extraction and comparisons between model predictions and device measurements.

The LIGT structure shown in Fig. 1 can operate in several modes (PIN, DMOST, LIGT, LIGT/DMOST) depending on the terminal configuration. We must therefore develop a systematic and consistent approach to modeling the various modes of operation. The physical nature of our constituent modules facilitates parameter extraction and requires minimal empirical optimization. In addition, the modular approach allows for a straightforward network representation of the LIGT structure as will be shown in this section. With the gate and drain tied to ground and the anode biased to a positive voltage, the LIGT structure operates as a pin diode. Although it may not be useful in LIGT circuit applications, the pin-diode current-voltage characteristic can be used to obtain information regarding recombination properties of the $n^-$ epi region ($\tau_H$) and of the $p^+$ region ($J_{NO}$) [6]. Such a study was undertaken and yielded, for example, $\tau_H$ = 2.6μs, which was later found to be commensurate with measured and simulated turn-off transients of the LIGT.

In the DMOST mode, the anode is left floating and the drain is set at a positive voltage relative to the source (cathode). The DMOST can be adequately modeled as a simple MOSFET (SPICE/Level 2) with a resistor, $R_{epi}$, tied to the drain which accounts for the large $n^-$ epi resistance. From a plot of the drain current versus the gate voltage in the linear region, the values for $R_{epi}$ (250Ω), the threshold voltage (2.7V), and the transconductance (K factor) can be extracted.

In the LIGT mode, the drain is left floating and a positive voltage is applied to the anode. With the gate biased above the threshold voltage, the n-channel supplies base current for the lateral $p^+n^-p$ BJT. Our quasi-two-dimensional modeling of this transistor is done by partitioning it into two one-dimensional transistors, $Q_1$ and $Q_2$, each represented by BJT modules described in Sec. II. The partitioning is defined based upon results we obtained from PISCES simulations, which show that the ratio of lateral-to-vertical injection from the $p^+$ anode (emitter) is nearly excitation-independent. The quasi-two-dimensional modeling via partitioning thus is a viable approach. The active areas for $Q_1$ and $Q_2$ are assumed to be defined by the depth of the anode diffusion and the thickness of the ($n^-$) silicon DI tub as illustrated in Fig. 1. The base width for $Q_1$ is defined by the geometry, and the base width for $Q_2$ is approximately that for $Q_1$ plus half the widths of the anode and cathode diffusions. This particular partition is indeed representative of the device as implied by (a) PISCES simulations, (b) experimental decomposition of current-voltage characteristics, and (c) relative excitations of $Q_1$ and $Q_2$ in the hybrid LIGT/DMOST mode of operation discussed later. The emitter saturation current density for $Q_1$ and $Q_2$ is extracted from the pin-diode current-voltage characteristic.

The SPICE model for the LIGT mode is shown in Fig. 3(a). It consists of a simple MOSFET and 11 UDCSs. The UDCSs labeled with the subscript one represent $Q_1$ and those with subscript two represent $Q_2$.

The current source $I_{CNPN}$ models the $n^+pn^-$ BJT at the cathode as it, when activated by the voltage drop in the p-base reflected by $R_{pB}$, effects the onset of latch-up, which is discussed later.

In the hybrid LIGT/DMOST mode of operation, the anode and drain are tied together and raised to a positive voltage relative to the source. The gate voltage, as in the DMOST mode, is above the threshold voltage. For low drain voltages, the device acts like a DMOST. The anode does not inject because it is at the same potential as the drain. As the drain current through $R_{epi}$ is increased, an internal voltage drop develops (vertically in this particular device) across the epi region. When this voltage drop becomes approximately 0.6V (viz., a diode drop) a portion of the anode ($Q_1$) becomes forward-biased and begins to inject holes into the epi base region. At this point the lateral $p^+n^-p$ transistor ($Q_1$) is turned on and, in the conventional understanding, tends to increase the total current. However, our experiments have revealed that the increase in the total current seen when this LIGT is triggered is due predominantly to an increase in DMOST current, and that the BJT current is much less than expected. The reason for this is the modulation of the epi resistance due to the injection of carriers by the LIGT. The modulation of this resistance tends to increase the DMOST current, but also tends to limit the excitation of $Q_1$, which is driven by the internal voltage drop. We note that this drop activates predominantly $Q_1$ and not $Q_2$, which is one reason why our assumed partitioning is representative. Obviously however the primary conduction mechanisms and the appropriate partitioning of a particular LIGT/DMOST depend critically on the device geometry.

The SPICE model for the hybrid device is shown in Fig. 3(b). It contains modules for the MOSFET, two resistors $R_{nS}$ and $R_{nB}$, the sum of which is $R_{epi}$, and a single lateral pnp transistor, $Q_1$. The value for $R_{nB}$ (25Ω), which we assume to be constant, is estimated by noting that it takes about 0.6V of internal voltage drop at the trigger current to turn on $Q_1$. The modulation of $R_{epi}$ is semi-empirically accounted for in $R_{nS}$ which is simulated by a UDCS. In that UDCS, we let

$$R_{nS} = R_f + \frac{R_0}{1 + \frac{\bar{p}}{N_{epi}}} \qquad (6)$$

where $N_{epi}$ is the doping density ($5\times10^{14}cm^{-3}$) in the epi and $\bar{p}$ is an average injected carrier density in $Q_1$ defined from (1). Using measured current-voltage characteristics [see Fig. 4(a)] at the onset of and immediately after the triggering of $Q_1$, we extract values for $R_f$ (100Ω) and $R_0$ (125Ω), independent of the gate voltage.

Both the LIGT mode and the LIGT/DMOST mode can undergo latch-up. Static latch-up occurs when the collector current of $Q_1$, $I_{C1}$, produces

approximately a diode voltage drop across the lateral resistance $R_{pB}$ in the base of the parasitic $n^+pn^-$ transistor. When this voltage drop develops, electrons are injected by the $n^+pn^-$ BJT into the base of $Q_1$, thus increasing its conduction. Removal of the gate voltage at this point will not turn off the LIGT since the regenerative process involving $Q_1$ and the $n^+pn^-$ BJT predominates. Our simulations and experiments indicate that $Q_2$ plays only a minor role in determining the latch-up current. This is due in part to the deep $p^+$ cathode diffusion and to the current path associated with $I_{C2}$. The hybrid mode has a much higher latch current because a large percentage of the total current is carried by the DMOST rather than in $I_{C1}$. However, for both modes of operation at the onset of latch-up, the emitter current of $Q_1$, $I_{E1}$, is approximately the same value.

The onset of latch-up in both the LIGT and the LIGT/DMOST modes is simulated by the model (Fig. 3) via a voltage-controlled current source, $I_{CNPN}$, in which the controlling voltage is developed across the $n^+pn^-$ base resistor, $R_{pB}$. The injection of electrons from the $n^+pn^-$ BJT is an exponential function of the aforementioned voltage drop, and depends on the Gummel number [2] ($\propto 1/R_{pB}$) of the p base region. Note in Fig. 3 that dynamic latch-up is also accounted for in the models. In this case, the charging current $dQ_{JC1}/dt$ contributes to the voltage drop across $R_{pB}$ and hence induces the latch-up.

## IV. SIMULATIONS/VERIFICATION

In Fig. 4(a) we show measured current-voltage curves for the hybrid LIGT/DMOST mode of operation for three different values of gate voltage. It can be seen that the trigger current for IGT ($Q_1$) excitation is approximately 23mA, independent of $V_G$. The increase in total current immediately after the triggering is due predominantly to an increase in the DMOST current as discussed in Sec. III. In Fig. 4(b) we show corresponding SPICE model current-voltage curves. Note that the triggering points for the hybrid mode of operation are reliably predicted, as well as the latch-up onsets. We note however that although our model faithfully simulates the DMOST region, the predicted conductance in the hybrid mode is less accurate. This inaccuracy is due in part to the semi-empirical approximate representation (6) of the modulated DMOST resistance. More physical UDCS modeling of this highly nonlinear modulation could be done to improve the accuracy. However to effect a generally valid model, a more physical DMOST module should be developed to replace the simple SPICE/Level 2 model.

In Fig. 5 we compare measured and model-simulated transient turn-off characteristics of the LIGT. At time t=0 the gate voltage is removed and a typical two-phase turn-off transient is observed [7]. Our model simulations are in good agreement with experiment. The turn-off time may seem faster than expected for a lifetime of 2.6μs, but this is due to the substantial $p^+$-emitter recombination [first

term in (4)] and its expedition of the turn-off transient [7]. We stress that such transient simulations are not possible with conventional SPICE transistor models. We also note that if the gate voltage is removed fast enough, the corresponding displacement current associated with the collector-base junction may be sufficient to forward bias the $n^+pn^-$ transistor and subsequently cause dynamic latch-up as discussed previously.

## V. SUMMARY

We have developed a device modeling methodology needed for the CAD of HV/P ICs that is also useful for optimal device (process) design. The methodology is based on a regional partitioning of LIGT structures through physical insight gained from numerical simulations (PISCES) and experimental results (special test devices). The regional partitioning of a lateral structure defines an array of new one-dimensional device modules, which properly (physically) model the unique features of HV/P devices. We have demonstrated this flexible methodology on an LIGT test structure for all possible active modes of operation. Both dc and transient measurements support the modeling methodology.

The constituent charge-based modules, which are easily implemented into SPICE via UDCSs, allow for a network representation of the structure that can be used to simulate the device under actual circuit conditions, a feature most device simulators do not have. Consequently, the methodology may be useful in optimizing device design under an actual circuit environment, in addition to the CAD capability it affords.

## ACKNOWLEDGEMENT

This work was supported in part by the National Science Foundation under Grant No. ECS-8419427.

## REFERENCES

1. M. R. Pinto, C. S. Rafferty, and R. W. Dutton, PISCES-II User's Manual, Stanford Electronics Laboratories, Stanford University, Stanford, CA, 1984.

2. I. E. Getreu, Modeling the Bipolar Transistor. New York: Elsevier, 1978.

3. F. Berz, R. W. Cooper, and S. Fagg, "Recombination in the End Regions of PIN Diodes," Solid-State Electron., vol. 22, pp. 293-301, 1979.

4. S. Veeraraghavan, J. G. Fossum, and W. R. Eisenstadt, "SPICE Simulation of SOI MOSFET Integrated Circuits," IEEE Trans. Computer-Aided Design of ICAS, vol. CAD-5, pp. 653-658, Oct. 1986.

5. C. A. Goodwin, M. A. Shibib, R. A. Furnanage, C. Y. Lu, P. C. Riffe, N. S. Tsai, and J. L. Schmoyer, "A Dielectrically Isolated Bipolar-CMOS-DMOS (BCDMOS) Technology for High Voltage Applications," this ECS Symposium, Philadelphia, PA, May 10-15, 1987.

6. R. J. McDonald, J. G. Fossum, and M. A. Shibib, "A Physical Model for the Conductance of Gated p-i-n Switches," IEEE Trans. Electron Devices, vol. ED-32, pp. 1314-1320, July 1985.

7. J. G. Fossum and R. J. McDonald, "Charge-Control Analysis of the COMFET Turn-Off Transient," IEEE Trans. Electron Devices, vol. ED-33, pp. 1377-1382, Sept. 1986.

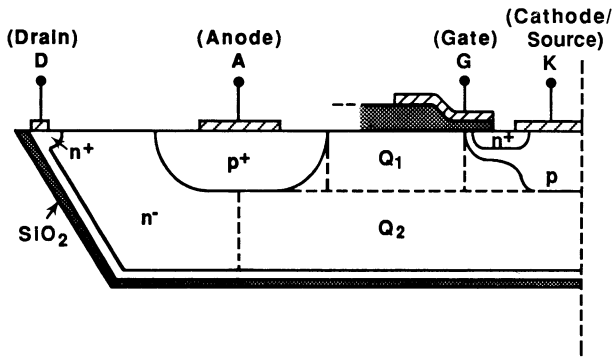



Fig. 1. Dielectrically isolated LIGT structure. The anode (A) is also referred to as the emitter of the constituent $p^+n^-p$ BJT. The cathode (C) is also referred to as the collector of the $p^+n^-p$ BJT and the source of the DMOST. The dashed lines indicate the partitioning of the BJT into two one-dimensional transistors, $Q_1$ and $Q_2$.

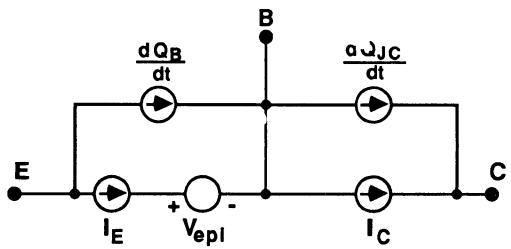



Fig. 2. Basic network representation of the low-β transistor module (forward mode). In the SPICE implementation, all elements are represented by UDCSs.

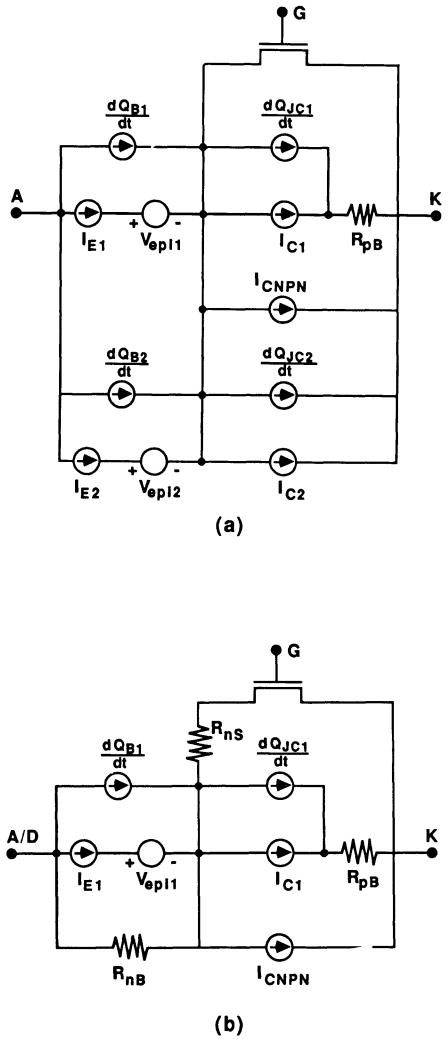



Fig. 3. Network representation of LIGT structure in (a) the LIGT mode of operation and (b) the hybrid LIGT/DMOST mode of operation.

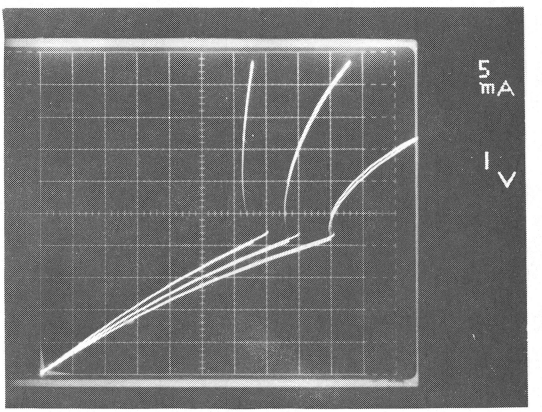



Fig. 4(a). Measured anode/drain current-versus-voltage characteristics for the hybrid LIGT/DMOST for gate voltages of 6V, 8V, and 12V. The traces terminate at the onsets of latch-up (which is not shown for the $V_G$ = 6V curve).

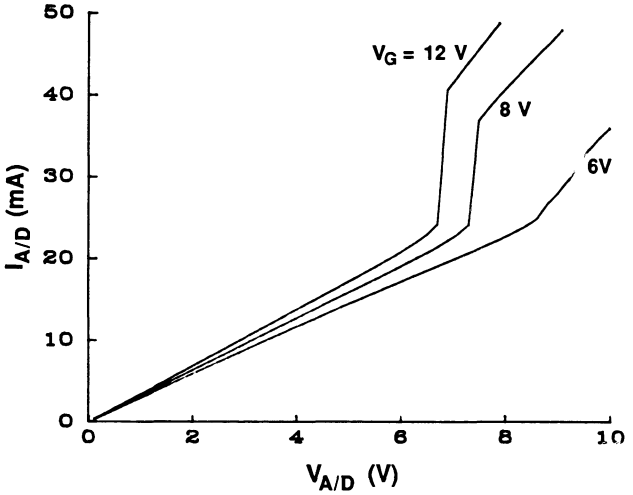



Fig. 4(b). SPICE model predictions for the hybrid LIGT/DMOST current-voltage characteristics, which correlate with the measurements in Fig. 4(a).

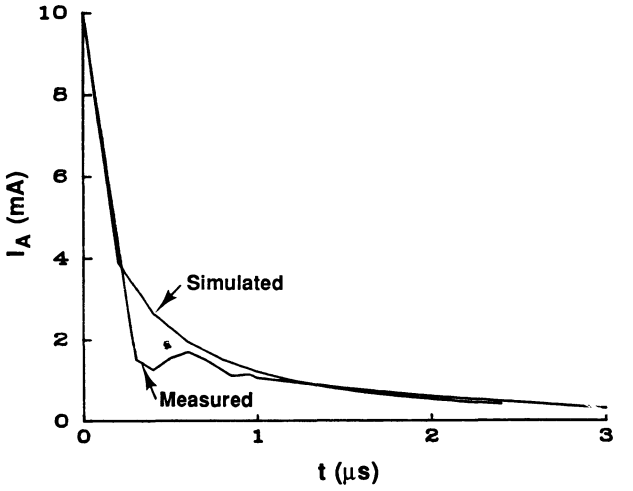



Fig. 5. Measured and simulated LIGT turn-off current transient for a 4.5V supply and a resistive load of 300Ω. The on-state current is 10 mA. The gate voltage was dropped at t=0 from 8V to zero in 200ns.

Proceedings of The Electrochemical Society, PV 1987-13, 343-352 (1987)
DOI: 10.1149/198713.0343PV © The Electrochemical Society

# MAGNETIC CZOCHRALSKI SILICON FOR POWER DEVICES

F.A. Selim and L.B. Major

High Voltage Systems Operation
General Electric Co.
205 Great Valley Parkway
Malvern, Pa. 19355

and

G.F. Fiegl
Unisil Corporation
405 National Avenue
Mountain View, Pa. 94043

ABSTRACT:

Magnetic Czochralski silicon (MCZ) with improved dopant homogeneity and low impurity concentration, i.e. oxygen and carbon, is grown for high voltage power devices. The radial resistivity was found to be as uniform as in FZ conventionally phosphorus doped Si but less uniform than FZ-NTD. MCZ Si showed no resistivity shift after high temperature diffusion. High lifetimes above 100 usec were achieved in 160Ω-cm Si after Al, Ga, B and phosphorus high temperature diffusions. High voltage rectifiers and thyristors processed using MCZ and FZ-NTD Si showed identical device characteristics. High blocking voltages and low on-state voltages with 80-100% of the theoretical values were achieved.

## INTRODUCTION:

The development of high power silicon thyristors and rectifiers has increased the demand for high resistivity and large diameter crystals with a dopant uniformity which exceeds the conventional Czochralski and float-zoned growth techniques. Moreover, power devices have been limited in current carrying capability by the crystal diameter of the FZ Si limitations.

The majority of semiconductor devices, i.e. ICs, are fabricated from CZ Si. CZ Si is, therefore, more available and can be obtained in larger diameter crystals without the limitations of the FZ technique. The major problem areas of CZ Si are: purity, oxygen contents, non-uniform distribution of dopant imposed by growth technique and residual electrically active impurities e.g. C, B, Al and P. The major impurity, however, is oxygen.

CZ Si with improved dopant homogeneity and low impurity concentration can be grown using magnetic field and improved crucible technologies[1]. However, the ultimate test for using this material is in processing discrete large area power devices. In the power device material utilization, where high uniformity - high resistivity Si is required, NTD-FZ Si remains the main stay in spite of serious deficiencies, such as problems of retaining high minority carrier lifetimes through NTD annealing in production [2,3]. The present trend to develop high power Si diodes, thyristors and GTO's is, hence, limited by the material technology, availability and cost of high resistivity large diameter FZ Si crystals.

The magnetic CZ Si promises to be a fruitful and cost-effective alternative. Although low cost large diameter 1000 ohm-cm uniform magnetic CZ wafers are feasible in the near future and can be used for high power devices, its applicability to high power devices has not been demonstrated. Meanwhile, change in the material properties as a function of the high temperatures processing and long diffusion times, required by deep junctions for power devices, have not been examined.

The objective of this work is to demonstrate the utilization of MCZ Si in processing high voltage diodes and thyristors. In this paper, the processing and characterization of 77mm MCZ Si for diodes and thyristors with voltage capability up to 4500 volts is presented. Device and material evaluation including resistivity uniformity, resistivity shift, lifetime and device characteristics are compared with standard NTD FZ Si.

EXPERIMENTAL:

The starting Si material used for these studies was N-type (phosphorus doped), MCZ Si, 1:1:1: orientation with a bulk resistivity of 160Ω-cm. The material was grown while applying a magnetic field of approximately 2500 Gauss by way of external magnet. Convective flow during crystal growth was reduced to the point where oxygen incorporation in the crystal became independent of free convection[4]. The resultant oxygen concentration level was 2.5 PPM ASTM 79[5]. (see Curve C Figure 1).

Further increase of the magnetic field to approximately 4500 Gauss applied to a 20 kg charge size has shown a reduction in melt temperature oscillations to a maximum of $0.2^{o}C$. Due to this highly stable temperature condition, the growth velocity of the crystal could be markedly improved. At the 4000 to 4500 Gauss level, free convection is virtually eliminated with the benefit of an undisturbed melt surface which in turn produces an ingot with a ripple-free appearance. Typical pull speed variations for 100 mm diameter <100> crystals observed

in conventional Cz growth for maintaining diameter variations of ± 1mm can be reduced by 50% when free convection in the melt has been sufficiently decreased.

Crystal melt interface morphology and meniscus are affected by the "magnetic viscosity" of the melt. The convex interface shape towards the melt is reduced while the meniscus height shows an increase for given growth parameters. Material characteristics of the ingots grown from Cz systems with magnetic fields applied generally show greater uniformity, both in longitudinal direction and in radial direction of the ingot.

100mm diameter < 100 > material, boron doped, showed no bulk stacking faults after two hours oxidation in wet oxygen at 1000°C, and no oxide precipitates after annealing in an argon atmosphere at 1000°C for fourteen hours. Phosphorus doped material showed a 5-10% reduction of radial dopant inhomogeneities measured by the spreading resistance method.

Convective striation patterns familiar to Cz growth could not be observed in phosphorus or boron doped material at > 2000 Gauss.

Donor formation at 450°C heat treatment cycles over several hundred hours did not show any effect on resistivity. Carbon concentration in the crystal was 0.05 PPM. Convective striation patterns familiar to CZ growth were not observed[6]. Minority carrier lifetime measurements, after several heat treatment cycles, showed greater uniformity and less deterioration compared with standard CZ Si.

High voltage junctions were processed through high temperature Al, G, B and P diffusions for either diode or thyristor devices. Devices were processed using FZ-NTD Si along with the MCZ Si to serve as control samples during diffusion. Resistivity uniformity, diffusion profiles and minority carrier lifetime were measured after each diffusion cycle. The open circuit decay technique was used to measure minority carrier lifetime after each diffusion.

Diodes and thyristors were evaluated for reverse-forward I-V characteristics, on-state voltage and recovery current, dv/dt, di/dt and device yield.

RESULTS AND DISCUSSION:

The four point probe technique was used to study resistivity uniformity and/or resistivity shift before and after diffusion. A typical 4-point resistivity measurement across wafer distance on both MCZ and FZ-NTD Si is shown in Figure 2. FZ-NTD Si showed more resistivity uniformity as expected. Resistivity variation in MCZ Si indicates the inhomogeneities in the phosphorus doping of the bulk

silicon crystal. However, there is no apparent resistivity shift after high temperature diffusion, a confirmation of low carbon and oxygen concentration in the starting Si material.

Al diffused diodes were processed using a 25 um junction depth. Reverse voltages, reaching 86% of the theoretical blocking capability were achieved. A typical FZ-NTD P-N junctions achieved 91% of the theoretical blocking voltage. The difference is attributed to the lower uniformity in resistivity. However high lifetime and diffusion profiles were identical to FZ-NTD devices. Table (1) shows a comparison of some junction characteristics of both MCZ and NTD-FZ Si.

NPNP SCR structures (Fig. 3) were processed and devices were evaluated and compared with standard FZ-NTD production devices. Lifetimes of diffused junctions after Al, GA, B and P are shown in Table 2. It is apparent that high lifetime can be achieved throughout the device processes. Other device characteristics such as on-state voltage, recovery current, dv/dt and di/dt were measured and compared with standard SCR production (Table 3).

## CONCLUSION:

MCZ Si with high resistivity and low oxygen and carbon concentration can be grown for high voltage power devices. The radial resistivity of MCZ Si is as uniform as conventional phosphorus doped Si but less uniform than FZ-NTD Si. The material resistivity shows no shift after high temperature processing. High minority carrier lifetime were measured after high temperature processing. Diodes processed using MCZ Si having a resistivity of 160 $\Omega$-cm showed blocking voltage of 4500V. Thyristors processed with same material showed a blocking voltage of 3500 and 3700 volts in forward and reverse direction, respectively, and 1.2 volts on-state voltage at 2000A and 120$^{o}$C.

It is concluded that MCZ Si yields high voltage power devices characteristics equivalent to devices processed with the FZ Si which is limited in diameter to the FZ growth techniques. When MCZ Si is doped with the NTD process, it would result in a higher resistivity uniformity.

## ACKNOWLEDGEMENT:

This work was partially sponsored by the Electric Power Research Institute (EPRI). The authors are grateful to Drs. N.G. Hingorani and H. Mehta for their support during this study.

REFERENCES:


1. K. Hosikawa, H. Kohda, and H. Hirata, Jap. J. Appl. Phys Vol. 23, No. 1, 1984 pp. L37-L39.

2. F.A. Selim, IEEE Electron Devices Letters, Vol. EDL-4, No. 7, P. 219, 1983.

3. M.H. Janus and O. Malmros, IEEE Trans. Electron Devices, Vol. ED-23, No. 8, p. 797, 1976.

4. K. Hoshi, N. Isawa, T. Suzuki and Y. Ohkubo; J. Electrochem. Soc., Vol. 132, No. 3, pp. 693-700, 1985.

5. T. Abe etal., ECS Semiconductor Silicon, P.54, 1981.

6. K.M. Kim and P Smetana, J. Appl. Phys., Vol. 58, No. 7, P. 2731, 1985.

TABLE 1. COMPARISON OF MCZ AND FZ-NTD SI P-N JUNCTION DIODE CHARACTERISTICS

| | MCZ | FZ |
|---|---|---|
| BLOCKING VOLTAGE $V_B$ (VOLTS) @ 2.5MA | 3700 | 3100 |
| % OF $V_B$ (THEORY) | 86 | 91 |
| (USEC) | 30 | 25 |
| JUNCTION DEPTH $X_J$ (UM) | 25 | 25 |
| RESISTIVITY (OHM CM) | 144-176 | 100-124 |

TABLE 2. LIFETIME (USEC.) COMPARISON AFTER AL, GA, B, P DIFFUSION

| | MCZ | FZ |
|---|---|---|
| AL | 30 | 29 |
| GA | 61 | 55 |
| B | 90 | 70 |
| P | 104 | 82 |

TABLE 3. TYPICAL CHARACTERISTICS OF PACKAGED DEVICES FOR THYRISTORS PROCESSED WITH MCZ AND NTD-FZ SI

| | MCZ | FZ-NTD |
|---|---|---|
| BLOCKING VOLTAGE @ R.T. (VOLTS) @ 20 UA LEAKAGE | | |
| FORWARD ($V_{DM}$) | 3500 | 3300 |
| REVERSE ($V_{RM}$) | 3700 | 3200 |
| ON-STATE VOLTAGE (V) $V_{TM}$ @ 2KA | 1.16 | 1.15 |
| RECOVERY CURRENT $I_R$ (A) | 71 | 57 |
| DV/DT (V/USEC) | 1400 | 1400 |
| DI/DT (A/USEC) | 150 | 150 |
| (TO 1500V FOR 1 MIN. @ 100°C) | | |

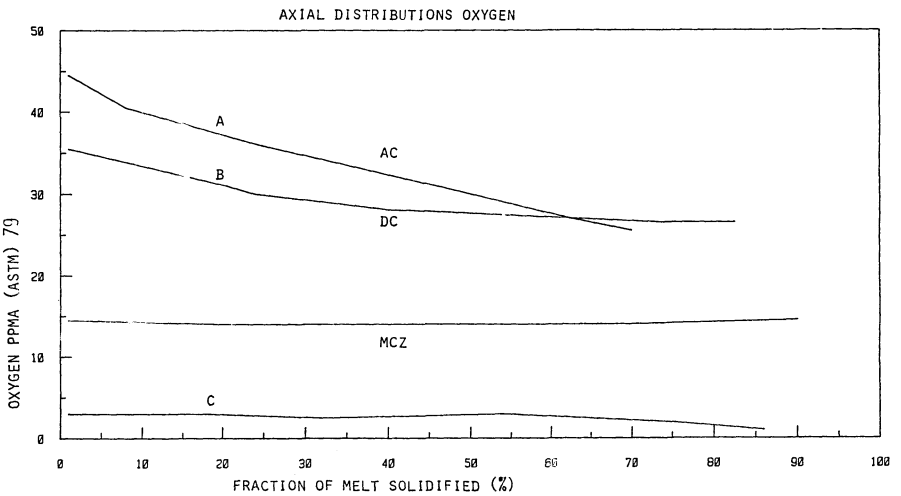



FIGURE 1. EFFECTS OF VARIOUS MAGNETIC FIELDS ON OXYGEN INCORPORATION IN THE CRYSTAL.

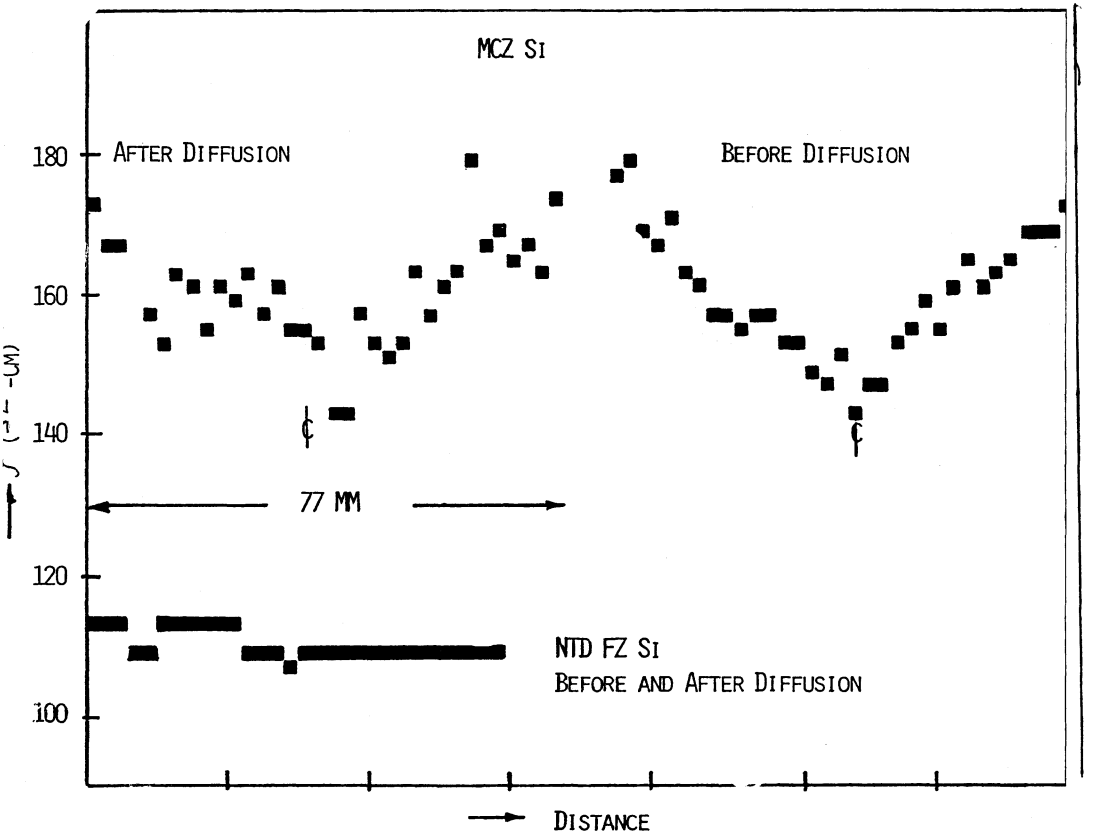



FIGURE 2. RESISTIVITY (Ω-CM) AS A FUNCTION OF DISTANCE (ARBITRARY UNITS) ACROSS WAFER DIAMETER.

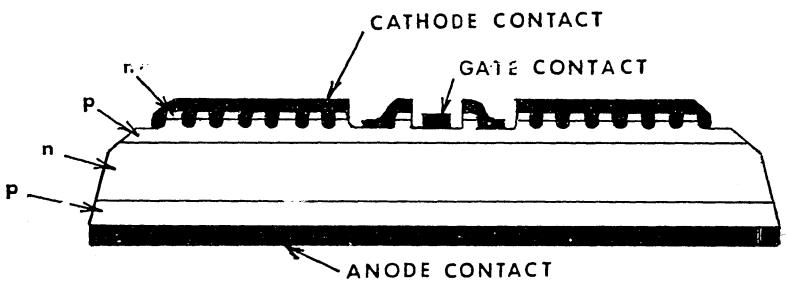



FIGURE 3. MULTI-DIFFUSED NPNP THYRISTOR STRUCTURES USED TO EVALUATE MCZ SI

INDEX


| WORD | PAGE |
|---|---|
| access resistance | 159 |
| accumulated layer | 157 |
| ambipolar transport | 332 |
| annealing (of Pt) | 197 |
| annealing induced acceptor | 200 |
| area ratio | 170 |
| arsenic drift in oxide | 243 |
| ATLAS | 96 |
| Auger microscope | 263 |
| automotive | 11 |
| barrier lowering | 265 |
| BCDMOS | 79,118 |
| BDL (buried drain lateral) | 53 |
| bipolar power transistor | 188 |
| BJT module | 332 |
| breakdown | 318,319,321 |
| breakdown voltage | 196 |
| breakdown voltage degradation | 250 |
| buried conductive layer | 243 |
| CANDE | 23 |
| capacitance | 226 |
| capacitor coupling | 100 |
| cascode | 44 |
| cathode-short structures | 175 |
| CFO model | 267 |
| channel length | 42 |
| characteristics | 174 |
| charging currents | 333 |
| chip surface potential | 253 |
| clock frequency | 56 |
| CMOS | 41 |
| COGMOS thyristor | 100 |
| collector-base breakdown | 188 |
| communications | 79 |
| compensation (by Pt in Si) | 199 |
| Complementary high voltage MOSFETS | 51 |
| conductivity modulated devices | 90,136 |
| contamination | 187 |
| corona | 251 |
| corona as a contact | 252 |
| crystallization from the melt | 241 |
| current pinching | 161 |
| current source | 54 |
| Czochralski | 343 |

deep depletion 228
DGDMOS 83,118
DI wafer 106
DI with single crystal substrates 241
dielectric isolation 118,241,96,133,135
distributed model 158
DMOS, lateral 118,318
DMOST 334
double offset gate 101
Drain extension 35
drift 318
EPIC method 97
equivalent circuit 174
etch and epitaxy 68
etch refill 69
extended drain 41
extraction program 177
failure analysis 255
Field plate 33,254
fields - vector addition 254
flat panel display 98,51
floating bias operation 101
Frenkel carrier generation 265
gate overlap 44
gate structure 176
gate-cathode resistance 176
graphical saturation 166
GTO 82
H P-ch. MOS 35
H-Bridge 20
heat treatment (of Pt doped Si) 200
HFIELDS 32
High side 11
humidity 232
HVCMOS 60
hybrid LIGT/DMOST 335
IDAS 32
IGTs 91
jfet, parasitic 319
JFETs 79
junction isolation 31,134
lamp furnace 242
latch up 336
lateral DMOS 90
LDMOS 53
LDMOST 297
LEADFRAME 221
leakage current vs temperature 108
LEGO 241
LIGT 334,280

LIGT - clamped anode 311
ligt - transient analysis 295
LIGT - turn off time 316
Low Leakage diode 33
MCT 150
MCZ 343
MEDUSA 298
minority carriers 229
model, lumped element 319
model, MOSFET circuit simulation 319
modelling 43,318
MODSIP 218
MOS, depletion mode 319
MOS, enhancement mode 319
MOS, LDD 319
Multipower BCD 31
offset drain 54
oxide thickness 162
oxygen donors 189
PADRE 296
pedestal 69
pipes 109
PISCES 43,318
plasma damage 110
plasma oxide annealing 110
platinum - in high voltage diodes 195
platinum-annealing of 194
platinum-diffusion of 194
pn junction isolation 52
PNPN 82
PNPN - parasitic 280
Poisson's equation 320
potential profiling 263
potential screening 266
power ICs 96
proton irradiation 152
push pull circuit 99
quasi-analytical model 163
quasi-saturation 167
quasi-saturation current 168
recombination 199
relative humidity 252
relaxation time 227
RESURF 45
reverse recovery time 198
Ron*area 34,121
Ron*Z 35
Rutherford backscattering 189
SCR's 90
selenium 187

self isolated 134,319
semi well isolation 52
shift resistor 99
simulation 177
simulation, 2d 318
SIP 218
SIPMOS 11
SIPOS 226,232,262
sipos conductivity 266
sipos model 264
sipos physical structures 268
Smart PIC 31
SMARTpower 20
solenoid driver IC 98
SORT 61
spectrometry 189
SPICE 45,333,178
spreading resistance 196
SSB model 268
substrate induced field 262
surface charging 251
surface current distribution 260
surface ions 250
SUXES 318
Tapered Oxide 32
temperature effects 169
three d effects 290
threshold voltage shift 110
thyristor 97
totem pole circuit 55
transient 228
tube resistance 161
turn off - LIGT 283
turn-on current 175
twin tub 60
VDMOS 157,53
Vertical DMOS 33
Walk-out 34,255
weak avalanche 42