PROCEEDINGS OF THE SECOND
INTERNATIONAL SYMPOSIUM ON

CLEANING TECHNOLOGY IN SEMICONDUCTOR DEVICE MANUFACTURING

Edited by

Jerzy Ruzyllo
Penn State University
University Park, Pennsylvania

Richard E. Novak
FSI International
Chaska, Minnesota

ELECTRONICS AND DIELECTRIC SCIENCE AND TECHNOLOGY DIVISIONS

Proceedings Volume 92-12

THE ELECTROCHEMICAL SOCIETY, INC., 10 South Main St., Pennington, NJ 08534-2896

Library of Congress Catalog Number: 92-71447
ISBN 1-56677-012-2
Printed in the United States of America

PREFACE

In 1988, the Technical Program Planning Committee of the Electrochemical Society agreed to sponsor a series of symposia devoted to semiconductor cleaning technology. Under the auspices of the Electronics and Dielectrics Science and Technology Divisions of the Society, the First International Symposium on Cleaning Technology in Semiconductor Device Manufacturing was held during the Society Fall Meeting in October 1989, in Hollywood, Florida. This event was noteworthy because it was the first conference devoted solely to wafer cleaning technology and for the first time this element of semiconductor device fabrication was recognized as a legitimate, important part of the microelectronic manufacturing science and engineering.

The attendance, as well as the number and the quality of papers presented at this first "Cleaning Symposium", was beyond expectation. This confirmed that a meeting devoted solely to wafer cleaning technology was both needed and timely. The proceedings volume from that first symposium has been widely cited and enjoys a wide-spread popularity. The initial success solidified even further, the commitment of the Society and organizers to the series of symposia on the same topic which would assure a continuing exchange of views and ideas on wafer cleaning technology. Consequently, these symposia are organized on a biannual basis during the Fall Meetings of the Electrochemical Society.

This softbound proceedings volume contains the papers presented at the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing held at the Electrochemical Society Fall meeting in Phoenix, Arizona, October 14-18, 1992. The symposium was sponsored jointly by the Electronics and Dielectrics Science and Technology Divisions of the Society.

The presentation of the second symposium demonstrated significant progress in the two years since the first symposium in the fundamental understanding of the issues involved in advanced wafer cleaning. This was readily noticeable in the technical content of the presented papers. The large number of participants and their probing questions during the sessions and in informal settings attested to wafer cleaning being viewed as a critical manufacturing process. For a long time following the establishment of the basic approach to wafer cleaning twenty years ago, most of the developments in wafer cleaning were based on the experimental findings with only limited contribution from reasoning based on scientific considerations. Recent years have shown this situation to be changing rapidly and many papers in this volume are an excellent example of this trend. Our understanding of surface reactions involved in both wet and dry cleaning is clearly growing. Newly developed tools have allowed innovative approaches to wafer cleaning resulting in increased production yield and improved device reliability. Consequently, we are now better prepared, intellectually and technically, to make decisions concerning the directions of further R & D efforts and industrial implementation of new or modified wafer cleaning methods. As this trend continues, wafer cleaning technology will become a key process that will help determine the feasibility of using a fully integrated

cluster tool process. The organizers hope that the first two "Cleaning Symposia" together with the third one to be held in October 1993, will have a noticeable contribution to this evolution.

We would like to take this opportunity to thank all symposium authors and participants who were responsible for the informative and productive meeting. In particular, we would like to thank all invited speakers for their excellent contributions. Moreover, we are pleased to acknowledge our colleagues who assisted us in editing this volume and who chaired the symposium sessions.

Richard E. Novak
Jerzy Ruzyllo

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FACTS ABOUT THE ELECTROCHEMICAL SOCIETY, INC.

The Electrochemical Society, Inc., is a nonprofit, scientific, educational, international organization founded for the advancement of the theory and practice of electrochemistry, electrothermics, electronics, and allied subjects. The Society was founded in Philadelphia in 1902 and incorporated in 1930. There are currently over 5000 scientists and engineers from more than 40 countries who hold individual membership; the Society is also supported by more than 100 corporations through Patron and Sustaining Memberships.

The technical activities of the Society are carried on by Divisions and Groups. Local Sections of the Society have been organized in a number of cities and regions.

Major international meetings of the Society are held in the Spring and Fall of each year. At these meetings, the Divisions and Groups hold general sessions and sponsor symposia on specialized subjects.

The Society has an active publications program which includes the following.

JOURNAL OF THE ELECTROCHEMICAL SOCIETY - The JOURNAL is a monthly publication containing technical papers covering basic research and technology of interest in the areas of concern to the Society. Papers submitted for publication are subjected to careful evaluation and review by authorities in the field before acceptance, and high standards are maintained for the technical content of the JOURNAL.

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MONOGRAPH VOLUMES - The Society has, for a number of years, sponsored the publication of hardbound Monograph Volumes, which provide authoritative accounts of specific topics in electrochemistry, solid state science and related disciplines.

BEHAVIOR OF HYDROGEN AND FLUORINE BONDS ON CHEMICALLY CLEANED SILICON SURFACES

M. Hirose, T. Yasaka, K. Kanda, M. Takakura and S. Miyazaki
Department of Electrical Engineering, Hiroshima University
Higashi-Hiroshima 724, Japan

The chemical stability and the oxidation kinetics of hydrogen-terminated silicon surfaces obtained by HF or pH modified buffered HF treatment have been studied by x-ray photoelectron spectroscopy and FT-IR-ATR. Silicon-fluorine bonds as a minority species on the as-treated surface appear to remain at reactive sites such as atomic steps and chemically passivate the surface against oxidation. The layer-by-layer oxidation observed for HF-treated surfaces is explained by a model in which the oxidation starts from step edges and propagates along the surface. In consistence with this model a step-free Si(111) surface prepared by pH modified BHF has no detectable fluorine bond due to the absence of reactive sites and hence the surface is hardly oxidized for 300 min in clean room air.

INTRODUCTION

Preparation of native-oxide free silicon surfaces is needed for various process steps of advanced ULSI fabrication. The surface chemical cleaning prior to ultra-thin gate oxide growth, metal contact formation and selective CVD or epitaxy is particularly important. Also, the surface roughness on atomic scale must be minimized in the gate oxide/silicon interface to improve the device performance and reliability. HF or BHF treated silicon surfaces are terminated mostly with hydrogen and the bonding configurations have been identified by multiple internal infrared reflection spectroscopy (1,2). Ideal hydrogen termination has been realized for an Si(111) surface treated by pH modified BHF, while an Si(100) surface is shown to be atomically rough (3). Fluorine coverage on an HF treated Si(100) surface is about 10 % and reduced to a few % by 10 min water rinse. This minority fluorine plays significantly important role at the onset of silicon surface oxidation (4). In this paper we describe the growth mechanism of native oxide on Si surfaces treated in aqueous HF or pH modified BHF solutions in connection with the behavior of fluorine and hydrogen bonds.

EXPERIMENTAL

Si(100), (110) and (111) cz wafers with donor or acceptor concentrations of $10^{15} \sim 10^{18}cm^{-3}$ were used as substrates. They were

cleaned in an organic solution, boiled in $H_2O:H_2O_2:HCl$ = 86:11:3 for 10 min and dipped in $H_2O:H_2O_2:NH_4OH$ = 4:1:1 for 2min (not boiled). The wafer was finally dipped in a 5% HF solution or buffered HF (BHF) solutions (40% NH_4F:50% HF=4:1 or 7:1). Si-H bonds on the chemically treated wafer were examined by FT-IR-ATR (Attenuated Total Reflection) in which the incident light was S- or P-polarized and the ATR crystal was Ge. The silicon wafer was stored in clean room air or in pure water. At each step of storage time, the chemical bonding features of the Si surface was measured by x-ray photoelectron spectra (XPS) of Si_{2p} and F_{1s} core levels. The photoelectron escape angle between the detector axis and the direction normal to the Si surface was kept at 75° for the surface sensitive measurements.

RESULTS AND DISCUSSION

Fluorine bonds on HF treated surfaces

Fluorine coverage on an HF cleaned Si surface depends upon HF concentration and wafer rinse time as shown in Fig. 1. It should be noted that two orders of magnitude variation of HF concentration causes rather little change in the fluorine coverage. Exceptionally high fluorine coverage at 50% HF without water rinse could be attributed to adsorbed HF molecules on the surface because it is dramatically reduced by 1 sec water rinse. The result of Fig. 1 suggests that fluorine selectively remains at chemically reactive sites such as atomic steps or surface defects where silicon etching in HF solution predominantly occurs. The native oxide growth on Si surfaces with different fluorine coverages has been measured at 25°C in an $N_2:O_2$=4:1 gas ambient with a flow rate of 1 liter/min and an H_2O concentration of 0.2 ~ 0.5 ppm. As clearly shown in Fig. 2, the onset time of oxide growth is strongly dependent upon the surface fluorine coverage. The existence of a critical amount of Si-F bonds (~ 12%) on Si dramatically suppresses the oxidation, and the decrease in F coverage enhances the initial oxidation rate. The fluorine coverage remains unchanged regardless of the N_2+O_2 gas exposure time. Even at an H_2O concentration of 10 ~ 13 ppm in N_2+O_2 gas flow no oxidation occurs for the wafer without water rinse after HF cleaning. In clean room air with an H_2O content of 1.1% at 25°C the native oxide growth does not proceed for a few tens minutes when the fluorine coverage is about 12%. From these results it is likely that Si-F bonds remain at chemically reactive sites such as atomic steps or surface defects. Since fluorine has the highest electronegativity, the valence electron transfer from the neighboring Si and hydrogen atoms to fluorine takes place. Such polar nature induced in the covalent bonds might stabilize Si-Si and Si-H bonds at chemically reactive sites.

Layer-by-layer oxidation

The native oxide layer thickness measured as a function of storage time in pure water is shown in Fig. 3. It is interesting to

note that the oxidation curve exhibits plateaus where the oxide thickness apparently saturates at about 2, 4, 6 and 8 Å regardless of doped impurities. These saturated oxide thicknesses coincide well with a structural model of the SiO_2/Si(100) interface proposed by Herman et al (5). This implies that the layer-by-layer oxidation occurs on a hydrogen-terminated Si surface and that the oxidation reaction proceeds parallel to the surface. This idea is quite consistent with the fact that the oxidation of the hydrogen-terminated Si surface occurs from the backbond of surface Si-H bond (6). From these results it is likely that the oxidation is initiated at chemically reactive sites such as step edges and propagates along the surface as schematically shown in Fig. 4. The oxide thickness saturation observed in Fig. 3 could be explained by the transition time from the state (a) to (b) in Fig. 4 because the oxidation of the second monolayer needs the incubation time for oxygen penetration from the step edges A and B to the sites E and F. This kind of layer-by-layer oxidation is also observed for HF treated Si stored in clean room air (4).

In Fig. 3 the oxidation rate of n^+ Si is significantly faster than that of p^+, while those of n and p-type Si are in between. The Si oxidation rate is known to be enhanced by forming O_2^- ions through free electron transfer from Si to adsorbed O_2 molecules. If it is assumed that the empty electron state of adsorbed O_2 is located near the Fermi level of p-type Si substrate (Ev + 0.2 eV), the electron transfer from Si easily occurs for n^+, n and p-type Si in this order. The formation of O_2^- ions also induces the surface electric field which enhances the oxidation rate. Calculated Debye length for a donor concentration of 5.0×10^{18} cm^{-3} is 18 Å which provides the surface electric field as high as ~ 10^5 V/cm for the band bending of a few kT. This value is enough to significantly enhance the oxidation rate for n^+ Si (7).

Crystallographic orientation effect

The oxidation of Si(111) surfaces is slower than Si(100) and the plateaus appear at thicknesses of about 1, 2 and 3.5 Å. The oxidation rate is highest for n^+ and lowest for p^+ and in between for n as in the case of Si(100). The influence of crystallographic orientation on the oxidation rate is shown for n^+ Si in Fig. 5. The oxidation kinetics of hydrogen terminated surfaces could be understood by the topological aspect of the surface atom arrangement. Namely, the density of reactive sites of HF-treated Si surfaces might be different for different crystalline orientations. The other idea is the difference in the probability of oxygen penetration from the surface: An oxygen molecule with a size of 2.71 Å easily penetrates through the (100) surface because the 1 x 1 surface has an atom void size of 3.08 Å for (100). This implies that oxygen molecule can attack the back bonds of surface Si-H bonds without any steric hindrance by the top surface atoms. In contrast to this the surface atom void sizes of (110) and (111) are 2.74 Å and 2.08 Å, respectively, being equal to or smaller than the size of O_2 molecule. Hence, the penetration of molecular oxygen into the second silicon layer of (110) and (111) surfaces is not easy and the electron tunneling probability from Si to adsorbed O_2 is

lowered, leading to the reduced oxidation rate. The mechanism of the observed crystal orientation dependence of oxidation rate is not completely understood. Nevertheless, it is worth while to note that the oxidation kinetics depends upon the surface microstructure.

Surface roughness and chemical reactivity

Native oxide growth on hydrogen-terminated silicon surfaces is apparently influenced with the atomic scale topology such as steps and crystal orientations. This implies that the fluorine bond concentration and the oxide growth rate or the chemical reactivity are changed by changing the surface flatness. As far as the Si(111) surface is concerned, the surface morphology is significantly changed by pH values of BHF solutions as reported by a previous paper (3). Also, fluorine bond concentrations of BHF treated surfaces are altered by pH values of BHF (8). Therefore, the kinetics of native oxide growth must be influenced by pH modified BHF treatment.

Silicon surface morphology and oxidation kinetics

The fluorine coverage of 5% HF treated or pH modified BHF treated Si(111) surfaces are considerably different as shown in Fig. 6, implying different surface morphology. The fluorine coverage on a BHF cleaned silicon is about one third of the HF cleaning case. NH_4OH addition to the BHF solution causes the gradual decrease of the surface fluorine bonds whose minimum quantity appears at pH=5.3 for NH_4F:HF = 7:1, while in the case of NH_4F:HF = 4:1 the fluorine coverage is not very sensitive to NH_4OH content X below 2.0. Further increase of the NH_4OH concentration results in the increase of fluorine bonds originating from the surface products such as $(NH_4)_2SiF_6$. At NH_4OH fractions above X=2.5, such microcrystalline silicates precipitate on the surface and the N_{1s} XPS signal is observable at a binding energy of 398 eV and the F_{1s} signal exhibits a chemical sift from 686 eV to 688 eV. The variation of fluorine coverage in Fig. 6 might reflect the varying surface morphology which can be probed by measuring the hydrogen bonding configurations (1~3). In fact, the ATR spectra of Si(111) surfaces are dramatically changed by HF or BHF treatment as shown in Fig. 7. The spectrum of the BHF (pH=5.3) treated surface is dominated by a very sharp vibrational line at 2083.7 cm^{-1} which corresponds to the stretching mode of monohydride (Si-H) bond perpendicular to the surface as confirmed by the fact that the absorption intensity is dramatically reduced by S-polarized light. The absorption intensity at 2083.7 cm^{-1} is close to a value observed for Si-H bonds on an atomically flat surface (3). A shoulder at 2087 cm^{-1} arises also from the uncoupled vibration of monohydride bonds. A small peaks at 2098 and 2107 cm^{-1} are assigned to be $Si-H_2$ bond. The main peak (2083.7 cm^{-1}) intensity of BHF (pH=4.5) treated Si is smaller than the case of pH=5.3, showing a deteriorated flatness of the surface. For a 5% HF-treated surface the absorption intensity of Si-H is very small and its linewidth is broad. Also, rather intense dihydride modes appear at 2098 and 2107 cm^{-1}. This indicates that the HF treated

surface is significantly rough compared to the case of BHF (pH=5.3 and 4.5) treatment. Nevertheless, the native oxidation rate of 5% HF treated Si(111) is slower than that of a BHF (pH=4.5) treated surface as shown in Fig. 8 because the chemically reactive sites such as atomic steps or surface defects of HF treated Si is passivated with enough Si-F bonds (4), being different from the case of the BHF (pH=4.5) treated surface. In contrast to this, the BHF (pH=5.3) cleaned surface has no fluorine bond, showing an atomically flat morphology with very little reactive sites as demonstrated by the ATR spectrum in Fig. 7. Consequently, the surface is chemically enert and no oxidation reaction proceeds in clean room air for 300 min. It is shown that a rather rough, hydrogen-terminated surface with enough (~ 12%) fluorine bonds or a completely flat, hydrogen-terminated surface without fluorine bond is chemically stable against oxidation.

CONCLUSION

An atomically flat Si(111) surface terminated with hydrogen is produced by pH modified BHF treatment and it is extremely inert against oxidant. HF-treated Si(100) and (111) surfaces without water rinse are rather rough, but they are chemically stable when reactive sites such as atomic steps or surface defects are passivated with sufficient fluorine bonds. A rough surface with a low fluorine coverage is easily oxidized. It is also shown that the layer-by-layer oxidation proceeds on hydrogen-terminated Si surfaces.

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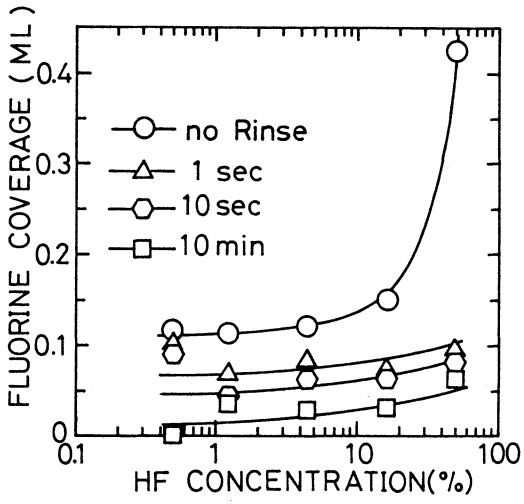

Fig. 1 Fluorine coverage as a function of HF concentration for different pure water rinse times.

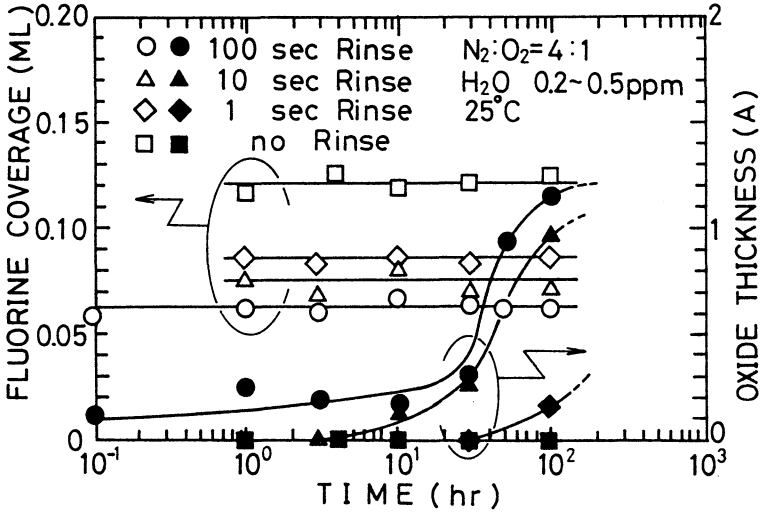

Fig. 2 Fluorine coverage and oxide thickness versus dry O_2+N_2 exposure time for wafers with different fluorine coverages.

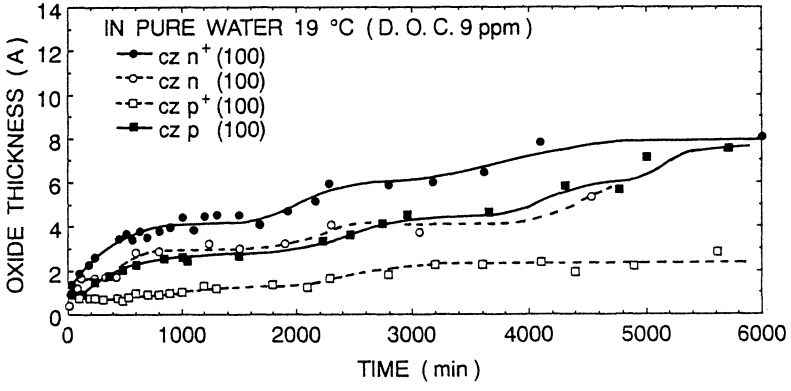

Fig. 3 Native oxide growth on Si(100) after 4.5% HF treatment as a function of oxidation time in pure water.

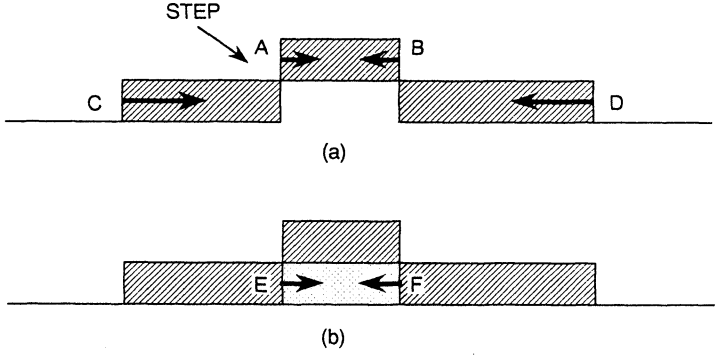

Fig. 4 The lateral oxidation of the first monolayer is thought to occur from the step edges A, B, C and D (a). A significant reduction of the lateral oxidation rate occurs at the beginning of the second monolayer oxidation (b). A plateau in an oxidation curve appears when the oxidation proceeds from the first monolayer to the second monolayer edges E and F.

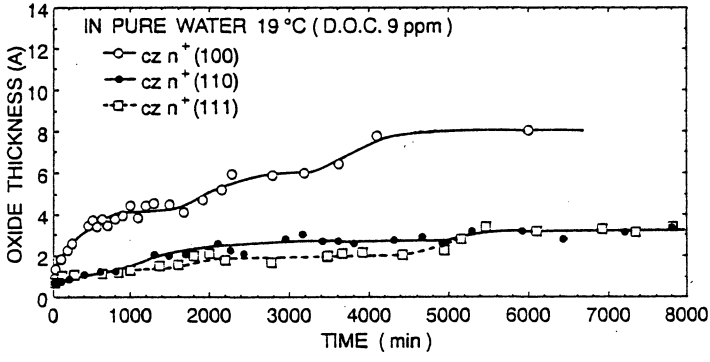

Fig. 5 Native oxide growth on n^+-Si wafers with different crystalline orientations after 4.5% HF treatment as a function of stored time in pure water.

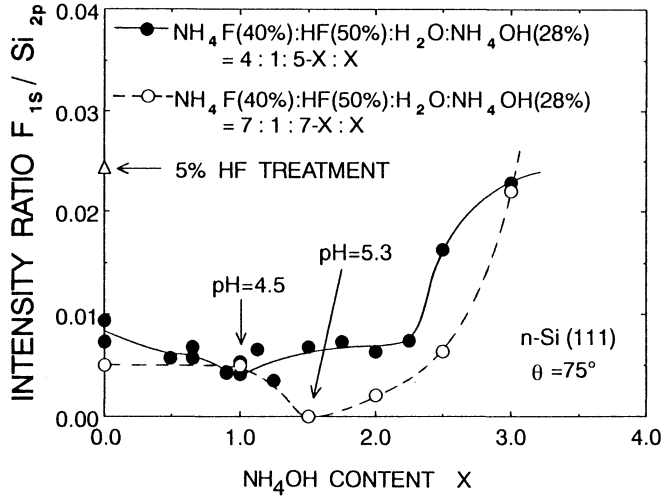

Fig. 6 Integrated intensity ratio of F_{1s} to Si_{2p} for n-Si(111) surfaces prepared by BHF solutions as a function of NH_4OH content X.

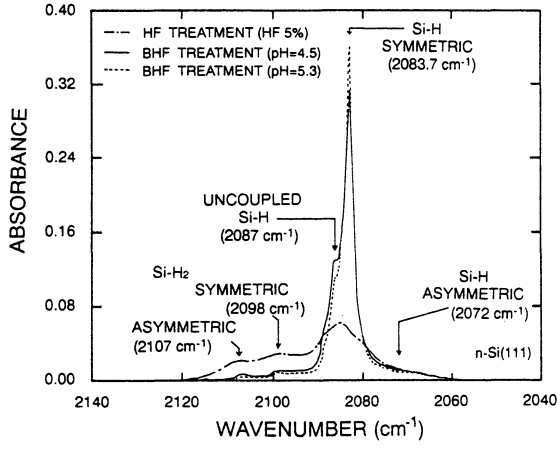

Fig. 7 Internal reflection spectra of HF-treated or BHF (pH=4.5, 5.3) treated Si(111) surface.

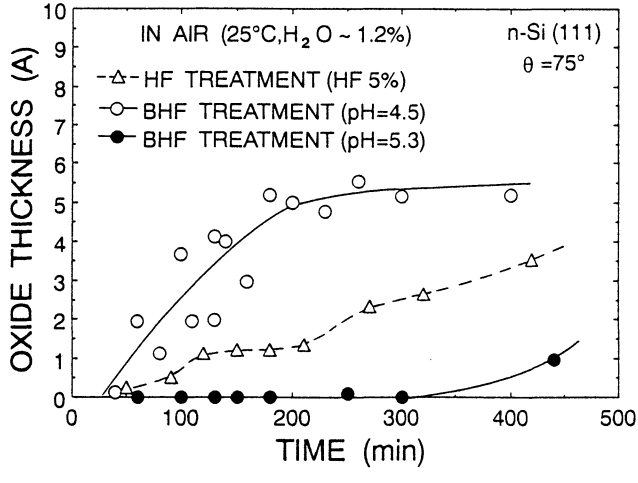

Fig. 8 Native oxide growth on n-Si(111) after 5% HF or BHF (pH=4.5 and 5.3) cleaning in clean room air with 1.2% H_2O at 25°C.

THE BENEFITS OF SC-1/SC-2 MEGASONIC WAFER CLEANING

W. A. Syverson, M. J. Fleming, P. J. Schubring
IBM General Technology Division
Essex Junction, Vermont 05452

ABSTRACT

Chemical-spray wafer processes are limited in their ability to remove very small foreign material (FM) particles from wafer surfaces because classical fluid boundary-layer phenomena act to inhibit particulate removal. However, by using megasonics wafer-cleaning technology in conjunction with the SC-1/2 chemistries, we have significantly improved device defect densities. This paper summarizes several experimental findings using the megasonics wafer-cleaning technology.

INTRODUCTION

Spray-wafer processing is commonly thought to remove particles while preparing a wafer surface for the subsequent process step. However, experiments have shown that, although spray tools are good for chemical processing, they do not effectively remove very small particulate-based contaminants. Due to classic fluid-dynamic boundary-layer phenomena, wafer-surface particulate contamination is actually trapped at the wafer surface despite high-velocity chemical sprays and DI-water rinsing.

Megasonic wafer-cleaning technology greatly reduces traditional fluid-dynamic wafer cleaning limitations and focuses attention to where it belongs: at the wafer's surface. Utilizing the incompressibility and excellent energy transmissibility of liquids and the gas-evolving properties of the SC-1/SC-2 solutions, major reductions in wafer particulate defect densities have been achieved at IBM's advanced semiconductor manufacturing facility in Essex Junction, Vermont.

This paper describes the configuration of hardware and the techniques used for our wafer-cleaning evaluations, and summarizes our experimental findings from using megasonics technology with the SC-1/SC-2 chemistries.

MEGASONICS TOOL CONFIGURATION

The 125-mm megasonic design used at IBM's Vermont facility is customized to the existing tank configuration. The design incorporates dual bottom-mounted direct-coupled tantalum-covered megasonic transducers (Figure 1). The transducers operate in the frequency range of 750 kHz to 980 kHz and up to 150 watts per transducer. Wafers in 25-slot cassettes are immersed in either the SC-1 (5:1:1, H2O:H2O2:NH4OH) or the SC-2 (5:1:1, H2O:H2O2:HCL) wafer-cleaning solutions and are cycled over the transducers using an external chain-drive mechanism. Standard DI-water rinses and centrifuge wafer drying are employed. Tool software is programmable for any level of power or tank temperature desired, as well as the speed and number of cycles that the wafers make over the transducer.

APPROACH

Typically, wafer surfaces are very highly chemophilic when immersed in a wet chemical solution. The solution does not quickly drain from the wafer surface; it clings to the surface when the wafers are removed from direct contact with the solution. This clinging phenomena may also act to trap contaminants present in the solution. Figure 2 is a schematic diagram of insoluble contaminants in a wet chemical solution. As the solution is rinsed from the wafer's surface, the insoluble contaminants can be driven toward the wafer surface until they adhere to it. When the contaminants become resident on the surface, they can be very difficult to remove.

Much of the experimental data in this paper includes using the conformal deposition characteristics of the LPCVD polysilicon deposition process as an analytical technique. With this technique, wafer-surface particulates can be magnified to the point where they can be detected by using traditional foreign-material (FM) inspection methods. We have found that this technique is quite reliable in identifying particulates that are substantially below the typical detection limits of most FM inspection tools.

EXPERIMENTS AND RESULTS

Temperature Optimization

Using the SC-1 and SC-2 wafer-cleaning chemistries in tandem, experiments were conducted to find the optimal temperature for operation of the megasonic units. It was determined that FM levels were generally reduced as tank temperatures were increased. However, post-processing the wafers with LPCVD polysilicon deposition identified that, for very small FM, 55 °C was the optimal process temperature for SC-1 and SC-2 megasonic wafer cleaning. This was confirmed with the results of the MOS-tested wafers which were processed simultaneously (Table 1).

Process Window Optimization

Experiments were conducted to determine the best power/cycle conditions for FM removal. Using the software flexibility afforded by the tool, the experimental conditions were set as indicated below. Tank temperature for the SC-1 and SC-2 solutions was 55 °C. Each cell reported was the mean of data from three bare silicon wafers. The TENCOR Surfscan threshold setting was the minimum detectable particle diameter.

The data in Table 2 indicates that maximum particle-removal efficiencies occur under conditions of maximum power, maximum number of passes over the megasonic transducers, and slowest wafer movement. When the wafers were subsequently processed through LPCVD polysilicon deposition, the FM differences became even more obvious. The data in Table 3 reaffirms the theory that current spray-process cleaning does not remove very small FM nearly as efficiently as the equivalent megasonic SC-1/SC-2 tank process. This data has been repeatedly verified in a multitude of similar experiments.

Megasonic SC-1/SC-2 Wafer Cleaning Efficiencies

Based upon the optimal temperature and process-window conditions found, an experiment was conducted to demonstrate the cleaning efficiencies of megasonics under worst-case conditions. Oxide wafers were either stripped or etched in a 5% buffered hydrofluoric acid solution. Other oxide and silicon/oxide/nitride wafers were immersed for 20 minutes in a hot phosphoric acid solution. These wafers were then processed through either the SC-1 or SC-2 wafer-cleaning solutions. Half the wafers were processed with the megasonic energy "on"; the other wafers were processed in the same tank, but with the megasonic energy "off". The particle-removal efficiencies were then calculated and compared (Table 4). In every case, wafers processed with the megasonic energy "on" were significantly cleaner than identical wafers processed through the same tank with the megasonic energy "off", confirming that megasonic transducer energy plays an important role in the removal of process-induced particles from wafer surfaces.

CONCLUSION

The use of megasonic technology with the SC-1 and SC-2 wafer-cleaning chemistries is absolutely essential for today's semiconductor manufacturing process. Megasonic cleaning vastly reduces device defect densities and may be key to advancing the next generation of semiconductors.

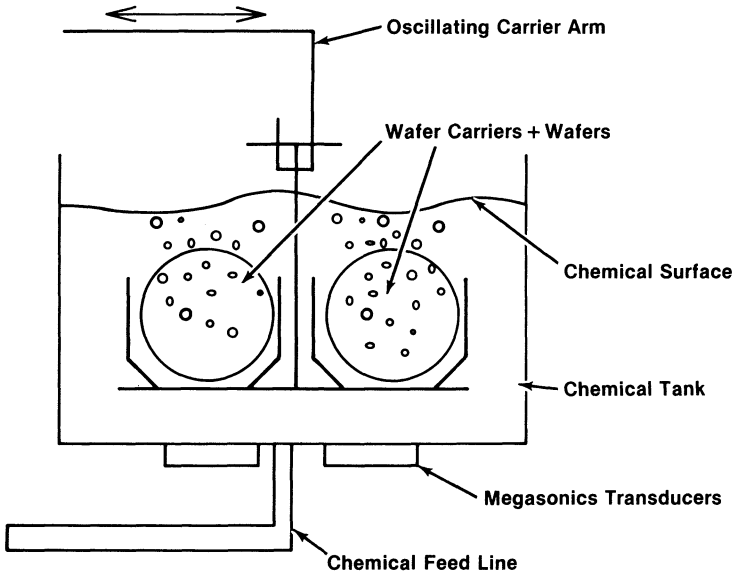

Figure 1. Megasonic tank configuration (side view).

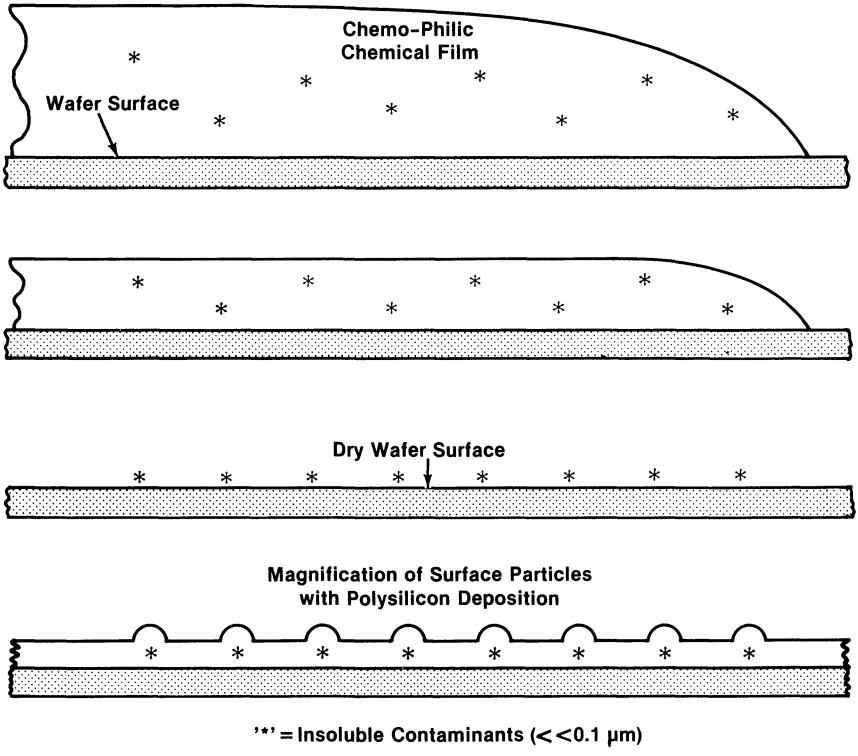

Figure 2. Insoluble contaminants in a wet chemical solution.

Table 1. Megasonics temperature optimization.

		Numbers of Particles Counted Using TENCOR* FM (@ 0.24 μm)			Number of Particles Counted Using LPCVD Poly (430 nm)		% Passing MOS Test Double-Ramp Breakdown	
Temp	Wafer #	Pre	Post	Delta	0.9 μm	0.6 μm	1st Ramp	2nd Ramp
25°C	1	251	58	-193	33	64	100.0	94.8
	2	122	209	87	23	51	*	*
	3	69	14	-55	9	28	*	*
	4	61	47	-14	16	17		
	5	40	34	-6	22	56		
Average		109	72	-36	20	43	100.0	94.8
40°C	1	308	38	-270	21	45	96.6	91.4
	2	99	5	-94	5	9	100.0	94.8
	3	90	11	-79	8	23	89.7	89.7
	4	83	57	-26	9	16		
	5	57	42	-15	23	39		
Average		127	31	- 97	13	26	95.4	91.9
55°C	1	221	18	-203	23	40	100.0	100.0
	2	197	47	-150	9	17	100.0	94.8
	3	104	38	-66	8	18	89.7	89.7
	4	67	2	-65	1	2		
	5	40	22	-18				
Average		126	25	-100	10	19	96.6	94.8
70°C	1	321	5	-316	12	21	98.3	86.2
	2	129	21	-108	16	23	100.0	93.0
	3	98	17	-81	20	30	98.3	87.9
	4	90	5	-85	10	20		
Average		160	12	-148	14	23	98.9	89.0
Control (No Processing)							96.6	89.7
							98.3	91.4
Average							97.5	90.5

Table 2. Megasonics SC-1/SC-2 process window.

TENCOR* FM Data @ 0.24 μm						
	6 Passes 10 min		2 Passes 5 min		6 Passes 5 min	
Power Level	FM Post-Count	Percent Removal	FM Post-Count	Percent Removal	FM Post-Count	Percent Removal
140	20	88%	21	80%	61	79%
125	24	82%	60	66%	39	87%
100	34	76%	88	51%	51	76%
75	90	61%	84	67%	53	71%
50	60	32%	96	55%	69	67%
Spray Clean	78	67%	—	—	—	—

Table 3. Post polysilicon deposition (0.43 μm).

TENCOR* FM Data @ 0.6 μm			
Power Level	6 Passes 10 min FM Count	2 Passes 5 min FM Count	6 Passes 5 min FM Count
140	30	92	312
125	88	252	401
100	114	363	298
75	325	240	211
50	197	375	310
Spray Clean	665	—	—

Table 4. Megasonics SC-1/SC-2 cleaning efficiency.

	Particle Removal Efficiencies	
Experimental Cell	SC-1	SC-2
BHF Strip		
Megasonics	86%	88%
No Megasonics	10%	(82% add)
BHF Etch		
Megasonics	50%	(19% add)
No Megasonics	11%	(240% add)
H_3PO_4 Oxide		
Megasonics	85%	76%
No Megasonics	46%	2%
H_3PO_4 Nitride		
Megasonics	90%	94%
No Megasonics	56%	24%

AQUEOUS OZONE CLEANING OF SILICON WAFERS

Jeremy K. Tong and Donald C. Grant
FSI International
322 Lake Hazeltine Drive
Chaska, Minnesota 55318-1096

Charlie A. Peterson
EMPAK
1501 Park Road
Chanhassen, Minnesota 55317

ABSTRACT

Control of particle and metal contamination on wafer surfaces during the manufacturing of high density semiconductor devices has become increasingly important in recent years. Although traditional RCA and modified RCA cleans are still popular, many believe that more advanced methods using new chemistries and cleaner chemicals are needed for coming generations of microchips. This paper describes a new cleaning technique developed which uses ozonated water as one of the cleaning chemicals. The cleaning sequence includes three steps: **S**ulfuric Acid **O**zonated water **M**ix (SOM)/**D**iluted **H**ydrofluoric Acid (DHF)/ozonated water. Cleaning performance is described in terms of residual metals and particles on wafer surfaces. Performance was found to be equal to or better than a popular modified RCA clean consisting of a **S**ulfuric Acid Hydrogen **P**eroxide **M**ix (SPM)/**D**iluted **H**ydrofluoric Acid (DHF)/Ammonium Hydroxide Hydrogen **P**eroxide **M**ix (APM)/**H**ydrochloric Acid Hydrogen **P**eroxide **M**ix (HPM) chemical dispense sequence.

INTRODUCTION

Contamination control on silicon wafers during the manufacturing of state-of-the-art semiconductor devices has become increasingly critical. It is well known that there are four major types of contaminants on wafers: organics, metallics, contaminated oxide and particles[1]. These contaminates are historically removed by wet RCA cleans and modified RCA cleans. Although RCA and modified RCA cleans have been used for over 20 years and are still popular, many in the industry are starting to realize their limitations. More advanced cleaning methods using new cleaning chemistries and cleaner chemicals are needed as device line width further shrinks to 0.5μm and lower.

One popular version of the RCA clean contains four major chemical steps performed in the following sequence:

SPM (**S**ulfuric Acid/Hydrogen **P**eroxide Mix)
DHF (**D**iluted **H**ydrofluoric Acid)
APM (**A**mmonium Hydroxide/Hydrogen **P**eroxide **M**ix)
HPM (**H**ydrochloric Acid/Hydrogen **P**eroxide **M**ix).

The basic functions of these chemical steps are as follows: SPM is used in the first step to remove organic contamination originating from transportation in wafer carriers, residual photoresist or organic adsorption from the atmosphere. If not removed, these organics can shield the removal of other contaminants in subsequent cleaning steps. DHF is used to remove the thin layer of contaminated native oxide. APM is used to oxidize light organics, remove particles and grow a thin layer of clean oxide to protect the contamination-prone bare silicon. HPM is used to first oxidize then complex metallics on wafer surfaces. These are subsequently removed by rinsing with DI water.

One major drawback for repeatedly using H_2O_2 as the oxidant in this type of cleaning sequence is metal contamination by H_2O_2 itself. Because H_2O_2 is chemically unstable, it has historically been manufactured and stored in Aluminum container and metal stabilizers were often used for safety reasons. Although higher purity unstabilized H_2O_2 is available today, it's very expensive and may become contaminated during transportation.

The contamination issue of H_2O_2 suggests using other oxidants with similar oxidation potentials. Table I list several chemicals that have high oxidation potentials[2]. Ozone, with an oxidation potentials of 2.07 electron volts in the gas phase and 1.24 when dissolved in water, becomes an obvious choice. In order to be able to achieve better mixing results with other chemicals such as H_2SO_4 and HCl, ozonated water was used instead of ozone gas in the new ozone clean discussed in this paper.

The wet cleaning method developed uses water with high concentrations of ozone as one of the cleaning chemicals. Cleaning is achieved using only H_2SO_4, DHF and ozonated water in three chemical steps:

- SOM (Sulfuric Acid/Ozonated water Mix)
- DHF
- Ozonated water

The basic functions of these three chemical steps are as follows: SOM is used to remove organic contamination, more or less the same function as the SPM step in the modified RCA clean. DHF is used to remove the thin layer of contaminated oxide. Ozonated water is used as last step to oxidize and rinse away light organics, metallics and

particles and at the same time grow a thin layer of clean oxide to protect the bare silicon. This clean eliminates three of the chemicals that are used the modified RCA clean described earlier: H_2O_2, NH_4OH and HCl.

OZONE CHEMISTRY

Ozone has been historically used as an oxidant in waste treatment and drinking water sterilization since the turn of the century. In recent years, ozone has been slowly introduced into microelectronics industry for use as a strong oxidant.

Ozone has basically the same role in the ozone clean as H_2O_2 in the modified RCA clean — oxidation. Ozone and H_2O_2 decompose virtually the same way:

$$H_2O_2 \longrightarrow O^- + H_2O$$

$$O_3 \longrightarrow O^- + O_2$$

In what state the O^- exists is questionable. The stronger oxidizing effect (thus cleaning mechanism) of ozonated water is probably due to the O^-, the product of the rapid decomposition of ozone. The decomposition mechanism of ozone is not clearly understood. In aqueous ozone solution, decomposition products could be O_2, HO^-, O^-, O_2^- and/or other radical groups.

Ozone leaves no harmful residual when it decomposes. It is sparingly soluble in water, especially at lower water temperatures. Table II lists the solubility of ozone in water at different water temperatures[3]. Generally ozone is about 10 times more soluble in water than oxygen. The lower the water temperature, the higher the ozone solubility.

In practice, the concentration of dissolved ozone never reaches the theoretical value because of:

- poor mass transfer
- organic matters in water which react with ozone and catalyze and accelerate its decomposition ozone decomposition
- salts in water which reduces ozone solubility
- ozone has a relatively short half-life

The half-life of ozone in high purity DI water is about 20 minutes.

EXPERIMENTAL

Experiments to compare the effectiveness of the modified RCA clean and the ozone clean were performed in centrifugal spray processors (FSI International TITAN® and MERCURY® Multi Position Acid Processors). A schematic of a spray processor process chamber is shown in Figure 1. In a centrifugal spray acid processor, pressurized chemicals are atomized with nitrogen gas and sprayed onto silicon wafers held in a rotating turntable inside a closed chamber. Hot and cold ultra pure DI water are used to rinse the wafers. Nitrogen gas is used to purge and dry the chamber.

Because ozone is inherently unstable, high purity ozonated water was generated near the point of use (POU). By continuously feeding high concentration (about 60,000 ppm v/v), well filtered ozone gas into a closed Teflon contact chamber filled with high purity cold DI water, concentrations of ozonated water in the 10-15 ppm were consistently obtained. Figure 2 shows the schematics of the POU ozonated water generator. This chamber was then pressurized with high purity nitrogen gas to deliver the ozonated water to a centrifugal spray acid processor.

The cleans compared used the following chemical expose times:

Modified RCA clean	Ozone clean
SPM 60 seconds	SOM 60 seconds
DHF (0.5%) 90 seconds	DHF (0.5%) 90 seconds
APM 90 seconds	O_3-H_2O 210 seconds
HPM 90 seconds	

The cleans were compared by examining residual metals and change in particle concentrations (post-clean minus pre-clean) as a result of the cleans. In addition, The thickness of the resulting chemical oxide on the wafer surface and the surface contact angle with DI water (Figure 3) were measured.

The metal removal effectiveness of the cleans was compared using wafers which had been contaminated and ones which were previously cleaned using a modified RCA clean. The contaminated wafers were prepared by dipping the wafers in DI water : city water (5:1) mixture for three minutes.

The particle removal effectiveness of the cleans was compared by ten runs of three wafers each . Particle levels were measured before and after the clean and the difference was calculated.

Residual metals following the cleans were measured using both Secondary Ion Mass Spectroscopy (SIMS) and Total Reflection X-Ray Fluorescence (TRXRF)[4]. SIMS was used to analyze for low molecular weight contaminants such as sodium while TRXRF was used to analyze for transition metals like Iron and Manganese. Particles were measured using an Estek 8500 wafer surface inspection system. Oxide thickness was measured using a Gaertner L116ALC Ellipsometer. The surface contact angle with water was measured using a Goniometer.

RESULTS AND DISCUSSIONS

Typical residual metal levels on wafer surfaces following the two cleans are compared in Tables III and IV. Table III presents SIMS analysis and Table IV presents TRXRF analysis. The SIMS results are shown as relative elemental abundance (REA) defined as:

$$REA = \frac{\text{Element signal peak height}}{\text{Silicon signal peak height}} \times 10^6$$

The TRXRF results are in the unit of 10^{12} atoms/cm^2.

The SIMS data show that the ozone clean leaves lower levels of residual Na, K, Mg, Al and Ca, virtually the same levels of Cu (lower than detection limit) but slightly higher levels of F. The slightly higher level of F may result because DHF is the last chemical the wafer sees before the final ozonated water dispense. The largest difference is seen for Br. It is believed that the higher level of Br seen with the modified RCA clean is a result of Br contamination in the HCl used in the HPM step. Elevated Br levels for cleans using HPM as last step have been reported previously[5]. The TRXRF data show that the ozone clean gives lower residual metal levels for virtually all of the transition metals.

The ozone clean is believed to produce a surface with lower metals than the modified RCA clean because the ozonated water grows a cleaner oxide than APM. It has been well documented that surfaces have very low metal content following exposure to dilute HF[6-8]. However, metals tend to adsorb onto the wafer surface from the basic APM solution and the HPM clean is used to remove these metals[9]. The ozone solution used to grow the oxide has a neutral PH and , because it is made with ultra high purity water, the metal content is very low. Hence metal precipitation does not occur.

The thickness of the oxide following the ozone clean was approximately 10 Angstroms. The wafers were completely hydrophilic when dipped in water with measured contact angles of 30-35 degree. The modified RCA cleaned wafers were also completely

hydrophilic and had contact angle of 5-10 degree. A hydrophobic wafer surface has a contact angle of 55 degree or higher.

Figure 4 shows the particle removal capability of the ozone clean for particles of >= 0.3μm. The figure indicated that the clean added a small number of particles to wafers which had very low starting particle levels and removed particles from those with higher starting levels. The crossover from adding particles to removing particles occurred at a starting particle level of approximately 35 particles/150mm wafer. Figure 5 shows the typical particle performance of the modified RCA clean in the same spray processor. The particle removal efficiency of the ozone clean is close to but not as good as the modified RCA clean. Particle performance is expected to significantly improve when the ozone clean process is further optimized.

CONCLUSIONS

A cleaning chemistry based on the use of high concentration ozonated water has been developed. The clean provides a hydrophilic wafer surface with residual metal levels lower than those resulting from a modified RCA clean. Residual particle levels are slightly higher than those resulting from a modified RCA clean. The only chemicals used in the clean are H_2SO_4 and HF. Hence the cost associated with purchasing and disposing of the NH_4OH, H_2O_2 and HCl used in the modified RCA clean are eliminated.

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Table I. Oxidation Potentials of Selected Oxidants(2)

Reaction			Potential
$F_{2(g)} + 2e$	<——>	$2F$	2.87 eV
$O_3 + 2H^+ + 2e$	<——>	$O_2 + H_2O$	2.07 eV
$H_2O_2 + 2H^+ + 2e$	<——>	$2H_2O$	1.78 eV
$Cl_{2(g)} + 2e$	<——>	$2Cl$	1.36 eV
$O_3 + H_2O + 2e$	<——>	$O_2 + 2OH$	1.24 eV

Table II. Solubility of Ozone in Pure Water(3)

Temperature (^oC)	0	10	20	30	40	50	60
Solubility (ppm)	39	29	21	7	4	1	0

Table III. Typical Residual Metal Levels of Ozone Clean and Modified RCA Clean (SIMS Analysis)

	Relative Elemental Abundance						
	F	Na	K	Cu	Mg	Al	Ca
Clean Starting Wafers							
Modified RCA Clean	140	225	65	<20	22	1575	113
Ozone clean	200	105	25	<20	10	1064	98
Contaminated Starting Wafers							
Modified RCA Clean	145	330	160	<20	N/A	N/A	N/A
Ozone Clean	250	125	30	<20	N/A	N/A	N/A

Table IV. Comparison of Residual Transitional Metal Levels of Ozone Clean and Modified RCA Clean (TRXRF Analysis)

Atoms/cm^2

	Mn	Fe	Zn	Br	Cr	Co	Cu
Clean Starting Wafers							
Modified RCA Clean	<0.4	0.3	0.2	1.4	<0.6	<0.4	<0.2
Ozone Clean	<0.4	<0.3	<0.2	<0.3	<0.6	<0.4	<0.2
Contaminated Starting Wafers							
Modified RCA Clean	<0.4	<0.3	<0.2	1.8	<0.6	<0.4	<0.2
Ozone Clean	0.5	<0.3	<0.2	<0.3	<0.6	<0.4	<0.2

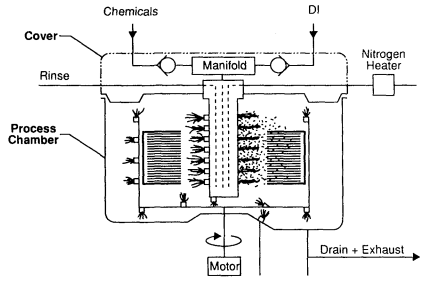

Figure 1: Schematics of a Centrifugal Spray Acid Processor

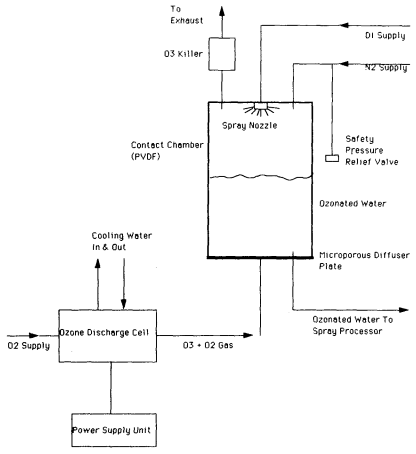

Figure 2. Schematics of Point-of-use (POU) Ozonated Water Generation System

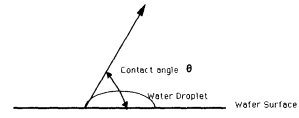

Figure 3. Technique for Measuring Surface Contact Angle with Water

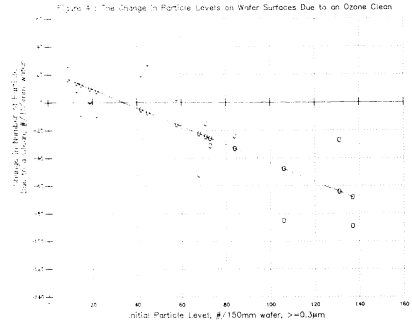

Figure 4 : The Change in Particle Levels on Wafer Surfaces Due to an Ozone Clean

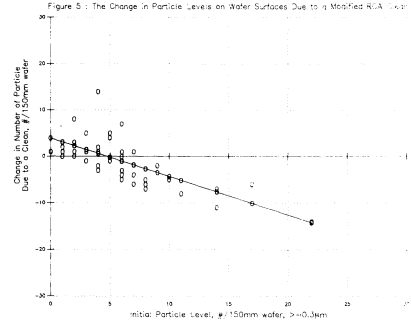

Figure 5 : The Change in Particle Levels on Wafer Surfaces Due to a Modified RCA Clean

WETTABILITY OF SILICON WAFERS IN CHOLINE SOLUTIONS

Jin-Goo Park and Srini Raghavan
Arizona Materials Laboratories and
Department of Materials Science and Engineering
University of Arizona
Tucson, AZ 85721

Wettability of silicon wafers in choline containing solutions has been investigated using the Wilhelmy plate technique. Key experimental variables studied were choline concentration, hydrogen peroxide addition, wafer type and orientation and immersion cycling. Choline improved the water wettability of wafers and at concentrations greater than 1000 ppm, rendered the wafers very hydrophilic. Air drying of wafers contacted with choline resulted in oxidation and improved wettability.

INTRODUCTION

Wet chemical cleaning of silicon wafers is widely practiced in the semiconductor industry. The commonly used RCA standard cleaning processes (1) are based on acidic or alkaline hydrogen peroxide solutions. Among the alternative cleaning chemicals that have been proposed for cleaning silicon wafers, choline (2-hydroxyethyl trimethyl ammonium hydroxide), a strong base (pK_b = 5.06) which is free from sodium, has generated much attention (2,3). Immersion of HF etched wafers in a choline solution followed by water rinsing has been claimed to result in very clean wafers (4).

Muraoka et al. (5) have developed several techniques to clean silicon wafers using choline. They have reported that dilute aqueous solutions of choline with selected nonionic surfactants can remove heavy metals from the silicon surface and prevent replating of these metals from solution. Harri and Hockett (6) studied the influence of different wet cleaning sequences on high temperature oxidation. Cleaning sequences involving choline showed fewer oxidation induced stacking faults (OISF), lowest levels of heavy metals, and oxides with good electrical properties.

The role of cleaning solutions in modifying the wettability of HF/BOE cleaned wafers has not been established. Such studies can be carried out using the contact angle technique. Contact angle measurement is a surface sensitive technique that has previously been shown to be able to characterize the surface of etched silicon wafers (7).

Menon and Donovan (8) related cleaning efficiencies to hydrophilic/hydrophobic nature of wafer surfaces after various wet cleaning steps. Glass beads, silicon dust and

PSL particles were deposited on both p and n type wafers having contact angles ranging 12 to 64°. For all three particle types and both wafer conductivity types, the low contact angle surfaces retained fewer particles after cleaning than the high contact angle surfaces.

During wafer cleaning, dynamic contact angle values are much more important than static angles especially since fill and dump cycles are commonly used during rinsing. Dynamic contact angles can be easily measured by the Wilhelmy plate technique (9). In this method, contact angle is deduced from a force measurement on a sample as a function of immersion depth in a liquid. There are usually two reproducible, stable contact angles: (1) an advancing contact angle, which is measured when a liquid solution is advanced over a previously unwetted surface; and (2) a receding contact angle observed when water recedes over a previously wet surface. The difference between the two angles is referred to as contact angle hysteresis.

Little published information exists on the fundamental aspects of wettability of silicon in choline containing solutions. This paper reports the results of a research undertaken to investigate the wettability of wafers in choline containing solutions using a dynamic contact angle analysis technique.

EXPERIMENTAL MATERIALS AND PROCEDURES

Materials

100 and 150 mm silicon wafers (10-100 Ω-cm resistivity), with and without thermally grown oxide coatings, were used in this research. Choline was purchased from Sigma Chemical Co. as a 50% solution. Aliquots of this solution were appropriately diluted with 18 MΩ-cm DI water to prepare choline solutions ranging in concentration from 6.5 to 10000 ppm (1 wt%). Electronic grade H_2SO_4 (98 %), H_2O_2 (30 %) reagents and 3:1 BOE (NH_4F:HF) were used in sample preparation.

Procedures

Wafers were cut with a diamond saw into 13 mm × 19 mm size samples in a class 100 cleanroom. Immediately after cutting, samples were spin-rinse cleaned with RO-DI water to remove silicon particles produced during cutting. Analysis of cut samples by SEM/EDXA and Auger techniques showed no contamination other than oxygen and carbon from the atmosphere during cutting. Samples were transferred to a class 10 cleanroom for further chemical cleaning. Piranha (8:2 H_2SO_4:H_2O_2) etch was performed for 10 minutes followed by a DI water rinse for 5 minutes. Wafers were then etched using 3:1 BOE (NH_4F:HF) for 30 sec and rinsed in DI water for 30 sec. The samples were then dried using dry nitrogen gas.

A Cahn DCA-312 Dynamic Contact Angle Analyzer was used in measuring the force on sample plates as they were immersed in and emersed from aqueous solutions at a speed of 64 μm/sec. All measurements of the contact angle and surface tension were made in a laminar flow hood with an atmosphere of class 100 quality. Contact angles were calculated using the following equation:

$$F = \gamma_{LV} P \cos \theta / k \quad (1)$$

In the above equation, F is the force on the sample plate (corrected for sample weight) at zero immersion depth as determined by the balance (dynes), γ_{LV} is the surface tension of the liquid/vapor interface (dynes/cm), θ is the contact angle, and k (= 0.981) is a conversion factor from "mg" to "dynes." Figure 1 shows a typical Wilhelmy plate hysteresis loop for bare p(100) silicon wafer sample in DI water. The sample was taken through two successive cycles.

Solution pH and oxidation and reduction potentials (ORP) were measured using a Cole-Parmer epoxy body combination Ag/AgCl electrode and an Orion platinum redox electrode.

RESULTS AND DISCUSSION

Characterization of Choline

The pH, redox potentials (reported on a standard hydrogen electrode scale) and surface tension of choline containing solutions were measured as a function of concentration; the results are shown in Figure 2. A rapid change in pH from 5.6 to 9.3 was observed when the concentration of choline was raised from 0 (DI water) to 6.3 ppm. For choline concentrations in excess of 6.3 ppm, the change of pH was less rapid. The solution redox potential decreased with increasing choline concentration.

It can be inferred from the surface tension data that choline is not surface active at the air-solution interface until a solution concentration of 400 ppm. Above 400 ppm, the surface tension started to decrease and reached 47.6 dynes/cm at 10000 ppm (1 wt%).

Wettability of BOE Etched p(100) Wafers

Most of the wafers used in measuring contact angles were single side polished (SSP) wafers. Some measurements were done on double side polished (DSP) p(100) wafers to determine the dependence of contact angles on surface finish. Multiple immersion/emersion cycles were performed to observe the change in advancing and receding angles on Si wafers in choline solutions. However it was found that contact angle values did not change significantly after the second cycle.

Figure 3(a) shows advancing (θ_A) and receding (θ_R) contact angles on bare p(100) wafers (single and double side polished) during the first immersion/emersion cycle as a function of choline concentration. Double side polishing did not alter advancing (θ_A) and receding (θ_R) contact angles significantly. Advancing angles remained almost constant until a choline concentration of 400 ppm and then began to decrease. This may be related to the onset of surface activity of choline at this choline concentration as mentioned previously. The receding angles decreased gradually and were around 20° at choline concentrations in excess of 5000 ppm.

The second-cycle behavior of wafers in choline solutions is shown in Figure 3(b). On both SSP and DSP wafers, θ_A decreased significantly with increasing choline concentrations above 200 ppm. A comparison of Figure 3(b) to 3(a) would clearly reveal that the second cycle immersion θ_A values are almost identical to θ_R values at high choline concentrations. A DI water rinse after the choline treatment did not return the wafers to the original hydrophobic states.

In order to probe the interaction of choline with the silicon surface, samples exposed to choline solution were analyzed by X-ray photoelectron spectroscopy (XPS). Two types of samples were used: (1) a sample immersed in choline (1 wt%) for 10 minutes, then rinsed and dried, and (2) a sample subjected to a two cycling test in choline. In sample 2, the area exposed to both solution and air during cycling was analyzed. The analysis showed the presence of Si(2p) peaks corresponding to SiO_2 only on the sample subjected to two cycle immersion test. It is pertinent to point out that in two cycle tests the sequence of exposure is as follows solution-air-solution-air. It appears that exposure of choline contacted silicon to air resulted in oxide formation and hence lower contact angles. Thus if a quick dump rinser with multiple cycles is used for choline rinsing, the wafer wettability can be highly improved.

Wettability of p(100) with Thermally Grown Oxide

The wetting of oxide-coated p-type Si of (100) orientation was next investigated. Figure 4(a) shows advancing and receding angles of choline solutions on oxide-coated (570 Å) p(100) wafers. Advancing angles in the first cycle decreased as choline concentration increased. Zero advancing angles (complete wetting) were measured in the second cycle above 100 ppm choline. Receding angles decreased slowly until 200 ppm and increased to 20° at 10000 ppm. The cycling did not affect the receding angles at all over the entire choline concentration. Figure 4(b) shows the contact angles in DI water of samples subjected to a two cycle immersion in choline followed by a DI water rinse for 5 min. Zero advancing and receding angles were measured for samples cycled in choline solutions of concentrations 5000 ppm or higher.

Effects of Wafer Orientations and Types on Wettability

The effects of choline on the wettability of p(100), n(100) and n(111) wafers are shown in figures 5 and 6. Figure 5 shows advancing and receding angles on BOE etched p(100) and n(100) wafers as a function of concentration of choline. Almost identical behavior was observed on both types of wafers. This reveals that dopants do not affect the wettability of wafers of same crystal orientation.

Contact angles on n-type wafers of (100) and (111) orientation are presented in Figure 6(a) and (b). The surface energy of (111) and (100) planes of silicon has been reported to be 1230 dynes/cm and 2130 dynes/cm, respectively (10). Higher solid surface energy (γ_{SV}) should ideally lead to better wetting. The measurements of both advancing and receding angles on BOE etched silicon wafers, however, showed no effects of crystal orientation on wettability. This might be due to the passivation of silicon surface by species like hydrogen (7,11,12). A low value of critical surface tension of wetting of 27 dynes/cm has been reported for such a surface. Even though freshly formed (100) surface has a higher surface energy than (111) surface, the wetting behavior of silicon surfaces appears to be dominated not by solid-vapor interfacial energies but by passivated surfaces which have a lower surface tension than etching solutions.

Effect of Hydrogen Peroxide on Wettability in Choline Solutions

As mentioned in the background section, choline/peroxide solutions have shown promise as cleaning agents for silicon wafers. Addition of H_2O_2 to choline solutions increased redox potentials but decreased the pH. The effect of H_2O_2 addition to choline solutions on wafer wettability is shown in Figure 7(a) and (b). In 400 ppm choline solution, H_2O_2 significantly lowered advancing angles in the second cycle. Receding angles remained the same in both the first and second cycles in the entire hydrogen peroxide concentration investigated. At a choline concentration of 5000 ppm, the second cycle advancing and receding angles were low and identical. The decrease of advancing angles in the second cycle in both 400 and 5000 ppm choline solutions indicates that hydrogen peroxide helps to increase the wettability of silicon.

SUMMARY AND CONCLUSIONS

The Wilhelmy plate technique was used in measuring both advancing and receding contact angles of choline solutions on bare and oxide coated silicon wafers. Single and double side polished p(100) bare wafers showed the same advancing (θ_A) and receding (θ_R) angles in the first cycle in choline. Single side polished wafers showed a reversal of angles ($\theta_A < \theta_R$) in the second cycle, but this was not observed on the double side polished wafers.

On oxide coated p(100) wafers, advancing angles decreased in the first cycle as choline concentration increased and complete wetting was observed above 100 ppm of choline in the second cycle.

Types and orientations of silicon wafers did not affect the wettability of silicon surface after buffered HF etching. This might be due to the passivation of silicon surface by hydrogen.

Hydrogen peroxide was effective in increasing the wettability even at lower choline concentration.

ACKNOWLEDGMENTS

The authors wish to thank the Center for Microcontamination Control at the University of Arizona for the financial support. Special thanks are extended to Mr. C. Schneider and J. Beauchamp of Intel Corporation, and Mr. J. Crozier of National Semiconductor Corporation for their help with wafer samples.

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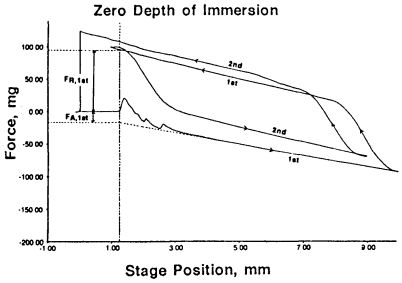

Figure 1. A typical Wilhelmy plate hysteresis loop for a bare p(100) silicon wafer sample in DI water.

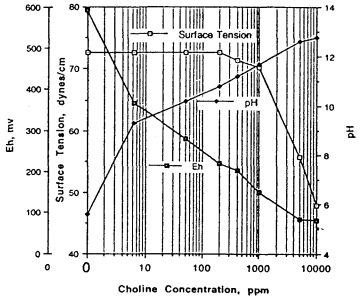

Figure 2. Surface tension, pH and redox potential (mv, vs. SHE) of choline solutions.

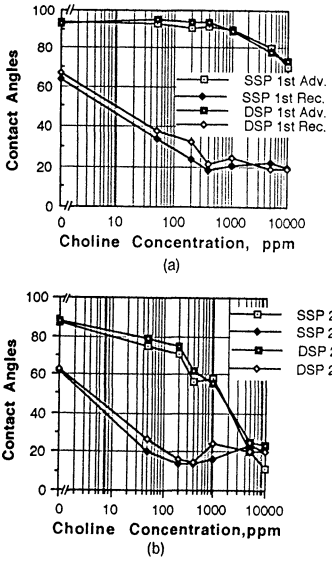

Figure 3. Advancing (θ_A) and receding (θ_R) angles on p(100) bare wafers in choline solutions, (a) first cycle and (b) second cycle.

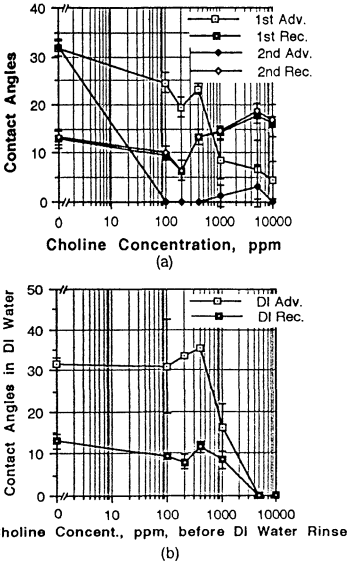

Figure 4. Advancing (θ_A) and receding (θ_R) angles on oxide coated p(100) wafers in (a) choline solutions and (b) in DI water after conditioning in choline followed by a DI water rinse for 5 min.

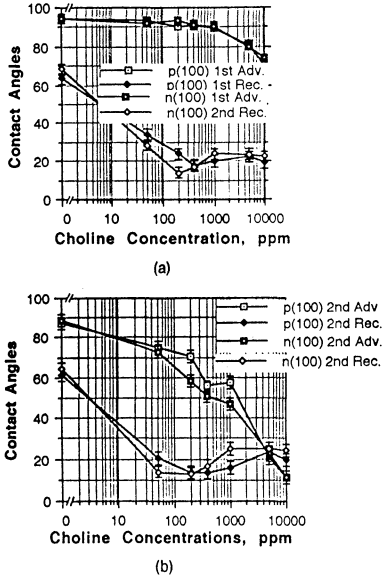

Figure 5. Wettability of BOE etched p(100) and n(100) wafers in choline solutions.

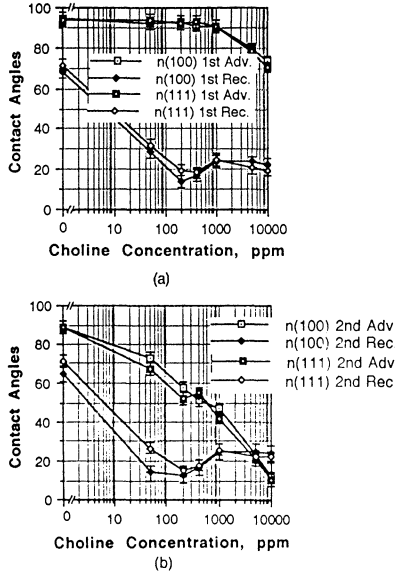

Figure 6. Effect of wafer orientation on wettability.

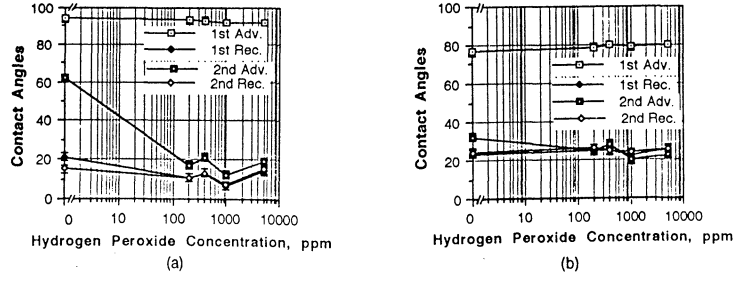

Figure 7. Advancing (θ_A) and receding (θ_R) angles on BOE etched DSP p(100) wafers as a function of hydrogen peroxide concentration; (a) choline content in solution 400 ppm and (b) 5000 ppm.

MEASUREMENT OF DI-WATER QUALITY

D. J. Siconolfi, R. P. Frankenthal, and J. D. Sinclair
AT&T Bell Laboratories
Murray Hill, NJ 07974

A system to measure the total amount of nonvolatile dissolved and fine particle (<0.06 μm in diameter) contamination in water at the part per billion level is described. Measurement is accomplished by counting the number and size distribution of particles generated by aerosolizing the water. This system has been used to measure contamination in four water systems. Solid particles (>0.06 μm in diameter) in the liquid phase were found to contribute negligibly to the abundance of particles formed by aerosol generation.

Introduction

As feature size moves well into the submicron region, even minute amounts of contamination in the environment, processing equipment, process chemicals, and process by-products can be detrimental to the yield and reliability of electronic devices.

High-purity water for reagent solutions and rinses is the most commonly used liquid for the manufacture of integrated circuits. Particles present in the liquid may deposit directly on these circuits, while soluble matter dissolved in the water may deposit as solid particles when aerosols generated from the water evaporate. The concentration and size distribution of particles >0.06 μm in diameter in the liquid phase can be measured by laser light scattering (1). Determination of the total amount of nonvolatile dissolved and fine particle (<0.06 μm in diameter) contamination in high-purity water may be accomplished by atomizing a small volume of the water to form an aerosol and measuring the concentration and size distribution of airborne particles after the aerosol has been dried (2-4).

As part of an ongoing effort to evaluate of the effect of particles on the corrosion and reliability of electronic materials and devices, a study was initiated to characterize the concentration and size distribution of salt particles generated by forming aerosols from an aqueous solution. An essential first step is to measure the concentration and size distribution of background particles generated from the water used to make the solutions. In this paper, we describe the method that was used to detect and characterize the aerosol particles. Four water supplies were evaluated. The detection limit for the total amount of nonvolatile dissolved and fine particle contamination was 1 part per billion (ppb).

Experimental

The water sources were two house DI water systems (DI-1 and DI-2), a dedicated Millipore Milli-Q Plus Water system (DI-3) in the authors' laboratory,[1] and a sample of water from an outside source that had been treated with O_3 to oxidize organics. This O_3 – treated water was introduced directly from its container into the atomizer. In the DI-3 system, tap water is first treated by reverse osmosis; then it is passed through activated charcoal to remove dissolved organics, through ion-exchange resins to polish out inorganic ions to 18 megohm-cm resistivity, and through a final organic scavenger. The DI-1 and DI-2 waters flowed through their extensive individual distribution systems, which are composed of tin and PVC tubing, respectively, to the point of use. The DI-3 water was obtained at its source. None of the DI-water systems was equipped with particle filtration. The concentration of particles >0.06 μm in these water ranged up to $10^5/cm^3$ for the DI-1 and DI-2 waters and was as low as $20/cm^3$ for the DI-3 water. The DI-1, -2, and -3 waters were passed through 12 feet of 1/4" plastic tubing, through a liquid particle sensor, and through an additional 5 feet of plastic tubing to the aerosol generator. Three different tubings were used. These were polyurethane (PU), PTFE Teflon (PTFE), and PFA Teflon (PFA). Additional particles were found in the waters from their flow through the tubing. The concentration of particles measured in the water increased in the order PTFE<PFA<PU.

The aerosol was produced with a TSI Model 3075 constant-output atomizer assembly. For this instrument, compressed nitrogen gas (N_2) that is dried over silica gel and passed through a Pall 0.01 μm filter is expanded through a small orifice to form a high velocity (ca. 3 l/min) jet. The water is supplied at a constant rate of 1 cm^3/hr by a syringe pump and is atomized by the N_2 jet. As the aerosol emerges from the atomizer nozzle, it is dried by a stream of N_2 (13.5 l/min) that is preheated to the desired temperature. Further drying, if necessary, is achieved by a TSI Model 3062 diffusion dryer. Any electrostatic charge on the particles is neutralized to near-Boltzmann charge equilibrium by positively and negatively charged nitrogen ions produced by means of a Kr-85 radioactive source in a TSI Model 3012 aerosol neutralizer.

Three types of monitors were used to measure the size distribution and concentration of the particles in the gas stream: (1) a TSI Model 3752 laser particle counter (LPC) that is stated by the manufacturer to measure the concentration of particles >0.2 μm and >0.5 μm in diameter; (2) a TSI Model 3760 condensation nucleus counter (CNC) that is stated by the manufacturer to measure the concentration of particles >0.014 μm in diameter; (3) a Particle Measuring Systems laser aerosol spectrometer (LAS) that segregates particles into size ranges stated to be >0.09, >0.20, and >0.50 μm in diameter. All work was performed in a Class 1 cleanroom.

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1. None of the DI waters is intended for use in the development or manufacture of semiconductor devices.

Results and Discussion

System background test: When the atomizer was operating without any water in the syringe, i.e., the syringe was pumping only N_2, very few particles >0.014 μm in diameter were detected (Fig. 1a). (The resolution of the CNC at the operating conditions of these experiments is 10 particles/ft^3.) Of the 221 data collection intervals shown, zero particles were detected in 196 of them. A large fraction of the particles detected were $>$ 0.2 μm in diameter (compare Figs. 1a and 1b). (The resolution of the LPC at the operating conditions of these experiments is 5 particles/ft^3.)

Concentration of particles produced by the atomizer: Average particle counts are given in Table I for all experiments on the DI-1, -2, and -3 waters. Each number is an average of 4 runs. Each run was of 6-8 hours duration with particle counts taken every 2 minutes. Consequently, each concentration in the table is an average of 700 to 1000 data points. Since the particle concentration resulting from operation of the system is negligibly small (Fig. 1), no background correction was necessary. A background correction for particles in the liquid water was also not necessary. This can be understood from the particle concentration expected in the aerosol when 1 cm^3 of water containing a given particle concentration is atomized. If 1 cm^3 of water with a solid particle content of $10^5/cm^3$ (the highest observed for any water) is atomized at a liquid feed rate of 1 cm^3/hr and a total N_2 flow rate of 16.5 l/min, the particle concentration in the resultant aerosol attributable to these particles will be $2900/ft^3$. Since the measured concentrations in the aerosol (sum of each row in Table I) are three to four orders of magnitude greater, essentially all the particles detected in the aerosol must originate from nonvolatile, dissolved matter or particles <0.06 μm in diameter, e.g., colloidal silica, in the liquid water.

Several conclusions may be drawn from these data. (a) Good agreement is observed between the LPC and LAS particle counters, providing additional confidence in the reliability of these measurements. (b) Within experimental error, there is no difference among the concentrations and size distributions of the aerosols generated from the three waters. (c) There is a small but real effect of temperature. To illustrate this, the results from the DI-3 water and PU tubing are summarized in Figure 2, where particle concentration is plotted as a function of aerosol temperature and particle size. For all sizes, the particle concentration decreases slightly with increasing temperature. This can be attributed, at least in part, to the volatilization of low-boiling point organics (2). (d) Within experimental error, the three plastic tubings do not affect the concentration or size distribution of the aerosol particles.

The dissolved matter that gives rise to the particles in the aerosol is not ionic, since the concentration of dissolved salt in the water is <1 ppb, as calculated from the resistivity of the water (>18 MΩ−cm) and the calibration curve of Egan (5). By process of elimination, the dissolved matter is probably largely organic. The data for the O_3 − treated water are also shown in Figure 2. The large difference in concentration for the DI-3 and O_3 − treated waters is consistent with the conclusion that the dissolved matter is mainly organic. The results are explained as follows: Since the number concentration of aerosol droplets is not changed by the level of contamination, the total

Table I

Particle concentrations and 95% confidence intervals for aerosols generated from the different waters.

			Log (particles/ft^3)					
Water	Tubing	T,°C	>0.014 μm (CNC)	>0.09 μm (LAS)	>0.20 μm (LPC)	>0.20 μm (LAS)	>0.50 μm (LPC)	>0.50 μm (LAS)
DI-1	PU	22	7.21±0.01	5.30±0.05	4.67±0.03	4.65±0.02	3.20±0.03	2.93±0.03
	PU	70	7.16±0.01	5.08±0.03	4.54±0.04	4.58±0.04	2.94±0.04	2.55±0.05
	PU	120	7.09±0.01	4.83±0.02	4.14±0.02	4.06±0.03	2.51±0.03	2.24±0.07
	PTFE	120	7.16±0.01	5.07±0.01	4.44±0.02	4.36±0.02	2.71±0.02	2.62±0.04
	PFA	120	7.19±0.00	4.79±0.01	4.12±0.03	3.99±0.02	2.49±0.04	2.50±0.07
DI-2	PU	22	7.28±0.00	5.41±0.01	4.86±0.02	4.79±0.01	3.11±0.02	2.68±0.03
	PU	70	7.26±0.01	5.13±0.01	4.61±0.03	4.47±0.02	2.63±0.02	2.09±0.05
	PU	120	7.21±0.01	5.18±0.02	4.54±0.03	4.39±0.02	2.69±0.02	2.27±0.05
	PTFE	120	6.96±0.02	5.16±0.02	4.22±0.03	4.09±0.03	2.60±0.06	2.65±0.10
	PFA	120	7.26±0.01	5.29±0.02	4.62±0.03	4.52±0.02	2.83±0.03	2.76±0.05
DI-3	PU	22	7.28±0.01	5.35±0.02	4.77±0.03	4.68±0.03	2.89±0.03	2.59±0.04
	PU	70	7.24±0.00	5.10±0.02	4.56±0.04	4.46±0.02	2.81±0.02	2.43±0.04
	PU	120	7.21±0.01	5.01±0.02	4.44±0.02	4.34±0.03	2.59±0.03	2.35±0.08
	PTFE	120	7.20±0.01	5.02±0.02	4.44±0.03	4.39±0.02	2.80±0.03	2.63±0.06
	PFA	120	7.14±0.01	4.91±0.02	4.38±0.07	4.29±0.03	2.78±0.05	2.68±0.08

number of particles should be identical for all contamination levels. However, particle size will decrease as the concentration decreases, so that the particle-size distribution curve shifts to lower sizes. The tail in the distribution at large diameter (>0.5 μm) vanishes, while the number of particles <0.014 μm increases. The number of particles >0.014 μm decreases only 20% because the shift in the distribution curve moves many of the large particles into sizes between 0.014 and 0.2 μm.

From the particle-concentration and particle-size distribution data in Table I, we estimate the total concentration of nonvolatile dissolved and fine particle contamination in the liquid water from which the aerosols were generated. The average data for the DI−3 water from Table I are plotted in Figure 3 as particle concentration vs. the lower size limit of the particle diameter. The abscissa is divided into 9 size channels from 0.014 μm to 2 μm (Fig. 3),[2] and the particle concentration in the N_2 carrier gas of each channel is obtained by subtracting out the particle concentration of all channels containing larger particles. The mass/ft^3 of particles for each channel is then calculated assuming a diameter equal to the upper size limit of the channel and a particle density of 1 g/cm^3. From the sum of the masses/ft^3 in each channel and the liquid water and N_2 feed rates, the concentration of nonvolatile dissolved and fine particle contamination is calculated to be 8×10^{-8} g/cm^3 $H_2O(l)$. The calculation assumes that a negligible amount of water is lost in atomization or by adsorption on the walls of the apparatus. It was determined experimentally that the loss of water during atomization was only 3 ± 2%. Deposition of dried particles on the walls was determined to be small, i.e., <10%. Deposition of wet aerosols, before drying, could not be measured or estimated. The path of travel of these aerosols through the 3/8" i.d. tubing was approximately 1 ft. The overestimation inherent in using the upper limit of the particle size in the mass calculation is estimated to be a factor of 2-4 and opposes any error caused by loss due to deposition of wet aerosol particles.

For the DI-3 water, 8×10^{-8} g/cm^3 is the typical and 3×10^{-9} g/cm^3 is the lowest concentration of nonvolatile dissolved and fine particle contamination measured. The O_3 − treated water contained 2×10^{-9} g/cm^3 of such contamination.

Conclusions

An analytical system for measuring nonvolatile dissolved and fine particle (<0.06 μm in diameter) contamination at the ppb level in water has been described. The system is relatively simple and inexpensive to setup and run. It is an invaluable aid in any laboratory or factory that must maintain a high level of purity in its processing water. The method should also be applicable to other processing liquids as long as these liquids are compatible with the materials they will contact in the atomizer, particle counters, and auxiliary equipment.

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2. All particles >1.0 μm are assumed to fall in the channel 1-2 μm, which is not shown in Figure 3.

The system was applied to the analysis of aerosols generated from four different waters. Although the solid particle content of the waters differed by several orders of magnitude, the aerosols generated from three of these differed little in concentration or size distribution. In the fourth water, dissolved organic matter was oxidized by O_3, and the concentration of contamination was markedly less. It was shown that the aerosol particles come mainly from nonvolatile dissolved matter (primarily organic) and possibly from particles in the liquid water < 0.06 μm in diameter, e.g., colloidal silica.

Acknowledgement

We thank J. B. Bindell for very valuable discussions.

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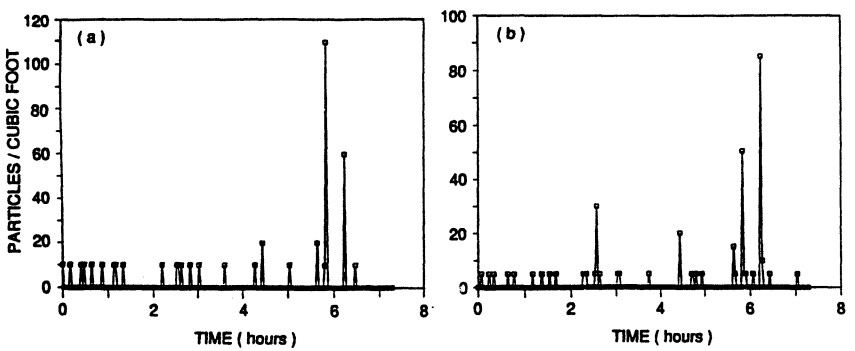

Figure 1. Background concentration of particles in the system. The system was fully operating except that it was pumping N_2 gas instead of water. (a) Particles > 0.014 μm, as measured with a CNC; resolution of counter is 10 particles/ft^3. (b) Particles > 0.20 μm, as measured with a LPC; resolution of counter is 5 particles/ft^3.

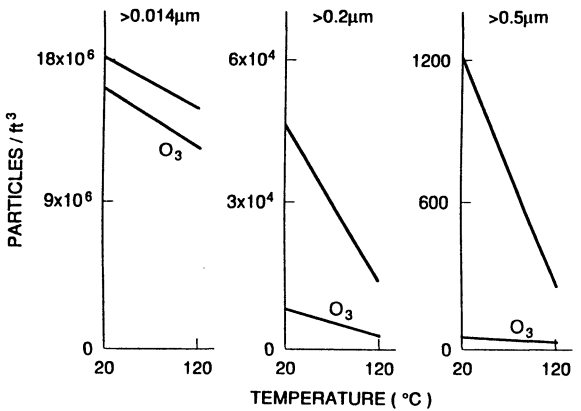

Figure 2. Particle concentration for aerosols generated from DI-3 water and O_3 – treated water as a function of aerosol temperature.

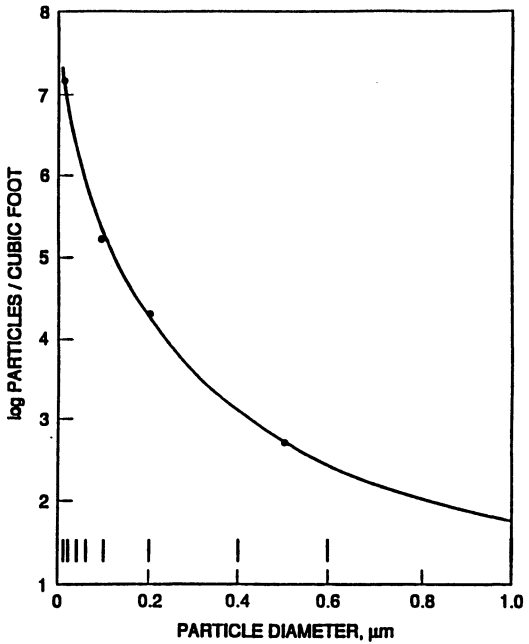

Figure 3. Particle concentration vs. diameter for the smallest particles, as measured for DI-3 water. As an initial step in calculating the concentration of nonvolatile dissolved matter in liquid H_2O, the concentrations within channels that are shown across the bottom of the figure were determined, as indicated in the text. It was assumed that all particles > 1 μm were in the channel from 1 – 2 μm, which is not shown.

A SIMPLE MODEL FOR RINSING

A.Tonti
SGS-Thomson Microelectronics
2,V.Olivetti
20041 Agrate,Italy

A new and simplified treatment is given of the tank rinse process,mainly as a guide to technologists and equipment designers.The rinse is seen as a unidimensional diffusion process within the hydrodynamic boundary layer.Equations are given to describe this process,as well as the relation between the impurity contaminant concentrations monitored and the (much higher) effective ones at the wafer surface.Monitoring techniques and equipment optimization are described,with emphasis on megasonic rinsing as the most effective process.

GENERALITIES

The rinse process has not yet received a complete theoretical treatment,not even in an approximate form.

Apart from a series of very elementary papers (1-4) which, nevertheless,are rather clarifying form a purely technical point of view,the only complete treatment has been given by Kubik (5) but the mathematical approach is rather ad-hoc,not starting from first principles. His equations are rather unwieldy and some results,as e.g.the carryover layer thickness,are at odds with accepted values.

An in-depth treatment has been given by Hu (6) but unfortunately without a complete model.

In this situation it is felt that the subject is ripe for a complete treatment.

THE BOUNDARY LAYER APPROXIMATION APPROACH

At the end of a wet process step an hydrophilic surface is covered by a thin film of a rather concentrated solution,called "carryover",of about 20 micron thickness (7).

Within this layer ions from the chemical,ions and molecules from impurities and suspended particles are trapped.

During the following rinse in an overflow tank,where the speed of water is of the order of 1 cm/s on the wafer surface,a boundary layer develops with a mean thickness given by

$$\overline{\delta}=\frac{2}{3}L\sqrt{\frac{\nu}{UL}} \qquad [1]$$

where U is the water velocity,L the wafer diameter and ν the kinematic viscosity.Inserting the normal values for these parameters we obtain a mean boundary layer thickness of 0.26 cm.

Even in the case of a very strong stirring (e.g. by nitrogen bubbling) δ is still around 300 microns,and therefore is in any case much greater than the dragout film thickness.

The carryover film is safely embedded within the boundary layer and protected by it even during introduction in the rinse tank and subsequent extraction.

In the boundary layer approximation the rinse process may be described by the unidimensional diffusion of ions or particles out of the

carryover film into bulk d.i. water,taken as perfectly stirred. This is a classical diffusion problem which may be treated in an approximate way to give,as a final result (7):

$$f = \frac{c(0,t)}{c_o} = \frac{b}{\sqrt{\pi D t}} \qquad [2]$$

where f is the fraction of contaminant left close to the surface after rinsing for a time t, b is the carryover film thickness,around 20 microns,and D is the diffusion coefficient for the contaminant species.

The boundary layer approximation is widely used in engineering;it replaces an exact solution of the three-dimensional diffusion equation in a moving medium - a rather formidable task - by an approximate solution which only takes into account the diffusion within the boundary layer, taken as immobile,and into the perfectly stirred bulk water.

This makes the whole diffusion process rather insensitive to the actual conditions within the rinse tank:it is mainly the boundary layer condition that matters.

The approximation chosen neglects the lateral motion of the fluid within the boundary layer,which sweeps away the contaminants and speeds the diffusion up.As such,it is strictly applicable to infinite surfaces:on finite ones it gives conservative estimates for the rinse parameters (e.g. time or residual concentration).

Inserting in eq.[2] the appropriate values for D,we may find the residual concentrations of ions and particles in the original dragout film after rinsing for a given time t,say 1000"or 16'(see Tab.I). These are of the order of 0.01 for ions and 0.3 for particles.

RINSE MONITORING

Contaminants within the tank or at the overflow outlet may be monitored by several techniques.Particles may be counted and sized:ions may be monitored by resistivity measurement or by specific analytical techniques (ion chromatography or sensitive spectral methods like GFAA, ICP/OES or ICP/MS).

The latter ones lend themselves to a quantitative process characterization,while the first one is mostly aimed at process control.

With standard instruments the practical sensitivity of conductivity measurement in pure water at 25 deg C is about 0.3 nS/cm at 54.82 nS/cm, equivalent to about 0.1 ppb NaCl. With the best instruments it may be pushed up to 0.03 nS/cm,or about 10 ppt Na Cl.

The best measurement setup is by means of two cells,at the inlet and outlet,with a differential output.This arrangement eliminates most of the electrical and electrochemical noise and drift,and requires a much less exacting temperature compensation,particularly over the limited range of interest (19 to 25 degrees C).

A practical limit on the rinse water conductivity may be obtained by the allowable surface contamination (say 10^{10} at/sqcm) which,taking a 20 micron carryover film thickness,translates into 0.2 ppb Na,0.5 ppb NaCl or 1.3 nS/cm conductivity increase (17.8 Mohm.cm at 25 deg C).

We must not take,however,this value as a good rinse end point!

THE RINSE PROCESS IN AN OVERFLOW TANK

We first make the hypothesis of perfect mixing,i.e. the solution is so well stirred that outside the boundary layer the concentration is equal

everywhere to the outlet one, c_m.

At t=0 and x = 0 c = c_o, while at x > 0 c = 0.

For t > 0 at x = 0:

$$c(x) = c(0,t)\exp\left(\frac{-x^2}{4Dt}\right) = \frac{c_o b}{\sqrt{\pi Dt}}\exp\left(\frac{-x^2}{4Dt}\right) \qquad [3]$$

The concentration gradient dc/dx and the diffusion flux per unit area, F, are given by:

$$\frac{dc}{dx} = c(0,t)\exp\left(\frac{-x^2}{4Dt}\right) * \left(-\frac{2x}{4Dt}\right) = -\frac{c(0,t)}{2Dt\sqrt{\pi Dt}}\exp\left(\frac{-x^2}{4Dt}\right) \qquad [4]$$

$$F(x,t) = -D * \frac{dc}{dx} = \frac{1}{2} * c(0,t) * \frac{x}{t}\exp\left(\frac{-x^2}{4Dt}\right) \qquad [5]$$

and, at the boundary level outer side, where x = $\bar{\delta}$, the outgoing flux per unit area is:

$$F(\bar{\delta},t) = \frac{1}{2}c(0,t) * \frac{\bar{\delta}}{t}\exp\left(-\frac{\bar{\delta}^2}{4Dt}\right) \qquad [6]$$

while the total outgoing flux is:

$$\Phi_i = A_{tot} * \frac{c(0,t) * \bar{\delta}}{2t}\exp\left(-\frac{\bar{\delta}^2}{4Dt}\right) \qquad [7]$$

taking also eq.[3] into account, we finally derive the following expression for the time evolution of the outlet contaminant concentration:

$$c_m = \frac{\Phi_i}{\phi_w} = \frac{A_{tot}}{\phi_w} * c(0,t) * \frac{\bar{\delta}}{2t}\exp\left(-\frac{\bar{\delta}^2}{4Dt}\right) = \frac{A_{tot}}{\phi_w} * \frac{c_o b}{\sqrt{\pi Dt}} * \frac{\bar{\delta}}{2t}\exp\left(-\frac{\bar{\delta}^2}{4Dt}\right) \qquad [8]$$

Taking, now, reasonable values for the parameters:

$A_{tot} = N*A_w + A_c \sim 900$ sq cm

$\rho_w \sim 10$ l/min ~ 160 cm^3

b $\sim$ 20 micron $\sim 2*10^{-3}$ cm

we may plot the resulting c_m values for several stirring levels and contaminant species (see fig.1).

It is worth while noting that c_m is always much smaller than the surface concentration c(0,t). Therefore a low concentration of contaminant in the overflow stream is absolutely no guarantee that the rinse is completed.

The only way to verify completion is to record the minimum time at which no harmful effects are present, or to stop the flow of water and measure the final concentration after enough time has been given for the impurity to completely diffuse in water.

OVERFLOW TANK RINSE

As we have seen it is very important to strive for the best stirring by nitrogen bubbling, high flowrates, efficient monitoring and so on.

The rinse is hardly completed in 15'.It may be necessary to lengthen it:

to eliminate a concentrated chemical from the surface (in the worst case,100% initial concentration,it is still about 1% after 15' rinsing and 0.5 % after 1 h:there may be acute problems due to subsequent corrosion or surface contamination)

to eliminate a contaminant:if the initial level is 1 ppm,after 15' we may still have about 10 ppb at the surface,which may still give rise to residual contamination at a 2 $*10^{11}$ at/sqcm level:definitely too much for submicron integrated circuits.

The tank design should be without dead spots,and of the smallest practical size,e.g.enough to accommodate one carrier with 1 cm clearance.

The flow pattern should be optimized in order to minimize dead zones and maximize the water velocity on the wafer surface.These two scopes are contradictory.

In a small tank the best solution seems to be a distributed feed which is stronger under the carrier,as may be obtained with a distribution plate with different size holes.

In a bigger tank the best one seems to be a concentrated, fan shaped feed to sweep the whole wafer surface,plus some side flow to suppress dead spots.

Round tanks minimize dead spots in the corners but give rise to a waste of useful volume and flowrate.

Of all these conditions,the most important one is that relative to a strong stirring effect by nitrogen bubbling.

It is also important to effectively monitor the water conductivity at the inlet and outlet:to actually reach 0.1 nS/cm excess conductivity over the initial one may require more than 20', and the same applies also to particle monitoring,which is important in critical rinse steps,at least as an engineering study.

From the above remarks overflow tank rinsing emerges as an inherently inefficient technique.

CASCADE AND QUICK DUMP RINSING

In the case of static tank rinsing the advantages of a sequential cascade process have been discussed (6).The argument,leaning on the high ratio between the tank and the carryover volume,strictly applies only to equilibrium,i.e. extremely long rinse times.

A similar argument applies,however,also to sequential overflow cascade rinses far from equilibrium,i.e. at reasonably short rinse times.

If the residual fraction after a 15' rinse is 0.0088,after a 7.5' one will be 0.0124 ;after an additional 7.5'in a different bath it will be $(0.0124)^2$ or 0.000154.This big improvement is entirely due to the removal of the biggest part of the boundary layer,which speeds up diffusion.

Similar arguments apply to quick dump rinsing:each cycle is equivalent to a short (~1') overflow stirred rinse.

One disadvantage is that it is very difficult to monitor the water conductivity;QDR is also not advisable for hydrophobic wafers,due to the multiple passes through a liquid surface,except under the very cleanest conditions.

The optimization of QDR calls for:

a generous drain time at the end of each dump phase in order to reduce the carryover layer thickness (at the same time it is necessary to

avoid drying the surface up:the use of clean nitrogen,saturated with water vapor,for tank backfill might be advisable).
very effective nitrogen bubbling and stirring;
small tank size,no dead zones;
moderate to strong water flowrates (less than 1' change time).

ADDITIONAL WAYS OF IMPROVEMENT

Temperature

It acts by lowering the viscosity and therefore b;at the same time D is increased.A factor 10 improvement may be theoretically expected between room temperature and 95 deg.C.

Full flow processing

This technique offers distinct advantages for hydrophobic wafers,since no pass is made through a liquid surface.On the other side,the advantages of multiple cascade rinses are negated:it is expedient to maximize diffusion by increasing the stirring rate (nitrogen injection, ultrasonics, high water flowrate,etc.).

ULTRASONICS

This case has been again completely treated by Hu (6).Its big advantage lies in the fact that the sonic field induces an intensive streaming in the liquid,and its thin acoustic boundary layer replaces the much thicker hydrodynamic boundary layer,so that diffusion is enormously accelerated.
The acoustic boundary layer thickness is given by:

$$\delta_a = \sqrt{\frac{\eta}{\pi \nu \rho}} \qquad [9]$$

where η is the dynamic viscosity,ρ the liquid density and ν the sonic frequency.
At a 40 kHz frequency (typical ultrasonic) the boundary layer is only 3 micron,and at 1 MHz (megasonic) only 0.6 micron thick.
Since now the sonic boundary layer is much thinner than the carryover film,the diffusion conditions change drastically (6).An approximate expression for the residual fraction becomes:

$$f = \frac{8}{\pi^2} \exp\left(-\frac{D\pi^2 t}{4\delta_a^{\,2}}\right) \qquad [10]$$

where δ is the acoustic boundary layer thickness.

The residual concentration fractions may be tabulated for 0.5 micron particles ($D^{-}8*10^{-9}$),for several rinse times (see tab.II).
The residual concentration of the much more mobile ions is always zero.
Megasonics,so,seem to be the ultimate tool to achieve really efficient rinses.To take full advantage of its capability,provisions must be made to minimize corrosion on the transducers and windows,as well as particle generation from the walls under the intense sonic beam.Perhaps the best arrangement is that in which the beam does not touch the walls,and the carrier is swept to and fro across the static beam.

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TAB.I - RESIDUAL CONCENTRATIONS AFTER A 15' RINSE

CONTAMINANT	DIFFUSION COEFFICIENT	RESIDUAL CONCENTRATION
Na	$1.33 * 10^{-5}$ cm²/s	0.0088
Au,Cu,Fe,Ni	$0.7 * 10^{-5}$ cm²/s	0.0121
0.3 /u particles	$1.4 * 10^{-8}$ cm²/s	0.26
0.5 /u particles	$8 * 10^{-9}$ cm²/s	0.34

TAB.II - RESIDUAL PARTICLES AFTER ULTRASONIC RINSING

TIME	ULTRASONIC RINSE	MEGASONIC RINSE
1"	0.65	$3.4 * 10^{-3}$
10"	0.09	$1.3 * 10^{-24}$
60"	$1.6 * 10^{-6}$	0
100"	$2.5 * 10^{-10}$	0

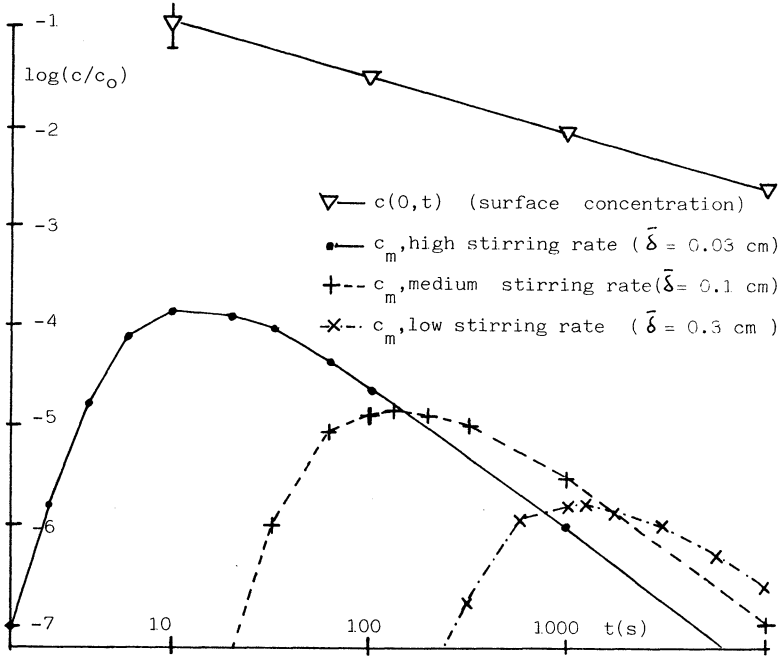

Fig.1 Outlet concentrations of contaminant (Na) vs. rinse time

VAPOR PHASE CLEANING OF METALLIC IMPURITIES ON SILICON USING NITRIC OXIDE BASED REACTIONS

Ronald M. Gluck

EASTMAN KODAK COMPANY
Microelectronics Technology
Bldg. 81, Rm 324
Rochester, New York 14650-2019

ABSTRACT

Nitric oxide is shown to volatilize copper impurity from silicon surfaces at 500°C. Gold can be volatilized with mixtures of nitric oxide and anhydrous hydrochloric acid at 900-1000°C, although each gas used alone is ineffective. A thin silicon reaction product is formed at temperatures of 800°C and above, which inhibits subsequent oxidation. This film can be removed with 1.1:1 selectivity to silicon using a plasma of CF_4, H_2 and N_2. Nitric oxide bonding and chemistry is reviewed. Metal complexes with nitric oxide and chlorine are discussed. A microscale picture of the metal removal process is developed using vibrationally excited cleaning gases. The potential improvements associated with electronically excited reagents are considered.

INTRODUCTION

The emergence of vapor phase cleaning of silicon was reported at the first cleaning technology symposium two years ago. Concepts such as HF vapor processing to remove surface oxides (1), ultraviolet (2), or remote plasma (3) activated halogen to reduce metallic contaminants and ultraviolet ozone systems (4) for organic elimination, were presented. These developments are useful for devices with small dimensions and high aspect ratios where liquid cleaning systems are becoming less effective. Additionally, vapor phase cleaning has additional advantages such as reduced particulates associated with cleaner reagents, no drying residues and compatability with integrated processing (5).

This paper will discuss the novel use of nitric oxide (NO) alone and in combination with anhydrous hydrochloric acid (HCl) vapor as a cleaning agent for silicon devices. The technology was disclosed in 1977 (6) and patented in 1979 (7).

Nitric oxide has been reported to react with a large variety of materials, including metals, ionic species, and organics. Due to its odd unpaired electron it can bond by sharing an electron pair to give a covalent compound X - NO, accept an electron to form a nitrosyl compound $X+NO^-$ or donate 1 to 3 electrons to form a nitrosonium compound $X-NO^+$. This paper will specifically report on the removal of metallic copper and gold from silicon and the removal of a reaction product film formed by the action of cleaning gases. A hypothesis of the cleaning chemistry will be presented.

EXPERIMENTAL

Radiotracer copper ^{64} and gold ^{198} were plated on silicon surfaces from hydrofluoric acid solutions. The samples were subjected to reactive gas exposures in a diffusion furnace, operating in the range 500 - 1100°C for periods from 1 to 15 min. Nitric oxide concentrations ranged from 1.9% to 32.6% and HCl concentrations were varied from 2.7% to 64%, with the carrier gas being nitrogen. Neutron activation analysis and radiotracer analysis were used to monitor impurity levels. ESCA was employed to characterize the composition of a film formed on the silicon surface by reaction with the cleaning gases. This film was created at cleaning temperatures of 800°C and above. Film removal was studied using plasma etching with mixtures of CF_4, H_2, and N_2 gases in a quartz barrel type reactor.

RESULTS

It was found that Cu^{64} could be efficiently removed from silicon using NO alone, but that use of HCl improves the cleaning efficiency. The data shown in fig. 1 shows the % Cu^{64} remaining on samples after treatment with reactive gases for 2 min as a function of temperature. The initial Cu^{64} doping level used was $1 \times 10^{15}/cm^2$.

Removal of Au^{198} was found to be relatively inefficient using either NO or HCl alone. However, by using combinations of the reagents, Au^{198} could be removed with greater effect. The efficiency of Au^{198} removal is shown in Fig. 2 as a function of temperature for a range of gas compositions. The cleaning time was 5 min and the initial doping level was in the range $3 \times 10^{10}/cm^2$ to $4 \times 10^{12}/cm^2$. The effect of Au^{198} doping concentration and gas exposure time on cleaning efficiency is shown in Fig. 3. It is seen that a majority of the loss occurs in 1 min or less. Higher cleaning gas

concentration improves the final removal efficiency by 16%. The effect of doping level is minor.

A typical self limiting film formed on silicon by a 5 min exposure to NO and HCl was depth profiled using ESCA with argon gas sputtering. The film composition as a function of etch time is shown in Table 1.

TABLE 1 ESCA profile after cleaning with 5.4% HCl/4.5% NO 5 min at 1000°C

Etch Time	Si Neutral	Si Oxidized	O	N	Cl
0	0.20	0.24	0.46	0.07	0.03
30 sec	0.37	0.22	0.33	0.05	0.03
1 min	0.42	0.21	0.30	0.05	0.02
2 min	0.61	0.15	0.20	0.02	0.02
3 min	0.70	0.11	0.14	0.03	0.02

The etch rate is approximately 10 Å/min and the measurement depth extends about 20 Å below the etched surface. Silicon was found in two forms; one typical of self bonding, termed "Si Neutral" and one that is bonded to other atoms, termed "Si Oxidized". Non-silicon atoms are present at highest levels at the top surface of the film. The presence of a silicon reaction film was found to affect the thickness of subsequent oxidations as shown in Fig. 4. The % inhibition is given by

$$\% I = \frac{\text{Tox-u - Tox-G}}{\text{Tox-u}} \times 100$$

Where Tox-u is the oxide thickness of untreated silicon dry oxidized at 1050°C for 60 min and Tox-G is the thickness of the resulting dielectric formed on a gas-cleaned sample exposed to the same oxidation. It is seen that an oxidation inhibition effect is created at temperatures in excess of 800°C, where Au^{198} cleaning is optimized.

The removal of the silicon reaction film ($SiO_xN_yCl_z$) was studied using plasma etching with CF_4, H_2, and N_2 in a quartz barrel reactor. The etching conditions and results are summarized in Table 2. For experimental convenience, the selectivity defined as film etch rate/Si etch rate, was optimized for thermal oxide films, which could be prepared and thickness monitored easily. The selectivity of $SiO_xN_yCl_z$ film was determined for the conditions found to optimize SiO_2. Assuming a $SiO_xN_yCl_z$ film thickness

of 80 Å, a 1:1 selectivity of the plasma etch and a 50% overetch to assure complete removal, less than 70 Å of silicon is consumed per clean cycle.

TABLE 2 Plasma etching optimization for selective etching of $SiO_xN_yCl_z$

Film Material	Etch CF_4	Gas H_2	Ratio N_2	Pressure (Torr)	Temperature °C	Film Etch Rate Å/min	Si Etch Rate Å/min	Selectivity
SiO2	1	1	2	0.39	115	47.5	85	0.1:1.8
SiO2	1	1	2	0.39	150	80	87	0.9:1.0
SiO2	1	2	4	0.35	130	52	49	1.1:1.0
SiO2	1	1	2	0.39	200	118	70	1.4:1.0
$SiO_xN_yCl_z$	1	1	2	0.37	200	78	70	1.1:1.0

DISCUSSION

Nitric oxide bonding

The field of nitric oxide-metal chemistry is quite diverse due to the reactive nature of nitric oxide and its ability to form compounds by either donating, sharing, or accepting electrons. The electronic structure of nitric oxide as shown in Fig. 5 contains an unpaired electron. A low ionization potential of 9.5 eV exists that promotes the donation process to form nitrosonium ions or shared electron bonds. Most of the reported NO reaction products are termed coordination compounds in which 1 to 3 electrons are donated to form bonds to a central metal atom. The metal typically coordinates to 4 to 6 ligands of which NO can be one of many types. Other ligands include halogen, hydroxyl, oxygen, and a multitude of organic molecules. NO also will react with strong electropositive metals such as Na, K, and Ba to form ionically bonded nitrosyl compounds.

Nitric oxide compounds

The most important property of nitric-oxide metal compounds from the perspective of this paper is their limited thermal stability. The highest reported stability is for metal nitrosyls, with KNO decomposing at about 300°C. A list of metal compounds that contain NO or NO and Cl is shown in Table 3. Most of the compounds were obtained from a review by Johnson and McCleverty (8).

TABLE 3 Metal compounds containing NO or NO and Cl Groups

$V(NO)Cl_4$	$K_2Os(NO)Cl_5$	$\{Ni(NO)Cl_2\}_n$(d>150°C)	$Ru(NO)_4$
$V_2(NO)Cl_2$	$Cs_2Os(NO)Cl_5$	$\{Fe(NO)_2Cl\}_2$	$Fe(NO)_4$(d>0°C)
$V_2(NO)Cl_8$	$K_2Pt(NO)Cl_5$	$\{Co(NO)_2Cl\}_2$(m = 101°C)	$Co(NO)_3$
$\{MO(NO)_5Cl_2\}_n$	$Na_2Pt(NO)Cl_5$	$Mn(NO)Cl_3$	$Ba(NO)_3$
$\{W(NO)_2Cl_2\}_n$	$\{Ni(NO)Cl\}_n$	$Fe(NO)_3Cl$(s = 110°C)	K(NO)(d = 300°C)
$\{Rh(NO)_2Cl\}_n$	$Cu(NO)Cl_2$		Na(NO)(d = 155°C)

n = oligameric s = sublimation temp. d = decomposition temp.
m = melting temp.

The coordination compound with greatest stability is $\{Ni(NO)Cl_2\}_n$, which decomposes above 150°C. Dimers or polymeric compounds generally exhibit more stability than monomers.

Nitric oxide complexes

A relevent area of metal - NO chemistry deals with the formulation of complexes using matricies such as solidified inert gases and metalized zeolites. Tevault and Nakamoto (9) studied $\{SnCl_2$ - NO$\}$ and $\{PbF_2$ - NO$\}$ in solid argon at 10 K using infrared spectroscopy. Chao and Lunsford (10,11) formed $\{Cu(I)$-NO$\}^+$ and $\{Ag(I)$-NO$\}^+$ in Y type zeolite structures by exposing the metal ion exchanged zeolite to partial pressures of NO at room temperature. Electron paramagnetic resonance and infrared spectra were used to characterize the complexes. Breckenridge et al, (12,13) have shown that vaporized Zn (425°C) and Cd (290°C) mixed with NO and excited by ultraviolet radiation can create an electronically excited state in NO,which is not seen when the metals are absent. The existence of a metal - NO complex during the energy transfer between excited state metal atoms and ground state NO molecules was discussed. As a final example of metal - NO interactions, Ritter and Weishaar (14) studied the kinetics of the reaction of gas phase neutral transition metals Sc, Ti, and V in the ground state with NO at 300 K using a fast flow reactor. They found that laser-induced fluorescence of the metal species was reduced at a higher rate by NO than other gases like O_2 and N_2O. The experimental data could not be reconciled with their models that assumed metal reaction via an oxidation mechanism. A metal - NO complex was not considered but may be responsible for the observed effects. The preceding survey does not confirm the existence of metal - NO or metal - NO - Cl complexes at the elevated temperatures used for silicon cleaning. However, it serves as background to support a hypothesis in which volatile complexes (or compounds) are

formed at high temperature zones in the presence of metal and cleaning gas, ultimately transporting metallic species to cooler regions.

Microscopic model

The cleaning process can be viewed as competition between a volatilization process that physically removes contaminants and diffusion processes that drive impurities into the bulk silicon. Silicon surfaces are usually covered with native oxide unless special precautions are made to exclude oxygen. Impurity metals can be located on top of the native oxide, buried in the layer, or can be present in contact with bulk silicon. The metals can be present as positively charged ions or neutral atoms. Some metals form strong bonds to oxygen that tends to reduce diffusion into the bulk silicon.

The cleaning process starts with exposure to the reactive gases followed by heating. As the silicon increases in temperature, the cleaning gas becomes more reactive by assuming vibrationally excited states. The cleaning gas forms volatile species with the metals as shown schematically in Fig. 6. The specific nature of these volatile species is open to conjecture. They may well be fully coordinated monomeric compounds with 4 to 6 ligands, since volatility is not an issue, or partially coordinated complexes. The fact that gold requires both NO and HCl reactants for effective cleaning suggests that both ligands are involved. Metal ions bonded to oxygen may retain those bonds, but will not volatilize without additional bonding to cleaning gas. The synthesis of metal - NO compounds is facilitated by having metallic species in an oxidized state so that NO ligands replace existing ones. This implies that catonic species should react at least as well as neutral metals.

At temperatures in excess of 800°C the cleaning gases form a layer of $SiO_XN_YCl_Z$. This is presumed to occur by diffusion of the reactants through the native oxide layer to the bulk silicon. In addition, the cleaning gas apparently also reacts with the growing film since the ESCA results show neutral silicon species at the surface and higher concentrations of nitrogen at the surface than near the silicon substrate. The metallic impurities present on, or in the native oxide must react very quickly with the cleaning gases to prevent loss to the bulk where most metals have very high diffusion coefficients. Both metals involved in this investigation were plated on the silicon surface as neutral metals. The subsequent formation of native oxide may have displaced the metals from direct contact with the bulk. The calculated diffusion rates for copper at 500°C and gold at 900°C in bulk silicon are 5.8 and 7.0 μm/sec, respectively. This translates into an average displacement of 10Å in less than 2×10^{-4} sec. The conclusion to be

drawn is that either the metals volatilize within less than 1 sec or that a diffusion barrier exists due to the initial native oxide or any subsequent $SiO_xN_yCl_z$ formed. The diffusion barrier argument is supported by the gold removal data of Fig. 3 where 12 to 30% of the metal is removed between 1 and 5 min of the process. Also the self limiting nature of $SiO_xN_yCl_z$ attests to it being an effective barrier to the cleaning gases.

At temperatures less than 800°C the silicon does not react with the cleaning gas to form a barrier. The removal of noble metals such as gold will not occur, but more reactive metals such as copper are swept away. If noble metals are not present in sufficient concentrations to create device problems, the cleaning can be carried out as a simple one-step process.

Cleaning improvements

Alternative forms of cleaning gas activation may be used to potentially improve surface cleaning efficiency. Temperatures needed to effect cleaning may be reduced by promoting the cleaning reagents to an electronically excited state by plasma generation or ultraviolet radiation. These excited gases should be sufficiently reactive to metallic species to create a reaction similar to that seen for vibrationally excited gases. The thermal requirements would be limited to levels needed to keep the reaction products in a gaseous state. Assuming the reaction products to be similar to compounds or complexes discussed previously, temperatures of 300°C or less should be adequate. Impurity diffusion effects would be minimized that would favor higher cleaning efficiency. Multicycle processes of cleaning and $SiO_xN_yCl_z$ removal might also be used to advantage.

If the relative reactivity of noble metals is higher than silicon using alternative activation, effective removal of these metals may be possible without the formation of $SiO_xN_yCl_z$. An apparatus that could be used to test the effects of alternative cleaning gas activation is shown in Fig. 7. Forms of activation of gases include direct RF plasma using transparent electrodes, plasma afterglow or ultraviolet radiation. Thermal activation could be pulse heating from radiant lamps. If $SiO_xN_yCl_z$ is formed, high selectivity removal using plasma etching with planar RF electrodes would reduce silicon loss.

ACKNOWLEDGMENTS

The author would like to thank Mr. David Hamblen for optimization of the plasma process for removal of silicon reaction product films and Dr. Roger Baetzold for helpful discussions on nitric oxide chemistry.

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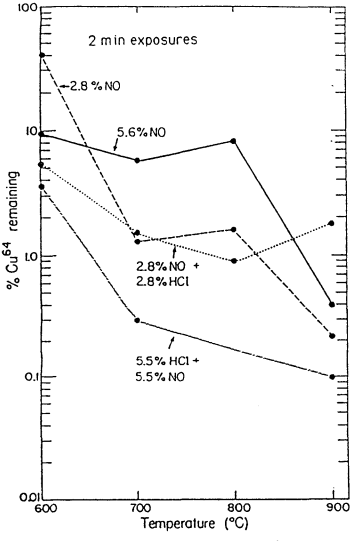

FIG. 1. Effect of temperature on Cu^{64} removal

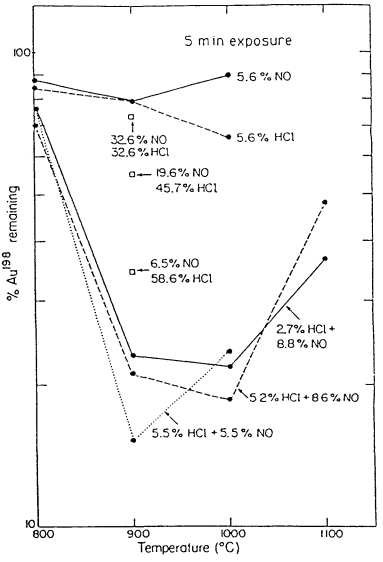

FIG. 2. Effect of temperature on Au^{198} removal

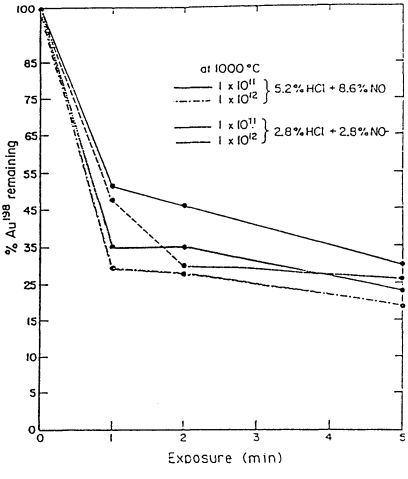

FIG. 3. Effect of Au^{198} doping, gas concentration and time on Au^{198} removal

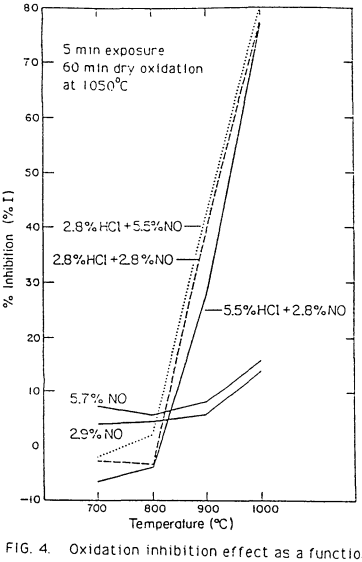

FIG. 4. Oxidation inhibition effect as a function of cleaning gas temperature

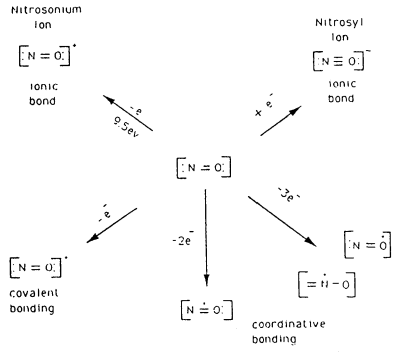

FIG. 5. Nitric oxide bonding types

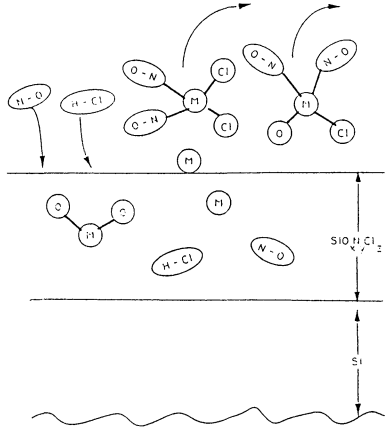

FIG. 6. Vapor phase cleaning process

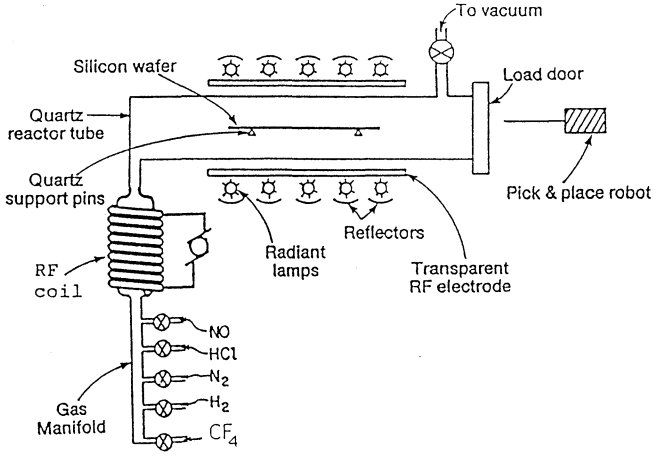

FIG. 7. Vapor phase cleaning apparatus

PRE-OXIDATION CLEANING OF SILICON USING REMOTE PLASMA

David C. Frystak[1] and Jerzy Ruzyllo

Center for Electronic Materials and Processing
Department of Electrical and Computer Engineering
The Pennsylvania State University
University Park, PA 16802

ABSTRACT

Presented in this paper are results of investigations into the feasibility of the use of plasma afterglow discharges in the cleaning of silicon surfaces prior to thermal gate oxidation. Gas mixtures of O_2, HCl/Ar, and NF_3/H_2/Ar were used to remove organic impurities, metallic impurities, and thin oxide layers respectively from the Si surface. Control of silicon etching during remote plasma cleaning in HCl/Ar is necessary to obtain a good SiO_2-Si interface. Reliability studies of thermal oxides grown on remote plasma cleaned substrates indicate that the process yields results comparable to conventional wet wafer cleaning.

INTRODUCTION

The quality of SiO_2 layers thermally grown on Si surfaces is a function of the cleanliness of the Si surface prior to the oxidation process. Surface cleaning is typically performed using liquids but in a variety of applications gas-phase alternatives are being sought after to perform this task. Among possible gas-phase, or dry, wafer cleaning methods, remote plasma cleaning appears to offer notable advantages in pre-oxidation cleaning.

The remote plasma technique has been investigated as a means of stimulating chemical reactions in the gas-phase for the removal of organic and metallic contaminants from the Si surface as well as for removing thin passivating oxide layers [1]. The results of a series of experiments on remote plasma cleaning are summarized and discussed in this paper.

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[1]) Present address: Texas Instruments, Inc., P.O. Box 655012, MS 944, Dallas, TX 75265

EXPERIMENTAL

In the reported investigation, silicon wafers were treated in the afterglow of a microwave plasma discharge. A diagram of the afterglow reactor used in this experiment is presented in Fig. 1. The gases are excited by means of a microwave discharge using a power source operating at 2.45 GHz and 400 watts. Premixed gases flow through a fused silica tube which passes through the resonant cavity of the generator. The substrates are located down stream from the site of the plasma discharge within a fused silica chamber housed in a conventional resistance heated furnace. The substrate temperature can be varied from room temperature to 1000°C. High purity fused silica is used to provide a clean environment in which the experiments can be performed. The plasma afterglow consists of excited species which are able to react with the silicon surface as well as any surface contaminants present on the wafer. Such a design is free from the hazards of ion bombardment associated with conventional plasma processing.

An outline of the basic experimental process flow is presented in Fig. 2. A variety of gas combinations were investigated and developed into useful cleaning processes. The processes can be applied individually or can be combined into a complete cleaning process performed in-situ with photoresist stripping. Subsequent thermal oxidation was performed on the cleaned substrates. The impact of the remote plasma processing was evaluated by means of electrical characterization of MOS capacitors formed on the treated substrates as well as with SIMS and NAA measurements. Comparisons were made with samples cleaned using standard wet chemical processes.

RESULTS AND DISCUSSION

A. Removal of Metallic Impurities

The gas phase removal of metallic impurities from the silicon surface is a difficult task. A reactive environment must be created in which volatile compounds of the metal species are formed. Prior to formation of such compounds the temperature of the silicon substrate must be held at levels sufficiently low to prevent diffusion of the metals into the bulk.

The afterglow of a gas mixture of HCl/Ar was found to be effective in removing Fe and Cu from the silicon surface [2]. The process involved exposing silicon wafers to a HCl(1):Ar(1) afterglow mixture at a substrate temperature of 200°C. Initial evaluation of the wafer cleaning processes consisted of SIMS analysis for detection of the presence of these impurities from intentionally contaminated substrates. The

results of SIMS profiling of Fe in oxidized Si wafers are presented in Fig. 3. Results are shown for the Fe contaminated, afterglow cleaned and wet cleaned after contamination and uncontaminated control samples. Samples exposed to wet cleaning or afterglow cleaning following the contamination step show a much lower Fe signal than the contaminated wafers. The SIMS data shows that the iron concentrations within the bulk of wet cleaned and afterglow cleaned samples are comparable to that of the control case. The data indicates that both cleans are removing a high percentage of the iron from the surface.

Cleaning experiments were also performed on samples intentionally contaminated with copper. Afterglow treatments were examined to determine the effectiveness of the HCl/Ar chemistry in removing the Cu impurity. A SIMS depth profile comparing levels of copper present within the processed samples is shown in Fig. 4. The control, wet cleaned and afterglow cleaned samples have very similar concentrations of Cu in the SiO_2 and Si interface region. Again, within the detection limit of SIMS, afterglow cleaning appears to be as effective as wet cleaning in removing the gross level of intentional copper contamination deposited on the silicon surface.

The lower amounts of metallic impurities detected in the afterglow treated samples are attributed primarily to the removal of the metallics from the sample surface during the afterglow etching/cleaning process. Diffusion of metallics away from the interface during afterglow processing at 200°C does not account for such a dramatic reduction of the impurities as demonstrated by SIMS measurements within the bulk Si of contaminated samples oxidized at 1000°C. The addition of oxygen to HCl/Ar mixtures had no impact on the removal of Cu from the silicon surface as determined by SIMS measurements. Also, varying the HCl concentration from 50% to 1% in argon had little effect on the removal of Cu as determined within the limits of SIMS measurements.

In summary, SIMS data indicated that both the wet and afterglow cleaning processes discussed above can remove the metallic impurities Fe and Cu from the Si surface to levels below detection by the SIMS tool. Thus, within the detection limit of SIMS, the described mode of dry cleaning is as effective as wet cleaning in removing the gross level of intentional contamination from the silicon surface. Further electrical characterization of these samples was used to determine if the cleaning processes were adequately removing these artificially large amounts of metallic impurity to levels acceptable for microelectronic device fabrication. Nonuniform etching of the Si surface during remote HCl/Ar plasma cleaning was found to influence these measurements.

Etching of Silicon in HCl/Ar Afterglow Mixtures

It was found that the presence of chemical oxide on the Si surface reduces the Si etch rate and can influence the formation of surface roughness. Efforts were made to control and minimize the amount of chemical oxide formed on the sample surfaces prior to treatment in the afterglow system by means of a wet etch in $1HF:20H_2O$ followed by a deionized water rinse and nitrogen drying sequence. Both the rinse time, which influences fluorine coverage of the substrate, as well as the exposure time to room air are known to affect the formation of chemical oxide [3]. Varying the rinse time from 30 seconds to 60 seconds caused the Si etch rate at 400°C to decrease by as much as 40 percent. Such results demonstrate how changes in Si surface chemistry can dramatically affect low temperature gas-phase etching reactions.

Silicon etching in an afterglow of 10%HCl/Ar at a substrate temperature of 200°C is presented in Fig. 5. A measure of the silicon consumed versus time of etching following a 30 second water rinse and nitrogen dry is presented. The etching reaction appears to be self limiting for longer etch times. Non-uniform etching under these conditions manifested itself in the form of etch pits on the Si surface which were observable by dark field imaging.

The etch rate of thermal SiO_2 under the process conditions discussed above was found to be negligible. No removal of thermally grown field oxide was detected on substrates exposed to 10%HCl/Ar afterglow at 200°C and 1 torr for times ranging from 1 to 8 minutes. Change in oxide thickness is negligibly small indicating that the radical gas species within the afterglow are not capable of SiO_2 etching under the given processing conditions. These results also imply that no measurable re-deposition of reactor chamber material is taking place. The measured values of refractive index of these same oxide films were also unchanged by the process.

Formation of Surface Roughness

Despite the encouraging results of SIMS analysis of afterglow cleaned samples, side effects associated with afterglow processing in HCl/Ar mixtures, specifically roughening of the silicon surface, resulted in a degradation of some of the electrical properties of the subsequently formed SiO_2-Si structures. Effects of afterglow processing performed on non-contaminated (control with dry cleanup) samples was investigated in order to develop a more controllable etching process. A discussion of these studies is given in the following section.

Defect Delineation. Defect studies of afterglow treated samples were carried out in order to more closely examine the physical condition of the silicon surface following afterglow processing and to correlate findings with the results of electrical measurements performed in this study. Yang etch [4] was performed on the wafers after thermal oxidation and thermal oxide etch with buffered HF solution. Etch pits generated by non-uniform afterglow etching with HCl/Ar were delineated and enlarged by the preferential etch. The formation of etch pits was found to be dependent upon the condition of the silicon surface prior to the afterglow process. This nonuniform etching lead to the formation of silicon surface roughness which resulted in the reduction of breakdown voltage of thermal oxides grown on these surfaces. The effect of the Si surface conditions, specifically the inhomogeneous coverage of the silicon surface with ultrathin native oxide, was found to influence the etch rate and the formation of etch pits.

The density of etch pits has a strong dependence on the initial substrate temperature. Using dark field imaging, the etch pit density could be evaluated. The density of etch pits increases drastically as the substrate temperature is increased above 200°C for applications of the HCl/Ar afterglow treatment. For 5 minute etches in 10%HCl/Ar, the densities generated at 300°C and 400°C were found to be 20 and 35 times greater than the 200°C case. No etch pits were detected on the control samples which were not exposed to afterglow treatment prior to thermal oxidation. Even at 200°C the density of etch pits was unacceptable from a device point of view and modifications to the process time were necessary in order to improve control of the etching.

Impact on Oxide Breakdown Field. Following the afterglow treatment, samples were thermally oxidized at 1000°C in O_2 forming oxides in the range of 20 nm to 25 nm in thickness. Aluminum evaporation was used to form MOS capacitors with an electrode area of 7.85×10^{-3} cm^2 for use in taking oxide breakdown voltage measurements. As was stated earlier in the discussion, oxide breakdown voltage is known to be sensitive to surface roughness [5], in this case that which is formed during pre-oxidation cleaning. The ramp-voltage technique was used to measure oxide breakdown voltage.

Distributions of breakdown events for oxides grown on substrates processed under various conditions were compared to study the electrical consequences of the etching treatments. Samples were treated with various concentrations of HCl in the gas mix for 30 seconds at three different temperatures. Afterglow treatments at a substrate temperature of 200°C and HCl concentrations of 10% or less tended to not have a detrimental effect on the characteristics of the subsequently grown thermal oxides. Fifty percent cumulative failure of

capacitors formed on these samples occurred at fields of 10 MV/cm or greater which were comparable to the control samples, i.e. those not exposed prior to thermal oxidation to the HCl/Ar afterglow. At processing temperatures of 300°C and 400°C, the oxide breakdown field characteristics are degraded. At both temperatures, 50% cumulative failure of capacitors tested occurred at applied fields of 5 MV/cm or less. Other workers have observed similar results and have demonstrated that they are produced by surface roughness which affects both the growth of the thin oxide film and the local enhancement of electric field across the dielectric [6].

The non-uniform etching of the surface tended to be more prevalent at temperatures greater than 200°C, HCl concentrations in excess of 10%, and for treatment times greater than 30 seconds. For processes operating beyond these conditions, the presence of a thin oxide film formed in as little as 30 seconds in an O_2 afterglow inhibited non-uniform etching resulting in dramatic improvements in the oxide breakdown voltages. Thin oxide films were reported to not inhibit the formation of metal-chloride species during UV/Cl_2 treatments of silicon surfaces [7].

Direct measure of surface roughness produced by HCl/Ar afterglow exposure was made using a surface profilometer and by light scattering observations. Surface roughness was evaluated for samples exposed to 10%HCl/90%Ar afterglow at 400°C for times of 30 and 300 seconds and compared to non-etched control samples. After 300 seconds exposure, the sample surface is very rough as compared to the undamaged control sample indicating that Si etching under these conditions is very non-uniform. The surfaces appeared very hazy and exhibited a maximum value of peak-to-peak roughness of 1150 angstroms. Even after 30 seconds at this temperature, damage is evident in the form of haze observed through light scattering measurements and in the occurrence of etch pits on the surface observed using dark field microscopy. The increase in roughness with time of exposure correlated with the degradation of dielectric breakdown characteristics as a function of treatment time for thermal oxides grown on these surfaces. Limiting the etch time is seen as one means of controlling roughness, although substrate temperature and surface conditions very strongly influence Si etching in this mode.

B. Oxygen Afterglow Surface Treatments

The use of an O_2 afterglow to remove organics inherently leaves the Si surface passivated with an oxide layer. Afterglow oxidation studies at temperatures and times of interest in the application of dry wafer cleaning are presented in Fig. 6. This type of treatment serves to remove photoresist and organic residues as well as to passivate the

etched silicon surface and may ultimately be used to form gate oxide on the Si immediately following the clean up step [8].

Photoresist stripping is a film removal step which can be integrated into an overall dry wafer cleaning technology and can be applied prior to pre-oxidation cleaning within the same reactor. The photoresist strip rate in an oxygen afterglow within the wafer processor used in these studies was found to be 650 nm/min which is comparable to other commercially available afterglow systems.

C. Oxide Etching

Hydrogen was added to mixtures of NF_3/Ar to achieve selective etching of SiO_2 over Si. The SiO_2 etch rate is presented as a function of the NF_3:H_2 ratio in the gas mixture in Fig. 7. A constant flow of 20 sccm of NF_3 was maintained as the concentration of H_2 was varied, which resulted in only a slight change in overall pressure of the process. Once again a process pressure of 1 torr was maintained using a treatment time of 30 seconds. No SiO_2 etching was observed for H_2 flow rates of 100 sccm or greater indicating that an abundance of hydrogen in the afterglow quenches the etching process. Oxide etching was observed as the H_2 concentration was reduced. A linear dependence on the NF_3:H_2 ratio occurs between the values of 0.5 and 2.0. As the hydrogen concentration is decreased still further, the afterglow behaves more like the NF_3/Ar case with the etch rate leveling off to a constant value. No SiO_2 etching was observed using an unexcited gas mixture with NF_3:H_2 equal to one.

Silicon etching in NF_3/H_2 afterglow was evaluated for gas concentration ratios of 0.1 to 1.0 resulting in etch rates as high as 48 nm/min for the 1:1 case. No Si etching was observed at ratios of 0.5 or below, which is similar to the oxide etching results. When the hydrogen ratio is brought down to an equal level with NF_3 an abrupt activation of silicon etching is observed. This is further indication that hydrogen is quenching the etching process.

The Si etch rate decreases due to the scavenging of fluorine by the hydrogen resulting in the formation of HF. Further increases in hydrogen concentration eventually limit the oxide etching rate as well. Plasma discharges of NF_3/Ar will contain the species NF_x and F_x where x=1,2, or 3. The species will exist in both the ionized state and the radical state. After recombination, the afterglow will contain primarily radical (excited) species and some ions. Fluorine radicals are responsible for etching both the silicon and silicon dioxide. Fluorine gas reacts with SiO_2 to form volatile SiF_4 while the liberation of SiF_2 is expected to dominate at the silicon surface [9]. The addition of hydrogen to the discharge allows for the formation of HF in the plasma as well as in the afterglow during recombination. The

reaction between SiO_2 and HF gas is very sensitive to moisture and in the absence of water vapor the oxide etching will be inhibited [10]. The selectivity of the etch process was thus found to be very high at the NF_3:H_2 ratio of 0.5. The oxide etch rate is in the range of 2 to 2.5 nm/min for these conditions which is adequate for the removal of native oxide.

D. Overall Cleaning Process

A complete dry cleanup procedure was developed based on the integration of individual processing methods described above [1]. The individual steps were combined into a sequence designed to optimize the cleaning action while being compatible with the other processing steps. Details of the processes involved and the sequence in which they are applied are outlined in Table I. This cleaning process was used to prepare the Si surface for thermal oxidation and was applied in-situ immediately following photoresist stripping in O_2 afterglow.

Electrical characterization of MOS capacitors were used to evaluate the proposed cleaning scheme using the process flow outlined in Fig. 2. A direct comparison of the results with those obtained using a wet resist strip/standard RCA clean is made in each case. Vacuum annealing at 750°C, step 6 in the sequence (Table I), was added to assist in volatilizing any metal complexes remaining on the sample surface after a HCl/Ar afterglow treatment and a subsequent oxide etching step.

The resulting electrical characteristics of MOS capacitors formed on dry and wet cleaned surfaces are summarized in Table II. Also included in the comparison is data from capacitors formed on the existing field oxide. The results show that the dry cleaning sequence is comparable to the standard wet clean processing. A more detailed explanation follows.

The distribution of interface trap density, D_{it}, for dry and wet cleaned samples prepared during this investigation are comparable and are centered in the low 1E+10 range. The average value of D_{it} for the dry clean was 2.1E+10 $cm^{-2}eV^{-1}$ which was slightly higher than that of the wet clean.

Distributions of minority carrier lifetime for wet and dry cleaned samples were obtained from C-t measurements. The shape of the C-t response indicated that the generation rate is dominated by bulk effects and not interface effects following the dry clean. Zerbst analysis of these measurements indicated that the minority carrier generation lifetime varied from 244 μsec to values greater than 400 μsec in the dry processed silicon. Results were comparable for the two cleaning modes, the average value of the dry clean being slightly lower than the wet clean (Table II). These results are very encouraging, indicating that the bulk Si and the

interface are free from process induced defects and deep level impurities.

Median values of oxide breakdown field of MOS capacitors formed on dry and wet cleaned samples are both greater than 10 MV/cm (Table II). More complete breakdown statistics for these samples are presented in the form of histograms in Fig. 8. Low field breakdown events which are observed in both cases and are comparable in distribution are attributed to particle contamination associated with wafer handling. Under applied breakdown fields characteristic of the intrinsic dielectric strength of SiO_2, the dry cleanup produces a tighter distribution of oxide breakdown field than does the wet cleanup.

Further characterization of the oxide properties included TDDB and Charge-to-Breakdown measurements. The results of TDDB measurements, performed using a stress field of 10.5 MV/cm, are presented in Fig. 9 and the times at which 50% cumulative failure occur are listed in Table II. Charge-to-Breakdown, QBD, analysis was performed using an injected current of 1.27E-4 amp/cm^2 and average values are listed in Table II. These results further indicate that the integrity of the subsequently formed oxide and interface of the dry cleaned samples is comparable to that of the wet cleaned samples.

The presence of metallic impurities on the wet and dry cleaned samples was evaluated using Neutron Activation Analysis and compared to results of control samples which did not undergo photolithography. The oxide films, silicon surface region and the silicon bulk were analyzed for trace metal impurities. In general, the levels of impurity tended to be comparable between the three sample types indicating that both cleans are effective in removing impurities introduced by the photoresist. A comparison of copper and gold in the oxide layers is presented in Fig. 10 showing that both impurities are present after processing and that the dry clean is more effective in removing Cu than gold. Mobile ion content within the samples was determined from flat-band voltage shifts of C-V data following bias temperature stress of the oxide. The mobile ion densities within the dry and wet cleaned samples were comparable.

SUMMARY AND CONCLUSIONS

Afterglow treatments using HCl/Ar gas mixtures have been demonstrated to be effective in removing Fe and Cu contaminants from the Si surface. Clear differences between cleaned and uncleaned samples demonstrated that conditions are sufficient for gas phase transport of metal chloride species from the Si surface. The formation and volatilization of metal-chloride species occurs simultaneously with the etching of the Si surface. Such etching processes were found to be

non-uniform if residual oxide was left on the surface.

Oxygen afterglow treatments are capable of photoresist stripping from patterned wafers following lithography and wet etching of field oxide in HF solution. Photoresist strip rates of 650 nm/min were attained using this approach at substrate temperatures of 200°C. This resist stripping process leaves the exposed Si surface passivated with oxygen. Thin oxide films inhibit etching of Si in HCl/Ar afterglow ambient.

The removal of thin oxide layers is a necessary part of an overall wafer cleaning process. Afterglow mixtures of $NF_3/H_2/Ar$ have shown promise as a means of selectively removing oxide films which passivate the Si surface and trap impurities. Thermal oxide etch rates of 2.5 nm/min were achieved using $1\%NF_3/2\%H_2$ mixtures.

The remote plasma processes described above can be applied individually or in combination with each other to accomplish the task of removing organic and metallic impurities as well as native/chemical oxide from the Si surface. An improvement in the reliability of SiO_2 films grown on remote plasma cleaned Si surfaces was observed by means of TDDB measurements under the conditions of constant voltage stress and constant current stress. Overall, the remote plasma wafer cleaning process, which produces results that are comparable to those obtained using standard wet cleans, shows promise in future cleaning applications.

ACKNOWLEDGEMENTS

The support obtained from Texas Instruments, Inc., throughout this investigation is acknowledged.

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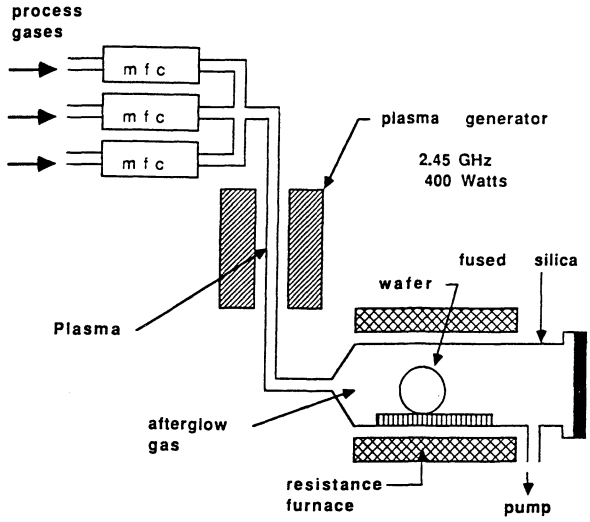

Fig. 1. Remote plasma reactor configuration.

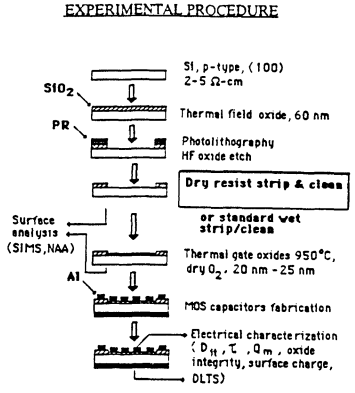

Fig. 2. Outline of the basic experimental process flow.

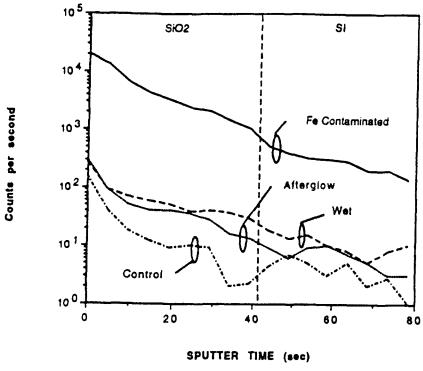

Fig. 3. SIMS depth profile of iron in oxidized silicon wafers comparing the wet and dry cleaning process.

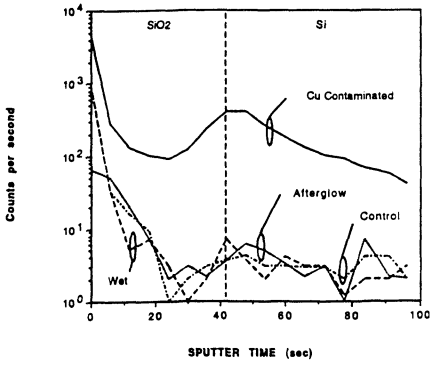

Fig. 4. SIMS depth profile of copper in oxidized silicon wafers comparing the wet and dry cleaning process.

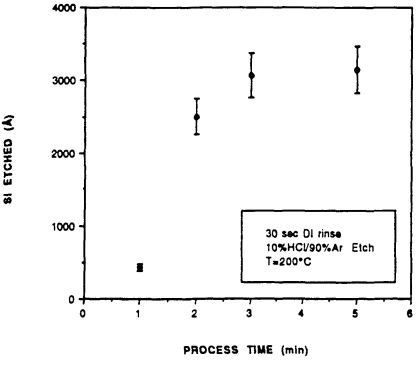

Fig. 5. Characteristics of silicon etching in HCl/Ar afterglow.

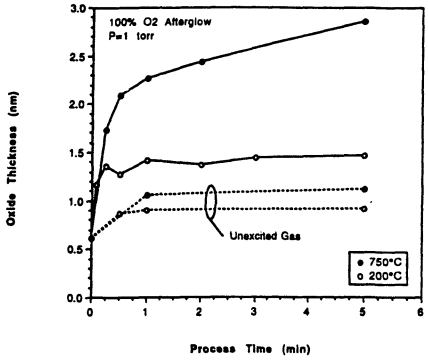

Fig. 6. Results of afterglow oxidation studies.

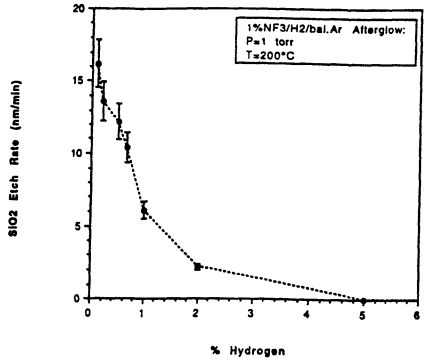

Fig. 7. Characteristics of silicon dioxide etching in mixtures of NF3 and H2.

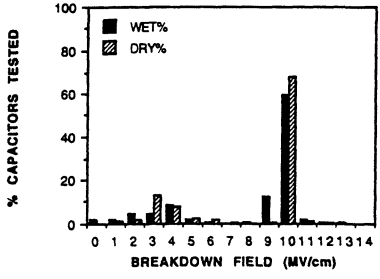

Fig. 8. Oxide breakdown histogram comparing films grown on wet and dry processed surfaces.

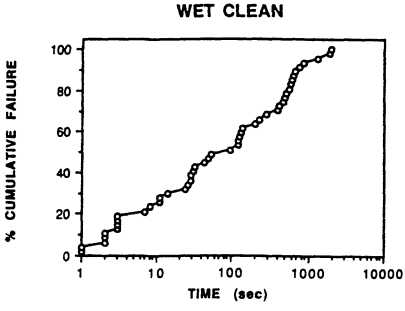

Fig. 9a. TDDB distribution for oxide film grown on wet processed surface.

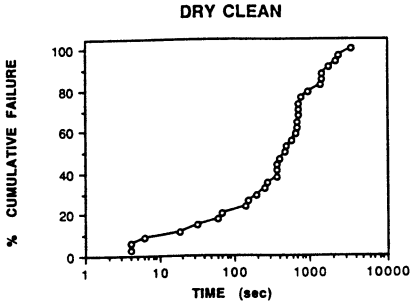

Fig. 9b. TDDB distribution for oxide film grown on dry processed surface.

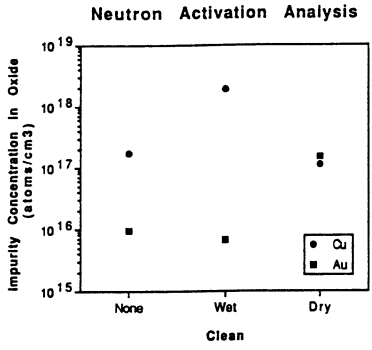

Fig. 10. Comparison of concentrations of copper and gold in oxide films for wet and dry processed samples as measured using NAA.

TABLE I.

PROPOSED DRY CLEANING PROCEDURE

STEP	Gas comp.	T (°C)	p (Torr)	Etch rate (nm/min)	Process time (sec)
1. Resist strip (1000 nm)	O_2	200	1	650	120
2. Residual oxide (1.4 nm) etch	NF_3 1% H_2 2% Ar 97%	200	1	2.5	40
3. Fine organics removal/oxide regrowth (1.3 nm)	O_2	200	1	—	30
4. Metal complexing	HCl 10% Ar 90%	200	1	Si etch 30 nm	30
5. Residual oxide etch/partial volatilization of metal compounds	NF_3 1% H_2 2% Ar 97%	200	1	2.5	40
	Temperature ramp				a)
6. Final volatilization of metal compounds	vacuum anneal	750	0.02	—	120
7. Protective oxide regrowth (2 nm)	O_2	750	1	—	25

a) TIME OF TEMPERATURE RAMP DEPENDS ON HEATING ELEMENTS USED

TABLE II.
SUMMARY OF ELECTRICAL CHARACTERIZATION

	MOS CAPACITORS						
	Interface trap density, D_{it}, $\times 10^{10} eV^{-1} cm^{-2}$		Carrier lifetime τ, μsec.	Median oxide breakdown field, MV/cm		TDDB (median) at 10.5 MV/cm, sec	Charge to breakdown, $\times 10^{-4}$ C
	Gate	Field	Gate	Gate	Field	Gate	Gate
WET CLEAN	1.4	1.0	400	10.1	8.8	137	1.95
DRY CLEAN	2.1	1.52	387	10.4	8.7	485	2.65

UV-EXCITED DRY CLEANING OF SILICON SURFACES CONTAMINATED WITH IRON AND ALUMINUM

Rinshi Sugino, Masaki Okuno, Mayumi Shigeno, Yasuhisa Sato,
Akira Ohsawa, and Takashi Ito
Fujitsu Laboratories Ltd.,
10-1 Morinosato-Wakamiya, Atsugi 243-01, Japan

Yoshiko Okui
Fujitsu Limited,
1015 Kamikodanaka, Nakahara-ku, Kawasaki 211, Japan

UV-excited dry cleaning using photoexcited chlorine radicals reduces iron and aluminum contamination on a silicon surface. The iron and aluminum contaminants used had a surface concentration of 10^{13} atoms/cm^2. These contaminant atoms were intentionally introduced via an ammonium solution. The silicon etching rates from the UV-excited dry cleaning differed greatly with iron and aluminum contaminants. Both iron and aluminum on the silicon surface were completely removed by UV-excited dry cleaning at a cleaning temperature of 170℃. Furthermore both iron and aluminum concentrations on the silicon surface were decreased two orders of magnitude when the surface was etched only 2 nm deep.

INTRODUCTION

In VLSI/ULSI production, to achieve a high degree of wafer surface cleanliness it is essential to use dry cleaning rather than a conventional wet process. It is well known that dry cleaning has some advantages over the conventional wet process.[1)]

The authors recently reported that UV-excited dry cleaning of silicon with photo-excited chlorine radicals reduces residual metals such as Fe, Ca, Na, and Mg surface contamination after wet cleaning.[2)] More recently, UV-excited dry cleaning has decreased n^+p junction leakage currents.[3)]

This paper describes a mechanism and method of UV-excited dry cleaning which lightly etched an intentionally-contaminated silicon substrate. Iron and aluminum contaminants were used with a surface concentration of 10^{13} atoms/cm^2. On the basis of these results, we present an effective UV-excited dry cleaning technique for iron and aluminum contamination.

EXPERIMENT

Four-inch boron doped p-type silicon wafers with a resistivity between 9 and 11 Ωcm and (100)-oriented surfaces were used in the experiments. The silicon wafers were first cleaned with an NH_4OH-H_2O_2-H_2O solution, HNO_3, and deionized water. The silicon surface thus obtained was used as the reference for each evaluation. After this wet cleaning step, the wafer surfaces were contaminated by immersion in an ammonium solution (NH_4OH-H_2O_2-H_2O) containing either iron or aluminum. Contaminated wafers were then continuously rinsed with deionized water, then dried by heating in a nitrogen atmosphere. The wafer contamination process is shown in Table 1.

Iron and aluminum concentrations on the silicon surfaces were measured by flameless atomic absorption spectrophotometry (AAS) using an HF-running dissolution method. Iron concentration in the contaminated ammonium solution was 50 ppb. The surface iron concentration of a wafer treated in the ammonium solution was $0.5\text{-}1.3\text{x}10^{13}$ atoms/cm^2. The iron-contaminated silicon wafer was used for both AAS and X-ray photoelectron spectroscopy (XPS) measurements. For AAS measurements aluminum concentration in the ammonium solution was 2 ppb, and the wafer surface concentration after the treatment was $0.7\text{-}0.8\text{x}10^{13}$ atoms/cm^2. For XPS measurements aluminum concentration in the ammonium solution was 54 ppb, and the wafer surface concentration after the treatment was $1.5\text{x}10^{14}$ atoms/cm^2.

The UV-excited dry cleaning equipment consisted of a quartz chamber, a halogen lamp to heat the wafer, and a microwave-excited UV mercury lamp. The UV intensity of wavelengths from 200 to 300 nm was 22 mW/cm^2. High-purity chlorine at a pressure of 2.7 kPa was used as the cleaning gas.

RESULTS AND DISCUSSION

Contamination model of iron and aluminum

Iron $2p_{3/2}$ spectra measured by XPS for the iron-contaminated silicon surface and the reference as comparison are shown in Fig. 1. Contaminant iron atoms were expected to be bonded with oxygen atoms. This conclusion is drawn from the iron peak at 711 eV, which is shifted to the high energy side by 5 eV compared to the ordinary metallic iron peak is at 706 eV.[4] Iron contaminants existed as hydroxides (Fe-OH for example) on the silicon surface. Iron hydroxides are involved in the native oxide of silicon.

Figure 2 shows aluminum 2p spectra measured by XPS. The 2p peak of aluminum is at 74.3 eV, also shifted to the high-energy side. The peak shift is about 2 eV from ordinary metallic aluminum and is a result of aluminum and oxygen bonding.[3] Here also, we think that contaminant aluminum atoms were in the form of hydroxyl groups such as $Al(OH)_3$.

The native oxide structure of silicon contaminated with iron and aluminum was evaluated by multireflection of attenuated total reflection (ATR) method in infrared region.[5,6] As shown in Fig. 3, around a 2100 cm^{-1} absorbance peak derived from the presence of SiH_2 is observed for the aluminum-contaminated silicon; whereas, the absorbance peak is not observed for the iron-contaminated silicon. It is thought that the iron and aluminum contaminants existed as hydroxides on silicon surfaces where more amount of SiH_2 species are contained in the aluminum-contaminated silicon. The difference is thought to be attributed to H_2O_2 decomposition enhanced by the presence of iron in the ammonium solution.

From these XPS and ATR measurements, we can derive the model of surface structure with native oxides of silicon contaminated with iron and aluminum as schematically shown in Fig. 4.

Etching for contaminated silicon surfaces

The etching reaction of silicon and chlorine radical takes place through the native oxide.[7] It can be thought that the etching characteristics are affected by the native oxide structure, and the amount of the SiH_2 species in the native oxide of silicon determines the etching rate.

The etching rate of the contaminated silicon was increased with an increase in etching temperature. Figure 5 shows etching depth versus UV irradiation time at 170℃ and 140℃ for iron-contaminated silicon. At 140℃, there is a delay before etching begins. The etching rate at 170℃ was higher than at 140℃.

The etching rate of aluminum-contaminated silicon was different from the etching rate of iron-contaminated silicon. Figure 6 shows the etching depth versus UV irradiation time at 170℃ and 140℃ for aluminum-contaminated silicon. At 140℃, the silicon etching rate was constant with no delay at the beginning. The silicon surface was etched 20 nm without UV irradiation while heating at 170℃.

The measured etching rates of silicon differed greatly depending on the contaminants. For a given temperature, the etching rate of silicon contaminated with aluminum was higher than that of silicon with iron contamination. It is conceivable that the SiH_2 species in the native oxide influences the etching reaction of the silicon substrate.

UV-excited dry cleaning for contaminated silicon

Figure 7 shows the iron concentration on the silicon surface after UV-excited dry cleaning. The surface concentration of iron decreased by silicon etching and is temperature dependent. At 140℃, the iron concentration decreased only one order of magnitude from the initial level. At 170℃ the surface concentration of iron decreased two orders of magnitude from the initial contaminant concentration, below the limit of detection by AAS.

Figure 8 shows the aluminum concentration on the silicon surface after UV-excited

dry cleaning. At 140℃, the aluminum concentration decreased by cleaning by less than one order of magnitude, even after etching to a depth of 40 nm. At 170℃ and at a 20-nm or more etching depth, the aluminum concentration was below the limit of detection.

Both iron and aluminum contaminants with the surface concentration of 10^{13} atoms/cm^2 were completely decontaminated by using UV-excited dry cleaning and a cleaning temperature as high as 170℃.

Combining the contamination model in Fig. 4 and these experimental results, we can consider the dry cleaning model as follows: chlorine radicals penetrate the native oxide and attack metal hydroxides of contaminants followed by vaporization of metal chlorides.

Effective cleaning using lower etching rate

The preceding results suggest that removal of iron or aluminum from a silicon surface requires a high cleaning temperature rather than deeply etching depth. However, we could not control thin region etching of less than 20 nm with aluminum-contaminated silicon at high temperatures. This problem was solved by decreasing the etching rate by using a lower chlorine pressure than the previous 2.7 kPa.

At 170℃ and a chlorine pressure of 0.95 kPa, the iron concentration on the silicon surface was decreased by two orders of magnitude from the initial level, below the limit of detection by AAS. The surface was etched only 2 nm after 30 seconds of UV irradiation.

At 170℃ and a chlorine pressure of 0.27 kPa, the aluminum concentration of the silicon surface was also below the limit of detection. The surface was etched only 2 nm deep after 30 seconds of UV irradiation.

CONCLUSIONS

We investigated a mechanism and method of UV-excited dry cleaning which lightly etched an intentionally contaminated silicon substrate. The iron and aluminum contaminants used had a surface concentration of 10^{13} atoms/cm^2. These contaminant atoms were found to be bonded with the oxygen atoms. The silicon etching rates from the UV-excited dry cleaning differed greatly between iron and aluminum contaminants. Both iron and aluminum on the silicon surfaces were completely removed by UV-excited dry cleaning at a cleaning temperature of 170℃. Both iron and aluminum concentrations on the silicon surface were below the limit of detection by AAS when the surface was etched only 2 nm deep.

ACKNOWLEDGEMENT

The authors thank Dr. S. Watanabe for the ATR measurements and his helpful suggestions.

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Table 1 Preparation of contaminated silicon wafers by iron and aluminum

Sample
p-Si (100), 4 inch, CZ, 10 Ω-cm

Pre-cleaning (reference)

NH_4OH-H_2O_2-H_2O (1:1.5:4)		10 min
HNO_3	hot	5 min
H_2O	boil	5 min

Al and Fe contamination

HF 3%		15 s
Al: 2, 54 ppb Fe: 50 ppb	in NH_4OH-H_2O_2-H_2O (1:1.5:4)	5 min

After each treatment: H_2O rinse, 10 min

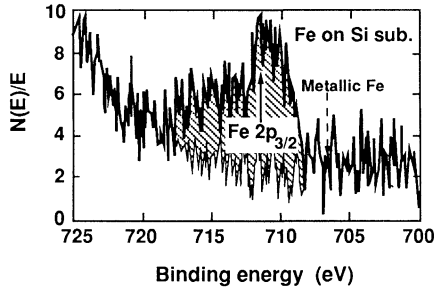

Fig. 1 XPS spectra of an iron $2p_{3/2}$ region on the silicon surface with iron contaminants and the reference for comparision.
The surface concentration of iron was 1.3×10^{13}atoms/cm^2.

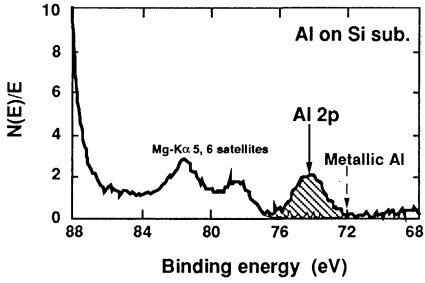

Fig. 2 XPS spectra of an aluminum 2p region on the silicon surface with aluminum contaminants and the reference for comparision.
The surface concentration of iron was 1.5×10^{14} atoms/cm^2.

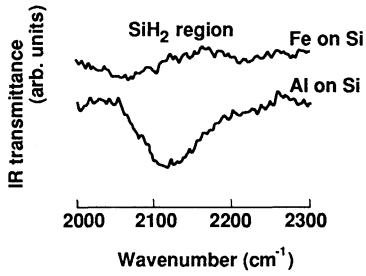

Fig. 3 Infrared spectrum by attenuated total refrection of the contaminated silicon. The absorbance peak around 2100 cm^{-1} was assigned as SiH_2.

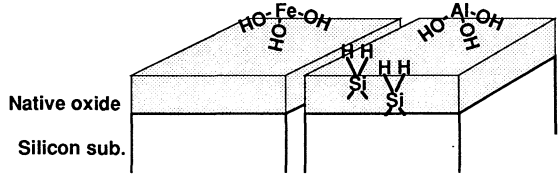

Fig. 4 A scheme of the silicon surfaces contaminated with iron and aluminum.

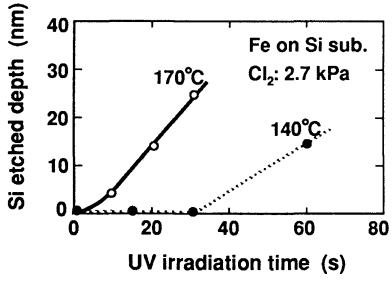

Fig. 5 Etched depth of silicon with iron contaminants versus UV irradiation time.

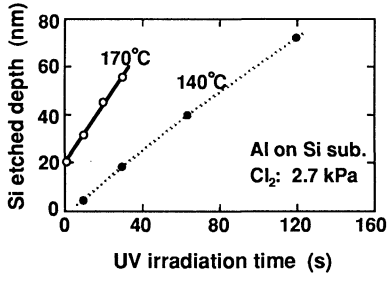

Fig. 6 Etched depth of silicon with aluminum contaminants versus UV irradiation time.

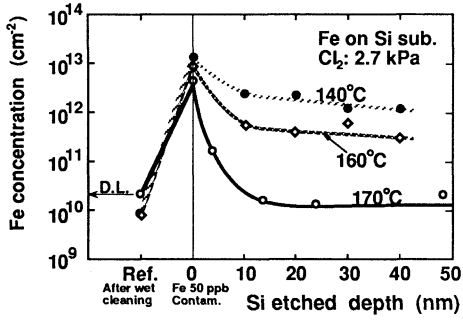

Fig. 7 Iron concentration on the silicon surface before and after UV-excited dry cleaning.

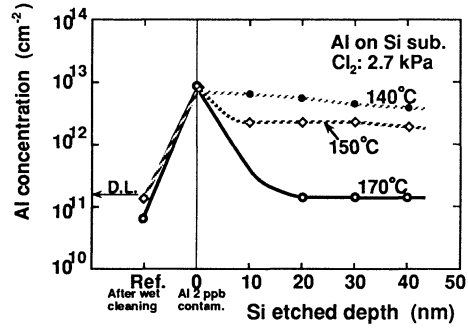

Fig. 8 Aluminum concentration on the silicon surface before and after UV-excited dry cleaning.

UV/FLUORINE ETCHING OF NATIVE SILICON OXIDES

Kevin Torek and Jerzy Ruzyllo

Center for Electronic Materials and Processing
The Pennsylvania State University
University Park, PA 16802

The feasibility of UV enhanced etching of grown and deposited silicon oxides, including the silicon native/chemical oxide, using NF_3 at atmospheric pressure is examined. Etching is evaluated by ellipsometry and contact resistance measurements. No etching takes place with UV radiation off. With UV light, oxide etch rates ranging from 0 to 120 Å/minute are obtained for the oxides studied, depending on the type of oxide and gas mixture. BPSG etches faster than the other oxides, while thermal oxides do not etch. The effects of adding hydrogen or moisture to the gas mixture are also explored. Hydrogen added to a 10 vol. % NF_3 in Ar gas mixture alleviates silicon surface pitting while at the same time decreasing the BPSG etch rate. Moisture addition on the other hand, accelerates etching. The current-voltage characteristics of ohmic Al contacts on UV/NF_3:H_2:Ar treated p-type silicon were studied to evaluate etching of native/chemical oxide. The contact resistances obtained were the same as those for HF:H_2O etched surfaces.

INTRODUCTION

During silicon surface treatments prior to operations such as contact deposition, epitaxy, and gate oxidation, there is a need to etch native/chemical oxide in order to expose the bare silicon surface. Also, native oxide may contain lifetime decreasing metals which it would be advantageous to remove along with the oxide itself [1]. Integration with subsequent steps requires that this etch be accomplished in the gas phase. The native/chemical oxide etch should be selective with respect to other oxides typically present on the wafer surface, such as thermal, CVD, and BPSG.

Techniques considered for etching of native/chemical oxide off the silicon surface include water solution HF treatment, low-energy ion sputtering, H_2 reduction, remote plasma H_2, and vapor HF etching. The current issues in native oxide etching include etch rate, temperature, surface damage, and etch selectivity.

Among the various techniques suitable for process integration vapor HF etching is considered at present the most often [2-4]. An in-situ rinse following the vapor etch has been shown to remove from silicon surface trace metals [3] and other residues which the vapor etch alone leaves behind.

The purpose of this experiment is to evaluate the effectiveness of atmospheric pressure UV enhanced NF_3 etching of native/chemical silicon oxide from the silicon surface. The UV absorption spectrum of NF_3 has a broad band below about 200 nm with the absorption coefficient increasing monotonically for shorter wavelengths. The absorption cross section of NF_3 at 184.9 μm is approximately 0.1 - 0.5 x $10^{-20}cm^{-2}$ [5,6]. Chemistries similar to the one used in this experiment were used previously with promising results in excimer laser [7], and remote plasma enhanced processes [8].

EXPERIMENTAL

In this experiment the UV source was a conventional low pressure mercury vapor lamp with 10 mw/cm^2 power to the sample at the shortest wavelength of 184.9 nm. Process variables included NF_3 concentration, temperature, and the addition of hydrogen or moisture to the NF_3/Ar gas mixture. The gas ratios were maintained in the nonexplosive range [9]. Etching was performed under atmospheric pressure. To evaluate the selectivity of the UV/NF_3 etching technique, etch rates were determined for various oxides of interest in silicon device technology, namely, dry and wet thermal, CVD, sputtered, native/chemical, BPSG, and spin-on-glass. Oxide film thickness was measured using ellipsometry. To determine etch rates, oxides were typically etched for 30 minutes to achieve significant changes in the oxide thickness. Etch times between 30 seconds and 10 minutes were used during native oxide etch back experiments. Native oxide etch rates were derived from the portion of the (linear) thickness vs. etch time curve for which the native oxide thickness is above the detection limit of the ellipsometer (about 10Å).

For the case of native/chemical oxide etching, in which case the 20Å starting oxide thickness was prepared by boiling wafers in DI water, contact resistance measurements were used in addition to ellipsometry as a gauge of oxide thickness changes. For this purpose, Al was evaporated onto both front and back wafer surfaces and vertical two terminal I-V characteristics were measured. Contacts on HF dip etched and deionized water rinsed, as well as unetched silicon served as references.

RESULTS AND DISCUSSION

Under the process conditions applied in this study, no oxide etching was taking place without UV irradiation. This confirms that UV light is breaking the N-F bond and producing free fluorine essential in oxide etching. With UV irradiation, etching was observed, with etch rates varying significantly for various oxides. For all etching experiments without intentional moisture addition, changing the wafer temperature from room temperature to 150°C had negligible impact on the etch rate. This is an indication that the rate-limiting reaction in this etching mode is the photolysis of NF_3 rather than substrate temperature.

The results of the etch study using various concentrations of NF_3 in argon are summarized in Fig. 1 and Fig. 2. In general, the etch rate was found to increase with increasing NF_3 content in the etching mixture. As seen in Fig. 1, the highest etch rate was recorded for BPSG with etch rates for other oxides under investigation being substantially lower. With the exception of spin-on-glass, SOG, for which etch rate of 15 Å/min was observed at 100% NF_3 (Fig. 1), these etch rates never exceeded 5 Å/min even at 100% NF_3 (Fig. 2). Within the resolution of the ellipsometer no etching was observed for thermal oxides for a 30 min., 100% NF_3 etch, and similarly negligible etching was also determined for CVD and sputtered oxides. This is an indication that selective etching can be accomplished using UV generated chemistries.

Fairly consistent changes in the etch rate with NF_3 concentration were observed for native/chemical oxides (Fig. 2). The etch rate of 4 Å/min was achieved at 100% NF_3. However, the etching of chemical oxides in 100% NF_3 results in pitting of silicon surface. The severity of this roughening increases with overetching and is therefore difficult to avoid for the thin chemical oxide. To circumvent this problem, the amount of NF_3 in argon was reduced to 10% and hydrogen was added to the NF_3/Ar mixture. This approach was successfully applied earlier in excimer laser [7] and remote plasma etching of silicon oxide [8]. The role of hydrogen in this case is to prevent excessive etching of silicon by scavenging fluorine [8]. At the same time, some reduction of oxide etch rates can be expected and in fact was observed in this study. The results of UV enhanced etching in 10% NF_3 in Ar with various amounts of hydrogen added are summarized in Fig. 3 and Fig. 4. The decrease of the oxide etch rate with the increase of hydrogen content in the etching mixture is the best seen in the case of BPSG (Fig. 3). This trend is much less clear in the case of other oxides, for which much slower etch rates were observed to begin with (Fig. 4). On the other hand, silicon surface pitting was not observed when hydrogen was added to the NF_3.

Because of the high reactivity of NF_3 with H_2, some formation of gaseous HF is expected in the etching ambient. Moisture has a marked effect on oxide etching in the presence of HF gas and is therefore expected to impact the etch rates. To evaluate the effect of moisture on the etching characteristics, a brief experiment was performed in which vapor was introduced by bubbling Ar gas through heated deionized water. Since the amount of water vapor added could not be accurately controlled, this experiment was meant only to provide initial, qualitative information on the possible effect of moisture addition to the etching mixture. The results shown in Fig. 5 indicate substantial increase of etch rates for all oxides studied. This increase most probably stems from the presence of gaseous HF. The addition of moisture may stimulate rapid reaction between HF and SiO_2.

In the reported study, difficulties were encountered when using the ellipsometer to determine exact changes in the thicknesses of very thin (< 10Å) native/chemical oxides. Consequently, additional information with regard to UV/NF_3 etching of such oxide was obtained through electrical characterization of aluminum contacts to UV/NF_3 etched silicon surfaces. Conclusions in this regard can be drawn here on the basis of the shape of the I-V characteristics obtained, as well as values of contact resistance. In this way, the effectiveness of the oxide etching method under investigation can be evaluated.

Ohmic contacts were formed by Al evaporation onto 7.6 Ω-cm boron doped silicon pretreated for 10 minutes with UV irradiation in NF_3:H_2:Ar ambient. Figure 6 shows the current-voltage characteristics of 1 mm dia. Al ohmic contacts, along with those of identical Al contacts on HF (1):H_2O (10) dipped and rinsed silicon, as well as unetched silicon, i.e. covered with ultra-thin chemical oxide prior to Al deposition. In each case, the I-V characteristics were measured following a 30 min. post-metal anneal at 400°C. The linear and symmetric I-V characteristics confirm the ellipsometric data indicating that the native/chemical oxide is removed by the UV enhanced process.

CONCLUSIONS

UV light from a low pressure mercury vapor lamp has been used to stimulate NF_3 etching of various oxides used in silicon device technology. The rate limiting step in the NF_3 chemistry studied appears to be photolysis of the precursor gas as the increase in the temperature of the reactor to 150°C had no effect on the etch rates. Moisture added to the gas mixture accelerates etching, while hydrogen has the opposite effect. A UV enhanced etch of native silicon oxide using 1% H_2 and 10% NF_3 in Ar prior to Al contact formation results in the same ohmic contact resistance as an HF dip etch.

UV enhanced etching of silicon oxides has potential applications either as part of an overall cleaning scheme or specifically for native/chemical oxide removal prior to additive processing steps such as contact metallization or epitaxial deposition.

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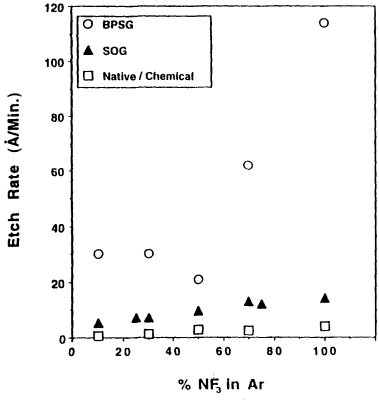

Fig. 1. Oxide Etch Rates vs. NF_3 Concentration.

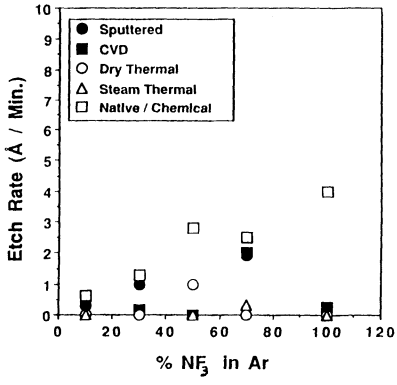

Fig. 2. Oxide Etch Rates vs. NF_3 Concentration.

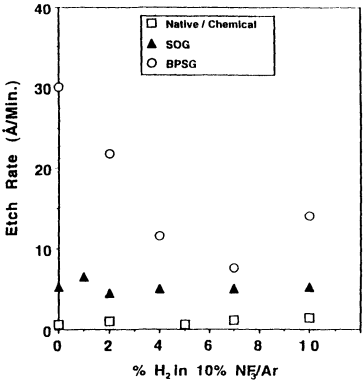

Fig. 3. Oxide Etch Rates vs. H_2 Concentration in 10% NF_3/Ar.

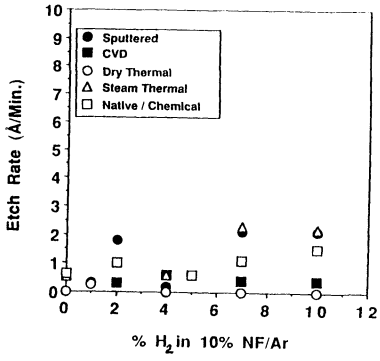

Fig. 4. Oxide Etch Rates vs. H_2 Concentration in 10% NF_3/Ar.

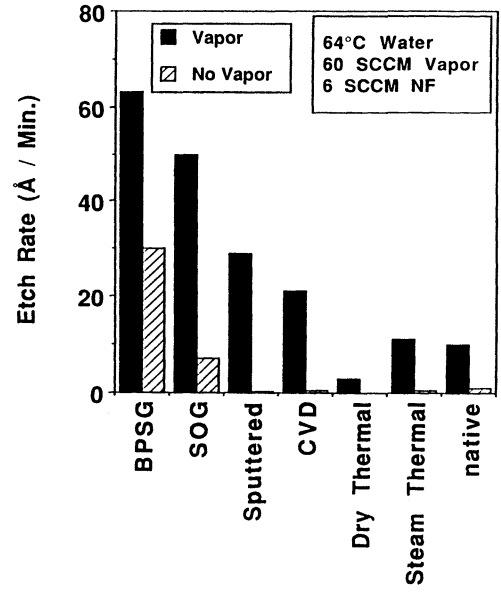

Fig. 5. Oxide Etch Rates With Vapor Added.

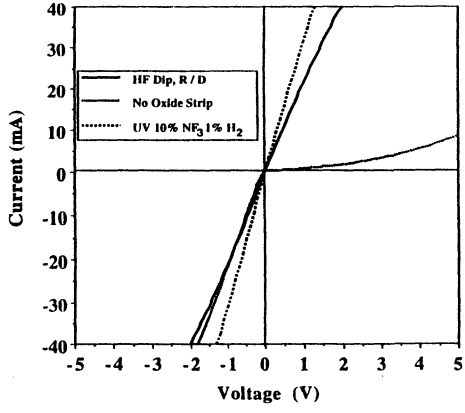

Fig. 6. I - V Characteristics of 1.00 mm dia. Al Contacts to p-Type Si Prepared Using Different Native Oxide Etches.

ELECTRON CYCLOTRON RESONANCE NF_3 PLASMA ETCHING OF SiO_2 AND CF_x POLYMER ON Si

B.-C. Chung, M. Delfino, W. Tsai, S. Salimian and D. Hodul
Varian Research Center
3075 Hansen Way
Palo Alto, CA 94304-1025

An electron cyclotron resonance (ECR) excited NF_3 plasma has been used to remove SiO_2 and CF_x polymer layers on Si substrates. In-situ analyses have been performed by utilizing diagnostic techniques such as plasma emission spectroscopy, mass spectroscopy and X-ray photoemission spectroscopy (XPS) to characterize the NF_3 cleaning. Etch rates of both layers have been obtained under different process conditions. Thermal SiO_2 etch rates with 3σ (± 3 standard deviations) values within 10% across a 150-mm Si wafer have been achieved with rf bias. Without rf bias, more uniform etch rates with 3σ values in the range of 4% have been routinely obtained. The polymer etch rates are a factor of 2 faster than those for SiO_2. Plasma emission spectroscopy used to monitor gaseous contamination indicates that oxygen is the major contamination species in the NF_3 cleaning process. In addition, results of actinometry measurements, which correlate the concentration of fluorinated species with process variables, imply that the oxide cleaning process is dominated by the fluorine atoms. In-situ XPS evaluation of <100> Si wafers exposed to the NF_3 plasma cleaning process indicates the presence of a thin $SiN_xO_yF_z$ residue on the surface.

INTRODUCTION

Cleaning of both silicon native oxide and CF_x polymer residue on a silicon surface is essential prior to epitaxial film growth or metal deposition during IC fabrication. Lately, dry cleaning techniques have acquired tremendous attention to fulfill this task

in ultra-large-scale integration (ULSI) applications where device dimensions in the submicron range need to be cleaned prior to sequential process steps; meanwhile, low particulate and damage levels generated in the process are required. Additionally, dry cleaning techniques can be used to the best advantage in cluster process systems where wafers can be cleaned in one process module and then transferred to another module under vacuum for the subsequent process.

Different dry cleaning techniques to remove silicon oxide or by-products of the IC process have been developed in the past few years. For instance, anhydrous HF has been used to remove native oxide from silicon wafers (1), UV-enhanced chlorine radicals have been employed to remove metallic contaminants (2), and UV-enhanced ozone has been applied to scavenge the organic molecules on the wafers (3). In addition, the cleaning of wafers by plasmas has been extensively studied using various gases, such as argon (4) and hydrogen (5) plasmas excited by electron cyclotron resonance (ECR). ECR microwave plasmas can provide high ion densities at low ion energies (6). Therefore, a dry cleaning process employing the ECR technique has recently attracted great attention in the ULSI process where low damage on the processed wafers is required. Lately, utilization of NF_3 plasmas to remove both SiO_2 and CF_x polymer has gained attention because of both the chemical and ion-enhanced reactions involved in this process (7-9).

This paper describes the application of ECR-excited reactive gas (NF_3) to remove SiO_2 and CF_x polymer, and also the utilization of in-situ characterization techniques including plasma emission spectroscopy and X-ray photoemission spectroscopy to evaluate this ECR NF_3 cleaning process.

EXPERIMENTAL

Experiments were performed in a Varian M-2000 multichamber integrated process system configured with experimental ECR and XPS modules. The experimental clean module comprised of a microwave ECR source has been described elsewhere (10). This ECR source was mounted on a standard Varian vertical, capacitively-coupled, 13.56-MHz rf etch module evacuated

with a turbo-molecular pump to sustain a base pressure below $2x10^{-7}$ Torr. Wafers were transferred to the ECR chamber through a single-wafer loadlock and processed at a pressure of 1 mTorr.

Substrates used in the etch rate study consisted of a 1000 Å thermal oxide layer thermally grown on 150-mm <100> Si wafers. The microwave power applied to the wafers was varied in the range of 500 to 1500W, whereas the rf power was varied in the range of 0 to 150W to provide a self-induced dc bias ranging from -5 to -200V. The wafers were measured with an ellipsometer (Rudolph Research AutoEl-III) before and after each experiment to determine the etch rate and uniformity. In the case of the polymer cleaning experiments, the CF_x polymer layer (11) was deposited onto <100> Si wafers by reacting CHF_3 with N_2/O_2 in a plasma discharge, where 8:1:3 (CHF_3:O_2:N_2) rf plasma was generated at a pressure of 360 mTorr in a parallel-plate etcher at 50 kHz. The thickness of the polymer layer was measured by surface profilometry both before and after the NF_3 cleaning process.

In-situ characterization techniques such as plasma emission spectroscopy, mass spectrometry and X-ray photoemission spectroscopy were used to evaluate the NF_3 cleaning process. Plasma emission spectroscopy, with the capability of performing actinometry measurements, was used to monitor gaseous contamination and to correlate the concentration of fluorinated species with process variables. An EG&G 1235 triple grating spectrograph with a 1465 multichannel analyzer was used for these measurements. The resolution of the 1200 groove/mm grating used is 0.12 nm and blazed at 500 nm. A differentially-pumped mass spectrometer (UTI 100C) was also used to study the gas chemistry.

XPS analysis of Si wafers was performed using a modified Surface Science Instrument Model 301 XPS mounted on an ultra-high vacuum chamber where data acquisition was at mid-10^{-9} Torr. Photoemission was excited over a nominal 1000 x 1300-μm^2 elliptical spot with monochromatic-focused $AlK\alpha_{1,2}$ radiation at 1486.6 eV. Photoelectrons were collected at a takeoff angle of 35°. Binding energies were determined with a 50-eV pass energy and referenced to the Au $4f_{7/2}$ peak at 83.9 eV.

RESULTS

Etch Rate of SiO_2

Removal of the SiO_2 layers by ECR-excited NF_3 plasma was studied with and without the application of rf bias. The effect of rf bias on the etch rates of SiO_2 is shown in Fig. 1. The self-induced dc bias was varied in the range of -5 to -200V by changing the rf power to the electrode from 0 to 150W. As expected, results indicate that the etch rate of SiO_2 increases with increasing rf bias. Also, the applied self-induced dc bias drastically enhances the SiO_2 etch rate. Furthermore, since the ion density of NF_3 is primarily controlled by the microwave power, increase of etch rate should be expected by increasing the ECR power. This increase of etch rate is observed in Fig. 1 when the net microwave power is increased from 1100 to 1500W.

In addition to the etch rate study at 1100W, SiO_2 uniformity with 3σ varied from 6 to 9% has been routinely achieved as rf bias changed from -30 to -200V. However, more uniform etch rate with 3σ values in the range of 4% have been obtained in the processed wafers without bias.

Figure 2 shows the dependence of SiO_2 etch rates on the ECR power for wafers processed without rf bias. Since the density of fluorine atoms and ions is mainly controlled by the microwave power, the energy of the incoming ions are primarily changed by varying the rf bias. Therefore, with ECR power only, SiO_2 etch rates are lower than those where a rf bias is applied to the electrode. Nevertheless, the results shown in Figs. 1 and 2 indicate that good SiO_2 etching rates can be achieved with or without bias.

Etch Rate of Polymer

Figure 2 also shows the dependence of polymer etch rates on the applied microwave power as the wafers were processed without dc bias. An increase of polymer etch rates is observed as the microwave power varied from 500 to 1500W. As compared to the SiO_2 etch rates, polymer etch rates are a factor of 2 higher. Furthermore, at 1500W and without rf bias, the polymer etch rate

of ECR-excited NF_3 plasma is a factor of 4 higher than that of a polymer layer removed by rf-biased ECR Ar plasma (11).

ECR-excited NF_3 is also employed to clean the CF_x polymer residue inside submicron contact holes. Patterned Si wafers intentionally coated with a CF_x polymer layer were cleaned by NF_3 plasma with microwave power at 1100 W and without rf bias. Preliminary results from cross-section SEM measurements show that the ECR NF_3 plasma has completely removed the polymer layer deposited at the bottom and on the side walls of the patterned contact holes.

In-Situ Gas and Surface Analysis

For contamination studies employing plasma emission spectroscopy, O^* (777.2 nm) emission line was constantly monitored upstream in the ECR plasma discharge (6" from the substrate) with respect to the F^* (775.5 nm) line in the ECR NF_3 plasma. Typical emission spectra are shown in Fig. 3. Besides the peaks related to Ar, N and fluorinated species, a conspicuous O^* peak was observed. It is speculated that the main source of oxygen was from the chamber wall. These results are consistent with the information collected from mass spectrometry measurements where dissociation of NF_3 into F and N via the ECR plasma is evident. Moreover, the presence of O^+ (16 amu) and SiO^+ (44 amu) when the NF_3 was excited by the ECR microwave is also consistent with the species detected by plasma emission spectroscopy.

To understand the specific role of fluorinated species in the ECR plasma etching, a low concentration of Ar (5%) was added to the NF_3 as an actinometer gas to quantify the relative F_2 concentration at ground state (12). The flow rates of NF_3 and Ar were 6.0 sccm and 0.3 sccm, respectively; the chamber pressure was maintained at 1 mTorr. As shown in Fig. 4, a linear relationship was observed to correlate the relative F concentration, depicted by the ratio of F^* (775.5 nm)/Ar^* (750.4 nm) intensities, and the applied ECR microwave power. This is similar to the behavior of the oxide etch rate with ECR microwave power (Fig. 2). This suggests that the oxide cleaning process is primarily controlled by the fluorine atoms produced from ECR NF_3 plasma.

The efficacy of the ECR NF_3 cleaning process for native silicon oxide was investigated by in-situ XPS. Figure 5a is a low resolution X-ray photoemission and Auger spectrum of the original native Si oxide. The usual silicon and oxygen transitions are observed with carbon in the form of adventitious hydrocarbon, the same as that observed in ECR-excited Ar plasma (4). After a 1-minute exposure of the Si wafer to an ECR-excited NF_3 plasma, the spectrum (Fig. 5b) shows transitions associated with fluorine and nitrogen in addition to that associated with native silicon oxide. The carbon has been removed by the plasma to below detection limits. A comparison of atomic ratio to Si, which is derived by trapezoidal integration of the Si 2s, 0 1s, N 1s and F 1s transitions after subtracting the background spectrum and applying appropriate sensitivity factors, is made before and after plasma exposure. The summarized result listed in Table I indicates that a thin residue layer has been formed as a by-product of exposing the Si wafer to an NF_3 plasma. This layer is rich in fluorine and has a high level of nitrogen and oxygen. No other elements are detected. The O/Si ratio is more or less representative of the surface after a 1-min plasma exposure. It typically varies from 0.06 to 0.28 and shows no clear correlation with ECR conditions, i.e., pressure, exposure time and microwave power.

A more detailed examination of the Si 2p transition shows a peak associated with this residue at 103.5 eV, having a full-width-half-maximum (FWHM) of 2.5 eV. In contrast, the shifted Si 2p peak due to the original native Si oxide is positioned at 103.1 eV and with a FWHM of 1.8 eV. Noting that a binding energy shift of the Si 2p transition is equal to 1.15 eV per Si-F bond (13), 1.05 eV per Si-O bond (14) and 0.62 eV per Si-N bond (15). The observed result here suggests that the broadening of the peak and the shift to higher binding energy are a consequence of forming a $SiN_xO_yF_z$ residue on the surface. The thickness of the residue is approximately 1 nm, when calculated from the ratio of the integrated residue to elemental Si 2p intensities and assuming both to have a 3-nm electron escape depth.

CONCLUSIONS

In summary, an ECR-excited NF_3 plasma has been applied to remove SiO_2 and CF_x polymer layers deposited on <100> Si wafers.

Etch rate studies have been performed by varying microwave power and rf bias. Without rf bias, the ECR-excited NF_3 plasma etches oxide and polymer layers. However, a thin $SiN_xO_yF_z$ residue remains as a by-product of exposing <100> Si to an ECR-excited NF_3 plasma. In-situ plasma emission spectroscopy has also been employed to monitor the gaseous contamination present in the ECR-excited NF_3 plasma. A noticeable amount of oxygen is present in the ECR module due to the observation of a sharp oxygen emission peak. It is speculated that the chamber wall is the main source contributing to this contamination. Furthermore, quantification of the fluorine concentration by actinometry indicates the key role of fluorine atoms contributing to the ECR NF_3 cleaning process for SiO_2.

ACKNOWLEDGMENT

The able technical assistance of J. Sonico, C. Holloway, R. McFarland, R. Underhill and N. Anderson is greatly appreciated.

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Table I

Comparison of atomic ratios characterized by XPS measurements for Si wafers before/after exposure to 1-min ECR-excited NF_3 plasma. The notation ND refers to not detected, where the detection limit is estimated at 0.5 at%.

Atomic Ratio	Native Oxide	ECR Plasma
O/Si	0.80	0.097
C/Si	0.04	ND
F/Si	ND	1.05
N/Si	ND	0.20

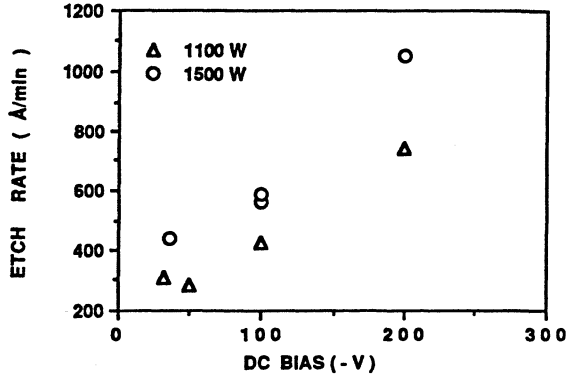


Fig. 1 Dependence of thermal SiO_2 etch rates on dc bias.

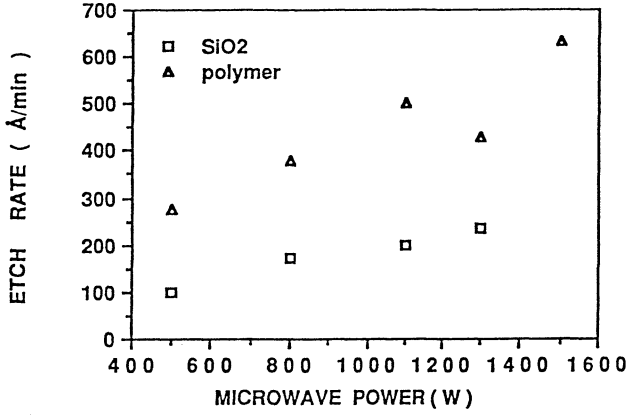


Fig. 2 Dependence of thermal SiO_2 and polymer etch rates on microwave power.

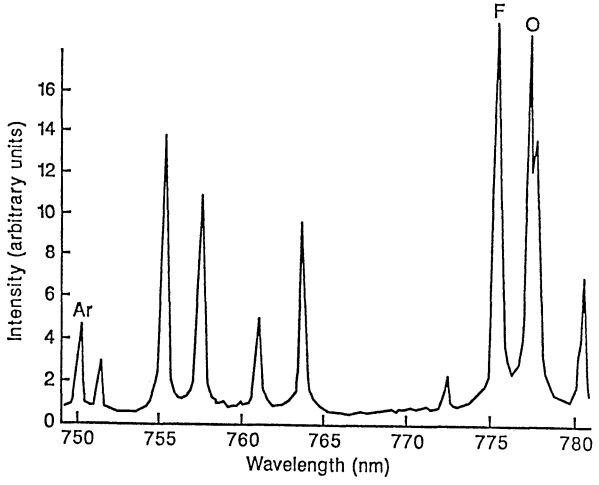


Fig. 3 Emission spectrum of ECR NF_3 plasma excited at 1300W.

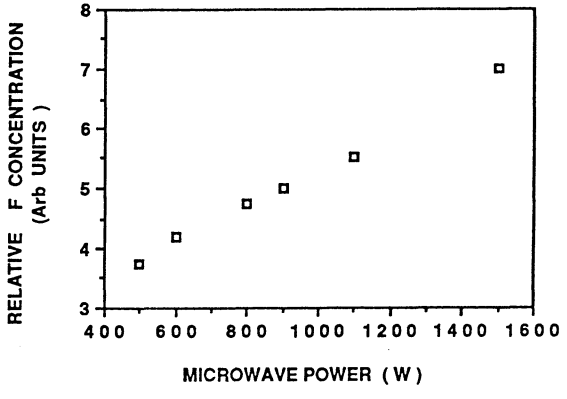
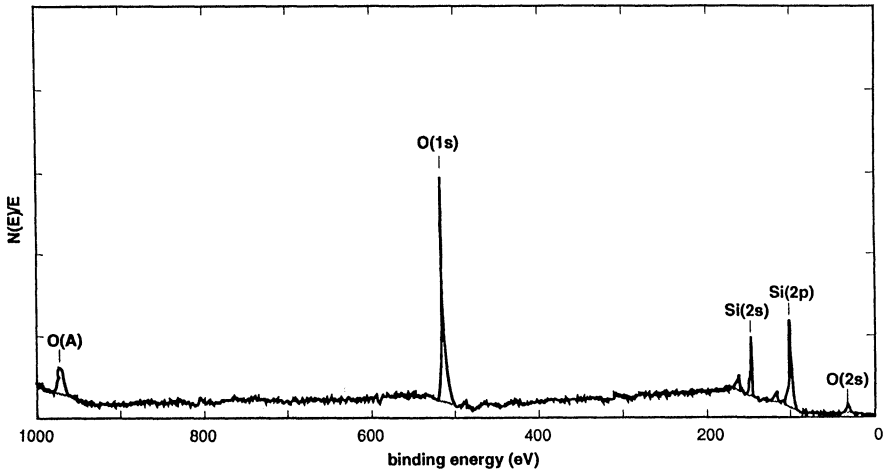
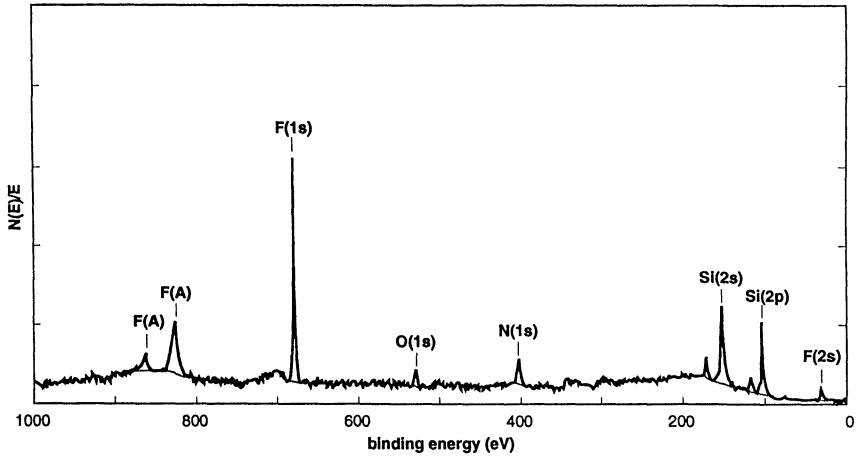


Fig. 4 Actinometry measurements of relative fluorine atom concentration as a function of microwave power.



(a)



(b)

Fig. 5 Low-resolution (50-eV pass energy), X-ray photoemission spectrum of: (a) <100> Si with a nominal 150-nm thick native oxide and (b) after 1-min exposure to an ECR-excited NF_3 plasma at 1.1 kW.

IN-SITU PRE-OXIDATION THERMAL CLEANING OF SILICON IN NO/HCl

Rodney Ridley and Jerzy Ruzyllo

Center for Electronic Materials and Processing
Department of Electrical and Computer Engineering
The Pennsylvania State University
University Park, PA 16802

The purpose of this investigation was to study thermal cleaning of silicon surfaces in NO/HCl gas mixture, and to integrate this cleaning mode as an in situ cleanup applied prior to conventional thermal growth of gate oxide. Results obtained indicate feasibility of this approach. The electrical characteristics of MOS capacitors formed on NO/HCl cleaned surfaces did not display significant difference as compared with devices processed in the traditional manner.

INTRODUCTION

Ideally, a silicon surface cleaning performed prior to gate oxidation should be carried out in situ, i.e., inside the conventional oxidation furnace tube. By not allowing the exposure of silicon surface to the ambient air in between cleaning and thermal oxidation steps, better control of the thin oxide growth can be achieved, and also, an improved gate oxide integrity should result. The possibility of surface cleanup integration with subsequent atmospheric pressure thermal oxidation may potentially offer significant advantages, but technically viable solutions to this problem still remain to be found.

A method of silicon surface thermal cleaning using NO:HCl:N_2 gas mixture, which was proposed several years ago [1] as a general purpose cleaning, offers promise in pre-gate surface treatments. It is a thermally enhanced gas phase cleaning technique, which has been shown to remove metals from the silicon surface. The metals are removed via a volatile form of metal compounds, most probably nitrosyls. Also, this technique using strongly oxidizing ambient is capable of removing organic contaminants from the surface. One of the consequences of the NO/HCl cleaning is a film containing oxygen, nitrogen and chlorine formed on the wafer surface. This "oxy-chloro-nitride" (OCN) film, typically about 40-60Å thick remains on the surface as a result of NO:HCl:N_2 exposure at elevated temperature.

The purpose of this investigation was to study further the NO/HCl thermal cleaning of silicon surfaces and to integrate it as an in situ clean up applied prior to the conventional thermal growth of gate oxide. One of the important aspects of this investigation was to determine the effect of the "oxide-chloro-nitride" (OCN) film on the kinetics of subsequent oxide growth. Another key issue in this study concerned effectiveness of surface cleaning using in situ NO:HCl:N_2 exposure. The MOS characterization was used to evaluate the outcome of this cleaning process.

EXPERIMENTAL

In this study p-type,(100), CZ grown silicon wafers with a resistivity of 6-9 ohm-cm were used. After initial thermal oxidation, wafers were subjected to a conventional photolithographic process during which field oxide was partially removed from the surface. It is assumed that the resist is the main source of contamination in silicon device processing, and hence, wafers following photolithography were used in this study as starting samples. After wet stripping of the resist, wafers were: (i) loaded directly into the oxidation furnace for in-situ cleaning and oxidation (Process I), or (ii) cleaned using standard wet clean and then loaded into the furnace to be thermally oxidized (Process II). All furnace treatments were carried out at 900°C. Cleaning in Process I was performed using 5% NO: 3-5% HCl: 90-92% N_2 mixture while thermal oxidations were carried out in dry oxygen. In Process I wafers were loaded in the furnace with NO:HCl:N_2 mixture flowing which means that temperature of the wafer during the cleaning process was ramped from about room temperature to 900°C. The total time of NO:HCl:N_2 exposure was 5 min. during which time cleaning action was taking place [2], and approximately 40-50Å thick film of "oxy-chloro-nitride" (OCN) was formed on the surface. Two variations of Process I were investigated. In Process IA wafers after NO:HCl:N_2 treatment remained in the furnace and thermal oxidation followed in-situ. In Process IB, after NO:HCl:N_2 treatments, wafers were taken out of the furnace, and the residual "oxide" (OCN film) was stripped off in water solution of HF. The wafers were then re-loaded into the furnace for thermal oxidation. Results of each process were evaluated using MOS characterization of aluminum gate capacitors fabricated on the processed wafers. This characterization included measurements of interface trap density, minority carrier lifetime, and oxide breakdown field.

In order to determine the effect of the OCN film on the oxide growth kinetics series of additional oxidations was carried out. Also, the etch rates of thermal oxides grown on OCN covered silicon were studied in an attempt to evaluate composition of such film.

RESULTS AND DISCUSSION

Oxide Growth

A first part of this investigation was devoted to the study of the effect of the OCN film resulted from NO/HCl cleaning on the kinetics of subsequent thermal oxidation of silicon. The OCN film after reaching a certain thickness was observed to display self-limiting growth, which coincides with previously published results [1,2]. The actual growth kinetics of the OCN film are not well understood, but it has been shown that this film consists of silicon, oxygen, nitrogen and chlorine, in the form of $SiO_xN_yCl_z$ [2]. The OCN film was approximately 40-50Å thick as determined using ellipsometry. While examining the OCN film thicknesses, we needed to determine its index of refraction which was found to be 1.471.

The results of an investigation of the oxide growth rate following NO/HCl exposure and OCN film formation are shown in Fig. 1. Comparison of curves shown in this figure clearly indicates that OCN film slows down oxide growth rate. This effect is more pronounced at longer oxidation times and may indicate reduced diffusivity of oxidizing species through the growing oxide. These results indicate that although OCN film slows down oxidation, it does not inhibit it to any significant extent, and hence, this film does not have to be removed following NO/HCl cleaning and prior to subsequent oxidation. This demonstrates feasibility of applying this surface treatment as an in situ pre-oxidation cleaning.

Oxide Etch Back

The etch rate of silicon oxide in HF water solution is an indication of its chemical composition across the film, and hence, etch rate studies can be used to evaluated homogeneity of such films. This technique was used in this experiment to determine the location of the oxy-chloro-nitride phase in the thermal oxides grown following NO/HCl exposure. The results, presented in Fig. 2, clearly show very slow etch of the oxide close to its surface. The etch rate is then increasing up to the value expected for stoichiometric SiO_2 as thin layers of oxide are gradually being etched off. Knowing that the etch rate for nitrided oxide in HF water solution are substantially slower than those for silicon dioxide, we are concluding that the OCN phase was displaced during thermal oxidation toward the oxide surface while the stoichiometric oxide was growing underneath. Rough estimation of the thickness of this OCN "skin" gives value of about 40-60 Å which is essentially the same as the thickness of OCN film on the silicon surface prior to oxidation. These results were the same in the case of initially 250 Å thick oxide and 1200 Å thick oxide suggesting that the oxy-chloro-nitride "skin" remains on the surface of the oxide during oxidation at 900°C regardless of the time of oxidation.

Electrical Characterization

The bulk of this study was devoted to the electrical characterization of MOS capacitors formed on the silicon substrates processed in the manner described

earlier in this report. These measurements are used as a preliminary evaluation of the effectiveness of NO/HCl cleaning.

The high frequency and quasi-static C-V measurements were used in this investigation to determine interface trap density. Some metals, for instance iron, tend to remain during thermal oxidation at the SiO_2-Si interface where they introduce energy states in the silicon bandgap. Those interface states can be quantitatively determined from C-V characteristics of MOS structures. In Fig. 3 values of interface trap densities for Processes IA and IB studied in this experiment are compared with those obtained using conventional wet cleaning prior to thermal growth of the gate oxide. As seen in this figure, trap densities achieved using Process IA, in which case NO/HCl thermal cleaning was in situ followed by thermal oxidation without etching OCN film off, are comparable with those obtained for conventional wet clean-thermal oxidation process. This can be viewed as an indication of at least some cleaning action taking place during NO/HCl exposure resulting in the reduced content of the interface metals. We draw this conclusion knowing that if not cleaned following resist stripping, thermally oxidized Si wafers display substantially higher values of interface trap densities than those shown in Fig. 3.

As compared to the Process IA, somewhat higher values of interface trap densities were measured for Process IB (Fig. 3). In this case wafers following NO/HCl exposure were removed from the furnace, OCN film was etched off in HF water solution followed by rinse/dry cycle, and then wafers were re-introduced to the furnace for thermal oxidation. It appears that these additional processing steps and wafer handling resulted in the increased values of interface trap densities. At the lack of direct evidence, it is difficult to definitely conclude on the exact reasons for this increase. Still one can speculate that trace metals were added to the surface during operations performed on the wafers between NO/HCl exposure and thermal oxidation. These results also indicate that no detectable amount of metallic species is embedded in the OCN film. If this wouldn't be a case, then removal of OCN film should improve characteristics of SiO_2 interface rather than cause their deterioration.

Results of minority carrier lifetime measurements performed on the wafers processed in the same manner as above show trends very similar to those observed for interface trap density. Summary of results presented in Fig. 4 shows comparable performance of conventional wet clean-thermal oxidation process and Process IA. On the other hand, inferior results were observed again for the Process IB. It is known that metals in silicon interacting with structural defects can form recombination centers responsible for the reduction of the minority carrier lifetime. If allowed at the silicon surface, these metals, for instance copper, can diffuse into silicon during thermal oxidation. From the results presented in Fig. 4 a conclusion can be drawn that Process IB results in the higher content of metallic contaminants in silicon that Process IA. Most likely those metals originate from the surface which was more contaminated following Process IB.

In contrast to interface trap density and minority carrier lifetime, the measurements of oxide breakdown field did not reveal meaningful differences between Processes IA and IB (Fig. 5). Additional experiments will be carried out to determine reasons for higher than expected number of low-field breakdowns in each case.

SUMMARY

The effect of in-situ NO:HCl:N_2 silicon surface cleaning prior to gate oxidation was investigated. The oxy-chloro-nitride film remaining on the silicon substrate following this treatment does not inhibit subsequent thermal oxidation. Using MOS characterization the effectiveness of the NO:HCl:N_2 cleaning process was determined to be comparable with conventional wet cleaning, but only if performed in situ without intermediate HF etch, rinse/dry operations carried out between cleaning and oxidation.

The effects of the NO:HCl gas phase cleaning technique are not fully understood yet, but this investigation did however serve to lay the groundwork for its further exploration as an in-situ pre-gate oxidation clean. Further thorough investigation involving surface analysis is needed to determine its final usefulness in silicon IC processing.

ACKNOWLEDGMENTS

Authors are pleased to acknowledge support of this study obtained from the Applied Research Laboratory of the Pennsylvania State University and Texas Instruments, Inc.

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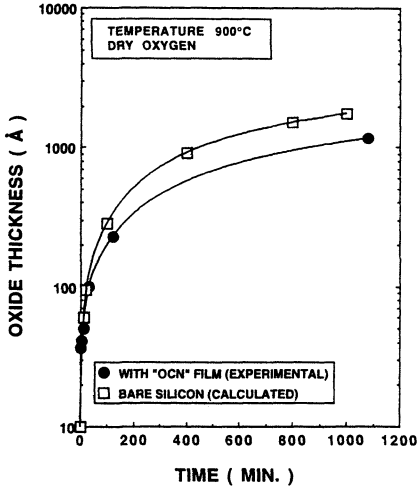

Fig. 1 Oxide growth rate curves. Theoretical curve was obtained using Ref. 3.

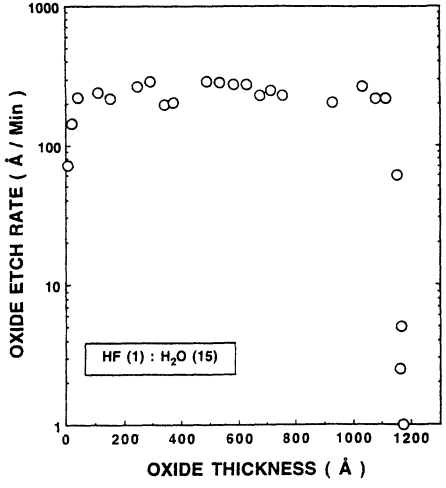

Fig. 2 Etch rate of oxides grown in this study (n = 1.465).

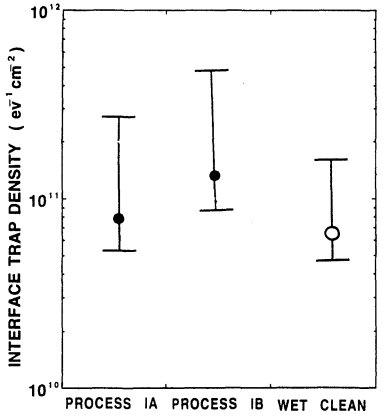

Fig. 3 Results of interface trap density measurements.

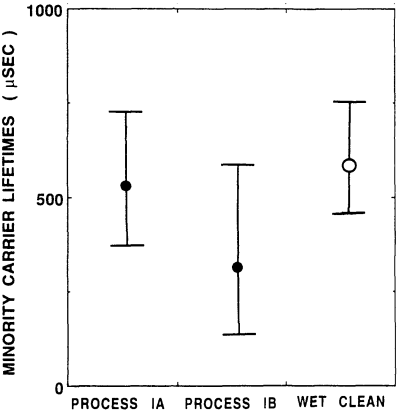

Fig. 4 Results of minority carrier lifetime measurements.

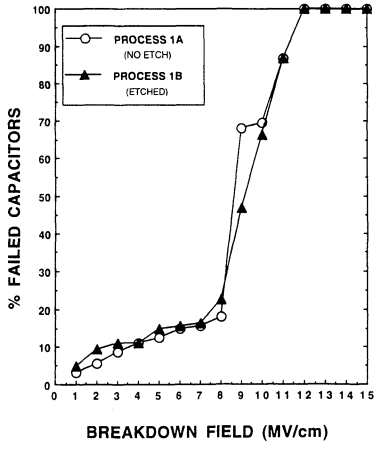

Fig. 5 Cumulative oxide breakdown statistics for process 1A & B. 128 capacitors were tested per process.

CHEMICAL VAPOR CLEANING FOR THE REMOVAL OF METALLIC CONTAMINATION FROM WAFER SURFACES USING 1,1,1,5,5,5-HEXAFLUORO-2,4-PENTANEDIONE

J.C. Ivankovits, D.A. Bohling, A. Lane*, and D.A. Roberts†
Air Products and Chemicals, Inc., Allentown, PA 18195
*Texas Instruments, Dallas TX 75265
†Schumacher Co., Carlsbad, CA 92009

An effective technique has been found for the removal of trace metallic contaminants from silicon wafer surfaces using 1,1,1,5,5,5-hexafluoro-2,4-pentanedione (HFAC) as a chemical vapor cleaning agent. The gas phase reaction of HFAC with surface iron and copper metal contaminants forms volatile reaction products at low temperatures (≤ 300°C). RBS analyses after chemical vapor cleaning of intentionally contaminated wafers shows that surface contamination is significantly reduced. Nickel and chromium also are removed from silicon oxide surfaces, but less effectively. The gas/solid interactions and mechanisms controlling metal removal are described.

INTRODUCTION

Presently, surface contaminants are removed from integrated circuit wafer surfaces either via plasma or wet etch/clean methods (1). Although these methods have been effective in removing most electrically active contaminants, the number of these cleaning steps is becoming very large. For the fabrication of standard high density integrated circuits, in excess of seventy wet process steps can be required during a full wafer production cycle. In devices which have larger design rules (>0.5μm), contaminants such as photoresist, oxide, nitride, etc., can be removed in plasma or wet cleaning processes which are reasonably efficient. As device geometries become more demanding, cleaning becomes more problematic. The shift to smaller line-widths and the advent of cluster tool environments has made the concept of fully dry processing very attractive. Plasma processes are still appropriate in a cluster environment, but are ineffective in removing unimolecular or molecular clusters of many of the transition metals and group I and group II mobile ions from a wafer surface without inflicting significant collateral damage. With the exception of selected group IV, V and VI halides, standard halogen etch products are not very volatile. Reactive ion etch can sometimes be effective, but this method can be equated to sputter cleaning, and could possibly lead to problems with re-deposition of dielectric material or other species, due to lack of selectivity (2,3,4). For this reason, it is necessary to develop alternative cleaning methodologies. This paper explores the concept of adding organic ligands capable of forming volatile metal complexes in the gas/solid system. Metals are then removed as volatile, stable coordination compounds.

The metals deposited upon the native oxide of the silicon wafers used in this study are assumed to be as the metal oxide species, with an oxidation state on the metal center greater than zero. We speculate that most metals deposited on bare silicon or on a hydrogen terminated silicon surface, using methods such as direct sputtering or from contaminants in cleaning/rinse solutions, will be reduced by the silicon (5). The fate of metal contamination on bulk field oxide is also fairly clear, likely remaining at higher oxidation states. Metal contamination on these surfaces from sources such as "cleaning" solutions can be

controlled to an extent, as described in a recent patent by Siemens, by adding metal complexing agents to the cleaning medium (6). Metal contamination can also come from other sources, such as photoresist ashing steps. However, removal of trace metals after they have become surface contaminants is extremely difficult (7). Additionally, these contaminants can cause problems in subsequent device manufacturing processes.

Gräf and Mühlhoff, et al, have recently published work showing how copper, once chemisorbed to the silicon wafer surface, can not be removed by simple wet cleaning methods (7). Furthermore, they have shown that even trace amounts of copper catalyze the growth of native oxide, especially under humid conditions. Copper actively cycles as a reduction/oxidation catalyst, likely sitting at the silicon/native oxide interface. Obviously, removal of trace copper, in light of the information presented by Gräf, would be desirable. Unfortunately, although copper is routinely found in Al/Cu alloys used in device fabrication, it is also one of the most difficult metals to remove by standard plasma techniques.

Main group metals, in their elemental state, can potentially be removed by the formation of volatile metalorganic compounds in a methane/hydrogen plasma (8). This technology has been developed by the compound semiconductor industry as an effective way to etch InP, AlGaAs, ZnSe, and other III-V or II-VI device structures. Methyl and hydrogen radicals react with the alloy metals forming volatile species such as trimethyl gallium, dimethyl aluminum hydride, and other organometallic compounds. A fact which is highly advantageous is good selectivity towards formation of the organometallics over etching of almost all standard mask materials, including SiO_2, Si_3N_4, and photoresist. However, plasma processes can lead to substantial damage to the devices.

The concept of forming volatile compounds with surface metals in a cleaning process is supported by consistent examples, as described for the formation of volatile organometallics in plasma etching of III-V materials. Similarly, we have pursued methods for *reactive* removal of transition metals from surface with the addition of potential ligands in the vapor phase to selectively react with metallic contaminants. Rather than the highly energetic and potentially damaging methods of plasma cleaning, the ligands react with the surface metals, forming metal complexes at the semiconductor surface. These metal complexes are volatile, and subsequently desorb, leaving a surface which is residue and damage free. This paper describes the effective removal of trace iron and copper from wafer surfaces utilizing 1,1,1,5,5,5-hexafluoro-2,4-pentanedione (HFAC) and trifluoroacetic acid (TFAA) as volatilizing agents. Chromium and nickel are removed to a lesser extent. The process employs the gas phase reaction of HFAC or TFAA with surface metals, forming volatile metal-organic reaction products, resulting in what we call Chemical Vapor Cleaning or CVC.

EXPERIMENTAL

The substrates in this study were {100} silicon, and were used directly as received from the vendor. Metals were deposited onto the wafer native oxide surfaces using standard evaporative techniques at 10^{-5} to 10^{-6} torr chamber pressure. Wafer surface metal concentrations were determined by Rutherford Backscattering analysis. RBS was performed using a 2.4 MeV helium ions with detectors at 170° and 99° to the beam. Uncertainty is estimated as ± one standard deviation from the mean of determinations using two beams. Sensitivity varied from 2% to 5% with the analyzed metal. The practical detection limit of this technique is ca. 0.5×10^{13} atoms/cm^2 for the contaminants studied.

Each wafer was scored and segmented into approximately one inch square samples. These were mounted at a 30 degree angle in a pyrex wafer boat and inserted into a small pyrex tube furnace. Filtered zero-grade (80/20 N_2/O_2) air was bubbled through a glass bubbler containing the chelating ligands 1,1,1,5,5,5-hexafluoro-2,4-pentanedione (HFAC) and trifluoroacetic acid. Based upon the vapor pressure of the reagents used, the partial pressure of the coordinating ligands was approximately 125 torr (16.5%). Process temperatures used were 200°C and 300°C, with total exposure to the process environment between twenty and forty minutes. Experimental control wafers were exposed to the one atmosphere total pressure thermal process without coordinating ligands in the gas phase.

RESULTS AND DISCUSSION

The results of several Chemical Vapor Cleaning experiments are summarized for copper, iron, chromium, and nickel in Table 1. At 200°C, using an atmosphere of HFAC, copper surface contamination is significantly reduced. Iron and nickel are removed to lesser extent, and chromium is not affected by our process. Raising the temperature to 300°C increases the removal rate of iron contamination from the surface, but has little additional effect on nickel and chromium. As can be seen from the data in Table 1, initial analyses of the wafers prior to cleaning showed surface metal concentrations for iron and copper of 7.99×10^{14} and 3.45×10^{14}, respectively. Analysis after the dry cleaning process gave concentrations of $\leq 2.9 \times 10^{13}$ atoms·cm^{-2} and $\leq 2.1 \times 10^{13}$ atoms·cm^{-2} for iron and copper, respectively, both of which were near the lower detection limit or LDL for the RBS technique used in the initial metals analyses. To confirm that metallic contamination was being removed, control samples were run in the furnace under identical thermal processes, but without any gas phase coordination compounds as a reaction medium. As can be seen by the thermal process data in Table 1, little or no interdiffusion of the surface contaminants into the native oxide or bulk silicon is seen.

Since the wafers were not cleaned or etched prior to processing, evaporative metal depositions were made upon native oxide, rather than on a hydrogen terminated surface. It is assumed that the copper was likely present at the wafer *surface* as copper (I) and (II) oxides. The initial surface chemistry of iron, nickel, and chromium in these experiments is less clear, although after exposure to atmosphere, all of the metals were probably present as their oxides; Fe^{II} and Fe^{III} oxides, Ni^{II} oxide, and Cr^{III} oxide, respectively. Surface metal silicides might also have been present, especially after subsequent thermal processing of the wafers (9).

Equation 1 suggests a plausible route for the removal of copper and other transition metal oxides by CVC. Using the working assumption that the metals are present as their oxides, the primary reactions affecting removal are thought to be between copper (I), copper (II), and iron (III) oxides and the free gas phase 1,1,1,5,5,5-hexafluoro-2,4-pentanedione. Specifically, the HFAC reacts with and is deprotonated by the metal oxide (i.e. $Cu^{II}O$) yielding the volatile metal-organic coordination complex and water vapor. A typical reaction with the metal oxide is:

$$CuO + 2H^{+}HFAC \longrightarrow Cu(HFAC)_2 + H_2O \qquad (1).$$

Reactions of HFAC with pure samples of Cu^{I}, Cu^{II}, and Fe^{III} metal oxides using conditions similar to those in our cleaning studies have been demonstrated in our laboratories in extensive experiments examining the bulk reactivity of the metal oxides with various ligand systems. We have shown that the direct reaction of HFAC with copper oxides ef-

ficiently produces a volatile copper ß-diketonate as the dihydrate, $Cu(HFAC)_2 \cdot 2H_2O$ (10). Although we anticipated from our bulk experiments better removal of chromium and nickel, the driving forces towards reaction of these surface metals with gas phase HFAC are not as large as for iron and copper under our process conditions, as we see smaller changes in the surface concentration of these metal species as compared to copper and iron. Clearly, however, there is a process window for removal of all the metals studied in these experiments, although this window is somewhat limited with chromium and nickel. Removal rates may be affected by the ultimate coordination complex volatility, although this is not a dominant property influencing the initial surface reactions.

The chemistry surrounding the reaction of HFAC with surface transition metal contaminants is not unique to HFAC. Trifluoroacetic acid (TFAA) has also been examined as a potential coordinating reagent (Table 2). Although its reactivity is quite a bit lower towards chromium, nickel, and iron, copper is removed to similar levels as for HFAC (see Figure 2). TFAA coordinates with the metal ions similarly to HFAC, although it is less sterically hindered, which may affect the stability of partially formed surface chemical moieties. The TFAA is not sufficiently reactive with either chromium or nickel, under the process condition utilized in these experiments, to cause any complexation and removal of the metal coordination compound as a volatile species. It is possible that the competing reverse reaction (deposition) is more prevalent with the TFAA than for HFAC.

CONCLUSION

Chemical Vapor Cleaning (CVC) using chelating ligands appears to have great promise for the removal of metallic microcontaminants on semiconductor material surfaces. We have determined that 1,1,1,5,5,5-hexafluoro-2,4-pentanedione and trifluoroacetic acid are both effective at removing specific metallic contaminants from silicon native oxide surfaces. Copper can be effectively removed from this surface at 200°C, and iron is efficiently removed at 300°C using either HFAC or TFAA chemical vapor cleaning agent. Nickel and chromium are more problematic, volatilizing only in the presence of HFAC under the process conditions used in our study. Although further study is required to determine the specific surface states and reaction mechanisms occurring with these reactive cleaning processes, they are effective as a methodology for reaching the goal of totally dry chemical vapor cleaning processes.

ACKNOWLEDGMENTS

Air Products and Chemicals, Inc., is acknowledged for its independent support of this project. Acknowledgments from Texas Instruments go to the TI Microelectronics Manufacturing, Science, and Technology program, supported by the Wright Laboratory Manufacturing Technology Directorate (WL/MTE), Electronic Technology Directorate (WL/ELA), and DARPA Defense Sciences Office (DARPA/DSC).

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TABLE 1. Surface metal concentration as determined by RBS using 1,1,1,5,5,5-hexafluoro-2,4-pentanedione as the cleaning agent. Thermal process only data utilized long reaction times at ≥300°C without chelating cleaning agents in the gas phase. HFAC 200°C and 300°C are for wafers processed at their respective temperatures at 1 atmosphere total pressure and with 125 torr partial preassure of the cleaning reagent.

METAL	INITIAL CONC.	THERMAL ONLY	HFAC 200°C	HFAC 300°C
Fe	7.99×10^{14}	8.1×10^{14}	3.13×10^{14}	0.29×10^{14}
Cr	7.01×10^{14}	6.9×10^{14}	8.74×10^{14}	4.45×10^{14}
Cu	3.45×10^{14}	3.6×10^{14}	0.31×10^{14}	0.21×10^{14}
Ni	5.31×10^{14}	5.4×10^{14}	2.91×10^{14}	2.62×10^{14}

TABLE 2. Surface metal concentration as determined by RBS using trifluoroacetic acid as the dry cleaning agent. TFAA 200°C and 300°C are for wafers processed at their respective temperatures at 1 atmosphere total pressure with 125 torr partial preassure of the cleaning reagent.

METAL	INITIAL CONC.	TFAA 200°C	TFAA 300°C
Fe	7.99×10^{14}	7.01×10^{14}	2.8×10^{14}
Cr	7.01×10^{14}	6.35×10^{14}	6.09×10^{14}
Cu	3.45×10^{14}	0.48×10^{14}	0.23×10^{14}
Ni	5.31×10^{14}	7×10^{14}	4.97×10^{14}

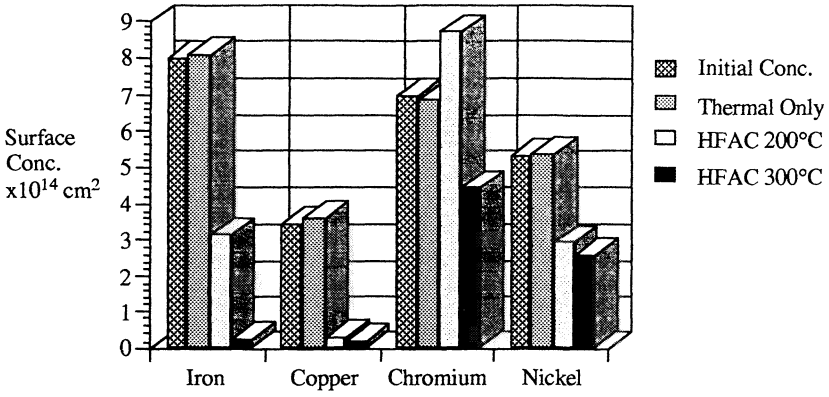

Fig. 1. Surface metal concentration as determined by RBS using 1,1,1,5,5,5-hexafluoropentanedione (HFAC) as the reactive cleaning agent. Thermal process data was determined at ≥300°C using long times. Total system pressure, P_{System} = 1atm. Partial pressure for the reactive cleaning medium was P_{HFAC} = 125 torr. HFAC 200°C and HFAC 300°C are for wafers run at the respective temperatures.

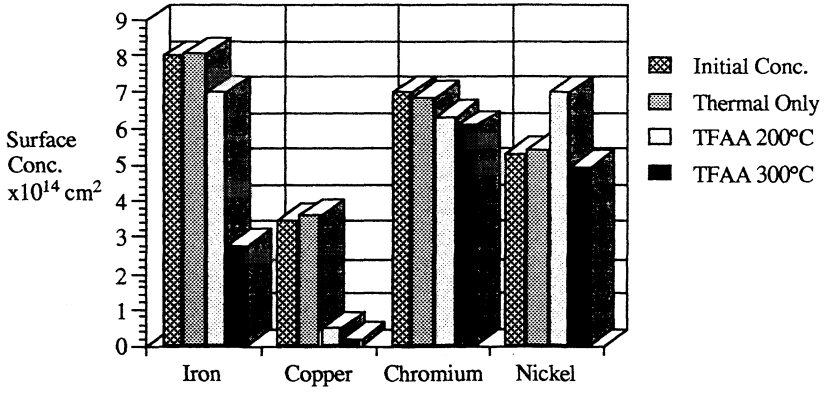

Fig. 2. Surface metal concentration as determined by RBS using trifluoroacetic acid (TFAA) as the reactive cleaning reagent. Thermal process conditions were as described in Figure 1. P_{Total} = 1atm. P_{TFAA} = 125 torr. TFAA 200°C and TFAA 300°C are for wafers run at the respective temperatures.

VAPOR-PHASE CLEANING: MECHANISMS OF ORGANICS DEPOSITION AND REMOVAL

Satish Bedge,[a] Gary A. Ruggles[b] and H. Henry Lamb[a]

[a]Department of Chemical Engineering
[b]Department of Electrical and Computer Engineering
North Carolina State University
Raleigh, NC 27695

Langmuir-Blodgett (LB) transfer was used to deposit pentadecanoic acid (PDA) films on silicon internal-reflection elements covered by photochemically grown oxide layers. Fourier transform infrared multiple-internal-reflection (FTIR-MIR) spectroscopy was used to characterize the oxide layers and the LB films. PDA surface concentrations were highly reproducible, as evidenced by integrated areas of the C-H stretching absorptions. The kinetics of UV/air photo-assisted oxidation of the resultant films was measured by using FTIR-MIR spectroscopy. A first-order rate law with an apparent rate constant of 0.5 min^{-1} was determined. For a dense PDA film, carbonyl (C=O) moieties were detected that are plausible surface intermediates in the total oxidation of the PDA hydrocarbon tail to CO_2 and H_2O. A 5.5-min UV/air treatment was found to be equivalent to a 10-min RCA SC1 clean in removing PDA films from hydrophilic silicon surfaces.

INTRODUCTION

Ultraviolet (UV)/air and UV/O_2 are advanced oxidation processes (AOP's) that have been applied to removal of organic contaminants from surfaces;[1] as such, they are dry, gas-phase alternatives to the RCA SC1 (NH_4OH:H_2O_2:H_2O) step in liquid-based silicon wafer cleaning. This work aims at an improved understanding of room-temperature UV/air cleaning of organics from silicon, through kinetics measurements of photo-assisted oxidation of organic films with well-defined compositions and surface structures.

In the initial quartz-cleaning experiments reported by Vig[1] and in early work on silicon wafer cleaning,[2] UV/air cleaning of process-related contaminants such as photoresists, pump oils, skin oils and solvent residues was investigated. Only recently have investigations of the surface chemistry of photo-assisted oxidation of organics on silicon appeared in the literature. Kasi and Liehr[3] examined UV/O_2 oxidation of organic compounds applied dropwise to clean hydrophobic silicon wafers. In their work, the photochemical growth of an oxide layer on the wafer, concomitant with organics removal, had to be considered. Here we report on an investigation of UV/air oxidation of Langmuir-Blodgett (LB) surfactant films applied to silicon covered by a photochemically grown oxide layer. Fourier transform infrared multiple-internal-reflection (FTIR-MIR) spectroscopy

was used to characterize the surfaces and to measure the kinetics of organics removal by UV/air treatment. In addition, a direct comparison was made of the efficacies of UV/air and RCA SC1 treatments for organics removal.

EXPERIMENTAL METHODS

Infrared internal-reflection elements (IRE's) were fabricated from double-polished (100)-oriented silicon wafers (Virginia Semiconductor). Lightly doped n-type float-zone silicon (2000 Ω-cm) was used because of its excellent mid-infrared transmission characteristics, owing to the absence of oxygen precipitates that are common to Czochralski silicon. The (100) faces were cleaned by UV/air treatment (*vide infra*) to remove trace hydrocarbon contamination and to grow thin (10-20 Å) oxide layers[4] that rendered the surfaces hydrophilic.

LB films were deposited using a Lauda FW1 film balance equipped with a surface pressure controller. Pentadecanoic acid, PDA, (99%+, Aldrich Chemical) was spread on the surface of pH 2 aqueous solutions prepared from electronic grade hydrochloric acid and 18 MΩ-cm deionized water that had been UV/air treated in a Barnstead D3603 OrganicPure unit. In the film balance, the air-water interface was cleaned of surface active residues by repeated compression and aspiration of the surface layer, until a negligible surface pressure was measured on compression. PDA films were spread using toluene as the solvent; the toluene evaporated slowly leaving a monolayer of surfactant at the air-water interface. PDA surface pressure-surface area (π-a) isotherms were obtained for each film used in coating an IRE, and the isotherms were in good agreement with those reported previously.[5] With the film expanded to 60 cm^2/molecule, an IRE was submerged in the trough; the film was compressed to the desired surface pressure in the liquid expanded (8 dynes/cm) or liquid condensed (20 dynes/cm) region of the π-a isotherm; and the IRE was raised slowly through the air-water interface at a speed of 2.5 mm/min by a stepper motor.

The silicon IRE's were UV/air treated using a low-pressure mercury lamp (BHK, Inc.) that was rated at 15 mwatts/cm^2 at a distance of 2.54 cm. The lamp was mounted in an aluminum enclosure with a lamp-to-surface distance of 0.5 cm. To clean both faces of an IRE it was necessary to expose alternately each face to the lamp. To measure the kinetics of organics removal, IRE's were removed at fixed intervals and FTIR-MIR spectra were measured.

FTIR-MIR spectra were measured using an Analect FX-6260 spectrometer equipped with a Harrick Scientific VRA-SRO accessory and a narrow-band mercury-cadmium-telluride detector. The infrared beam (ca. 13 mm in diameter) entered the double-sampling IRE through a 48° bevel, was internally reflected along the length of the crystal, was reflected from the opposing gold-coated 48° bevel, and was again internally reflected, finally exiting through the entry bevel. 50x16x1 mm and 10x16x1 mm double-sampling IRE's were used, giving 100 and 20 internal reflections, respectively. The larger elements gave high sensitivity to C-H and Si-H stretching vibrations, but they had an infrared cutoff of ca. 1500 cm^{-1}. By employing 10x16x1 mm IRE's, the optical path of the infrared beam in silicon was reduced, allowing detection of the Si-O stretching bands of the 10-20 Å thick SiO_2 films grown by UV/air treatment. These elements could not be used to detect surface species at submonolayer coverage because of the smaller number of internal reflections.

To characterize the oxide layer formed during UV/air treatment, a 10x16x1 mm IRE was precleaned by UV/air treatment, etched in 1% HF, and reoxidized by UV/air treatment. A 50x16x1 mm IRE was treated in parallel to characterize the hydrogen termination and organics contamination of the surfaces. FTIR-MIR spectra were measured after each step. Teflon beakers used for HF etching were cleaned using a Piranha etch (*vide infra*).

A comparison was made between UV/air treatment and conventional NH_4OH:H_2O_2 cleaning for organics removal. PDA monolayers were deposited on two IRE's. One of the IRE's was UV/air treated for 5.5 min. The other was subjected to a 10-min immersion in a 1:1:5 bath of NH_4OH:H_2O_2:H_2O at 80°C. FTIR-MIR spectra were measured before and after each treatment. Organic contamination from labware was minimized by boiling in Piranha etch (H_2SO_4 containing ammonium peroxy-disulfate at 120°C) for 30 min immediately before use.

RESULTS AND DISCUSSION

Passage of wafers through air-water interfaces where surface-active organic molecules are adsorbed is a mechanism of organic contaminant deposition on silicon surfaces.[6] As this mechanism is the basis of Langmuir-Blodgett (LB) film transfer,[7] this technique was chosen to deposit uniform monolayer organic films on silicon. Surfactant molecules like pentadecanoic acid (PDA) have a hydrophilic head group (e.g., carboxylic acid) and a hydrophobic hydrocarbon tail group. These amphiphilic molecules adsorb at air-water interfaces with their head groups in water and with their tail groups extending toward air. In LB transfer, a solid surface is slowly passed through an air-water interface containing an adsorbed organic film. If the surface is hydrophobic, a monolayer of surfactant will be transferred during immersion and will coat the solid with the tail groups in contact with the surface. Conversely, if the surface is hydrophilic, a monolayer of surfactant will be transferred during withdrawal and will coat the solid with the head groups in contact with the surface. If the transfer is ideal (transfer ratio near unity) the structure and density of the parent film at the air-water interface will be retained.

PDA was chosen for deposition because of its well-characterized phase behavior at the air-water interface.[5] If the area per molecule is greater than 500 $Å^2$, the PDA molecules are in a two-dimensional gas-like state in which they are oriented randomly and there are significant interactions of the hydrophobic tail groups with the water surface. On compression at 25°C (Figure 1), a liquid-expanded (LE) phase begins to form in which the tail groups lift from the water surface but there is still significant disorder. A single LE phase is present after isothermal compression to ca. 44 $Å^2$ per molecule. Further compression of the film leads to a constant-pressure phase transition to the liquid-condensed (LC) phase in which the film has long-range order and a significant degree of chain alignment.

In this work, PDA films were transferred onto hydrocarbon-free hydrophilic silicon internal-reflection elements (IRE's) that had been UV/air treated, etched in 1% HF, and reoxidized by UV/air treatment. The FTIR-MIR difference spectra (Figure 2) that were obtained following HF etching demonstrate removal of the photochemically grown oxide and hydrogen termination of the surface. The spectrum in the Si-H stretching region was

measured by using a 50x16x1mm IRE and reveals mixed dihydride (SiH_2: ν=2115 cm^{-1}) and monohydride (SiH: ν=2087 cm^{-1}) termination of the surface. Ideal termination of a Si(100) surface should result in dihydride species; Higashi and Chabal[8] have suggested that the presence of monohydride species on Si(100) surfaces is indicative of (111) faceting. The difference spectrum in the Si-O stretching region, that was measured by using a 10x16x1mm IRE, contains two broad negative peaks at 1055 and ca. 1180 cm^{-1}. The difference spectra obtained after the final 5-min UV/air treatment indicate loss of hydrogen and regrowth of a photochemical oxide layer.

The PDA surface concentration of each LB film was controlled by the surface pressure that was maintained during passage of the IRE through the air-water interface. LE and LC films were transferred by maintaining surface pressures of 8 and 20 dynes/cm, respectively. The LB coatings were characterized by FTIR-MIR spectroscopy; strong absorption bands assigned to C-H stretching modes (CH_2: ν_a =2918 cm^{-1} and ν_s=2850 cm^{-1}; CH_3: ν_a=2962 cm^{-1} and ν_s=2874 cm^{-1}) were observed. The PDA surface concentration (A) of each film was estimated from the integrated area of the C-H absorptions. The surface concentrations resulting from the transfer of each type of PDA film to silicon IRE's were found to be reproducible to within ca. ±10%, confirming that LB transfer is a valuable method for reproducibly applying organic coatings to silicon.[9] For coatings formed by transfer of LE films, the C=O stretching absorption (ν=1705 cm^{-1}) of the acid group was detected, but this absorption was very weak or absent in less dense coatings formed by transfer of LE films. For both types of LB coatings, we suggest that the hydrophilic head groups of PDA molecules are in contact with the hydrophilic surface produced by UV/air treatment of Si(100).

LB films of PDA on hydrophilic silicon IRE's were subjected to UV photo-assisted oxidation in air:

$$CH_3\text{-}(CH_2)_{13}\text{-}COOH \xrightarrow{\text{UV/air}} 15CO_2 + 15H_2O \qquad [1]$$

An ozone-generating low-pressure Hg lamp was used. Coatings with initial PDA surface concentrations (A_0) of 1.43 and 2.37 (arbitrary units) were prepared by transfer of LE and LC films, respectively. An ill-characterized PDA coating with a much higher surface concentration (A_0 = 4.63) was prepared by transfer of an adsorbed film that had collapsed, perhaps to a bilayer structure, at the air-water interface. The kinetics data obtained by using FTIR-MIR spectroscopy (Figure 3) demonstrate that UV/air treatment for 10 min results in 95-98% removal of the initial PDA coating, irrespective of the initial surface concentration.

A simple integral test of the kinetics data (Figure 4) indicates that UV photo-assisted oxidation of PDA on silicon covered by a pre-existing oxide layer follows first-order kinetics with respect to the surface concentration of CH groups:

$$r_{PO} = k\,A \qquad [2]$$

Under the ambient conditions of these experiments, the apparent rate constant k was ca. 0.5 min^{-1}. For the two films with lower surface concentrations, this simple rate law was obeyed until greater than 95% removal of CH groups was achieved. In contrast, for the dense film the photo-oxidation rate declined more rapidly with time than predicted by

first-order kinetics (Figure 4). The origin of this effect is unclear. Kasi and Liehr[3] have suggested that the incomplete removal of organics by UV/O_2 treatment at room temperature is caused by subsurface entrapment of hydrocarbon fragments in the growing photochemical oxide layer. This explanation is less plausible here, as the surface was passivated by growth of a photochemical oxide before LB transfer.

The FTIR-MIR data obtained during UV/air treatment of the dense LB coating provide evidence of surface intermediates that contain C=O groups. Difference spectra (Figure 5 a.-e.) were generated by subtracting from the spectrum measured after each treatment step, the spectrum recorded following the preceding step. The first difference spectrum (Figure 5a) illustrates the effects of depositing the PDA film, as indicated by positive C-H and C=O absorptions. The succeeding difference spectra (Figure 5 b.-e.) indicate that the C-H stretching absorptions decreased monotonically with each UV/air treatment. In contrast, absorption in the C=O stretching region increases during the early stages of photo-assisted oxidation of the PDA coating (Figure 5 b.-c.), and then decays dramatically (Figures 5 d.). The last 10-min treatment results in little reduction of the C-H and C=O absorptions, since very little organic contamination remains on the surface. The concentration profiles of the CH and CO groups suggest that photo-assisted oxidation of the PDA hydrocarbon tail to CO_2 and H_2O proceeds through carbonyl (C=O) surface intermediates. XPS spectra reported by Kasi and Liehr[3] also provide evidence of surface carbonyl species after UV/O_2 treatment of alcohols on silicon. The final difference spectrum (Figure 5 e.) illustrates the effects of the UV/air treatment sequence: essentially complete removal of carbon-hydrogen and carbonyl moieties.

Finally, a comparison was made of UV/air treatment and an RCA SC1 treatment for removal of PDA from hydrophilic silicon. The results (Figure 6) indicate that UV/air cleaning for 5.5 min is equivalent to a 10-min immersion in an SC1 (NH_4OH:H_2O_2:H_2O) bath at 80°C.

CONCLUSIONS

Passage of silicon wafers through air-water interfaces incorporating surface-active organic molecules is a microcontamination mechanism that can be exploited to prepare reproducible films for investigations of organics removal from silicon surfaces. FTIR-MIR spectroscopy is a unique and highly sensitive characterization technique for C-H, Si-H and Si-O species on silicon surfaces. UV/air photo-assisted oxidation of PDA on silicon covered by a passivating photochemical oxide layer follows first-order kinetics with respect to the surface concentration of CH groups. For a dense PDA coating, carbonyl groups were detected that are likely surface intermediates in the total oxidation of PDA. Room-temperature UV/air treatment and a 1:1:5 NH_4OH:H_2O_2:H_2O treatment at 80°C are equally effective at removing PDA from hydrophilic silicon.

ACKNOWLEDGEMENTS

This work was supported by the NSF Engineering Research Center for Advanced Electronic Materials Processing (CDR-8721505) and by the EPA Center for Waste Minimization and Management at North Carolina State University. We thank Professor Ruben Carbonell and Professor Peter Kilpatrick of the Department of Chemical Engineering for their assistance.

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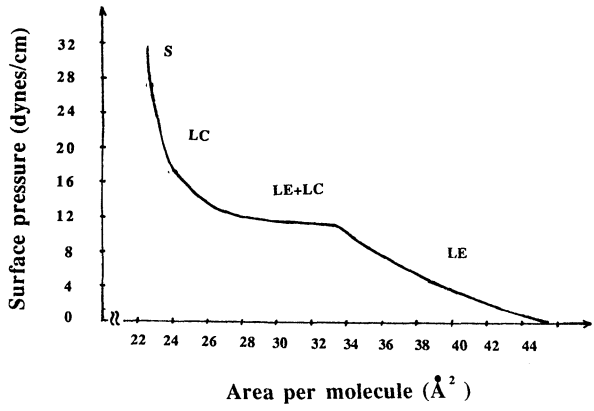

Figure 1: Experimental π-a isotherm for a PDA monolayer film on a pH 2 aqueous substrate at 25°C.

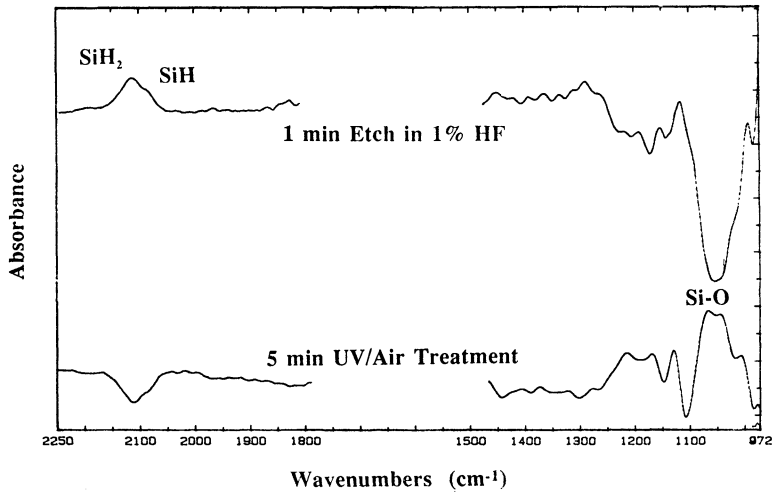

Figure 2: FTIR-MIR difference spectra of: 1% HF etching of a photochemically grown oxide layer on Si(100) (upper spectra) and regrowth of an oxide layer by UV/air treatment (lower spectra).

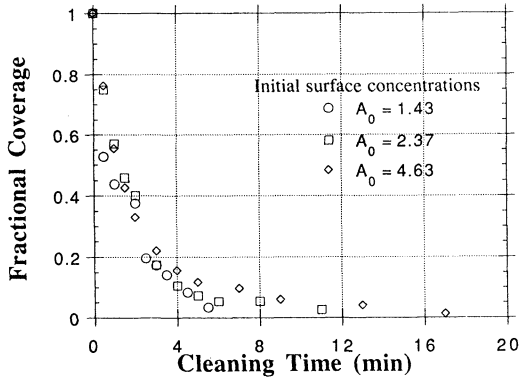

Figure 3: Kinetics data for the photo-assisted oxidation of PDA monolayers on pre-existing photochemical oxide layers.

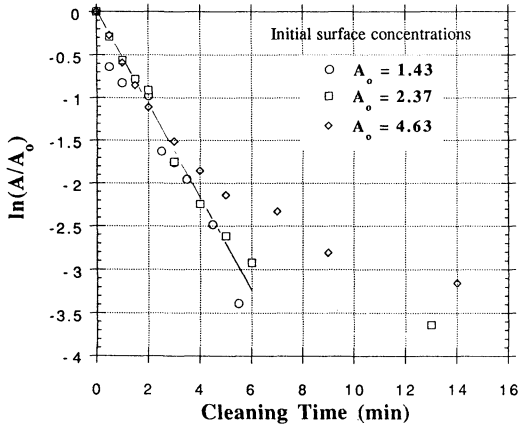

Figure 4: Fit of kinetics data for PDA photo-assisted oxidation to a first-order rate law.

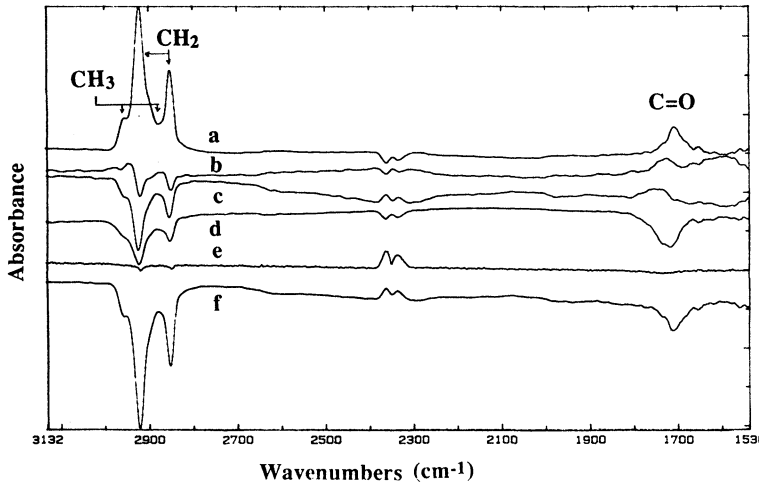

Figure 5: FTIR-MIR difference spectra: (a) spectrum of IRE coated with a PDA monolayer minus spectrum of clean IRE with a photochemically grown oxide layer; (b) spectrum of IRE after UV/air treatment for 1 min minus spectrum of IRE coated with a PDA monolayer; (c) spectrum of IRE after UV/air treatment for 6 min minus spectrum of IRE after UV/air treatment for 1 min; (d) spectrum of IRE after UV/air treatment for 22 min minus spectrum of IRE after UV/air treatment for 6 min; (e) spectrum of IRE after UV/air treatment for 32 min minus spectrum of IRE after UV/air treatment for 22 min; (f) overall effect of treatment: spectrum of IRE after UV/air treatment for 32 min minus spectrum of IRE coated with PDA monolayer

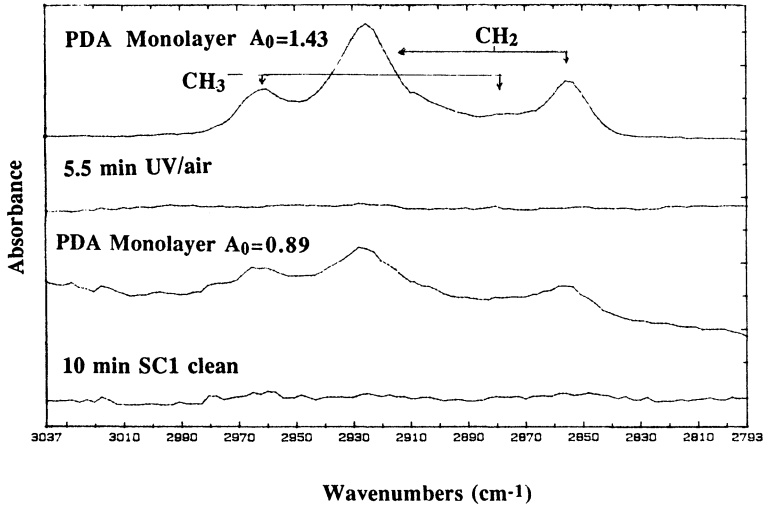

Figure 6: FTIR-MIR spectra illustrating the oxidative removal of PDA from hydrophilic silicon by a 5.5-min UV/air treatment and by a 10-min treatment in 1:1:5 $NH_4OH:H_2O_2:H_2O$ at 80°C.

ELECTRONIC STRUCTURE, SURFACE MORPHOLOGY AND EPITAXY OF REMOTE H-PLASMA CLEANED Si(100)

T. P. Schneider, J. Cho, D.A. Aldrich, Y.L. Chen, D. Maher,and R.J. Nemanich
Department of Physics and Department of Materials Science and Engineering, North Carolina State University, Raleigh, N.C. 27695-8202.

ABSTRACT

Low temperature (50-400°C) and low pressure (10-300 mTorr) processing conditions for remote H-plasma cleaning of Si(100) substrates were investigated. After plasma exposure, ordered surfaces were obtained which displayed 2x1, 3x1 and 1x1 LEED diffraction patterns. The surface phases following the H-plasma clean were dependent on temperature and pressure. The electronic states of the surfaces were explored with angle resolved uv-photoemission spectroscopy (ARUPS) and states due to Si-H bonding were identified. The surface morphology was examined with TEM. Suitability of the cleaning process for low temperature epitaxy was demonstrated by MBE growth on a 2x1 surface.

INTRODUCTION

The combination of ex situ wet chemical clean and in situ H-plasma exposure has proved useful as a surface preparation procedure for oxidation, plasma deposited oxide and plasma CVD epilayer growth (1-4). Major advantages of the H-plasma cleaning process include the low temperature processing and chemical passivation of the ordered surface. In this study the surface morphology for different H-plasma exposure conditions is explored. The surface morphologies are characterized by the resulting LEED diffraction patterns, and the electronic states of the different surfaces are measured with Angle resolved UPS. Here H induced surface electronic states can be correlated with the H bonding configurations. In addition, low temperature Si epi by MBE is demonstrated on the H-plasma exposed surfaces.

The approach of combined ex situ and in situ clean is to prepare chemically stable well characterized surfaces suitable for oxidation, oxide deposition or epi growth. The ex situ process removes the major amounts of hydrocarbon and oxide surface contaminants. The H-plasma exposure removes residual contaminants and allows relaxation into an ordered surface morphology.

Previous work has demonstrated that the H-plasma passivates the Si surface and reduces the surface chemical activity (1,3,5). The H-passivated surface has proved suitable for homoepitaxial growth of Si by remote plasma enhanced chemical vapor deposition (RPECVD) (1,2). Research by T. Yasuda, et. al. (4), showed that remote H-plasma

exposed Si(100) surfaces were suitable for low temperature deposition of SiO_2. Furthermore, the work indicated that the Si/SiO_2 interface had a low defect density, $D_{it} \sim 1\text{-}3x10^{10}/cm^2$ eV (4).

Previous approaches of remote H-plasma exposure included indirect or direct excitation of the H. In the indirect excitation, a plasma of Ar or He is excited which interacts downstream with the H. Direct excitation refers to the case when no upstream carrier gas is used, i.e. H_2 gas was directly excited and dissociated in the plasma. In the case of direct plasma excitation the Si(100) surfaces following processing at 300°C exhibited 2x1 reconstructed surfaces as indicated by low energy electron diffraction (LEED) (3,5).

The H-plasma exposure has also been utilized to produce H-passivated Ge(100) and $Si_{0.8}Ge_{0.2}$(100) substrates (6). Following H-plasma exposure at 300°C and 180°C of the $Si_{0.8}Ge_{0.2}$(100) and Ge(100) surfaces, respectively, the surfaces exhibited ordered two domain 2x1 and 1x1 reconstructions.

This study further investigates the Si(100) morphology for H-plasma exposure for variations in temperature and H pressure. The electronic structure of these H-passivated surfaces was determined by ARUPS. High-resolution transmission electron microscopy (HRTEM) was used to study the surface morphology after H-plasma exposure and the epi interface after MBE growth of Si on an H-plasma exposed substrate.

EXPERIMENTAL

Prior to the in situ H-plasma surface preparation, the wafers were cleaned with a two step ex situ process. The substrates studied were Si(100), 25 mm. dia., phosphorous doped (n-type), with a resistivity of 0.8-1.2 ohm-cm. The substrate thickness was 12-20 mils. The ex situ cleaning consisted of a uv-ozone exposure followed by a dilute HF spin etch {HF:H_2O:ethanol:(1:1:10)} (7). In the two step process the uv-ozone addressed removal of hydrocarbons and the spin etch removed the oxide leaving a hydrogen passivated but disordered surface.

The plasma reactor was connected to a surface analysis system which included LEED, AES, and ARUPS. The plasma cleaning and surface analysis systems were UHV compatible. The base pressure of the plasma reactor was $2.0x10^{-9}$ Torr, and the base pressure of the surface analysis chamber was $<2.0x10^{-10}$ Torr. The arrangement provided for detailed in-line surface analysis following the plasma cleaning.

The H-plasma was generated by an inductively coupled rf field through a 12 turn copper coil encircling a quartz tube (dia.= 3.175 cm). The hydrogen flowed through the coil region and was partially ionized by direct excitation, *i.e.* no carrier gas was used. The substrates were positioned 40 cm. downstream relative to the center of the plasma tube. For the surface cleaning in this study the power was 20 watts, and the pressure ranged from 10 to 300 mTorr. For all pressures the plasma was mostly confined to the discharge tube, but for pressures less than 20 mTorr a much weaker plasma glow did extend throughout the chamber.

The samples were inserted into UHV through a loadlock to the H-plasma reactor and exposed to plasmas with the following conditions: pressure = 10 to 300 mTorr, temperature = 50-400°C, flow = 10.00 sccm H_2, rf-power = 20 Watts, and duration = 2 mins.

Following the H-plasma cleaning, the wafers were transferred to the analysis chamber. LEED patterns were obtained using a beam energy of 60.8 eV, and AES was measured to monitor the O and C surface concentrations. The samples were then transferred to the ARUPS chamber. ARUPS measurements were excited with 21.2 eV uv-radiation from a He I discharge lamp. The photoemitted electrons were analyzed with a 50 mm. hemispherical electron analyzer mounted on a two angle goniometer. The measurements in this study had an energy resolution of 0.15 eV and an angular resolution of 2°.

The cross-sectional HRTEM micrographs were obtained from the surface regions of H-plasma cleaned samples and from the interface of MBE growth of Si on an H-cleaned Si surface. The Si was deposited by a custom MBE system (base pressure < 1.0×10^{-10} Torr). The sample was H-plasma cleaned in the plasma-surface analysis system and transferred through atmosphere to the MBE system suffering an exposure to air for ~5 mins. The substrate temperature during deposition was 550°C, and a growth rate of .33 Å/sec. was used. A layer thickness of 200 Å was deposited.

RESULTS AND DISCUSSION

A Surface After ex situ Clean

The Si(100) surface exhibits a 1x1 LEED pattern following the uv-ozone/HF spin ex situ cleaning (3-5). In addition, the AES shows that the oxygen and hydrocarbon contamination is less than 9 and 4 % in the surface region respectively. Previous IR measurements of HF etched Si(100) have indicated at least three different Si-H bonding configurations on the surfaces which have been attributed to SiH, SiH_2, and SiH_3 (8). The ARUPS spectrum of the surface after the spin etch is displayed in Fig. 1. The spectrum shows no evidence of oxide or the surface states observed from a clean surface. In addition, there is no evidence of organized electronic states from the ordered H passivated structures. The characteristics of the ordered H-terminated surfaces are discussed in the following sections. The lack of H induced electronic states indicates that the H-bonding on the surface is not simply a dihydride bulk terminated surface. It is more likely that the surface exhibits significant disorder, and variations in bonding arrangements. Thus, the results are consistent with the IR measurements.

B H-Plasma Exposed Surfaces

Following H-plasma cleaning, the surface morphology can exhibit 1x1, 3x1, and 2x1 surfaces (1-5). The different morphologies are obtained by variations in processing pressure and sample temperature. Examples of the 1x1 and 2x1 LEED patterns are shown

in Fig. 2. The observed surface reconstructions for the processing ranges considered are displayed in Fig. 3. For temperatures of 50-200°C during H-plasma cleaning, the LEED indicated the 1x1 surface phase (Fig. 2a). The 1x1 surface phase has been modelled to have a bulklike arrangement of the surface atoms uniformly saturated with atomic H in the dihydride phase. The dihydride model involves two H atoms bonded to each Si surface atom (9,10).

For processing temperatures of 275-400°C, the LEED displayed the two domain 2x1 phase (Fig. 1b). The 2x1 reconstruction can be obtained for both H-terminated and atomically clean Si(100) surfaces. The LEED pattern was symmetrical, showing two domains, one rotated 90° with respect to the other. As indicated by scanning tunneling microscopy (STM) measurements, the domains occur on terraces separated by single atomic steps (11). The LEED pattern in Fig. 2b showed diffuse half-order spots and streaking from the [10] spots extending towards the half order spots in the [11] direction. The diffuse scattering can be interpreted in terms of finite domain size. An approximate domain size can be calculated by use of the Scherrer relation for angular diffraction peak width. The relation is given by $L = \lambda (\Gamma \cos \theta)^{-1}$ where L is the domain size, λ is the deBroglie wavelength of the incident electrons, Γ is full width at half maximum of the diffraction peak (in rad), and θ is the angle of the diffracted electrons relative to the surface. For 60.8 eV electrons the wavelength is 1.5Å and an approximate peak width of 5° suggests L ~ 28Å. The streaking in the diffraction patterns is also an indication of disorder. One possible explanation is that the streaking was due to misalignment of the dimer rows which can be shifted by one lattice site without changing the local atomic symmetry.

The LEED indicated the Si(100):3x1 phase for processing conditions of temperature = 250°C and pressure = 150-350 mTorr. The model for the hydrogen passivated 3x1 phase consists of alternating mono- and dihydride bonding in linear chains on the surface (8). The location of the 3x1 phase between the 1x1:H and 2x1:H phases in Fig. 3 is consistent with this model.

The comparison of ARUPS spectra obtained following different processing conditions is shown in Fig. 1. The feature at 6.2 eV below E_f in the 300°C case has previously been attributed to Si-H states of the monohydride 2x1 structure for H-plasma exposed surfaces (5). The feature at ~3.5 eV below E_f in the 300°C H-plasma cleaning spectra has recently been attributed to the Si-Si dimer bonding of the reconstructed surface (12). The ARUPS spectra recorded from the surface cleaned at 100°C showed only a broad feature at ~6 eV (i.e. in the region of the Si-H bonding), and no evidence of the feature associated with the Si-Si dimer bonding. From these results we propose that the surface after low temperature H-plasma exposure exhibits predominantly dihydride Si-H bonding. In either case, 100 or 300°C, the spectra did not show states near the gap which are due to dangling bond states (5) indicating that the H passivated these chemically active sites. Furthermore, we have previously noted that the H-passivated results are consistent with an unpinned surface Fermi energy (3,5).

HRTEM used for microstructural studies of high power H-plasma exposure of Si(100) has shown that for long duration (>5 mins.) exposures, the near surface region

contains platelet defects (13-15). The platelet defects appear to be due to H diffusion into the substrate thus forming H stabilized "bubbles" along (111) planes (14,15). Fig. 4 is a cross-sectional HRTEM micrograph of a Si(100) surface cleaned at 300°C. In the case of short duration ($\leq$2 mins.) H-plasma cleaning, the surface was smooth and no obvious platelet defects could be observed.

C. Low temperature Epitaxy on H-plasma Exposed Si(100)

Lattice imaging of the interface formed after MBE growth of Si is displayed in Fig. 5. The Fourier transform of the lattice on both sides of the interface indicated that the reciprocal lattice vectors where the same. The analysis also showed that the reciprocal lattice vectors were continuous across the interface. Hence, the Fourier analysis confirmed that the MBE-grown layer was epitaxial. The slight contrast in the micrograph along the interface may be attributed to surface damage due to ion milling during the sample preparation for HRTEM. In this example MBE growth on Si(100) has been achieved without raising the substrate temperature above the MBE growth temperature of 550°C (ie. no high temperature UHV anneal).

CONCLUSION

The results presented here showed ordered surface morphologies which were dependent on substrate temperature and pressure during H-plasma cleaning. At lower temperatures dihydride 1x1 surface were obtained while at temperatures near 250°C, 2x1 or 3x1 surfaces were obtained at different pressures. At higher temperatures, the 2x1 ordered surface was obtained.

The resulting electronic structure of the H-plasma cleaned 1x1 and 2x1 Si(100) surfaces were obtained. Disorganized electronic states were observed after the ex situ preclean. No dimer bonding was indicated in the ARUPS spectra for the 1x1 surface. For the 2x1 surface, H induced states and Si-Si dimer bonding electronic states were identified. The cross-sectional HRTEM micrographs indicated that the the surface was smooth following H-plasma cleaning and that low temperature MBE growth on the H-passivated surface resulted in an epitaxial layer.

ACKNOWLEDGEMENTS

We acknowledge helpful discussions with M. Mantini, R. Rudder and R. Markunas. This work was supported in part by the NSF through grant CDR 8721505.

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FIGURE CAPTIONS

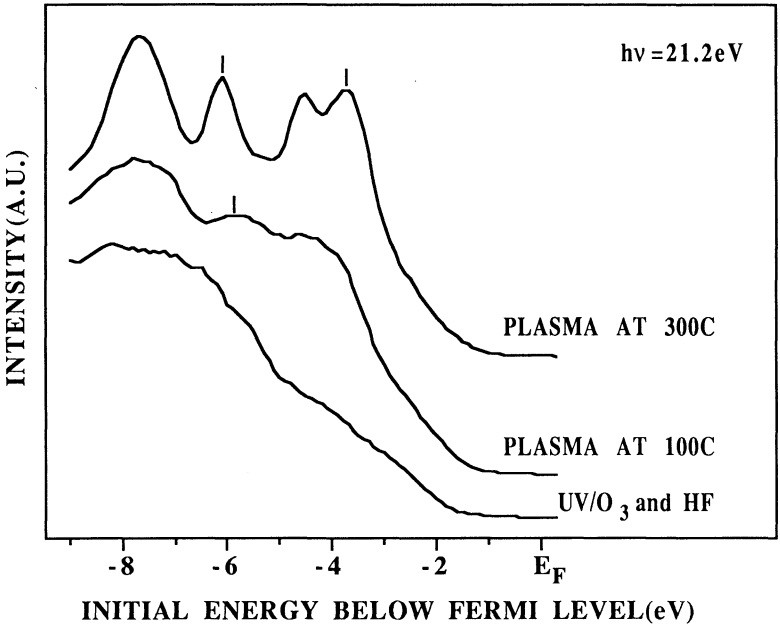
Fig. 1 ARUPS spectra: a) after uv-ozone/HF treatment showing a broad spectra with no organized electronic states due to Si-H bonding; b) after 100°C H-plasma exposure which shows a broad feature at ~ 6 eV below E_f which is associated with the dihydride phase of Si-H bonding; and c) after 300°C H-plasma cleaning showing the monohydride Si-H features at 5.4 and 6.2 eV. Also, the feature at ~3.5 eV is attributed to the Si-Si surface dimer bonding.

Fig. 2 LEED patterns obtained with a beam energy of 60.8 eV: a) 1x1 after 100°C H-plasma cleaning indicating a bulklike arrangement of surface atoms; and b) 2x1 after 300°C H-plasma cleaning indicating a reconstructed surface.

Fig. 3 Pressure-Temperature-Surface Phase of the Si(100) surface indicating the surface morphology .

Fig. 4 HRTEM micrograph of H-plasma cleaned Si(100) surface.

Fig. 5 HRTEM micrograph of the interface of MBE-grown Si on an H-plasma cleaned Si(100) substrate. The interface is indicated by the arrow. No defects were obvious at the Si(100) substrate surface, at the interface, or in the epilayer.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PLASMA AT 300C
PLASMA AT 100C
UV/O 3 and HF
INTENSITY(A.U.)
-8
-6
-4
-2
E F
INITIAL ENERGY BELOW FERMI LEVEL(eV)

Fig. 1

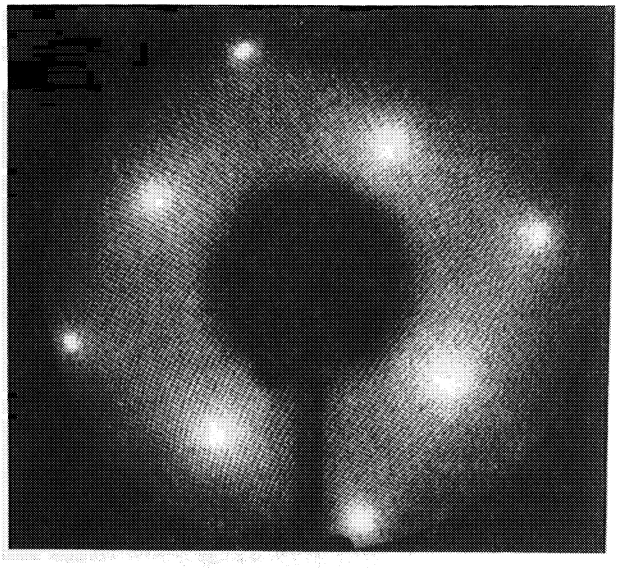


Fig. 2a

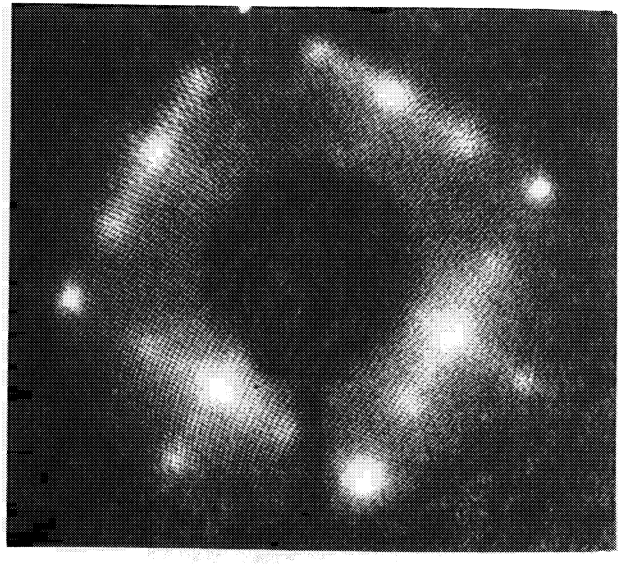
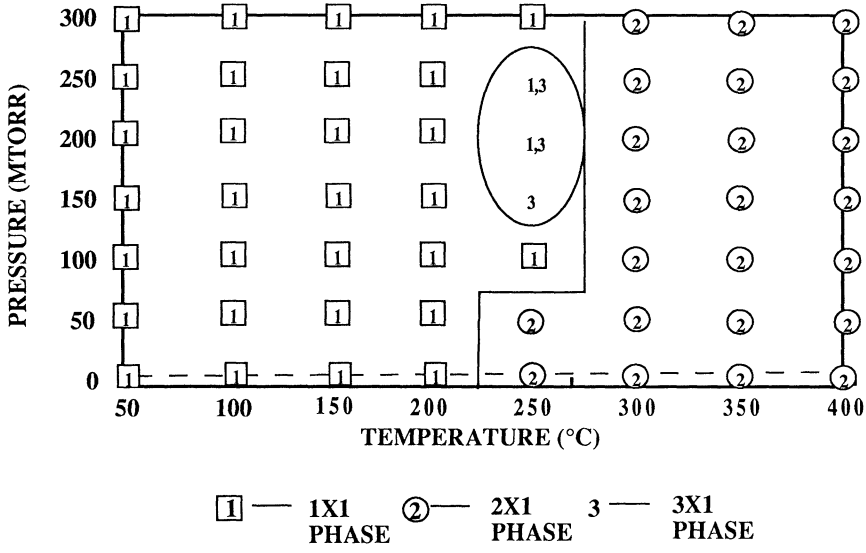


Fig. 2b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250
200
150
100
50
0
1,3
1,3
3
50
100
150
200
250
300
350
400
TEMPERATURE (°C)
1 — 1X1 PHASE
2 — 2X1 PHASE
3 — 3X1 PHASE

Fig. 3

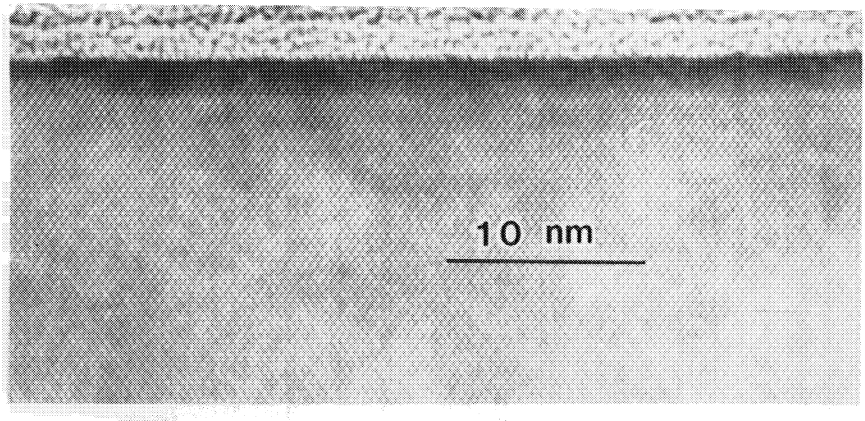

Fig. 4a

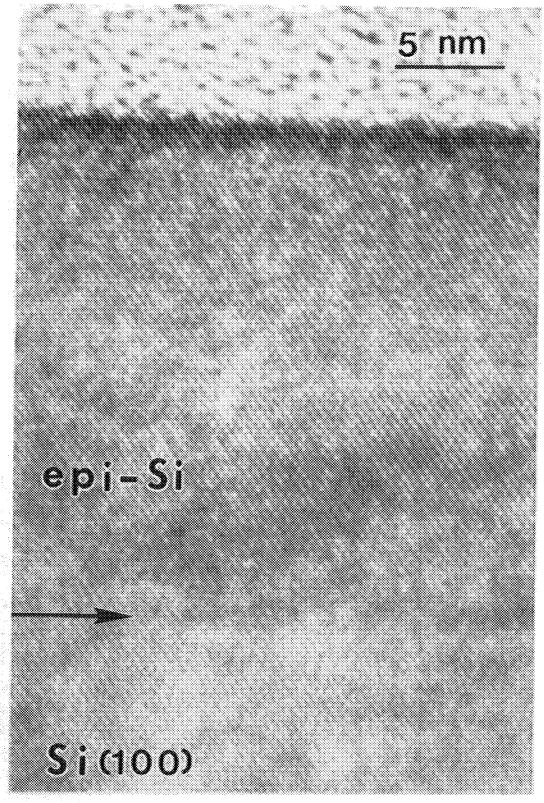

Fig. 4b

THE REMOVAL OF ETCH DAMAGED SILICON BY VARIOUS CLEAN-UP METHODS

Karen Reinhardt
Advanced Micro Devices
5204 East Ben White Blvd.
Austin, Texas 78741

ABSTRACT

An etch-induced damage and contamination removal process has been developed that effectively removes the damaged silicon and the polymeric residue deposited on the silicon surface in a plasma oxide etch process. The underlying silicon has the damage level restored to that of unetched silicon, as measured with thermal wave modulated reflectance (TWMR). Rutherford backscattering (RBS) measurements confirm the results obtained by the thermal wave diagnostic technique. X-ray photoelectron spectroscopy (XPS) and time of fight secondary mass spectroscopy (TOF-SIMS) determine the surface contamination caused by the polymer formation induced by the oxide etch. The efficiency of the post etch clean-up steps in removing the polymeric material can also be determined by XPS and SIMS. Surface photovoltage (SPV) measures the surface induced charge during the etch step and also measures any heavy metal contamination the wafer may acquire during the etch process.

INTRODUCTION

Effective and efficient clean-up of the silicon wafer surface after a plasma etch process is essential to the fabrication of high yielding integrated circuits. The silicon lattice damage and the contamination to the wafer surface during the plasma etch process causes damage to the silicon and may effect the oxide quality grown after processing and may also lead to contact resistance problems. Contamination from polymers and metals must be removed before the next high temperature processing step. High energy radiation and ions cause damage to the silicon surface that must be minimized and effectively annealed.

A production worthy etch process must impart minimal damage to the silicon substrate during the fabrication of integrated circuits. But due to the nature of the plasma etch process which uses carbon containing gas compositions, high energy electro-magnetic radiation, and ion bombardment; the transistors being fabricated are exposed to these undesirable effects. The damage removal process is designed to remove the

polymer that forms on the wafer surface,[1,2] to remove the silicon damaged by the electromagnetic radiation and ion bombardment,[1,3,4] and to remove any metal contamination sputtered onto the surface during the etch process.[5]

The structural and chemical damage associated with the etch process may be evaluated with a variety of readily available analytical equipment. Thermal wave modulated reflectance (TWMR) analysis has shown to be a viable technique for measurement of the silicon substrate damage during the etch process.[6,7] Rutherford backscattering can determine the extent of the silicon lattice damage; and the damage levels can be compared to the TWMR signal.

X-ray photoelectron spectroscopy (XPS) is used to determine the bonding structure of the polymer deposited on the silicon surface during the etch process.[8] XPS is a low energy radiation diagnostic technique that does not decompose the polymer during the analysis. Static secondary ion mass spectroscopy is used in conjunction with XPS to determine the elemental concentrations and the thickness of the organic film.

Surface photovoltage (SPV) analysis is used to measure minority carrier lifetimes and diffusion lengths. This technique indicates the radiation damage imparted to the silicon during the etch process and also can be used to determine if heavy metals are being sputtered onto the etch surface during the etch process.[9,10]

EXPERIMENTAL

Etch systems

A Lam Research Corporation Rainbow 4500 system is used to perform some of the etch experiments. The Lam 4500 system is a parallel plate split powered diode; the power is generated at 400 KHz; the top electrode material is graphite coated anodized aluminum. The wafer is held onto the backside helium cooled electrode with a polymer coated clamp; the wafer is cooled to a temperature of approximately -20°C. The clamp is covered with Kapton tape, to simulate the polymeric material that forms during the etch process.

A LRC Autoetch 590 system is also used to perform some of the etch experiments. The Lam 590 is a parallel plate diode system with power applied to the bottom electrode generated at 13.56 MHz. The top electrode is aluminum coated with graphite; the bottom electrode and the side walls are aluminum.

An Applied Materials Technology 8310 system is used to perform some of the etch experiments. The AMAT system is an RIE hexode reactor and is powered at 13.56 MHz. The electrode is aluminum; the aluminum wafer platten is Lexan or Ardel coated. The hexode material is stainless steel.

The oxide etch process evaluated in these experiments contains two steps. The first step etches the oxide with high selectivity to silicon, and the second step removes the damaged silicon caused by the first step. The oxide etch processes use a reducing, polymer forming, gas composition. The gas compositions include CHF_3, with either C_2F_6, CF_4, or O_2, and an inert gas such as helium or argon. The damage removal processes evaluated a variety of process compositions. Gases that effectively etch silicon, SF_6, NF_3, and CF_4, with and without an inert gas, and mixtures of the fluorine containing gas with an inert gas and O_2 were tried. Table 1 shows various combinations of process gases and parameters investigated.

Oxide growth processes

The wafers are oxidized in a horizontal furnace tube at 1000°C for 15 minutes in a steam/oxygen ambient atmosphere.

Diagnostic equipment

The system used to measure the damage to the silicon is a Therma-Wave Incorporated Therma-Probe 200. The basic optical configuration of the Therma-Probe system is thoroughly described in reference 6. Full wafer maps can be obtained. The RBS, XPS, and TOF-SIMS data were obtained using commercially available diagnostic equipment. The diffusion lengths and the minority carrier lifetimes were measured on a Semiconductor Diagnostic Incorporated CMS III. This system uses non-destructive and non-contact techniques. Full wafer maps can also be obtained.

Sample preparation

The damage monitor samples were prepared using P-type <100> Cz silicon substrates. Approximately 1000 A thermal oxide was grown and etched back in buffered oxide etch to remove the lap-back damage caused by the wafer fabrication process. This procedure also ensured that all wafers received the same thermal cycles prior to the etch step. To simulate production conditions, silicon wafers were exposed to the plasma for the same time a device wafer would be exposed to the plasma after the oxide was cleared during the overetch step.

RESULTS

Thermal wave modulated reflectance analysis

The TWMR detect the disruption of the silicon lattice. Previous results show that as ion bombardment increases through an increase in the power and a decrease in the pressure, silicon damage increases.[11,12] The ions in the plasma are accelerated toward the silicon with increasing energy at higher power densities. Therefore, as the ions impact the silicon lattice, increasing damage occurs with increasing power density of the plasma. Table 2 shows a comparison of the TWMR signal with different etch systems, etch conditions, and etch compositions. Results show that different etch systems have an effect on the degree of lattice damage and by elimination of the inert gas from the etch process, the degree of damage decreases.

XPS/TOF-SIMS analysis

XPS and TOF-SIMS detect the polymeric contaminants deposited onto the wafer surface during process. The amount of polymer formed during etching is a function of the ratio of CHF_3 to CF_4. The selectivity of the oxide etch rate to poly etch rate increases as the amount of polymer formed increases. The selectivity and the silicon damage are affected by the same factors; which indicate less damage occurs when a layer of fluorocarbon polymer is deposited onto the wafer during etching. Speculation is that the fluorocarbon layer prevents ion penetration into the silicon, thus limiting the intensity of the damage. The depth of the polymer is dependent on the time the wafer is exposed to the polymer depositing plasma and the selectivity of oxide to silicon. XPS comparing various etch systems and conditions are shown in Table 3.

This data shows that the etch systems studied deposit polymer on the wafer during the etch process. Minor differences in the bonding structure are apparent, but in general the polymers deposited show C-CF_x and CF_x peaks. This type of polymer is hard to remove with an oxygen plasma. A fluorine-rich plasma, which can oxidize the polymer and etch the silicon that may have Si-C bonds, is the most effective in removing the polymer; however, at a sacrifice of also removing silicon. Figure 1 shows XPS spectra after an oxide etch process and after a plasma clean-up process.

Surface photovoltage analysis

SPV detects any heavy metals and the inclusion of any non-annealable charge traps in the silicon substrate. Plasma exposure of the silicon surface implants ions and electrons

into the lattice. Heavy metals sputtered from the reactor may also deposit on the wafer surface. The implanted electrons cause a change in the recombinant lifetime. As the power density increases, more ions are implanted into the substrate and more heavy metals are deposited on the surface. SPV measurements show a substantial decrease in diffusion lengths after plasma etch and oxidation. SPV results are summarized in Table 4.

Effects on oxide growth

The degree of silicon lattice damage and the thickness of the polymeric layer affect the thermal oxide growth on the silicon. Table 5 shows examples of normalized oxide thickness grown on a silicon wafer after various process conditions. Oxide that is grown immediately after oxide etch, when there is a large amount of polymer on the wafer, has an inhibited growth rate. Oxide that is grown on a wafer that has silicon lattice damage has an accelerated growth rate. As little as 30 A of polymer on the wafer surface can inhibit the oxide growth. For example, less than 50 A of oxide is grown on a polymer coated wafer versus 400 A on an uncontaminated wafer.

Oxide etch step

Results show that the oxide etch step imparts damage to the silicon lattice by disruption of the bonding structure as indicated by TWMR. Polymeric residues are deposited onto the surface during the etch process as seen with XPS and TOF-SIMS. SPV data show that the diffusion length is decreased substantially after plasma exposure.

These results compare well with previous data. Etching with pure CHF_3 or pure CF_4 in an RIE system[13] and etching with CHF_3/O_2 in a similar RIE system[14] showed that silicon damage increased, as indicated by minority carrier generation lifetime decrease. Results confirm that the polymer formation contributes to the decrease in the damage imparted to the wafer during etching.

Damage removal step

Silicon damage during the etch process has been traditionally removed by first subjecting the wafer to an oxygen plasma in which a thin layer of silicon is oxidized and then removing the oxide by an HF or BOE dip[3,15]. Another technique is to subject the wafer to a high temperature anneal or oxidation of the silicon.[16,17] Drawbacks in these methods include inadequate control of the silicon removal depth, and limitation of the applications of the high temperature process. Therefore, an in situ, low power, plasma assisted

damage removal processes have been developed that do not use elevated temperatures and allow only the damaged silicon to be removed.

Since the damage to the substrate by the oxide etch step is substantial and the damage is greater than 350 A in depth, the damage removal step must remove the damaged silicon uniformly to the appropriate depth and must not impart damage of its own to the lattice structure.

Results show that etch-induced silicon lattice damage is best removed in a diode type system. The hexode system is capable of achieving a reduced damage oxide etch, but the clean-up steps do not effectively removed the silicon lattice damage. The diffusion lengths are reduced for all types of etch processes, and do not show significant improvement after the clean-up process. Results show that all systems investigated are effective at removing polymeric material during the clean-up step.

SUMMARY AND CONCLUSIONS

Plasma etch-induced damage and contamination can be quantified with the use of readily available analytical tools. The use of 1WMR, SPV, and XPS/TOF-SIMS have shown to be useful diagnostic techniques for application to etch process characterization. A successful method for removing the damage and contamination can be achieved by the implementation of a post oxide etch clean-up process. The most effective gas compositions for the clean-up step are fluorine containing, such as SF_6 or NF3. Carbon containing etch compositions are not suggested for the clean-up step. An inert gas added to the clean-up mixture complicates the damage removal process by providing an undesirable ion bombardment component, when a chemical etch is more desirable. Therefore, the elimination of inert gases in the clean-up process is recommended. By determining the effects of the etch equipment and the process parameters on the analytical measurement, the processes can be modified to effectively remove the polymeric contamination, reduce the damage to the silicon substrate, and minimize the effects of ion bombardment on the wafer surface. This contributes to an optimized final etch process.

ACKNOWLEDGEMENTS

The author would like to thank Paul Rhoades of Lam Research Corporation, Francois Dumesnil of Therma-Wave, and Mike Edgell of Charles Evans for helpful discussion and Ruby Raheem of the AMD Analytical Lab for the RBS measurements.

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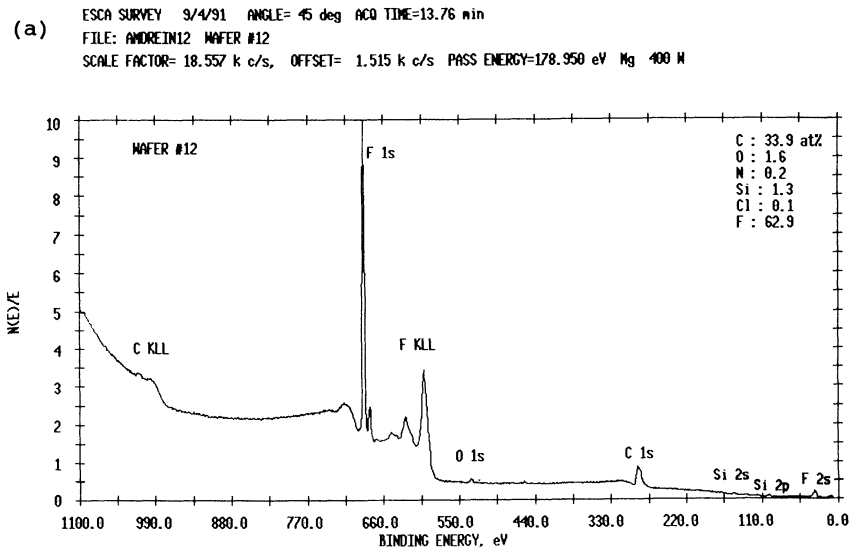
Figure 1. (a) X-ray photoelectron spectra after an oxide etch process. Carbon and fluorine containing residue are present on the wafer surface. (b) X-ray photoelectron spectra after an oxide etch and subsequent clean-up process. Carbon and fluorine concentration have decreased.

(a)



(b)

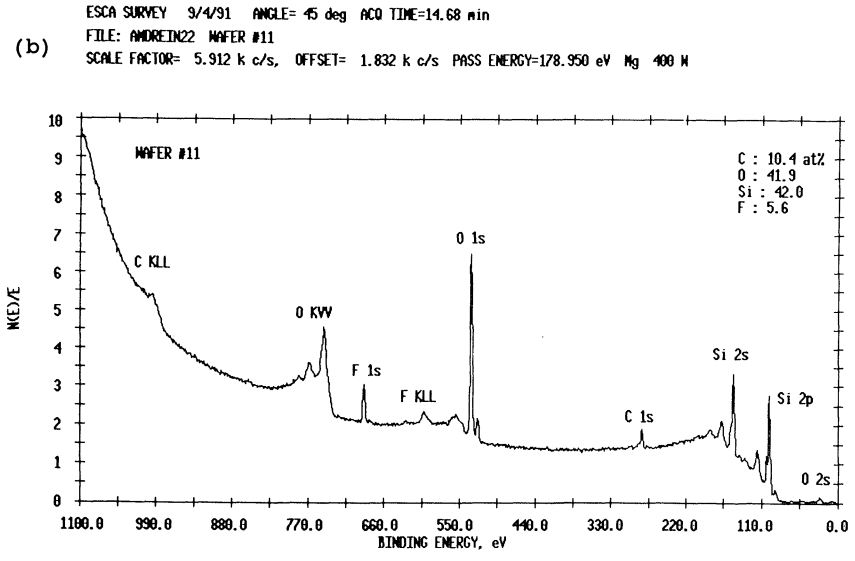


Table 1. (a) Oxide etch processes and parameters used for the evaluation of etch-induced damage and contamination. (b) Clean-up processes and parameters for post oxide etch silicon damage and polymer removal.

(a)

SYSTEM	TYPE	GAS COMPOSITION	PRESSURE	POWER
S1	diode plasma 13.56 MHz	$C_2F_6/CHF_3/He$	1.0 - 2.0 torr	400 - 800 watts
S2	diode split power 400 KHz	$CF_4/CHF_3/Ar$ $CF_4/CHF_3/He$ CF_4/CHF_3	0.4 - 1.0 torr	300 - 800 watts
S3	hexode RIE 13.56 MHz	CHF_3/O_2 $CHF_3/O_2/Ar$	30 - 50 mtorr	1600 - 2400 watts

(b)

SYSTEM	TYPE	GAS COMPOSITION	PRESSURE	POWER
S1	diode plasma 13.56 MHz	CF_4/He $NF_3/O_2/He$	250 - 500 mtorr	350 - 550 watts
S2	diode split power 400 KHz	SF_6/Ar SF_6/He SF_6	0.8 - 1.4 torr	30 - 100 watts
S3	hexode RIE 13.56 MHz	CF_4/O_2 $CF_4/O_2/Ar$	100 - 200 mtorr	100 to 500 watts

Table 2. Thermal wave modulated reflectance signal obtained from the various oxide etch processes before and after the clean-up step.

SYSTEM	PROCESS	PRE-PROCESS	POST-PROCESS	POST-OXIDATION
S1	etch $C_2F_6/CHF_3/He$	33.0	290	
S1	etch $C_2F_6/CHF_3/He$ clean $NF_3/O_2/He$	36.3	63.6	
S1	etch $C_2F_6/CHF_3/He$	40.8	86.3	
S2	etch $CHF_3/CF_4/Ar$	37.0	480	30.6
S2	etch CHF_3/CF_4	32.7	305	32.9
S2	etch $CHF_3/CF_4/He$	47.8	405	33.0
S2	etch $CHF_3/CF_4/Ar$ clean SF_6/Ar	33.7	128	31.5
S2	etch CHF_3/CF_4 clean SF_6	37.4	54.7	33.8
S2	etch $CHF_3/CF_4/He$ clean SF_6/He	40.7	122	31.4
S3	etch CHF_3/O_2	36.1	121	40.8
S3	etch $CHF_3/O_2/Ar$	50.0	297	78.8
S3	etch CHF_3/O_2 clean CF_4/O_2	37.5	178	

Table 3. Surface contaminant concentrations from the oxide etch process before and after clean-up.

SYSTEM	PROCESS	C %	F %	O %	Si %
S1	etch $C_2F_6/CHF_3/He$ clean CF_4/O_2	20.0	3.2	45.0	32.0
S1	etch $C_2F_6/CHF_3/He$ clean $NF_3/O_2/He$	8.0	3.7	32.0	56.0
S2	etch $CHF_3/CF_4/Ar$	40.0	47.0	7.0	5.5
S2	etch CHF_3/CF_4	33.9	62.9	1.6	1.3
S2	etch $CHF_3/CF_4/Ar$ clean SF_6/Ar	20.9	18.8	34.6	24.2
S2	etch CHF_3/CF_4 clean SF_6	10.4	5.6	41.9	42.0
	CONTROL	9.9	0.7	42.2	46.0

Table 4. SPV diffusions lengths (um) obtained from the oxide etch processes before and after the clean-up step.

SYSTEM	PROCESS	PRE-PROCESS	POST-PROCESS	POST-OXIDATION
S1	etch $C_2F_6/CHF_3/He$	246	306	
S1	etch $C_2F_6/CHF_3/He$ clean $NF_3/O_2/He$	286	286	
S1	etch $C_2F_6/CHF_3/He$ clean CF_4/He	189	223	
S2	etch $CHF_3/CF_4/Ar$	250	367	103
S2	etch CHF_3/CF_4	269	342	97.1
S2	etch $CHF_3/CF_4/He$	266	368	118
S2	etch $CHF_3/CF_4/Ar$ clean SF_6/Ar	277	293	147
S2	etch CHF_3/CF_4 clean SF_6	302	297	113
S2	etch $CHF_3/CF_4/He$ clean SF_6/He	280	300	111
S3	etch CHF_3/O_2	297	378	66.4
S3	etch $CHF_3/O_2/Ar$	326	301	153
S3	etch CHF_3/O_2 clean CF_4/O_2	310	296	

Table 5. Normalized oxide growth (A) after oxide etch process with and without the clean-up etch step.

SYSTEM	PROCESS	OXIDE	SYSTEM	PROCESS	OXIDE
S2	$CHF_3/CF_4/Ar$	959	S2	$CHF_3/CF_4/Ar$ SF_6/Ar	1101
S2	CHF_3/CF_4	979	S2	CHF_3/CF_4 SF_6	1052
S2	$CHF_3/CF_4/He$	953	S2	$CHF_3/CF_4/He$ SF_6/He	1060
S3	CHF_3/O_2	989	S3	CHF_3/O_2 CF_4/O_2	996
S3	$CHF_3/O_2/Ar$	1019		CONTROL	1000

THE COMBINED EFFECT OF SILICON SURFACE ROUGHNESS AND METAL IMPURITY CONTAMINATION ON GATE OXIDE INTEGRITY

M. Meuris, M. Heyns, P. Mertens, S. Verhaverbeke
IMEC vzw, Kapeldreef 75, B-3001 Heverlee, Belgium
and
A. Philipossian
Digital Equipment Corporation, 77 Reed road,
Hudson, MA 01749, USA

In this paper, some aspects of the pre-oxidation cleaning technology are discussed. The influence on gate oxide breakdown properties of modified RCA cleans is investigated. An (0.25/1/5) ratio of the SC1 mixture ($NH_4OH/H_2O_2/H_2O$) at 70°C is proposed as the best compromise between the particle removal efficiency and the silicon surface roughening effect occurring during this step. When clean chemicals are used the SC2-step ($HCl/H_2O_2/H_2O$) is not necessary to obtain good quality gate dielectrics. The waiting time of RCA-cleaned wafers in the cleanroom air before furnace loading was correlated with breakdown statistics. For wafers treated in contaminated chemicals a recovery of the gate oxide integrity was observed. The loading and ramp-up cycle before gate-oxidation in pure inert gas, was found to generate silicon surface roughening. Therefore, a mixture of inert gas and O_2 must be used during this processing step.

INTRODUCTION

In the MOS technology, metal contamination and silicon surface roughness are considered as two of the most important parameters which can cause defect-related breakdown of gate oxides. A good cleaning procedure should therefore be optimized not only to reduce particle densities, but also to yield acceptable metal contamination and surface roughness results. Up until recently, RCA-type pre-oxidation cleaning technologies have been widely used with reasonable success in obtaining good quality thermal oxides. During the last few years, the metal contamination has been reduced considerably by using chemicals with fewer metal impurities (i.e. down to the ppb level) and the research to improve the standard RCA clean has especially focused on the problem of Si surface roughening. The existence of a clear correlation between surface roughness of the Si substrate and defect-related dielectric breakdown was demonstrated by Heyns et al. [1] in the First International Symposium on Cleaning Technology in Semiconductor Device Manufacturing in October of 1989. During the last two years, considerable progress has been made to fully understand the causes and mechanisms of this effect. Moreover, improvements were proposed to reduce the Si surface roughening during the cleaning steps. In this paper some recent findings in this research area are presented.

THE RCA CLEAN

Surface Roughness :

A typical RCA-type cleaning sequence consists of two steps. The first step (referred to as SC-1) is used to reduce particle contamination and consists of a $NH_4OH/H_2O_2/H_2O$ mixture. The recommended

temperature in this bath varies between 70 to 90°C and the immersion time between 10 to 15 minutes. Originally a 1/1/5 mixture was proposed [2]. More recently, this SC-1 step was found to generate considerable silicon surface roughening [3] resulting in a degradation of the gate oxide integrity. Subsequently, a new mixture with an $NH_4OH/H_2O_2/H_2O$ ratio of 0.25/1/5 was proposed [4]. This ratio was suggested to be optimal in balancing the particle removal efficiency (which degrades with reduced NH_4OH) and the surface roughening behavior (which improves with reduced NH_4OH). The cleaning action of this mixture was explained by the hydroxyl groups from the basic solution which tend to negatively charge both the silicon surface and the particles [5]. The slow etching of the silicon in this mixture undercuts the particles which are then removed from the silicon surface by the repulsive Coulombic forces. These forces are also responsible for holding the particles in the solution. By increasing the NH_4OH concentration, the etch rate increases, thus increasing the particle removal efficiency. On the other hand, higher etch rates will enhance the Si surface roughening, thus resulting in an increase in the defect-related breakdown of thermal oxide layers. Consequently, the 0.25/1/5 mixture at 70°C was proposed as the best compromise between these two counteracting phenomena.

The changes in particle removal efficiency and surface roughening with varying NH_4OH/H_2O_2 ratio, is a very important issue when one wants to implement an improved SC-1 clean in a practical processing environment. In order to have optimum and reproducible results, the NH_4OH/H_2O_2 ratio should not vary drastically over time. This is difficult to obtain in practice since NH_4OH is very volatile, and at the same time, H_2O_2 can readily decompose into O_2 and H_2O [6]. To prevent outgassing of NH_4OH, we use always a cover plate in these experiments. The decomposition of H_2O_2 can only be retarded by lowering the temperature of the bath. Therefore a temperature of 70°C is chosen as a compromise between chemical activity and de-

composition.

Another problematic issue for the SC-1 clean is that the chemical oxide after this step is known to be easily contaminated with metals. It has already been shown that there is a direct correlation between the metals contained in the peroxide and the metal contamination on the silicon surface after the SC-1 step [7]. This can be explained by the fact that a chemical oxide is formed on the Si surface by the oxidizing action of the peroxide (which thereby incorporates all the metals within the peroxide solution in the chemical oxide) and the simultaneous etching of this chemical oxide by the NH_4OH. As a result an equilibrium between metals contained in the mixture and metals incorporated in the chemical oxide will result.

In summary, it is found that the SC-1 clean is successful in removing particles, but Si surface roughening and metal contamination in the chemical oxide can still be problematic issues.

Metal Contamination:

In order to obtain a lower metal concentration level on the a e Si surfacsecond step is normally applied in an RCA-type cleaning sequence. This step (referred to as SC-2) consists of a mixture of $HCl/H_2O_2/H_2O$ (1/1/5 ratio). Immersion time and temperature are typically the same as in the SC-1 clean. Variation of the HCl/H_2O_2 ratio was found to have only minor effects on the final metal contamination [8]. The HCl/H_2O_2 mixture has a negligible effect on the silicon (i.e. the Si surface etches at a very slow rate). Therefore, generally speaking, no additional Si-surface roughness results from this step. When very clean chemicals are used in the SC-1 step (with overall metal contents at the ppb level), performing the SC-2 step does not improve the breakdown properties of the gate oxide any further. This can be seen from the result of Fig. 1. In this figure the yield of capacitor structures, made on 15 nm thermally grown oxides, is plotted as a

function of chemical vendor used in a complete RCA-clean (SC-1 and SC-2). Yield is defined as the total percentage of capacitors surviving a breakdown field of 12 MV.cm^{-1}. At this field, typically the cross-over between defect-related and intrinsic breakdowns is observed in a Weibull plot.

The precise definition of yield and the details of the RCA-cleaning procedure are described in [7]. Six wafers having a total of 200 capacitors per wafer were measured for 2 capacitor areas (1.2E-2 cm^2 and 3.85E-2 cm^2), giving sufficient statistical validity. One can see from Fig. 1 that cleaning with chemicals of any of the 4 vendors results in almost identical gate oxide integrities. Note that the vendors used in this test are different from the ones tested in a previous publication (ref. [7]) and, on the average, were of lower metal impurity levels. In the same experiment, gate oxides were also grown on wafers which were only immersed in the SC-1 mixture. For these wafers the metal contamination of the chemical oxide present before the thermal oxidation directly reflects the metal concentration in the peroxide of the different chemical vendors. Capacitor structures were made on these wafers. The resulting breakdown properties are shown in (Fig 1b). A dramatic difference is seen between these results and the results obtained on the wafers which underwent the complete RCA-cleaning cycle (Fig. 1). The use of chemicals of vendor CC (with the highest metal content for certain specific metals in the peroxide) results in very poor breakdown statistics. In the case where chemicals of vendor DD are used (with a very low metal impurity content), the subsequent SC-2 mixture has only a minor effect on gate oxide integrity. The differences in breakdown properties between the results of Fig. 1a and b can be completely attributed to the metal contamination which is present on the wafers after the SC-1 step. From this, it can be concluded that, although the SC-2 step is not necessary when very clean chemicals are used, it makes the gate oxide integrity less sensitive to differences in the metal content of chemicals (at least

when these levels are below the low-ppb range).

It should be noted that the definition of "quality" for chemicals is not straightforward. In general the quality of chemicals is defined by considering the metal impurity content and particle concentration in the chemicals. However, it was demonstrated that these were not the only important parameters. There exists a surface roughening effect which differs between various chemical vendors [7] and which dominates the breakdown properties of the gate oxides when a complete RCA-clean is used (SC-1 and SC-2). When only a SC-1 clean is used, a combination of this roughening effect and metal contamination in the chemical oxide becomes the main cause of defect-related dielectric breakdown.

Recently S. Verhaverbeke et al. [9, 10] pointed out that various metals have a different impact on the gate oxide integrity. Metals such as Ca, Al and Fe were detected as being extremely important in causing defect related breakdown. Especially for the Ca contamination it was illustrated that its effect is to induce Si surface roughness when it is present on the silicon wafer during ramp up in the oxidation furnace.

THE HF-DIP PROCEDURE

Some metals on the Si surface can be removed by performing a HF-dip. The HF dissolves the chemical oxide, thus removing the metals which are incorporated in this oxide. In typical cases, a 0.5 to 2 % HF concentration at room temperature is used and the immersion times varies form 20 to 60 seconds. Two major problems can occur when using such a procedure. The first problem is particle addition to the Si surface after the HF-dip. This is due to the resulting hydrophobic silicon surface which is very reactive and can easily attract particles. A possible solution for this is the addition of small amounts

(in the order of 1 %) of H_2O_2 to the diluted HF [11]. Low particle densities can also be obtained after the HF-dip when appropriate rinsing and drying procedures are adopted. Nevertheless, the HF-dip procedure should still be considered as a critical processing step. It must be noted that gas phase HF-cleans are not effective in removing metals. Even though they dissolve the chemical oxide, the metallic contamination can not be effectively lifted off of the Si surface. A subsequent rinsing step can partially remove these metals, however it places a tremendous burden on reducing the particle densities. A second problem is the plating-out of noble metals on the silicon surface immersed in diluted HF. Copper, which is often a trace impurity in HF, is especially important in this respect. Even a small Cu content of 1 ppb in the HF can cause Cu to plate-out in the range of 1E11 to 1E12 atoms/cm^2 on the silicon surface [12]. Also in this case, an addition of H_2O_2 to the HF bath can reduce Cu outplating on the silicon surface [13, 14].

Hence, when the particle addition and Cu plating-out during HF-treatments can be avoided or reduced, a HF-dip can be recommended before gate oxidation. The Si surface after such a step is normally hydrogen passivated. On the other hand, hydrocarbons may be present on the silicon surface. The effect of this is largely unknown and the transport of wafers after the HF-dip to the oxidation furnace still has to be studied in more detail.

WAITING TIME EFFECTS

In a normal processing environment, the waiting time between the cleaning procedure and the loading of the wafers in the gate oxidation furnace is not always well controlled. Therefore, a series of experiments were designed to investigate this effect in more detail. After an RCA-clean, wafers were placed in Class-1 clean room air for waiting periods ranging from 0 to 4 hours before loading in the oxi-

dation furnace. Thermal oxides were grown to a thickness of 15 nm. Polysilicon capacitor structures were then made and the gate oxide integrity was evaluated. More details on the RCA cleaning procedure and the oxidation conditions used in these experiments can be found in [7]. Experiments were performed with chemicals from 4 different vendors. The wafers underwent an RCA-type cleaning using in each case only chemicals from one vendor. After cleaning, the wafers were split into 3 different batches. On one batch, the oxidation was performed immediately after the cleaning, the second batch experienced a waiting time of 2 hours between these steps, and the third batch a waiting time of 4 hours. It is important to note that under our experimental conditions, the wafers were protected during the waiting time by a chemical oxide which was formed during the RCA cleans. The average capacitor yield obtained on various wafers is shown in Fig. 2. A clear trend is observed towards improved breakdown statistics when the waiting time between the cleaning and the loading in the oxidation furnace is increased. Furthermore, it is remarkable that this effect depends strongly on the chemical vendor used in the cleaning treatment. For example when vendor A is compared with vendor D, it is seen that the effect is much stronger for the latter chemical supplier. The observation that the gate oxide quality improves when the waiting time between the cleaning and the furnace loading is increased is in contrast with what is intuitively expected.

Over various runs, it was generally observed that the waiting time effect is stronger for chemicals with higher overall metal contamination. This point was therefore investigated in greater detail. An experiment was performed where the cleans were done with the same chemicals as used to obtain the results shown in Fig. 1. The chemicals from vendor AA were the cleanest and were used as a reference. The chemicals from vendor CC showed some metal contamination and were treated as a typical example of slightly contaminated chemicals. Only an SC-1 clean was performed in these experiments since, in such cleans, the metal concentration of chemical oxide directly reflects the

metal impurity concentration of the chemicals. The average yield on gate oxide capacitors is shown in Fig. 2b. From the results it is clearly seen that the 'contaminated' chemicals of supplier CC cause a waiting time effect. When the oxide was grown directly after the cleaning, no large area capacitors were found to survive fields up to 12 MV/cm. A waiting time of 2 hours in clean room air in-between the cleaning and the gate oxidation, results in a slight recovery of the gate oxide integrity, although even in that case the yield is low. When wafers stayed 4 hours in the clean room a recovery of the gate oxide was noted. The clean chemicals of vendor AA did not show a waiting time effect. From this it is concluded that when a low metal content is present in the chemical oxide after the clean, no (or only a very small) waiting time effect is observed. When considerable amounts of metal contamination are present in the chemical oxide, the gate oxide integrity will improve upon waiting in-between the cleaning and the loading in the gate oxidation furnace.

As an explanation for these results, it is suggested that when a contaminated chemical oxide is present on the wafers, some contaminants which are deposited on the wafer from the clean room air can have a compensating effect. A common contaminant in clean room air is boron [15], which can be responsible for uncontrolled Vt-shifts of transistors. The amount of boron which can adsorb on the silicon surface during exposure to clean room air, is proportional to the exposure time. When a wafer with some metal contaminants in the chemical oxide and some boron contamination from the clean room air is placed in the oxidation furnace, a metal-boron complex can be formed during heating. This complex has an enhanced diffusivity into the silicon, as compared to the diffusivity of the metal itself. In this way, metals are removed from the silicon surface during the heating and are diffused into the bulk silicon. In Fig. 4 a pictural description of this phenomenon is shown. These metals can effect the minority carrier lifetime in the bulk, but will no longer contribute to the number of defect-related breakdowns. Therefore, the formation of such

boron-metal complexes will improve the gate oxide integrity. For Fe and Cu, two of the main contaminants which are sometimes observed in the chemical oxide after the SC-1 clean, the formation of such complexes has already been demonstrated [16, 17, 18]. The assumption that other metals can also form these complexes is very reasonable, since the driving force behind the formation of these complexes is the difference in the electronegativity between the boron and most transition metals (boron forms a negative center in silicon which attracts the positively charged metals).

In order to further lend support to the suggested model, a systematic survey of previous breakdown experiments was performed where gate oxides were grown on n-type and p-type wafers simultaneously under identical conditions. It was observed that there is a general trend towards improved breakdown statistics for the oxides grown on the p-type as compared to n-type wafers. The differences in yield which were observed varied from approximately 10 % up to 50 % in one specific case. In most cases where n-type layers were implanted in p-type material, no statistical difference could be found between the two types of wafers. This suggests that the presence of boron can lead to an enhanced diffusion of metals into the bulk silicon and an improvement in the gate oxide integrity.

PURE GASES IN OXIDATION SYSTEMS

A final step before gate oxidation is the loading of the wafers into the furnace and a ramp-up of the temperature of the furnace to the oxidation temperature. In this section of the paper we report on some experimental observations which illustrate that one should exercise caution when using ultra clean processing technology without complete knowledge of the underlying physical mechanisms, since in some special cases specific contaminants can be beneficial to the pro-

cess.

The aim of these set of experiments was to study what would happen with a silicon wafer when a conventional furnace tube was rebuilt so that loading and temperature ramp-up of the wafers could be performed in an ultra clean argon or nitrogen atmosphere containing trace impurities (i.e. in the ppb range). To this purpose, wafers were heated up in a closed RTP (Rapid Thermal Processing) system in an Ar ambient. In the RTP system, the partial pressure of O_2 and H_2O in argon was considerably lower (the estimated value for this experiment is 0.8 mTorr) than what can normally be achieved in conventional oxidation tubes (the estimated value for the experiment is 20 mTorr). It is well known that the infiltration of ambient air is more pronounced in conventional atmospheric furnaces. All of the wafers used in these experiments were RCA-cleaned. Half of these wafers were also subjected to an HF-dip. A set of wafers was then heated in pure Ar atmosphere in the RTP system. A second set was heated in the same RTP system but in a gas mixture containing Ar and 1 % O_2. A third set of wafers was loaded in a conventional oxidation tube, which then underwent a ramp-up cycle without oxidation. Before and after these various heating cycles, the haze of the wafers was measured with a Tencor Surfscan 4500 (average total in ppm, standard definition of the equipment). The haze number can be used as a parameter to describe the surface roughness of the wafer. The haze measured after the heating cycle gives a measure of the Si surface roughness induced during loading and ramp-up cycles in the different gaseous environments.

In Fig. 3 the haze (surface roughness) is plotted for RCA-cleaned wafers with and without a subsequent HF-dip. The 1-minute annealing treatments in the RTP system were done at temperatures ranging from 850 to 1200°C. The ramp-up to the desired processing temperature lasted only a few seconds. The process gases used were pure Ar (Fig. 3a) and a mixture of 1 % O_2 in Ar (Fig. 3b). In the conventional

oxidation furnace (Fig. 3b), equally prepared wafers were ramped up at a rate of 5°C/min in Ar to temperatures varying between 850 and 1000°C.

It can be observed that RCA-cleaned wafers which are heated in the RTP-system in an inert ambient (pure Ar-gas), are becoming very rough at anneal temperatures above 900°C. The maximum roughness is reached at a temperature of approximately 1050°C. Above this temperature, the roughness starts to decrease. On the other hand, initially, the HF-dipped wafers do not exhibit such a pronounced roughness effect. These surfaces begin to roughen at temperatures above 1000°C.

The temperature dependence of the Si surface roughening during heating in inert ambient can be explained by the decomposition of the chemical oxide on the RCA-cleaned wafers by the formation of voids [21]. At high temperatures, in ambients containing a low oxygen partial pressure, the following reaction takes place :

$$SiO_2(s) + Si(s) \rightarrow 2\ SiO(g)$$

This reaction is locally triggered by defects and removes the chemical oxide from the Si surface by the formation of voids. It is important to note that silicon is consumed during this reaction. As a result, large oxide-free regions are formed in locations where the silicon is strongly etched. This is the origin of the large increase in haze. When for a fixed anneal time the temperature is increased, larger voids are formed, ultimately leading to the emergence of an oxide-free silicon surface. In an effort to lower its free energy, this surface will tend to smoothen itself out during the high temperature anneal. Under our experimental conditions, this is observed for temperatures above 1100°C. The roughening of the silicon surface during the heating cycle is thus not induced by metal or other contamina-

tion, but simply by a chemical process involving the decomposition of silicon dioxide under conditions of high temperatures and low oxygen partial pressures. This process is, therefore, very sensitive to small variations in the oxygen partial pressure.

In the case of HF-dipped wafers, this roughening due to the oxide decomposition does not occur because little, or no, chemical oxide is present. The roughening which is observed above 1000°C, can be attributed to the formation of silicon carbide at this high temperatures [19, 20]. The origin of this effect is the hydrocarbon contamination which is often observed on HF-dipped samples (see Fig. 5). When the silicon wafer is heated up, the hydrogen-silicon bonds will be broken and hydrogen is released from the silicon surface. Some hydrocarbons have a stronger bond with silicon and are stable at high temperatures. Once above 1100°C, this can lead to the formation of siliconcarbide. In ref. [20] such a model was proposed to explain the siliconcarbide clusters, measured with high resolution transmission electron microscopy, after heating of HF-dipped wafer in an oxygen-free ambient.

When small amounts of oxygen (1 %) are added to the ambient during the heating cycle (Fig. 3b), no roughening of the wafers is observed. This is due to the fact that, not only the oxide decomposition reaction does not occur, but fresh thermal oxide layers are grown on the silicon surface as well. The oxide thickness after the RTP step, as measured with spectroscopic ellipsometry, on the RCA-cleaned wafers was found to vary between 1.7 and 5.3 nm for anneal temperatures of 850 and 1200°C, respectively. The oxide on the HF-dipped wafer was only 0.3 nm thinner after the RTP-step. The growth of this thin oxide layer during the heating protects the silicon surface from being etched in the inert ambient and, therefore, no Si surface roughening occurs. For the HF-dipped wafers, the silicon carbide formation is inhibited by the formation of gaseous carbon oxides (CO and CO_2) [20]. For these wafers, no roughness increases occur during heating in

an oxygen containing environment.

Similarly, as for the experiments in standard horizontal furnace (Fig. 3b), no roughening is observed after a thermal cycle in pure argon. This can be attributed to the fact that in standard horizontal furnaces, unless special precautions are taken, ambient air infiltration is high enough to result in substantial oxygen partial pressures in the inert annealing ambient, thus avoiding the problems of oxide decomposition and silicon carbide formation. This effect has to be taken into account when a standard furnace is upgraded to handle ultra-pure gases. In most cases, after these improvements (which are mostly in the form of improved sealing capabilities), oxygen has to be deliberately introduced in the furnace ambient during heating cycles to prevent the roughening of the silicon surface, and subsequently the degradation of the oxide breakdown properties. In addition to this surface roughening, which is a chemical reaction of silicon oxide in an inert environment at high temperatures, specific metal contaminants on the silicon wafers can also introduce Si-surface roughening by another mechanism [9, 10].

CONCLUSIONS

Some improvements of the pre-oxidation cleaning technology were proposed. When a (0.25/1/5) ratio is used for the SC1 mixture ($NH_4OH/H_2O_2/H_2O$) at 70°C of the RCA-clean a good compromise is obtained between the particle removal efficiency and the silicon surface roughening effect. This roughening effect was demonstrated to vary between the chemicals from different vendors. When very pure chemicals are used the SC2-step ($HCl/H_2O_2/H_2O$) can be omitted. The effect of the waiting time of RCA-cleaned wafers in the cleanroom air before furnace loading on the breakdown statistics was investigated. When wafers cleaned in contaminated chemicals are placed in the clean room a recovery of the gate oxide integrity was

observed during this waiting time. A boron-metal complexing model was proposed to explain the experimental observations. The loading and ramp-up cycle before gate oxidation in pure inert gas was investigated. A relationship between annealing in inert ambients and silicon surface roughening was observed, which can be related to SiO void formation Therefore, a mixture of inert gas and O_2 must be used during the pre-oxidation heating.

ACKNOWLEDGMENTS

Digital Equipment Corporation and Wacker-Chemitronic are greatly acknowledged for financial support of this study. Ann Opdebeeck and Marc Dulst, Marc Van Dievel and Bruno Knuts are acknowledged for technical assistance.

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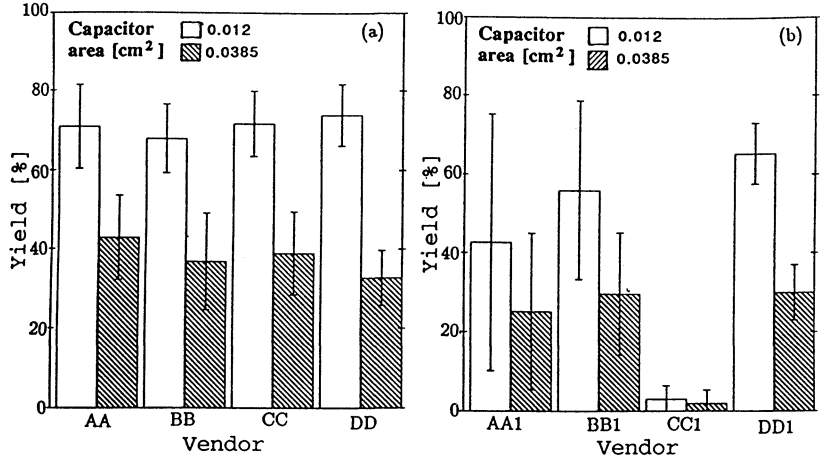

Figure 1: Yield of capacitor structures cleaned with chemicals from different vendors before gate oxidation. (a) SC1 + SC2 mixture clean; (b) SC1 mixture clean.

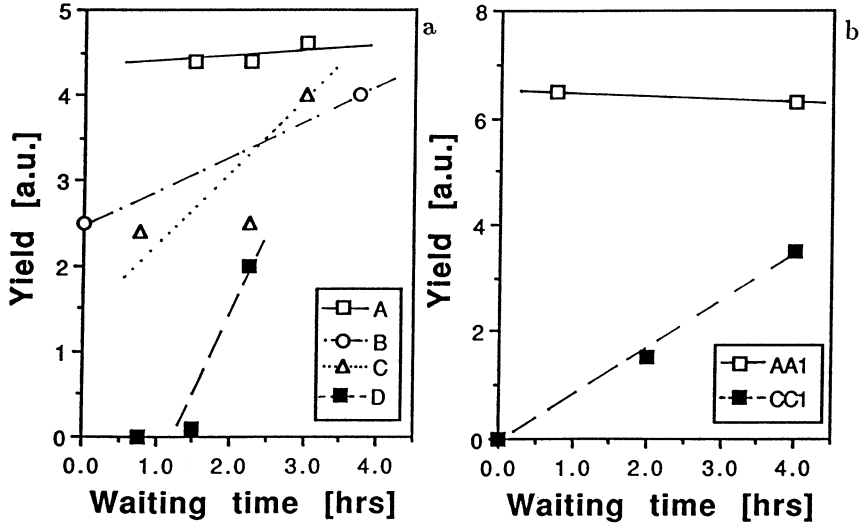

Figure 2: Yield of capacitor structures cleaned with chemicals from different vendors as a function of waiting time in the cleanroom before gate oxidation. (a) RCA-clean for 4 different chemcial vendors; (b) SC1-clean for 2 different chemicals, AA: "clean" CC : "contaminated".

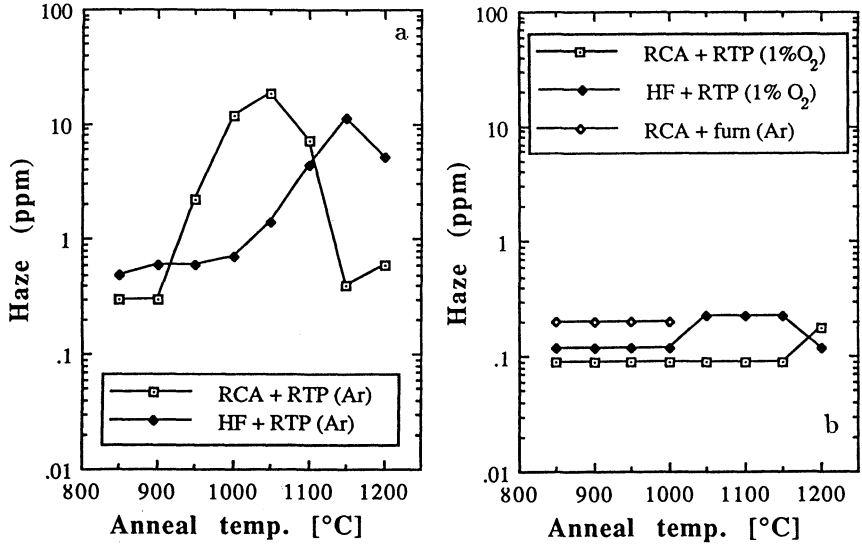

Figure 3: Haze (in ppm, measured in a Tencor Surfscan) as a function of annealing temperature for RCA-cleaned and HF-dipped wafers. (a) RTP for 1 minute in pure Ar-gas; (b) RTP for 1 minute in a mixture of 1 % O_2/Ar-gas compared with ramp-up in Ar-gas in a classical furnace tube (RCA + furn).

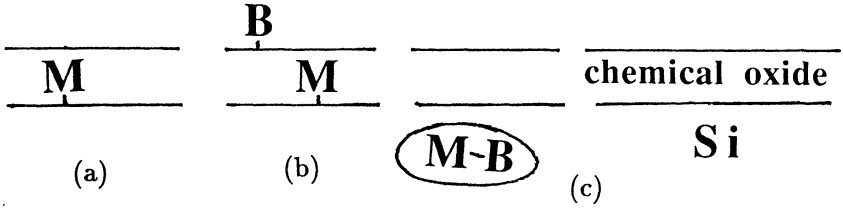

Figure 4: Pictural description of the boron-metal complexing model: (a) metal (M) present in the chemical oxide; (b) boron (B) comes on the wafer from the cleanroom air; (c) M and B diffuse into the silicon to form a B-M complex.

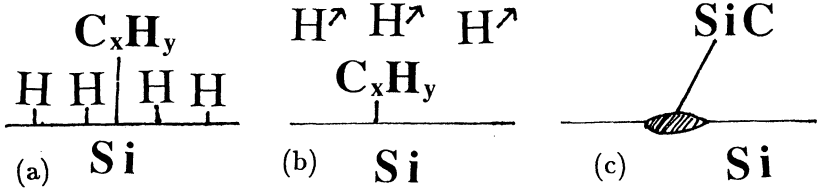

Figure 5: Pictural description of the siliconcarbide formation after heating of HF-dipped wafers in inert ambient: (a) hydrogen passivated silicon surface with some hydrocarbons after HF-dip; (b) when heating up hydrogen evaporates, leaving some hydrocarbons on the surface ; (c) at high temperatures siliconcarbide is formed.

THE EFFECT OF SC1 CLEANING OF THE SURFACE MICROROUGHNESS OF P+ AND P- SILICON WAFERS

Saeed Pirooz, Jose C. Coria-Garcia, and Larry W. Shive

MEMC Electronic Materials Company, Inc.
501 Pearl Drive, P.O. Box 8
St. Peters, Missouri 63376

ABSTRACT

As LSI has developed higher pattern density, surface defects and trace impurities have become severe problems for device manufacturing yield and reliability. In this paper we have investigated the effect of SC1 chemistry on the surface micro-roughness, or so called haze, of P+ and P- silicon wafers. We also studied the effectiveness of an automatic wafer inspection system, Censor ANS-100, for the surface micro-roughness measurements. Time of immersion and the ratio of ammonium hydroxide/hydrogen peroxide concentrations were found to be the major contributors to surface roughness. Whole wafer surface roughness measurement is essential to understanding the effect of cleaning steps on surface microroughness.

INTRODUCTION

An ammonium hydroxide, hydrogen peroxide mixture in RCA cleaning is mainly used for its excellent efficiency for the removal of particles. However, it has been shown that wafer surface roughness which appears as a so-called haze develops on the surface of the wafer. This is due to the fact that SC1 chemistry slightly etches the silicon surface. Thus, increased wafer roughness or haze is one of the consequences of this process [1].

Wafer surface roughness is gaining an increasing importance because of its effect on the electrical properties of very thin gate oxide films [2] and on the fine pattering of high aspect - ratio contact holes [3] in the ULSI manufacturing. Therefore, for the production of ultra-clean wafers, it is imperative to address the surface smoothness of the wafers in addition to the control of the particles and contamination [4]. The following items are important factors for improvement of the SC1 cleaning process to minimize the surface roughness.

1) Optimization of the concentration of NH_4OH and H_2O_2.

2) Accurate measuring of the surface micro-roughness or haze.

In this paper, we describe the effect of $NH_4OH/H_2O_2/H_2O$ ratio, in SC1 cleaning process, on the surface roughness of P+ and P- wafers. We also present the results of our evaluation of an automatic wafer inspection system, CENSOR ANS-100, for measurement of Si surface roughness.

EXPERIMENTAL

Five inch diameter, lightly boron doped P- type <100> wafers, with a resistivity of 30-60 Ohm-cm and five inch, heavily doped P+ type <100> wafers, with a resistivity of 0.003-0.010 Ohm-cm were used in our experiments. The wafers were obtained from the Czochralski crystal process and were cleaned by a modified RCA cleaning process [5]. None of the wafers were especially treated to remove any sub-surface polishing damage. NH_4OH and H_2O_2 were purchased from Ashland Chemical Co. Eighteen mega-Ohm DI water was employed in all solutions and rinsing processes.

A full factorial experimental design was followed. The NH_4OH-H_2O_2-H_2O concentrations were varied from the low of 0.01% (V/V) NH_4OH and 0.01% (V/V) H_2O_2 to the high of 10% (V/V) NH_4OH and 10% (V/V) H_2O_2. Temperature in the baths was kept constant at 80 degrees C. The immersion time in each of the cleaning solutions was a low of 5 minutes and a high of 60 minutes.

The surface micro-roughness before and after cleaning was evaluated using five different instruments. These instruments were: MEMC hazemeter, Atomic Force Microscopy (AFM from Park Scientific Instruments), two different noncontact surface profilers (WaferMax Noncontact Profiler from Zygo Corporation and TOPO 3-D Noncontact System from WYCO Corporation), and an automatic wafer inspection system (CENSOR ANS-100).

RESULTS AND DISCUSSION

The influence of various ratios of NH_4OH/H_2O_2, and various immersion times on the surface micro-roughness of both P+ and P- Si wafers was investigated. General trends observed on different instruments were in good agreement. As suggested (1), surface roughness increases with increasing NH_4OH/H_2O_2 concentration ratio, and with increasing time. Figure 1 shows the AFM images (PSI) for the p+ wafers. The image of the untreated wafer is shown in Figure 1a. Figure 1b shows the AFM image of the wafer after it was treated at the low (0.01%) concentrations of NH_4OH and H_2O_2. Figure 1c shows the wafer which was treated at high concentrations (10%) of ammonia and peroxide for sixty minutes. As it is indicated from the AFM images, the surface roughness increases with longer time. Figure 2 shows the contrast, for etched back wafers, between light concentration of NH_4OH (0.01%/0.01%) and short time (5.0 minutes) vs. high concentration (10.0%/10.0%) and long time (60 minutes), in 3-D images from a noncontact profilometer, (Zygo WaferMax Noncontact Profiler). Here, the surface roughness agrees well with the AFM results.

A sample of the haze maps obtained with the CENSOR ANS-100 is shown in Figure 3. As illustrated, Censor produces full wafer microroughness maps. The advantage of whole wafer mapping versus single point, small field of view sampling of the previously mentioned methods is obvious. Patterns of rougness become clear as does the high variability within a single wafer. The differences in haze data before and after the etching of the wafers in the $NH_4OH/H_2O_2/H_2O$ solutions are presented in Figures 4 and 5.

Although, general roughness increased for p+ and p- wafers in all the SC1 solutions, the results shown in Figure 4 suggest that the increment of roughness is dependent on the exposure time of the wafers. For example, a p+ wafer exposed 60 minutes to a solution of 0.01% / 0.01% (V/V) of NH_4OH/H_2O_2 shows an increase in roughness of four times that of the p+ wafer exposed to the same solution for 5 minutes. A similar behavior is observed for p- wafers.

It is observed from Figures 4 and 5, that the degree of roughness is higher for concentrations of 0.01% peroxide than for concentrations of 10.00% peroxide, independent of the ammonium hydroxide concentration. These later results suggest

that a low peroxide concentration does not quench the etching process by the ammonium hydroxide under the present experimental conditions.

Results from Figure 5 show that for an exposure time of 5 minutes the overall roughness of p+ and p- wafers was equivalent. However, the overall roughness of p+ wafers is higher than that of p- wafers for an exposure time of 60 minutes. This behavior contradicts the fact that the etch rate of p- wafers is higher than that of p+ wafers in basic solutions. Keeping in mind that surface roughness and etch rates are independent phenomenona, the above results led us to believe that, although, p+ wafers etch slower, their surface becomes rougher than p- wafers over a prolonged period of time. The exact cause of this roughness is still under investigation.

Another noteworthy observation is that the uniformity of the roughness of p- wafers across the wafer changes moderately between 5 and 60 minutes exposure time, as compared to p+ wafers. The p+ wafer's roughness pattern changes dramatically with immersion time. Future studies in this area will comprise a detailed spectrochemical characterization of the p- wafer surface in the presence and absence of ammonium hydroxide.

CONCLUSIONS

We experimentally proved that the concentration of NH_4OH and the immersion time in SC1 cleaning process have a marked impact on the surface micro-roughness of the Si wafers. As ratio of NH_4OH/H_2O_2 and immersion time increased so did the surface roughness. Yet, at prolonged time, this effect was more pronounced for the P+ wafers than for the P- wafers. We also examined the effectiveness of an automatic wafer inspection system, CENSOR, in measuring surface micro-roughness. The results were very promising, as the obvious benefit of measuring particles and whole wafer surface roughness on the same wafer inspection system is overwhelming.

ACKNOWLEDGEMENTS

The authors would like to thank Censor Inc., Zygo Corporation, Park Scientific Instruments and WYKO Corporation for providing

sample analysis. We would also like to thank K. Lamb and D. Van Tassel.

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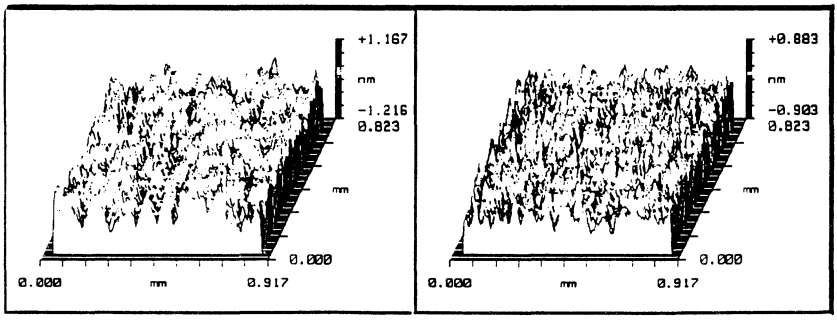
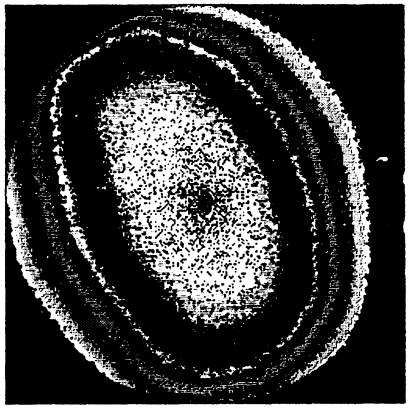
(a) (b) (c)

Fig. 1: Surface roughness of P+ silicon wafers with varied [NH_4OH] and time. (a)AFM image of the untreated wafer, (b)AFM image of the lightly treated SC1 for 5 minutes, (c) AFM image of heavily treated SC1 for 60 minutes.

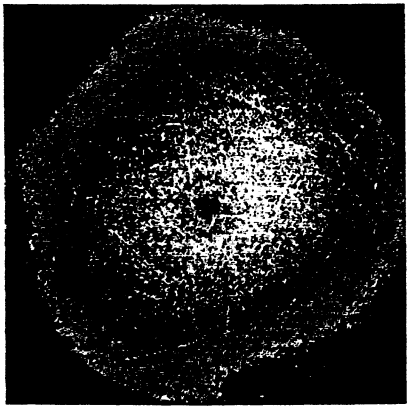


(b) (a)

Fig. 2: Profiles of P- wafers obtained from a 3-D non-contact profilometer. (a) light SC-1 for 5 minutes, (b) heavy SC-1 for 60 minutes.



(a)



(b)

Fig. 3: Whole wafer surface micro-roughness maps. (a) map of an untreated wafer, (b) map of a heavy SC-1 treated wafer.

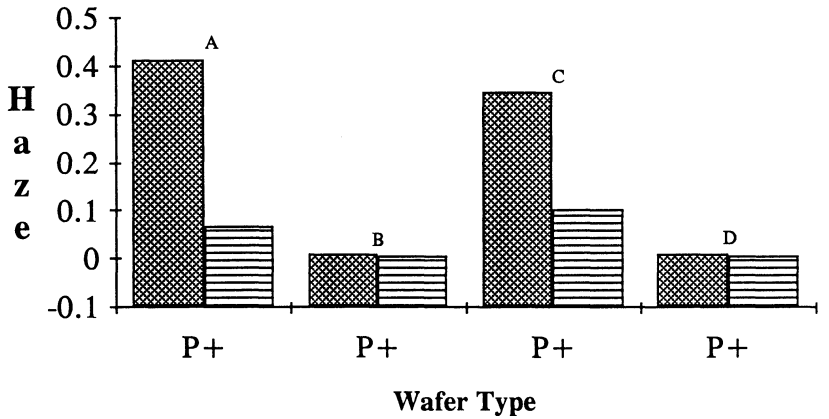


Fig. 4: Comparison between surface roughness values for P+ wafers under four different conditions. [NH_4OH]/[H_2O_2] concentrations for the conditions were: A, 0.01%/0.01%; B. 0.01%/10%; C. 10%/0.01%; D. 10%/10%. Dark bars represent immersion time of 60 minutes and light bars are for 5 minutes.

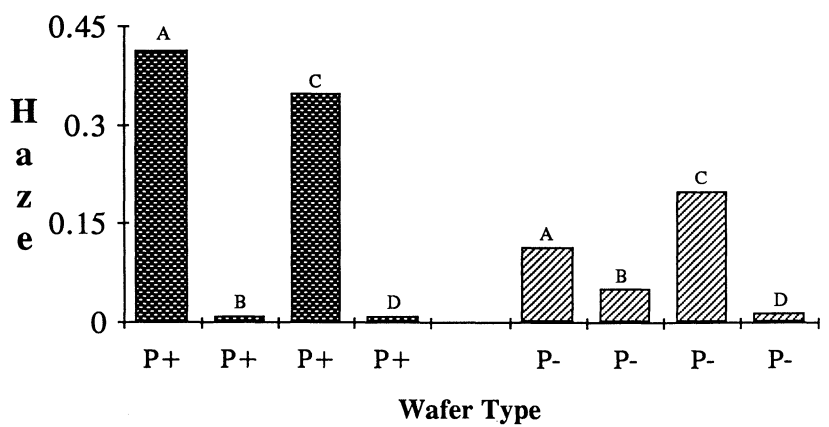


Fig. 5: Delta of surface roughness values for P+ and P- wafers for the immersion time of 60 minutes. [NH_4OH]/[H_2O_2] concentrations for the conditions were: A, 0.01%/0.01%; B. 0.01%/10%; C. 10%/0.01%; D. 10%/10%.

DEPOSITION CHARACTERISTICS OF TRANSITION METAL CONTAMINANTS FROM HF-BASED SOLUTIONS ONTO WAFER SURFACES *

Eugene Hsu, Harold G. Parks, Robert Craigin
Department of Electrical and Computer Engineering
University of Arizona
Tucson, AZ 85721

Scott Tomooka **, John S. Ramberg
Department of Systems and Industrial Engineering
University of Arizona
Tucson, AZ 85721

Robert K. Lowry
Harris Corporation
P.O. Box 883
Melbourne, FL 32901

Metal contamination levels are a concern in integrated circuit manufacturing because they degrade electrical performance. This work uses statistical design of experiments to determine deposition characteristics of transition metal contaminants onto silicon surfaces from process chemicals that are used in wafer cleaning. Copper, gold, molybdenum, silver, lead, chromium, tin, titanium, manganese, and tungsten were added to BOE and HF solutions. Wafers were immersed in these solutions and evaluated by TXRF surface analysis.

INTRODUCTION

It is well known that presence of transition metals can degrade the electrical performance of solid state devices. Metal impurities can create generation-recombination centers in silicon that increase reverse-bias junction leakage (1). Metal impurities have also been found to affect oxide breakdown strength and metal-oxide-semiconductor (MOS) capacitor leakage by dislocation decoration and stacking fault formation (2 & 3). Degradation of device performance can adversely affect circuit function of ULSI circuits including advanced dynamic RAM cells (4).

Sources of these trace contaminants include the process equipment, process materials, and even process chemicals used in wafer cleaning operations (3). Stainless steel in process equipment can introduce ion contamination from its constituent iron, chromium, and nickel atoms, especially through mechanical wear. Novel processes, incorporating advanced interconnect materials, can also introduce transition metal contaminants. Process chemicals in use today are quite pure, depending upon the grade used, but can easily be contaminated through improper handling or storage techniques. Because metal contamination can come from several sources, it is important to know what levels of conta-

* This research was sponsored by SEMATECH under contract 88-MC501.
** Now with Honeywell Inc., Phoenix, AZ.

mination are low enough to be acceptable for a particular application and how effective the wafer cleaning solutions are. The effectiveness of a given cleaning process may depend upon several factors including type of metal species, solution chemistry, condition of the wafer surface, and rinsing/drying procedures.

HF-based immersions have long been used for patterning, etching, and cleaning of silicon device surfaces (5). Their use in wafer cleaning for advanced processes is increasing, especially before the critical gate oxidation for MOS devices. This paper discusses investigation of the deposition characteristics of transition metal ion contaminants from HF-based solutions onto silicon wafer substrates.

OBJECTIVE

Given various levels of a contaminant in a solution, one would like to predict the contaminant's surface concentration on a wafer processed in that solution. Thus, the objective of the deposition experiments is twofold:

1) Determine *which* transition metal contaminants deposit from various solutions onto silicon wafer surfaces under specific conditions. Identify contaminants in a general way by order of magnitude differences over a wide range of solution concentrations, rather than minute differences in response.

2) Establish *empirical models* for contaminants shown to deposit under specified conditions. Relate metal contamination levels in those solutions (in ppb) with the surface level contamination (in surface densities) on wafers that have been immersed in them through multi-level experiments.

To accomplish this twofold objective, the experiment was conducted in two sequential phases.

APPROACH

Experimental design facilitates the study of many factors in one experiment, thereby increasing the amount of information obtained. Phase I, designed to identify contaminants that deposit onto wafer surfaces, utilized a 2^{8-4} fractional factorial design to estimate the main effects of independent and their two-factor synergistic interactions (Table III). This is a resolution IV design, which permits estimation of main effects independent of their two-factor interactions (6). However, while the effect of two-factor interactions may be estimated, the alias pattern is complex.no main effects are aliased with each other or any two-factor interactions.

One factor was solution type. The solution types used were 5:1 hydrofluoric acid (HF) and 9:1 buffered oxide etchant (BOE or BHF) with trace surfactant. Various concentrations of HF solutions such as these are often incorporated in cleaning processes, especially those prior to the critical gate oxidation.

The remaining seven factors were contaminants. Contaminant choices were based upon many factors including presumed likelihood of their deposition, theoretical trap levels in silicon, and their presence in the fabrication process. Copper and gold were investigated at 25 and 250 ppb levels in the solutions, while chromium, tungsten, lead, molybdenum, and titanium were added at 250 and 2500 ppb levels. In a two-level fractional factorial design, each factor is studied at two levels in a balanced manner. Copper and gold were examined at lower concentrations because of anticipated strong deposition tendencies (7 & 8). Other contaminant levels were set at higher concentrations to improve the chances of observing a response above the detection limits of current surface analysis technology. Notice that all contaminants were added to each of the experimental runs at either a high or low level. Such a situation (in which many metal impurities are present) might arise in an actual process as the result of cumulative contamination from multiple sources and from metal alloys used in equipment or processes. A statistical design such as this provides increased efficiency by examining many factors in one experiment. It can also identify synergism between main effects that might otherwise be overlooked in more conventional experiments.

The wafers used were <100> with a 15 – 25 Ω-cm As-doped epitaxial layer. The wafers for each experimental run were placed in a cassette, immersed in the contaminated acid bath for 60 seconds, cascade-rinsed in deionized (DI) water for 30 seconds, and dried with nitrogen. Surface analysis of the wafers was performed by total reflection x-ray fluorescence (TXRF), a non-destructive technique with detection limits that can approach 10^{10} atoms/cm^2 under optimum conditions (9 & 10). Contaminant concentrations in solutions were verified by inductively coupled plasma (ICP) spectrometry.

Phase II experiments (Table II) were designed to investigate the deposition characteristics of metal contaminants that were identified by Phase I as exhibiting strong deposition tendencies. With a factorial design similar to the one in Phase I, copper and molybdenum were each investigated at four levels. These four levels were created by combining two separate two-level columns of the fractional factorial design and their corresponding interaction column. The levels chosen — 50, 100, 200, and 500 ppb — correspond to levels 1, 2, 3, and 4 in Table II. These levels are approximately equally spaced on a logarithmic scale. Solution type was retained as a factor, using 19:1 HF and the same 9:1 BOE with surfactant. Three additional factors were included in the study at two levels each. Silver, manganese, and tin contaminants were added at 100 and 1000 ppb levels to determine whether or not they would deposit onto wafer surfaces.

RESULTS

The two-level Phase I experiment was primarily intended to identify contaminants that deposit. Hence, only surface concentration differences of at least an order of magnitude were considered significant. Results of Phase I indicate that copper and gold deposit in either solution in proportion to their respective concentrations. Molybdenum appeared to deposit in proportion to the amount of copper present. Lead indicated some deposition, but spectral interferences may account for this response. Chromium at high concentrations was barely detectable (in the 10^{10} atoms/cm^2 range); better TXRF analysis conditions would be necessary to confirm that it deposits. Titanium, with a detection limit of about 10^{10} atoms/cm^2, did not appear on most of the wafers. Tungsten did not deposit above the detection limits, which were in the upper 10^{12} atoms/cm^2 range.

Much of the literature regarding metal contaminant deposition presents the data on logarithmic scales because the data contaminant levels studied are orders of magnitude apart. The copper and molybdenum levels in our experiment were set close enough to plot on either a natural or log scale. The deposition data from Phase II plotted on a natural scale clearly indicates that on a natural unit scale, the response variability increases with response mean, as anticipated (figure 1). The same data plotted on a log scale displays more uniform data variability with increasing response mean (figure 2). This indicates that logarithmic transformation of the response is in fact the proper method for modeling the deposition characteristic.

For the Phase II copper response, four measurements with undetected response were identified as outliers. These outliers consisted of two measurement locations per wafer from each of the two wafers that were processed in one particular run. The consistent results of those four measurements suggest that misprocessing of the run, rather than process chemistry, explains that variability. The standard deviation of the log of the Phase II copper response on two locations measured across a wafer is 0.06; the standard deviation between two wafers from the same run (excluding the nested variability across a wafer) is 0.09. Thus, the deposition was relatively homogeneous across a wafer. Least-squares regression analyses of Phase II results indicate that copper deposits onto wafer surfaces in a linear characteristic with respect to solution concentration over the 50 to 500 ppb contaminant range (figure 3). Solution type was also identified as a significant factor in copper deposition. The presence of other factors did not have an effect on the copper deposition. Figure 4 shows the deposition model in figure 3 converted back to natural units. This deposition model predicts copper *surface density* from copper *solution concentrations* by these equations:

$$\text{HF: } \text{Cu [atoms/cm}^2\text{]} = 3.16 * 10^{11} * (\text{ Cu [ppb] })^{1.0} \quad [1]$$

$$\text{BOE: } \text{Cu [atoms/cm}^2\text{]} = 2.00 * 10^{11} * (\text{ Cu [ppb] })^{1.0} \quad [2]$$

This model has an R^2 of .93, indicating that the model accounts for 93% of the variation in the sample data.

Molybdenum deposits but not in proportion to its presence in solution. Silver was also identified as a contaminant that deposits. Both molybdenum and silver deposition appear to depend on presence of some of the other factors and possibly multi-factor interactions. In fact, both enhancement effects and inhibitory effects were observed in Phase II results. Manganese did not deposit above its detection limit of 3×10^{10} atoms/cm^2. Tin results were not interpretable due to unexpected TXRF spectral interferences. Results of both Phase I and II contaminant deposition experiments are summarized in Table III. Detailed characterization of these results including investigation of synergistic effects is currently in progress and will be reported in future publications.

CONCLUSIONS

These experiments have examined deposition of ten transition metal contaminants that could be present in a fabrication process and that may have detrimental effects on semiconductor devices. Copper, gold, molybdenum and silver were identified as contaminants that deposit from BOE and HF.

Empirical models, which account for differences in copper surface density based upon solution type and contaminant concentration, have been formulated.

The information from these deposition experiments is useful for determining chemical purity levels necessary to minimize device degradation. By identifying which elements are most critical for process chemical purity, this information can also focus efforts in the semiconductor and the chemical industries where they are needed most.

ACKNOWLEDGEMENTS

The authors wish to thank Mr. Steve Slasor of Harris Corporation for his ICP analysis.

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Run	Cu	Au	Cr	W	Pb	Mo	Ti	Solution
1	–	–	–	–	–	–	–	HF
2	+	–	–	–	–	+	+	BOE
3	–	+	–	–	+	–	+	BOE
4	+	+	–	–	+	+	–	HF
5	–	–	+	–	+	+	+	HF
6	+	–	+	–	+	–	–	BOE
7	–	+	+	–	–	+	–	BOE
8	+	+	+	–	–	–	+	HF
9	–	–	–	+	+	+	–	BOE
10	+	–	–	+	+	–	+	HF
11	–	+	–	+	–	+	+	HF
12	+	+	–	+	–	–	–	BOE
13	–	–	+	+	–	–	+	BOE
14	+	–	+	+	–	+	–	HF
15	–	+	+	+	+	–	–	HF
16	+	+	+	+	+	+	+	BOE

Table I. Phase I experimental design. For Cu and Au, '–' and '+' levels correspond to 25 and 250 ppb. For all other contaminants, '–' and '+' levels represent 250 and 2,500 ppb.

Run	Cu	Mo	Ag	soln	Mn	Sn
1	1	1	-	HF	-	-
2	2	1	-	BOE	+	+
3	3	1	+	HF	+	+
4	4	1	+	BOE	-	-
5	1	2	+	BOE	+	-
6	2	2	+	HF	-	+
7	3	2	-	BOE	-	+
8	4	2	-	HF	+	-
9	1	3	+	BOE	-	+
10	2	3	+	HF	+	-
11	3	3	-	BOE	+	-
12	4	3	-	HF	-	+
13	1	4	-	HF	+	+
14	2	4	-	BOE	-	-
15	3	4	+	HF	-	-
16	4	4	+	BOE	+	+

Table II. Phase II experimental design. For Cu and Mo, levels 1 through 4 represent 100, 200, and 500 ppb concentrations. For Ag, Mn, and Sn, '–' and '+' levels represent 100 and 1000 ppb levels.

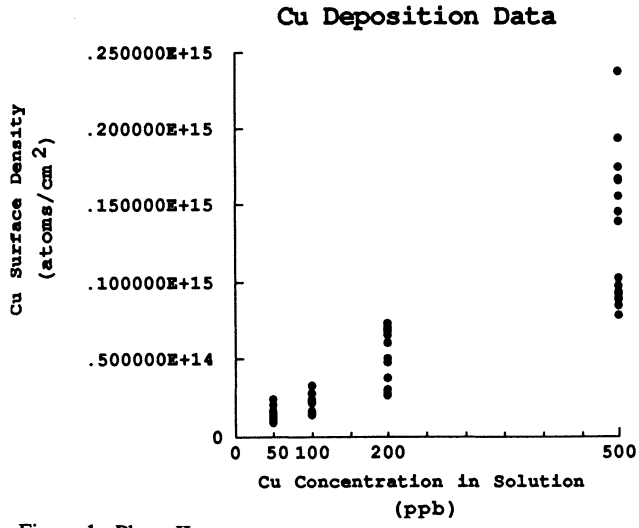

Figure 1: Phase II copper response measured by TXRF on natural scales.

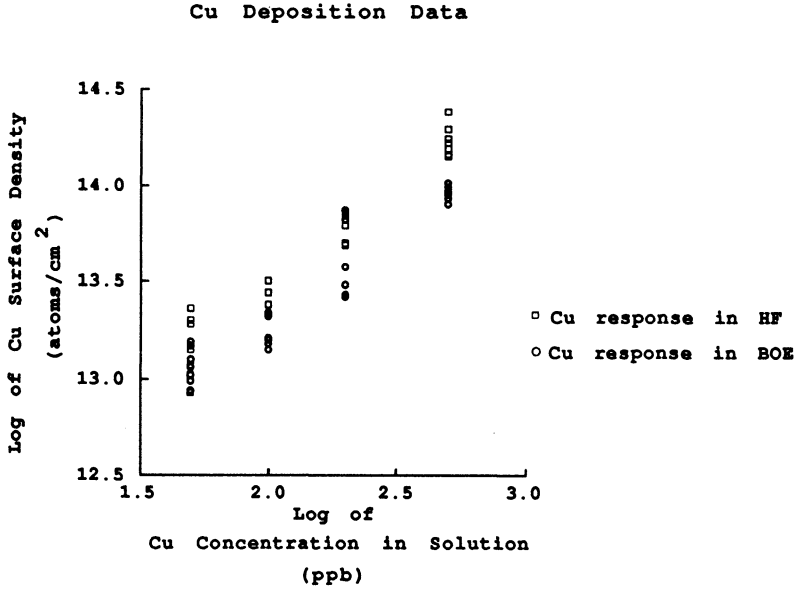

Figure 2: Log of Phase II copper response measured by TXRF.

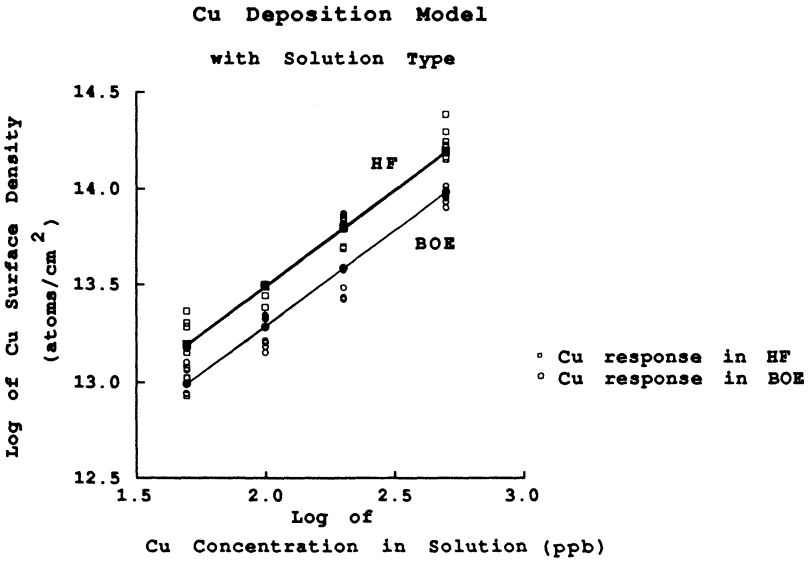

Figure 3: Copper deposition model and data, on logarithmic scales.

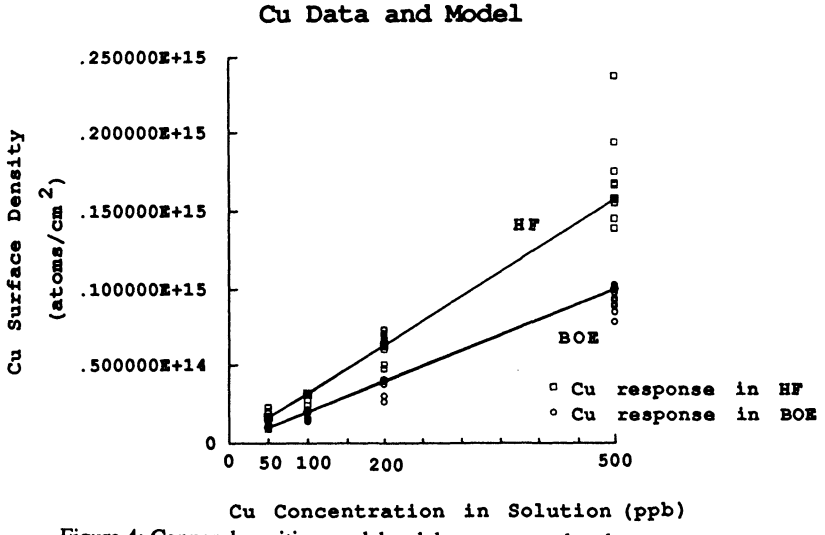

Figure 4: Copper deposition model and data, on natural scales.

Contaminant	Solution Concentration Range (ppb)	Deposits?	Detection Limit (atoms/cm^2)	Factors
Copper	50—500, 25—250	yes	~10^{10}	Cu, Solution type
Gold	25—250	yes	~10^{10}	Au
Molybdenum	50—500, 250—2500	yes	~10^{11}	Cu
Silver	100—1000	yes	~10^{11}	Ag, Sn, Solution type, & some of their interactions
Manganese	100—1000	no	~10^{10}	n/a
Titanium	250—2500	no	~10^{10}	n/a
Tungsten	250—2500	no	upper 10^{12}	n/a
Chromium	250—2500	uncertain	~10^{10}	n/a
Lead	250—2500	uncertain	n/a	n/a
Tin	100—1000	uncertain	n/a	n/a

Table III. Results summary of the two deposition experiments.

METAL CONTAMINATION REMOVAL ON SILICON WAFERS USING DILUTE ACIDIC SOLUTIONS

O.J. Anttila* and M.V. Tilli
Okmetic Ltd.,
Sinimäentie 12,
SF-02630 Espoo, Finland
(* present address: Department of Electrical Engineering,
Stanford University, Stanford, CA 94305)

Several acids as very dilute (1:100 - 1:10^6) water solutions were tested to remove metallic contaminants on silicon wafers. TXRF, DLTS and minority carrier recombination lifetime measurements were used to characterize the removal efficiencies. The resulting surface concentrations for iron were well below the 10^{10} at/cm^2 level for most solutions. The particle levels were low, comparable to an SC-1 clean. The minority carrier bulk lifetimes were in excess of 100 μs for the oxidized acid cleaned wafers, except to the dilute hydrofluoric acid cleans. Iron was found to be the dominant lifetime shortening contamination for concentrations larger than 10^{11} at/cm^3.

INTRODUCTION

The RCA solutions are commonly used for cleaning silicon wafers during IC manufacturing processes. There are, however, some drawbacks in their properties: The SC-1 solution (hot ammonium hydroxide - hydrogen peroxide - water solution; also known as 'APM') leaves the surface particle free, but there may be a considerable deposition of iron, zinc and aluminum on the wafers (1-3). On the other hand, the SC-2 solution (hot hydrochloric acid - hydrogen peroxide - water solution, also known as 'HPM') removes those metals to low levels, but there is a significant increase in the particle counts (2,4). A sequence composed of an SC-1 clean to remove particles, followed by a very dilute acid, e.g. 1 part of HCl in 10^4 parts of DI water to remove metals, seems to perform considerably better than a standard RCA clean.

EXPERIMENTAL

The material used was 125 mm P100 material, the resistivity being about 30 Ωcm. The material was freshly polished without any final clean. The wafers were first cleaned using a modified RCA clean. The last step was an efficient particle removing APM clean. The wafers were then transferred wet into a tank containing the diluted acid solution, kept there for a predetermined time interval, rinsed in a dump rinse tank and dried in a rinsedryer. The particles larger than 0.3 μm were counted using an automatic laser inspection equipment (Estek WIS-800).

Altogether, 16 cassettes, 24 wafers in each cassette, were cleaned. 5 sample wafers were taken out of each cassette, of which 3 wafers were for minority carrier lifetime (a laboratory equipment based on microwave reflection

technique at about 24 GHz) and DLTS (Deep Level Transition Spectroscopy, Semitrap DLS-82E) measurements, and 2 wafers for VPD-TXRF (Vapor Phase Decomposition Total Reflection X-Ray Fluorescence, Atomika XSA 8000 at GeMeTec GmbH) analysis.

The acids used for the final cleans were hydrochloric acid (37 %), hydrofluoric (50 %), nitric (70 %), and acetic (100 %) acids, in dilutions ranging from 1:100 to $1:10^6$ for HCl, and dilutions of $1:10^3$ and $1:10^5$ were used for the other acids. The final cleaning temperature was always room temperature, and the clean time was 60 seconds. In addition to this, the 1:1000 HCl solution was tested using different times: 5 s, 15 s, and 10 minutes. Two reference cassettes did not receive any dilute acid clean after the last APM step.

For the lifetime and the DLTS measurements, three wafers of each cassette were oxidized at 1000 °C in dry oxygen for 30 minutes, after which they were annealed in argon for an additional 15 minutes. The cooling rate was 15 °C/min down to 850 °C; the unloading rate was 150 mm/min.

RESULTS

The particle results are shown in Fig. 1. The reported values are average counts per wafer in a cassette of 24 wafers, after excluding the six worst and six best wafers. The horizontal lines in Fig. 1 represent the averages of the reference cassettes. Most of the cleans gave particle results comparable to the reference wafers. All but one of the most dilute acids (dilution ratio $\geq 10^4$) did not add any particles onto the wafers within the accuracy of the measurements. There seems to be a trend that higher concentrations of acids gave higher particle counts. The HF cleaned wafers were hydrophilic after the clean.

In Fig. 2, the lifetime results of the same cleans are shown. Three wafers from each clean were measured two days after the oxidation. The reported values are measured at the wafer centers. A low carrier injection level of about 10^{13} /cm^3 was used, generated by a short GaAs laser pulse. All the tested dilute acid cleans gave considerable increases in the minority carrier recombination lifetimes compared to the reference wafers. The reference wafers showed lifetimes of about 5 to 6 μs, as all the acid cleaned wafers had lifetimes from 17 to 48 μs, with the exception of 1:1000 HF cleaned wafers, whose lifetimes varied between 55 and 82 μs. In further studies, it was, however, found out that the *bulk* lifetimes of the HCl, HNO_3, and CH_3COOH cleaned and oxidized wafers were considerably longer than the lifetimes shown in Fig. 2.

Metallic surface contamination after the cleans was measured using VPD-TXRF (5,6). The measured surface iron concentrations are shown in Fig. 3. The results show low, no more than $2 \cdot 10^{10}$ at/cm^2 iron concentrations for all acid cleans. The $1:10^5$ HF left about $2 \cdot 10^{10}$ at/cm^2 iron on the wafers. The most dilute HCl cleans showed larger scatter in their surface iron values than stronger solutions. The reference wafers had $2.1 \cdot 10^{11}$ at/cm^2 of iron. The statistical error in the TXRF measurements of the acid cleaned wafers was $2 \cdot 10^9$ at/cm^2 (1σ value). The zinc concentration given by VPD-TXRF was, in almost all wafers, below $3 \cdot 10^{10}$ at/cm^2.

DLTS was used after oxidation to measure the concentration of Fe-B pairs, which essentially equals to the bulk iron concentration in p-type silicon. Before making the metal contacts, about 40 μm of silicon was etched away from the sample surfaces. Magnesium was used as contact metal. The measured bulk iron concentrations are shown in Fig. 4. All the acid cleaned wafers showed bulk iron concentrations below $2 \cdot 10^{11}$ at/cm^3, except the 1:10^5 HF cleaned wafer, where there was $6.3 \cdot 10^{11}$ at/cm^3 of iron. The DLTS measurements showed larger differences between different acid cleans than TXRF analysis.

DISCUSSION

The 1:1000 HF cleaned wafers had relatively high iron concentrations, but their lifetimes were, however, much larger than in the other acid cleans. To find out, if this difference in lifetimes was really caused by a higher *bulk* lifetime, i.e. reduced contamination other than iron, or by a lower surface recombination rate at the oxide interface, the recombination lifetimes of the DLTS sample wafers were measured in an electrolyte (7). The oxide was removed in 10 % HF, the surface layers removed in an HNO_3-HF-CH_3COOH solution, and the samples were then passivated in a hot H_2SO_4-H_2O_2 mixture. The minority carrier lifetimes were measured in a 5 % HF solution (7) a few days later. During the measurements, the samples were illuminated with feeble incandescent light. The slight background illumination was found to be necessary to reduce the surface recombination to a low level, probably because of surface traps. The low level of surface recombination was established by measuring unoxidized wafers of the same material as used previously; the measured lifetimes varied between 350 and 750 μs.

The lifetime measurements of the heat treated samples in the electrolyte showed that the higher lifetime in the 1:1000 HF cleaned wafers, compared to the other acid cleaned wafers, was caused exclusively by a lower surface recombination rate at the oxide interface. A lifetime of 88 μs was measured for the 1:1000 HF cleaned wafer in the electrolyte, as a value of 82 μs was measured from the same wafer as oxidized. The 1:10^5 HF cleaned wafer gave a lifetime of 36 μs in the electrolyte, the oxidized value being 17 μs only, and the APM cleaned wafer gave a result of 4.5 μs vs. 5.2 μs. All the other wafers showed lifetimes between 130 and 270 μs when measured in the electrolyte. It is not clear why the surface recombination rate in the 1:1000 HF cleaned wafers was considerably smaller than in the other oxidized wafers.

In Fig 5., the correlation between the minority carrier lifetimes measured in the electrolyte and the bulk iron concentrations is shown. The correlation curve is drawn assuming that the lifetime is limited by two separate factors, which both have their own independent lifetimes. One is the bulk iron concentration, and this first lifetime is supposed to be linearly dependent on the inverse of the iron concentration (8,9). The other component is the combined effect of all additional lifetime limiting factors, and it assumed to be the same for all the wafers. The iron limited lifetime was found to be about 21 μs / 10^{12} at/cm^3, in good agreement with previous reports (8,9). The best fit for the lifetime for zero bulk iron concentration was about 390 μs. From Fig. 5 it can be seen that for concentrations larger than 10^{11} at/cm^3, iron was the dominant

lifetime shortening contamination. This bulk concentration corresponds to no more than a few times 10^9 at/cm^2 of surface concentration.

In Fig. 6, the correlation between the measured surface and bulk iron concentrations are shown for those cleans, to whom both measurements were performed. If zero bulk iron concentration before oxidation and 100 % diffusion from the surface into the bulk is assumed, a factor of 32 /cm is required to convert the surface concentrations to bulk concentrations for 625 μm thick wafers. The real correlation factor in this experiment is below 32 /cm, as a part of the iron was gettered into the thermal oxide (9). The influence of the oxidation was monitored in the following manner. Wafers of the same material as before were cleaned in an APM solution, after which four wafers were oxidized in a process described earlier. In addition, four other wafers, cleaned simultaneously, were annealed in argon for 10 minutes in 1050 °C, and unloaded at a rate of 150 mm/min from 1050 °C. The minority carrier lifetimes were measured from these 8 wafers in the 5 % HF. The lifetimes were longer by a factor of 1.9 ± 0.1 in the oxidized wafers compared with the wafers annealed in argon. As the lifetimes and the bulk iron concentrations correlate closely for the high concentrations after an APM clean, it can be assumed that the oxidation reduced the iron concentration in the bulk by this factor, 1.9 ± 0.1. The high cooling rate of the argon annealed wafers decreases the lifetime, too, but the effect was found to be minor. Taking the effect of the oxidation into consideration gives us a correlation factor of about 17 /cm between bulk and surface iron concentrations. The dashed lines in Fig. 6 are drawn using these two values, 32 /cm and 17 /cm.

No good fit can be seen between the data points and the theoretical lines, except for the larger iron concentrations. There may be several reasons for this. There is always some iron, normally in the range of 10^{10} at/cm^3, in the bulk of silicon after the wafer manufacturing process. The VPD-TXRF measures an average over the area of a whole wafer, as the DLTS measures an area of about 1 mm^2, only. Furthermore, it looks like there would be a background level of a few times 10^9 at/cm^2 in the VPD-TXRF measurements.

The particle behavior observed in Fig. 1, the more dilute acids giving lower particle levels, is intuitively understandable. Very low concentrations of acids should behave, so far as particles are concerned, in a manner which is essentially similar to pure rinse water. Alkaline, i.e. high pH solutions usually give low particle counts, but low pH solutions do not (2,10). This behavior is thought to be connected with the surface charge of the wafers and that of the particles in the chemical solution or in the rinse water. Most particles in chemical solutions have negative surface charge, and in order to achieve low particle levels on a wafer, the wafer surface charge must be negative, too (10-12). If high concentrations of acids, i.e. low pH solutions are used, the charged shells with high ion concentration around the particles and the wafers are thin, thereby making it easy for the particles to overcome the repulsive electric forces (10). If the solution is kept dilute, its ability to reduce the negative charge on the wafer surface must be lower, too, thereby probably leaving the wafer in a state capable of effectively rejecting the particles during the clean and the subsequent rinses. Surface charge analysis (13) should be performed to test this last hypothesis.

The iron behavior in the dilute acids is understandable as well. In alkaline solutions, iron tends to be deposited on the solid surfaces, as the solubility of iron hydroxides to water is very low (14). Thus, high concentrations of iron are measured on wafers after e.g. an APM clean (2). The same is true for zinc and aluminum, too. The rinse does not normally help, as, according to the solubility products ($5 \cdot 10^{-17}$ for iron(II) hydroxide and $3 \cdot 10^{-39}$ for iron(III) hydroxide (14)), about 99 % of the iron(II) hydroxide would remain undissociated at pH 7, the iron(III) hydroxide remaining undissociated down to pH of about 1. The pH of the rinse water can, however, be easily changed to a value well below 7, e.g. the dilution of $1{:}10^6$ of HCl gives a pH of about 5. This change in water pH, i.e. replacing the hydroxyl ions with hydronium ions, seems to be able to drastically increase the solubility of iron into the water. Theoretically, this should cause about 98 % of the iron(II) hydroxide to dissociate, thus decreasing the amount of the insoluble ferrous hydroxide in the liquid by a factor of 50. In addition, if dilute acid solutions in the range of 1:1000 mixing ratio or higher are used, the purity of the solution and thus that of the wafers will be much less dependent on the chemical cleanliness, but on the DI water purity, instead.

Any measurements concerning the ability of the dilute acids to remove aluminum from the wafer surfaces were not performed. Such experiments must be made in the future to guarantee that aluminum will not affect disadvantageously to the oxide quality grown after dilute acid clean. The removal of other transition metals must also be studied in more detail, especially for Cu, Ni, and Cr. Comparisons between now suggested dilute acid cleans and other chemical cleans, traditionally used before high temperature treatments, should also be performed to find out the influence of the dilute acid cleans on thin oxide characteristics. The 1:1000 HF may have a beneficial effect on oxide interface quality.

CONCLUSIONS

A superior particle and metals removal performance compared with the widely used RCA clean can be obtained, if the final HPM clean is replaced by a very dilute acid solution at room temperature. The previous step before the dilute acid must be an alkaline particles removing step. The role of the last step is to remove the metals deposited during the previous step, without adding particles on the wafers. No oxidizing agent is required with the dilute acids as their etching power is very weak.

The iron level after a dilute acid clean is normally low, well below 10^{10} at/cm^2 level, according to the DLTS and the VPD-TXRF measurements. The minority carrier lifetime measurements established the removal of metals deposited by the previous APM step. The VPD-TXRF was not able to measure the differences in the low levels of iron left on the wafers. There may be a background level of a few times 10^9 at/cm^2 in the VPD-TXRF system used. Iron was found to be the dominant lifetime limiting factor for concentrations larger than 10^{11} at/cm^3. After most acid cleans and subsequent oxidation, the minority carrier recombination lifetimes were found to be well in excess of 100 μs in the bulk. HF solutions were found to behave differently to other tested acids. They left more iron on the wafers, especially the more dilute $1{:}10^5$ solution, but the resultant minority carrier surface recombination rate in oxidized wafers after

1:1000 HF was superior to those achieved using other acids.

ACKNOWLEDGMENTS

The DLTS measurements were performed by Mr. Niklas Henelius, whose aid is gratefully acknowledged. Special thanks are due to Dr. Jukka Lahtinen for fruitful discussions.

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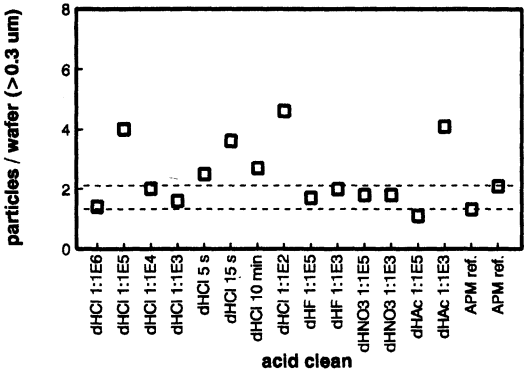

Fig. 1: Average particle counts after dilute acid cleans. The averages of the two reference cassettes are marked with dashed lines.

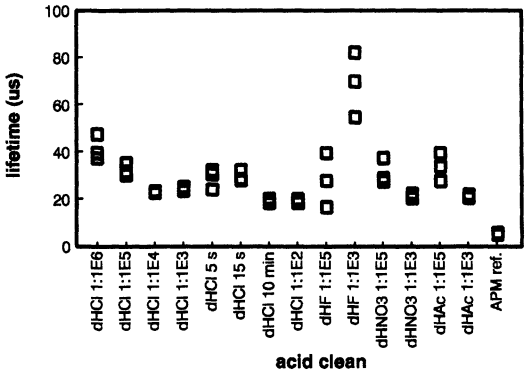

Fig. 2: Minority carrier recombination lifetimes after dilute acid cleans. The wafers were in as oxidized state. Every data point represents one wafer measured at the center of the wafer. Proper surface passivation in an electrolyte reduced the surface recombination further, and most acid cleans gave lifetimes in excess of 100 μs.

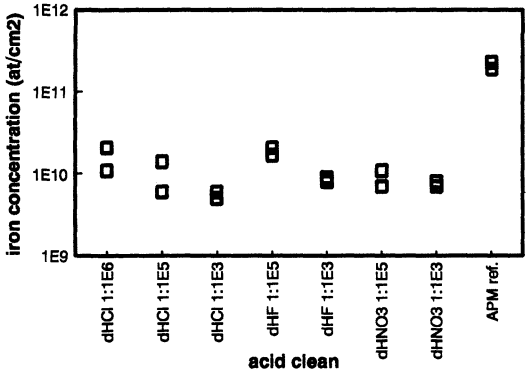

Fig. 3: The measured surface iron concentrations with VPD-TXRF in different cleans. There were always two wafers analyzed per clean.

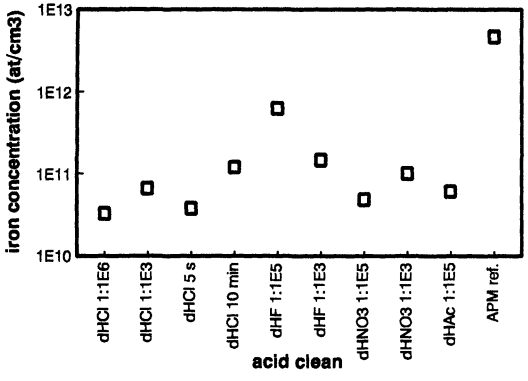

Fig. 4: The measured bulk iron concentrations with DLTS in different acid cleans. Only one wafer per clean was analyzed. The measuring points were at the wafer centers.

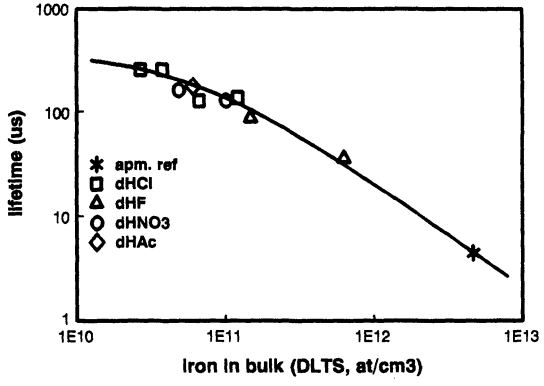

Fig. 5: The correlation between measured bulk iron concentrations and minority carrier lifetimes. The sample wafers were the same for the two measurements. The lifetimes were measured in 5 % HF solution to eliminate the surface recombination.

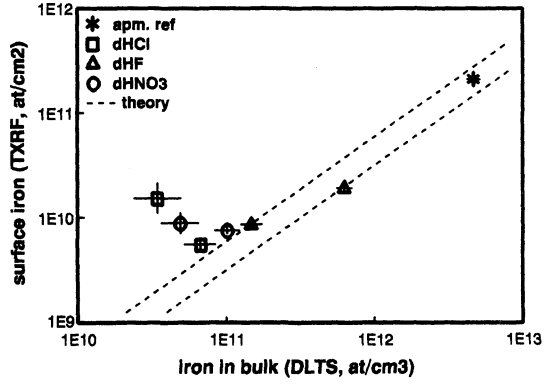

Fig. 6: The correlation between TXRF and DLTS measurements. The sample wafers for different measurements were taken from simultaneous cleans, but the wafers were not the same. The dashed lines represent theoretical correlation, using factors of 32 /cm and 17 /cm to convert the surface concentrations to bulk concentrations.

THE EFFECT OF METALLIC CONTAMINATION ON VOID FORMATION, DIELECTRIC BREAKDOWN AND HOLE TRAPPING IN THERMAL SiO_2 LAYERS

S. Verhaverbeke, M. Meuris, P.W. Mertens A. Kelleher, M.M. Heyns and R.F. De Keersmaecker

IMEC v.z.w., Kapeldreef 75, B-3001 Leuven, Belgium

M. Murrell and C.J. Sofield

B477 Harwell Laboratory, Oxfordshire , OX11ORA, U.K.

ABSTRACT

In this study the relationship between metallic contamination, void formation, dielectric breakdown and hole trap density is investigated. It was found that void formation and defect-related dielectric breakdown are not directly correlated since they are triggered by different metals. The density as well as the shape of the voids is influenced by the H_2O and O_2 partial pressure in the ambient.

INTRODUCTION

In MOS-technology, early dielectric breakdown has usually been attributed to metallic contamination. However, Heyns *et al.* (1) already established that other factors such as the silicon surface roughness are also important. This was confirmed more recently by Meuris *et al.* (2). They observed that there is no unique relation between metallic contamination and dielectric breakdown. However, a one-to-one correlation between dielectric breakdown and surface roughness could be observed and an improved pre-oxidation cleaning with lower silicon surface roughening was proposed (3). In the present work, the relationship between metallic contamination and dielectric breakdown is studied in more detail using the formation of voids by the decomposition of SiO_2 at high temperatues as an investigation tool. The mechanism of void formation is reasonably well understood (4,5) and the existence of a direct relationship between void formation and metallic contamination was already demonstrated. The starting point of this study was that if there would exist a direct relationship between metallic contamination and dielectric breakdown, then there should also be a correlation between void formation and dielectric breakdown (6). If this correlation is not experimentally observed it would demonstrate again that there is no straight-forward correlation between metallic contamination and breakdown.

EXPERIMENTAL DETAILS

The wafers used in these experiments were <100> and <111> n-type doped Si-wafers with a 125 mm diameter. Wafers with different levels of contamination were obtained by performing various RCA-type cleanings under several conditions using commercially available ULSI-grade chemicals of different vendors. The metal concentration on the wafers after the cleaning was evaluated using an Atomika XSA-800 Total reflection X-

Ray Fluorescence (TXRF) system (7). All elements from Sulfur to Krypton and from Silver to Bismuth can be measured with this technique. Before the TXRF measurement the metals were concentrated by using a Droplet Surface Etching (DSE) method (2) after Vapour Phase Decomposition (VPD) of the native oxide in HF (8). In this measurement procedure the chemical or native oxide is first dissolved by an HF-vapour which leaves the metals on the Si-surface. Afterwards a 50 µl droplet of a collection solution is used to collect these metals. A mixture of 0.5%HF-1%H_2O_2-98.5%H_2O was used for this purpose. This mixture was optimized to obtain a maximum reproducibility and collection efficiency (2). The droplet is then dried on the wafer and the drying spot is measured with TXRF.
In order to study the void formation a 15 nm oxide was grown on the wafers in dry O_2 at a temperature of 950°C in a double-walled furnace. Warm-up and cooling-down were performed in Ar. Afterwards the wafers were annealed in a rapid thermal anneal (RTA) system in an Ar ambient at temperature of 1200°C for 1 minute or in a regular furnace at 1200°C for 30 minutes. The oxygen content in the RTA-system was measured to be 0.33 vpm and the moisture content 1.2 vpm. Following the data of Smith and Ghidini (9, 10) under these conditions the oxide decomposes according to the equation Si(s) + SiO_2(s) -> 2SiO(g). At higher H_2O and O_2 partial pressures direct etching of Si by H_2O can also occur according to the reactions H_2O + Si -> SiO + H_2 and O_2 + 2Si -> 2SiO. These reactions give rise to the formation of voids in the oxide. Once the voids are nucleated, they grow laterally over the Si-surface. The density of the voids is equal to the density of nucleation centers for the void formation.
On the samples used for evaluation of the oxide breakdown properties a poly-Si layer was deposited directly after the oxidation and doped with phosporous. Capacitors were made by standard lithography and wet etching. The typical capacitor area used to evaluate the breakdown statistics is $3.85*10^{-2}$ cm^2. Breakdown measurements were performed on at least 100 capacitors on each wafer. The yield was defined as the percentage of capacitors which show an intrinsic breakdown behaviour in a Weibull plot. Typically these are capacitors which survive a field of 12 MV/cm.

RESULTS AND DISCUSSION

Metallic contamination, void formation and dielectric breakdown

It was already demonstrated that there exists a direct relationship between metallic contamination and void formation (4,5). However, these experiments were performed at intentionally contaminated wafers with contamination levels which are much higher than what is relevant under normal processing conditions. Therefore, in these experiments the relation between metal contamination and void formation was investigated in more detail at lower contamination levels. A correlation with the gate oxide integrity was also made. The results for a series of wafers obtained from various cleanings is given in table I. This table summarizes the results obtained on 17 batches which were cleaned under varying circumstances and with chemicals of different characteristics. In each case a different wafer, but coming from the same cleaning bath, was used for determining the void nucleation density, for measuring the metallic contamination by VPD-DSE-TXRF and for establishing the electrical breakdown properties. On some batches, either only void formation or breakdown tests were performed together with VPD-DSE-TXRF.
From this table it is clear that the void formation is not directly related to the gate oxide yield. For example it is seen that while batches 2, 3 and 6 have about the same number of voids (approximately 18 to 19 voids/cm^2) the yield for the batches varies between 11%

and 60%. Also batch 1 and batch 4 have nearly the same void density but show a significant variation in the gate oxide yield. The metal contamination is dominated by the contribution of Ca and is directly related to the yield. This is in agreement with another investigation where this effect was studied in more detail (11). The relationship between Ca contamination and yield is illustrated in fig.1. The spread on the data is partially due to the statistical nature of the effect and partially to some experimental factors. The measurement of the Ca concentration and the yield determination was done on different wafers and although they were treated together in the same chemical bath some variation may exist on the exact Ca-level from wafer-to-wafer. Additionally, various types of cleanings were used including cleanings in a automatic spray cleaner and using a conventional wet bench. Therefore, variations may exist on the particle density which can mask the effect of the Ca. Other factors are the Al concentration on the wafers and the cleaning-induced surface roughening (2) which can also drastically change the breakdown characteristics. However, even taken all these variations into account the relation between a decreased Ca contamination on the wafer and an increased yield is still very striking. The data even suggest that there is a threshold value for the Ca contamination around 10^{11} cm^2. The Ca concentration on the wafer must be lower than this value before reasonable yields can be obtained. The origin of the Ca on the Si-surface will be discussed elsewhere (11).

Normally all metals on a silicon surface are in their oxidized form. After a $NH_4OH/H_2O_2/H_2O$ chemical oxidation, they are mostly in the $M(OH)_X$ form, while after a dry ozone treatment, they are dominantly in the MO_X form. At every temperature there is an oxygen partial pressure above which this situation is stable. However, under this oxygen partial pressure, those metals which have a lower free energy of formation then SiO will be reduced to their metallic form, thereby oxidizing the silicon and forming volatile SiO species. Indeed, Fe, Cu and Zn form oxides that will be reduced to oxidize Si. Ca, on the other hand, has an oxide which is much more stable then the oxides of Si and thus, Ca will not be reduced (12, 13). From this consideration it is suggested that the void formation is not correlated to the total density of metals on a surface, but only to the number of reducible metals. This correlation is shown in fig.2. Despite the statistical fluctuations the trend towards higher void densities with larger contamination levels of reducible metals is very clear. The fact that the Ca contamination does not contribute to the void formation is clearly illustrated by batch 8 which has a very high Ca contamination but only a small number of void nucleation centers.

Summarized it is found that there is no direct correlation between dielectric breakdown and void formation since they are both triggered by other contaminants. In these experiments it was found that Ca can have a dominant effect on the oxide breakdown properties but does not directly contribute to the void formation. Liehr *et al.* (5) have found that stacking faults decorated with metals can serve as nucleation centra for voids, while dislocations (as introduced by implanting phosphorous) did not introduce any void nucleation centra. This last finding was confirmed in our investigation where it was observed that the void density on SIMOX wafers was identical to that found on Czochralski material for identical contamination levels. However, the dislocation density on SIMOX wafers typically was in the order of 10^5 cm^{-2} which is much higher than on Czochralski material. No important density of stacking faults was observed on either material. These findings again stress the point that the presence of specific metal contaminants is a prerequisite for the formation of voids.

Void growth mechanism

The growth mechanism of the voids after nucleation was also studied in more detail. As a general finding it was observed that the number of voids does not change significantly with time, in agreement with previous studies (5,6). This indicates that the ones which are nucleated grow with time, but no new ones are nucleated. In our study all voids were found to have about the same diameter at a certain time. This suggests that the void growth mechanism is independent of the contamination type. The void nucleation mechanism is apparently not the rate limiting step. Neither the nucleation, nor the lateral growth mechanism is completely isotropic and the amount of anisotropy is dependent on the H_2O and O_2 back pressure. This can be seen by comparing the voids grown on <100> and <111> material and for low and high H_2O and O_2 partial pressures.
For identical contamination levels the void density is much smaller on <111> wafers then on <100> wafers. The void size, however, is identical on the two wafer types. This shows that nucleation is easier on <100> then on <111> substrates. This can be explained by the larger surface free energy of <100> surfaces as compared to <111> surfaces. The lateral growth of the voids is dependent on the crystallographic axes. A SEM picture of a void grown on <100> material is shown in fig.3. The outer shape is circular, but in the center of the void features which follow the (100) and (110) axes are seen. In fig.4 a void grown on a <111> substrate is shown. It is clear that the outer shape is hexagonal, thus following (1 $\bar{1}$ 0), ($\bar{1}$ 10) and (01 $\bar{1}$) axes. The Si voids also show etch features inside the void with a three-folded symmetry.
In order to illustrate the dependence on the H_2O and O_2 partial pressure, wafers with comparable contamination levels were annealed in a hot wall furnace at atmospheric pressure with a flow of 13 slm of Ar or in a RTA (cold wall) furnace with a flow of 10 slm of Ar. The H_2O and O_2 partial pressure was estimated to be around 20 mTorr in the hot wall furnace and around 0.8 mTorr in the RTA furnace. After 30 min at 1200°C in the hot wall furnace a void density of about 1 void/cm^2 was found with an average void diameter of 50 μm. This void size was already obtained after a 3 min anneal at the same temperature in the RTA furnace. The void density after this RTA-step was about 20 times higher than in the previous case. This demonstrates that when the H_2O and O_2 back pressure during the high-temperature anneal is reduced, more voids are nucleated and their growth is enhanced. Also the shape of the voids alters with changing partial H_2O and O_2 pressures. This is illustrated in figs.3 and 5 for <100> substrates. RTA-annealing at 0.8 mTorr for 3 min at 1200°C results in voids which are circular in shape, as is shown in fig.3. When the annealing is performed in a furnace at an oxygen back pressure of 20 mTorr during 30 min at 1200°C voids are formed which follow the crystallographic axes and, therefore, have a rectangular shape. This is illustrated in fig.5. The reason for this is that when the H_2O partial pressure rises the reaction $H_2O + Si \rightarrow SiO + H_2$ becomes more important and this reaction was shown to be anisotropic (10).
The density of voids was observed to have a weak dependence on the oxide thickness. This is shown in table II for oxides ranging from 4.7 to 12.8 nm. The origin of this effect is suggested to be the lower metal surface concentration after longer oxidation times as more contaminants can diffuse into the Si-bulk.

Void formation and hole trapping

It was demonstrated above that the influence of reducible metals on the dielectric breakdown is not very large. However, they can have a strong impact on the gate oxide integrity when an annealing is performed in an inert ambient. Annealing in an inert

atmosphere after the oxidation under the presence of metallic contamination was shown to induce hole traps and low-field leakage (6). This phenomenon was found to be very strongly dependent on the back pressure of oxygen in the annealing ambient and a relation with the formation of voids was proposed. However, there exists some evidence that the effect of metals on hole trapping can in some cases be more direct than this. It was demonstrated that the introduction of Zn in a thermal oxide layer can form a hole trap and leads to an increase in the radiation sensitivity (14). Verhaverbeke *et al* (15) showed that the implantation and subsequent annealing of Cl in an Si/SiO_2/poly-Si structure resulted in an improvement of the breakdown statistics and a decrease in the hole trap density. Eventually, this can be explained by the reduction of active metal-related defects by the action of the Cl.
A commonly used technique to investigate the hole trapping properties of oxide layers is the avalanche injection technique (16). To this purpose highly doped n-type substrates are needed. Eventually, ion implantation can be used to increase the Si-surface doping level. However, it was observed that when the hole trapping properties of oxides grown on homogeneously doped substrates are compared with layers grown on implanted substrates (having an identical surface doping level) systematically more hole traps are found on the oxides grown on the implanted samples. This is shown in table III. On implanted substrates also a larger number of void nucleation centers is observed (6). This is either due to residual implantation damage or to the metallic contamination often introduced during ion implantation. When an annealing is performed in an inert ambient an increase in the hole trap density is found (see table III). This increase is independent on the initial hole trap density and the type of substrate used. This suggests that the increase in hole trap density during annealing is an intrinsic property of the SiO_2 and is not triggered by some local defect. The macroscopic void formation phenomenon is triggered by some local defect but the lateral expansion is also an intrinsic property. This lateral expansion, due to the reaction $Si(s) + SiO_2(s) \rightarrow 2\ SiO(g)$, is intrinsic to the Si/SiO_2 interface and could eventually be the cause for the increase in hole trap density upon annealing in an inert ambient.

CONCLUSIONS

It was demonstrated that the void formation and the defect-related dielectric breakdown are not directly correlated since they are triggered by different metals. Ca was found to be very important in the degradation of the breakdown properties, but apparently has no effect on the formation of voids. This latter mechanism is dominated by reducible metals. Their effect on the dielectric strength of thermal gate oxides becomes very pronounced when an annealing is performed at a high temperature in an inert ambient. Under these conditions silicon can be etched through the formation of voids which strongly degrades the gate oxide integrity. The void growth mechanism was found to be dependent on the Si-substrate orientation and oxygen back pressure during the high-temperature annealing. The relation between hole trapping and void formation was also discussed. The results of this investigation provide some important guide-lines to improve the gate oxide integrity in a normal processing environment.

ACKNOWLEDGMENTS

This work was supported by the European Community in the framework of the ESPRIT Basic Research Action PROMPT.
Bruno Knuts and Marc Vandievel are thanked for helping with the electrical measurements. Carine Allaerts is thanked for helping with the annealing cycles.

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Table I : Void density, yield and metallic contamination on 17 batches of differently cleaned wafers. In some cases either the yield or the void density was not measured (n.m.).

Batch number	Voids (cm^{-2})	Yield (%)	Metallic contamination (10^9 cm^{-2})				
			Ca	Fe	Cu	Zn	Ni
1	50	44	38	13	10	23	5
2	18	11	87	4	11	14	1
3	18	49	64	10	6	15	3
4	48	72	9	5	5	27	1
5	13	40	29	9	4	16	2
6	19	60	9	10	1	9	1
7	97	n.m.	490	16	5	125	4
8	4	n.m.	1015	16	4	18	1
9	44	n.m.	140	18	5	50	24
10	5	n.m.	27	2	5	10	1
11	n.m.	16	625	12	4	85	5
12	n.m.	70	80	7	3	6	1
13	n.m.	25	350	72	15	195	41
14	n.m.	33	85	3	2	7	1
15	n.m.	10	140	18	5	50	24
16	n.m.	22	255	10	5	36	2
17	n.m.	25	735	47	8	84	7

Table II : Void density after annealing as a function of oxide thickness.

Oxide thickness (nm)	Voids (cm^{-2})
4.7	18
6.9	6
9.2	4
12.8	3

Table III : Hole trapping properties as a function of starting material (highly-doped or implanted substrates) and anneal treatment.

Starting material	Initial hole trap density (10^{11} /cm^2)	after 30 min anneal in N_2 (10^{11} /cm^2)	increase in trap density (10^{11} /cm^2)
highly doped	10	16	6
implanted	35	41	6

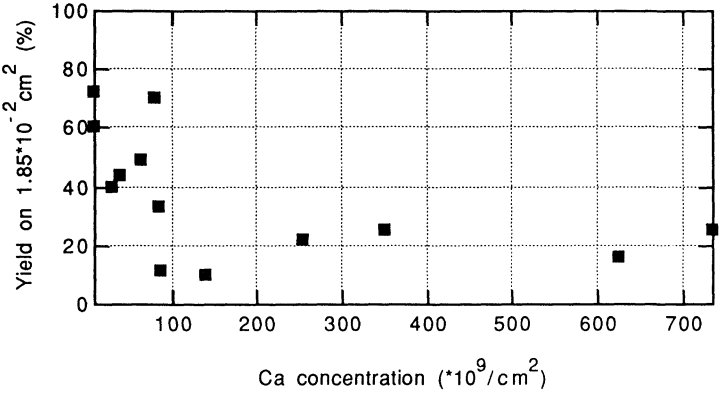

Fig. 1 : Relation between the Ca concentration and the yield.

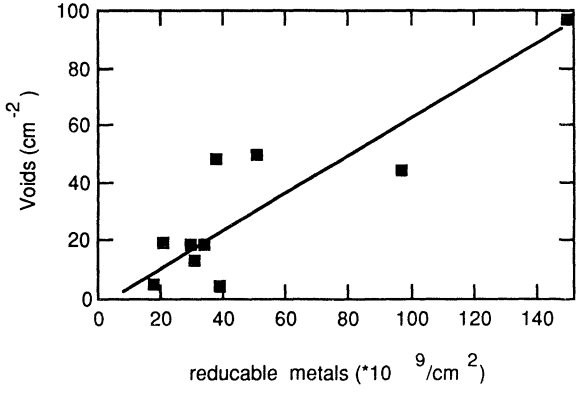

Fig. 2 : Void density after annealing as a function of the density of reducable metals on the Si-surface prior to the oxidation.

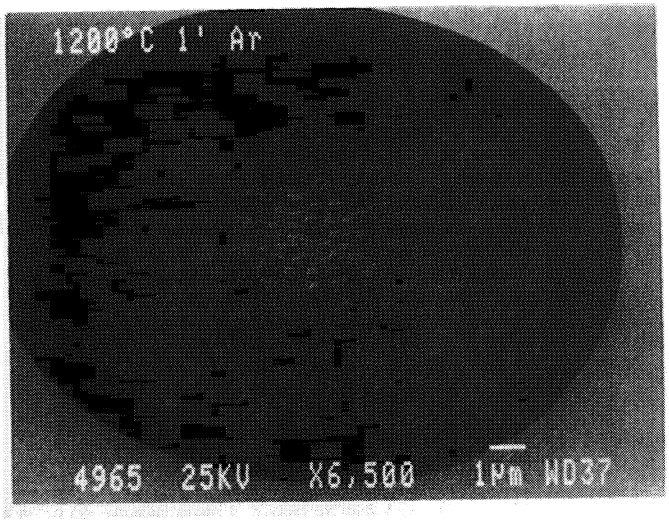

Fig. 3 : Typical void on a <100> substrate.

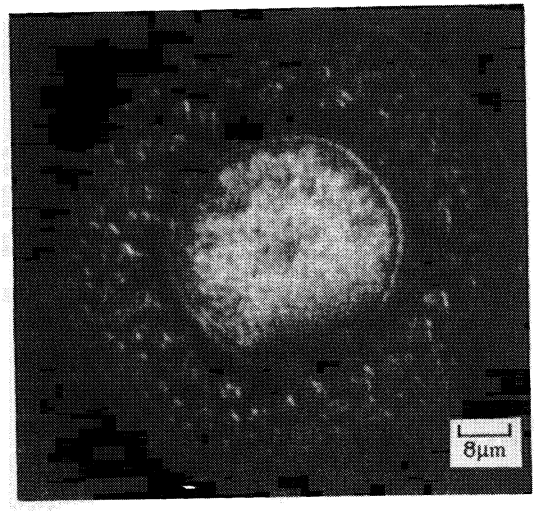

Fig. 4 : Typical void on a <111> substrate.

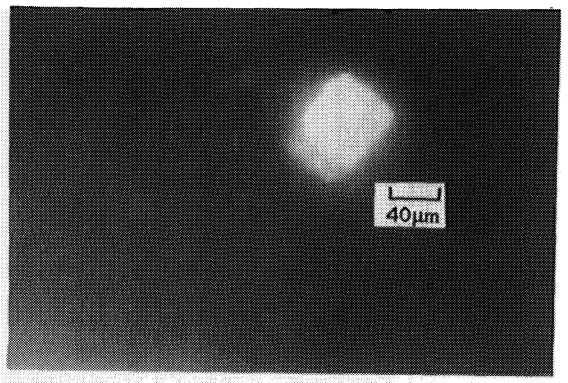

Fig. 5 : Typical void on a <100> substrate after annealing in an ambient with a high water and oxygen back pressure.

THE REMOVAL OF TRACE QUANTITIES OF THERMALLY DEPOSITED CU AND FE ATOMS FROM THE SILICON SURFACE USING STANDARD AQUEOUS CHEMICAL CLEANING PROCEDURES

M.L. Kniffin* and C.R. Helms
Department of Electrical Engineering, Stanford University, Stanford CA 94305

ABSTRACT

Using Auger electron spectroscopy, we have examined the ability of a variety of standard aqueous chemical cleaning procedures to remove trace quantities of thermally deposited copper and iron atoms from the surfaces of silicon substrates. It was determined that the technique for preparing the metal contaminated test standard prior to metal deposition had a significant impact on the experimental results. This suggests that the silicon surface chemistry and the chemical environment of the metal impurities plays an important role in determining the cleaning efficiency of a given wet chemical processing sequence.

INTRODUCTION

It is well known that the presence of trace quantities of alkali and heavy metals on the surface of a silicon substrate can have catastrophic effects on both device performance and process yields. The development of efficient methods for the removal and control of these impurities is of critical importance to the advancement of integrated circuit technology.

The desire to optimize currently existing wet chemical processing techniques and the recent development of alternative wafer cleaning technologies [1,2] have brought about a renewed interest in understanding the basic physics and chemistry behind the removal and control of metallic impurities. As part of a broader program to understand and improve the cleaning efficiency of newly developed wafer processing techniques, we have conducted a study of the ability of standard aqueous chemical cleans to remove trace metal impurities from silicon surfaces.

A systematic examination of the relative efficiency of various wafer cleaning techniques requires the development of an appropriate set of test standards with known concentrations of metallic surface contamination. Metal impurities can exist in numerous forms on a wafer surface and the most efficient technique for removing a given contaminant may depend strongly upon the chemical environment of the impurity atom as well as the chemistry of the silicon surface. Previous studies have focused primarily on the removal of metallic residues that were plated or deposited onto the silicon surface from intentionally contaminated aqueous chemical solutions [3,4]. As a point of comparison, we have examined the removal of thermally deposited copper and iron atoms from the surfaces of both bare and oxidized silicon substrates.

*Present Address: Motorola Inc., 5005 E. McDowell Rd., MD C108, Phoenix, AZ 85008

EXPERIMENT

In order to fabricate the contaminated silicon wafers, an electron-beam evaporator was modified to facilitate the deposition of sub-monolayer concentrations of metal atoms. Depositions were performed by setting a very low evaporation rate ($< 10^{13}$ atoms-cm^{-2}-sec^{-1}) with the shutter closed, then opening the shutter to expose the wafer surface for a fixed period of time. Using this technique it was possible to reproducibly and uniformly deposit trace quantities (10^{12} to 10^{15} atoms-cm^{-2}) of metal impurity atoms over large portions of the surfaces of 4- and 6-inch diameter silicon wafers. With a more accurate mechanically activated shuttering mechanism, the controllable deposition of much lower ($\sim 10^{11}$ atoms-cm^{-2}) concentrations of metallic impurities should be possible.

Using this deposition system, silicon wafers could easily be contaminated with many of the transition and noble metal impurities that are commonly encountered in integrated circuit fabrication. However, for the purposes of this investigation we focused primarily on the removal of iron and copper impurities from the silicon surface. These metals were chosen because they are commonly found in semiconductor process equipment and are frequently deposited onto the surfaces of silicon wafers during processing [2,5,6]. The two metals also exhibit distinctly different aqueous chemistries [7] and thus provide a measure of the importance of metal chemistry in determining the efficiency of a particular wafer cleaning technique.

Metal contaminated wafers were prepared using two different pre-deposition aqueous chemical cleaning procedures for the silicon substrate. These pre-deposition cleans were chosen to provide silicon substrates with distinctly different surface chemistries. This was done in order to ascertain whether or not the chemical environment of the metal atoms and the chemistry of the silicon surface play a significant role in determining the ability of subsequent chemical cleans to remove trace metal contaminants from the wafer surface. The first method used to prepare the silicon substrates was as follows:

I. NH_4OH:H_2O_2:H_2O (1:2:5) 70°C, 10 min.
DI water rinse, 5 min.
Nitrogen blow dry.

This treatment tends to yield a silicon surface which is relatively free of carbon contamination, but is passivated by a thin native oxide layer [8]. Metal atoms deposited onto these surfaces are expected to exhibit oxide- or silicate-like bonding. The second method used to prepare the silicon substrates was as follows:

II. NH_4OH:H_2O_2:H_2O (1:2:5) 70°C, 10 min.
DI water rinse, 5 min.
HF:H_2O (1:50), 1 min.
Nitrogen blow dry.

This cleaning procedure tends to leave the silicon surface relatively free of carbon and oxygen contamination [8]. Substrates prepared in this manner were immediately inserted into the evaporation chamber following the final etch step, in order to minimize the

accumulation of carbon and oxygen that inevitably occurs during exposure of a bare silicon surface to the laboratory ambient [8]. Metals deposited on these surfaces might be expected to exhibit more silicide-like bonding than those deposited onto a surface passivated with a native oxide. They are also more apt to be incorporated into a re-grown native oxide layer or covered in a carbonaceous film.

The metal contaminated wafers were cleaved into quarters and subjected to a variety of different chemical cleaning sequences aimed at reducing the surface impurity concentration. These cleaning sequences were based on combinations of the various process steps found in several different standard procedures for silicon substrate preparation [3,4,9-11].

To assess the relative efficiency of the various chemical cleans, both the as-deposited and post-cleaning surface metal concentrations were monitored using Auger electron spectroscopy (AES). In order enhance the detectability limit for metallic impurities, the operating conditions for the analysis system and the Auger scan parameters were chosen to give the maximum achievable signal to noise ratio. Under the appropriate operating conditions, we found that this technique could detect metal impurities at relatively low concentrations ($\sim 5 \times 10^{12}$ atoms-cm^{-2}).

A comparison of the Fe$_{LMM}$ (703 eV) or Cu$_{LMM}$ (920 eV) Auger signal strength to the substrate Si$_{KLL}$ (1619 eV) Auger signal intensity was used to obtain a quantitative estimate of the residual metal contamination. The relative Auger signal strengths were converted to absolute metal concentrations using experimentally determined elemental sensitivity factors. The sensitivity factors were calculated from total reflection X-ray fluorescence (TRXF) measurements taken on a representative subset of the as-deposited metal contaminated standards. The correlations between the relative metal and silicon Auger peak-to-peak heights and the surface impurity concentrations are plotted in figure 1. The iron and copper signal intensities vary in direct proportion to the metal concentration over several orders of magnitude, thus providing an accurate measure of the surface impurity concentration.

RESULTS AND DISCUSSION

Our results for RCA-based [3,4] and MPR-based [11] cleans are summarized in Table I. One can see that the technique used to prepare the metal contaminated test standard often had a major impact on the experimental results.

A change in the procedure for cleaning the test wafer prior to metal deposition often significantly altered the ability of a given wet chemical processing sequence to successfully reduce the surface impurity concentration. This is illustrated dramatically in figure 2, which compares Auger spectra taken from the surfaces of two different test standards following a standard RCA clean. Though the initial iron concentration present on the surfaces of these two wafers was the same, one can see that the residual impurity concentration differs significantly.

The removal of Fe and Cu from the surfaces of silicon wafers which had been precleaned in an ammonium hydroxide-hydrogen peroxide solution proved to be relatively

simple. Any cleaning sequence involving an aqueous chemical solution in which the particular metal is expected to be soluble readily reduced the metal impurity concentration to below the detectability limit of our analysis technique. This observation is consistent with the results of previous studies which have examined the removal of chemically deposited copper and iron impurities [3,4] from the silicon surface.

Cleaning sequences which stripped the native oxide from the silicon surface were also able to substantially reduce the concentration of iron and copper atoms present on the surfaces of these wafers, regardless of the expected solubility of these metals in the etch bath. As a consequence, any processing sequence involving immersion in a chemical solution containing hydrofluoric acid also tended to lead to a substantial reduction in the surface impurity concentration.

Metals deposited onto silicon surfaces which had been cleaned in a dilute hydrofluoric acid solution were significantly more tenacious. Substantial reductions the concentration of copper and iron impurities present on the surfaces of these wafers could only be realized by subjecting the sample to a cleaning procedure which removed the top surface of the substrate *via* the growth and subsequent dissolution of a thin native oxide layer. This could be achieved by introducing an intermediate hydrofluoric acid etch step to the standard RCA and MPR cleans. We found that immersing the substrate in a solution containing hydrofluoric acid and a mild oxidant such as dilute nitric acid or dilute hydrogen peroxide was also an effective means of removing copper and iron impurities from these surfaces. A similar observation has been made by Hosoya *et al.*, who has examined the removal of metallic impurities introduced during reactive ion etching of the silicon surface [12].

These results demonstrate that chemistries for metal removal are strongly dependent upon the silicon surface chemistry and the chemical environment of the metal impurities. This is an important consideration when interpreting the literature and when evaluating the applicability of a cleaning technique to a given process.

ACKNOWLEDGEMENTS

This work was supported by Advantage Production Technology, Inc., SEMATECH through Advantage, and SEED funding from Texas Instruments.

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	Fe Preclean		Cu Preclean	
	$HF:H_2O$	$NH_4OH:H_2O_2$	$HF:H_2O$	$NH_4OH:H_2O_2$
AS DEPOSITED	1×10^{14} atoms-cm^{-2}	6×10^{14} atoms-cm^{-2}	1×10^{15} atoms-cm^{-2}	2×10^{14} atoms-cm^{-2}
RCA	6×10^{13}	below detectability limit	3×10^{14}	below detectability limit
RCA + HF	below detectability limit	below detectability limit	below detectability limit	below detectability limit
MPR	2×10^{13}	below detectability limit	1×10^{14}	below detectability limit
MPR + HF	below detectability limit	below detectability limit	below detectability limit	below detectability limit

Table I. Efficiency of copper and iron removal for RCA-based and MPR-based cleans, as determined by Auger electron spectroscopy. The standard RCA clean consists of a 10 minute immersion in a $NH_4OH:H_2O_2:H_2O$ (1:2:5) solution at 80°C, followed by a 10 minute immersion in a $HCl:H_2O_2:H_2O$ (1:2:7) solution at 80°C. The standard MPR clean consists of a 10 minute immersion in a $H_2SO_4:H_2O_2:H_2O$ (1:1:5) solution at 95 °C followed by a 10 minute immersion in a HNO_3:HCl (1:3) solution at 70°C. The RCA + HF and MPR + HF cleans include a 30 second $HF:H_2O$ (1:50) etch between sequential process steps.

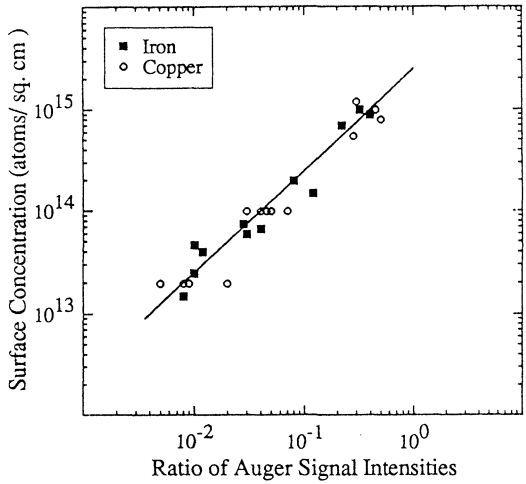


Figure 1. Plot of the Cu_{LMM}:Si_{KLL} and Fe_{LMM}:Si_{KLL} Auger signal intensity ratios as a function of surface copper or iron concentration as measured by total reflected x-ray fluorescence. The intensity ratios exhibit a linear dependence on concentration over several orders of magnitude.

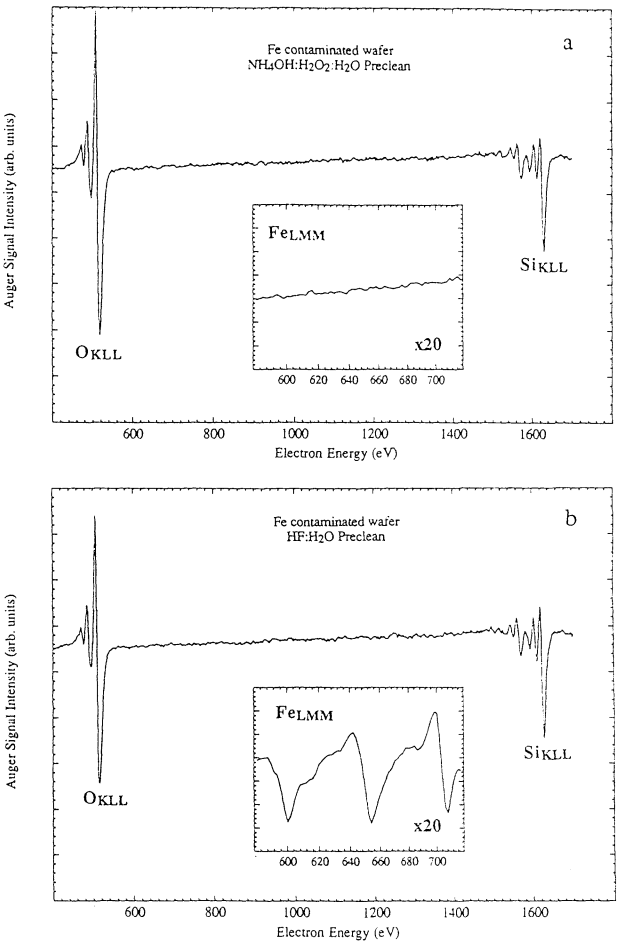


Figure 2: Auger spectra taken from the surfaces of two different iron contaminated silicon wafers following a standard RCA clean. The initial iron concentration was on the order of 10^{14} atoms per sq. centimeter for both of these wafers. The spectra shown in part (a) were taken from a wafer which had received an ammonium hydroxide-hydrogen peroxide clean prior to metal deposition. The Fe_{LMM} signal from this surface is identical to that of an uncontaminated control wafer, indicating that the RCA clean succeeded in removing most of the iron impurities from this wafer. The spectra shown in part (b) were taken from a wafer which had received a dilute hydrofluoric acid clean prior to metal deposition. The Fe_{LMM} signal shown in this figure corresponds to a surface iron concentration on the order of 10^{14} atoms per sq. centimeter, indicating that the standard RCA clan was not an effective means of removing iron impurities from the bare silicon surface.

WAFER-SURFACE METALLIC CONTAMINATION AND POLYSILICON DEPOSITION

W. A. Syverson, P. J. Schubring
IBM General Technology Division
Essex Junction, Vermont 05452

ABSTRACT

Metallic contamination of wafer surfaces results in accelerated, localized defects in a film during the low-pressure chemical-vapor deposited polysilicon (LPCVD Poly) process. The defects are horn-like in configuration and can cause electrical shorts in semiconductor devices. In many cases, the sizes and shapes of the horns are uniquely characteristic of the specific metallic contamination tested. This paper describes the technique used and the experimental results obtained.

INTRODUCTION

Previous experimental work at IBM's Essex Junction, Vermont, facility determined the presence of certain metal-based particles on wafer surfaces (e.g., aluminum, tin, etc.) due to the use of the process wet chemical hydrogen peroxide (H_2O_2). These particles substantially increased the wafer-surface foreign-material (FM) levels observed after processing through low-pressure chemical vapor deposited polysilicon (LPCVD Poly).

A related experience with a different metal-based contaminant, contained in sulfuric acid used for wafer cleaning, strongly indicated that the metal contamination was accelerating the LPCVD Poly deposition rate preferentially at the point of contamination. The accelerated deposition resulted in the formation of a polysilicon 'circular defect' which was characteristic of the sulfuric acid from one specific supplier (Figures 1 and 2). Many of these circular defects also had well-defined polysilicon horn-shaped formations emanating from their geometric centers (Figure 3). Various shapes of these horns were also observed on separate defects.

Standard pre- and post-chemical-exposure FM monitoring techniques were totally ineffective in detecting wafer-surface contamination prior to polysilicon deposition and the traditional analyses (Auger, ESCA, etc.) were equally ineffective. However, when we processed exposed wafers with LPCVD Poly, the wafer-surface metallic contamination was detected.

This paper describes a technique for the LPCVD Poly semiconductor process that we used to analyze a set of known wafer surface contaminants; the unique experimental results are also described.

APPROACH

Since a silicon-oxide surface is standard in many semiconductor wafer processes, it was selected as our experimental platform. Using clean 45-nm oxide wafers, we deposited a known metal-based contamination on the wafer surfaces. (Laboratory purity grade material was used for all metallics tested.) Approximately 400 nm of LPCVD Poly was then deposited on the wafers. The wafers were then visually inspected with an optical microscope and photographed using a scanning electron microscope (SEM).

Two identical experimental tests were conducted to confirm repeatability of the solid and powder sources of each contamination. During the second experimental test, other sources of metals and deposition techniques were evaluated. Commonly used photoresist developers were evaluated during the second test for horn-like formations.

RESULTS

Table 1 summarizes the experimental results. Nearly all metallics tested resulted in some type of polysilicon horn formation. Surprisingly, many of the horns appeared to be uniquely characteristic of the specific element tested. Also, tests on alkali-metal solutions commonly used in developing photoresist resulted in a variety of horn-like formations. Of all samples tested, only lead, carbon, and the organic photoresist developer tetramethyl ammonium hydroxide (TMAH) did not produce polysilicon horn-like defects.

CONCLUSION

Metal-based contamination on wafer surfaces can be a major source of defects in semiconductor devices. A uniquely sensitive standard semiconductor process has been described and characterized that can be used as an in-line analytical tool to determine the presence of metal-based contamination on wafer surfaces.

Table 1. Polysilicon horn vs. metallic contamination.

Metal	Length μm	Description of Polysilicon Horns
Aluminum	1.0	Conical in shape.
Barium	1.0	Conical in shape.
Calcium	0.5-1.0	Straight, cylindrical in shape.
Chromium	0.7-1.0	Horn-like in appearance.
Cobalt	0.2-0.5	Elliptical in shape.
Copper	10.0	Thin and very sharp, highly refractive.
Gold	1.0-3.0	Cylindrical, bent, "halo" at base.
Iron	1.0	Conical in shape.
Magnesium	0.3-0.4	Numerous and twisted in shape.
Manganese	1.0	High density, conical in shape.
Molybdenum	2.0-5.0	Long, straight, cylindrical in shape.
Nickel	2.0-3.0	Conical and uniform in shape.
Platinum	0.5-1.0	Conical in shape and convoluted.
Silver	0.5	Conical, uniform in shape.
Tantalum	5.0	Cylindrical, rounded tips.
Tin	3.0	Thin, monocrystalline, rounded ends.
Titanium	0.5-1.0	Conical in shape.
Tungsten	0.5-1.0	Conical in shape.
Zinc	0.5-1.0	Conical in shape.
KOH	0.3-0.5	Variety, conical in shape, convoluted.
NaOH	1.0-3.0	Variety, cylindrical in shape.
$NaSiO_3$	0.5	Variety, conical in shape.
Carbon	-	No horns noted.
Lead	-	No horns noted.
TMAH	-	No horns noted.

Table Notes:

- For Magnesium, the first run did not yield any distinctive horn-like patterns whereas the second run yielded the data shown.
- For Aluminum, the solid source did not yield any horns due possibly to the inherent presence of an aluminum oxide film covering the solid source.
- For Iron, the solid source did not give any definite horn-like shapes, also possibly due to the presence of an oxide layer over the iron source. The iron filings and powder both propagated horns.
- The KOH samples were both processed in the same run. One sample was a solid source, a KOH pellet, while the liquid source was the actual solution used in the manufacturing process. Both samples contained horns.

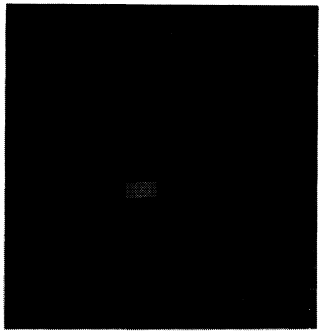


Figure 1. Dark-field optical photograph of a circular defect.

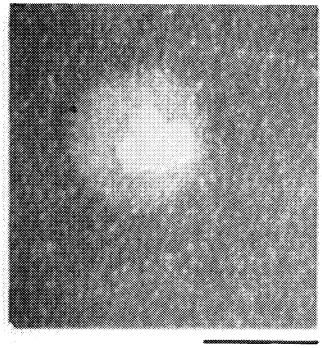


Figure 2. SEM micrograph of a circular defect.

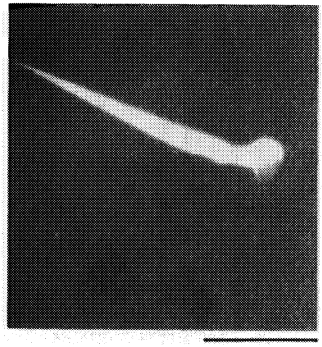
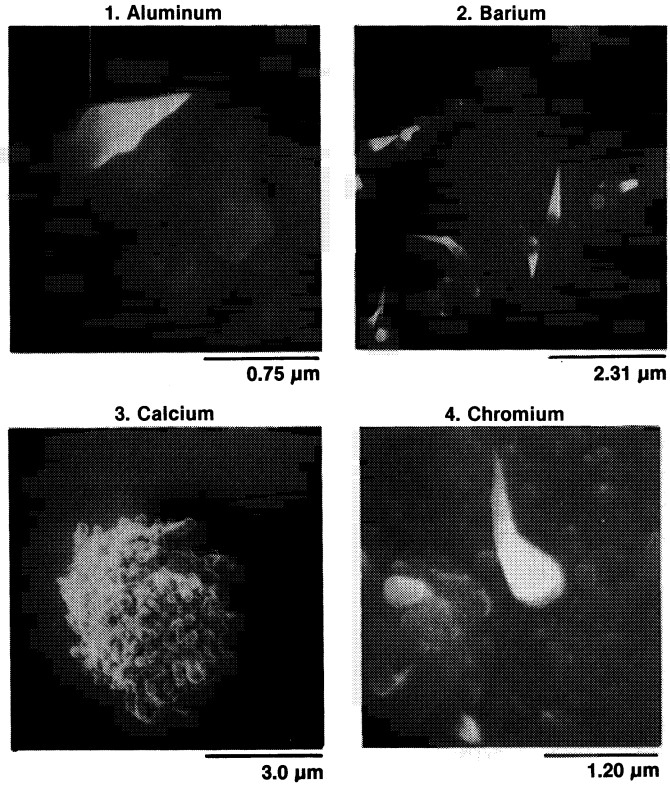
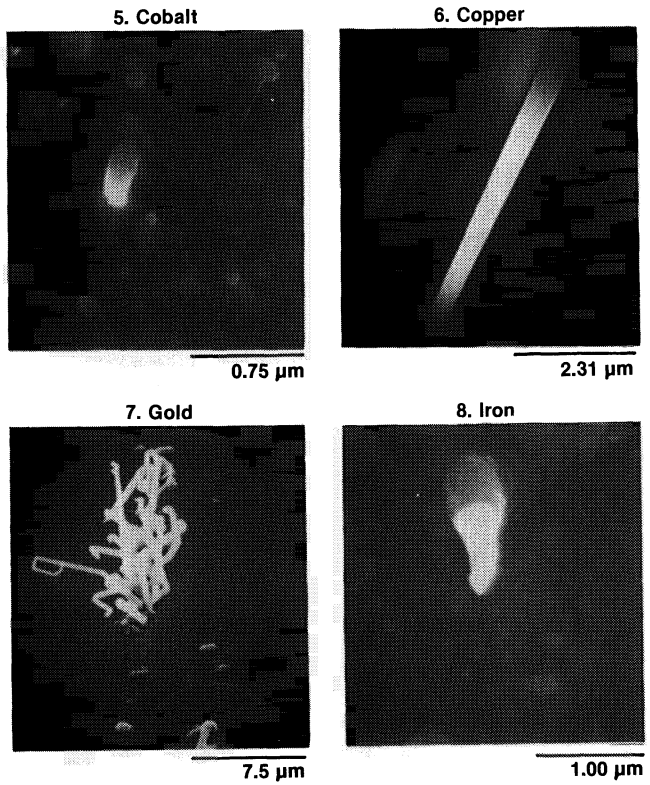


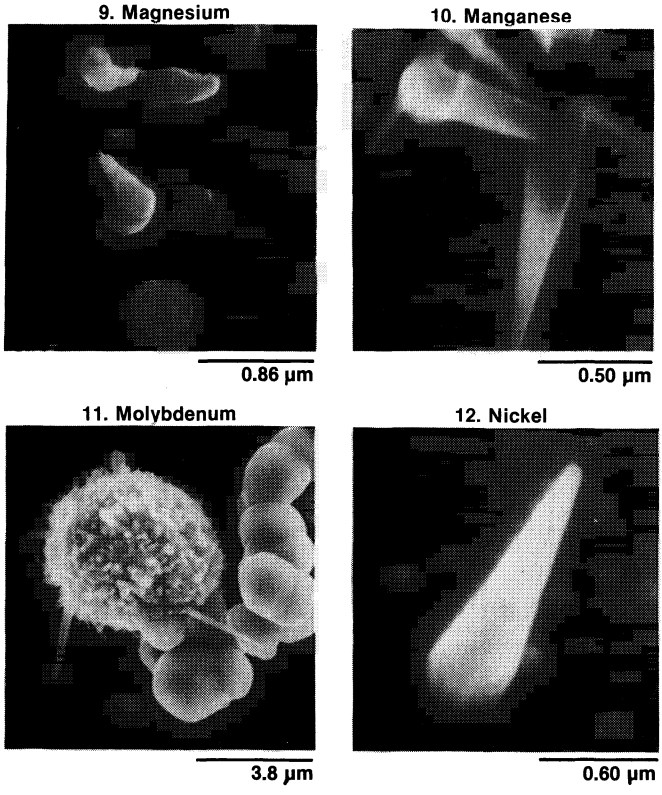
Figure 3. SEM micrograph of a circular defect with a polysilicon horn.



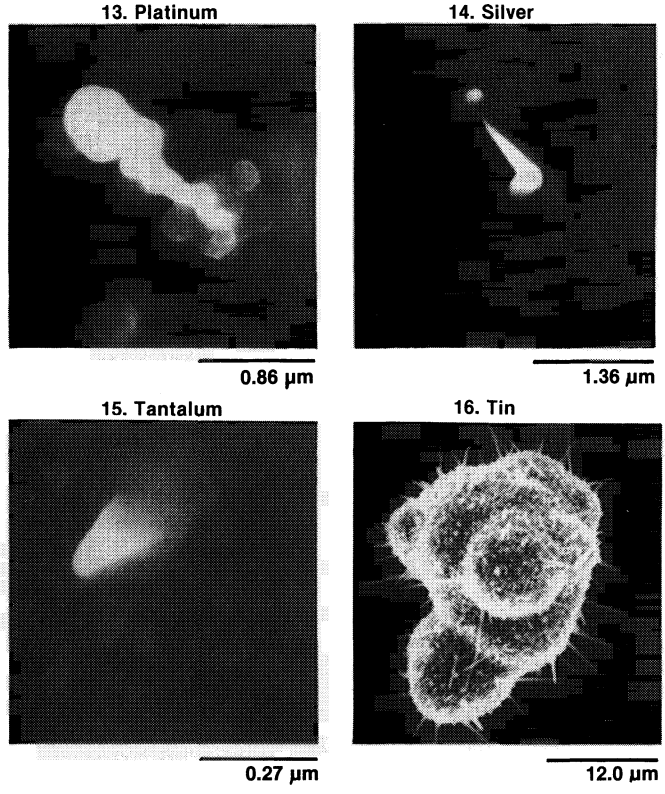
Appendix A: Examples of metallic interaction with polysilicon deposition.



Appendix A (cont.): Examples of metallic interaction with polysilicon deposition.

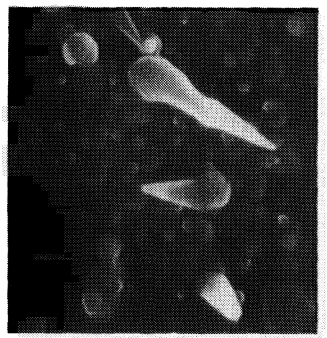


Appendix A (cont.): Examples of metallic interaction with polysilicon deposition.



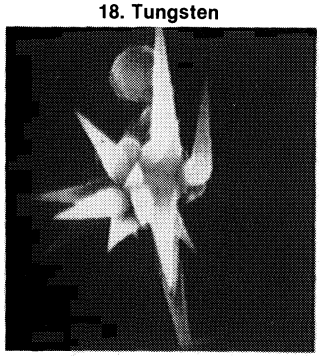
Appendix A (cont.): Examples of metallic interaction with polysilicon deposition.

17. Titanium



0.75 µm

18. Tungsten



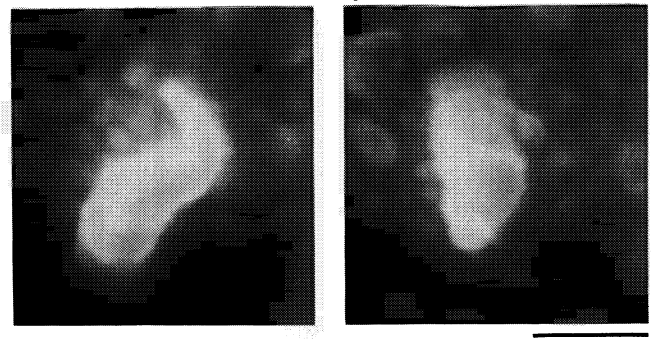
1.76 µm

19. Zinc

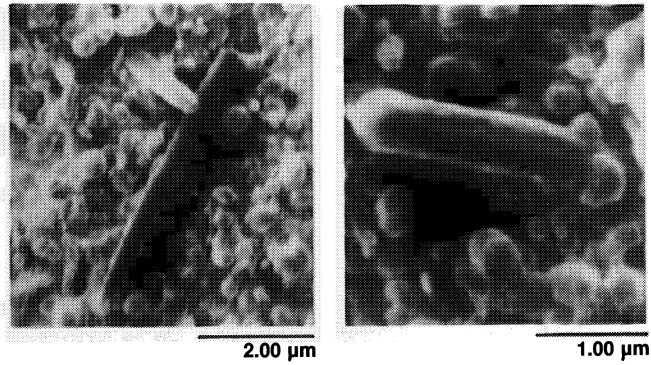
1.20 µm

Appendix A (cont.): Examples of metallic interaction with polysilicon deposition.

1. Potassium Hydroxide

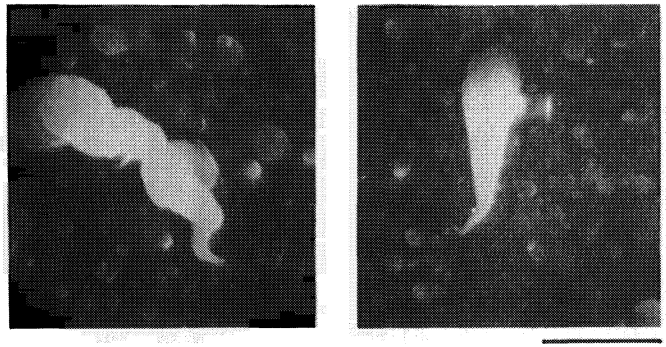


2. Sodium Hydroxide



Appendix B: Effects of alkali metal photoresist developers and polysilicon deposition.

3. Sodium Metasilicate



Appendix B (cont.): Effects of alkali metal photoresist developers and polysilicon deposition.

WAFER CLEANING AND DRYING TECHNIQUE IN LOW PRESSURES

I.Oki, T.Biwa, J.Kudo, and T.Ashida
Sharp Corporation
VLSI Research and Development Laboratory
2613-1 Ichinomoto - cho Tenri City,
Nara 632, Japan

ABSTRUCT

A wafer cleaning and drying process in low pressures is developed to prevent wafer contamination from chemicals absorbed in a teflon cassette during wet cleaning process. In this newly developed process, wafers in a teflon cassette are boiled in hot D.I. water in low pressures (-600 mmHg) and then dried in low pressures of N_2 ambient after drainage of the D.I. water. It is shown that the wafer contamination due to chemicals absorbed in a teflon cassette is prevented. The efficiency of cleaning narrow trenches is also improved with this process.

INTRODUCTION

In a wet cleaning process of LSI manufacturing, the drying technique in IPA (Isopropyl Alcohol) vapor is commonly used. However, wafer contamination during IPA vapor drying process from chemicals which are absorbed in teflon cassettes has been regarded as a serious problem. This is one of so called chemical carry-over effects. [1] To solve this problem , we have developed a contamination free wafer cleaning and drying process in low pressures. [2]

EXPERIMENTAL

We have developed a wafer cleaning and drying process as shown in Fig.1. The cleaning and drying sequence is as follows.

(1) Wafers in a cassette are placed in the inner quartz bath and hot D.I. water (60 °C) is injected into the quartz bath.

(2) The outer quartz chamber is depressurized by an aspirator to 150 - 200 mmHg (the wafer and cassette cleaning process)
(3) Pure N_2 gas is introduced into the outer chamber and D.I. water is drained.
(4) In N_2 ambient, the outer chamber is depressurized by an aspirator to 150 - 200 mmHg again. (the wafer and cassette drying process)

In the following experiments, CZ silicon wafers of P-type, 6-inch, resistivity of 15-20 ohm.cm were used.

The wafer surface contamination and particles after drying in IPA vapor and in low pressures are evaluated by TRXRF (Total Reflection X-Ray Fluoresence) mesurement [3] (TECHNOS :TREX 610), and laser particle counter (ESTEC : WIS 850). In this experiment, teflon cassettes chemically contaminated by H_2SO_4 is used.

The electrically active surface contamination on silicon wafers, after drying in IPA vapor and in low pressures, are evaluated by the surface photovoltage measurment [4] (SEMITEST : Surface Chage Analyzer, SCA), and the life time measurement by micro - wave reflection measuring apparatus (LEO : LTA-130A) .

The wafer cleaning effect is examined by dielectric breakdown measurement of trench MOS diodes with and without hot D.I. water boiling in low pressures after trench etching by RIE. Trench MOS diodes were fabricated according to the process flow shown in Fig.2

The cleaning of chemically contaminated teflon is examined by ion chromatography measurement of residual SO_4 ions in a teflon chip. The experimental procedure is shown in Fig.3

RESULTS AND DISCUSSIONS

Fig.4 shows the TRXRF spectra of Si wafers after drying in IPA vapor and in low pressures using chemically contaminated (by H_2SO_4) teflon casette. Surface concentration of sulfur, which is believed to be SO_4 ions evaporated from a teflon cassette, is more than 1 x E13 atoms/cm^2 in case of drying in IPA vapor while 2 x E11 atoms/cm^2 in case of drying in low pressures. It should be noted that the contamination level is lower than a starting wafer in the latter case.

Fig.5 shows the wafer surface particles (> 0.16um) after drying in IPA vapor and in low pressures using a chemically contaminated (by H_2SO_4) teflon cassette. In case of drying in IPA vapor, more than 1000 particles are detected, while in case of drying in low pressures, wafer surface particles are less than 100.

In case of wafer drying in IPA vapor, chemicals, which are absorbed in a teflon cassette, are evaporated from the cassette,and wafer contamination and particles are increased by those chemicals. In case of wafer drying in low pressures, such contaminations are prevented because chemicals are washed away from wafer surface by hot D.I. water boiling in low pressres, and the chemical contaminants from the teflon cassette is exhausted before reaching wafer surface in low pressures.

Fig.6 and Fig.7 shows the surface state density of Electrode (SCA probe) / Silicon interface and the wafer minority carrier lifetimes after drying in IPA vapor and drying in low pressures. Wafers are dipped in HF (1%) for 1 min and rinsed in D.I. water before drying to remove native oxide. The surface state density is lower in case of drying in low pressures. The average lifetime is 78 us in case of drying in low pressures and 33 us in case of drying in IPA vapor.

The degradation of surface state density and wafer minority carrier lifetime in case of drying in IPA vapor is considered to be due to the contamination of hydrocarbons (IPA fragment, for example $(CH_3)_2CH$ etc.) on silicon surface. [5]

Fig.8 shows the dielectric breakdown histgrams of trench MOS diodes with and without hot D.I. water boiling in low pressures after trench etching by RIE using $SiCl_4$ + N_2 gas. The breakdown frequency in low electric field region (2 - 5 MV/cm) is decreased by hot D.I. water boiling in low pressures.

This means that the contaminations in the trenches after RIE etching are removed by hot D.I water boiling in low pressures effectively.

Fig.9 shows the residual SO_4 ion concentration in a teflon chip (dipped in H_2SO_4 for 20 days) measured by ion chromatography after various cleaning processes. The efficiency of removing SO_4 ions in the cleaning in low pressures is substantially higher than the cleanig in hot D.I. water in atmospheric pressures.

The improvement of removing SO_4 ions from the teflon chip is explained as follows. In hot D.I. water boiling process in low pressures, a net-like structure of teflon molecules is broaden so that SO_4 ions trapped in the net-like structure are easily extracted into surrounding hot D.I. water. The efficiency of removing SO_4 ions is not improved in drying in low pressures. This means that the D.I. water ambient is necessary to remove SO_4 ions effectively.

CONCLUSIONS

A new wafer cleaning and drying process in low pressures has been developed and the following conclusions are obtained.

(1) Wafer surface contamination and particles caused by chemicals which are absorbed in teflon cassettes can be prevented by wafer drying process in low pressures.

(2) The efficiency of cleaning trenches and chemically contaminated teflon cassette is improved by hot D.I water boiling in low pressures.

ACKNOWLEGMENT

The authors would like to thank Mr. Ryuichiro Miyake for his support and helpful discussions.

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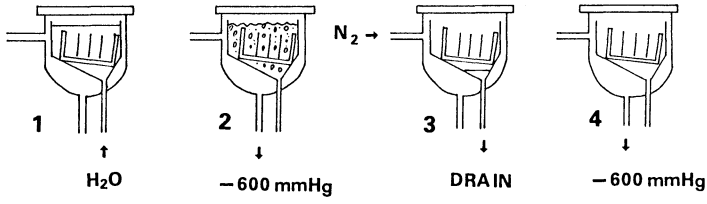


Fig.1
Apparatus and sequence of the wafer cleaning and drying process in low pressures

P(100) resistivity
15-20 ohm.cm
↓
CVD SiO_2 deposition
600nm
↓
CVD SiO_2 etching
(trench mask)
↓
trench etting
$SiCl_4$ + N_2
depth 2.5um
diameter 1um
↓
Hot D.I water boil
in low pressres
↓
HF (1%) cleaning
↓
Oxidation
950°C dry O_2 20nm
↓
N+ poly Si electrode

Fig.2
Process flow of trench MOS diodes

Teflon chip (35 cm^2)
in H_2SO_4 for 20 days
↓
Cleaning

A: No cleaning
B: Hot D.I water (60 °C) 5min
C: Hot D.I water (60 °C) boiling in low pressures (-600 mmHg) 5min
D: C + drying in low pressures (-600 mmHg) 5 min
E: D x 2

↓
Teflon chips are boiled in D.I. water (100 °C ,30 min) to extract residual SO_4 ions
↓
Ion Chromatograph measurement of SO_4 ions

Fig.3
Experimental procedure of cleaning evaluation of chemically contaminated teflon

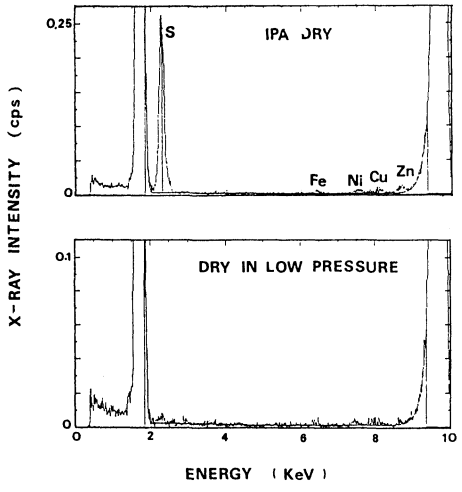


Fig.4
TRXRF spectra of Si wafers after drying in IPA vapor and drying in low pressures using chemically contaminated teflon cassette

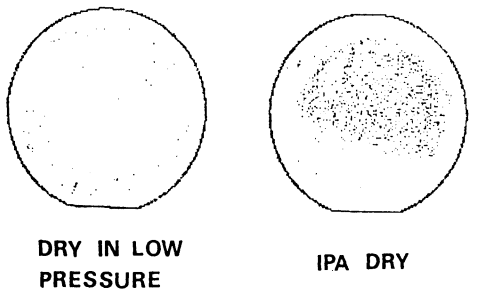


Fig.5
Wafer surface particle maps after drying in IPA vapor and drying in low pressures using chemically contaminated teflon cassette

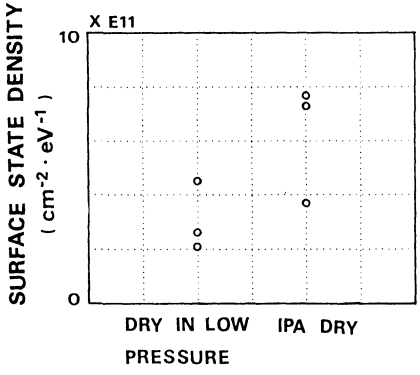


Fig.6
Surface state densities of Electrode (SCA probe) / Silicon interface after drying in IPA vapor and drying in low pressures

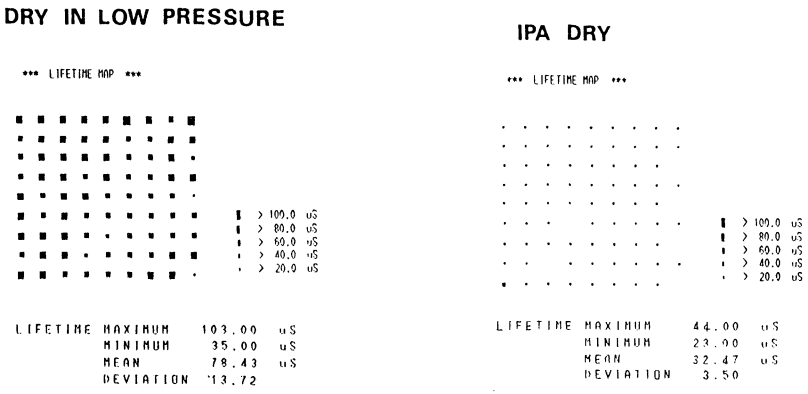


Fig.7
Minority carrier lifetimes after drying in IPA vapor and drying in low pressures

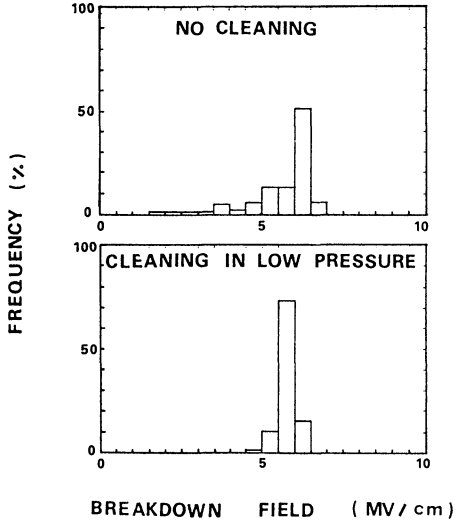
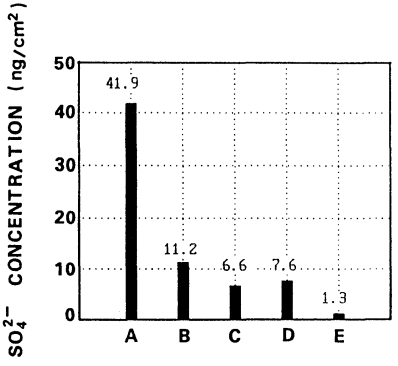


Fig.8
Dielectric breakdown histgrams of trench MOS diode with and without hot D.I. water boiling in low pressures



A: No cleaning
B: Hot D.I water (60 °C) 5min
C: Hot D.I water (60 °C) boiling in low pressures (-600 mmHg) 5min
D: C + drying in low pressures (-600 mmHg) 5 min
E: D x 2

Fig.9
Residual SO_4 ion concentration in teflon chip after various cleaning process

AN INVESTIGATION OF LIQUID-BASED PARTICLE DEPOSITION ONTO SEMICONDUCTOR WAFERS; THE ROLE OF ELECTROSTATIC WAFER/PARTICLE INTERACTIONS

Deborah J. Riley and Ruben G. Carbonell
Department of Chemical Engineering
North Carolina State University
Raleigh, North Carolina 27695-7905

ABSTRACT

The liquid-based deposition of particles onto semiconductor wafers has been investigated by exposing wafers to a variety of sample contaminants in stirred aqueous solutions. Test results clearly demonstrate the importance of electrostatic wafer/particle interactions in cleanroom-liquid particle deposition. While deposition from bulk DI water is often absent if an electrostatic repulsion exists, dramatic deposition can occur if an attraction exists between the wafer surface and the contaminant. Further, the importance of solution chemistry in defining deposition is demonstrated. Alterations of solution ionic strength or pH can dramatically alter the resultant particle deposition in a manner which is consistent with well-established principles of colloid science. If trace quantities of certain contaminants become present in the DI supply, particle charge reversals can occur which dramatically influence resultant deposition; despite the unplanned results that charge reversal leads to, depositions which occur have been found to be completely consistent with predictions based upon the electrostatic interactions which actually exist in the test system.

INTRODUCTION

The contamination of wafer surfaces from processing liquids is recognized as a serious problem in the microelectronics industry due to the adverse effects that contaminants have on device yields. While numerous researchers work to develop improved cleaning techniques for removing deposited particles from wafer surfaces, a preferred solution to the problem of particulate contamination might be the prevention or minimization of particle deposition before it occurs. If particulate contamination is ever to be controlled, however, a complete understanding of the mechanisms leading to deposition will be required. While such understanding is not yet complete, recent studies strongly indicate that well-known principles of colloid science can provide valuable insights into the problem of cleanroom-liquid particle deposition.

Most solid surfaces, when placed in an aqueous solution, acquire a surface charge. This charge usually results from the dissociation of ionizable groups on the solid's surface or from the unequal adsorption of potential-determining ions from the solution. With most oxides (including silicon dioxide), H+ and OH- are potential-determining ions, thus the pH of the solution determines the overall charge on the solid surface. At pHs below the point of zero charge (pzc) of the solid, the surface will be net-positive, and at pHs above the solid's pzc, the solid will be net-negative. For silicon dioxide, the pzc is approximately 2.

Because a charge exists at the solid surface, counterions are attracted to the solid/liquid interface [1]. Often, some counterions are accommodated very close to the solid surface in a region known as the Stern layer and the balance of the countercharge exists in a diffuse cloud around the solid. For a negatively charged surface (such as silicon dioxide at the pH of deionized water), more positively-charged counterions than negatively-charged co-ions are found in the liquid close to the oxide surface. These excess positive ions balance the intrinsic surface charge and, eventually, at some distance from the solid surface, the electrostatic potential of the particle/liquid system drops to zero; in the bulk solution, the number of positive ions and negative ions are equivalent. Outside the diffuse layer, the particle appears neutral to other surfaces in solution; if solid surfaces come close enough for their diffuse layers to overlap, the solids appear charged to one another and their double layers interact.

In 18 MΩ DI water, there are very few ions present, so very large diffuse layers result before surface charges are completely balanced. A calculation of the Debye length at 25°C in 18 MΩ DI suggests that diffuse layers can become approximately 1 μm thick [1]. Because of this, two surfaces which come within one or two microns of one other will begin to experience double layer overlap, and electrostatic interactions begin to influence the system. 18 MΩ DI water is a very common cleanroom liquid, so situations in which very large diffuse layers exist must be considered in examining cleanroom deposition. As the ionic strength of a solution climbs, double layers shrink in thickness, and the range of electrostatic interactions is reduced.

We have conducted a series of investigations in recent years which illustrate that the electrostatic interactions which exist in cleanroom liquids play a dominant role in the deposition process. Through the use of various wafer surfaces, test contaminants, solution pHs and ionic strengths, we have shown that deposition response is consistent with expectations based upon classical double layer theory. Further, when anomolous deposition behavior occurred in the laboratory, we were able to trace the problem to an unexpected alteration of contaminant charge; a charge reversal was observed in the laboratory which dramatically influenced particle deposition. The deposition which resulted during these anomolous test runs was consistent with the behavior that would be expected for the electrostatic interactions which were actually observed during these runs.

EXPERIMENTAL

To conduct this study of liquid-based particle deposition, a standard experimental technique was used for most tests. These experimental protocols have been described in slightly more detail previously [2-5].

Deposition of particles has occurred primarily onto 4-inch p-type silicon wafers having an orientation of <100>; in a limited number of studies, silicon wafers coated with a 1000 Å thick CVD silicon nitride film were utilized. Particle counts on all wafers were obtained with an Estek WIS-600 surface scanner with a lower detection limit of 0.3 μm.

Particles employed have included 1.6 μm soda-lime glass beads (Duke Scientific), 1.6 μm aminopropyl glass beads, 0.1-3.0 μm silicon nitride particles (Johnson Matthey), 0.35-3.0 μm quartz particles (Duke Scientific), and both 0.487 μm (Polysciences) and 1.00 μm (Duke Scientific) polystyrene latex beads. A System 3.0 Zetameter was used for the monitoring of particle zeta potentials, and at the pH of deionized water it was found that

the soda-lime glass, quartz particles, and polystyrene latex beads exhibit a negative charge; silicon nitride and aminopropyl glass were both found to be strongly positive. Note that the aminopropyl glass is obtained by subjecting the soda-lime glass to a nonaqueous silanization reaction [6] which leads to the attachment of aminopropyl groups to the bead surface. Whereas the soda-lime glass has a pzc of approximately 2, a pzc of 10.6 is recorded for the aminopropyl beads; this leads to the creation of a particle with a size and shape identical to the soda-lime glass but with an opposite charge in water. The soda-lime glass (zeta potential ~ -26 mV in DI water) and the aminopropyl glass (zeta potential ~ + 100 mV) were the particles used to collect most of the data presented in figures in this paper; the behavior of the other particles, however, has been found to be consistent with the behavior of the glass beads. The sign of the surface charge of the particles (relative to the sign of the wafer charge) has been observed as being the most important factor in determining the particles' deposition behavior.

The suspending media in these tests was 18 MΩ DI water; two different supplies of water have been utilized. All tests were performed at the MCNC facility in Research Triangle Park, North Carolina, and one source of water was their in-house supply. The alternative source of 18 MΩ DI water used in recent tests is a cleanroom facility at the North Carolina State University campus. To adjust the pH and the ionic strength of the DI water, quantities of KCl, HCl, or KOH were added to the water shortly before the particles were introduced. The HCl and KOH were low particulate grade aqueous liquids sold by Ashland Chemical Company (HCl) or Allied Chemical (KOH), and the KCl was an ultrapure grade powder sold by Johnson Matthey.

Before each experimental run, all glassware to be used and all wafer surfaces to be contaminated were cleaned and prepared. Glassware and quartzware were rinsed with acetone, rinsed with DI, submerged in 50:1 water:hydrofluoric acid, then rinsed again with DI. Silicon wafer surfaces were prepared by cleaning them with an SC1 solution. This clean involves submerging the wafers for 10 minutes in a 5:1:1 mixture of water, ammonia, and hydrogen peroxide heated to 75 °C, then rinsing in DI water. This clean removes organic contaminants and renders the wafers hydrophilic in nature (contact angle ~ 10°). When hydrophobic silicon wafers were tested (contact angle ~ 65°), the silicon wafers were prepared by cleaning in SC1, then submerging them into 1% HF for 30 seconds, followed by a 2 minute DI water rinse. Silicon nitride coated wafers were prepared with a 15 second dip in Buffered Oxide Etch and a subsequent DI rinse.

Unless otherwise noted, the following deposition procedure was used to collect data. Dilute seeded liquid solutions were prepared by pipetting a known volume of a concentrated solution of contaminant particles into a known volume of test liquid in a precleaned 7.2 liter quartz tank. The mixture was stirred using a magnetic stirrer set to the mid-range of its available stirring speeds. The liquid particle concentration in the solutions was monitored using a PMS IMOLV.3 liquid particle counter. Test wafers were placed in a standard chemical-resistant cassette holder, then lowered into the liquid-filled quartz tank where they remained in the contaminated solution for the desired test time. Once the holder was removed from the solution, the wafers were dried quickly using a spin rinser/dryer ('dry' mode only) in which they were rotated for 5 minutes at 1000 rpm while heated nitrogen was blown over them. For tests involving the use of KCl, KOH or HCl in the water solution, it was necessary to briefly (10 seconds) rinse the wafers in deionized water before drying in order to remove chemical residue. After the wafers were dried, they were scanned using the WIS-600 to determine the total number of deposited particles.

DEPOSITION BEHAVIOR FROM 18 MΩ DI WATER

When the described procedures were used to study particle deposition from microelectronics grade DI water, the importance of electrostatic interactions was clearly demonstrated [2,3]. A majority of these studies were done with the SC1-cleaned hydrophilic silicon wafers; because these wafers are covered with a native silicon oxide layer, the wafers are expected to have a negative charge in DI water (pzc ~ 2 for SiO_2).

When negatively-charged contaminants (soda-lime glass, PSL, quartz) were used in deposition studies with the hydrophilic silicon wafers, it was found that a linear relationship existed between the liquid particle concentration and the resultant wafer contamination. The magnitude of deposition, however, was relatively low and extremely high concentrations of particles could be present in the water (> 150,000/ml) and still lead to wafer contamination levels which did not saturate the available surface scanner. Further, it was found that time of exposure to the contaminated water was irrelevant in terms of how contaminated the wafer became; a wafer submerged into a seeded DI solution for 30 minutes became contaminated with approximately the same number of particles as a wafer submerged for only 30 seconds (Figure 1). Note that in Figure 1, and in subsequently presented graphs, the adhered particle concentration (y-axis) is presented as a normalized wafer coverage. This value is the total number of particles that would deposit during the test onto a four inch wafer if the liquid particle concentration had been 10,000 particles/ml. Because a linear relationship between coverage and liquid particle concentration was noted for all particles tested, this normalized wafer coverage was readily found by dividing the actual number of particles found on the wafer surface by the liquid particle concentration that was recorded, then multiplying by 10,000.

The obvious lack of a submersion time dependence for negatively charged particles suggests that these contaminants do not deposit from the bulk liquid onto the wafer surface while the wafer remains submerged in liquid. Further studies [2,3] have conclusively demonstrated that native-oxide covered silicon wafers will not actually become contaminated with negatively-charged test particles until the wafers are withdrawn from a seeded DI water solution and dried. Particles which adhere to the wafer surface are those particles which remain suspended in the thin film of liquid clinging to the wafer as it enters the spin dryer. As the wafer dries, the thin film of water is removed, and some of the particles are forced into contact with the wafer surface where they adhere. The repulsion between the negatively charged particles and the wafer surface is so strong, in fact, that simply rinsing the wafers before they are dried effectively eliminates particle deposition. Negatively-charged particles in the contaminated water film are either very weakly attached to the wafer surface or remain suspended in the liquid and do not contact the wafer before drying occurs; once the wafer is dried, however, some particles become attached, and it becomes much more difficult to remove these particles from the wafer surface. Once contact has occurred, strong, short-range van der Waals forces are able to hold deposited particles in place. Deposition results reported by Michaels, et al. [7] and Itano, et al.[8] are consistent with observations made here that very little bulk deposition of negatively-charged particles occurs onto a negatively-charged wafer surface from deionized water media.

In contrast, when positively-charged particles (aminopropyl glass, silicon nitride) were used in this investigation, results were dramatically different than results observed with negatively-charged particles. When an electrostatic attraction existed between the particle and the wafer surface (positively-charged particles and a negatively-charged native oxide wafer), a linear relationship between liquid particle concentration and wafer coverage

was still observed, but the magnitude of deposition at a given liquid concentration was dramatically increased. Further, submersion time in the seeded solution was found to have a strong influence on wafer contamination. Figure 1 illustrates not only the increased magnitude of deposition occurring when positively charged particles are used rather than negatively charged particles, but also the relative importance of submersion time for the two types of test particles. While this plot was created for soda-lime glass and aminopropyl glass beads, it is representative of the behavior observed when all negatively-charged and positively-charged particles were tested.

The importance of time suggests that deposition from bulk liquid while the wafer remains submerged is an important deposition mechanism when an electrostatic attraction exists between a particle and the wafer surface. Further studies, in fact, suggest that bulk deposition is the primary contamination mechanism in these situations. When doing several 5 minute submersion tests with silicon nitride particles and hydrophilic silicon surfaces, we found that aproximately 50-60% of deposited particles were becoming attached from bulk liquid while the wafer was submerged, 30-40% of the particles appeared to attach during insertion of the wafer into the solution, and roughly 10% of the positively charged particles appeared to adhere through the withdrawal (thin film) mechanism. If longer submersion times are used, these percentages become even more heavily weighted towards particle deposition from bulk liquid. When positively-charged particles were used, it was not possible to prevent deposition by rinsing the wafers before they were dried. In contrast to the behavior found when a double layer repulsion controlled the system, deposition in the presence of a double layer attraction occurred before the wafer was dried and appeared to be strong in nature.

When alternative wafer surfaces were tested, results continued to support the idea that electrostatic interactions play an important role in cleanroom liquid-based deposition. Because silicon nitride particles are found to have a positive zeta-potential, we suspect that silicon nitride wafers will have a positive charge in water. When doing tests with nitride-coated wafers, we indeed found that they readily attracted *negatively* charged particles yet repelled the positively charged particles that are so readily attracted to native-oxide silicon wafers. While this deposition trend is opposite to the response found with the hydrophilic silicon wafers, it is consistent with expectations based upon the anticipated electrostatic interactions in the system. We have also noted that particles on silicon nitride coated wafers are not readily removed by the SC1 clean that works well on silicon and silicon oxide wafers. Silicon nitride wafers were extremely difficult to reclean and salvage for future work; the insensitivity of nitride wafers to popular chemical cleans suggests that nitride surfaces may offer an interesting challenge to those designing improved cleaning techniques.

Silicon wafers treated with hydrofluoric acid (HF) were also considered in deposition studies with 18 MΩ DI water [4]. Silicon wafers treated with HF are hydrophobic in nature and, as a result, deposition from the thin film mechanism becomes impossible (there is no film of water clinging to these wafers as they enter the dryer). Common experience of cleanroom workers would suggest that hydrophobic wafers more readily collect contaminant particles than their hydrophilic counterparts, yet results of this investigation suggest that they are no more likely to collect particles from bulk solution than native oxide covered (hydrophilic) silicon wafers. Despite treatment with HF and an overall hydrophobic surface behavior, test results suggest that regions remain on the silicon surfaces which are ionizable in aqueous solutions and lead to a negative surface charge. As with hydrophilic wafers, negatively-charged particles showed no tendency to deposit from

bulk liquid onto these hydrophobic wafers, while deposition of positively charged contaminants was readily apparent. Hydrophobic wafers did, however, show an increased tendency to gather hydrocarbon film contamination from the liquid environment, and the hydrophobic surfaces appeared to be extremely sensitive to gas/liquid interfacial exposure. If the wafers were sprayed with water in a quick dump rinser, background contamination counts rose dramatically over those found when a cascade style rinse was used. This noted sensitivity to interfacial contact may be largely responsible for the contamination problems experienced when hydrophobic wafers are processed.

THE INFLUENCE OF SOLUTION pH AND IONIC STRENGTH

Alteration of either the ionic strength or the pH of the liquid solution should theoretically have a notable influence on wafer contamination levels if electrostatic interactions play an important role in cleanroom-liquid particle deposition. Double layers are extremely thick in 18 MΩ DI water, yet increasing the ionic strength causes these layers to shrink dramatically; whereas double layer thicknesses of approximately 1 μm exist in 18 MΩ DI at 25°C, Debye lengths drop to about 1 nm in a solution containing 0.1 M of a 1:1 electrolyte [9]. Increasing ionic strengths can significantly reduce the range and thus the importance of electrostatic interactions. When pH is altered, the surface charges of both the wafer and the particle change because H+ and OH- ions in solution are potential determining for the surfaces being considered in this investigation. In acidic solutions, surfaces become less negative (with the soda-lime glass and the native oxide wafers becoming nearly neutral around a pH of 2). In solutions that are strongly basic, surfaces become more negative (or, for the aminopropyl glass beads, the particles go from being positively-charged to negatively-charged if the pH exceeds 10.6).

When investigating the influence of solution chemistry, it was indeed found that pH and ionic strength could have a strong impact on resultant deposition [5]. Figure 2 illustrates the impact that increasing ionic strength (through the addition of KCl) had on the deposition of soda-lime glass onto hydrophilic silicon wafers. To collect data in Figures 2 - 5, it was necessary to briefly rinse the wafers before drying to remove chemical residue; for that reason, deposition in Figure 2 at low ionic strengths is nearly absent. In these figures, an ionic strength of 2×10^{-6} M represents deposition from deionized water without the addition of chemicals.

In Figure 2, no evidence of deposition from bulk solution is observed if the ionic strength is very low; thick diffuse double layers at low ionic strengths are sufficient to prevent deposition in this system where an electrostatic repulsion exists between the particles and the wafer surface. As the ionic strength climbs, however, evidence of bulk deposition becomes apparent (larger wafer coverages after a 5 minute submersion than after a rapid immersion are indicative of active bulk deposition occurring in the system). The fact that shielding of electrostatic repulsions led to increased particle deposition confirms the suggestion that electrostatic interactions play an important part in this contamination problem. While deposition is induced in this repulsive system through a reduction in the range of double layer interactions, however, it was noted that the adhesion was not particularly strong. The use of a much stronger rinsing technique before drying led to a marked reduction in the number of particles that deposited in this system. While bulk deposition was still suggested by the data collected using a stronger rinse, the number of deposited particles attached firmly enough to withstand the strong rinse was relatively low.

Figures 3 and 4 are also presented for collection of soda-lime glass onto hydrophilic silicon wafers. Figure 3 shows results when HCl is used as the chemical additive and Figure 4 shows the influence of KOH on particle deposition. Note that while the addition of KCl (Figure 2) led to the alteration of ionic strength only, HCl and KOH lead to the alteration of both ionic strength and pH. In Figure 3, as the ionic strength climbs, the pH drops (at an ionic strength of 0.01 M, the pH is 2); in Figure 4, as the ionic strength climbs, the pH also rises (at an ionic strength of 0.01M, the pH is 12). When considering the influence of pH, it should not be forgotten that the double layers are shrinking as acid or base concentrations rise; these figures reflect not only the influence of pH, but also the influence of ionic strength. Comparison should be made of Figures 3 and 4 to Figure 2 for an illustration of the impact that pH alteration has on the deposition process.

When pH was reduced through the addition of HCl, deposition of soda-lime glass was found to be encouraged (compare Figures 2 and 3). This would be anticipated as both the wafer surface and the particle have a pzc of 2; as the pH drops, the surfaces become less negative. At a pH of 2, the repulsion should nearly vanish as both surfaces are approximately neutral. Deposition is encouraged with HCl because the repulsion preventing deposition is minimized. When a stronger rinsing technique was used, we found that the particles depositing when the pH was greater than 2 were relatively weakly bound (particle counts were reduced by the stronger rinse). Those particles depositing when the pH was 2 or lower, however, appear to be firmly attached; the stronger rinsing technique did not lead to significantly altered particle counts when the HCl concentration exceeded 0.01 M. This result is not unexpected, as the repulsion between the wafer and the particle should be nearly nonexistent at these lower pHs.

When pH was increased with KOH, deposition was discouraged compared to the situation involving ionic strength considerations alone (compare Figures 2 and 4). In this situation, the charge on each surface becomes increasingly negative, so the repulsion between surfaces becomes greater. While the higher ionic strength at high KOH concentrations tends to minimize the importance/range of the double layer repulsion, the fact that the charges are stronger than when KCl was the additive helps reduce deposition somewhat over the situation when the neutral salt was added. Note that when stronger rinses were used to collect data with KOH, the stronger rinse was able to remove all deposited particles. The repulsion that remained between the particle and the wafer at high pHs apparently led to relatively weak adhesion.

While this test series using soda-lime glass confirms the importance of solution chemistry in the particle deposition process, complimentary experiments using aminopropyl glass were also supportive of the role played by electrostatic interactions. Figure 5 illustrates the influence that ionic strength has on the deposition of aminopropyl glass beads onto hydrophilic silicon. For these surfaces, a double layer attraction is present at the pH of deionized water. In this system, increasing ionic strength above that of DI actually led to a slight reduction in bulk deposition; increases beyond a certain point, however, did not appear to encourage significant further reduction in deposition. For systems experiencing an electrostatic attraction, deposition may largely be controlled by the rate of particle transport to the vicinity of the wafer surface. When double layer thicknesses are extremely large (DI water) slight enhancement over this transport limit may occur, but for most ionic strengths tested, deposition is simply controlled by how fast diffusion and convection bring particles into the vicinity of the wafer surface. When smaller particles were tested, the impact of ionic strength was even smaller than indicated in Figure 5. Increasing ionic strength for systems experiencing electrostatic attraction does not impact deposition as much

as when a repulsion is present, because the electrostatic interaction ceases to be rate controlling. The wafer surface can effectively be thought of as a 'perfect sink' for all contacting particles as long as a repulsive interaction does not interfere. When aminopropyl glass was tested, stronger rinsing techniques did not have a significant impact on contamination levels indicating strong adhesion. Acidic solutions were found to have minimal influence on the magnitude of bulk deposition recorded, but basic solutions led to a dramatic drop in contamination as the particle became negatively charged and a repulsion between particle and wafer surface was introduced.

CHARGE INSTABILITY

Finally, anomalous test results obtained in the laboratory using certain DI water supplies may have important implications for researchers trying to control liquid particle deposition in a cleanroom environment. When the source of these unexpected results was identified, further support was found for the idea that electrostatics play a major role in the liquid-based contamination problem.

Beginning in late 1990, unexpected test results began to be observed in deposition studies; when negatively charged particles were initially placed into deionized water, they would not deposit significantly onto hydrophilic wafers as anticipated. As the contaminated solution became older, however, bulk deposition became evident and eventually the solution deposited particles as rapidly as if a positively charged particle were being tested. Attempts to find a possible source of this altered behavior eventually indicated that the water itself was responsible. All tests were done at the MCNC facility, and it was MCNC's water supply which led to these unexpected test observations. We found, however, that when we transported DI water from the NCSU cleanroom to the MCNC facility to repeat the test, this same aging phenomenon was absent (Figure 6). The tests comparing the two different water supplies were conducted on the same day using all of the same equipment in the same cleanroom facility; the only difference was the water source, yet the impact on deposition was dramatic. This was repeated on numerous different test days, yet the conclusions were always the same: deposition from NCSU DI water led to low contamination levels consistent with what is expected for a system experiencing electrostatic repulsion, but deposition from MCNC water now led to an obvious aging phenomenon in which deposition eventually proceeded as if the electrostatic repulsion were not present.

Based on the expectations we've developed regarding double layer interactions, deposition from the MCNC water supply behaves as if the particles (which should be negatively charged at the pH of deionized water) are becoming positively charged over time. Measurements of particle zeta potentials confirmed that this is actually what is occurring. Quartz and soda-lime glass particles were suspended in NCSU's DI water at various liquid particle concentrations, and it was found that negative zeta potentials were always recorded. When this same test was repeated with MCNC water, however, a concentration-dependent charge reversal was observed. At high particle concentrations (typical for studies of colloid properties and deposition outside of a cleanroom environment), the particles were found to be negatively charged as anticipated. At low particle concentrations, however, the measured zeta potentials were positive at equilibrium (Figure 7). Deposition studies take place at liquid particle concentrations that are far below the apparent cross-over concentration for these particles, and thus the deposition studies occur far within the region where positive zeta potentials result.

The exact cause of the reversal is unknown at this time, but such behavior would be consistent with the presence of trace quanitities of a hydrolyzable polyvalent cation in the water which adheres to the particle surface and alters its properties. Such reversals are well documented for silicon oxide in the colloid literature, but significant quantities of the ion are usually needed for the reversal to occur. These reported observations, however, are made with much larger liquid particle concentrations than we are concerned with here, and it is known that the ratio of total particle surface area to total ion concentration is critical in determining whether or not reversal results. If the concentration of the trace impurity is extremely low (as it must be to not be detected with routine water monitoring), such an unplanned reversal could occur only in water having extremely low particle counts. While such a reversal would therefore not be an issue in water supplies with a high concentration of particulate contamination, it could have important implications in a cleanroom environment where particle counts are very low. It is especially intriguing that we believe the MCNC water (which leads to the reversal) to be of even higher quality than the NCSU water (which does not readily undergo reversal). Understanding of this phenomenon is not yet complete and is an area of continuing investigation; that the anomalous deposition behavior was directly traced to an alteration of particle zeta potential, however, is further evidence for the fact that electrostatic interactions play a crucial role in cleanroom liquid deposition.

ACKNOWLEDGMENT

This work was done with the financial support of the Research Triangle Institute, the Semiconductor Research Corporation, and the EPA Center for Hazardous Waste Minimization at North Carolina State University.

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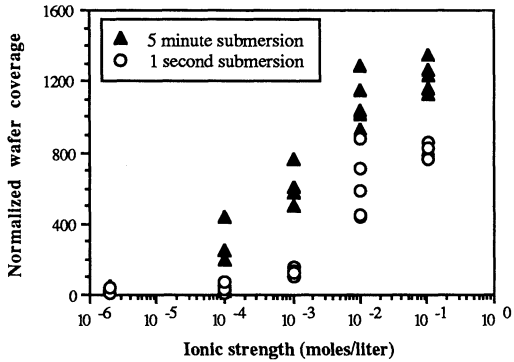

Figure 3: The influence of an acid (HCl) on the deposition of soda-lime glass onto hydrophilic silicon. As ionic strength increases, pH decreases.

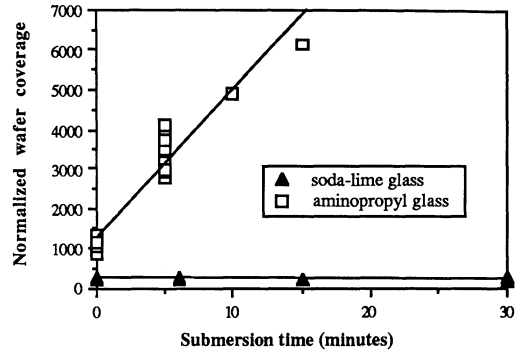

Figure 1: Wafer contamination as a function of submersion time. Soda-lime glass is repelled by the wafer, aminopropyl glass is electrostatically attracted.

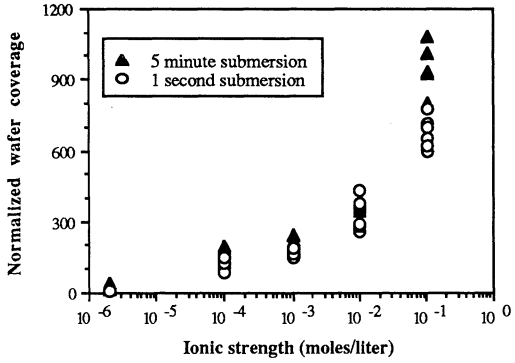

Figure 4: The influence of a base (KOH) on the deposition of soda-lime glass onto hydrophilic silicon. As ionic strength increases, pH increases.

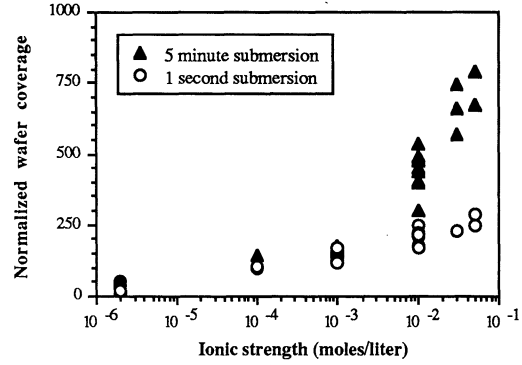

Figure 2: The influence of ionic strength on the deposition of soda-lime glass onto hydrophilic silicon. KCl is used to alter ionic strength.

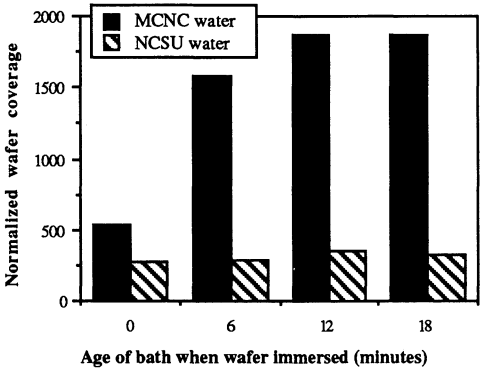

Figure 6: Number of soda-lime glass beads deposited on hydrophilic silicon after a five minute submersion in an aging DI solution.

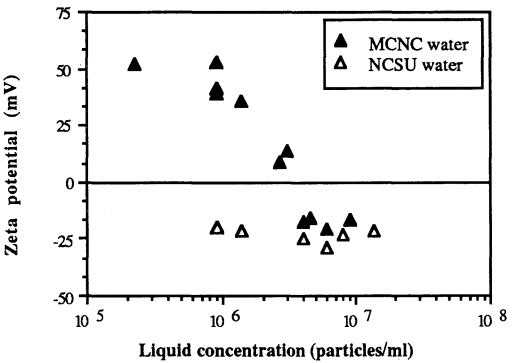

Figure 7: Zeta potential of quartz as a function of liquid particle concentration when suspended in two different supplies of DI water.

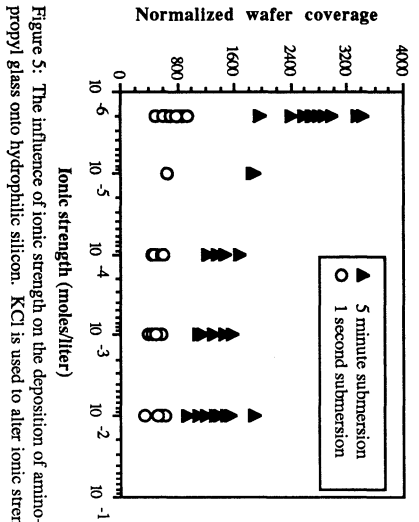

Figure 5: The influence of ionic strength on the deposition of amino-propyl glass onto hydrophilic silicon. KCl is used to alter ionic strength.

THE ACTIVITY OF HF/H_2O TREATED SILICON SURFACES IN AMBIENT AIR BEFORE AND AFTER GATE OXIDATION

Ara Philipossian

Digital Equipment Corporation
77 Reed Road, Hudson, Massachusetts 01749 USA

A strong correlation is observed among surface charge, contact angle and native oxide thickness in which, up to 10,000 minutes of exposure time to ambient air, the liquid-HF/H_2O and vapor-HF/H_2O treated surfaces seem to undergo three distinct periods of evolution. The results indicate that the vapor-HF/H_2O treatment yields surfaces with greater activity in ambient air. The trends, which are explained by considering the reaction between unpassivated trivalent silicon and hydroxyl groups, are shown to be consistent with XPS data on surface carbon, fluorine and oxygen. Following thermal oxidation, the total oxide charge, interface quality factor, oxide thickness, and contact angle are stable over time. This is attributed to the complete surface oxide coverage. The thermal oxide thicknesses of liquid-HF/H_2O and vapor-HF/H_2O treated surfaces are different and can be correlated to pre-oxidation surface XPS results. Following thermal oxidation, no differences between vapor-HF/H_2O and liquid-HF/H_2O are detected in terms of oxide charge, interface quality factor and contact angle.

INTRODUCTION AND MOTIVATION

ULSI CMOS technologies necessitate detailed understanding of the activity of freshly etched silicon surfaces in ambient air prior to gate insulator growth. An alternative, and at times, a compliment to the closed manufacturing concept, is the direct method of reducing the activity of silicon surfaces in ambient air by developing wafer

cleaning procedures for effective surface passivation. It is well known that cleaning procedures based on a combination of SC-1 and SC-2 chemistries are very effective in removing trace metallics and particles (1,2). Such procedures, when performed as the final cleaning step, result in the formation of a 6 to 10 Angstroms chemical oxide layer on top of the silicon (3,4). The resulting hydrophilic surface has been shown to have a high degree of activity in humid, ambient air. This has been attributed to the combined effects of Si-OH condensation and hydrolization of bridging Si-O-Si sites by water vapor, thus causing periodic film shrinkage and swelling, and in turn giving rise to surface heterogeneities (3,4). Moreover, as gate insulator thicknesses decrease to less than 75 Angstroms in order to satisfy ULSI device requirements, such chemical oxides become increasingly harder to tolerate.

On the other hand, procedures which employ hydrous or anhydrous HF chemistries as their last step are generally regarded to have less activity in ambient air. In fact recent investigations have shown that such processes lead to the near ideal electrical passivation of silicon surfaces (5,6). The passivation has been mostly attributed to the presence of Si-F and Si-H groups (5-9). It should be noted that processes using liquid-HF/H_2O as the final cleaning step have traditionally been regarded as substantial particle adders, however recent advances in wet chemical cleaning technology have ensured adequate cleanliness (10). While there have been conflicting reports regarding Cu contamination following such processes (11,12), one benefit of note is their effectiveness in removing contaminants such as Fe, Br, and Zn which are not entirely removed by RCA cleaning (11).

The hydrophobicity of liquid-HF/H_2O treated silicon surfaces has also been the subject of numerous investigations. Contact angle measurements have identified the presence of hydrocarbon and fluorocarbon containing compounds following liquid-HF/H_2O treatments irrespective of DI water rinsing (13,14). Similar residues have been observed on wafers after vapor-HF/H_2O and DI rinse treatments (15).

This study is yet another undertaking at characterizing the activity of silicon surfaces in ambient air following liquid-HF/H_2O and vapor-HF/H_2O chemistries. The work is motivated by the fact that more information is needed regarding the chemical and physical activity of silicon surfaces following HF-based sacrificial thermal oxide removal in commercially available, low pressure, continuous flow

vapor-HF/H_2O systems (16). In such systems, oxide removal occurs by the action of a thin condensed layer of hydrofluoric acid and water mixture. The ability to desorb condensed matter from wafer surfaces through rapid pumpdown prior to and following oxide removal is considered unique and may play an important role in the overall activity of freshly exposed silicon surfaces. This study will compare the effectiveness of such a process to the more conventional wet bench approach. The work will also attempt to address the quality and activity of thermally oxidized silicon following such treatments.

Literature review has identified the most prevalent technique for analyzing native oxide growth and Si-F bonding on silicon surfaces following HF treatments to be X-Ray Photoelectron Spectroscopy, XPS (5-7,9,14). Furthermore, High Resolution Electron Energy Loss Spectroscopy has shown these surfaces to be mainly comprised of Si-H groups (3,4). Contact angle measurements have also shed light on the hydrophobicity and hence the interaction of silicon in the presence of humid, ambient air (13,17,18). In an effort to improve our understanding of the complex mechanisms which account for the activity of silicon surfaces, this study hopes to determine whether the novel technique of Surface Charge Analysis, SCA (19-23) can be used to bridge the gap between XPS and contact angle data. SCA allows the immediate and non destructive characterization of the electronic properties of the Si/SiO_2 system without requiring gate electrode formation. Since SCA can be applied to chemical and thermal SiO_2 films of any thickness, the technique is believed to be appropriate for studying the activity of HF treated silicon surfaces in ambient air, as well as the quality and stability of thermal oxides grown on such surfaces.

EXPERIMENTAL

Monitor wafers were prepared by growing approximately 150 Angstroms of sacrificial thermal oxide on 1 to 10 ohm.cm, P-100, 125 mm, CZ silicon substrates. The wafers were then implanted with boron at a dose and energy of $1E10/cm^2$ and 110 KeV, respectively. The implantation was performed to yield oxide conditions typically encountered in CMOS IC fabrication lines prior to sacrificial oxide strip and gate oxide growth. Following ion implantation, a split was made at sacrificial oxide strip where half of the monitor wafers were subjected to liquid-HF/H_2O, and the other half to vapor-HF/H_2O conditions.

The liquid-HF/H_2O treatment was considered as the control

experiment, and was performed in a conventional wet bench. The procedure involved submerging monitor wafers in a 10:1 water and hydrofluoric acid bath at room temperature for 40 seconds in order to ensure complete removal of the sacrificial oxide. The wafers were then removed from the bath and rinsed in DI water for 8 minutes before undergoing a 5 minute nitrogen dry. The TOC of the DI water at the point of use was approximately 25 ppb. The vapor-HF/H_2O tests were performed in an Edge-2000 apparatus manufactured by Advantage Production Technology, Inc. Detailed description of various features of the system and typical cleaning procedures may be found elsewhere (16). In our case, the entire process was performed at room temperature. Following wafer insertion and initial desorption, the system was purged with argon for 4 seconds during which the chamber pressure was raised to approximately 1.6E-1 atm. This was followed by a 55 second oxide strip. The strip was performed by combining two streams of argon, which contained various amounts of chemicals, and directing them towards the wafer surface. The first stream was formed by flowing 1 SLM of argon through the vapor phase of an azeotropic mixture of water and hydrofluoric acid contained in a 30° C canister. The second stream, which provided supplemental water, was formed by flowing 4 SLM of argon through the vapor phase of a pure water system contained in a 60° C canister. A total pressure of 1.6E-1 atm was maintained during this interval. Upon etch completion, a secondary desorption was invoked by pumping the system, for 8 seconds, down to 2.6E-5 atm. The cycle ended by back filling of the etch chamber with argon, followed by wafer removal.

After the sacrificial oxide strip, the monitor wafers were further split into two groups containing equal numbers of vapor-HF/H_2O and liquid-HF/H_2O treated samples. The first group was used in Phase-1 of the study, and the second group in Phase-2. All post strip processing and analyses were identical for both groups.

In Phase-1, most of the wafers were subjected to a series of time-dependent characterizations during which the surface charge, the water/air/solid contact angle, and the apparent native oxide thickness were measured as a function of exposure time to ambient air at an average temperature of 20.5° C, and an average relative humidity of 45 percent. Exposure times ranged from several minutes to several days. Some freshly etched monitor wafer were analyzed with XPS in order to determine their surface composition.

The surface charge was measured using the Surface Charge Analyzer, SCA, which had a proven precision of 1E10/cm^2. The tech-

nique which was based on photoelectrical measurements (19,20) used low intensity light chopped at high frequencies. The resulting surface photovoltage signal was then used to characterize the electrical properties of the Si/SiO_2 system. The surface charge values were determined from the total charge of the Si/SiO_2 system with the silicon surface biased to align the Fermi level with the intrinsic level. Under such conditions, the contribution of interface traps to the charge could be neglected. As no additional processing was required, our measurements directly reflected variations in the HF/H_2O treated surfaces.

The contact angle was measured using a conventional optical goniometer. The technique, which had a precision of $\pm 2°$, involved visual measurement of the contact angle via a microscope equipped with a built-in protractor. A five microliter droplet of DI water was first introduced onto the substrate, and was allowed a certain amount of time to spread on the surface before contact angle measurements were made on both sides of the droplet. The average value of the left-hand-side and right-hand-side contact angles was reported for greater accuracy. The droplet age, was kept constant at 3 minutes. Precise control of the droplet age was very important due its pronounced effect on contact angle.

The apparent native oxide thickness was measured with a precision of ± 1 Angstroms using ellipsometery at a wavelength of 6328 Angstroms, beam angle of 70° and a fixed refractive index of 1.460. The results were then correlated to XPS data on actual native oxide thicknesses obtained from the literature.

In Phase-2, the monitor wafers were first divided into five groups containing equal numbers of wafers treated with liquid-HF/H_2O and vapor-HF/H_2O and were then subjected to a waiting period in ambient air. The purpose for these tests was to determine whether any correlations existed between thermal oxide characteristics and the exposure of HF/H_2O treated silicon surfaces to ambient air prior to thermal oxidation. Five waiting periods of 25, 55, 125, 1440, and 1560 were used. Wafers from all five groups were then combined and processed through a 150 Angstrom thermal gate oxidation cycle at 950° C. The initial temperature ramp-up and stabilization intervals were done in a diluted oxygen mixture, while the main oxidation was performed using oxygen containing 3 percent chlorine. The procedure included a 30 minute post oxidation nitrogen anneal. Following gate oxidation, selected groups of wafers were subjected to a series of time-dependent characterizations during which the total oxide charge, the Si/SiO_2 interface quality factor, the contact angle, and the thermal

oxide thickness were measured as a function of exposure time to ambient air.

It should be noted that surface charge analysis of substrates having oxide thicknesses of greater than a few monolayers (i.e. a thermal oxide) is a measure of the total oxide charge, and does not necessarily reflect charge density in the Si/SiO_2 or SiO_2/air interfaces. It should also be noted that, upon oxidation of the HF treated silicon surfaces, very high quality Si/SiO_2 interfaces were obtained. These corresponded to Si/SiO_2 interface state density values which were lower than the resolution limits of the SCA technique (i.e. less than $1E10/eV.cm^2$). However, for comparative purposes, the relative rate of change in the depletion width as a function of induced charge for each sample was determined from which a positive, numerical, and qualitative indication of the interface state density, termed the interface quality factor, IQF, was extracted.

RESULTS AND DISCUSSION

Phase-1; Silicon Surface Characterization Following HF Treatments:

Figure 1 shows the variation of surface charge with ambient air exposure time for both liquid-HF/H_2O and vapor-HF/H_2O treated surfaces. The error bars represent one standard deviation. The vapor-HF/H_2O treated wafers experience greater change and can be characterized as the more active of the two types. This can also be deduced from the larger standard deviation associated with this treatment. Upon exposure to ambient air, liquid-HF/H_2O and vapor-HF/H_2O treated surfaces undergo three distinct evolutionary periods:

The initial evolutionary period persists up to approximately 100 minutes of air exposure time, during which, the wafers exhibit very low levels of activity. This is believed to be mainly due to hydrogen passivation of the silicon surfaces.

The intermediate evolutionary period ranges from approximately 100 to 1000 minutes. During its preliminary stages, the wafers experience the rapid annihilation of the hydrogen passivation layer, and the subsequent formation of positively charged trivalent silicon centers at the surface. The rapid formation of such positively charged centers, is readily detected by the surface charge analyzer. During the secondary stage of this period, the rate of change of surface charge with ambient

air exposure time begins to decrease and eventually diminishes. This is believed to be due to the gradual reaction of the available trivalent silicon centers with airborne hydroxyl groups thus resulting in the formation of electronegative Si-OH sites. The fact that there seems to be a delay time associated with this charge compensation process may be attributed to the presence of an incubation period prior to native oxide formation (14,24).

The final evolutionary period ranges from approximately 1000 to 10000 minutes (and possibly beyond). It is initially characterized by steady, yet moderate, decreases in surface charge. This phenomenon is essentially a continuation of the secondary stage of the intermediate period in which hydroxyl groups continue to replace trivalent silicon centers, thus rendering the surfaces less and less positive. Towards the end of the third evolutionary period, the rate of change of surface charge with ambient air exposure time slows down. This indicates that a balance is beginning to be reached between the combined effects of Si-OH condensation and hydrolization of the Si-O-Si backbones by water vapor, and the reaction of neighboring Si-OH groups to form bridging Si-O-Si bonds (3,4).

In the initial and intermediate evolutionary periods, the surfaces treated with liquid-HF/H_2O exhibit a net lower charge. This phenomenon can be explained by considering the nature of the chemical impurities left on the freshly etched silicon surfaces. XPS analysis of several monitor wafers immediately following HF/H_2O treatments has shown the liquid-HF/H_2O treated samples to have approximately 2.2 times more oxygen on their surface compared to the vapor-HF/H_2O treated wafers. The oxygen, which is most probably bonded or chemically adsorbed to silicon, can be traced to the DI water rinsing step of the liquid-HF/H_2O process. In spite of the short duration of the rinse step, the high dissolved oxygen content of the DI water (possibly 1 ppm) can react with a small fraction of the Si-H groups to form highly negative Si-O centers, thus resulting in a less positive overall surface charge during the first 1000 minutes of exposure time to ambient air. The fact that no significant differences are observed between the two treatments in the final evolutionary period is most probably due to complete oxidation of the silicon surfaces.

Carbon analysis of all samples indicated significant amounts of physisorbed surface hydrocarbons. In the case of the liquid-HF/H_2O process, this may be attributed to organic leachate from the walls of the wet bench and the acid bottles, as well as ion exchange resins used

in DI water production (13,14). Organic residues following vapor-HF/H_2O treatment may have originated from the interaction of the azeotropic mixture with the walls of the canister or from reactor itself. The liquid-HF/H_2O treated wafers seemed to have roughly 1.5 times as much hydrocarbons compared to their vapor-HF/H_2O counterparts. While this was most probably due to the fact that vapor-HF/H_2O treatment did not include a rinse step (DI water, having a TOC of 25 ppb, will act as an additional source of organics), the effectiveness of the post oxide strip desorption interval of the vapor-HF/H_2O process could not be ruled out. The fluorine content of the liquid-HF/H_2O treated wafers were within the detection limit of the instrument, however surfaces treated with vapor-HF/H_2O contained measurable amounts of Si-F groups. Due to the hydrous nature of the vapor-HF/H_2O treatment of this study, we suspect an Si-F coverage of only a few hundredths of a monolayer. It should be noted that Morita and coworkers (9) who have studied the effect of anhydrous HF treatment, report the presence of a completely fluorine terminated silicon surface.

Before we could proceed with the planned contact angle versus ambient air exposure time experiments, the variation of the contact angle as a function of droplet age was studied. A strong dependence of contact angle was observed with droplet age, thus characterizing the air/water/solid system as dynamic, in which water continuously altered the solid surface through oxidation and roughening, thus rendering the surface more hydrophilic. The measurements indicated that, up to a droplet age of 6 minutes, the contact angle decreased by $3.7 \pm .2°$ per minute. Statistically, no slope differences were observed between liquid-HF/H_2O and vapor-HF/H_2O treated samples. For purposes of comparing our results to those obtained by Gould and Irene who adopted an inverted bubble technique for measuring the contact angle and did not observe such a phenomenon (13), a useful transformation of our data could be made. Since for each experiment, the equation of the straight line relating contact angle with droplet age was known, the extrapolated y-intercept was perceived as the initial contact angle had it been measured immediately following droplet introduction.

Alternatively, it was decided to fix the droplet age for each measurement at 3 minutes. This allowed sufficient time for focusing and angle measurement using the microscope/protractor assembly, without resulting in droplet breakdown due to evaporation. Figure 2 shows the variation of the contact angle with exposure time to ambient air

for both liquid-HF/H_2O and vapor-HF/H_2O treated surfaces. It is interesting to note that, over time, the contact angle was more sensitive to changes on the vapor-HF/H_2O treated surface. Furthermore, despite the contact angle differences between the two processes, both curves experienced three distinct periods of evolution which correlated well with previously observed trends in surface charge.

During the initial period, which again persisted for approximately 100 minutes, the liquid-HF/H_2O treated wafers showed greater hydrophilicity. This was consistent with XPS data taken immediately following HF treatments which showed oxide densities to be 2.2 times greater on the liquid-HF/H_2O treated wafers. In spite of the fact that these wafers had more organic residues, which in the absence of other effects should have rendered them more hydrophobic, the greater oxide coverage seemed to be the dominating factor in their relative hydrophilicity.

Figure 2 shows that after exposing the vapor-HF/H_2O treated samples to ambient air for 2 minutes, a contact angle of $62 \pm 2°$ was observed. This corresponded to a transformed, initial contact angle of $73 \pm 2°$ (i.e. at zero droplet age) which was close to Gould and Irene's (13), as well as Ohmi and Shibata's (19) reported values of $78 \pm 3°$ for unrinsed liquid-HF/H_2O treated substrates. The difference was most likely due to the fact that our vapor-HF/H_2O process was not exactly the same as their unrinsed liquid-HF/H_2O treatment.

During the intermediate period (again ranging from approximately 100 to 1000 minutes), rapid decreases in contact angle were observed thus indicating an increase in the surface polarity due to the emergence of charged trivalent silicon centers and their gradual reaction with hydroxyl groups. It is interesting to note that in the case of both liquid and vapor treated samples, the times corresponding to the sudden the decrease in contact angle (Figure 2) are well synchronized with the emergence of positively charged trivalent silicon centers (Figure 1).

In the third evolutionary period, the contact angles for both types of surfaces begin to approach their respective final values. This is due to the gradual replacement of trivalent silicon centers with Si-OH groups, and the emergence of the previously stated steady state condition. In the case of the vapor-HF/H_2O treated surface, the contact angle reached a final value of $35 \pm 2°$ which corresponded to

a transformed, initial contact angle of 41 ± 2°. This was in close agreement with Gould and Irene's (13) reported value of 39 ± 3° for thermally oxidized silicon. It is interesting to note that in the third evolutionary period, despite the presence of equivalent monolayers of oxide, the vapor-HF/H_2O treated surfaces show greater hydrophilicity. Under such conditions, the only discrepancy between the two surfaces must be the lower concentration of physisorbed organics present on the vapor-HF/H_2O treated surfaces, thus rendering them more hydrophilic.

For the sake of completeness, the apparent native oxide thicknesses as a function of exposure time to ambient air following liquid-HF/H_2O and vapor-HF/H_2O treatments was also studied. The results are shown in Figure 3. During these measurements, the refractive index was fixed at 1.460. The slight differences between the two curves may be due to actual refractive index differences caused by various amounts of surface organics. Since we did not perform time-dependent XPS analysis, in order to determine the actual native oxide thickness, our data was correlated to actual native oxide results available from the literature. Figure 3 shows our results to be in agreement with the ellipsometric findings of Raider and coworkers (7) who additionally, performed time-dependent XPS for native oxide thickness measurement (also shown in Figure 3). The fact that their XPS results agree semi-quantitatively with the recent results of Morita and coworkers (9), emphasizes the validity of their approach. Moreover, the fact that our ellipsometric results are in close agreement with those of Raider and coworkers, leads us to deduce that, in our investigation, both liquid-HF/H_2O and vapor-HF/H_2O treated surfaces undergo three distinct periods of evolution which correlate very well with previously stated surface charge and contact angle trends.

Phase-2; Characteristics of Thermal Oxides Grown After HF Treatments:

Table I summarizes the variations of total oxide charge and IQF as a function of exposure time to ambient air for both liquid-HF/H_2O and vapor-HF/H_2O treated surfaces. For reasons of brevity, two sets of data, corresponding to waiting periods of 25 and 125 minutes are reported (data corresponding to other waiting periods is also quite similar to the ones reported here). The standard deviation appears parenthetically alongside each total charge value. The results indicate that, for a given waiting period, no significant variations in total

oxide charge and IQF are observed over time. And, when all five waiting periods are taken into account, on the average, there seem to be no clear differences between the various waiting periods or the methods of surface treatment. These observations are not surprising given the fact that the interaction of thermally oxidized surfaces with ambient air are governed by the same reaction mechanisms described in the final evolutionary period of Figure 1. Upon thermal oxidation, the total charge attains an average value of $2.4E11/cm^2$ which, when compared to the final surface charge results of Figure 1, seems to be 2 to 3 times lower. This is to be expected since thermal oxidation essentially accelerates the charge compensation process described in the final evolutionary period of Figure 1.

Table II shows the variation of the contact angle with exposure time to ambient air for both thermally oxidized liquid-HF/H_2O and vapor-HF/H_2O treated surfaces following waiting periods of 25 and 125 minutes. A droplet age of 3 minutes was maintained throughout the measurements. Regardless of sample history, an average contact angle of $33 \pm 2°$ is obtained which seems to be invariant over time. This is consistent with the above mentioned total oxide charge and IQF results and indicates a high degree of inactivity for thermally oxidized silicon surfaces in ambient air. Even though direct comparison of contact angle (which only represents the top monolayers of a film and is not particularly sensitive to atomic defects) with total oxide charge (which represents a bulk property of the thermal oxide) may not be justified, one can combine these with the fact that the Si/SiO_2 IQF is invariant with time to show the high stability of the thermally oxidized films in the bulk as well as the two interfaces of the film.

Contact angle measurements as a function of droplet age of up to 6 minutes, indicated that regardless of the HF treatment, the contact angle of thermally oxidized wafers decreased at a slower rate compared to freshly etched surfaces ($2.6 \pm .2$ as opposed to $3.7 \pm .2°$ per minute). In the case of thermally oxidized wafers, surface oxidation due to the water droplet, should no longer play a role in decreasing the contact angle. Instead the contact angle decrease may be attributed to increased surface roughness upon exposure to water (9). At a droplet age of 3 minutes, the observed average contact angle of $33 \pm 2°$, corresponds to a transformed contact angle of $40 \pm 2°$ (i.e. at zero droplet age). This agrees well with Gould and Irene's reported value of $39 \pm 3°$ for thermally oxidized silicon wafers (13). It should be noted that the observed inactivity of thermal oxide in the presence of

ambient air is at odds with the findings of Ohmi and coworkers who report an 11° drop in contact angle upon exposing thermally oxidized and annealed wafers to ambient air for 100 minutes (19).

In comparing the results of Table II with those of Figure 2 (i.e. Phase-2 with Phase-1), it is noticed that thermal silicon oxidation does not significantly reduce the contact angle beyond that of what has been accomplished by several monolayers of a chemical oxide. This is to be expected since contact angle is a function of the top several monolayers of a material and gives no information about its bulk properties. Furthermore, as indicated earlier, the observed differences in hydrophobicity between vapor-HF/H_2O and liquid-HF/H_2O treated surfaces in the final evolutionary period of Figure 2 were attributed to the presence of organic residues. After thermal oxidation (which should volatilize all organics) the fact that no differences in hydrophobicity are observed, reinforces our claim.

Regardless of the HF treatment and the waiting period, even up to several days of post oxidation air exposure time, no variations in the thermal oxide thicknesses were observed. However, the thermal oxide thickness differences between the liquid-HF/H_2O treated wafers and the vapor-HF/H_2O treated wafers were statistically significant. The thickness of the thermal oxide layer on the liquid-HF/H_2O treated wafers ranged from 147 to 151 Angstroms, while that of the vapor-HF/H_2O treated wafers ranged from 150 to 156 Angstroms. This may be due to the presence of more organics on the liquid-HF/H_2O treated wafers. Given the fact that temperature ramp-up in the oxidation furnace was performed in a oxygen-diluted nitrogen environment, it is unlikely that the lower growth rate in the case of liquid-HF/H_2O treated samples is due to the formation of silicon carbide islands as reported by Meuris and coworkers (25). Instead, we believe the growth rate difference to be due to the fact that, for a fixed oxidation time, in the case of the liquid-HF/H_2O treated wafers, a larger fraction of the oxidation time is spent in volatilizing the surface organics. Given the relatively short oxidation times necessary to grow 150 Angstroms at 950° C, the so called "incubation time", which is longer for the liquid-HF/H_2O treated samples, can be rate retarding. Such organic residues have been known to hinder native oxide growth in ambient air (7,14), and it is believed that our observations are an extension of this phenomenon.

ACKNOWLEDGMENTS

The author wishes to thank, Edward Culley for assisting in the overall experimentation. Laurie LeTarte and Dr. Anne Testoni for performing and interpreting the XPS results. Drs. Emil Kamieniecki (from SemiTest Inc.) and Daniel Jackson for critically reviewing the manuscript. Jeannine Perchard and Dr. Leszek Reiss (both from SemiTest Inc.) for assisting in SCA data extraction. Drs. Gregory Botsaris and Nak-Ho Sung (both from Tufts University) for loaning the optical goniometer and assisting in the interpretation of contact angle data.

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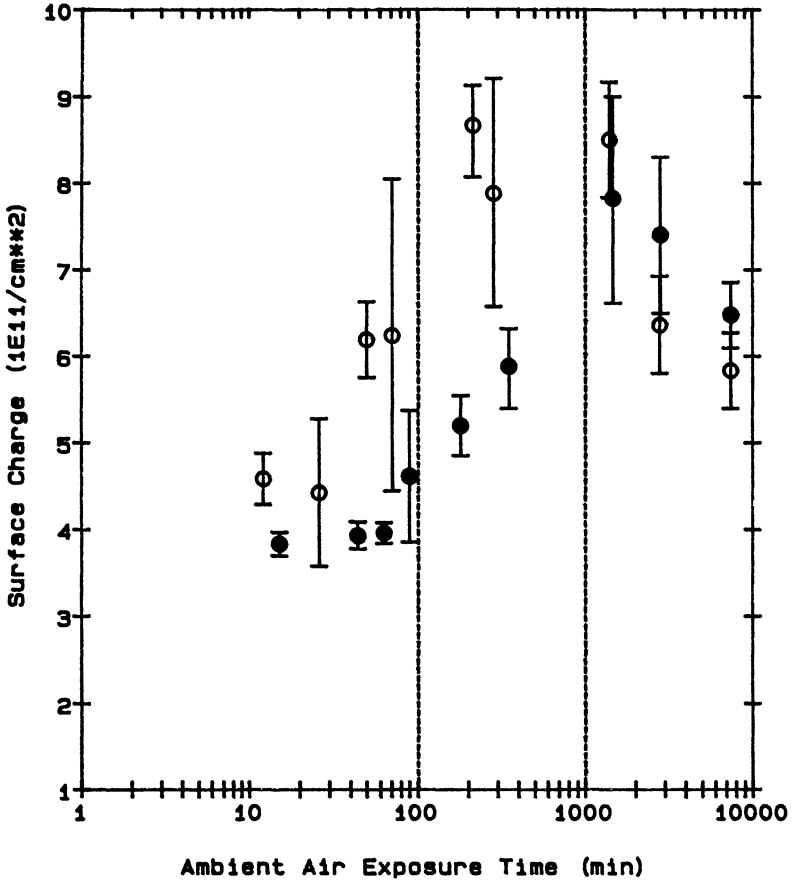

Figure 1: Surface charge versus ambient air exposure time for freshly etched surfaces. ○ vapor-HF/H_2O; ● liquid-HF/H_2O.

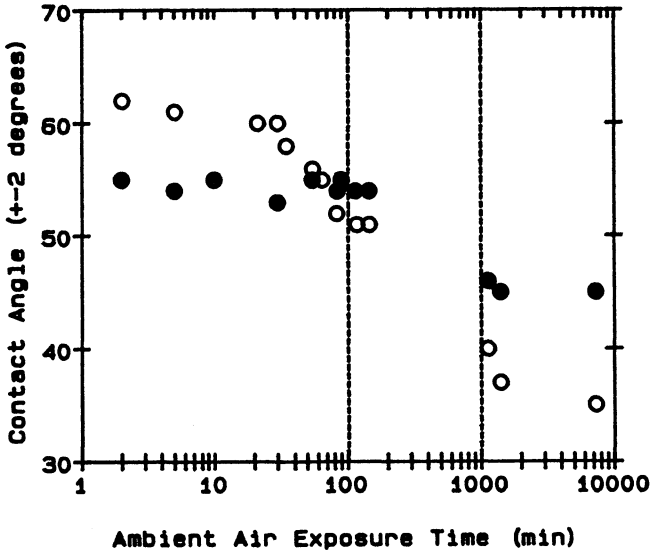

Figure 2: Contact Angle versus ambient air exposure time for freshly etched surfaces. ○ vapor-HF/H_2O; • liquid-HF/H_2O.

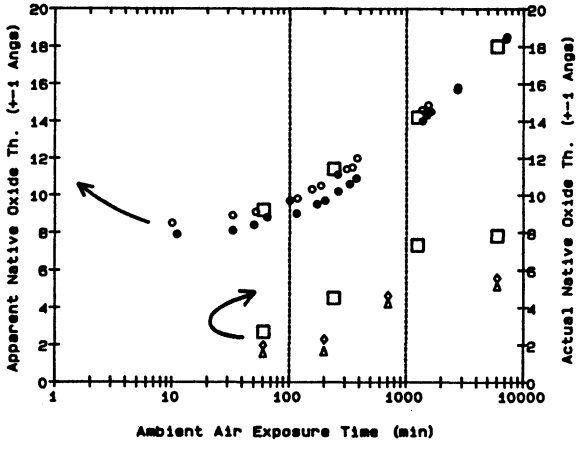

Figure 3: Apparent and actual native oxide thicknesses versus ambient air exposure time for freshly etched surfaces. ○ vapor-HF/H_2O, this study; • liquid-HF/H_2O, this study; □ liquid-HF/H_2O (7); ◇ liquid-HF/H_2O without DI rinse, (9); △ vapor-HF/H_2O, (9).

Table I:
Total oxide charge and IQF versus ambient air exposure time after thermal oxidation for waiting periods of (a) 25, and (b) 125 minutes.

A.A.E.T. (min)	Total Charge (1E11/sq.cm.)		Interface Quality Factor	
	liq-HF/H_2O	vap-HF/H_2O	liq-HF/H_2O	vap-HF/H_2O
12	3.06 (0.07)	2.57 (0.05)	1.66 (0.09)	1.53 (0.08)
32	3.31 (0.06)	2.82 (0.21)	1.58 (0.12)	1.48 (0.12)
92	2.44 (0.12)	1.89 (0.07)	1.26 (0.08)	1.30 (0.19)
149	3.38 (0.16)	3.02 (0.05)	1.62 (0.24)	1.57 (0.10)
1003	2.75 (0.13)	2.26 (0.07)	1.29 (0.10)	1.23 (0.05)
5660	3.14 (0.12)	2.39 (0.08)	1.63 (0.18)	1.47 (0.15)

(a)

A.A.E.T. (min)	Total Charge (1E11/sq.cm.)		Interface Quality Factor	
	liq-HF/H_2O	vap-HF/H_2O	liq-HF/H_2O	vap-HF/H_2O
23	2.43 (0.07)	2.81 (0.07)	1.27 (0.07)	1.46 (0.04)
69	2.57 (0.14)	2.79 (0.18)	1.55 (0.09)	1.39 (0.11)
127	1.58 (0.19)	2.08 (0.09)	1.29 (0.04)	1.20 (0.11)
181	2.82 (0.18)	3.02 (0.22)	1.48 (0.11)	1.53 (0.08)
1041	2.07 (0.20)	2.46 (0.11)	1.35 (0.14)	1.23 (0.18)
5695	1.84 (0.06)	2.89 (0.21)	1.61 (0.13)	1.22 (0.17)

(b)

Table II:
Contact angle versus ambient air exposure time after thermal oxidation for waiting periods of (a) 25, and (b) 125 minutes.

A.A.E.T. (min)	Contact Angle (degrees)	
	liq-HF/H_2O	vap-HF/H_2O
15	30	33
40	32	31
60	31	33
105	31	34
140	33	34
1200	34	34
7000	33	34

(a)

A.A.E.T. (min)	Contact Angle (degrees)	
	liq-HF/H_2O	vap-HF/H_2O
20	30	33
50	31	32
90	32	32
120	31	32
200	33	34
1000	33	34
6000	35	33

(b)

VAPOR-PHASE pre-CLEANS for FURNACE-GROWN and RAPID-THERMAL THIN OXIDES

D. B. Kao, B. R. Cairns, and B. E. Deal

ADVANTAGE Production Technology, Inc.
310 De Guigne Drive, Sunnyvale, CA 94086

ABSTRACT

The impact of vapor-phase cleaning is demonstrated by the electrical properties of polysilicon-gate capacitors with thin gate/tunnel oxides produced by both conventional batch-mode furnace oxidation and single-wafer rapid thermal oxidation. Substantial increases in the time-to-breakdown and charge-to-breakdown have been measured which demonstrate the advantages of reduced-pressure vapor-phase wafer cleaning processes. The benefits of vapor-phase precleans and rapid thermal processing can be combined in a cluster-tool system to further reduce handling and exposure of the wafers.

INTRODUCTION

As integrated circuits become more complex with ever shrinking geometries and higher device packing density, VLSI processing is demanding more stringent control of defects and contamination. Therefore, wafer cleaning procedures are receiving increasing attention. It is well known that aqueous cleaning procedures tend to add contaminants and leave uncontrolled localized native oxide patches, leading to yield losses through defects in gate oxides, poor adhesion of silicides, or variations in contact integrity. In addition, future advanced processing technology requires the chemicals to penetrate submicron steep features on the wafer surface. The limitations of present aqueous cleaning processes are becoming more unacceptable. Much research work has been devoted to finding alternative dry cleaning technologies (1, 2). While these dry processes avoid liquids by using gas phase chemistry, they typically require excitation energy to activate the chemical reactions needed for wafer cleaning at low temperatures. This added energy may be plasma, particle beam, or short wavelength radiation. Because all of them involve radiation of some sort, concerns arise regarding the possible effects of dry cleaning damages on the electrical properties of devices (3).

These drawbacks are alleviated by a recently developed reduced-pressure vapor-phase cleaning technology and system. As described in (4), compared to conventional wet processes, this type of process provides effective wafer cleaning and substantially reduces

chemical consumption and disposal. The implementation of vapor clean in a vacuum system results in process uniformity and controllability. In addition to oxide etches using the HF/H_2O vapors, the combination of HF/H_2O and HCl/H_2O vapors and other chemistries allows metallic impurity removal and etch rate adjustment.

Whereas pre-cleans are important in many processing steps, nowhere are they more critical than for thin gate or tunnel oxides. The effects of aqueous and vapor precleans on the electrical properties of furnace-grown thin oxides have also been reported (5, 6). Although the mainstay of thin oxide technology is still based on the traditional diffusion furnace batch processing, single-wafer rapid thermal oxidation is receiving increasing attention because of its unique capability of precise thermal budget control at high temperatures (e.g. 1150°C) and its compatibility with cluster-tool systems. In this paper, the impact of vapor-phase cleaning is demonstrated by the electrical properties of thin gate/tunnel oxides produced by both conventional batch-mode furnace oxidation and single-wafer rapid thermal oxidation.

VAPOR-PHASE CLEANING SYSTEMS

As previously described in (7), the vapor-phase wafer cleaning system EDGE 2000 etches native or thermal oxides using HF/H_2O vapor, and cleans the wafer using vapors of other chemicals such as HCl/H_2O. The process takes place at reduced pressures, and terminates by vacuum desorption. In the more advanced EDGE 2002 system, additional cleaning capability is provided with ozone and an infra-red heat source, and system performance is enhanced by extensive chamber and wafer temperature control, and consistent vapor delivery system.

As shown in Fig. 1, the major components of the EDGE 2002 are the process chamber, the delivery system of chemical vapors or gases, and the wafer temperature control system. The chamber is constructed of a specially formulated silicon carbide material [5] which provides mechanical strength and chemical resistance. It can also sustain wide ranges of processing pressures and temperatures. The pressure in the process chamber is usually maintained in the 100 to 350 Torr range. On one side of the chamber is a proprietary window which is chemical resistant and allows exposure of the wafer to external infra-red or ultraviolet light in an ozone rich environment. Wafer temperatures of greater than 200°C can be readily obtained. The vaporizers shown in Fig. 1 contain solutions of HF/H_2O, H_2O, or HCl/H_2O which are heated for the desired vapor supply. The vaporizer temperatures are controlled by process recipes and can be varied to provide process flexibility.

The optional O_3/IR process can be used as an in-situ cleaning step for organics removal prior to the oxide etching process, conditioning the wafer surface to assure etch uniformity and repeatability. Furthermore, as a post-treatment, a thin layer of oxide regrown in ozone is available for wafer surface protection. In the O_3/IR process, the ozone is fed into the process chamber while the wafer is being heated up by the infra-red lamp to a specified temperature, after which the ozone is turned off and the wafer is cooled down by a low-temperature inert gas.

Wafer Cleanliness

Particles. As reported in (7), the distribution of particle adders measured with a Tencor Model 5500 indicates that the vapor etching system normally does not add particles and that, in some cases, particles are removed - probably due to the final desorb cycle. A long-term particle monitoring log obtained on an Advantage Edge 2000 was recently published by Wong et. al. of Texas Instruments (8). Reproduced in Fig. 2, their data demonstrated that vapor-phase processing is substantially cleaner than wet chemical cleaning, as measured by particle counts.

Organic Impurities. Ozone and ultraviolet light have been used to remove organics in various cleaning applications (9), including wafer processing (5). We have found, by Static SIMS analysis, that the combination of ozone with infra-red heating is effective in reducing the concentration of carbon on wafers deliberately contaminated by an organic coating (10). Particle counts following an aqueous H_2SO_4+H_2O_2 strip of photoresist were also lowered substantially. The benefits of ozone/IR pretreatment before the vapor-phase oxide etch has also been characterized (10).

Metallic Impurities. It is not generally believed that HF solutions are effective in removing heavy metals from silicon surfaces. Nevertheless, experiments have shown (7) that after HF/H_2O vapor phase etching, metals are not added, and concentrations of many metallic contaminants are reduced. The analysis was accomplished with a total reflection x-ray fluorescence method (TXRF) (11). As with particles, the removal of metals by the HF process was likely due to the final, reduced pressure, desorb cycle. Wong et. al. (12), however, has shown that the HF/HCl vapor combination on an Advantage EDGE 2000 was effective in cleaning the residues of ashed photoresist which is known to be a source of metallic contamination. Investigations are currently underway to utilize alternative gas phase chemistries for removing metallic and other types of contamination.

Oxide Etching

One example of vapor-phase oxide etching is shown in Fig. 3, where a wide range of etch rates, from 2 to 33 Å/sec, have been obtained for various etch conditions. An azeotropic mixture of HF/H_2O (38.4 wt percent of HF) was maintained at temperatures ranging from 30 to 60°C in one vaporizer while DI water at 30 to 60°C was contained in the second vaporizer. The carrier flow rate through each vaporizer varied, but the total flow rate was maintained at 15 slpm. It can also be seen that a delay or offset time occurs before oxide etching takes place. This is because in vapor phase processing, the actual etching follows the formation of a thin layer of aqueous film which condenses on the oxide surface (13). This aqueous film is continuously replenished with reactants such as HF/H_2O. Concurrently, reaction products are permitted to evaporate. During the post-etch desorb cycle, this thin layer including reactants and by-products is physically removed and transported to the exhaust line.

The incubation or delay time discussed above can vary from nearly zero to tens of seconds. It is both process dependent and film type dependent, but is reproducible for a given film and process. The wafer surface condition, however, can be changed by the organics adsorbed through exposure to clean room air or contact with plastic wafer containers, which has been found to degrade vapor-phase oxide etching uniformity. The enhanced O_3/IR capability in the EDGE 2002 has been demonstrated to remove organic contamination and improve etching uniformity (10).

ELECTRICAL EVALUATION of VAPOR-PHASE Pre-CLEANS

The impact of vapor-phase cleaning has been demonstrated in eliminating tungsten silicide delamination and lowering sheet resistance in titanium silicide. In addition, better oxide breakdown characteristics and reliability have been shown for various test structures and oxide thicknesses. In this work, the effect of vapor precleans for both furnace-grown and rapid thermal oxides were investigated. Polysilicon-gate capacitors of different sizes were fabricated in field oxide openings on silicon wafers cleaned by both vapor-phase cleans and the conventional RCA-type aqueous procedures. These wafers were oxidized in the same oxidation processes in both the conventional batch-mode oxidation furnace and the rapid thermal processing system. The electrical properties of these oxides were then tested by high-frequency and quasi-static CV measurements to evaluate oxide charges and interface states. Breakdown current-voltage characteristics and stress endurance were also measured. In addition, charge trapping was monitored by flat-band voltage shifts following various durations of electrical stressing.

Furnace-Grown Thin Oxides

Typical breakdown histograms of furnace-grown thin oxides, as shown in Fig. 4, indicate an improved destructive breakdown field for the HF/HCl vapor-cleaned wafers (12.7 MV/cm) over the aqueous RCA cleaned wafers (11.9 MV/cm). The benefit of the vapor clean is more clearly demonstrated in the oxide endurance or reliability data as measured by TDDB and shown in Fig. 5. Similar results of improved breakdown characteristics have also been duplicated at different laboratories using different oxide thicknesses and isolation structures. For example, the recent publication by Texas Instruments (8) showed that substantial improvement of thin oxide reliability was obtained using vapor-phase pre-oxidation clean carried out on an Advantage EDGE 2000. Their results are reproduced in Fig. 6. While the C-V characterization of the oxides in (8) demonstrated certain dependencies on the pre-oxide cleans, the C-V data obtained in this work showed nearly identical oxide thickness, flat-band voltage, fixed charges, and interface state density. It is likely that these parameters were dominated by processing steps following the pre-clean and gate oxidation, such as poly deposition and doping, backside aluminum, and annealing.

It has been widely believed that the mechanism of oxide breakdown is intimately related to its charge trapping properties (5). In this work, charge trapping during Fowler-Nordheim tunneling stress was monitored by the shift in the flat band voltage. The density of positive oxide fixed charges derived from the flat band voltage shift is plotted in Fig. 7 for both the vapor-cleaned and wet-cleaned samples at stress electric fields of 9, 10, and 11 MV/cm. At a given electric field, the positive charges are seen to increase with the tunneling charges and then begin to level off. Both the initial rate of positive charge build up and the final saturated value are higher at higher electric field. As far as the vapor and wet precleans are concerned, it can be seen that no obvious differences exist in the charge trapping behavior studied here, in contrast to the different breakdown behaviors. One possible explanation is that the shift in flat-band voltage is an averaged measure of the entire capacitor, while breakdown test is a differentiating process which highlights the weakest spot of the device. Whereas less trapping in the ONO dielectric was linked to its high endurance (9), the effectiveness of cleaning seems to lie in its ability to remove localized contamination which would lead to a weakening of the dielectric.

Vapor-Clean and Rapid Thermal Oxidation

Single-wafer rapid-thermal oxidation is receiving increasing attention for thin gate and tunnel oxide applications. Besides allowing thermal budget control in optimizing impurity diffusion and thermal oxidation, improved oxide qualities of rapid thermal oxides have also been reported (14, 15). The advantages include reduced N_F and D_{it}, higher breakdown voltages, diminished charge trapping and, therefore, better endurance and reliability. The low thermal mass and small process chamber of the single-wafer system enable rapid switching of both temperature and process gases. This flexibility has also led to new composite thin dielectrics such as reoxidized nitrided oxide (ONO) (16).

The rapid thermal processing system used in this study is a Heatpulse 610 from A. G. Associates, in which the wafer is held by small quartz pins in a quartz tube and heated by arrays of tungsten-halogen lamps. The temperature is sensed by an optical pyrometer. The wafers were ramped up to 1150°C and oxidized in dry O_2 and then annealed in N_2 at 1050°C. A slip-free ring was used to improve temperature uniformity at the wafer edges to prevent the formation of slip defects in the silicon substrate. The rapid thermal oxidation kinetics of vapor-cleaned wafers is shown in Fig. 8 for 950°, 1050°, and 1150°C. The electrical characterization of rapid thermal oxides following vapor and aqueous cleans will be discussed in a later publication.

CLUSTER-TOOL FOR INTEGRATED PROCESSING

It is widely known that exposure to cleanroom air leads to deteriorated device properties, and stringent control is exercised in critical processing steps such as gate oxidation, poly-gate deposition, poly-emitter formation, and contact hole processing. It is also now a common practice to use an inert encapsulation for loading the wafers into an oxidation furnace. This trend invariably leads to the concept of integrated processing.

The Advantage EDGE 3000 incorporates vapor-phase wafer cleaning into integrated processing. As shown in Fig. 9, it is based on a load-lock cluster platform designed to provide multi-chamber sequential cleaning and processing capabilities. This flexible system can accept three MESC compatible modules. Wafer cleaning and oxide etching processes are carried out in SiC chambers with HF resistant and IR/UV transmitting windows. The process takes place at pressures between 20 and 400 Torr with wafer temperatures up to 300°C. In a typical two module configuration, an IR/O_3 cleaning module is used for organics removal, and a second module with azeotropic HF and HCl chemistries is used for uniform etching and stripping of oxides. An alternative configuration would include a cleaning module which removes metals and organics with UV-activated processes. Following the in-situ cleaning, the wafers would be transported in an inert or vacuum ambient to an adjoining reaction chamber for subsequent oxidation, CVD, or sputtering processes.

SUMMARY

It has been demonstrated that the reduced-pressure vapor-phase wafer cleaning processes remove unwanted native or chemical oxides and leads to improved oxide breakdown characteristics. This preliminary investigation also demonstrates the potentially beneficial combination of in-situ vapor-phase preclean and rapid thermal processing in a cluster tool arrangement.

ACKNOWLEDGEMENT

The authors wish to thank A.G. Associates for providing the rapid thermal system and process support. They also thank Dr. J. McVittie and the technical group at the Stanford IC Lab for assistance in device fabrication.

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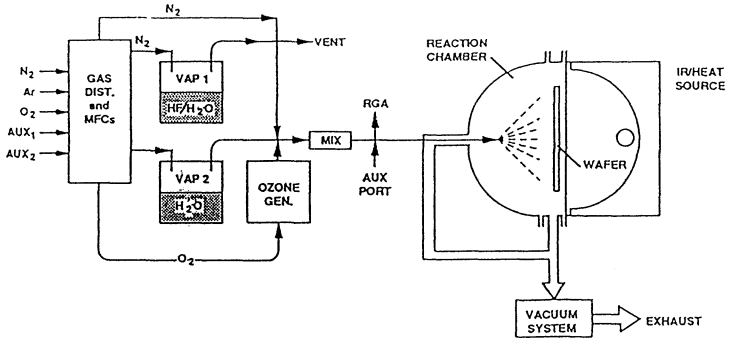

Fig. 1 Advanced vapor-phase cleaning system EDGE 2002.

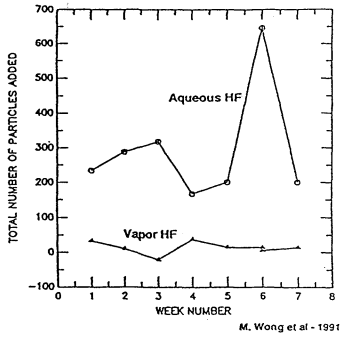

Fig. 2 Particle trend for aqueous and vapor HF native oxide deglaze.

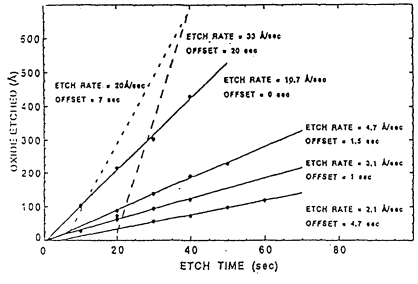

Fig. 3 Vapor etching of thermal oxides in HF/H_2O mixtures

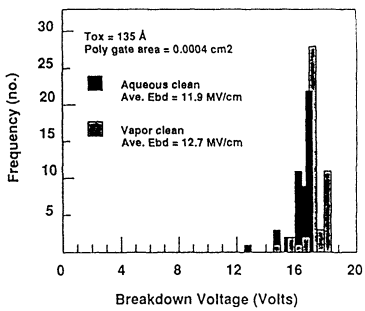

Fig. 4 Oxide breakdown histograms for vapor and aqueous pre-cleans.

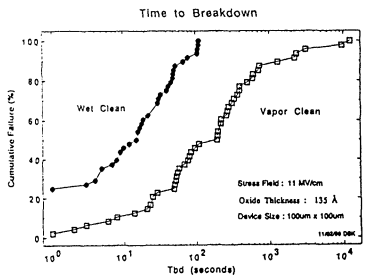

Fig. 5. Improved time-to-breakdown under constant voltage stress was obtained for vapor etch as compared with wet HF etch.

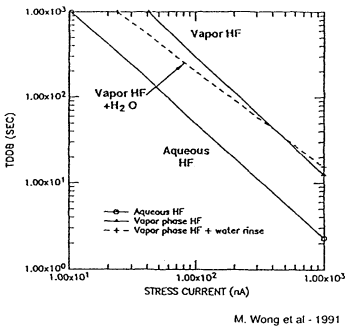

Fig. 6. Improved time-to-breakdown under constant current stress was obtained for vapor etch as compared with aqueous HF etch.

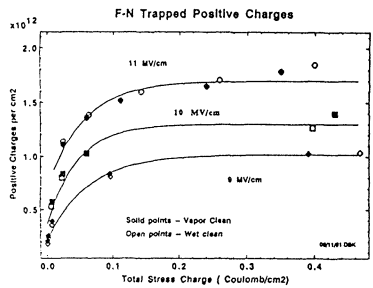

Fig. 7 Density of trapped positive charges as a function of total Fowler-Nordheim tunneling charges for different stress electric fields

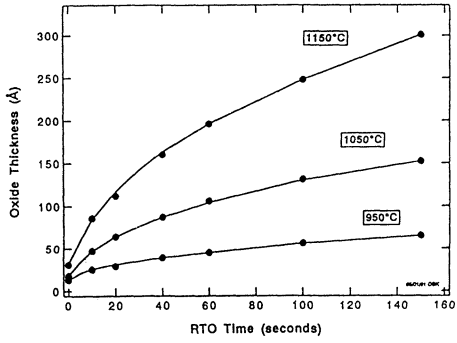

Fig. 8 Rapid thermal oxide growth as a functio of RTO time.

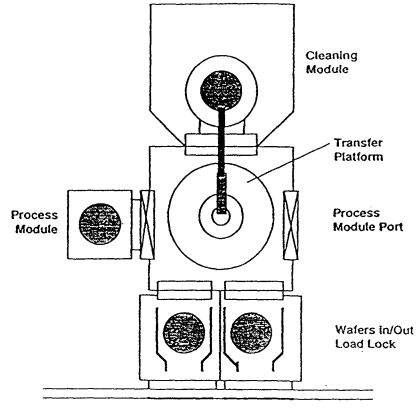

Fig. 9 EDGE 3000 Cluster tool configuration.

A NEW CLEANING METHOD BY USING ANHYDROUS HF/CH_3OH VAPOR SYSTEM

A.Izumi, T.Matsuka, T.Takeuchi and A.Yamano

DAINIPPON SCREEN MFG. CO.LTD Development Department 2. 322, Furukawa-cho, Hazukashi Fushimi-ku, Kyoto 612

For wafer surface cleaning technology, a new etching process of SiO_2 film by anhydrous HF/CH_3OH vapor system was investigated intensively. Especially CH_3OH was used as a solvent for HF instead of conventional H_2O. Silicon oxide film is etched by HF_2^- species as the case of HF/H_2O system. Improvements of the selectivity ratio of oxide etching (native oxide/BPSG), and suppression of the native oxide growth and particle generation after etching were attained. This HF/CH_3OH vapor etching system is hopeful as a pre-cleaning method of gate oxidation, CVD and epitaxial growth.

1.INTRODUCTION

Vapor phase etching system was developed by many researchers for wafer surface cleaning.[1] This vapor phase system is suitable for fine trench and contact holes with high aspect ratio. In order to have effective cleaning of the wafer surface, it is necessary to etch oxide film selectively and to suppress the native oxide growth and particle generation. However, this goal cannot be achieved using the conventional HF/H_2O vapor etching method. On the other hand, P.J.Grunthaner, R.P.Vasquez, and F.J.Grunthaner also investigated technology to etch GaAs oxide film by using a liquid mixture of anhydrous HF and alcohol (C_2H_5OH). From the point of their methodology and etching reaction mechanism, however, no detectable differences could be found in comparison with the etching method using HF aqueous solution.[2]

In this work we investigated a new etching process for oxide film using the anhydrous HF/CH_3OH vapor system. Primarily, CH_3OH in vapor phase was used as a solvent for HF, replacing conventional H_2O. We intended to improve the selectivity ratio of oxide etching, and suppress native oxide regrowth and particle generation after etching.

2.EXPERIMENT

The single wafer vapor etching chamber for HF/CH_3OH vapor system is equipped a the supply of N_2 gas as the carri-

er, a mixture of HF and CH_3OH vapor as etching species, and CH_3OH vapor for controlling the concentration of vapor mixture as shown in Fig.1. This system which consists of pipes, chemical tanks, etching chamber contains fluororesin. The source liquids are a mixture of HF and CH_3OH, and CH_3OH, respectively. Each source liquid is bubbled with N_2 gas and it's vapor is introduced into the etching chamber. The mixture of HF and CH_3OH used in this experiment is an azeotropic state in which the concentration ratio of vapor phase is equal to that of the liquid phase, and the concentration of HF and CH_3OH is 38.5 wt% and 61.5wt%, respectively. By using the mixture of HF and CH_3OH in an azeotropic state, we could control the steady supply of vapor.

The sample wafers used were 10-15 ohm-cm n-type (100) oriented single crystal silicon, 5 inches in diameter. Oxide film about 140 and 2000 Å in thickness was formed on the silicon wafers by the ordinary dry O_2 and steam oxidation at 950°C. BPSG film was deposited on wafers using ordinary low pressure CVD, about 2000 Å in thickness. In order to remove organic contamination and H_2O adsorbed on wafer surface, all sample wafers were irradiated with UV-ray in mid-air for 3 minutes prior to etching reaction using a low pressure mercury-lamp. Native oxide was produced on the bare wafer surface to about 10 Å thickness. Next, N_2 purge, vapor etching and N_2 purge were carried out in the etching chamber. In order to make a comparison with HF/CH_3OH, HF/H_2O vapor etching was also examined. The etching condition was set at 22°C and under the atmospheric pressure. The etching rate of native SiO_2 film and BPSG film was evaluated by changing the HF and CH_3OH concentration measured by ellipsometry. When thermal SiO_2 film was etched, the number of particles was counted by using the laser wafer surface inspection system, HLD-300B. An ESCA 5500MT analyzer was used to obtain photoelectron spectra.

3.EXPERIMENT RESULTS

Oxide etching rate and selectivity

The etching rates of native oxide and BPSG film were examined using the $HF\text{-}CH_3OH$ vapor system. Total N_2 carrier gas flow rate was 10L/min., which is the amount of (a) and (b) L/min. The symbol (a) represents the N_2 gas flow rate through the upper route in Fig.1, and (b) represents the N_2 gas flow rate through HF and CH_3OH mixture. The results, shown in Figs. 2 and 3, show a marked increase in the etching rate as the N_2 gas flow rate through HF and CH_3OH mixture, in other words, the concentration of HF increased. The etching rate was controlled by the CH_3OH concentration. In the case of high CH_3OH concentration, in which N_2 carrier gas was enriched with CH_3OH by bubbling, the etching rate of

BPSG film decreased to under 200 Å/min., and the etching rate of native oxide increased to over 10 Å/min. The etching rate of native oxide increased and the etching rate of BPSG film decreased by addition of CH_3OH vapor. In order to etch off the native oxide in contact hole, it is necessary to increase the etching rate of native oxide, and to decrease the etching rate of BPSG film. Etching loss of BPSG film results in a change in the contact hole size. The etching selectivity ratio (native oxide/BPSG) was over 1/20 in the process of HF/CH_3OH vapor system. This selectivity ratio was better than that of HF/H_2O vapor 1/100. The HF/CH_3OH vapor system seems promising for contact hole cleaning.

Surface condition

Native oxide growth after the etching process was suppressed effectively using the HF/CH_3OH vapor etching method. From ESCA measurement, peak around 104 eV of Si_{2p} spectra coresponding with native oxide disappeared after HF/CH_3OH vapor cleaning. Fig.4 shows this result in comparison to the case of wet etching by HF aqueous solution. In order to enhance the sensitivity of surface silicon, the take-off angle of the photoelectron was 20°. After rinsing the wafer with deionized water following etching, Si_{2p} peak about 104 eV appeared. This can be attributed to the regrowth of native oxide film on silicon wafer owing to H_2O.

Carbon contamination after HF/CH_3OH vapor cleaning was not more than that of wet etching using HF aqueous solution from measurement of ESCA C_{1s} spectra.

Particle counts after etching

Fig.5 shows particle counts of over 0.28μm size produced after etching of thermal oxide film (140Å) by changing N_2 gas flow rate (a) through the upper route in Fig.1 at 22 °C. N_2 gas through (HF/CH_3OH) mixture or (HF/H_2O) mixture is 1 L/min. Total N_2 gas flow is (1+a) L/min. The number of particle generation in the case of HF/CH_3OH vapor system decreased remarkably compared with that of the HF/H_2O vapor system. Particle counts decreased in correlation with the increasing of the N_2 gas flow rate for dilution of HF containing vapor. When N_2 gas flow rate for dilution increases, formation of the condensed layer of etching chemicals on the wafer surface can be easily avoided. Such condensed layers absorb H_2O produced by the etching reaction.

4.DISCUSSION

Etching species of HF/CH_3OH vapor system should be

produced as follows.[3)]

$$2HF + CH_3OH \longrightarrow HF_2^- + (CH_3OH)H^+ \quad (1)$$

This dissociation reaction is analogous to HF/H_2O system.

$$2HF + n(H_2O) \longrightarrow (H_2O)_nH^+ + HF_2^- \quad (2)$$

Silicon oxide film is etched by HF_2^- species as in the case of HF/H_2O system.[4)] In the case of high CH_3OH concentration, the etching rate of BPSG film decreased and the etching rate of native oxide increased compared with that of low CH_3OH concentration. This etching characteristic may be dependent on the use of CH_3OH vapor. In the case of high CH_3OH concentration, ionization of HF will be promoted and the concentration of HF_2^- species will be large,[3)] and the etching rate of native oxide increased. On the other hand BPSG film is liable to absorb H_2O. H_2O produced by the etching reaction is exhausted accompanying the CH_3OH vapor which has affinity for H_2O. So the etching rate of BPSG film decreased in the case of high CH_3OH concentration. These etching results appeared due to H_2O in the etching process being reduced.

H_2O and O_2 in the etching reaction cause the growth of native oxide on the wafer surface.[5)] H_2O promotes the oxidation of the silicon surface. Since the concentration of H_2O and O_2 during etching reaction is reduced in the HF/CH_3OH system, the re-oxidation of bare silicon surface after HF/CH_3OH vapor etching is suppressed.

Fig.6 shows a scheme for etching reaction in the SiO_2-HF-H_2O system. SiF_4, which is the product of the SiO_2 etching reaction, react with H_2O and change into SiO_2 and H_2SiO_3.[6)] This product is considered the cause of particles. By reducing H_2O in the reaction system using CH_3OH vapor, generation of these non-volatile products can be suppressed.

In the silicon oxide etching process, it should be noted as follows:

* H_2O content in the reactive agent vapor is reduced by using CH_3OH instead of H_2O.
* H_2O produced by the etching reaction is exhausted accompanying the CH_3OH vapor which has affinity for H_2O. It is necessary to avoid formation of the condensed layer of etching chemicals on the wafer surface which absorb H_2O produced by the etching reaction.

By removing the influence of H_2O as mentioned above, effective results consisting of good selectivity etching ratio and suppression of particle is obtained in the HF/CH_3OH vapor system. This HF/CH_3OH vapor etching system is promising as a pre-treatment of gate oxidation, CVD and epitaxial growth.

4.CONCLUSION

Improvements in the selectivity ratio of oxide etching (native oxide/BPSG), and suppression of the native oxide growth and particle generation produced after etching were attained using HF/CH_3OH vapor system. By removing the influence of H_2O, these effective results were obtained.

ACKNOWLEDGEMENT

The authors are grateful to MORITA CHEMICAL INDUSTRIES CO.,LTD for their contribution of chemicals.

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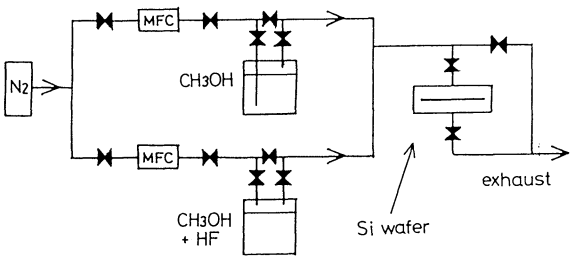

Fig.1 Schematic diagram of HF-CH_3OH vapor cleaning apparatus

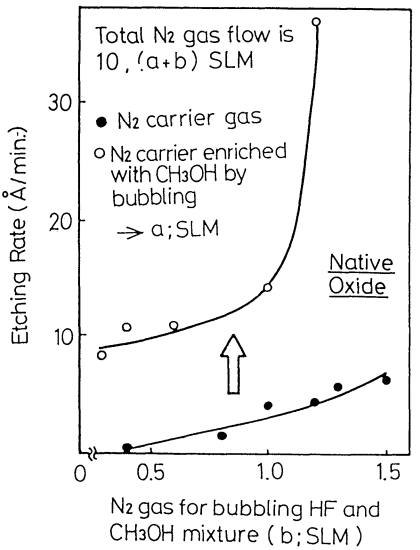

Fig.2 Native SiO_2 etching rate by HF and CH_3OH vapor

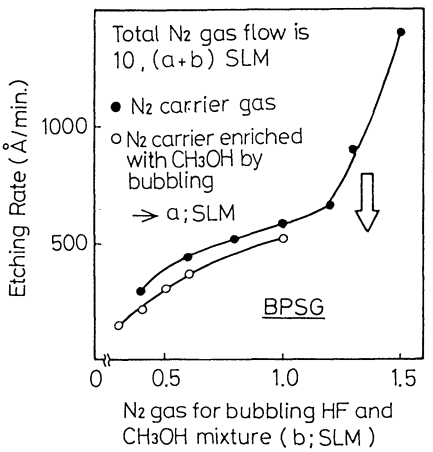

Fig.3 BPSG film etching rate by HF and CH_3OH vapor

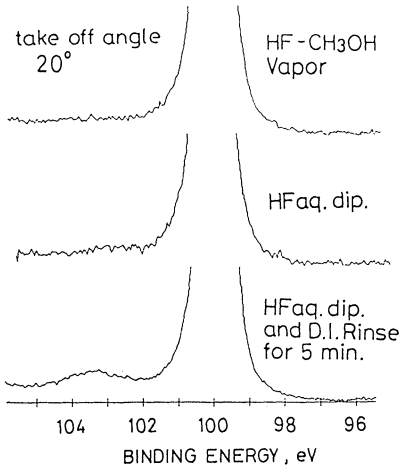

Fig.4 Si_{2p} ESCA spectra after etching native oxide.

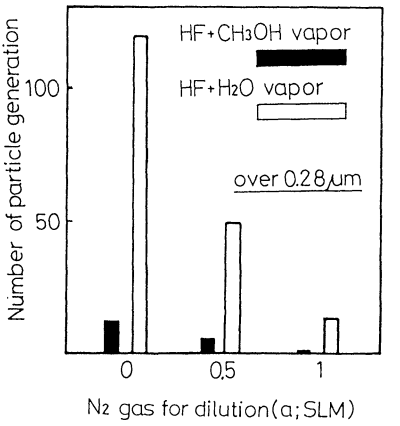

Fig.5 Particle counts after etching thermal oxide film (140Å) by changing N_2 gas flow at 22°C. N_2 gas for bubbling (HF/CH_3OH) or (HF/H_2O) is 1 SLM. Total N_2 gas flow is (1+a) SLM.

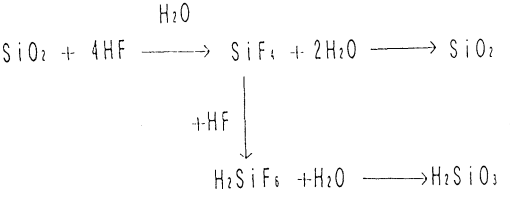

Fig.6 Scheme of etching reaction in SiO_2-HF-H_2O system.

MECHANISMS OF THE HF/H_2O VAPOR PHASE ETCHING OF SiO_2

C. R. Helms
Electrical Engineering Department
Stanford University, Stanford, CA 94305
B. E. Deal
Advantage Production Technology, Inc.
310 DeGuigne Drive, Sunnyvale, CA 94086

In this paper we report on studies of the mechanisms responsible for HF/H_2O etching and cleaning of Si surfaces. From these studies we have clearly established that the role of water is to provide a condensed solvent medium for the HF on the surface. Our results, as well as those in the literature, show that if the partial pressures of HF and H_2O are too low (or sample temperature too high) condensation does not occur and little or no etching is observed. Based on these ideas and vapor pressure data from the literature, we have developed a detailed model that provides for the calculation of the onset of condensation as a function of wafer temperature and reactant partial pressures. In addition, the model allows determination of the HF concentration in the condensed H_2O film, and thus the etch rate.

INTRODUCTION

Silicon dioxide etching based on the simultaneous exposure of the surface to HF and H_2O vapor has been the subject of numerous recent publications. The first report of vapor phase HF/H_2O etching of SiO_2 was by Holmes & Snell in 1966 (1). They observed that "the rate of attack of the oxide by the vapor close above the etching bath was comparable with that in the bath." They suggested the importance of surface condensation which, as we will see below, is a a key factor necessary for etching. Subsequent to the work of Holmes & Snell, Beyer & Kastl (2) also investigated a process based

on vapor phase HF/H_2O mixtures for etching of SiO_2 as did Blackwood, Biggerstaff, Clements and Cleavelin.(3) These investigators also found SiO_2 etch rates of similar magnitude to what can be obtained in HF/H_2O liquid phase etching. In all of the above-mentioned studies both HF and H_2O were required to achieve substantial etch rates even though H_2O is a reaction product for either

$$SiO_2 + 4HF \rightarrow SiF_4 + 2H_2O \quad [1]$$

or

$$SiO_2 + 6HF \rightarrow 6H_2SiF_6 + 2H_2O \quad [2]$$

which are thought to occur. In addition, for a given set of HF and H_2O partial pressures there is a maximum temperature above which little etching occurs. As we will see, consistent with the original suggestions of Holmes & Snell, these effects are consequences of the need to have a condensed layer or film on the SiO_2 surface to allow etching to take place. More recently the Hashimoto Chemical Industries/Tohoku University groups (4,5) have also investigated related processes concentrating on the etching of native oxide with very dry anhydrous HF. In their work a vapor phase HF critical concentration was found below which no etching was observed. This critical concentration depended on residual H_2O present, temperature, and flow rate as well as the nature of the SiO_2 being etched. They suggested that indeed water was necessary for etching to proceed. Once the reaction is initiated at sufficiently high HF pressures enough water will be produced to allow the reaction to continue. The Advantage Production Technology group has concentrated on developing a process where both the HF and H2O partial pressures are carefully controlled providing good etch rate control over a wide range(6,7). This approach has also been adopted by other groups as well.

In the present work we have taken the lead from the Holmes & Snell work in light of subsequent data to develop a quantitative model of HF/H_2O etching of SiO_2. The basis of the model is the assumption that etching will only proceed if a condensed HF containing liquid layer is present on the surface. A major part of the model is therefore determining those conditions of temperature, HF,

and H_2O partial pressures for condensation to occur. Proceeding on the assumption that etching then proceeds in the same way as for liquid solutions, we construct a steady state model that allows the calculation of HF concentration in the condensed liquid film.

A schematic of how this process works is shown in Fig. 1. Initially an SiO_2 surface is exposed to a vapor phase mixture of H_2O and HF(1a). If the partial pressures are sufficient then a condensed film of HF and H_2O will form and continue to grow on the SiO_2 surface (1b). Etching proceeds with the formation of H_2SiF_6 and additional water (1c). Although the partial pressure of SiF_4 over dilute H_2SiF_6:HF:H_2O solutions is relatively low some SiF_4 will evolve during the etching process. When the etching is complete and the HF and H_2O reactants are switched off the liquid H_2SiF_6/HF/H_2O film can be evaporated or rinsed off.

MECHANISMS

The chemistry of the actual SiO_2 etching process by HF/H_2O is beyond the scope of this paper and has been discussed by Judge(8) and more recently by the Hashimoto/Tohoku University groups(9) It is clear that in the liquid state an overall reaction of the form

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \qquad [3]$$

is responsible for the etching observed. In addition, for vapor phase etching the decomposition of H_2SiF_6 via

$$H_2SiF_6 \rightarrow 2HF + SiF_4 \qquad [4]$$

with the desorption of SiF_4 is a necessary step, unless a subsequent water rinse is employed.

For the present purposes we are interested in the comparison between measured liquid phase etch rates at a given HF concentration and the "vapor" phase etch rate at an identical calculated value of HF concentration in the condensed phase. Etch rates from liquid phase etching at 25°C., are availab;e. These data

with correspond to the Etch Rate = $900[HF]^2 + 30[HF]$. For lower concentrations of HF, especially for buffered HF such a dependence would not be expected; however, at these high concentrations the mechanisms are not well understood and a more accurate mathamatical fit is desired.

The processes occuring during etching are strongly effected by condensation and evaporation and much can be learned from the equilibrium vapor pressures of the various constituents involved. The most complete reference on HF/H_2O vapor/liquid equilibria appears to be that of Munter, Aepli and Kossatz (12). These data are shown in Fig. 2 where the equilibrium vapor pressures are plotted versus liquid composition for a series of temperatures. Without further analysis we can make a few obvious statements from these curves. First, in the low HF concentration limit the vapor pressure of HF is quite small so that the HF fraction in the liquid phase will be much larger than in the vapor phase. The converse is true for the high HF concentration limit. This in part explains the "anhydrous" etching results since any water present or created by the reaction will be retained in the liquid due to the very low H_2O vapor pressure for high HF concentrations. That point where the vapor phase and liquid phase concentrations are equal will typically be near the azeotroph which occurs at approximately 39 wt.%HF. (13)

In order to assist in predicting etching behavior the data of Fig. 2 have been modeled using a near regular solution approach (18), the results of which are also shown in the figure as the solid lines, and include the high HF concentration range beyond that investigated experimentally. At a given temperature a condensed phase will form only if the combination of vapor phase partial pressures is high enough so that the flux of molecules impinging on the surface is greater than that leaving by evaporation. This is shown in Fig. 3 for 20°C where condensation will occur on the high pressure side of the line (upper right) and no condensation is expected on the low pressure side of the line (lower left).

Having now established the conditions that lead to condensation and therefore etching, we will turn our attention to determining the concentration of HF expected in the condensed layer. This will be affected by the adsorption/desorption process as well as

the consumption of HF during etching and presence of reaction products. For the moment we will ignore these last factors so that we will consider the situation of condensation on an inert surface. In addition, we will assume the fluxes are linearly proportional to partial pressure. For these conditions the net steady state flux into the condensed layer will be

$$\Phi_{H_2O} = P_{H_2O} - P_o^{H_2O}(T,[HF])$$

$$\Phi_{HF} = P_{HF} - P_o^{HF}(T,[HF]) \qquad [5]$$

where the Φ's are the fluxes, P is pressure, T surface temperature and [HF] is the HF concentration in the condensed layer. P_{H_2O} and P_{HF} are the vapor phase partial pressures right above the surface and $P_o^{H_2O}$ and P_o^{HF} are the equilibrium vapor pressures at the sample temperature T and condensed layer composition [HF]. The HF concentration in steady state is then determined by the ratio so that

$$[HF] = \frac{P_{HF} - P_o^{HF}(T,[HF])}{P_{HF} - P_o^{HF}(T,[HF]) + P_{H_2O} - P_o^{H_2O}(T,[HF])} \qquad [6]$$

This is solved using the data of Fig. 2 and is shown in Fig. 4 at 25°C for various H_2O partial pressures. Note again the upper left region of this figure corresponds to conditions leading to no condensation. Note this also assumes a negligible pressure drop across any boundary layer or pressure gradient due to vapor phase diffusion limitations.

The vapor phase etch rates to be discussed here will be those from references (7,8) since accurate estimates of the partial pressures are available. Figure 5 shows the experimental vapor phase etch rates as a function of calculated HF concentration in the condensed film. For comparison the data of Fig. 2 for the liquid case are also shown as the solid line. The agreement is reasonably good but shows higher vapor phase etch rates at low concentration and lower vapor phase etch rates at higher concentration. The latter effect may be due to the comparison to liquid rates for stirred

conditions as well as the buildup of reaction products. The deviation at low concentration is likely due to the inaccuracy of the vapor pressure model for low HF concentrations where no data was actually available.

The above discussion would correspond reasonably well to the situation early in the etching process where the concentration of reaction products is low. However, as etching proceeds, the reaction products may tend to build up in the condensed layer. If we consider equation 2, we see 6 molecules of HF are consumed to form one molecule of H_2SiF_6 plus 2 molecules of H_2O. Therefore the case of "anhydrous" etching would also correspond to a case with a high concentration of reaction products. We have to date not attempted a detailed model for this part of the process. However, some qualitative comments are possible. First, regarding etching itself, Thomsen (14) has shown that H_2SiF_6 is capable of etching SiO_2 via

$$5H_2SiF_6 + SiO_2 \rightarrow 3H_2(SiF_6SiF_4) + 2H_2O \qquad [7]$$

In addition, the presence of high concentrations (<10 mole%) of H_2SiF_6 in HF/H_2O solutions significantly reduces the vapor pressures of both HF and H_2O above such solutions. This is an additional mechanism which will stabilize a condensed liquid phase in the high HF concentration "anhydrous" situations.

DISCUSSION

From the above discussion it is clear that the etching of SiO_2 from vapor phase HF/H_2O mixtures occurs after an initiation step by condensation of the HF and H_2O with identical mechanisms compared to what would be obtained from liquid phase etching. The major differences between liquid and vapor phase etching are the initiation step, the possible presence of high concentrations of reaction products in the condensed phase, and the need to desorb or rinse off the reaction products after the etch.

Initially it might seem that the "anhydrous" etching results are counter to this model. However, small amounts of water present in

the ambient, on the surface, or produced as a consequence of an initial surface reaction, especially in the high HF partial pressure limit are sufficient to produce a condensed phase. In addition, the even further reduced H_2O vapor pressure in the presence of high H_2SiF_6 concentrations will lead to a condensed phase for "anhydrous" conditions.

The model for the low HF concentration limit explains the observed thresholds for etching since at too high a temperature or too low an HF and/or H_2O pressure, a condensed phase will not be supported and therefore no etching will occur. Given this mechanism and assuming steady state etching we have developed a mathematical model which predicts the HF concentration in the condensed phase. In comparison with liquid etching data as a function of HF concentration the calculated vapor phase etch rates agree well with experiment. Further work needs to be done to account for high H_2SiF_6 concentrations and produce a time dependent kinetic model.

ACKNOWLEDGEMENTS

The work performed at Stanford was supported by Advantage Production Technology, Inc. and SEMATECH through Advantage.

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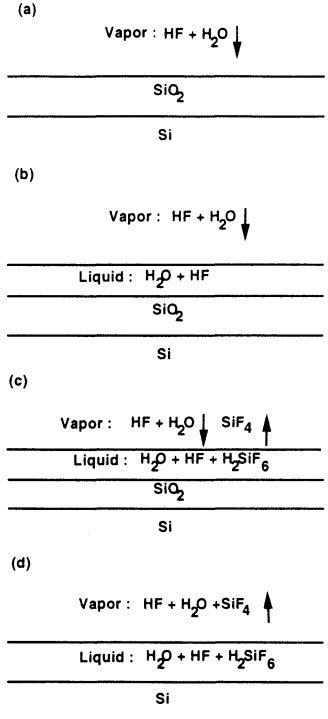

Fig. 1. Schemtic diagram of the various steps occurring during the HF/H_2O etching

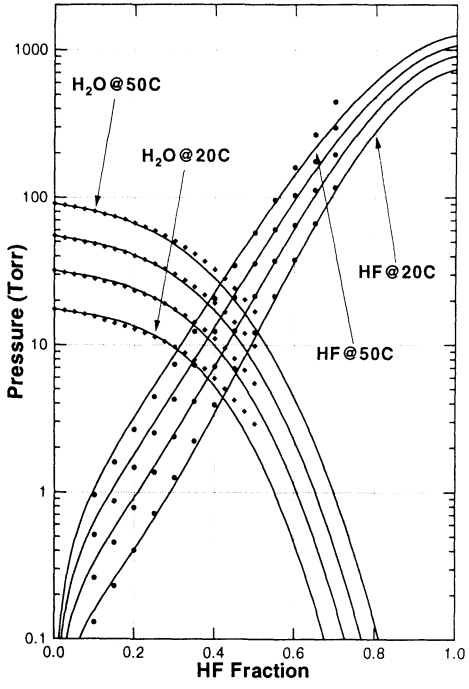

Fig. 2. Reconstructed data from Munter, et al (12), showing vapor pressures verses HF weight farction for 20, 30, 40, and 50 C along with model fit.

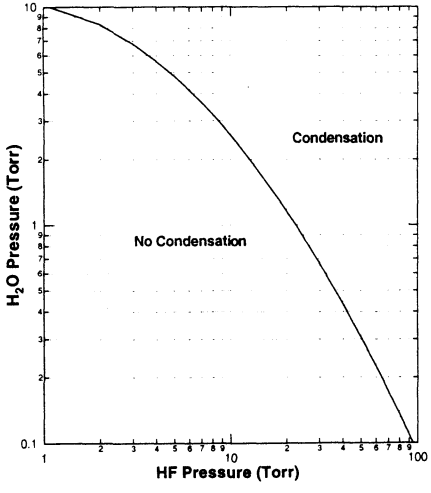

Fig. 3. Partial pressure diagram indicating what ranges correspond to a stable condensed phase.

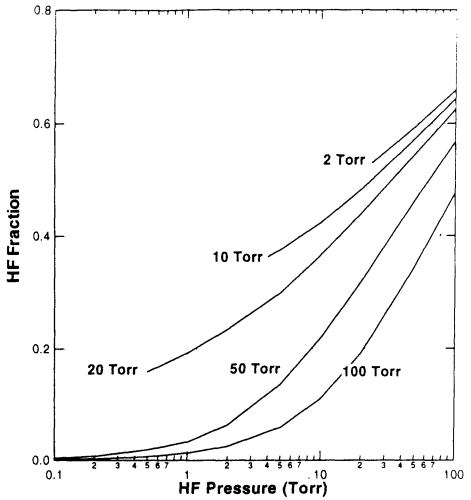

Fig. 4. Calculated HF fraction in the condensed phase verses HF partial pressure for HF/H_2O vapor phase mixtures at the H_2O pressures indicated. The curves for 20, 10, and 2 Torr terminate due to the requirement for condensation.

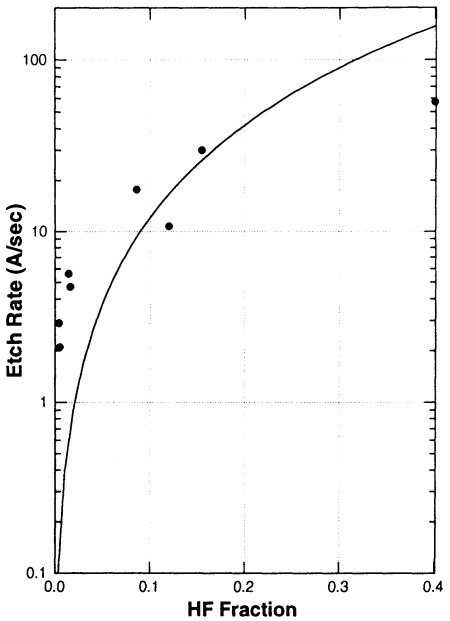

Fig. 5. Vapor phase etch rates from reference (7) verses calculated HF farction are shown as the points. The expected etch rate for a stirred liquid is shown as the solid line.

HF VAPOR ETCHING APPLIED TO POLYSILICON EMITTER TRANSISTORS

W.B. de Boer and R.H.J. v.d. Linden
Philips Res. Lab.
P.O.B. 80000-5600 JA Eindhoven
The Netherlands

Current gain and emitter resistance of polysilicon emitter transistors greatly depend on the thickness of the oxide layer at the polysilicon-silicon interface. In this investigation an HF dip and an HF vapor etch, both intended to remove native oxide prior to the growth of a polysilicon layer, are compared to one another. It is shown that the combination of HF vapor etching and processing in a controlled environment has a beneficial effect on poly-emitter transistor parameters, provided epitaxial, rather than polysilicon growth can be avoided.

INTRODUCTION

The interface between a deposited polysilicon layer and monosilicon substrate has influence on the characteristics of polysilicon emitter transistors. The effect of the interface on electron-hole recombination in the emitter is well known (1,2). An increasing amount of interfacial oxide gives rise to an increase in current gain (H_{FE}), as many researchers have shown. Unfortunately, the emitter series resistance (R_e) increases as well. In modern transistor design, focussed on smaller dimensions and higher switching speeds, it is mandatory to get the emitter resistance down (3).

Usually a thin interfacial oxide layer is obtained by growing polysilicon immediately after an HF dip, as opposed to a pre-poly treatment where deliberately a chemical oxide is applied by e.g. an RCA clean. In a common LPCVD reactor the wafers are loaded into the reactor while the reaction chamber is open to atmosphere at temperatures around 620°C. This causes the wafers to reach temperatures close to 600°C at ambient oxygen and moisture levels, which is sufficient to regrow some oxide before the poly

deposition starts.

A relatively new cleaning method is HF vapor etching. Rather than removing siliconoxide by dipping the wafer into a solution of HF in water, the wafer is etched by a mixture of HF gas and water vapor. Sometimes an inert carrier gas is mixed by. Experimental work suggest that an HF vapor etch leaves less oxide on a silicon surface than an HF dip (4). The purpose of this investigation is to compare both cleaning methods in terms of thickness of the interfacial oxide in relation to relevant transistor parameters.

EXPERIMENTAL

Fig.1 shows the lay-out of a prototype clustertool batch reactor, used for the majority of the experiments described here. After a nitrogen purge in the load-lock, the wafers are transferred to the HF vapor etch chamber, where native oxide is removed by a mixture of HF gas and water vapor at a total pressure of several Torr at room temperature. This gaseous etch is compatible with (LP)CVD processing, in contrast to an HF dip. Without breaking the vacuum the wafers are transferred to the deposition chamber, a vertical LPCVD reactor, to be deposited with polysilicon. Load-lock and transfer chamber were kept at a pressure of 1 Torr under a low flow of nitrogen. During loading the temperature of the LPCVD reactor is maintained at the deposition temperature of 620°C. The combination of an HF vapor etch and controlled ambient ensures that contamination of the wafer surface, occurring during transfer and heat-up, is minimized.

A cross section of the poly emitter transistor used in this experiment is drawn in fig.2. Table 1 shows a condensed version of the flow chart. The critical steps, determining the amount of interfacial oxide, are the poly preclean and the polysilicon deposition.

A 25 wafer batch was split in several groups, receiving different pre-poly treatments. After poly deposition, if feasible even before, all splits were put back together in one batch for the remaining steps of the flow chart: emitter drive/anneal and metallization. An RTA step, sometimes used to break up the interfacial oxide, was removed from the flow chart. The main goal of these experiments was not to break up the oxide, but to compare different cleaning methods to one another. The bad reproducibility of RTA in general was a secondary reason not to use it and to rely on furnace treatments instead.

A reference group of 5 wafers of each 25 wafer batch always followed the 'standard' process: HF dip and D.I. water rinse as pre-poly cleaning step and polysilicon deposition in a conventional horizontal LPCVD system with open tube wafer loading.

The availability of a cluster tool with load lock offers the possibility not only to check the influence of an integrated HF vapor etch, also the combination of HF dip and loading in a controlled environment can be investigated. During the short time the HF dipped and rinsed wafers are exposed to atmosphere before entering the load lock, only an insignificant amount of native oxide will grow (4).

A fourth variation was obtained by shortly exposing the HF vapor etched surfaces to oxygen at a pressure of 0.5 Torr, just prior to the start of the polysilicon deposition at a wafer temperature of 620°C. This makes sure the silicon surface will be covered with a thin oxide layer the moment polysilicon deposition starts. The reason for doing so will be explained below. Summarizing, there are four experimental groups (A-D), subjected to the following treatments:

A: clustertool HF vapor etch and polysilicon deposition.
B: clustertool HF vapor etch, oxide regrowth and poly deposition.
C: HF dip/D.I.water rinse, transfer into clustertool and poly deposition.
D: HF dip/D.I.water rinse, poly deposition in a conventional LPCVD reactor.

Groups A and C allow a comparison of HF vapor etch and HF dip with the influence of loading under ambient conditions excluded as far as possible. Groups C and D probe the influence of loading in a controlled ambient versus open tube loading.

Current gain and emitter series resistance measurements were performed on some 20 transistors per wafer to get statistically reliable values. Virgin wafers, subjected to the cleaning steps and poly deposition only, were used in SIMS and HRTEM analysis to get information about the amount of interfacial oxide.

RESULTS AND DISCUSSION

Before starting to run batches of wafers on the cluster tool reactor, some introductory experiments were done on a single

wafer laboratory set up, which performed the same function: HF vapor etch, transfer under controlled low pressure conditions into the deposition chamber and polysilicon deposition. The main difference with the cluster tool was the heat up time. In the single wafer reactor typically 3-5 minutes were needed to heat a wafer from room temperature to 620°C, while it took 45 minutes in the cluster tool to heat a batch of wafers.

Plotted in figs. 3 and 4 are Gummel emitter and base numbers (G_e and G_b) and there quotient, the current amplification factor H_{FE} (= G_e/G_b). The values on the vertical axis are plotted as an average of twenty measurements per wafer. To get an impression of the variations per wafer in relation to the variations between the experimental groups, the wafer number, indicating the sequence in the batch, is plotted on the horizontal axis. Wafers in one group are connected by lines. Fig.3 shows the results of three wafers processed in the single wafer reactor (equivalent to clustertool group A), compared to four wafers which received the standard treatment (group D). The wafers treated in the single wafer reactor can clearly be distinguished. The G_e number drops, consistent with a thinner interfacial oxide which is a less effective barrier for the hole current. The increase in G_b is more difficult to explain. One would expect a slightly deeper emitter and, consequently, a thinner base and lower G_b if the interface constitutes a diffusion barrier. The opposite happens, indicating a wider base. As a result H_{FE} drops by almost a factor of five (fig.3).

A HRTEM lattice image explains the nature of this contradiction. As can be seen in photo 1, the silicon layer deposited after the HF vapor etch is not a polysilcon layer but grows epitaxially. There are a lot of defects, nevertheless, discontinuities in the interfacial oxide layer cause the top silicon layer to line up epitaxially with the interface. As diffusion along grain boundaries, as happens in a polysilicon layer, is orders of magnitude faster than bulk diffusion, the epi layer strongly retards the diffusion into the substrate of arsenic, implanted in the poly (epi) layer. To avoid this unwanted effect, an oxidation step was introduced prior to polysilicon deposition (experimental group B).

Four groups of wafers (A-D) were processed in the cluster tool along the lines described above. SIMS results on non-device (virgin) wafers are summarized in table 2. SIMS indicates about equally

low oxygen contents for groups A and C and higher oxygen contents for B and D. The SIMS resolution may not be sufficient to reveal small differences in the amount of remaining oxygen. Also does SIMS not give information about the uniformity of the oxide layer. HRTEM pictures of the interface after poly deposition (photo 2) give more information. Although determination of the varying thickness of the amorphous layer at the interface is rather subjective, it seems clear that group A wafers (HF vapor etched) contain the smallest amount of oxygen. Contrary to what happened in the single wafer reactor, epitaxial growth does not occur in the batch reactor. The increased heat up time in the batch reactor may play a role here.

Thin interfacial oxide layers break up during the subsequent anneal step, causing polysilicon to recrystallize epitaxially. The degree of epitaxial recrystallization also is an indication for the thickness and continuity of the original interfacial layer. Photos 3 and 4 show the interface of group A and group D wafers after an anneal of 30 minutes at 900°C. Photo 3 shows extensive recrystallization after anneal on group A wafers, whereas group D wafers only show a rough interface (photo 4). This confirms the impression one gets from photo 2 and is in line with the differences in the transistor parameters: The emitter efficiency varies with the cleaning and loading treatment. In fact, G_e looks a sensitive measure for the amount of interfacial oxide. G_b is constant over the different experimental groups, except for some scatter in the data points (fig.4). There are no signs of a difference in As diffusion depth, caused by different interfacial oxide thicknesses. Recrystallization during the anneal treatment does not seem to have influence on the diffusion profiles. This is in contrast to the results in fig.3, where epitaxial rather than polycrystalline growth had a detrimental effect on the transistor characteristics.

In the case where G_b is constant, the H_{FE}'s (fig.4) reflect the variations in G_e and can be compared. The reduction in H_{FE} is caused by the reduction in emitter efficiency, which depends on the thickness of the interfacial oxide. The HF vapor etch combined with processing in the cluster tool is the most effective treatment from the methods tried here, to remove the native oxide and to keep it from regrowing. The HF dip/clustertool combination (group C) seems inferior to HF vapor etch/clustertool treatment, in spite of the SIMS results but confirming the impression one gets from the

micrographs (photo 2).

The emitter resistances are in agreement with the above results. Fig.5 shows the resistance of emitters of approximately 3.5 μm^2. Although the wafer averages show quite some scatter, group A wafers have the lowest emitter resistance and group D wafers the highest. On this particular structure a 30% reduction in emitter resistance between groups A and D was routinely obtained. Equally important is the improved process stability after an HF vapor etch. The standard deviation of the emitter resistance over a wafer is reduced to up to a factor of two when comparing the HF vapor etched wafers of group A to the control group D.

The oxide regrowth procedure (group B) allows the application of oxide thicknesses thinner than the minimum obtainable in conventional processing (group D) and thicker than the minimum resulting from an HF vapor etch (group A). Oxide regrowth will keep the deposited silicon layer from growing epitaxially. The increased fluorine amounts on the interface of the HF vapor etched wafers (table 1) do not seem to cause any harm.

CONCLUSIONS

The poly emitter process benefits from the combined action of an HF vapor etch and processing in a controlled environment. Compared to conventional processing, the emitter resistance and current gain are reduced, due to less interfacial oxide. Clustertool processing allows better interface control and improves process stability. In some cases an oxide regrowth step, preceding polysilicon deposition, may be necessary to avoid epitaxial growth.

ACKNOWLEDGEMENTS

The authors like to thank P. Zalm, R. Vriezema, A. de Veirman and C. Bulle-Lieuwma for characterization work and ASM AMTC for use of the prototype Advance 600 cluster tool.

This work was supported by the EEC under Esprit project 2016.

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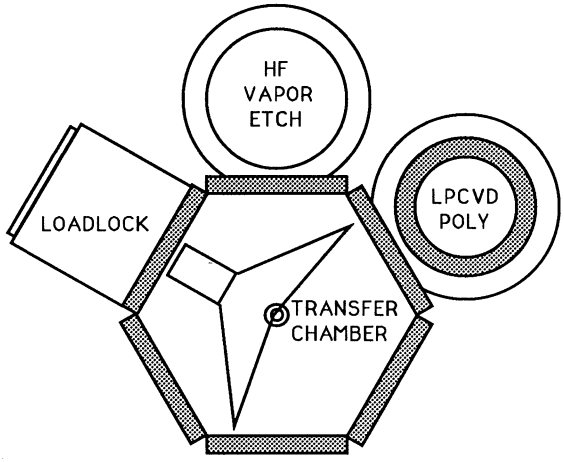


FIG. 1 - CROSS SECTIONAL SCHEMATICAL VIEW OF A CLUSTERTOOL WITH TWO WAFER PROCESSING MODULES, A LOADLOCK AND THREE EMPTY POSITIONS.

PROCESS FLOW
n-type material
backside getter diff.
oxidation +nitride dep.
litho definition
LOCOS isolation
litho definition
extrinsic base implant
preanneal
emitter window etch
base implant
anneal
poly preclean
poly deposition
emitter implant
poly patterning
anneal+emitter drive
metallization
AlSi patterning
alloy

TABLE 1 - OVERVIEW OF THE CONDENSED FLOW CHART. THE CRITICAL STEPS FOR THE INTERFACIAL OXIDE THICKNESS ARE IN BOLD FACE

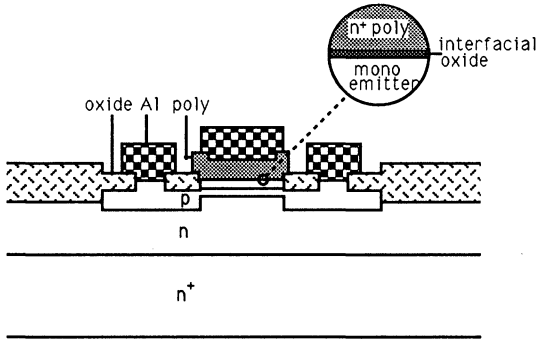


FIG.2 - CROSS SECTION OF A POLYSILICON EMITTER TRANSISTOR WITH ENLARGED EMITTER REGION.

group	SIMS dose (at/cm^2)	
	O	F
A	1.4E15	6.2E14
B	2.2E15	4.6E14
C	1.5E15	8.5E13
D	2.2E15	6.7E13

TABLE 2- OXYGEN AND FLUOR AT THE INTERFACE AS DETERMINED BY SIMS.

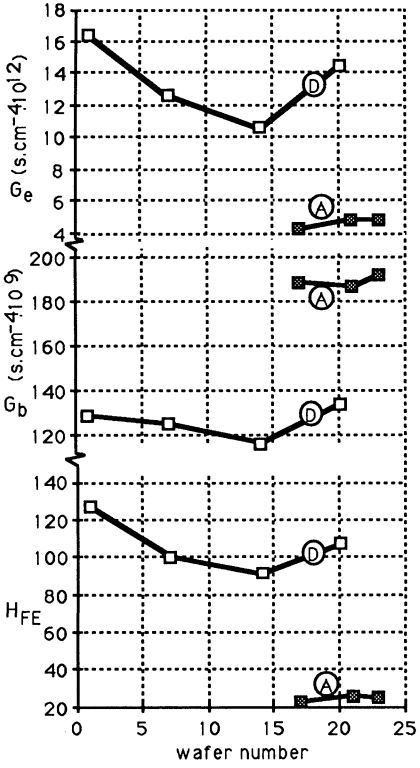


FIG.3- TRANSISTOR CHARACTERISTICS OBTAINED IN A SINGLE WAFER REACTOR.

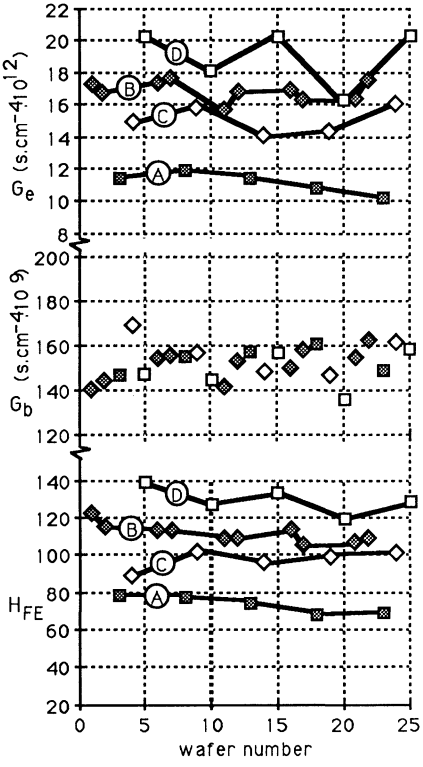


FIG.4- TRANSISTOR CHARACTERISTICS OBTAINED IN A CLUSTER TOOL REACTOR

LEGEND

- group A wafers: HF vapor etch/cluster tool processing
- group B wafers: HF vapor etch/cluster tool processing +reoxidation
- group C wafers: HF dip/cluster tool processing
- group D wafers: HF dip/conventional processing

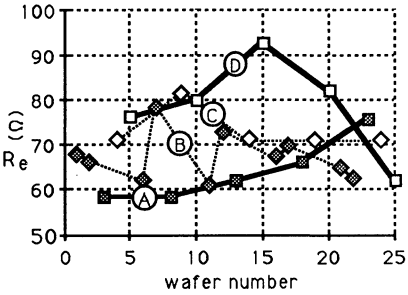
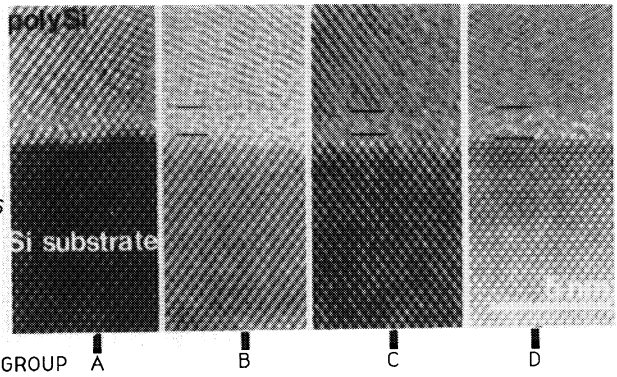


FIG.5- SAME WAFERS AS IN FIG.4: EMITTER RESISTANCE

PHOTO 1- AFTER AN HF-VAPOR CLEAN SOMETIMES THE SILICON LAYER GROWS EPITAXIALLY AS THIS HRTEM SHOWS. THE INTERFACIAL OXIDE LAYER IS NOT CONTINUOUS.

PHOTO 2- HRTEM MICROGRAPHS OF THE INTERFACE REGION AFTER POLY DEPOSITION SHOW DIFFERENT OXIDE LAYER THICKNESSES FOR DIFFERENT CLEANING STEPS.



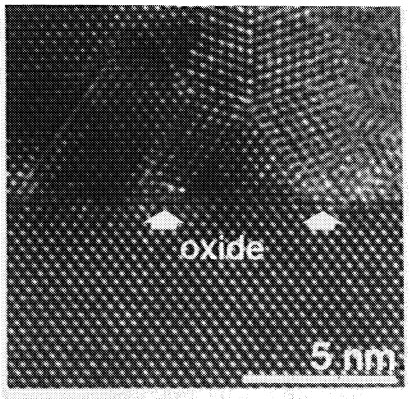


PHOTO 3- INTERFACE REGION OF GROUP A WAFER AFTER ANNEAL.

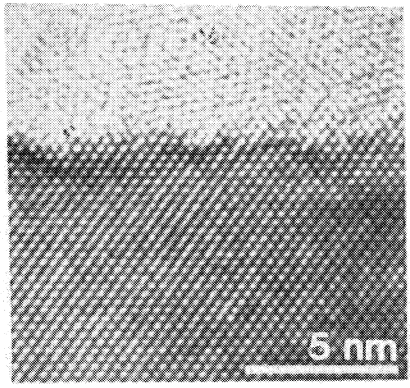


PHOTO 4- INTERFACE REGION OF GROUP D WAFER AFTER ANNEAL.

HF LAST PERFORMANCE IN CENTRIFUGAL SPRAY PROCESSORS

Kurt Christenson
FSI International
Chaska, Minnesota 55318

The HF Last cleaning process (H_2SO_4:H_2O_2 followed by HF) is of interest because it yields an oxide free, largely hydrogen terminated silicon surface with low levels of metallic contamination. However, the particle performance of HF Last cleans has often been erratic. Identified particle deposition mechanisms include the attraction of negative zeta potential particles by the positively charged silicon surface and deposition at the Si-liquid-gas interface. This paper will discuss a third mechanism associated with the presence of tiny water droplets on the wafer surface during the dry. The nature of these "particles" and the particle and metal process results in a centrifugal spray processor in which the number of surface droplets has been reduced will be discussed.

INTRODUCTION

A production worthy, aqueous based HF Last (HFL) process which leaves an oxide free silicon surface has long been sought by the semiconductor industry. Such a process is necessary for low temperature epitaxy[1], precise control of gate oxide thickness and is helpful in producing low resistance contacts[2]. HFL processes can also produce surfaces with very low metal levels[3,4] without the concern of surface roughening or pitting by RCA-1 chemistries. Further, HFL cleans reduce the process time, the number of chemicals and the quantity of chemicals required for a clean.

But, HFL processes have a long history of erratic particle performance rendering them unusable for many applications. Reported here are the results of HF Last processing in an FSI Mercury MP centrifugal spray processor. The rinse system of the Mercury was modified to eliminate any tiny droplets of water that dry in place on the wafers. The resulting particle and metal performances are presented.

EXPERIMENT

The mechanical arrangement of components in the FSI Mercury MP centrifugal spray processor is shown in figure 1. Cassettes of wafers are loaded into a turntable that rotates clockwise when viewed from above. There is a stationary spray post in the center with sources for chemicals, rinse water and nitrogen for solution atomization and drying (figure 2).

On the assumption that tiny water droplets on the wafers were somehow related to the formation of particles, the Mercury MP rinse plumbing was modified to produce primarily large droplets. Large droplets were created by colliding the streams of water from the Solution Line Rinse and the Final Rinse lines (figure 2). This stream of large droplets was used as the final step of the rinse to remove any tiny droplets that were left on the wafer by the cold, atomized rinse. The large droplets were removed from the wafer during the spin dry cycle.

The cleans were performed with "Megabit grade" chemicals with less than 10 ppb of any particular metallic contaminant. Particle data on 125 mm wafers was gathered on a WIS-150 particle counter for the HF Last cleaning sequence shown in table I. Metals performance was determined through TXRF measurements by Charles Evans & Associates, Redwood City, CA.

RESULTS AND DISCUSSION

A typical particle map for a standard HF Last process with atomized rinsing is shown in figure 3. Note the bands of particles and relatively clean areas that radiate from the bottom right corner of the wafer. The wafer was oriented in the cassette such that the spray post is at the bottom of the image and the direction of the centrifugal force is upward.

If the process is interrupted a few seconds into the spin dry cycle, the wafers have streaks formed out of tiny water droplets surrounded by relatively dry areas. Water droplets of varying sizes are produced by the atomized rinse. Large droplets are removed from the wafer by the centrifugal force of the spinning turntable. Very small droplets are not ejected by the centrifugal force and dry in place.

A dry streak with no tiny droplets occurs when a large droplet moves across the wafer and "picks up" the smaller droplets. To demonstrate this effect, hold a freshly etched, hydrophobic wafer vertically and dispense a fine mist of DI water onto the wafer with a hand spray bottle. (Do not use a bottle that has been contaminated with alcohol or a surfactant.)

The HFL particle performance results for the Mercury MP were dramatically improved by the modification of the final rinse. Particle data for HFL cleans was gathered on 125 mm wafers for particles greater than 0.3 μm. Figure 4 shows the average particle results for eight runs of 25, 125 mm wafers. The circles indicate the average number of particles added or removed from all 25 wafers. The triangles indicate the average for wafers 1-24, the top wafer is omitted. Figure 5 shows the particle data for the individual wafers in runs 1, 3 and 5 (the top wafer for run 5 was off scale). This is the finest particle performance for an HF Last application in a centrifugal spray processor that has been reported.

Mechanisms Of Particle Formation

A water droplet could produce a particle (or light scattering center) either by promoting a localized chemical reaction or by the residue of its dissolved solids. Any chemical reaction would have to proceed rapidly as the droplets dry in less than 10 minutes. Grundner et al[5] notes that the exchange from Si-F groups to Si-OH groups is largely complete in 30 seconds and that these Si-OH groups may nucleate oxidation. Morita et al[2] reports the growth of a 2.6 A oxide layer during a 2 minute rinse. However, the reaction then slows with the average oxide thickness rising to 3.3 A in 60 minutes. Unless oxide growth is initiated and proceeds very rapidly around crystalline defects or some other nucleation center, it is unlikely that the quantity of oxide would be sufficient to be detected by an optical particle counter.

The effect of wafer "quality" supports theories which involve a nucleation center. High quality, "prime" wafers have consistently given better particle performance than repolished wafers. Figure 6 shows the particle results for two HF Last cleans on the same boat of repolished wafers. The wafers were cleaned using a modified RCA clean (SPM, HF, RCA-1, RCA-2) before each of the HFL cleans to achieve low initial particle counts (<200 per wafer) and a consistent surface chemistry. There is a strong correlation between the number of "particles added" to a wafer between the two cleans. This correlation indicates that there is some attribute of wafers that influences their performance in HF Last cleans. Further work is necessary in this area.

Blackford[6] has found that the DI water in advanced IC production lines typically contains between 1 and 5 ppb by volume of dissolved solids. On a hydrophyllic, oxide coated wafer, the rinse water wets the wafer surface and forms a layer that is reduced to a thickness of a few microns by the centrifugal force of the spinning turntable. This water then evaporates and deposits any dissolved solids uniformly across the wafer with an average thickness of less than 0.0001 monolayer. Dissolved species or tiny (< 0.1 μm) particles which have passed through the water filters do not combine to form large particles and hence remain below the detection limit of present optical particle counters.

But freshly etched wafers are hydrophobic, any water left on the wafer gathers into beads. If the wafer contact area of the droplet remains constant as the droplet dries (the droplet collapses), the residue from a 300 μm droplet of water with 1 ppb dissolved solids would form a 300 μm disk with a thickness of 0.001 monolayer. It is unlikely that these disks could be detected by either optical particle counters or an SEM.

However, if the wafer contact area of the droplet contracts as the droplet dries (the droplet "shrivels up"), the residue of a 300 μm diameter droplet would form a 0.3 μm particle. Such a particle would be detected easily by either an SEM or an optical particle counter.

Correlation With Past Observations

The water drop mechanism does not explain all of the phenomena associated with HF Last processing. For instance, Bluhm notes that the particle performance of HFL cleans in baths can sometimes be improved by electrically grounding the wafer or the HF bath[7]. This effect is possibly related to the electrostatic effects in particle deposition from liquids described by Donovan et al[8].

However, the water droplet mechanism does explain many observations. It has long been known that Spin Rinse Driers (SRDs) should only be used to spin dry hydrophobic wafers, the rinse should not be used. This can be explained by noting that most of the water sheets off of the wafers as the boat is removed from the rinse bath leaving few tiny droplets. Spraying water on the wafers in the SRD is counterproductive.

Bluhm notes that "Makers of SRDs also report the severity of the [*HFL particle*] problem to depend on their spray nozzle designs, with large, low velocity flows producing the best results."[7] Presumably these low velocity flows consist of

relatively large droplets which slide off of the wafers more easily during the spin dry than do the small droplets from a high velocity jet.

It has been observed that there is a concentration of particles in the center of wafers processed in an SRD. This can be understood by noting that the centrifugal force on a droplet in an SRD is proportional to the drop's distance from the center of rotation. Even large drops near the center of the wafer feel little force and tend to dry in place. Drops near the center also have little chance of being "picked up" by a larger droplet that is traveling outward on the wafer.

There are a number of possible mechanisms which would explain the findings of Zazzera et al that cold rinses left fewer particles than hot rinses[9].
1) Hot water droplets can evaporate quickly enough to dry in place and leave a residue before a large droplet can pick them up.
2) Droplets of hot water could evaporate to dryness and form particles in the gas which then land on the wafer.
3) The hot water used in Zazzera's study had a higher content of dissolved solids than did the cold water.
4) Any localized corrosion phenomena that occurred would probably be accelerated by higher temperatures.

Zazzera also noted that long rinses, either hot or cold, added more particles than did short rinses. This observation is consistent with mechanisms 1, 2 and 4 of the previous paragraph. This effect is possibly related to the electrostatic effects in particle deposition from liquids described by Donovan et al[8]. Presumably a number of mechanisms contribute to the final particle count on HFL wafers. Experiments are under way to access the importance of each of these mechanisms.

Metals Performance

The numbers in table II demonstrate part of the potential metals performance of HF Last cleans. The performance was excellent for Cr and Zn, good for Fe and Ni and moderate for Cu. Note that all numbers are in units of 10^{10} / cm^2. Even the "moderate" Cu signal would have been below the detection limit of the previous generation of TXRF instruments.

The high level of Cu is typical for HF etches. Metals such as Cu which have a higher electronegativity than Si tend to plate out of solution[10]. Table III shows the electronegativities of some potential contaminants. Shimono et al showed that ppb levels of Cu in HF plated out and caused measurable reductions in recombination lifetime. But ppm levels of Al, Cr, Fe, and Ni caused no reductions, these metals did not plate out. Presumably the Fe and Ni signals in the present study result from metals that either were not removed from the wafer or from some other source, not from contamination in the HF.

Cu plating can be reduced greatly by the addition of a few percent of H_2O_2 or HCl to the HF[3,4]. Wafers cleaned with HF + H_2O_2 that had been spiked with 1 ppm Cu showed no degradation in carrier lifetime compared to those processed in clean HF[4]. It appears to be possible to achieve excellent particle and metal results simultaneously with HF Last processing in centrifugal spray processors.

CONCLUSIONS

The dominant source of particles in HF Last processes in centrifugal spray processors is tiny water droplets that dry in place on the wafer. These tiny droplets can be eliminated by gently rinsing with large droplets which collect any tiny droplets as they pass over the wafer. Particle performance of much less than ten particles greater than 0.3 μm in diameter added with promising metal performance in an HF last clean has been achieved in a production environment.

ACKNOWLEDGMENTS

The author is grateful to B. Carlson for his help in refining the process, to R. Renne, T. Cardinal and D. Gafney for machine modifications, to H. Savage, M. Beasley, D. Grant and D. Deal for their helpful discussions and support and to the FSI engineering staff for fixing my prototype designs.

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9. L. C. Zazzera et al, "Investigation of H_2SO_4:H_2O_2, Dilute HF and DI Water Silicon Wafer Cleaning Processes", in "Semiconductor Cleaning Technology/1989," J. Ruzyllo and R. E. Novak, Eds., PV 90-9, p. 43, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1990).

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11. D. B. Summers, "Chemistry Handbook", 2nd Ed., Willard Grant Press, Boston (1975).

TABLES

Table I. HFL cleaning sequence in the Mercury MP

2:1 H_2SO_4:H_2O_2
rinse with hot DI
90 seconds of 15:1 HF
rinse with cold DI
spin dry with N_2

Table II. TXRF Results On HF Last Wafers

	Cr	Fe	Ni	Cu	Zn
Control Wafers					
	<DL	4	6	7	400
	<DL	6	<DL	<DL	400
	<DL	2	5	5	300
	<DL	8	<DL	<DL	350
	<DL	8	5	6	400
HF Last Wafers					
	<DL	2	<DL	10	<DL
	<DL	2	<DL	15	<DL
	<DL	2	4	30	<DL
	<DL	3	<DL	15	<DL
	<DL	2	<DL	15	<DL
	<DL	<DL	4	45	<DL
Approximate Detection Limit					
	2	2	2	2	5

TXRF data for wafers after an HF Last clean. All numbers are in units of 10^{10} atoms/cm^2. "<DL" indicates that the signal is below the detection limit. TXRF measurements by Charles Evans & Associates, Redwood City, CA.

Table III. Electronegativities of Selected Contaminants[11]

1.5	1.6	1.8	1.9	2.2	2.4
Al Mn Ti	Zn Cr	Si Ni Sn Fe	Cu	Pt	Au

Elements with electronegativities near or above that of silicon can plate out of solution and cause metallic contamination on the wafer[10].

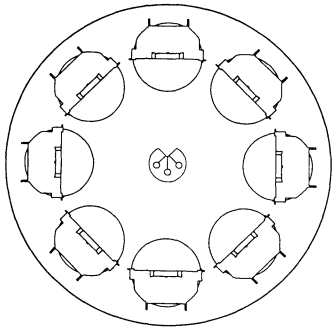


Figure 1

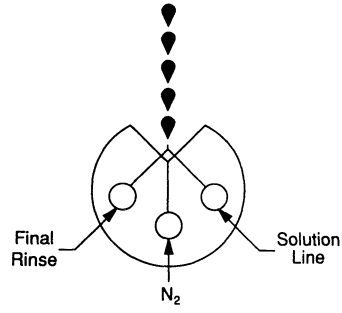
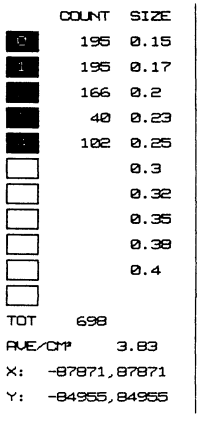


Figure 2



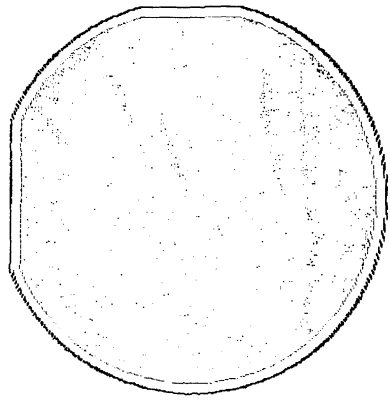


Figure 3

Figure 1. The mechanical arraignment of components in an FSI Mercury MP. Cassettes of wafers are loaded into a turntable that rotates clockwise when viewed from above. There is a stationary spray post in the center with sources for chemicals, rinse water and nitrogen for solution atomization and drying.

Figure 2. Mercury MP spray post with sources for chemicals, rinse water and nitrogen for solution atomization and drying. Large droplets of water were produced by colliding the streams of water from the Solution Line Rinse and Final Rinse lines.

Figure 3. Map of "particles" on an HFL wafer. Note the bands of particles that extend upward. There is a very similar banded pattern of tiny water droplets visible on the wafer at the beginning of the dry cycle. The bands of particles and droplets radiate outward from the spray post.

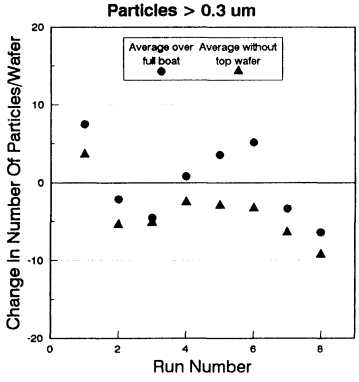


Figure 4

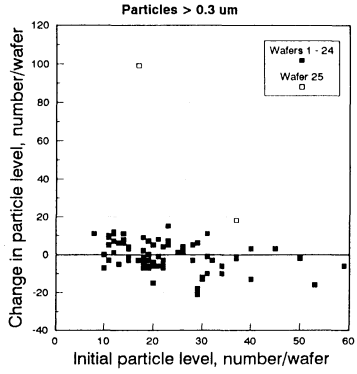


Figure 5

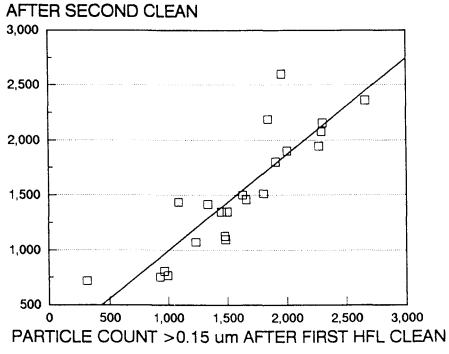


Figure 6

Figure 4. HF Last particle performance for 8 runs on full boats of 125 mm wafers. The circles indicate the number of particles added or subtracted averaged over all 25 wafers in the boat. The triangles indicate the averages for boat positions 1-24, the top wafer is omitted.

Figure 5. Particle data for the individual wafers in runs 1, 3 and 5 in figure 4. The top wafer for run 5 is off scale and is not shown.

Figure 6. Particle results for two HF Last cleans on the same boat of repolished wafers. The wafers were cleaned using a modified RCA clean (SPM, HF, RCA-1, RCA-2) before each HFL clean to achieve low initial particle counts (<200) and a consistent surface chemistry.

Monitoring of Heavy Metal Contamination During Chemical Cleaning with Surface Photovoltage

L. Jastrzebski, O. Milic, M. Dexter
Center for Microelectronics Research,
University of South Florida
J. Lagowski
Semiconductor Diagnostics, Inc., Tampa, Florida
D. DeBusk
National Semiconductor, West Jordan, Utah
K. Nauka
Hewlett-Packard, Palo Alto, California
R. Witowski, M. Gordon
SEMATECH, Austin, Texas
E. Persson
AT&T Microelectronics, Orlando, Florida

ABSTRACT

This paper presents SPV applications for the monitoring of chemical cleaning and purity of chemicals through mapping of minority carrier diffusion length, Fe concentration in the bulk, and surface contamination (surface charge and surface recombination). The non-contact, wafer-scale character of the new SPV approach, and refined apparatus, make this technique uniquely suited for heavy metal monitoring. This method was used to monitor Cu contamination in BHF by measurement of its effect on surface recombination and Fe contamination through it effect on bulk recombination after RTA step used to drive Fe deposited at the surface during cleaning into the bulk. Fe surface contamination was measured down to the 1 x 10^9 cm^{-2} level while the detection limit of this approach is 2 x 10^8 cm^{-2}. Different Fe contamination levels (1 to 13 ppb) present in different grades of H_2O_2 were easily distinguished. This procedure should allow one to monitor Fe contamination in H_2O_2 at the 1 ppt level. Cleanliness of incoming chemicals is not always a limiting factor and often is not related to the cleanliness of chemicals at the point of use (in the cleaning station).

INTRODUCTION

The continuing increase of IC circuit complexity, and the reduction of critical dimension that requires reduction of gate oxide thickness, generates a need for better control of heavy metal contamination. Published data on acceptable contamination levels, that do not deteriorate gate oxide integrity, are 10^{12} cm^{-2} for 1.25 μm technology (200 Å oxide thickness)(1) and 10^{10} cm^{-2} for 0.5 μm technology (125 Å oxide thickness).(2) By the end of this decade the acceptable limits will probably be reduced to 10^{8} cm^{-2}.(3) This puts stringent demands on cleaning methods and characterization techniques. There is an urgent need for a fast, inexpensive, high-throughput measurement method that can be used as a QC method to qualify, in real-time, cleaning processes, incoming chemicals, chemicals at point-of-use, and performance of cleaning stations.

We explore the application of SPV (Surface Photovoltage) to monitor chemical cleaning. Compared to other technologies such as TXRF or AAS, the application of SPV to monitor cleaning processes is rather new, although some impressive strides have already been made. The major advantages of the SPV approach over traditional techniques are: capability of contactless measurements on patterned (product) wafers, no sample preparation is required, the short measurement time (on the order of seconds) which allows real-time feedback and unmatched sensitivity (on the order of 10^{8} cm^{-2} for Fe).

The constant photon flux surface photovoltage method(4) was used to monitor heavy metal contamination introduced by wet chemistry. We used a commercial Contamination Monitoring System (CMS III), manufactured by Semiconductor Diagnostics, Inc., to measure lifetime under conditions of very low excitation level, surface recombination velocity and surface charge.

Principles of Surface Photovoltage

In the constant photon flux SPV method, minority carrier diffusion length is determined from a spectral dependence of the surface photovoltage, ΔV, and specifically from a dependence of ΔV on the light penetration depth, α^{-1}, where α is the absorption coefficient.(4) A depletion (or inversion-depletion) type surface barrier (shown in Figure 1 for an n-type semiconductor) is best suited for measurement. This assures preferable collection of the excess minority carriers in the surface space charge region, while the majority carriers are repelled from the surface and play an insignificant role. In this method the accumulation of minority carrier should be a predominant mechanism leading to the surface photovoltage.

Two additional mechanisms shown in the bottom of Figure 1, trapping of minority carriers by deep levels and trapping by surface states, are essential in non-contact SPV-DLTS,(5) however, they interfere with diffusion length measurement. They introduce hysteresis corresponding to long-time constant components (in silicon in the minutes to 10 ms range) of the light-on/light-off SPV relaxations. They are suppressed using light-chopping frequencies in the 500-600 Hz range which is high in comparison to the inverse of surface state time constant.

To avoid unambiguity related to the dependance of lifetime on the generation rate, SPV measurements were carried out under conditions of very low excitation -- 10^{11} to 10^{13} photon/cm^2 per second. For these generation rates an excess minority carrier concentration in n-type 10 Ωcm silicon with lifetime of 10^{-5} sec (100 μm diffusion length) is on the order of 10^8 to 10^{10} cm^{-3}, which is 10^{-7} to 10^{-5} of majority carrier concentration. It has to be pointed out that this generation rate is 10^6 to 10^8 times lower than the generation rates used in lifetime measurement methods using laser generation (e.g., PCD microwave reflectance or ELYMAT). Dependence of lifetime on generation rate, shown in Figure 2, demonstrates that a significant difference in the measured values of the lifetime at low and high generation rates could exist. The change of lifetime with generation rate is a function of majority carrier concentration and characteristic of recombination centers present in silicon. As was pointed out by Zoth(6), in the case of Fe measurements, results obtained at low generation rates are not transferable to high generation rates. The procedure for Fe measurements and Fe calibration curves developed for low generation rates and discussed below are not transferable to other lifetime measurement techniques which use high generation rates.

Dependance between the magnitude of the SPV signal, the penetration depth of light, and bulk and surface contamination (diffusion length, surface recombination and surface charge) were derived(4) and can be expressed for depleted surface as:

$$\Delta V = \Phi_{eff} \frac{kT}{qn_0} \frac{\exp(-qV/kT)\ \alpha L}{qn_0(S + D/L)\ (1 + \alpha L)} \qquad [1]$$

and for the inverted surface is:

$$\Delta V = \Phi_{eff} \frac{kT}{qn_i^2} \frac{n_0\ \alpha L}{(S + D/L)\ (1 + \alpha L)} \qquad [2]$$

where n_0 and n_i are the free carrier concentration in the bulk and intrinsic concentration, V is the surface barrier height, S is the surface recombination, D is

diffusion coefficient of minority carriers, L is diffusion length, α is light absorption coefficient, and Φ_{eff} is the effective photon flux absorbed in silicon.

Both equations can be written in the form:

$$\frac{\Phi_{eff}}{\Delta V} = A \frac{1}{L} (S + D/L) (\alpha^{-1} + L) \qquad [3]$$

where:

$$A = \frac{qn_i^2}{kTn_0} \qquad \text{for inversion}$$

$$A = \frac{qn_0}{kT} \exp\left(\frac{qV}{kT}\right) \qquad \text{for depletion}$$

The last term provides information about L while the other terms provide information about S and V.

It follows from Equation [3] that, in the constant photon flux SPV measurements, the slope of the line $\Phi_{eff}/\Delta V$ versus α^{-1} can be used to evaluate the product (S + D/L) exp(qV/kT) for the depleted surface region and (S + D/L) for the inversion region (providing that n_0 is known for the measured wafer), when the intersection of the line with the "x" axis will determine L (see Figure 3).

All previous discussion considered a very low excitation level, however, using the same SPV apparatus, but a high excitation level, the surface barrier height, V, can also be determined. With increasing light intensity the SPV signal reaches saturation which occurs when the amount of minority carriers at the surface leads to flat band conditions (see Figure 4). This will occur for generation rates on the order of 10^{17} to 10^{18} photon per cm^2/sec. Then, the SPV signal will correspond to the barrier height. Surface barrier, for the depleted case, is related to surface charge, Q_{ss}, through the expression(7):

$$Q_{ss} = \sqrt{\frac{2 n_0 \epsilon_s kT}{q^2} \left(\exp\left(-\frac{qV}{kT}\right) + \frac{qV}{kT} - 1\right)} \qquad [4]$$

where ϵ_s is the dielectric constant of silicon and V is the surface barrier.

This SPV approach to surface charge determination is contactless and is different than the approach used by the Surface Charge Analyzer (SCA), which forces flat band conditions with an external voltage applied by an electrode pressed to the wafer surface.

Certain metal impurities deposited on the silicon surface, and not driven into the bulk, could manifest themselves as efficient surface recombination centers or could introduce surface charge. Our investigation of the effect of heavy metals on surface charge and surface recombination has just began and our knowledge is still rather limited. So far, we have established that Cu on the surface of p-type 10 Ωcm silicon has a rather limiting effect on the barrier height (surface charge), but a dramatic effect on surface recombination. Figure 5 shows the effect of Cu on surface charge for a p-type silicon wafer intentionally contaminated with Cu. These wafers were cleaned with SC-1, SC-2 prior to the contamination and copper was deposited from BHF contaminated with Cu salt to concentrations varying between 1 ppb and 1 ppm. The samples were subsequently rinsed with DI water. Corresponding Cu concentration was measured with TXRF. Unless the Cu surface concentration exceeds few 10^{14} cm^{-2}, its effect on surface charge is not noticeable. The effect of Cu on surface recombination is more pronounced. Figure 3 shows the SPV plot of I/SPV as a function of 1/alpha for two samples exposed to 100 ppb Cu contaminated BHF and non-contaminated (copper concentration of 1.5 x 10^{14} and 1 x 10^{12} cm^{-2}, respectively), which were measured after the DI rinse. Diffusion length is identical in these samples since they were not exposed to a heat treatment and Cu is only on the surface, but the slope, which is equal to:

$$\frac{qn_0}{kT} \exp\left(\frac{qV}{kT}\right)\frac{1}{L}(S + D/L) \qquad [5]$$

is different. For these contamination levels the barrier height (surface charge) is not changed (see Figure 5) and the observed change of the slope is caused by the surface recombination increasing by about an order of magnitude to 8 x 10^3 cm/sec. Figure 6 shows the dependence of surface recombination (S + D/L) on Cu surface concentration as measured by TXRF (corresponding to Cu concentration in BHF between 1 ppb and 1 ppm). Dependance is linear for about 3 orders of magnitude of change of Cu concentration.

Information about bulk contamination is contained in diffusion length which is related to minority carrier lifetime through the relationship:

$$L = \sqrt{D \cdot \tau} \qquad [6]$$

where τ is lifetime and D is the diffusion constant for minority carriers. Under

conditions of low excitation, lifetime is reversely proportional to the concentration of recombination centers, N:

$$\tau = \frac{1}{\sigma \cdot \underline{V} \cdot N} \qquad [7]$$

where σ is the capture cross-section and $\underline{V}$ is the thermal velocity.

Procedure for Fe determination in p-type silicon, based on the temperature behavior of Fe-B pairs from diffusion length measured by SPV, was proposed by Zoth from Siemens.(6) In p-type silicon at room temperature, Fe forms Fe-B pairs with energy levels around 0.15 eV as determined by DLTS.(6) Above 180°C these pairs decompose and Fe becomes interstitial with an energy level of approximately 0.5 eV,(6) which is a much more efficient recombination center than the Fe-B pair. If the silicon wafer is quenched from this temperature to room temperature then Fe will remain frozen in the interstitial state and diffusion length measured after this treatment will be reduced. Fe in an interstitial state is metastable at room temperature and will pair with boron to form Fe-B pairs. Time required to complete this process depends on B concentration and temperature. At room temperature, for boron concentration around 1 x 10^{15} cm^{-3}, this time is on the order of 100 hours and is reduced to 20 minutes at 80°C.(8) Using samples intentionally contaminated to different levels with Fe, an empirical relationship between diffusion length prior to and after 200°C annealing and Fe concentration was established and is shown in Figure 7. Fe concentration was measured with TXRF on the sample surface prior to RTA, or with DLTS after drive-in. The optimal procedure for determination of Fe concentration in p-type silicon is: (1) measure L (L_{before}); (2) anneal the sample for 2 minutes at 200°C followed by quenching to room temperature; and (3) remeasure diffusion length (L_{after}) within a few minutes of quenching. The quenching can be done by placing the wafer on a large aluminum block or in water.(8) Fe concentration can be calculated from :

$$Fe(cm^{-3}) = 1.05 \times 10^{16} (1/L_{after}^2 - 1/L_{before}^2) \quad (L \text{ in } \mu m) \qquad [8]$$

which, for small changes of diffusion length, $\Delta L = (L_{before} - L_{after})$, $\Delta L << L_{before}$ for low Fe, contamination levels could be expressed as:

$$Fe(cm^{-3}) = 1.05 \times 10^{16} \times 2/L_{before}^2 \times (\Delta L/L_{before}) \qquad [9]$$

where ΔL is the change of L due to 200°C annealing.

In silicon wafers with low background contamination levels, diffusion length is on the order of 350 μm (above this value, for 650 μm thick wafers, the measured value of L will be affected by back surface(11)). Since reproducibility in L measurements under cleanroom conditions is 2%, this change in L due to Fe activation can be detected, therefore, according to Equation [3], the projected detection limit for Fe is 4 x 10^9 cm^{-3}. So far, it has been cross-correlated to other measurement methods (DLTS, TXRF) only above 2 x 10^{11} cm^{-3}, or 10^{10} cm^{-2}, which is the sensitivity limit for Fe detection for these methods.

Sensitivity of Fe measurements could be further improved if thicker, ultra-pure silicon is used. Measurements carried out on 2.5 mm thick silicon samples, with diffusion lengths in the range of 900 μm, by silicon manufacturers allows one to monitor Fe contamination with a sensitivity of 4 x 10^8 cm^{-3}. This procedure is valid when Fe is the dominant impurity as is the common case in silicon.(2) However, our preliminary results indicate that a similar procedure could be used for Cr and Ni determination although, at the present time, neither a detailed procedure nor calibration curves are available yet.

In order to monitor the efficiency of cleaning processes by bulk contamination measurements, one has to drive into the bulk heavy metals left on the surface of a silicon wafer with a high-temperature annealing. The time and temperature of this high-temperature annealing should be such that heavy metals left on the silicon surface will dissolve in silicon (their concentration will be lower than the solubility limit) and time will be sufficient to distribute them uniformly through the silicon wafer. Figure 8 shows time, at a given temperature, for various heavy metals required to diffuse through wafer thickness and calculated using published diffusion constants.(9) During these calculations we assumed that heavy metals are driven from the front and back surface of a silicon wafer.

In our experiments we used RTA to drive-in heavy metals, although furnace anneals could also be used. RTA was chosen because of its speed advantage compared to conventional furnace annealing, and because background contamination levels in RTA are usually very low since RTA is a cold wall system. The typical procedure used for determination of Fe concentration left on the surface is illustrated in Figure 9. An example of surface Fe contamination left by the state-of-the-art cleaning process and measured by our method is shown in Figure 10. The lowest Fe contamination measured by this approach was 1 x 10^9 cm^{-2} (2 x 10^{10} cm^{-3}). At the present time, we are not sure what is Fe contamination level introduced by RTA. Unfortunately, there are no other methods with sufficient sensitivity to cross-correlate our measurements. Assuming that the RTA contamination background is not a limiting factor, and that Fe detection is related only to the sensitivity of SPV measurements (4 x 10^9 cm^{-3}), we believe that this approach can detect Fe contamination left by cleaning on the wafer surface with sensitivity of 2 x 10^8 cm^{-2}

(for standard thickness silicon wafers) and 2 x 10^7 cm^{-2} (for 2.5 mm thick ultra-pure silicon samples). This limit has not yet been established for other heavy metals.

RESULTS

An example of the application of SPV to identify problems with wet chemistry in IC processing lines is shown in Figure 11. This IC line experienced periodic problems with heavy metal contamination and the oxidation furnaces were initially suspected as a source of heavy metals. SPV measurements clearly identified the problem to be related to the wet chemistry. Wafers #1 to #8 were not cleaned and oxidized as-received from the silicon supplier in the suspected furnace. Wafers #9 to #24 were cleaned in various cleaning stations and oxidized with Wafers #1 to #8. Wafer #25 is a control wafer which was not exposed to any processing. A significant reduction of diffusion length is observed in the wafers which were cleaned prior to the oxidation compared to the wafers which were not cleaned. This clearly identifies the cleaning stations as the source of heavy metals. To identify which chemical was responsible for the heavy metal contamination, we individually exposed the wafers to each chemical used in the cleaning sequence, rinsed them, and drove the heavy metals deposited on the surface into the bulk in the same oxidation furnace. The results shown in Figure 12 clearly identify H_2SO_4 as the source of heavy metal contamination.

Another example of the problem with wet chemistry, which resulted in a highly-contaminated spot on the wafer, is shown in Figure 13. The presence of the localized spot was caused by pre-epi wet cleaning with H_2SO_4-based solution during the last cleaning step (the wafer was subsequently exposed to high-temperature treatment). This pattern is much more pronounced in the surface contamination map (changes by three orders of magnitude) than in the bulk contamination map (changes only by a factor of three). The nature of surface and bulk contamination is not presently known, except that the centers are not related to Fe. It is of interest to note that once the cleaning sequence was reversed, and H_2SO_4 eliminated from the last step, the highly contaminated spot disappeared.

Cleanliness of incoming chemicals is not always the limiting factor, often procedures and equipment impose serious limitations, and can be a source of heavy metal contamination which exceeds, by far, the levels present in incoming chemicals. Equipment design, material used for hardware and equipment maintenance are often decisive factors (e.g., cracking of the protective coating on a turntable of one type of self-contained acid processor was found to be a major source of contamination during cleaning prior to gate oxidation). Characteristic contamination patterns left by various processing tools were observed. These patterns are related to the distribution of chemicals during cleaning and indicates that

equipment design could have an impact on cleaning uniformity. Figure 14 shows an example of a contamination pattern measured as surface recombination variations across a wafer and characteristic for spin drying equipment. This wafer was BHF etched, followed by DI rinse and spin drying, and measured prior to any heat treatment. This pattern is most likely related to residual Cu contamination.

In the case of wet chemical benches, insufficient frequency of changing of the chemicals, driven often by economical considerations, could lead to a substantial build-up of contamination and reduction of cleanliness. The reduction of diffusion length and increase of Fe concentration in wafers after gate oxidation, as a function of cleaning cycles, for cleaning used prior to gate oxidation is shown in Figure 15. The observed reduction of diffusion length and the increase of Fe concentration illustrates a build-up of heavy metal contamination in the cleaning sinks. It is interesting to note that there is a certain delay before this build-up occurred, it took place after the first few cleaning cycles.

Currently used cleaning could leave a significant amount of contamination on the surface of silicon wafers. Figure 16 shows a histogram of Fe surface contamination measured for about a few hundred silicon wafers supplied during 1990-1991 by various silicon vendors to IC fabrication lines. Fe was measured after drive-in into the bulk by RTA. Fe contamination in the bulk (prior to RTA) is also shown. The center of distribution of surface contamination is around 2×10^{10} cm^{-2} (5×10^{11} cm^{-3} after RTA). The lowest measured concentration is on the order of 1×10^{9} cm^{-2} while the highest is around 10^{12} cm^{-2}. The bulk contamination (prior to RTA) is usually an order of magnitude below the value of surface contamination. The center of distribution of the bulk contamination is around 5×10^{10} cm^{-3}. It could be as low as a few $\times$ 10^{9} cm^{-3} and as high as a few $\times$ 10^{12} cm^{-3}. The acceptable contamination limits for various technologies are also given in the figure caption. These limits were derived under the assumption that Fe concentration has to be ten times lower than the threshold value which will start yield degradation for a given technology. In the case of surface contamination, an assumption was made that no additional cleaning prior to IC processing would be used which would reduce the surface contamination.

Evaluation of Contamination Level in Incoming Chemicals

To evaluate heavy metal contamination in wet chemicals, the wafers were dipped in the chemicals for 10 seconds at room temperature, rinsed and dried, and heavy metals plated from the chemicals on the surface were driven in by RTA. Figure 17 shows the results for peroxide and sulfuric acid intentionally contaminated with Fe at the level of 1 to 100 ppm. It is clear that the amount of Fe detected by SPV in the wafers is proportional to Fe contamination in the chemicals.

A variation of this procedure, which resulted in much enhanced sensitivity, was developed by AT&T Microelectronics of Orlando, and was used to monitor Fe contamination in H_2O_2 at the ppb level. The experimental wafers were given a preclean using a sulfuric acid/hydrogen peroxide+ HF+ SC-1+ SC-2 cleaning sequence in a spray processor. This was followed by exposing the wafers to boiling H_2O_2 (of different grades) for 30 minutes. The wafers were given a DI water rinse and spun dry. A 1150°C, 2 minute rapid thermal anneal (RTA) heat treatment was used to diffuse any remaining surface residue into the silicon. SPV measurements were used to evaluate the performance of the chemicals.

Four groups of wafers (both n- and p-type bulk) were collected and measured. The wafer treatments and the results are summarized below:

Group 1: As-received p-type and n-type bulk control wafers. No heat treatment.

Group 2: Both types of wafers treated with the preclean to remove surface contamination typically found on in-coming control wafers. After the clean the wafers were given a 1150°C RTA drive-in for 2 minutes to diffuse surface contamination into the bulk.

Group 3: Wafers were treated with the initial preclean as in Group 2. Then the wafers were immersed in boiling "semi" grade (13 ppb of Fe by ICP/MS) hydrogen peroxide for 30 minutes. This was followed by the same RTA drive-in as in Group 2.

Group 4: These wafers had the same sequence of treatments as Group 3 except high purity (1 ppb of Fe by ICP/MS) hydrogen peroxide was used in the final step. The 1150°C RTA followed the chemical treatments.

Table I
Fe Contamination Introduced from Boiling H_2O_2

Group	Diffusion Length (μm)	Fe (cm^{-3})	Fe (cm^{-2})	Fe Conc. in H_2O_2 ICP/MS (ppb)	Cost (a.u.)
As-Received (bulk)	330 - 350	0			
Preclean + RTA Only	220 - 250	2E11	1×10^{10}		
"Semi" H_2O_2	75	3E13	1.5×10^{12}	13	1
High Purity H_2O_2	110	4E12	2×10^{11}	1	X4

The boiling H_2O_2 can plate out significant quantities of contamination to the wafer surface which are diffused into the bulk of a wafer during subsequent heat treatments. The boiling treatment increases the plating of heavy metals over that usually experienced during a typical cleaning cycle. The high purity H_2O_2 performed significantly better. The "semi" standard grade H_2O_2 with 13 ppb of Fe introduced an order of magnitude more Fe contamination than the high purity grade with 1 ppb of Fe. Cost of the high purity H_2O_2 is about three to five times higher than the "semi" grade. It is interesting to note that the pre-treatment cleans using a full sequence of high purity chemicals was not enough to completely eliminate all traces of the residual contamination. Various cleaning sequences, done in either sinks or spray processors, have yielded similar results.

Assuming that sensitivity detection limit of these measurements is limited by SPV sensitivity, and not RTA background contamination, we believe that the detection limit for Fe in H_2O_2 for this approach is 1 ppt (based on an SPV detection limit of 4×10^9 cm^{-3}). For a given concentration of heavy metals in chemicals, the plating process stops when it reaches equilibrium. The detection sensitivity of the approach could be significantly enhanced if all impurities, present in liquid, would be left on the surface. This could be achieved by drying a drop of chemical on the silicon surface and driving the residual left on the surface into the bulk by RTA. This residue contains all heavy metals which were in the drop (loss of heavy metals during evaporation is negligible) and the amount of heavy metals left on the surface could be much higher than in the case of plating. Assuming 0.1 cm^3 of chemical left on an area of 1 cm^2, one should be able to measure Fe contamination at the sub-trillion level. For measurement sensitivity limit of 2×10^8 cm^{-2}, one should be able to detect 0.06 ppt of Fe in chemicals with standard thickness silicon wafers and

0.006 ppt with 2.5 mm thick silicon. The biggest practical problem with the application of this approach is inhomogeneous distribution of heavy metals on the surface left during drying of the droplet (followed by RTA). Additional work is needed to improve and qualify procedures and to establish practical detection limits for various chemicals.

DISCUSSION

Typically, cleaning procedures are designed as multi-step processes in which each step removes different types of contamination, e.g., in standard clean (SC-1, SC-2) commonly used throughout IC industry, the first step is designed to remove organic contamination, and the second step is designed to remove metallic contamination. The first step uses ammonia and peroxide and usually plates a significant amount of heavy metals on the silicon surface(2) which are supposed to be removed by the second step. To control the concentration of Fe and Ni on the silicon surface to a level of 1×10^{10} cm^{-2} during the SC-1 step, the purity of the chemical solution at the point of use has to be at the 0.1-1 ppb level. Therefore, in any multi-step process, the efficiency of the second step is critical for metal removal. Our data showed that the efficiency of removal by the second step of heavy metals introduced by the first step is not always uniform across a wafer and the improvement of its uniformity and reproducibility is an important issue.

Another interesting issue is an apparent reduction of cleaning efficiency (ratio between contamination removed to the total amount of contamination on the surface prior to the clean) with a reduction of the contamination level. This problem should be thoroughly studied by carrying out experiments designed to measure cleaning efficiency of various cleaning methods for different levels of intentionally introduced surface contamination. These experiments should be able to answer the question of whether this problem is caused by fundamental limitations of presently used chemistries or if it is caused by practical limitations associated with background contamination levels present in state-of-the-art cleaning equipment.

All presently available data was obtained for planar, non-patterned wafers. Presence of sub-micron pattern, with features which are narrow and deep (e.g., trenches), could significantly affect the cleaning efficiency since the flow of liquid into and out of a narrow trench will be influenced by capillary forces and surface energy. Recent successful measurements of heavy metal contamination in 16 Mbit DRAM's, after completion of processing, showed that one can use SPV to measure patterned wafers with 0.5 μm geometries and this opens the possibility of using SPV to study the effects of sub-micron pattern features on the cleaning.

We believe that development of a better understanding of the interactions of heavy metals with silicon surfaces, their effect on surface charge and surface recombination, and their characteristics in bulk of p- and n-type silicon is essential in order to establish better methods to identify the presence and measure the concentration of heavy metals other than Cu and Fe.

SUMMARY

This paper presented SPV applications for the monitoring of chemical cleaning and purity of chemicals through mapping of minority carrier diffusion length, Fe concentration in the bulk, and surface contamination (surface charge and surface recombination). The non-contact, wafer-scale character of the new SPV approach, and refined apparatus, make this technique uniquely suited for heavy metal monitoring. This method was used to monitor Cu contamination in BHF by measurement of its effect on surface recombination and Fe contamination through it effect on bulk recombination after RTA step used to drive Fe deposited at the surface during cleaning into the bulk. Fe surface contamination was measured down to the 1 x 10^9 cm^{-2} level while the detection limit of this approach is 2 x 10^8 cm^{-2}.

A procedure was developed to monitor heavy metal contamination levels in liquid chemicals. Different Fe contamination levels (1 to 13 ppb) present in different grades of H_2O_2 were easily distinguished. This procedure should allow one to monitor Fe contamination in H_2O_2 at the 1 ppt level. Cleanliness of incoming chemicals is not always a limiting factor and often is not related to the cleanliness of chemicals at the point of use (in the cleaning station). Quite often equipment itself can impose serious limitations. It is apparent that equipment designers could benefit from a better understanding of their equipment performance limitations.

The SPV approach is very new compared to more traditional methods such as TXRF and AAS, but has already proven its usefulness in monitoring problems with wet chemistry in IC processing lines. Compared to more traditional methods, the major advantage of SPV measurement is its measurement speed; information is obtained a few minutes after completion of a process step, as well as the capability of carrying out contactless measurements in patterned product wafers.

ACKNOWLEDGEMENT

This work was partially supported by an SRC/SEMATECH contract monitored by Dr. Harlow as part of SCOE activity.

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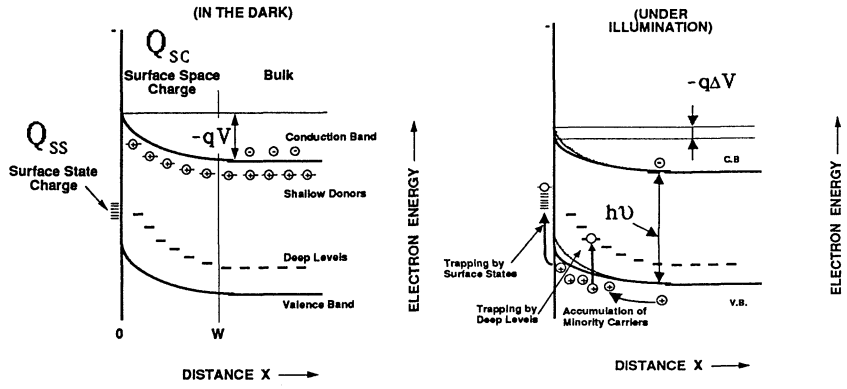

Figure 1. Energy band diagram near an n-type semiconductor surface with a depletion layer in the dark (left) and under low intensity illumination (right).

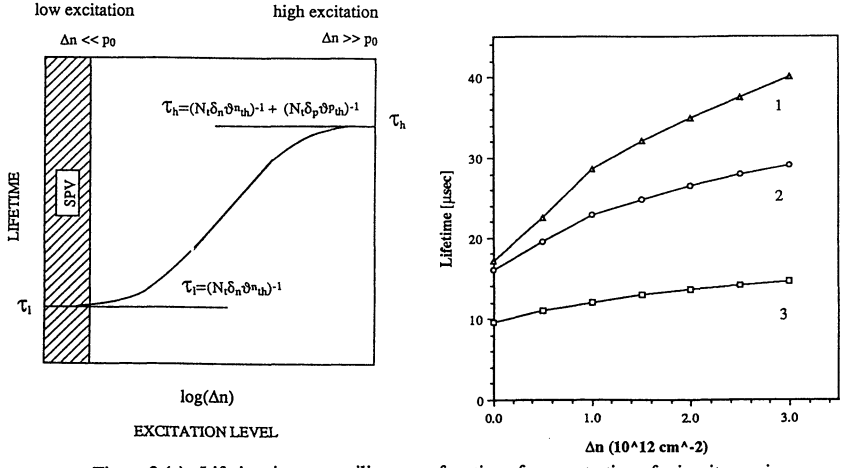

Figure 2 (a). Lifetime in p-type silicon as a function of concentration of minority carriers (generation rate). For high generation rate lifetimevalue could be significantly different than for low generation and depends on value of (capture cross-section for holes). If $\sigma_p << \sigma_n$ (e.g., donor type defect) then τ_H could be an order of magnitude higher than τ_l,for acceptor type defect $\sigma_n << \sigma_p$ and $\tau_H = \tau_l$. (b) Measured values of lifetime as a function of electron concentration in p-type silicon: 1 - p = 10^{14} cm^{-3}, 2 - p = 2.5×10^{14} cm^{-3} and 3 - 1.1×10^{15} cm^{-3}.[10]

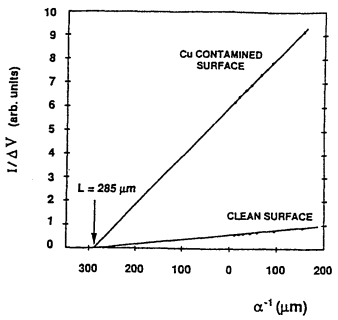

Figure 3. The sPV plots, I/ΔV versus α^{-1}, measured on the same wafer before and after surface contamination with copper. The intercept value determines the diffusion length, L, which remains unchanged. The slope of the line increases after contamination due to the high surface recombination (estimated as S = 8 x 10^3 cm/s).

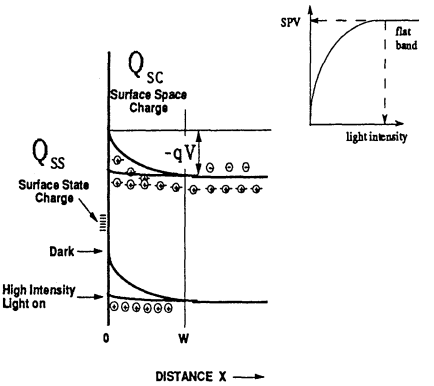

Figure 4. Condition used during Q_{ss} (surface charge) measurements and corresponding dependance of SPV signal on light intensity.

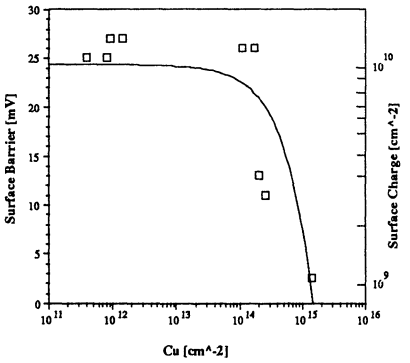

Figure 5. Surface charge (surface barrier) in p-type (10 Ωcm) silicon as a function of Cu surface concentration. Cu measured by TXRF on the surface.

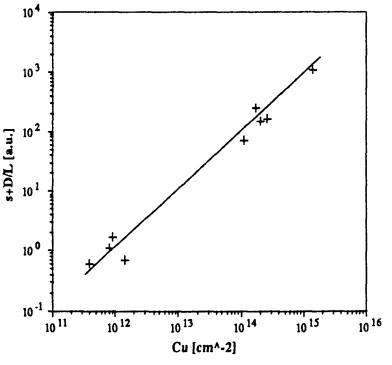

Figure 6. Surface recombination in p-type (10 Ωcm) silicon as a function of Cu surface concentration (TXRF).

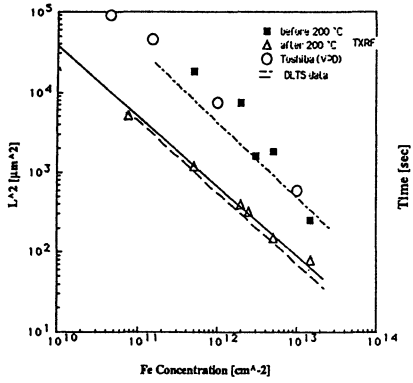

Figure 7. Dependence of diffusion length on Fe concentration prior to and after 200°C annealing (Fe activation). Dashed lines are DLTS measurements done by Siemens and RCA(3,6) after drive-in of Fe during high-temperature treatment; ● Δare our TXRF measurements; and ○are VPD measurements done by Toshiba.[12]

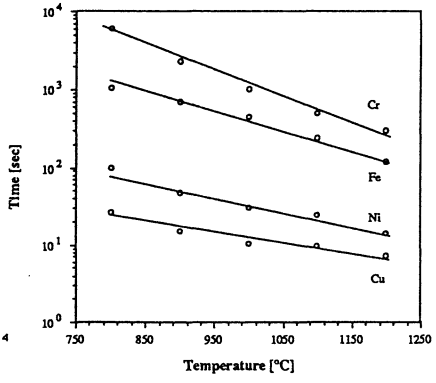

Figure 8. Time at a given temperature required for various heavy metals to diffuse through thickness of (625 μm) silicon wafer. Diffusion from the front and back surfaces.

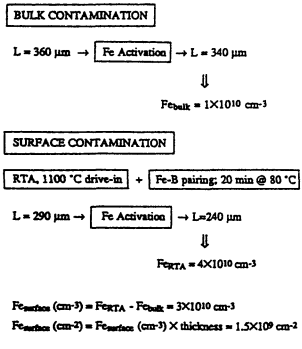

Figure 9. Procedure used to determine surface Fe contamination.

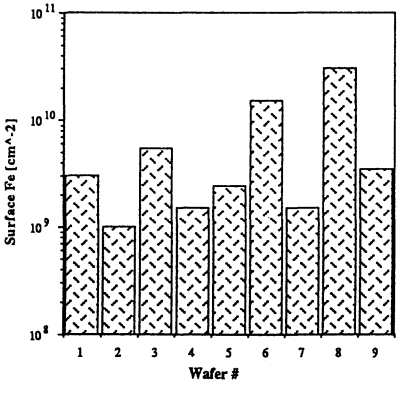

Figure 10. An example of Fe surface concentration left by state-of-the-art cleaning.

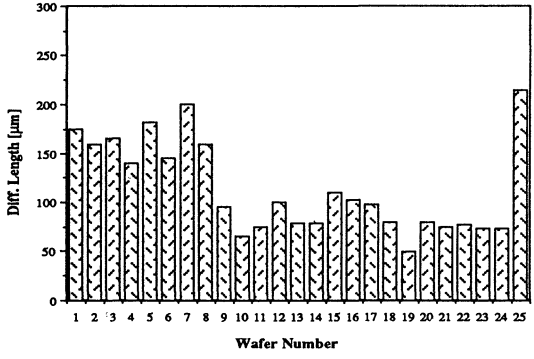

Figure 11. Contamination in wafers after oxidation in "suspected" furnace. Wafers 1 to 8 oxidized without cleaning, Wafers 9 to 24 were cleaned in various cleaning stations prior to oxidation. Wafer 25 was a control wafer. Reduction of diffusion length in Wafers 9 to 24 clearly identified cleaning stations as source of heavy metals.

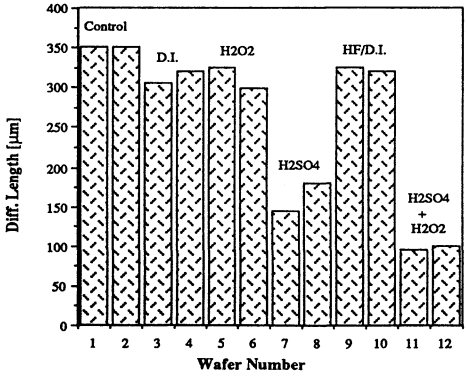

Figure 12. Diffusion length in wafers exposed to a single chemical used in cleaning (Figure 11) and oxidized. H_2SO_4 is identified as source of heavy metals.

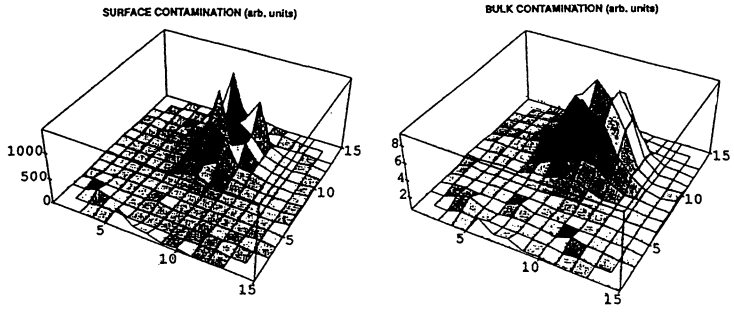

Figure 13. Localized contamination spot caused by pre-epi wet cleaning with H_2SO_4 present in the last step. Notice more pronounced effect on surface contamination than on the bulk contamination.

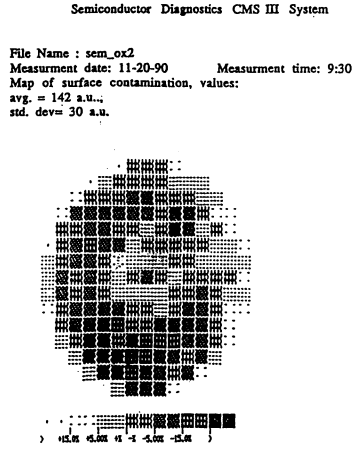

Figure 14. Characteristic surface contamination pattern left by spin drying equipment (BHF etch). Contamination measured as surface recombination (a.u.).

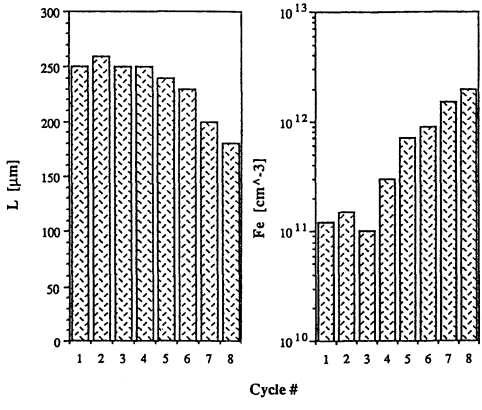

Figure 15. Increase of contamination level observed during cleaning in wet chemical benches prior to gate oxidation. L and Fe measured after gate oxidation. Notice that after about 3 to 4 cleaning cycles chemicals should be replaced.

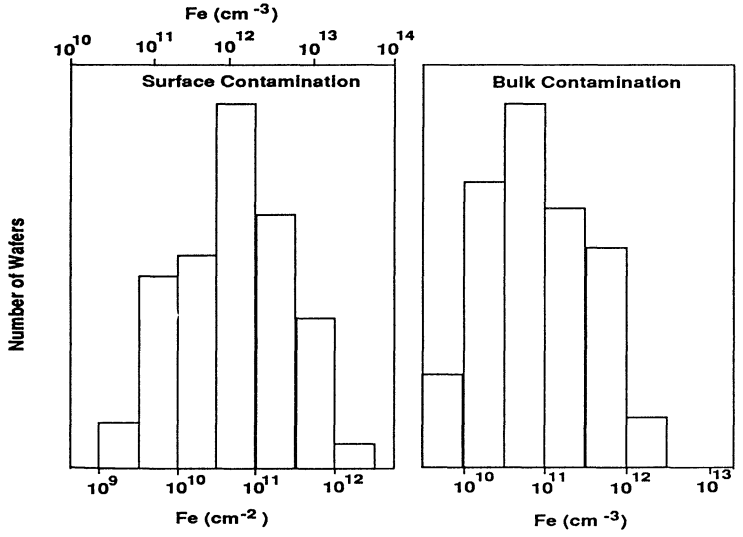

Figure 16. Histogram of Fe surface contamination in wafers supplied in 1990-1991 by various silicon vendors. Bulk Fe contamination in these wafers also shown in the figure. Acceptable threshold Fe concentrations are 10^9 cm^{-2} for 0.5 μm technology and 10^{10} cm^{-2} for 0.75 μm technology. Threshold concentrations causing yield degradation are 10^{10} cm^{-2} for 0.5 μm technology and 10^{11} cm^{-2} for .75 μm technology (see text).

CHEMICAL	Fe (ppm) Spectral Analysis of Chemicals	Fe (cm^{-3}) SPV	Corresponding Surface Concentration (cm^{-2})	L_o (μm)	L_1 (μm)
H_2O_2					
-1-	8	8×10^{11}	5×10^{10}	410	118
-2-	57	6×10^{12}	4×10^{11}	155	67
Sulfuric					
-1-	2.1	1.3×10^{12}	8×10^{10}	320	102
-2-	120	3×10^{13}	2×10^{12}	69	27

Figure 17. Fe contamination plated at room temperature for H_2SO_4 and H_2O_2 intentionally contaminated with Fe salt. Sensitivity of this approach could be enhanced by about 10^4 if boiling chemicals are used (see text).

DETECTION OF METAL CONTAMINATIONS FROM FURNACE TUBE MATERIALS

Masanori Kobayashi, Ken Yamazaki, Yoshiko Okui
and Tsutomu Ogawa
Process Development Division, Electronic Devices Group
FUJITSU LIMITED
1015 Kamikodanaka, Nakahara-ku, Kawasaki 211, Japan

A study of contaminations from furnace tube materials during annealing process was performed using "Sandwich Annealing Method": analysis of metallic impurities diffused into Si_3N_4 on the Si wafers, detection of the carrier lifetime in the Si wafers after being annealed between discs of furnace materials. The furnace tube materials studied were Type-I fused silica (electrical fusion of quartz powder), Type-II fused silica (flame fusion of quartz powder), and CVD-SiC-coated ceramic SiC (CVD-SiC/SiC). Transition metal contaminations of Cr, Fe, Ni and Cu from Type-I fused silica are more than those from Type-II fused silica and CVD-SiC/SiC, although the transition metal concentrations in Type-I and Type-II are in the same order. Type-I fused silica degrades carrier lifetime more than Type-II fused silica and CVD-SiC/SiC, which reflects transition metal contaminations. Na, K, Ca and Al contaminations from Type-I fused silica, Type-II fused silica or CVD-SiC/SiC, are below the detection limit.

INTRODUCTION

Fused silica has been used for annealing and oxidation of semiconductors, because of its high purity, as well as chemical stability and heat-resistivity. It has been reported, however, that metallic impurity penetrates through silica tube wall, resulting in contamination of Si wafers during annealing processes(1)(2). Moreover, impurities in fused silica, though its concentrations are below ppm, can also degrade the device characteristics of VLSI's.

In this paper, we study metal contaminations from furnace tube materials and their effects on the carrier lifetime in Si wafers using "Sandwich Annealing Method".

EXPERIMENTAL

"Sandwich Annealing Method"

A detection method, "Sandwich Annealing Method", is illustrated in Fig.1 and Fig.2. The procedure, shown in Fig.1, to detect metal contaminations from furnace tube materials is as follows: p-type 10Ω-cm (100) oriented 100mm diameter CZ Si substrates were deposited with 100nm thick CVD Si_3N_4 on both sides. After being sandwiched with 5mm thick and 100mm diameter discs of furnace tube materials, the samples were annealed in silica tube in N_2 ambient. Metal contaminants are supposed to diffuse into the Si_3N_4. The Si_3N_4 was then etched with an HF solution, whose metallic contaminants of Na, K, Ca, Al, Cr, Fe, Ni, Cu were detected with Atomic Absorption Spectroscopy (AAS).

The procedure shown in Fig.2, to detect the the carrier lifetime in Si wafers is as follows: n-type 10 Ω-cm (100) oriented 100mm diameter CZ Si substrates were oxidized at 900 ℃ in dry O_2 ambient to form 50nm thick SiO_2. After being annealed with the same conditions mentioned above, the samples were dipped in a diluted HF solution to remove the SiO_2. The samples were then oxidized again at 900℃ to form 25nm thick SiO_2, followed by being annealed at 450 ℃ in H_2-N_2 (H_2:3%) ambient to reduce surface states. Carrier lifetime in Si wafers was measured using photo-conductivity decay method with WAFER τ LTA-550 of LEO corporation.

Sample Preparation

The furnace tube materials studied were 18 items of fused silica from five venders shown in Table 1, and CVD-SiC-coated ceramic SiC (CVD-SiC/SiC), whose CVD SiC thickness was 10nm. In Table 1, Type-I and Type-II denotes fused silica formed by electrical fusion and by H_2-O_2 flame fusion of quartz powder, respectively.

The OH concentration of fused silica was detected measuring the absorption strength at 3663 cm^{-1} with Fourier Transform Infrared Spectrometer (FT-IR), whose typical spectra are shown in Fig.3.(3) The OH concentrations are shown in Table 1, where OH concentrations

in Type-I are 5-30 ppm, and those of Type-II, 150-300 ppm. The metal concentrations of Na, K, Ca, Al, Cr, Fe, Ni, Cu in fused silica were detected with AAS.

Application of "Sandwich Annealing Method"

"Sandwich Annealing Method" was applied for all the 18 items of fused silica and CVD-SiC/SiC with annealing condition at 1100℃ for 6 hr. in N_2 ambient, to survey the effects of the impurity and OH concentration in the furnace tube materials.

"Sandwich Annealing Method" was then applied for A-I-1 (Type-I), C-II-2 (Type-II) and CVD-SiC/SiC with annealing conditions at 900, 1000, 1100 and 1200℃ for 6 hr. in N_2 ambient, to study temperature dependence of the metal contaminations and the carrier lifetime degradation,

RESULTS

Metal Contaminations from Furnace Tube Materials

Fig.4 shows the correlations between OH concentration and Cr, Fe, Ni and Cu concentration in fused silica, where no particular relation is found.

Fig.5 shows the relations between OH concentration in fused silica and contaminations of Cr, Fe, Ni and Cu from the fused silica during 1100 ℃ 6 hr. annealing, where contaminations from Type-I fused silica are more than those with Type-II fused silica. In Fig.5, contaminations from CVD-SiC/SiC are also plotted, which are the same or below those from Type-II fused silica.

Fig.6 shows the carrier lifetime of the Si wafers with the same conditions mentioned above. Type-I fused silica degrades the carrier lifetime more than Type-II fused silica and CVD-SiC/SiC, which reflects the contaminations shown in Fig.5.

Being different from transition metal contaminations, contaminations of Na, K, Ca and Al from either fused silica or CVD-SiC/SiC with the same condition as mentioned above

are under detection limit. Detection limit for Na, K, Ca and Al was 1.2E10cm $^{-2}$, 1.0E10cm^{-2}, 1.0E10cm $^{-2}$ and 4.0E11 cm^{-2}, respectively.

Annealing Temperature Dependence of the Contaminations

Fig.7 shows the contaminations of Cr, Fe, Ni and Cu from A-I-1 (Type-I fused silica), C-II-2 (Type-II fused silica), and CVD-SiC/SiC with 900-1200 ℃ 6 hr. annealing. (Table 2 shows the metal and OH concentrations in A-I-1 and C-II-2.) All the above transition metal contaminations from A-I-1 are detected, which have strong dependence on the annealing temperatures. Contaminations of Fe and Cu from C-II-2 are detected, which are less than those from A-I-1 and have a weak temperature dependence. Contaminations of Cu and Cr from CVD-SiC/SiC are detected, of which Cu contamination has a weak dependence on annealing temperature.

Fig.8 shows the carrier lifetime in the same conditions as mentioned above. A-I-1 degrades the carrier lifetime more than C-II-2 and CVD-SiC/SiC, which reflects the transition metal contamination shown in Fig.7.

DISCUSSION

"Sandwich Annealing Method" has the following advantages:
1. easy and economical testing of the tube materials without making testing tubes,
2. sensitive detection due to the high trapping efficiency of contaminants from the testing materials,
3. precise detection without disturbance of the other conditions such as gas flow, and figure and size of the testing materials.

Using this method, we have found that transition metal contaminations from Type-I fused silica (electrical fusion) are more than those from Type-II fused silica (flame fusion), although the transition metal concentrations in Type-I and Type-II fused silica are in the same order. Because the OH concentration in Type-II is one or two orders higher than that in Type-I, OH is supposed to act as a trapping site of transition metals, such as replacing the

hydrogen with transition metal or forming a complex.

In view of the deformation resistance at high temperatures, Type-II fused silica, with more OH concentration, is inferior to Type-I fused silica. We are, therefore, in dilemma as to whether to choose cleanliness or deformation resistance.

Transition metal contamination and carrier lifetime degradation by CVD-SiC/SiC are almost the same as those by Type-II fused silica. CVD-SiC/SiC has superior deformation resistance, together with low metal diffusivity through the wall. Therefore, CVD-SiC/SiC is a promising furnace tube material especially for high temperature processes.

CONCLUSIONS

Metal contaminations from furnace tube materials and their effects on the carrier lifetime in Si wafers were studied using "Sandwich Annealing Method". Transition metal contaminations of Cr, Fe, Ni and Cu from Type-I fused silica were more than those from Type-II fused silica and CVD-SiC/SiC. Carrier lifetime degradation by Type-I fused silica was more than that by Type-II fused silica and CVD-SiC/SiC, which reflects transition metal contaminations. Na, K, Ca and Al contaminations from Type-I fused silica, Type-II fused silica or CVD-SiC/SiC, are below the detection limit.

ACKNOWLEDGEMENT

The authors thank Ms. K. Murao for Atomic Absorption Spectroscopy and Mr. M. Yoshida and Mr. H. Tsuchikawa for their encouragement.

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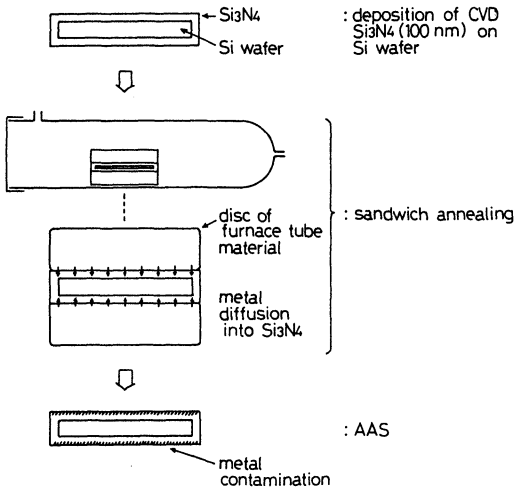


Fig. 1 Detection procedure of metallic contaminants from furnace tube materials using Sandwich Annealing Method.

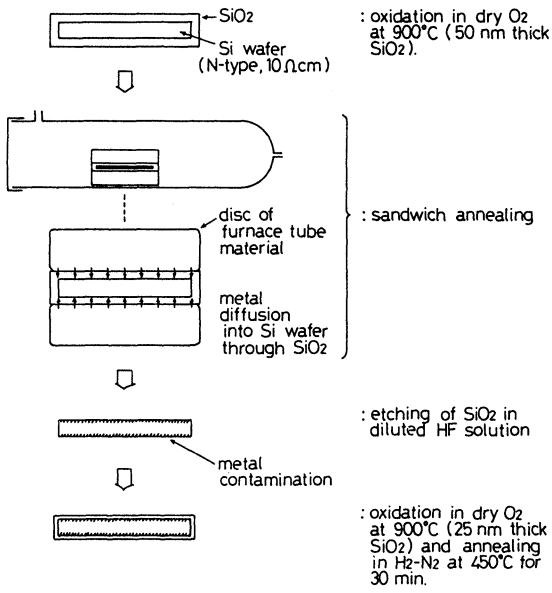


Fig. 2 Detection procedure of carrier lifetime degradation caused by metallic contaminants using Sandwich Annealing Method.

Table 1 18 items of fused silica

Vender	Item	Type(Fusion)	OH (ppm)
A	A- I- 1	Type -I (Electrical)	15.7
	A- I- 2		27.7
	A-II- 1	Type-II (Flame)	139.6
	A-II- 2		201
B	B- I- 1	Type -I (Electrical)	23.6
	B- I- 2		15.3
	B-II- 1	Type-II (Flame)	214
	B-II- 2		200
C	C- I- 1	Type -I (Electrical)	6.6
	C- I- 2		5.6
	C-II- 1	Type-II (Flame)	306
	C-II- 2		229
D	D- I- 1	Type -I (Electrical)	13.4
	D- I- 2		9.1
	D- I- 3		9.4
E	E- I- 1	Type -I	7.8
	E-II- 1	Type-II (Flame)	174.7
	E-II- 2		174.7

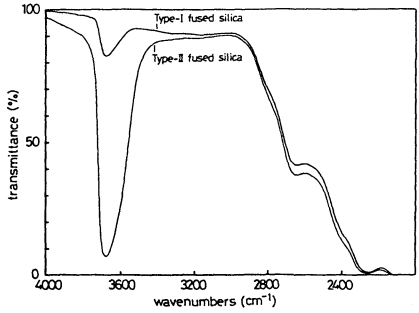
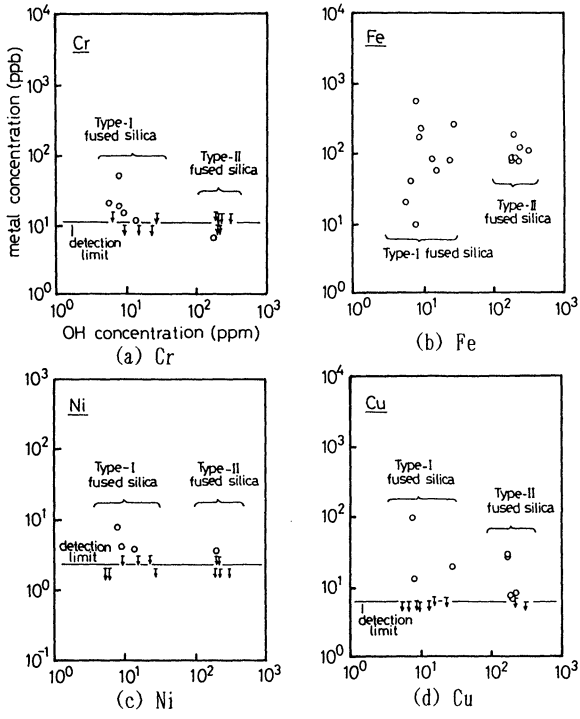


Fig. 3 Typical FT-IR spectra of Type-I and Type-II fused silica.

Fig. 4 Correlations between OH concentration and (a)Cr, (b)Fe, (c)Ni and (d)Cu concentration in fused silica.



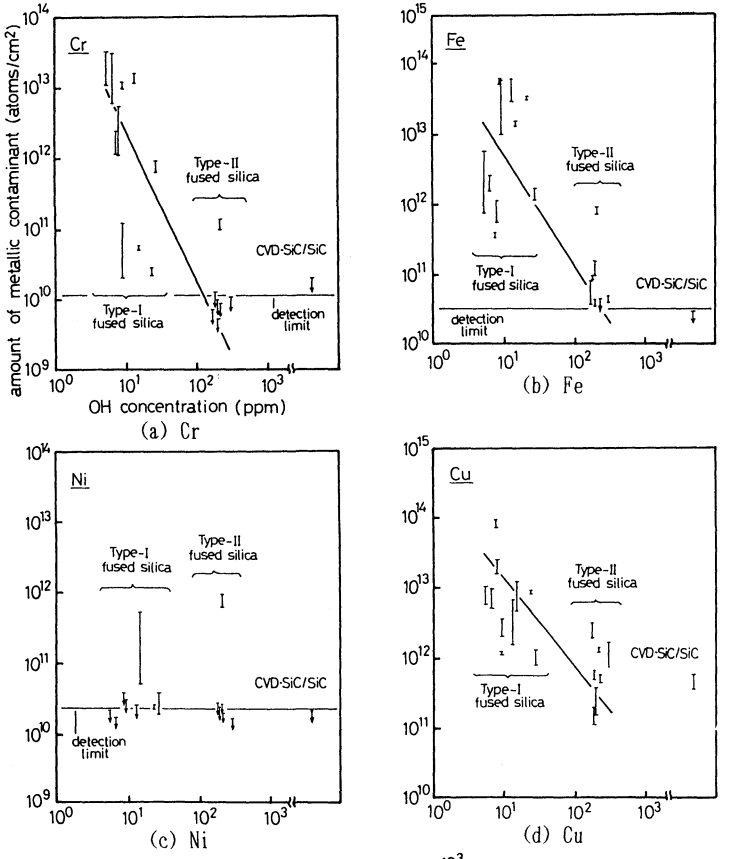


Fig. 5 Relations between OH concentration in fused silica and contaminations of (a)Cr, (b)Fe, (c)Ni and (d)Cu from the fused silica during 1100°C 6hr. annealing.

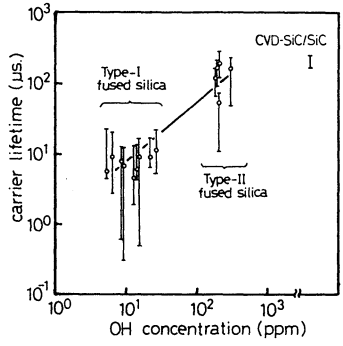


Fig. 6 Relations between OH concentrations in fused silica and the carrier lifetime of the Si wafers sandwiched between the discs of the fused silica and annealed (1100°C 6hr.).

Table 2 Metal and OH concentrations in A-I-1(Type-I fused silica) and C-II-2(Type-II fused silica).

	Na	K	Ca	Al	Fe	Cr	Cu	Ni	OH
A- I- 1	630	390	500	8400	550	50	13	7.6	15.7
C-II- 2	78	8.0	190	6600	120	<15	8.0	<2	229
								(ppb)	(ppm)

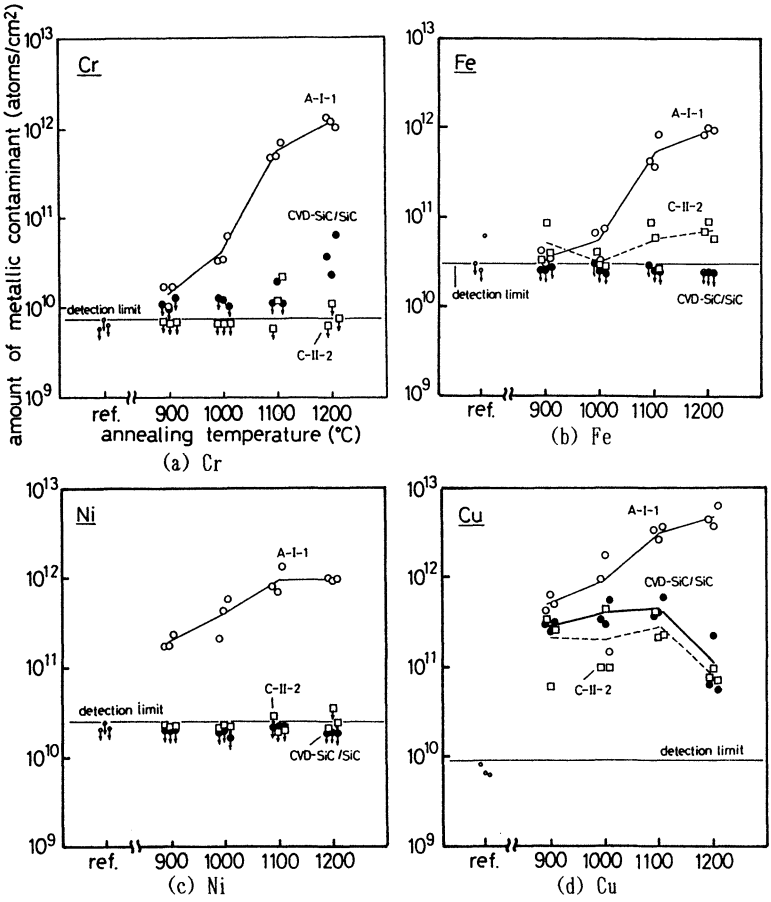


Fig. 7 Temperature dependence of the contaminations of (a)Cr, (b)Fe, (c)Ni and (d)Cu from A-I-1(Type-I fused silica), C-II-2(Type-II fused silica) and CVD-SiC/SiC with 900-1200°C 6 hr. annealing.

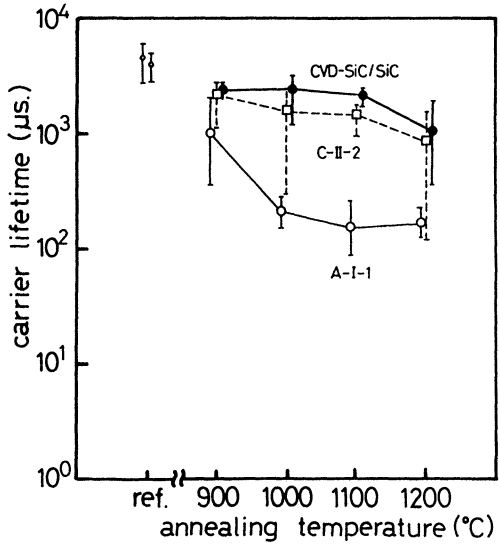


Fig. 8 Temperature dependence of the carrier lifetime of the Si wafers sandwiched between the discs of A-I-1(Type-I fused silica), C-II-2(Type-II fused silica) and CVD-SiC/SiC and annealed(900-1200°C 6 hr.)

TXRF ROUND ROBIN RESULTS

R. S. Hockett
Charles Evans & Associates
Redwood City, CA 94063

S. Ikeda
Ryukoku University, 2-23 Hayako-cho
Neyagawa City, Osaka 572, Japan

T. Taniguchi
Osaka Electro Communication University
2-23 Hayako-cho, Neyagawa City
Osaka 572, Japan

TXRF is expected to soon become a measurement of surface metal contamination for the commercial transaction of silicon substrates. In response to this emerging need, an ASTM F1.04 Subcommittee round robin has been completed for TXRF. The results are reported herein.

INTRODUCTION

In 1989 Eichinger, et al, reported the use of glancing x-ray fluorescence technology for the quantitative measurement of transition metal contamination on the surface of silicon wafers as a function of cleaning (1). The technique was called Total reflection X-Ray Fluorescence (TXRF). Since that time TXRF use has spread rapidly through the semiconductor industry. Recently, Watanabe reported the JEIDA survey results for 200 mm diameter silicon wafers (2). The results indicated an expectation that surface transition metal contamination for commercial wafers would need to be controlled at the 10^{10} atoms/cm^2 level, and that quantitative analysis and its standardization was therefore inevitable. The recent consensus report (3) from the Workshop on Silicon Materials for Mega-IC Applications sponsored by the ASTM, SEMATECH, SEMI and NIST was in agreement with the JEIDA survey results. Both studies placed an emphasis on TXRF as a method to meet this need.

In response to this need, two round robins have been completed for TXRF under the auspices of the ASTM F1.04 Subcommittee. (This Subcommittee has now been folded under Subcommittee F1.06.) Samples were silicon wafers with different levels of transition metal contamination on the surface. The first round robin, completed between

March and May of 1990, included six Perkin-Elmer ATOMIKA XSA-8000 units (4) in Europe and the U.S. The second round robin, completed between October 1990 and April 1991, included thirteen TECHNOS TREX 610 units (5) in Japan. Reference standards included residue approaches. This is a report of the results.

ATOMIKA XSA-8000 TXRF ROUND ROBIN

Samples and Calibration Standard

One calibration standard and five unknowns were used in the round robin. The samples were 100 mm diameter silicon substrates with surface contamination of Fe, Ni, Cu and Zn. One sample was a BLANK. The samples were shipped in a 25 wafer cassette and the standard was shipped in a single wafer cassette.

The standard was supplied by ATOMIKA. It was prepared at GKSS-Forschungszentrum by diluting an atomic absorption standard containing nickel, transporting a droplet of the liquid with known volume to the center of the silicon substrate, and allowing the droplet to dry. The assumption was made that the nickel did not leave by evaporation. The standard contained 1 ng of Ni (20×10^{12} atoms/cm^2 for an analysis area of 8 mm in diameter.) This calibration procedure was shown earlier to give TXRF surface analysis results consistent with vapor phase decomposition followed by atomic absorption spectroscopy and with nitrogen-beam Rutherford backscattering (6).

Procedure:

The samples were all measured once per day for four days. The calibration sample was first measured, then the five samples. Each sample and standard were analyzed in the center 8 mm diameter area for 1000 seconds. The instrument was operated with a Mo x-ray (17.5 keV) tube at 30 kV and 60 mA and with a grazing angle of 1.3 mrad. The ambient was air.

The data indicated the BLANK was contaminated after four of the six laboratories completed their measurements. Also, one wafer was broken and could no longer be used between the fifth and sixth laboratory measurements. The samples were remeasured after the completion of the round robin, and found to have not changed with the exception of the BLANK and the broken wafer. There is no other evidence to indicate accidental contamination of Fe, Ni, Cu or Zn on these samples.

Results

The statistical results of the round robin are shown in Table 1. The table gives the Lab averages, standard deviation (N-1), and one relative standard deviation in percentage (RSD%); and the grand average, standard deviation and RSD%, for Fe, Ni, Cu and Zn.

The data indicate interlaboratory percent relative standard deviation (RSD%) values of less than 10%, except when the amount of element is near the detection limit (about $3x10^{11}$ atoms/cm^2) in which case the RSD% is still less than 20%. The data also indicate that copper near the detection limit was not consistently detected by all the laboratories. A close study of the data indicate a systematic bias for Labs C and D compared to the Group average. Lab C read lower than the Group, and Lab D read higher than the Group, but these bias effects were less than 20%.

TECHNOS TREX 610 TXRF ROUND ROBIN

Samples and Calibration Standard

Two calibration standards and six unknowns were used in the round robin. One of the standards and four of the unknowns were taken from the earlier TXRF round robin study. All participating laboratories measured the same samples. The samples were 100 mm diameter silicon substrates with surface contamination of Fe, Ni, Cu and Zn. The samples were transported in a 25 wafer cassette.

The standard which was used in the earlier round robin was supplied by ATOMIKA via GKSS in Germany is labeled GKSS 181. The GKSS 181 standard contained 1 ng of Ni, or $1.3x10^{13}$ atoms/cm^2 and $2.0x10^{13}$ atoms/cm^2 for 8mm (XSA-8000) and (TREX 610) 10mm diameter analysis areas respectively. The second standard, labeled KEM K-3, was supplied by Kyushu Electronic Metals Company, a silicon wafer manufacturer in Japan. It was prepared in a similar droplet manner except the Ni level was 0.1 ng, one order of magnitude lower than the GKSS 181 standard.

Procedure:

The samples were all measured once per day for four days. The calibration samples were first measured, then the six samples. Each sample and standard were analyzed in the center 10 mm diameter area for 1000 seconds. The instrument was operated with a tungsten target, rotating anode (monochromator selecting the W L-beta line at 9.67 keV) at 30 kV and 200 mA and with a grazing angle of 0.05 degree. The ambient was vacuum. The GKSS 181 standard was used to quantitate the impurity levels on Samples 0/1, 1/1, 2/1, and 3/1 used in the earlier TXRF round robin, and the KEM K-3 standard was used to quantitate the impurity levels on Samples K/1 and K/2. The data indicate contamination was added during the round robin, both between labs and within labs.

Results

In order to compare the two different standards for consistency between each other, the average TXRF Ni count rate for standard GKSS 181 was ratioed to the average TXRF Ni count rate for standard KEM K-3 for each of the 13 participants. Since the total Ni on GKSS 181 was 1 ng, and the total Ni on KEM K-3 was 0.1 ng, the ratio of Ni count rates

should be 10. The data are shown in Table 2. The average result is 9.74 with a relative one standard deviation (RSD) of 16% (N=13). (Lab E appears to be outside of normal statistical behavior.) Thus, we conclude the two standards were consistent with each other, so that using standard GKSS 181 to quantitate four unknowns and using standard KEM K-3 to quantitate two other unknowns does not introduce a significant error in the estimation of reproducibility in this round robin.

The more significant difficulty in estimating the reproducibility is the addition of contamination during the round robin. This is illustrated by tracking the Fe, Cu and Zn levels on the two standards, using their Ni levels for quantification, as a function of lab test sequence. Figures 1 and 2 show the average (of four days) Fe, Cu and Zn levels versus lab sequence for GKSS 181 and KEM K-3 respectively. We note in Figure 1 that Cu was added early in the round robin and then lost, so there was also the loss of contamination, presumably particulate.

The addition of contamination did not always occur between labs, i.e., due to transport of samples. For example, at lab J on Sample 3/1 the Fe level was reported as a sequence of the four days as follows: 2.52, 2.49, 29.95, and 29.98 $x10^{12}$ atoms/cm^2.

The statistical results of the round robin are shown in Tables 3 through 6 for unscreened data. The distribution of RSD% within labs is shown in Figures 1 and 2. The long tail in the distribution (Figure 1) at higher RSD% is indicative of contamination added within a lab over the four days, not from contamination added between labs. The normal distribution of RSD% in the range of 0 to 18% suggests a within lab RSD% of about 10%, excluding added contamination. The distribution of RSD%'s has a three sigma of 50%. The results were then screened by excluding readings where the within lab RSD% for that element and that sample was above 50%, and by excluding lab E entirely where the Ni reading in Table 2 is out of range and the RSD%'s are all high, and by excluding readings between labs when contamination has been added at high enough levels to suggest a stepwise increase between labs. However, not all of the particulate data were screened out (e.g., Sample 3/1 Fe data in Table 3 at labs K, L and M is particulate and not screened out.) The screened results are summarized in Table 7.

There is also an error in Tables 3 through 6 due to mis-assignment of the two standards. The data for samples 0/1, 1/1, 2/1 and 3/1 should be multiplied by 0.65. The data for samples K/1 and K/2 should be multiplied by 1.3. The tables have not been corrected, because these errors do not alter the conclusions of the round robin. Table 7 includes the corrections. The estimate of precision from these data in Table 7 is an upper limit due to the contamination introduced, and is about 100%.

CONCLUSIONS

The earlier XSA-8000 TXRF gave excellent interlaboratory precisions. However, the method for angle calibration (pressing the wafer against a polished quartz block) was inconsistent with semiconductor cleanliness concepts, and the detection limits are no longer useful for many applications. This resulted in it no longer being commercial.

It is possible for two different groups to make consistent TXRF standards.

In the TREX 610 round robin significant levels of contamination were added, and sometimes subsequently lost, during the round robin, both within and between labs.

The TREX 610 data indicate an upper limit for interlaboratory RSD% of about 100%, due to the time-dependent contamination issue. The average within lab RSD% is about 10%, excluding contamination added.

Subsequent work is needed to demonstrate that interlaboratory correlations can be completed without introducing contamination.

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Table 1. ATOMIKA XSA-8000 TXRF Round Robin Results
(10^{12} atoms/cm^2)

LAB		FE STATISTICS (10^{12} ATOMS/CM^2)			NI STATISTICS (10^{12} ATOMS/CM^2)		
		SAMPLE 2	SAMPLE 3	SAMPLE 4	SAMPLE 2	SAMPLE 3	SAMPLE 4
A							
	AVE	1.70	2.82	26.54	0.40	2.70	19.14
	STD	0.28	0.33	0.65	0.08	0.11	0.31
	RSD%	16.6	11.6	2.5	19.9	4.1	1.6
B							
	AVE	1.39	2.78	27.12	0.29	2.87	19.22
	STD	0.21	0.26	2.02	0.06	0.41	2.12
	RSD%	15.4	9.5	7.4	20.5	14.1	11.1
C							
	AVE	1.45	2.48	26.53	0.30	2.55	18.49
	STD	0.21	0.08	1.25	0.06	0.10	0.94
	RSD%	14.3	3.2	4.7	19.8	3.9	5.1
D							
	AVE	1.58	3.16	32.55	0.41	3.21	22.41
	STD	0.26	0.19	1.4	0.06	0.18	0.83
	RSD%	16.3	6.1	4.4	14.2	5.5	3.7
E							
	AVE	1.57	2.95	29.49	0.28	2.96	20.17
	STD	0.13	0.32	0.85	0.06	0.19	0.66
	RSD%	8.1	10.8	2.9	19.9	6.4	3.3
F							
	AVE	1.43	2.90	BROKE	0.34	2.61	BROKE
	STD	0.09	0.06	BROKE	0.04	0.09	BROKE
	RSD%	6.2	2.0	BROKE	10.8	3.5	BROKE
	GRAND AVE	1.52	2.84	28.45	0.34	2.82	19.89
	STD	0.12	0.22	2.60	0.05	0.25	1.53
	RSD%	7.7	7.9	9.1	15.9	8.7	7.7

LAB		CU STATISTICS (10^{12} ATOMS/CM^2)			ZN STATISTICS (10^{12} ATOMS/CM^2)			
		SAMPLE 2	SAMPLE 3	SAMPLE 4	SAMPLE 0	SAMPLE 2	SAMPLE 3	SAMPLE
A								
	AVE	0.31	1.97	16.66	1.31	0.49	2.52	15.46
	STD	0.07	0.11	0.35	0.08	0.06	0.07	0.26
	RSD%	22.5	5.5	2.1	6.0	11.9	2.68	1.7
B								
	AVE	0.30	1.98	16.36	1.18	0.31	2.48	14.33
	STD	0.10	0.18	1.07	0.05	0.05	0.24	2.02
	RSD%	32.9	9.2	6.5	3.9	17.0	9.7	14.1
C								
	AVE	0.25	1.94	17.04	1.20	0.34	2.34	13.83
	STD	0.05	0.05	0.73	0.02	0.04	0.08	0.75
	RSD%	21.2	2.8	4.3	1.8	12.6	3.6	5.4
D								
	AVE		2.11	20.18	1.31	0.42	2.97	16.72
	STD		0.05	0.65	0.10	0.03	0.19	0.64
	RSD%		2.5	3.2	7.8	8.2	6.4	3.8
E								
	AVE	0.34	1.96	16.60	1.26	0.38	2.66	14.70
	STD	0.08	0.13	0.45	0.08	0.05	0.11	0.42
	RSD%	24.3	6.7	2.7	6.2	13.6	4.1	2.9
F								
	AVE		2.06	BROKE	1.28	0.36	2.75	BROKE
	STD		0.07	BROKE	0.06	0.06	0.08	BROKE
	RSD%		3.5	BROKE	4.6	15.7	2.9	BROKE
	GRAND AVE	0.28	2.00	17.37	1.26	0.38	2.62	15.01
	STD	0.05	0.06	1.59	0.06	0.06	0.22	1.13
	RSD%	18.1	3.2	9.2	4.4	16.8	8.5	7.5

Table 2. Ratio of Ni Count Rate for Two Standards

Lab	(Ni cps of GKSS 181) / (Ni cps of KEM K-3)
A	10.67
B	09.83
C	11.02
D	11.75
E	05.81
F	10.84
G	10.36
H	10.52
I	10.00
J	10.88
K	08.92
L	07.74
M	08.31
AVE	09.74
STD	01.58
RSD	16%

Table 3. TECHNOS TREX 610 TXRF Round Robin Results: Fe
(10^{12} atoms/cm^2)

LAB		Sample0/1	Sample1/1	Sample2/1	Sample3/1	SampleK/1	SampleK/2
A	AVE	0.098	1.470	0.411	0.873		
	STD	0.027	0.378	0.042	0.105		
B	AVE	0.622	0.903	1.828	3.498	0.110	0.153
	STD	0.044	0.207	0.120	0.299	0.031	0.044
C	AVE	0.635	0.901	1.475	3.138	0.461	0.147
	STD	0.163	0.109	0.258	0.225	0.609	0.019
D	AVE	0.698	1.211	1.110	1.154	0.709	0.075
	STD	0.064	0.603	0.155	0.134	0.417	0.005
E	AVE	1.630	2.955	3.173	5.876	0.526	0.593
	STD	0.834	1.268	1.088	1.626	0.200	0.195
F	AVE	0.613	1.600	0.870	0.840	0.035	0.069
	STD	0.026	0.141	0.037	0.096	0.003	0.018
G	AVE	1.104	1.801	1.456	2.321	0.256	0.654
	STD	0.214	0.138	0.114	0.144	0.036	0.082
H	AVE	1.345	2.335	1.759	2.413	0.477	1.340
	STD	0.089	0.107	0.232	0.172	0.012	0.230
I	AVE	0.633	1.650	0.768	1.398	0.295	0.870
	STD	0.099	0.129	0.135	0.276	0.031	0.121
J	AVE	1.134	2.558	1.534	16.236	0.568	1.621
	STD	0.033	0.566	0.083	15.855	0.058	0.074
K	AVE	1.149	2.220	1.589	40.112	0.519	1.351
	STD	0.074	0.077	0.088	2.138	0.018	0.087
L	AVE	3.950	6.180	5.080	38.600	1.350	3.550
	STD	0.379	0.263	0.189	3.660	0.129	0.173
M	AVE	2.227	5.348	3.170	42.590	0.782	2.231
	STD	0.088	0.119	0.068	0.744	0.021	0.041
GRAND AVE		1.218	2.395	1.863	12.235	0.507	1.055
	STD	0.984	1.625	1.263	16.591	0.347	1.048

Table 4. TECHNOS TREX 610 TXRF Round Robin Results: Ni
(10^{12} atoms/cm^2)

LAB		Sample0/1	Sample1/1	Sample2/1	Sample3/1	SampleK/1	SampleK/2
A	AVE		0.197	0.166	1.260		0.089
	STD		0.050	0.012	0.185		0.012
B	AVE	0.234	0.280	0.747	4.905	0.149	0.557
	STD	0.097	0.091	0.157	0.439	0.034	0.452
C	AVE	0.204	0.350	0.627	3.655	0.136	0.200
	STD	0.019	0.046	0.073	0.414	0.026	0.012
D	AVE	0.095	0.236	0.202	1.526	0.029	0.098
	STD	0.008	0.096	0.046	0.134	0.016	0.012
E	AVE	0.856	1.395	1.613	6.758	0.666	1.022
	STD	0.678	0.840	0.683	1.726	0.337	0.413
F	AVE	0.071	0.323	0.180	1.123	0.033	0.113
	STD	0.016	0.026	0.082	0.153	0.006	0.010
G	AVE	0.241	0.458	0.420	2.485	0.135	0.228
	STD	0.041	0.033	0.032	0.207	0.010	0.025
H	AVE	0.154	0.362	0.236	1.300	0.041	0.154
	STD	0.023	0.008	0.063	0.141	0.006	0.010
I	AVE	0.099	0.308	0.097	1.118	0.057	0.198
	STD	0.023	0.026	0.037	0.236	0.016	0.021
J	AVE	0.133	0.217	0.284	3.185	0.563	0.206
	STD	0.016	0.043	0.039	2.087	0.018	0.029
K	AVE	0.168	0.261	0.341	7.086	0.071	0.243
	STD	0.015	0.030	0.054	0.437	0.016	0.016
L	AVE	0.660	0.678	0.950	7.750	0.185	0.530
	STD	0.057	0.061	0.071	0.311	0.035	0.032
M	AVE	0.539	0.614	0.691	7.564	0.139	0.413
	STD	0.056	0.043	0.025	0.081	0.022	0.042
GRAND	AVE	0.288	0.437	0.504	3.824	0.141	0.312
	STD	0.255	0.323	0.425	2.660	0.173	0.263

Table 5. TECHNOS TREX 610 TXRF Round Robin Results: Cu
(10^{12} atoms/cm^2)

LAB		Sample0/1	Sample1/1	Sample2/1	Sample3/1	SampleK/1	SampleK/2
A	AVE	0.147	0.223	0.088	1.163		
	STD	0.054	0.062	0.016	0.124		
B	AVE	1.868	0.371	0.546	4.249	0.302	1.707
	STD	0.295	0.109	0.122	0.343	0.056	1.702
C	AVE	0.225	0.246	0.402	2.836	0.216	0.168
	STD	0.040	0.074	0.065	0.318	0.025	0.040
D	AVE	0.157	0.169	0.183	1.280	0.136	0.081
	STD	0.038	0.024	0.050	0.102	0.048	0.020
E	AVE	0.765	0.633	0.965	5.205	0.442	0.351
	STD	0.439	0.372	0.345	1.578	0.113	0.141
F	AVE	0.097	0.228	0.200	0.875	0.140	0.100
	STD	0.017	0.017	0.026	0.093	0.018	0.018
G	AVE	0.343	0.379	0.470	1.963	0.419	0.295
	STD	0.054	0.039	0.039	0.188	0.041	0.035
H	AVE	0.220	0.338	0.336	1.041	0.168	0.149
	STD	0.029	0.042	0.116	0.150	0.021	0.019
I	AVE	0.162	0.380	0.195	1.023	0.300	0.190
	STD	0.044	0.022	0.076	0.227	0.029	0.016
J	AVE	0.181	0.331	0.468	1.150	0.278	0.187
	STD	0.039	0.036	0.052	0.096	0.018	0.019
K	AVE	0.305	0.412	0.639	2.093	0.315	0.248
	STD	0.066	0.030	0.075	0.176	0.096	0.013
L	AVE	1.780	1.350	1.430	3.130	0.570	0.495
	STD	0.189	0.058	0.096	0.287	0.139	0.041
M	AVE	0.566	0.578	0.747	2.403	0.231	0.322
	STD	0.058	0.034	0.015	0.016	0.006	0.011
GRAND AVE		0.471	0.434	0.513	2.185	0.293	0.358
	STD	0.614	0.306	0.371	1.357	0.131	0.441

Table 6. TECHNOS TREX 610 TXRF Round Robin Results: Zn
(10^{12} atoms/cm^2)

LAB		Sample0/1	Sample1/1	Sample2/1	Sample3/1	SampleK/1	SampleK/2
A	AVE	0.487	0.748	0.490	3.065		
	STD	0.095	0.155	0.033	0.390		
B	AVE	5.030	4.111	2.748	12.150	0.114	0.224
	STD	0.678	0.119	0.351	0.870	0.018	0.168
C	AVE	1.784	0.700	1.417	7.033	0.135	0.062
	STD	0.194	0.095	0.210	0.755	0.043	0.023
D	AVE	1.042	0.510	0.712	3.391	0.096	0.032
	STD	0.134	0.030	0.148	0.328	0.024	0.012
E	AVE	5.435	1.934	3.251	12.082	0.545	0.659
	STD	2.542	0.897	1.090	3.053	0.201	0.196
F	AVE	0.720	0.643	0.665	2.830	0.060	0.077
	STD	0.105	0.031	0.060	0.386	0.010	0.015
G	AVE	2.563	0.839	1.231	5.032	0.180	0.323
	STD	0.362	0.042	0.080	0.439	0.011	0.023
H	AVE	0.895	0.648	0.821	2.823	0.086	0.302
	STD	0.124	0.054	0.189	0.306	0.007	0.035
I	AVE	0.728	0.605	0.410	2.575	0.130	0.350
	STD	0.243	0.042	0.118	0.519	0.022	0.037
J	AVE	0.540	0.451	0.807	2.971	0.098	0.348
	STD	0.058	0.060	0.042	0.320	0.015	0.018
K	AVE	0.976	0.531	1.135	3.991	0.109	0.498
	STD	0.210	0.047	0.096	0.184	0.017	0.024
L	AVE	3.130	1.550	3.500	7.130	0.318	1.330
	STD	0.435	0.577	0.271	0.299	0.075	0.126
M	AVE	2.490	1.289	2.449	5.536	0.608	2.916
	STD	0.359	0.286	0.254	0.133	0.122	1.052
GRAND AVE		1.986	1.120	1.505	5.431	0.207	0.593
	STD	1.676	1.004	1.088	3.349	0.185	0.811

Table 7. Summary Statistics of TREX 610 Results

Sample	0/1	1/1	2/1	3/1	K/1	K/2
Fe Statistics (10^{12} atoms/cm^2)						
Grand Ave	0.836	1.56	1.21	7.95	0.660	1.37
Std	0.580	1.01	0.789	10.4	0.432	1.30
RSD%	69	65	65	130	65	95
Ni Statistics (10^{12} atoms/cm^2)						
Grand Ave	0.187	0.284	0.328	2.49	0.239	0.405
Std	0.158	0.202	0.265	1.66	0.260	0.329
RSD%	85	71	81	67	109	81
Cu Statistics (10^{12} atoms/cm^2)						
Grand Ave	0.341	0.282	0.333	1.42	0.381	0.465
Std	0.387	0.191	0.232	0.848	0.163	0.549
RSD%	114	68	70	60	43	118
Zn Statistics (10^{12} atoms/cm^2)						
Grand Ave	1.29	0.728	0.982	3.53	0.269	0.771
Std	1.05	0.627	0.679	2.09	0.231	1.01
RSD%	81	86	69	59	86	131

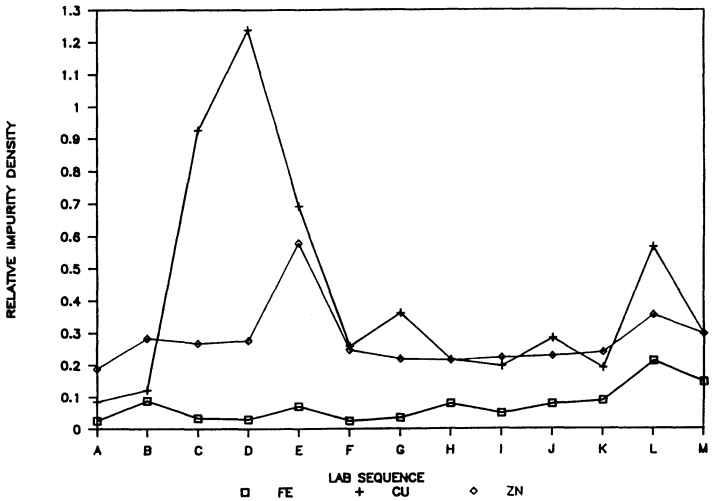

Fig 1. Impurity versus lab sequence on GKSS 181 (TREX 610 Round Robin)

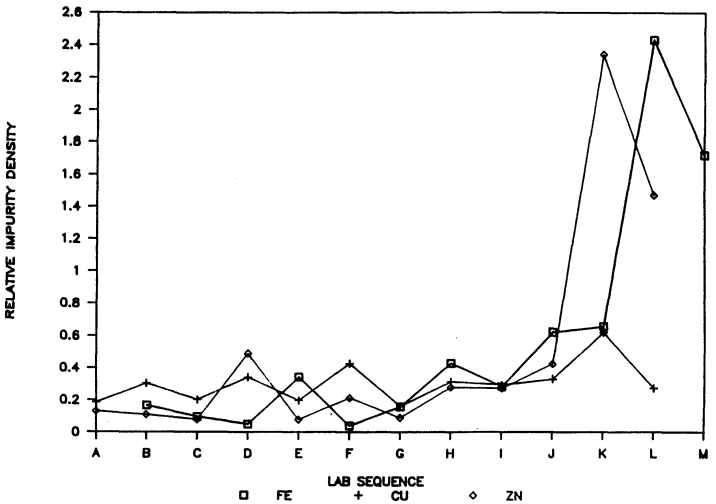

Fig. 2 Impurity versus lab sequence on KEM K-3 (TREX 610 Round Robin)

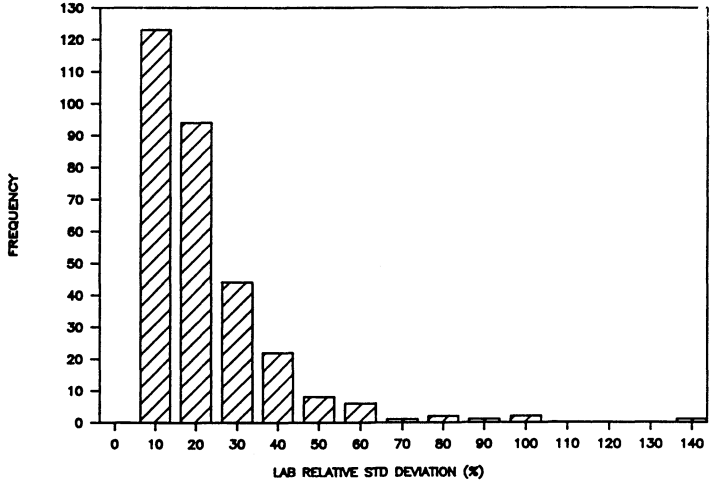

Fig. 3. Distribution of Within Lab RSD%: 0-140% (TREX 610 Round Robin)

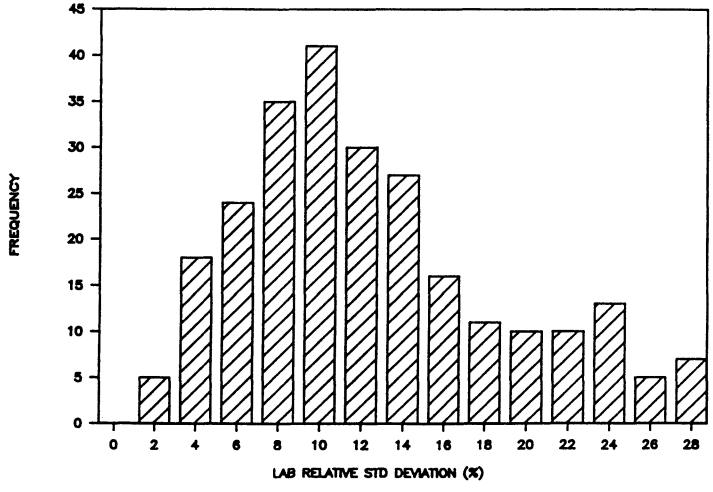

Fig. 4. Distribution of Within Lab RSD%: 0-28% (TREX 610 Round Robin)

TRACE ANALYSIS OF INORGANIC CONTAMINATION ON SI-WAFER SURFACE BY ION CHROMATOGRAPHY

D. Rathmann
WACKER-CHEMITRONIC GmbH
D-8263 Burghausen / Germany
PO-Box 1140

Although device yield and reliability provide the ultimate answer, process engineers must determine a suitable grade of acceptance for wafer cleanliness already before processing.
To check Si-wafer surfaces for alkali metals, alkaline earth metals and various anions we have developed the novel VPD-IC method.
The method was based on the vapor phase decomposition (VPD) of the native oxide by HF vapor and a subsequent scanning on the surface with a water droplet. The droplet was then analysed by means of ion chromatography (IC) equipped with a conductivity cell detector of high sensitivity.
Beside the control of wafer cleanliness, the new method was also applied to investigate the environmental influence upon Si-wafer surfaces.

Introduction:

Recently, both the variety of elements and their surface concentration have been proved to affect device reliability and yield (1-4). Therefore, cleanliness control must be extended beyond transient metals to alkali and alkaline earth cations and anions.

To achieve these goals we combined a modified vapor phase decomposition method (VPD) with ion chromatography (IC), providing a fast, routine multielement analysis technique for surface cleanliness control down to 1E10 ion*cm-2.
The performance of this novel technique was checked by VPD-AAS measurement on authentic Si-wafer samples.

Equipment:

For VPD preparation a PVDF chamber with PTFE wafer trays was used. The droplet of ultrapure water was handled by

a special micropipette also made of PTFE. Analysis was carried out with a Dionex ion chromatograph series 4000 equipped with a 50 µL injection loop and a CDM2 conductivity detector of high sensitivity. For cation separation standard Fast Cation I and II columns were used. Anion separation was done with a AS4a column. All chromatograpic equipment made by Dionex Corporation, Sunnyvale, California.
A clean bench of class 10 was used for the VPD preparation and the subsequent manual scanning.

Measurement Technique:

In order to dissolve the surface contaminations in the native oxide layer, the Si-wafer sample was placed into the PVDF chamber to react with HF vapor at room temperature (see Fig. 1). After the decomposition of the native oxide coverage the frontside surface was scanned by ultrapure water, collecting the soluble surface contaminants (see Fig. 2). A special micropipette was used to transfer the droplet that was then directly injected from the micropipette into the ion chromatograph. See Figure 3 for the prinicple of ion chromatography analysis. Example chromatograms of contaminated wafers are shown in Figure 4 and 5.

A second scan using another droplet of ultrapure water was applied to check the blank values. This second droplet showed values characteristic of the ultrapure water.

For identification and quantification the ion chromatograph was calibrated by using multi-element standard solutions from conditioned PFA bottles. As multi level calibration curves showed linearity for more than 2 magnitudes, a 4-point calibration was found to be sufficient (see Fig. 6). The ions calibrated were either Na^+, NH_4^+, K^+ or Ca^{2+}, Mg^{2+} or Cl^-, NO_3^-, PO_4^{3-} and SO_4^{2-}. Authentic samples of contaminated wafers were also analysed to check the calibration of alkali metals.
With the limit of quantification we have reached the ultratrace level down to 1E10 ion*cm-2. At this quantification limit the variation was found to be in the range of 5 to 10 percent. The measurement is comparable to the well established VPD-AAS analysis.

The recovery rates of the method were also tested by authentically contaminated "ultraclean wafers" using 1 ng Na (see Fig. 7 and 8) and were found to be higher than 98% (5).

Cross checking by means of VPD-TRXFA and by the method of VPD-AAS (6) showed adequate correlations (Fig. 9). A cross check for alkaline earth metals with TRXFA is under development.

Summary:

This novel VPD-IC technique became daily routine in our analytical laboratory for controlling frontside cleanliness. It provides high recovery rates as well as high accuracy down to the ultratrace range of 1E10 ion*cm-2. Monitoring of environmental influence has also been viable.

Now we are focussing on novel analytical reaction media that provide common access to a greater variety of inorganic and ionic surface contaminations by means of ion chromatography. Analysis of backside cleanliness with VPD-preparation will also be a hotly pursued goal.

ACKNOWLEDGEMENTS

The author wants to thank L. Fabry for helpful discussions and his critical comments on this paper. Cross check measurements done by L. Kotz and S. Pahlke were also thankfully acknowledged.

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Figure 1: Principle of VPD-Preparation

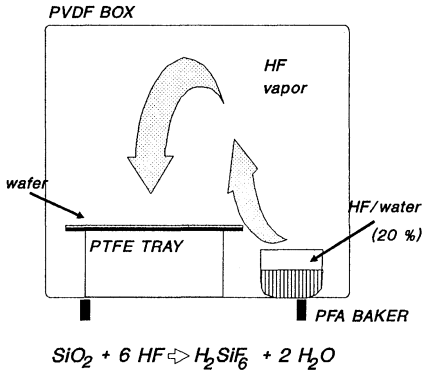


Figure 2: Surface Scan
after VPD Preparation

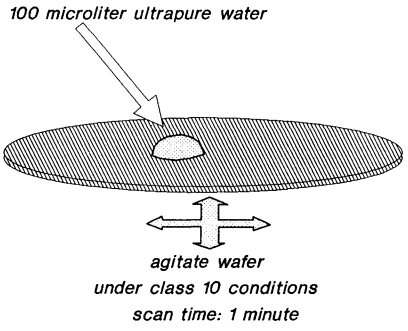


Figure 3: Principle of Ion Chromatography(IC)
Conductivity Detection

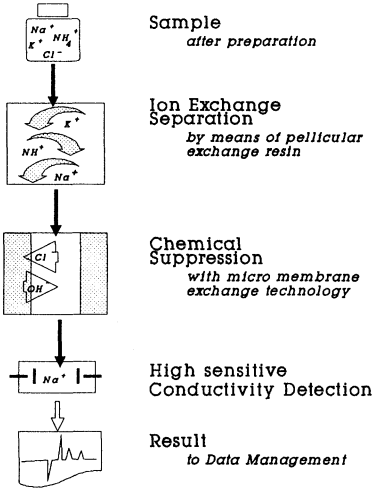
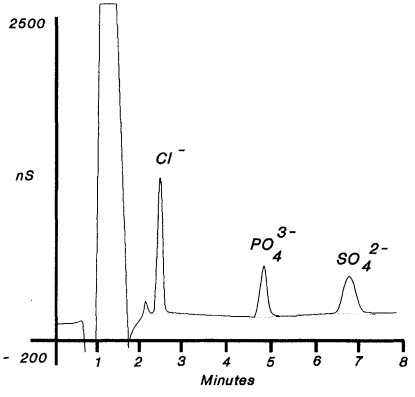
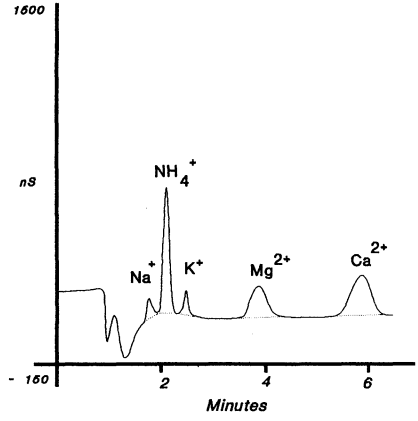


Figure 4: Chromatogram of Anions
after VPD-Preparation



Eluent NaOH / Na2B4O7

Figure 5: Chromatogram of Cations after VPD-Preparation



Eluent HCl /DAP

Figure 6: Calibration Curve VPD-IC Alkali Metals & Chloride

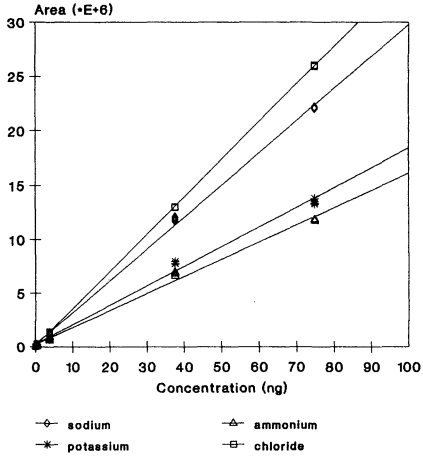


Figure 7: Recovery Rate of Sodium on authentically contaminated wafer surface

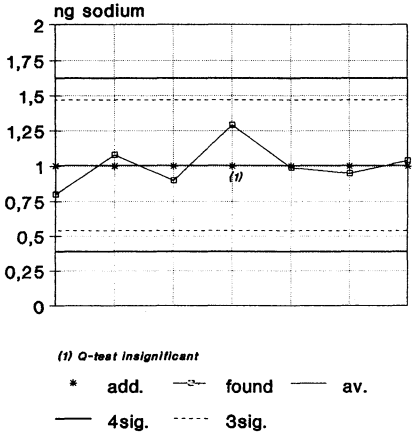


Figure 8: Recovery Rate Multiple Analysis

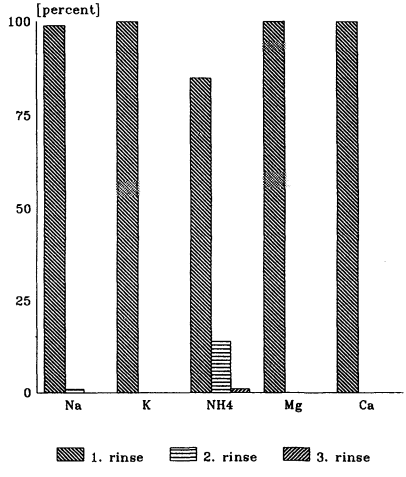
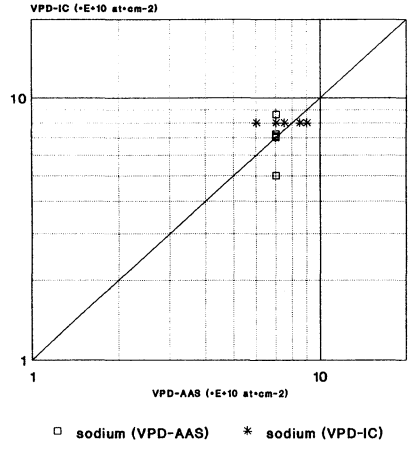


Figure 9: Cross Check Measurement
VPD-IC versus VPD-AAS
single values, sodium on si-wafers



DETERMINATION OF INORGANIC TRACE CONTAMINATION ON THERMOPLASTIC CARRIER SURFACE BY ION CHROMATOGRAPHY

D. Rathmann, L. Fabry
WACKER-CHEMITRONIC GmbH
D-8263 Burghausen / Germany
PO-Box 1140

Processing semiconductor silicon involve thermoplastic carriers and storage boxes. They contact the wafers and may liberate or transfer detrimental contamination like alkali metals or anions onto the wafer surfaces.
Recently, we have developed a novel routine analytical method to control carrier surface cleanliness by means of ion chromatography (IC) in the low range of 50 to 100 pg/cm2 of carrier surface. The IC-data on alkali metals were verified by AAS and ICP-MS measurements. Interactions between carrier contaminations and wafer surfaces were also investigated.

Introduction:

Surface and volatile bulk contaminations of storage boxes and shipping carriers can be detrimental to Si-wafer surfaces (1-4). For the optimization and the effective process control of carrier cleaning all the potential inorganic contaminants must be monitored.

Pursuing this goal we have developed a routine multielement method based on the aqueous solution of the ionic surface contaminants followed by ion chromatography analysis of alkali metals and anions. Carrier-wafer interactions and transfer reactions from bulk of the carrier to its surface could also be traced by the new analytical technique.

Equipment:

For sample preparation, that was done in a clean bench of class 10, a special spray chamber made of PTFE and plexiglass was used. The subsequent ion chromatography analysis takes place at an attached grey room. Analysis was performed at a Dionex 4000 ion chromatograph equipped with

standard enriching and separation columns and a CDM2 conductivity detector of high sensitivity.
All chromatographic equipment made by Dionex Corporation, Sunnyvale, California.

Measuring Technique:

The ionic contaminations of interest showed high solubility in water.
Therefore, the slots of the carrier under investigation were rinsed under a defined volume of spraying ultrapure water in the spray chamber. Ionic surface impurities such as Na^+, K^+, NH_4^+, and Cl^-, NO_2^-, Br^-, NO_3^-, PO_4^{3-}, SO_4^{2-} were solved at room temperature and collected as a liquid sample in a PFA bottle (see Fig. 1).

After completing the rinsing step, the impurities solved in the liquid sample were enriched on an on-line trace concentrator column (Trace Anion Column TAC and Trace Cation Column TCC). Then the enriched contaminations were injected automatically into the ion chromatograph to be separated and analyzed by a conductivity cell of high sensitivity as showed in Fig. 2.
The preparation blanks lay characteristically at the contamination level of that of the ultrapure water.

Identification and quantification of the impurities were done by calibration using liquid standard solutions (see Fig. 3, 4 and 5). Results were calculated by subtracting the preparation blank values from the sample values. Surface contamination was then calculated by the following equation:

$$C_{(surface)} = C_{(sample)} * V_{(water\ spray)} / A_{(rinsed\ surface)}$$

Basically, the limit of quantification (LOQ) was found to be in the range of 50 to 100 pg/cm2, depending on the size of the analyzed carrier and the rinsed surface.

Results:

Different types of uncleaned carriers (PP, HDPE or PBT) showed a variety of surface contaminations such as Na^+, K^+, NH_4^+, Cl^-, NO_2^-, NO_3^- and SO_4^{2-} in the range of 1 to more than 10 ng/cm2 (Fig. 6). Repeated rinsing steps proved the existence of a reservoir of NH_4^+ in the bulk of the carrier, that could recontaminate the plastic surface of the carrier under certain circumstances. This NH_4^+ contamination was also

detected by our novel VPD-IC method on Si-wafers stored in plastic carriers (5). Migration is forced by wet, acid surface. Under these conditions also an increasing amount of the other elements, detected after the first rinsing step, was observed (6,7).
However, aqueous cleaning (Fig. 7) and dry storage (Fig. 8 and 9) has proved to remove virtually all detectable contaminations.

Summary:

This new surface sensitive technique provides routine multielement measurements for control of carrier surface cleanliness in our analytical laboratory. Reproducibility proved to lie in the range of 5 to 10 percent variation at the trace level of the limit of detection.
The method can be used as a routine tool for optimizing carrier cleaning processes as well as for incoming or outgoing inspection.
Interactions between carrier and Si-wafer surfaces can also be a subject of investigation.

Acid reaction media, that will provide an acess to transient metal contaminations, are under investigation.

ACKNOWLEDGEMENTS:

The authors are indebted to H.F. Haas for the helpful discussions and to E. Heindl for the construction of the spray chamber.

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Figure 1: Carrier Surface Analysis
Principle of Spray Chamber

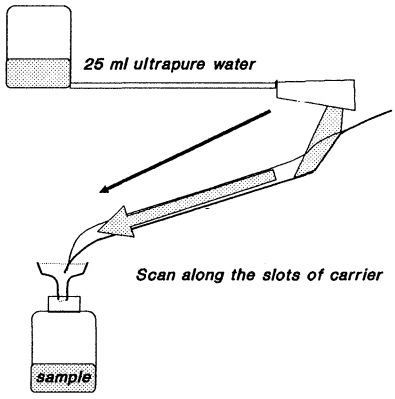


Figure 2: Principle of Ion Chromatography(IC)
Conductivity Detection

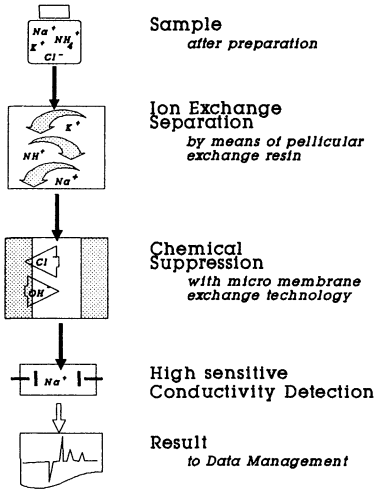
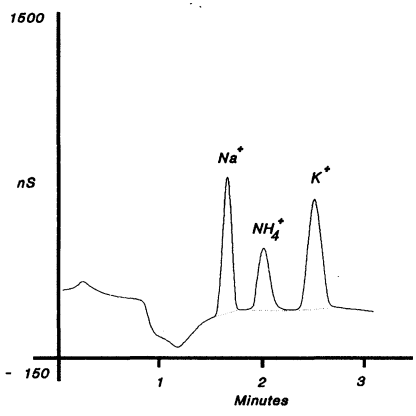
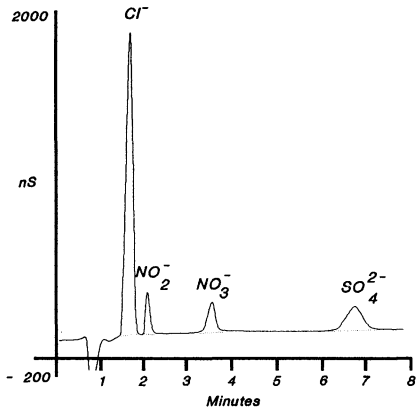


Figure 3: Chromatogram of Cations



Eluent HCl / DAP

Figure 4: Chromatogram of Anions



Eluent Na2CO3 / NaHCO3

Figure 5: Calibration Curve IC
Monitor Elements

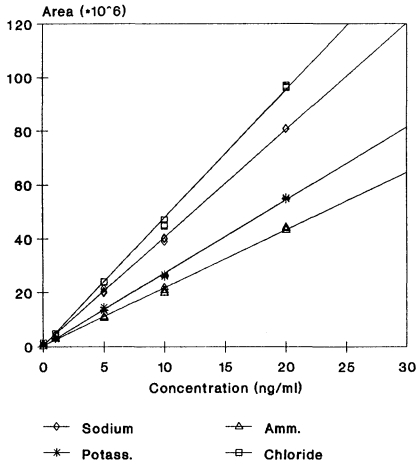


Figure 6: Trend Chart Uncleaned Carriers
Carrier Type A (PE)

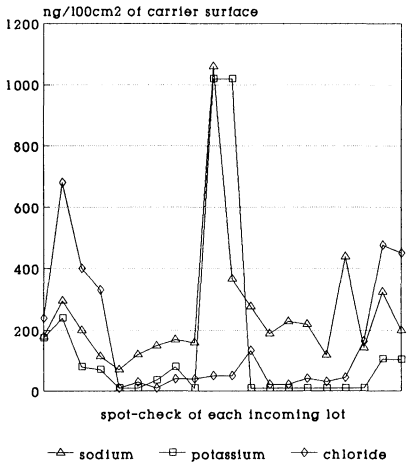


Figure 7: Trend Chart Cleaned Carriers
Carrier Type A (PE)

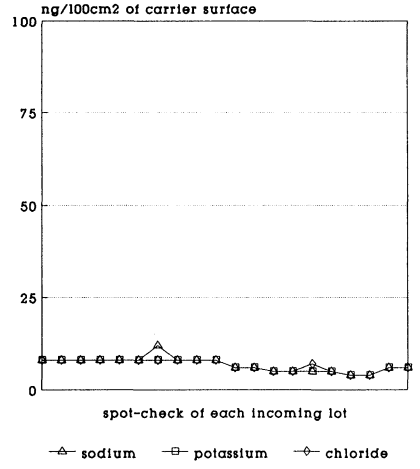


Figure 8: Migration of Sodium
from Bulk to Carrier Surface
under simulated storage conditions
48 hours at 40°C, 2 month at room temperatur

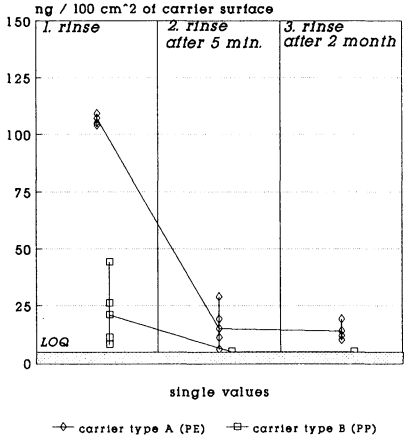
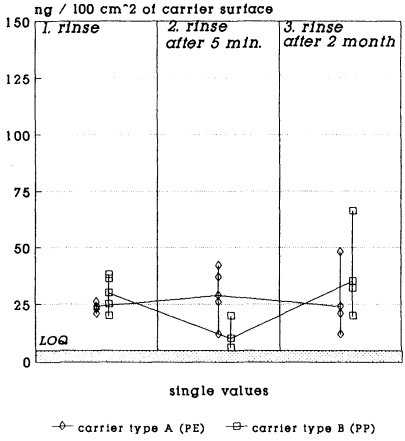


Figure 9: Migration of Ammonium from Bulk to Carrier Surface under simulated storage conditions

48 hours at 40°C, 2 month at room temperatur



TXRF MEASUREMENT OF SUBSTRATE BACKSIDE CONTAMINATION

R. S. Hockett
Charles Evans & Associates
Redwood City, CA 94063

A TECHNOS TREX 610 TXRF instrument is used for the direct measurement of metal contamination on the backside of silicon substrates, where contamination can come from cleaning or from processing equipment, such as transport equipment or wafer chucks.

INTRODUCTION

The focus of most analytical characterization of cleaning processes has been the frontside of polished substrates. This is partly because this surface is close to the active device region for IC processes, and partly because the backside of the substrate is more difficult to characterize analytically. Unfortunately, heavy metals on the substrate backside may easily diffuse to the frontside under even low temperature processing, and depending upon the thermal process ambient, heavy metals on the backside of one substrate may be able to desorb and transfer to the frontside of the neighboring substrate in the IC boat.

The most popular analytical techniques for metal contamination on the frontside of silicon substrates have been Secondary Ion Mass Spectrometry (SIMS) (1), Vapor Phase Decomposition followed by Atomic Absorption Spectroscopy (VPD/AAS) (2,3), and Total reflection X-Ray Fluorescence (TXRF) (4). SIMS has not been easily quantified for the frontside measurement, and the roughness of the backside makes this even more difficult. VPD/AAS can in principle be used for the backside measurement by simply inverting the wafer when using the horizontal VPD approach (3), however, the collection efficiency of the metals using the water droplet has not been demonstrated for a rough surface. TXRF has had difficulty in performing the backside measurement, because of the difficulty in establishing an angle calibration on a rough surface. This paper presents the successful use of TXRF to the backside measurement of metal contamination.

TXRF

TXRF is a non-destructive analytical technique which measures heavy metal contamination on the polished surface of silicon substrates. In TXRF x-rays normally impinge the surface of the sample at grazing angle, below the angle (0.19 degree) for total external reflection, and thereby excite only the top few monolayers with the evanescent wave. Emitted fluorescence x-rays are then detected by a Si(Li) energy dispersive spectrometer (EDS) which makes the technique a multi-element

measurement. The analysis area is 10 mm in diameter, and the analysis depth is approximately 3 nm for glancing angles below the critical angle. Detection limits are on the order of 10^{10} atoms/cm^2 for polished surfaces using the TECHNOS TREX 610 with a 9 kW rotating anode, tungsten target, monochromator (selects the W L-beta line), and vacuum (5). A schematic of the instrument in shown in Figure 1. Substrate mapping of multi-element contamination is also possible using the mechanical automation of the TREX 610. In addition, by varying the glancing angle it is possible to qualitatively determine if the contamination is on the surface or immediately below the surface (4, 6).

FRONTSIDE SUBSTRATE CHARACTERIZATION BY TXRF

Various metal contaminants have been observed by TXRF as a function of the cleaning chemistry of the silicon substrate. Eichinger, et al, (4) showed that copper in buffered HF easily plated onto the silicon wafer surface. Penka and Hub (7) showed iron in the RCA SC1 ($NH_4OH:H_2O_2:H_2O$) bath easily plated onto the silicon wafer surface. Hockett and Katz (8) showed that commercial silicon wafers in 1987-88 could have levels of Fe, Cu, and Zn on the order of 10^{12} atoms/cm^2. More recently the surface of commercial silicon wafers are much cleaner, on the order of 10^{10} atoms/cm^2.

A typical TXRF spectrum for the frontside (polished) of a commercial silicon wafer is shown in Figure 2. Here we see a plot of fluorescence intensity I in counts per second (cps) versus fluorescence energy in keV from 0 to 10 keV. At 1.74 keV there is a large Si peak from the silicon native oxide and substrate, and at 9.7 keV there is another large peak which is the diffracted W L-beta peak. In between we see from left to right peaks for S, Fe, Ni, Cu and Zn. In the table above the plot we see a list of the elements, the energy of the element peak, the net integrated intensity in cps, and the metal areal density of the elements in units of 10^{10} atoms/cm^2. The transition metals are in the mid to high 10^{10} atoms/cm^2. The sulfur is much higher in areal density and is expected to come from atmospheric SO_4^{-2} contamination in clean rooms (9). This spectrum was taken at 30 kV, 200 mA, in vacuum, for 1000 s. The Fe level for this commercial wafer is consistent with results claimed by Zoth and Bergholz using other techniques (10). Piranha bath cleaning leaves even higher levels of sulfur on wafers, depending upon the water rinse, and this sulfur is expected to be chemically bound to the surface in a different manner from atmospheric sulfur.

BACKSIDE SUBSTRATE CHARACTERIZATION BY TXRF

In normal TXRF x-rays impinge the surface of a highly polished or flat sample at grazing angle, below the angle for total external reflection, and thereby excite only the top few monolayers with the evanescent wave. In the analysis of the wafer backside the x-rays impinge the surface at many different angles, because of the backside roughness. In most cases the angle is above the critical angle so that total external reflection does not occur, and the measurement is more

like an XRF analysis with varying penetration depths across the 10 mm diameter analysis area. This application has been difficult in the past for TXRF instruments which use the silicon matrix signal for its angle calibration or which use a laser signal reflected from the sample surface for the frontside reference in the angle calibration. The TREX 610 can be used for this application, because its angle calibration does not use either of these approaches. The TREX 610 determines the zero angle position of the large area surface by detecting the W x-ray intensity with the scintillation counter (shown in Figure 1) in a non-reflecting mode. Then the low angle is set using stepper motors on a robot which tilts the sample. In this case the angle is defined with respect to an imaginary surface formed by the top of the rough peaks of the silicon backside.

It is now possible to qualitatively compare the contamination levels on different sample backsides by maintaining the same glancing angle among the samples. An approximate quantification can be also accomplished by using the high angle signal of a frontside reference sample. However, because the total surface area of the backside is unknown (due to its roughness), the areal density will be inaccurate.

To illustrate the different effects for frontside versus backside TXRF measurements, we will discuss the TREX 610 TXRF signal versus angle (i.e., anglescan) for copper contamination on the polished frontside (Figure 3a) and etched backside (Figure 3b) of a silicon wafer cleaned in a Cu-contaminated buffered HF bath which is known to effectively plate out the Cu (4). The anglescan of the frontside follows the expected shape for contamination plated to the surface of the silicon wafer (4, 6). The rise in the Cu signal with angle for angles below the critical angle of 0.19 degree is due to the increase in electric field strength at the surface as the glancing angle is increased. The drop in the Cu signal with angle for angles below the critical angle is due to both a decrease in electric field strength and the fact the surface Cu is only being excited by the transmitted wave for angles above the critical angle. The drop in Cu signal by 2x between the highest Cu signal and the Cu signal at about 0.31 degree is due to this latter effect (4). The shape of the Si signal versus angle is also as predicted for a polished surface (4).

Figure 3b shows the TREX 610 TXRF anglescan for copper contamination on the acid etched backside of the same wafer as for Figure 3a. In this case, the anglescan of the backside is quite different both for the Si matrix signal, as well as for the Cu signal. The Cu signal increases almost linearly with increasing glancing angle. The reason proposed for this difference is the analyte area is linearly increasing as the glancing angle is increased, while the x-rays which do excite the analyte volume are always penetrating rather than total reflecting. We note that because the Si matrix signal increases linearly with angle, there is no inflection point in the Si curve (as there is for the frontside, Fig. 3a) to define a unique angle for determining an angle

calibration using the Si matrix signal. This is why an angle calibration using the Si matrix signal for wafer backside is not possible.

To illustrate the anglescan behavior for particles on the backside we note Figure 4 shows the anglescan of what is suspected to be a stainless steel particle on the backside of an etched silicon wafer. The anglescan of the Fe, Ni and Cr is not only different in shape from surface plated Cu (Figure 3b), but also follows a shape different than expected for particles on the frontside of polished wafers (6).

The stability of the backside angle calibration can be inferred by Figure 5 which is a TREX 610 partial map of the backside of a 150 mm silicon wafer cleaned in a Cu-contaminated buffered HF bath. We notice the silicon and copper count rates are fairly constant with position, which we would expect if the glancing angle were kept constant from point to point on the backside. We also note the presence of some heterogeneous contamination, including Fe, Ni and Cr from stainless steel tweezers which were used to hold the wafer edge.

As an example of backside contamination from IC processing, Figure 6 shows spectra taken from the backside of a silicon wafer which went through an IC thermal process step. The quantification is not expected to be accurate, but the relative comparison is expected to be valid. We note the contamination is fairly uniform. The CONTROL measurement was taken from a non-processed and different wafer.

CONCLUSION

In conclusion the TECHNOS TREX 610 TXRF instrument can be used for the direct measurement of metal contamination on the backside of silicon substrates, where contamination can come from cleaning or from processing equipment, such as transport equipment or wafer chucks. With the recent reduction in surface metals on the polished surface of the silicon wafers in the last few years, the major source of surface metals may now lie on the wafer backsides, either from cleaning for from IC processing. The TXRF technique can be useful for the identification and reduction of this contamination.

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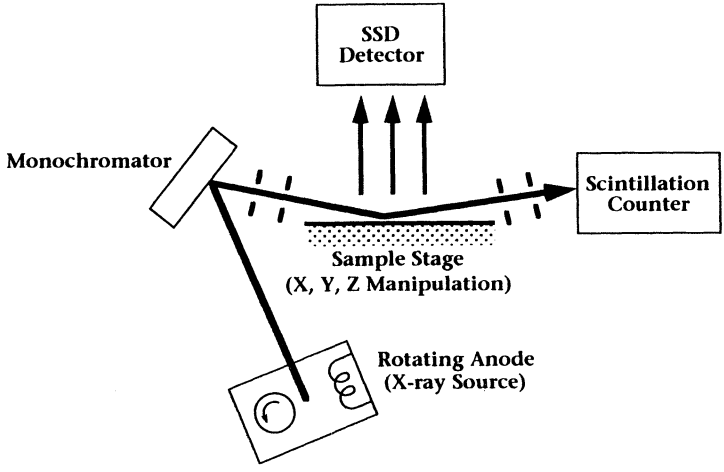

Fig. 1 Schematic of the TECHNOS TREX 610 TXRF instrument.

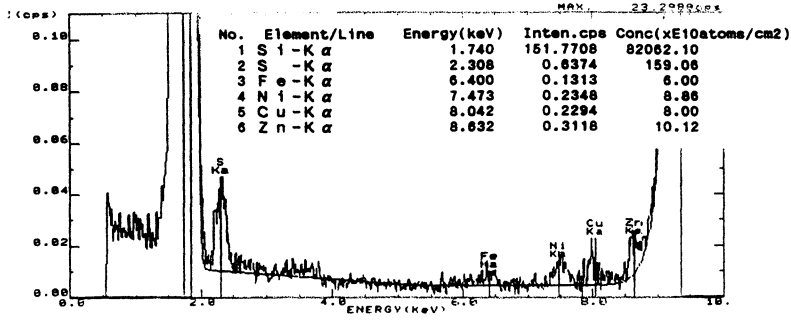

Fig. 2 TREX 610 TXRF spectra of the polished side of a typical commercial silicon wafer in 1991.

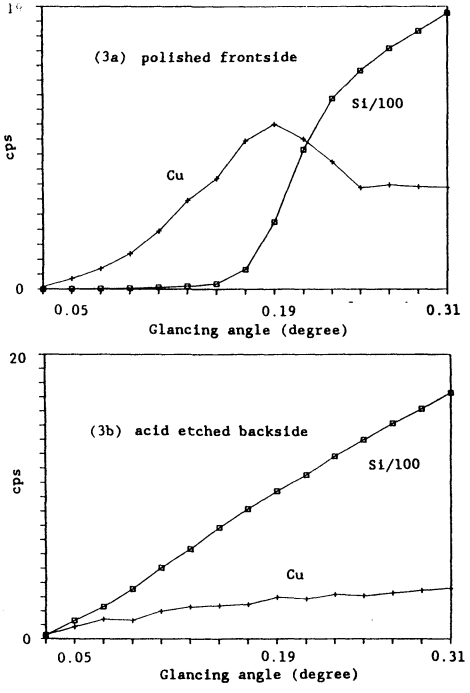

Fig. 3 TREX 610 TXRF anglescan of Cu contamination on a silicon wafer; (3a) polished frontside; (3b) acid etched backside.

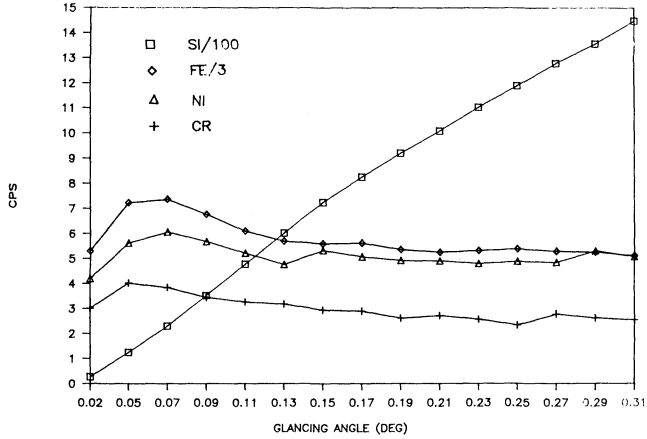

Fig. 4 TREX 610 TXRF anglescan of Fe, Ni and Cr for a stainless steel particle on the backside of an etched silicon wafer.

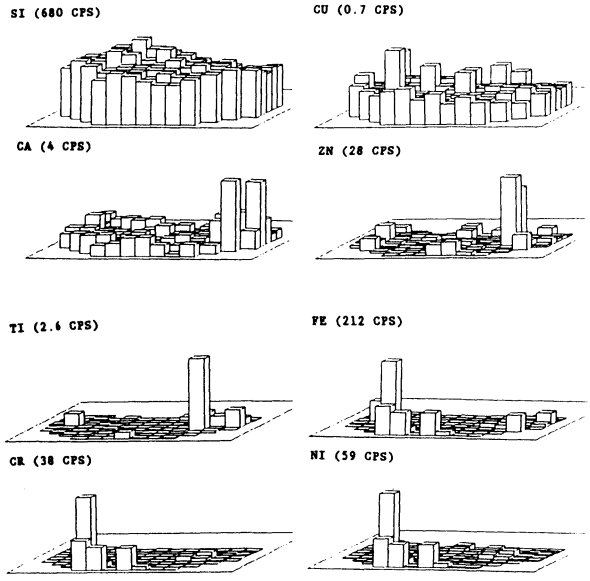

Fig. 5 TREX 610 TXRF multi-element partial map of the backside of a contaminated 150 mm silicon wafer.

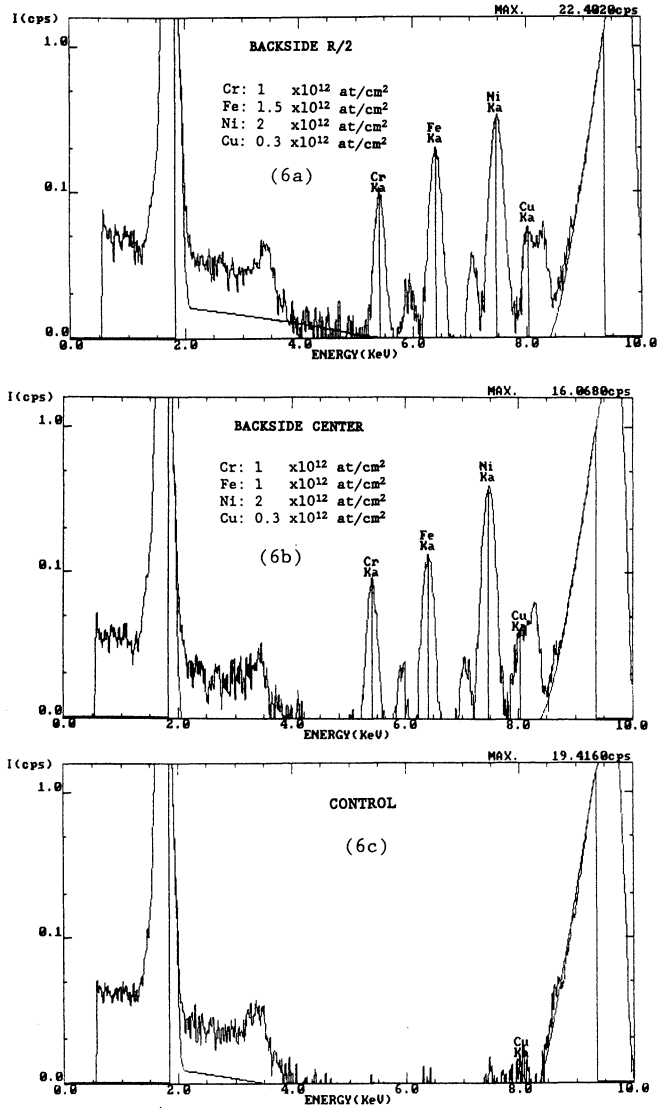

Fig. 6 TREX 610 TXRF spectra of the backside of a thermally processed silicon wafer; (6a) thermally processed center; (6b) thermally processed half radius; (6c) non-processed control.

TXRF EVALUATION OF RESIDUAL CHLORINE ON ETCHED AlCu METAL LINES

R. S. Hockett
Charles Evans & Associates
Redwood City, CA 94063

X. C. Mu and Li-Jia Ma
Intel Corporation
Santa Clara, CA 94538

A TECHNOS TREX 610 TXRF is used to measure the residual chlorine on planar and etched Al(Cu) metal lines as a function of reactive Cl ion etching, ashing and cleaning. The results show unexpected increases in surface Cl from cleaning after ashing, however, the surface Cl detected by TXRF does not correlate with corrosion margin test results. TXRF anglescans suggest the analysis area is the metal line tops even at high glancing angles, so sidewall Cl which may be more relevant to corrosion is not detected.

INTRODUCTION

The present trend in the silicon IC industry is toward the replacement of AlSi metallization by AlCu(Si). The latter offers improved electromigration resistance, and therefore holds promise of improved interconnect reliability. However, the addition of Cu to Al(Si) also increases the sensitivity of the metallization to moisture corrosion. Moreover, studies (1-3) have shown that reactive species, primarily chlorine, from dry etch processes accelerate this corrosion.

The analytical measurement of this chlorine has been accomplished by AES (1), XRF (2) and XPS (4). However, the detection limits of these analytical measurements for chlorine are on the order of high 10^{13} to low 10^{14} atoms/cm^2, i.e. about one tenth of a monolayer. Unfortunately, this analytical limit constrains knowledge on the effectiveness of various chlorine removal processes.

In an earlier paper we presented a new analytical approach to the chlorine measurement where the detection limit is in the low 10^{12} atoms/cm^2 range (5). Samples of Al(Cu), with and without reactive ion etching, were used in conjunction with Total reflection X-Ray Fluorescence (TXRF) to demonstrate the advantage of this approach. Corrosion tests were also completed. The results, which are summarized in Table 1 showed an unexpected increase in surface Cl from cleaning after ashing, however, the surface Cl detected by TXRF did not correlate with corrosion margin test results. There was some question whether the

TXRF was detecting the chlorine only on the metal tops, or could TXRF successfully detect the sidewall chlorine also. This paper is a continuation of that investigation, where TXRF anglescans are used to evaluate if the sidewall chlorine is being detected by the TXRF measurement.

EXPERIMENTAL

Sample Description

The samples were prepared as follows. For the control wafers, p<100> silicon wafers were used for this study. A 1.0 micron thick BPSG film was deposited on the wafers. Subsequently, a 0.45 micron layer of Al-Cu(0.5%) was sputter deposited on the BPSG layer. These wafers then went through resist coating (1.8 microns), ashing with O_2 down-stream plasma, and wet acid clean sequentially. The TXRF spectra were taken at each step of the processing to serve as control spectra. For the etched wafers, the same BPSG and metal stack was used. The wafers were then patterned through litho and etch step with a 0.9 micron trench width and 1.2 micron metal line width. Two different RIE etching processes were used: a) a chlorine gas chemistry with CHF_3 additive (Process A); b) a chlorine gas chemistry with CF_4 additive in the main etch and CHF_3 additive in the over etch and passivation steps (Process B). The etched wafers were then processed through D.I. water rinse, O_2 down-stream plasma ashing, and acid 1, acid 2 and acid 3 clean. TXRF spectra were taken at each step of the process to detect any residual Cl present on the wafer. Wafers were also inspected thoroughly with an optical microscope at each step and at different time intervals for corrosion margin study.

TXRF Equipment

The TXRF measurements were made using a TECHNOS TREX 610 instrument (6). In this technique x-rays from a 9 kW rotating anode with a tungsten target are monochromatized to the W L-beta line of 9.67 keV. The x-rays impinge the sample at glancing angle, normally below the angle for total external reflection (0.19 degrees for silicon). The evanescent x-ray wave penetrates only a shallow distance into the planar sample at glancing angles below the critical angle. The fluorescence x-rays are detected using a 80 mm^2 Si(Li) energy dispersive spectrometer (EDS) with a Be window. The EDS makes the analysis a multi-element technique for Al through Zn in the periodic table. The analysis area is determined by an aperture near the detector and is 10 mm in diameter. The analysis is completed in vacuum. The detection limit for chlorine on silicon is in the low 10^{12} atoms/cm^2 range using the TECHNOS TREX 610.

In this work TREX 610 measurements were made at multiple glancing angles from 0.05 to 0.50 degree on some of the planar samples, normally patterned samples, and some specially patterned Al(Cu) samples where the

metal lines extended the entire diameter of the 150 mm wafer. The purpose of the latter samples was to better evaluate whether the chlorine on the metal sidewalls could be detected. Because the TREX 610 angle calibration method does not use a matrix signal, we were able to make the measurements both on planar (control) and patterned samples.

RESULTS

Planar Samples

The TXRF anglescans for planar sample #23 (deposited Al(Cu) on BPSG plus Clean) and patterned sample #15 (etch patterned Al(Cu) on BPSG before ashing) are shown in Figures 1 and 2 respectively. These figures illustrate the basic TXRF differences between planar and patterned samples.

For the planar sample the Al and Cu signals have an abrupt rise between 0.15 and 0.23 degree indicative of total external reflection, and then the Al signal increases slowly while the Cu drops slowly. The relative behavior of the Cu and Al signals suggest there is some segregation of Cu to the top of the Al film. The Si signal from the deep underlying BPSG begins to increase at a higher angle than for the Cu and Al, and the transition is not as abrupt. The Si signal rises at the higher angles more rapidly than for the Cu and Al, because the Si from the BPSG and substrate is a bulk signal, while the Cu and Al are from a surface film which is eventually penetrated.

Of particular importance is the shape of the anglescan for the chlorine on the planar sample. The shape of the Cl anglescan is as expected for Cl lying just on the surface of a planar Al film (7).

Patterned Samples

For the patterned sample we note the incoming x-rays are penetrating the photoresist on top of the metal lines, and then exciting the elements of interest which emit fluorescence x-rays which subsequently travel out through the resist before reaching the detector. A schematic of the sample/x-ray configuration is shown in Figure 3. The fluorescence x-rays from the organics in the photoresist are not detected by the TXRF Si(Li) detector which has a Be window.

In this case Figure 2 shows the Al signal has a much different behavior with angle compared to the planar Al signal. For the patterned wafer the Al generally increases with angle, but there is no abrupt transition indicative of total reflection and the Al does not always increase, i.e., there is not a monotonic increase in Al with increasing angle. In contrast the Cu signal does increase monotonically, and there is the semblance of a transition, though not sharp enough to indicate normal total reflection below the transition angle. The relative

behavior of the Cu and Al is very different from the planar sample, and does not have a simple explanation.

The anglescan for the Cl, which is very high from the Cl ion etching process, suggests the detected Cl is primarily on top of the photoresist, which is where it is expected after the etching process. If the Cl were only on the photoresist sidewall and if the x-rays could reach this Cl, then the Cl signal would not change with angle. The rise and drop in Cl signal at low angle is what suggests surface Cl on the photoresist, and even though the Al anglescan indicates there is no collective total reflection from the Al, there may be some surfaces where it occurs. If there is Cl on the photoresist sidewall and if it were detected in the analysis, there would be a superposition of the Cl signals from the sidewall and from the tops in the anglescan. It is possible, depending upon the ratio of the Cl levels in the two cases, that the sidewall Cl signal is being masked by the Cl top signal.

In order to see if we could distinguish between the Cl on the photoresist tops versus on the sidewall, the patterned samples were rotated with respect to the incoming x-ray beam, so that the x-ray beam was sometimes parallel, perpendicular or at 45° with respect to the metal line pattern. No differences in Cl level could be detected, either at low angles or at high angles. However, because the normal patterned wafers have the metal lines in rectangular shapes, it was not possible to expect a clear orientation for all the metal lines within the analysis area of 10 mm in diameter.

For this reason specially prepared patterned wafers were made where the metal lines ran parallel to each other over the entire wafer diameter. Two samples were used in this part of the investigation: #3 after the photoresist strip, and #7 after photoresist strip and clean. Anglescans were measured with the sample lines oriented either parallel or perpendicular with respect to the incoming x-ray beam. The ratio (parallel/perpendicular) of the Cl count rate was calculated for each angle on a sample. The average ratio for sample #3 was 0.91 with a standard deviation of 0.14 (RSD of 15%), and the average ratio for sample #7 was 1.03 with a standard deviation of 0.23 (RSD% of 22%). The ratios showed no trend with increasing angle.

In addition the sample orientation with respect to the incoming beam was changed in 20 increments between parallel and perpendicular for a constant TXRF angle of 0.5 degree. For sample #3 the RSD% of the Cl for the 20 angles was 7%, and for sample #7 the RSD% of the Cl for 20 angles was 3%. There was no evident trend in the Cl signal versus the orientation over the 20 angles.

CONCLUSIONS

The TXRF angelscan is not able either to detect the sidewall Cl, or to distinguish the sidewall Cl from the Cl on the line tops. The TXRF using the TREX 610 is able to detect the Cl on the line tops, and can be useful in studies to reduce this Cl as a function of cleaning or other processing.

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Table 1. TREX 610 TXRF Results for Cl (5)
(units of 10^{12} atoms/cm^2)
(*I indicates an interference from high S)

WF#	Cl	Corrosion Margin	Process
01	43		Al(Cu)
05	I*		Al(Cu) + PR
06	1		Al(Cu) + PR + ASH
23	120		Al(Cu) + Clean
15	4100	>2.5 hr	ETCH A
20	1900	>8 hr	ETCH A + DI
19	3000	>8 hr	ETCH A + DI repeat
21	5	>8 hr	ETCH A + DI + ASH
18	60	>7 day	ETCH A + DI + ASH + Acid 1
17	7000		ETCH A + SRD + DRY
22	7500	20 min	ETCH B
16	6800	>2 hr	ETCH B + DI
13	6500	>2 hr	ETCH B + DI repeat
14	10	>8 hr	ETCH B + DI + ASH
12	96	>7 day	ETCH B + DI + ASH + Acid 2
24	120	>7 day	ETCH B + DI + ASH + Acid 2 + Acid 3

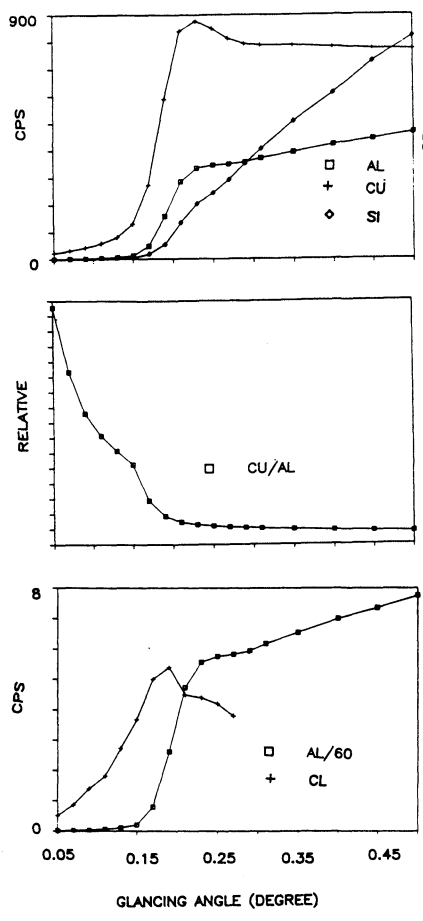

Fig. 1 TREX 610 anglescans of planar Al(Cu) metal on BPSG.

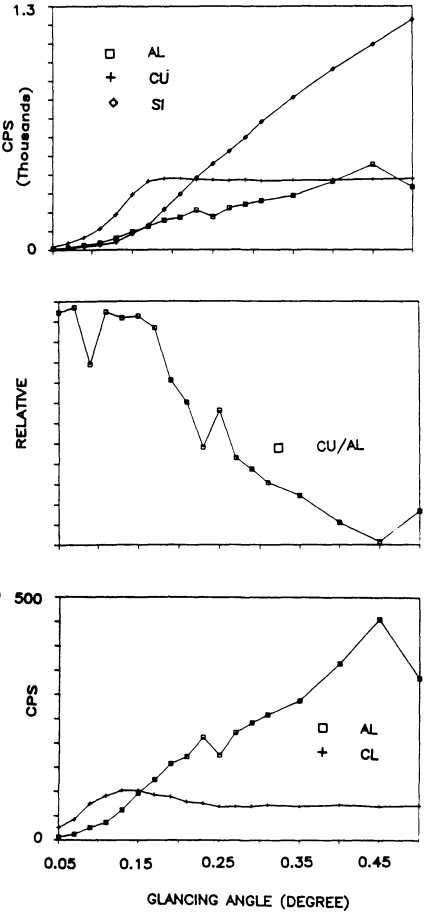

Fig. 2 TREX 610 anglescans of patterned Al(Cu) metal on BPSG.

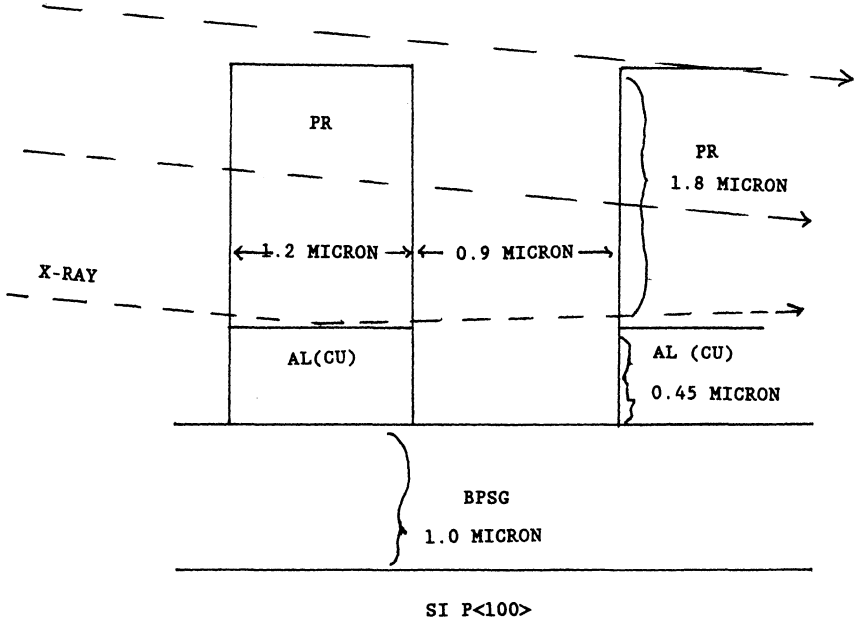

Fig. 3 Schematic of sample/x-ray configuration

A Method for Evaluating Cleaning Techniques for the Removal of Particulates from Semiconductor Surfaces

C.J. Gow*, R.E. Smith, W.A. Syverson, R.F. Kunesh,
E.D. Buker, K.B. Albaugh, and L.S. Whittingham

IBM General Technology Division
* Dept. B43 Bldg. 972-1
Essex Junction, Vermont 05452

The dependence of cleaning processes upon wafer surface and contamination type necessitates the development of consistent evaluation procedures to enable equipment and process performance comparisons. Several particle contamination methods have been tested for cleaning efficiencies using the SC-1 chemistry (ammonium hydroxide : hydrogen peroxide : water; 1:1:5) with and without megasonic energy. One surface-contamination method which differentiates between the two cleaning techniques has been chosen to evaluate a new megasonic cleaning system.

OBJECTIVE

Cleaning processes are essential as the semiconductor industry strives toward higher density chips with lower defect densities. Particle removal is crucial to eliminate defects from processes which do not meet contamination requirements and to clean wafers for foreign material (FM) inspections on equipment. Since the cleaning process depends upon the wafer surface and the contamination type, consistent test conditions have been developed to allow equipment and process comparisons.

BACKGROUND

To meet industry's demands for wafer cleaning a wide variety of techniques and process equipment have been developed (1,2). One method, megasonic cleaning, was first developed in the late 1970s (3) and has been shown to be highly effective in particle removal (1,4,5,6). Most of the data reported on megasonic cleaning has focused on the use of the SC-1 chemistry (1 part ammonium hydroxide to 1 part hydrogen peroxide to 5 parts water) (4,5). The effectiveness of the megasonic cleaning on particle removal has been reported on a wide range of contamination including polystyrene latex spheres, silicon dust, glass, and city water (5,6,7). For this study, the main criterion for the surface-contamination test is to mimic conditions found in semiconductor processing. The contamination method must also have a

controlled generation of particles and a moderate cleaning efficiency for the standard process to allow for differentiation between cleaning techniques.

APPROACH

In this paper the standard SC-1 process is studied with and without the addition of megasonic energy. Four contamination methods were tested in an established 125-mm wafer production line. In two of the methods thermal oxide wafers (22.5 nm) were run through 10:1 buffered hydrofluoric acid (BHF) to either completely strip off the oxide or to etch a thin layer from the surface. In the third test thermal oxide wafers were processed through a 165 °C phosphoric acid (H_3PO_4) bath. In the fourth case thermal oxide wafers with a LPCVD silicon nitride film (100 nm) were processed through the hot phosphoric acid until all the nitride was removed. The four tests were then split again: one half of the wafers in each test were processed through a ten minute SC-1 megasonic process at 55 °C and the other half was processed through the same tanks without megasonic energy. All the wafers were rinsed for ten minutes with DI water and spun dry. The transducers were run at 140 W with a frequency of 807 kHz. The tests were evaluated and the best was used to study a new megasonic cleaning system.

RESULTS

The results for the initial testing are presented in Table 1. All particle measurements were conducted on a Surfscan 5000 (Tencor Instruments, Mountain View, CA) with a minimum particle-size sensitivity of 0.26 μm. Measurements were made before and after the SC-1 clean.

The BHF cases were eliminated as possible test choices based on the low particle counts after BHF processing. These conditions could be readily produced using prime wafers processed through an initial wafer clean. In comparing the hot phosphoric acid cases, the wafers which had the nitride film removed were most representative of particle contamination on product wafers. This oxide/nitride case was chosen as the best test for evaluating the cleaning efficiency of the new megasonic system. Bare silicon wafers cleaned using a spray processing system were also used in the megasonic system testing.

The testing for the megasonic system was conducted using 200-mm wafers. Runs through a SC-1 bath were made with both oxide/nitride and bare silicon wafers in each boat with filler wafers in the remaining slots. In these cases a 60 °C SC-1 bath was used and wafers were processed for 12 minutes followed by a three-cycle quick-dump rinse and a spin dry. Two runs were made per bath; one with the megasonic energy on and one without. The order of the runs was alternated to eliminate bath-life effects. The transducers were run at 120 W (approximately 2.8 W/cm^2) with a frequency of 875 kHz. Particle measurements (0.3 μm sensitivity) were made before and after processing using WIS 8500 (Estek Corp., Charlotte, NC). The results are

shown in Figures 1 and 2 where the precounts and postcounts are the average number of particles for all the wafers in a given run.

Further testing on the megasonic system was conducted in a 200-mm wafer manufacturing environment. Wafers were processed in a 65 °C SC-1 for 12 minutes followed by a jet rinse, final rinse and spin dry. Particle measurements were made before and after processing using a Surfscan 5500 (Tencor Instruments, Mountain View, CA) with a minimum particle-size sensitivity of 0.26 μm. Oxide/nitride challenge wafers were used to test the system and the results are shown in Figure 3. Monitor wafers, used to check over 150 processing tools, were also run and the results are shown in Figure 4. Finally, bare silicon wafers contaminated with drinking water and allowed to air dry overnight were cleaned (Figure 5).

CONCLUSIONS

The selected contamination test presented here provides a technique for comparing particle removal from SC-1 solutions. The results from Figures 1 and 3 clearly show that the megasonic energy introduced to the SC-1 chemicals removes additional particles which cannot be removed with the chemistry alone. The results from the bare silicon wafer study indicate that the megasonic energy aids in keeping overall particle counts down, but the additional energy does not significantly remove more particles than the chemistry alone for the sample size evaluated. The megasonic energy does achieve lower particle counts on line monitor wafers (Figure 4) where the particle contamination is a random mixture of tool/line contamination. The contamination caused by drinking water however, can be readily eliminated by the SC-1 chemistry alone (Figure 5). A controlled challenge, allowing partitioning of particle removal between the chemistry and megasonics, has been demonstrated to improve the ability to optimize the cleaning process.

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Table 1. Initial test study.

	With Megasonic Energy		Without Megasonic Energy	
	Precount	Postcount	Precount	Postcount
BHF Strip	79	11	100	64
	117	11	87	46
	65	15	65	117
BHF Etch	27	7	87	79
	29	30	27	21
			49	43
Oxide (Hot H_3PO_4)	334	50	704	453
	250	39	500	202
	322	48		
Oxide/Nitride (Hot H_3PO_4)	1289	125	388	185
	818	97	495	129
	873	73	502	300

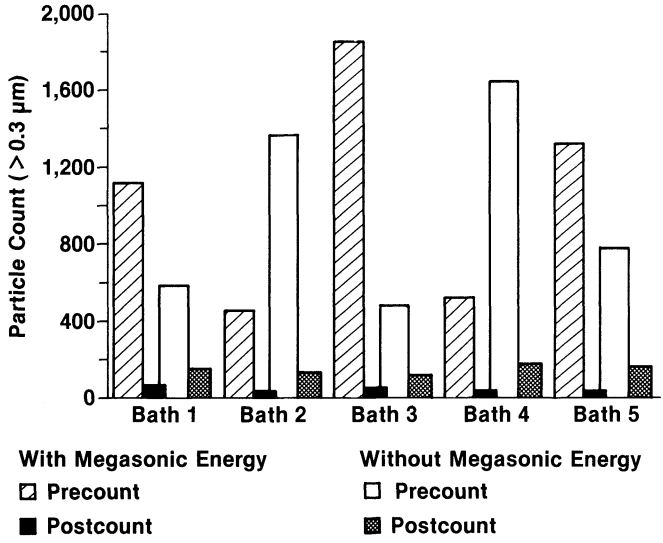

Figure 1. Oxide wafers with nitride film removed using hot phosphoric acid.

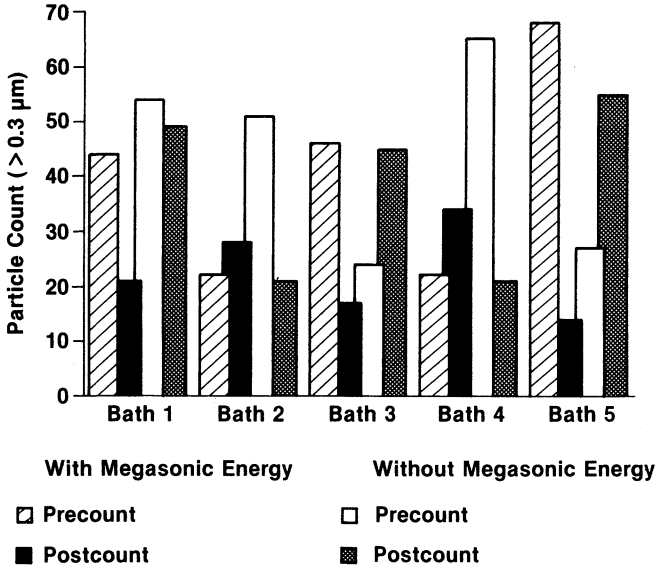

Figure 2. Bare silicon wafers.

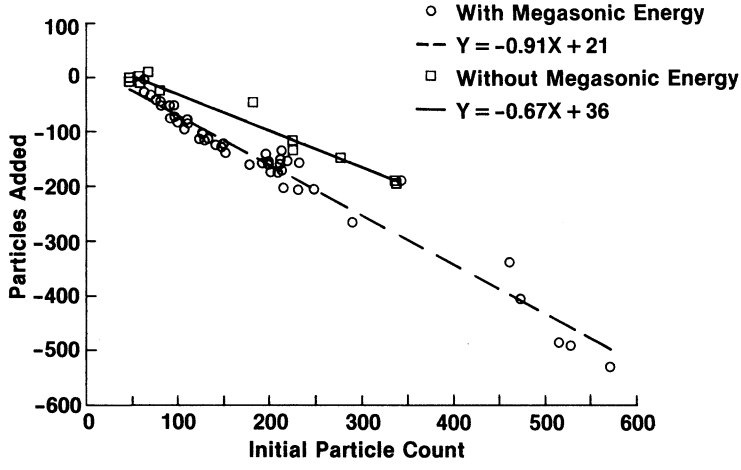

Figure 3. Challenge wafers 12-min SC-1 process.

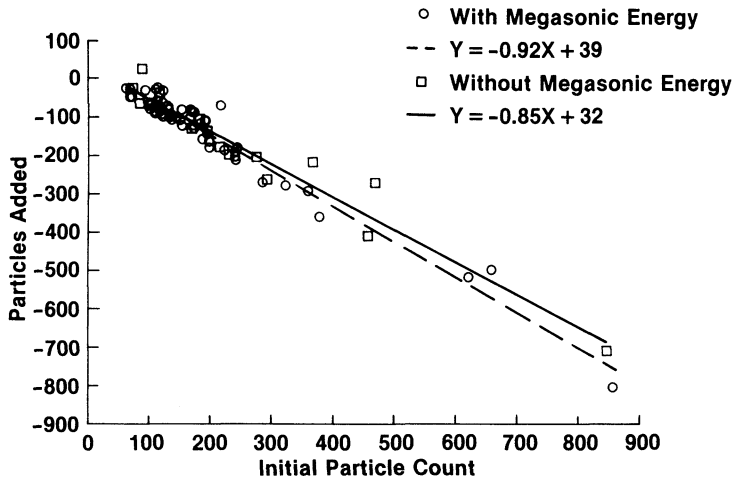

Figure 4. FM line monitor wafers 12-min SC-1 process.

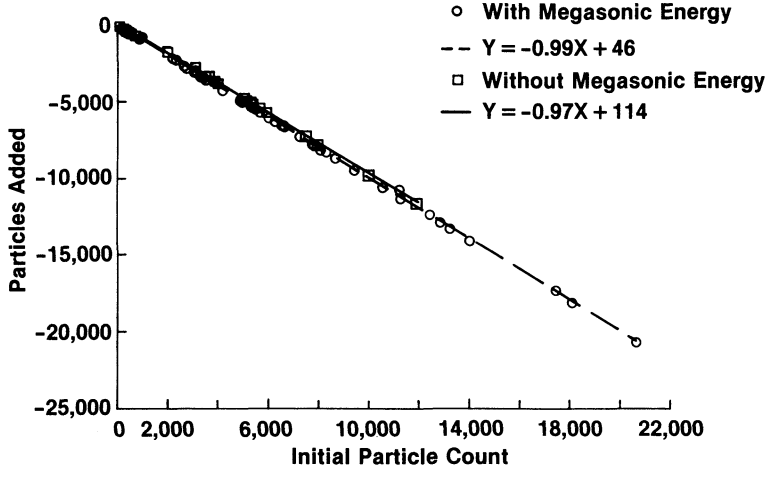

Figure 5. City water challenge 12-min SC-1 process.

CHARACTERIZATION OF AN ANHYDROUS HF PRE-GATE OXIDATION ETCHING PROCESS[a]

Part I. Experimental
Part II. Reliability, and Functionality

B. Witowski*, J. Chacon#, V. Menon
SEMATECH, Inc.
2706 Montopolis Drive
Austin, Texas 78741

* On assignment - Harris Semiconductor
Research Triangle Park, NC
On assignment - AT&T Corporation
Orlando, FL

A pre-gate oxidation anhydrous HF etching process was developed using statistical experimental methods for 120Å and 90Å gate oxides. It will be shown that for a 200Å sacrificial oxide etch a within-wafer non-uniformity of less than 2.5% can be achieved. The process was characterized for its ability to remove metals using TXRF and surface photovoltage, as well as remaining fluorine using XPS. In addition, the environmental aspects of HF waste disposal were evaluated.

INTRODUCTION

Wet chemical processing is an integral part of any semiconductor manufacturing process. Numerous wet chemical cleaning and etching operations can be found throughout a typical device process flow. Most are the result of the realization that the cleanliness of the wafer surface is an essential requisite for the successful fabrication of VLSI and ULSI silicon devices.[1] Common wet chemical processing methods are batch processes utilizing either immersion (e.g. wet benches) or centrifugal acid spray technologies.

The general trend towards smaller device geometries with high aspect ratio features has prompted questions concerning the limitations of wet chemical cleaning for critical applications. Increased environmental concerns have also resulted in more stringent waste disposal laws, which have resulted in higher wet chemical disposal costs. These increasing costs have prompted the semiconductor industry to look for alternatives to existing wet chemical cleaning processes. Gas/vapor phase cleaning/etching technology is an alternative to wet chemical processing.

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[a] This manuscript combines the two sequential presentations delivered at the symposium in Phoenix, AZ.

This paper describes the characterization of a commercially available wafer cleaning tool which uses a mixture of anhydrous HF and moisture to provide controllable oxide etching. The tool also incorporates a rinse function which enables post-etch residues to be rinsed using DI water. The anhydrous HF was "transported" to the process chamber via a carrier gas (Figure 1). Moisture was brought to the process chamber, where the N_2/HF and N_2/moisture were combined for silicon dioxide etching. The tool chosen for this study was the Excalibur ISR 200 manufactured by FSI International. The application that was chosen for this project was pre-gate oxidation cleaning/etching.

A second objective was to demonstrate that if technical parity between wet and "dry" cleans was achieved, the major benefit would be that of a reduction of both chemical consumption and environmentally-hazardous fluorinated waste, as well as possible reductions in the cost/wafer processed. Experimental attributes of anhydrous HF etching and in situ rinse were compared with conventional HF/SC-1/SC-2 cleans. These cleans were done in a commercially available, single cassette acid spray processing tool.

The overall reaction between anhydrous HF and silicon dioxide in the presence of moisture is as follows:

$$SiO_2 + 4HF \leftrightarrows SiF_4 + 2H_2O \qquad [1]$$

It is believed that the reaction proceeds according to the following hydration mechanism:[2]

$$2HF + H_2O \leftrightarrows H_3O^+ + HF_2^- \qquad [2]$$

$$SiO_2 + 2H_3O^+ + 2HF_2^- \leftrightarrows SiF_4 + 4H_2O \qquad [3]$$

Recent studies have resulted in the addition of rinsing and high speed drying steps to the overall process (following the HF purging from the process chamber). This "in situ rinse" process was added to remove residues from the wafer surface following either complete thermal oxide etch-back to silicon or any type of doped oxide etching.[4] The residues are believed to be formed from the reaction of silicon fluoride with water to form silicon dioxide (reverse reaction of (3)) or from the reaction of silicon fluoride with hydrofluoric acid to form fluorosilicic acid (4).

$$SiF_4 + 2HF \leftrightarrows H_2SiF_6 \qquad [4]$$

Studies have shown that techniques such as rinsing or heating the wafer surface have been successful in removing the residue from the wafer surface.[4] The rinsing technique has also been found to aid in the removal of metal fluorides (iron, zinc, etc.) from the wafer surface[3].

The following parameters were characterized:

- Lifetime, measured using the surface photovoltage technique;
- Mobile ion concentration using the TVS (triangular voltage sweep) method;
- Metal removal capability using TXRF and SIMS;
- Amount etched and etch non-uniformity;
- Particle removal/addition;

Silicon dioxide film thickness was measured using a Prometrix FT-500 film thickness measurement tool. Wafers with a nominal thickness of 6300Å of thermal oxide were used to determine the amount of oxide removed during an anhydrous HF etch process.

Particle measurements for this project were done using a Tencor Surfscan 5500 bare wafer particle detection tool. The calibration of these tools was carried out using latex spheres of 0.364μm and 1.091μm particle size with particle levels of 1100 and 500 per wafer, respectively. The stability of the tool was monitored on a daily basis using standardized particle test wafers.

The following instruments were also used in this project:

- Total X-Ray Fluorescence (TXRF) - Perkin-Elmer Atomika XSA 8000 TXRF tool
- X-Ray Photo-emission Spectroscopy (XPS) - Vacuum Generator ESCA Lab MKI System
- Secondary Ionization Mass Spectroscopy (SIMS) - Perkin-Elmer PHI 6300
- Current/voltage meter and probe station for TVS - Hewlett-Packard 4140B Picoammeter/Voltage Source with an Alessi R16 2500 semi-automatic stage
- Surface Photovoltage (SPV) - Semiconductor Diagnostic CMS tool

TOOL START-UP AND PASSIVE DATA COLLECTION

The start-up of the process module was designed to demonstrate (1) the etch rate characteristics of thermal oxide as a function of anhydrous HF and vapor flows and (2) the baseline particle level of the tool. The start-up results indicated that the system was functioning normally, achieving expected mean oxide etch removals (900Å to 1400Å range) and particle neutrality. The particle performance of the tool was subsequently demonstrated to be within acceptable levels for the start-up (< 30 adders $\geq 0.2\mu m$).

The medium term stability of the tool was examined by measuring the etch delta (amount etched) once per day for nineteen days. In order to establish the major sources of variation in the tool, a variance component analysis of this data was run using an RS/1[4] procedure written by the statistics department at SEMATECH. Preceding the data analysis, the medium term variance due to the Prometrix FT-500 was subtracted from the raw wafer variance. This procedure is outlined by R. Potter[5]. The results are shown in Table 1.

Table 1. ANOVA Table for variance component analysis of the anhydrous HF/ISR module

Variance Source	Degrees of Freedom	Variance Component	Standard Deviation	Percent
Total	569	9141.06	95.601	100.0
Run-run	18	1077.17	32.820	11.8
Waf-waf	38	1510.70	38.868	16.5
W/I wafer	513	6553.19	80.952	71.7
Grand mean			1418.49	
Std Ind			95.20	

The total nonuniformity for the selected process was 6.5%, with the major source of variance coming from the within-wafer component (71% of the total variance). The 6.5% figure was substantially higher than the project goal of $< 3.5\%$ for oxide etches in this range, although it should be remembered no attempt had been made to optimize the process; the purpose of the passive data collection was to determine tool stability and analyze sources of variance. The results of this study were used to develop an experimental strategy for reducing the within wafer variance component.

PROCESS DEVELOPMENT

The objective of this experimental process was to develop a recipe which would minimize the within-wafer etch nonuniformity for a nominal 200Å etch. The experiment was designed as a resolution IV fractional factorial, which meant that no two factor interactions were confounded with the main effects. The process variables that were identified and the constraints on these variables were developed such that the widest possible experimental space was examined. A typical etch/rinse recipe (along with the variables in this experiment) is shown in Table 2.

Table 2. Main Recipe driver and rinse recipe for designed experiment.

DRIVER RECIPE

Step #	Step Name	Step Time	N2 (%)	Vapor (%)	HF (%)	Rinse Recipe
0	Purge	5	100			
1	Stabilize	3	40			
2	Pre-Treatment	X1	Y1	X3		
3	Etch 1A	5	Y2	X5	Z	
4	Etch 1B	X6	Y3	X8		
5	Shutdown	1	20			
6	Go to Rinse	1	20			1
7	Shutdown	1	80			

Note: X2, X4, X7 are variables for Total Gas Flow; Y1=X2+X3, Y2=X4+X5, Y3= X7+X8; Z is HF flow to achieve 200Å etch

RINSE RECIPE 1

Step #	Step Time	N2 (%)	Water (on/off)	RPM
0	1	20	off	22
1	3	20	on	1500
2	4	20	on	1000
3	1	20	off	1000
4	10	80	off	3000

Variables **X1** and **X6** were the times for the pre-etch treatment and post-etch

treatment ("Etch 1B" in Table 2), respectively. From previous work it was determined that sufficiently uniform pre-treatment could be attained in 11 seconds or less. The lower limit chosen for this variable was 5 seconds because the MFC did not stabilize to the desired gas flow within a shorter time period.

Three other variables included in the experiment were N_2 carrier flow for vapor pick-up during the pre-treatment (**X3**), etch (**X5**), and post-treatment (**X8**) steps. The level of this variable was believed to be related to the amount of water vapor being carried in the process chamber.

The total flows of N_2 (the combined gas flows from the vapor pick-up and the mainstream) during the pre-treatment (**X2**), etch (**X4**), and post-treatment (**X7**) steps were selected as the final three variables. The upper constraint on these variables was limited by the amount of flow allowed through the chamber before the chamber back-pressure became unstable. This was empirically determined to be 26 slm. The lower constraint was determined by the maximum flow through the vapor pick-up of 10 and the minimum flow for the N_2 in the HF carrier stream (4 slm). The lower constraint for the total flow of gas was therefore 14 slm. Since the total gas flow and vapor N_2 flow were variables, the mainstream N_2 carrier flow could not be fixed. The total N_2 flow was obtained by subtracting the N_2 flow for the water vapor pick-up from the total gas flow at a given condition.

The last variable was not constrained but was used to control to a nominal etch value. This was the anhydrous HF gas flow. The HF set point for the nominal 200Å removal was determined by an iterative process for each of the 19 runs in the experiment. The percent oxide etch nonuniformity was determined for each of the runs by taking the standard deviation of the 10 point Prometrix FT-500 measurement, dividing by the mean oxide etched, and then multiplying by 100.

Using the RS/1 and RS/1 Discover[6] software to analyze the experimental data, an empirical model of the system was developed. The main effects which governed oxide etch nonuniformity were determined to be pre-treatment time, pre-treatment total flow, etch vapor flow, etch total flow, post-treatment time, and post-treatment total flow. Since the two- and three-level interaction terms were confounded with one another, the confounded interaction terms were examined for the likelihood that they had a possible interaction. For example, the interaction of pre-treatment and post-treatment times was confounded with the interaction of etch vapor flow and etch total flow. Since it was known that the etch rate was a function of vapor content, it seemed more likely that the etch vapor flow/etch total flow interaction would occur than the pre and post-treatment time interaction. The selected interaction term was then included in the model.

This procedure was used on two of the four significant interaction terms suggested by the system. For the remaining two, it was not possible to eliminate enough two factor interactions such that a non-confounded model was achieved. Table 3 lists the significant terms in the model and their level of significance. It should be noted that

the pre and post-treatment moisture times were not significant factors over the 2 to 10 slm flow range of the vapor pick-up MFC.

The data fit the model with an R-squared of 0.94 and an adjusted R-square of 0.87. These results indicated that the model was quite acceptable for an experiment of this type. To achieve these results, the nonuniformity response was transformed by taking the log of each response and fitting the model to the transformed data. There was no statistical lack of fit in the model when it was tested.

Table 3. Least squares coefficients table for designed experiment

#	Term	Coeff	Std Error	T-Value	Significance
1	1	0.07699	0.17404	1.93	0.089
2	PreTreatment Time	0.00715	0.00370	4.37	0.002
3	PostTreatment Time	0.00969	0.00222		
4	EtchMoisture	-0.02105	0.01626		
5	EtchTotalFlow	-0.00468	0.00701		
6	PostTrtmtFlow	0.01060	0.00333		
7	PreTrtmtFlow	0.02703	0.00701		
8	4*5	0.00353	0.00046	7.64	0.0001
9	4*6	-0.00087	0.00046	-1.89	0.0956
10	4*7	-0.00110	0.00046	-2.39	0.0438
11	5*7	-0.00110	0.00031	-3.58	0.0072

# cases = 19	R-sq = 0.9439	RMS Error = 0.04439
Resid df = 8	R-sq (adj) = 0.8737	Cond. No. 85.8

The model was then run through an optimization algorithm to determine the set points of the significant factors that would minimize the nonuniformity of the etch. The optimized recipe, which had a predicted within wafer etch nonuniformity of 1.8% for a nominal 200Å etch.

MANUFACTURABILITY

I. Equipment and Process Marathon #1

The objective of the marathon was to stress the tool under simulated manufacturing conditions in order to obtain process, manufacturability, and equipment reliability

data for the tool. The tool was subjected to a three week/7 days per week/24 hours per day marathon.

Manufacturing technicians collected both etch and particle data at four hour intervals over each eight hour shift. The intervals were chosen such that two data collection runs were performed per shift; thus, a total of six data collection runs were performed per 24 hour time-period. Weekend data collection runs were limited to two per day.

Virgin particle test wafers direct from the supplier were used for particle testing. These wafers generally had an initial particle count of < 100 particles of size $\geq 0.2\mu m$. Wafers, having 6300Å of thermally grown oxide, were used as etch test wafers.

A sample size of three wafers per data collection run was chosen for both types of process wafers (etch and particle). The individual wafer particle counts (two bins were chosen: ≥ 0.2 and $\geq 0.38\,\mu m$), amount of oxide etched, and within-wafer etch non-uniformity (one standard deviation) were recorded.

The tool was programmed to continually process wafers, using the selected 200Å etch recipe, in between data test runs via the loop test option. The wafers that were continually processed were 6300Å thermally grown oxide wafers. This thickness was chosen because it would allow the use of the 25 dummy wafers in a continual 200Å processing mode for at least a 12 hour period. These wafers were changed after every 12 hour period.

Table 4 shows the marathon #1 results. The tool was able to process and handle approximately 18,000 wafers while experiencing only one failure during the marathon. The one failure was related to the degradation of the O-ring that sealed the drain cup assembly from the etch area of the ISR process chamber. The degradation was probably caused by the rubbing movement of the O-ring as a result of the up and down movement of the drain cup assembly during processing. As will be shown, the drain cup O-ring rubbing problem affected both the tool's etch and particle performance.

The etch effect of the degraded o-ring was believed to be due to the failure of the o-ring to form a perfect seal between the drain cup and etch area. The lack of seal allowed additional moisture to be present in the etch area which affected etch control and uniformity. The tool's o-ring has been replaced with one which is believed to be more durable. It is believed that this new o-ring will be more resistant to wear than the previous material. In the interim, cleaning of the o-ring is recommended as part of any preventative maintenance program.

Figure 2 shows the mean etch data run results obtained for the three-week burn-in period. Each data point corresponds to the mean etch data from three etch monitors. The upper and lower limits correspond to a three standard deviation variation from the mean. A tighter distribution was achieved once the o-ring was cleaned. The

overall etch uniformity (within-wafer, wafer-to-wafer, and run-to-run) also was improved as a result of the o-ring cleaning. The overall uniformity went from 3.0% for the entire burn-in period to 2.51% for the period after the o-ring cleaning (1σ values). The pre o-ring clean data showed various points which were out of statistical process control (according to Western Electric rules). The post o-ring data only had one point which was out of statistical process control.

Table 4. - Marathon 1 results

PARAMETERS	RESULT
Utilization	90.4%
Equipment Dependent Uptime	99.8%
MTBF	441.4 Hrs.
MTTR	1.2 Hrs.
Throughput	41 wafers/hour
Mean Particle Adders $>0.2\mu m$	19
Etch Non-Uniformity (Total of run-run wafer-wafer and within wafer components)	2.5%*

* After O-ring fix

Figure 3 shows the process capability chart after the o-ring clean. Post o-ring clean etch data indicated a stable, capable process having a Cp value of 1.87 using the internal etch non-uniformity specification.

The degradation of the o-ring generated an increased number of particles ($\geq 0.2\,\mu m$) as seen in Figure 4 (each data point corresponds to the mean of three sample wafers). The degradation manifested itself as a continuous increase in the number of particles added to the wafers. The mean number of particle adders decreased from 75 prior to the o-ring issue to 19 particles added for the burn-in period following the replacement of the o-ring.

This marathon run demonstrated that two issues remained to be resolved:

- Centering the recipe to achieve a 200Å etch delta
- Need for performing a periodic preventive maintenance (cleaning) on the drain cup o-ring

II. Equipment and Process Marathon #2

The objective of this second marathon was to observe the stability (particle adders and etch characteristics) of the optimized recipe after centering for a 200Å oxide removal. A second objective was to examine any improvements that resulted from the use of a new o-ring material on the process chamber o-ring seal.

The experimental methodology was identical to that used on marathon 1 except that only a one week burn-in period was performed, and the HF flow was also brought down from 18% to 17% during the etch step in an attempt to center the oxide removal at 200Å.

The initial particle levels that were measured on the incoming particle wafers in this time period had higher levels than in the previous marathon. The initial particle levels ranged anywhere from 90 to 300 particles of size $\geq 0.2\mu m$. Nevertheless, these wafers were used as particle sampling wafers during the one week period. Results will be presented for all wafers and wafers with initial counts less than 150 particles $\geq 0.2\mu m$.

The process was found to remove an average of 36 particles $\geq 0.2\mu m$ during the one week period, an improvement in the overall mean particle counts relative to marathon #1. A graph of particle adders versus initial particle count can be seen in Figure 5a. This improvement may have been due to the high initial wafer particle counts. A second calculation was made taking into account only wafers having an initial count $\leq$ 150 particles (size $\geq 0.2\mu m$). A mean removal of 5 particles size $\geq 0.2\mu m$ resulted. Figure 5b shows the mean particle counts using only wafers that had no more than 150 initial counts.

In addition, the process was also found to add an average of 8 particles of size $\geq 0.38\mu m$. This value was identical to that obtained in marathon #1. No explanation was found for this increase. The tool seems capable of removing smaller particles, but adds those of sizes $\geq 0.38\mu m$.

Table 5 shows a comparison of marathon #2 and marathon #1 (post o-ring clean). A mean etch of 192Å was obtained during the one week marathon run. This value fell short of the targeted removal of 200Å. The entire one week burn-in etch data can be seen in Figure 6. The upper and lower specification limits correspond to a three standard deviation value from the mean. A total (run-to-run, wafer-to-wafer,

and within-wafer) process etch uniformity of 2.7% (1σ) was obtained for the one week burn-in. A more sensitive HF MFC, one that could be adjusted at intervals smaller than 10 cc/min., was indicated in order to center the process closer to 200Å total removal.

Table 5. Comparison of Marathon #1 Results with Marathon #2 Results

PARAMETER	MARATHON #1	MARATHON #2
Mean Particles Added		
$>0.20\mu m$	19	-5
$>0.38\mu m$	8	8
Mean Oxide Etched	211	192
Etch Non-Uniformity	2.5%	2.7%

Overall, the etch process was shown to be capable with an achieved Cp value of 1.32. An etch process capability study, obtained from the mean etch data points for the one week burn-in, can be seen in Figure 7. The figure shows a skewed distribution of the data points to the left of the target value of 200Å.

Figure 8 shows a plot of the within-wafer etch non-uniformity versus amount of thermal oxide etched for this process. Varying the oxide etched was achieved by changing only the HF flow during the etch step of this process. As can be seen, the non-uniformity did not significantly increase until the amount oxide etched decreased to about 50Å. This plot demonstrates the robustness of this process over a relatively wide range of oxide etched.

A more sensitive HF MFC was required to center the process to 200Å using the existing recipe parameters. The existing process was shown to be capable (Cp=1.3) using the given process specification limits of $\pm$ 15Å from a target of 200Å. The process was capable of removing particles between the size ranges of 0.2 and 0.38 microns, but added an average of 8 particles of size $\geq 0.38\mu m$.

ATTRIBUTE CHARACTERIZATION

Metals

The presence of heavy metal contaminants on the wafer surface prior to high

temperature operations has been found to be detrimental to both device reliability and functionality. Heavy metals affect the quality of thermal oxides leading to parasitic device isolation failures and lower achieved breakdown voltages for MOS gate oxides. Extensive failure analyses carried out at many companies worldwide have shown a correlation between non-visible defect density and heavy metal contamination.[7] Several experiments were performed to determine the metal removal capability of the anhydrous HF tool with in situ rinse process.

Experiment #1. The objective of this experiment was to evaluate the ability of the process module to remove inorganic surface contamination with and without the insitu rinse process following a standard etch. An experiment was also run to evaluate whether or not the metal contamination could be removed simply by an in situ rinse (no etch) following the intentional wafer contamination.

Intentional contamination was carried out using several methods. The first method used bare silicon wafers which were coated with an 8000Å thick layer of commercial photoresist. The wafers were subsequently ashed with an O_2 plasma. This procedure resulted in contamination of the wafer surface with iron, copper, nickel, and zinc. Chromium was intentionally contaminated on wafer surfaces by immersing the wafer in a chromic acid solution.

The contaminated wafers were processed in the anhydrous HF process module using the pre-gate (200Å etch) etch recipe only or the etch recipe followed by the in situ rinse. The as contaminated and processed wafers together with non-contaminated, non-processed wafers (to act as a control), were analyzed for metal contamination using total reflection x-ray fluorescence (TXRF). The data was collected for 1000 seconds ($\approx$50% dead time) at three areas across each wafer.

Table 6 shows the results obtained from all these splits. The values shown represent the mean of three measurements taken per wafer and are given in units of E12 atoms/cm^2. The resist ashed wafers showed both copper (1.0 E12 atoms/cm^2) and iron (1.6 E12 atoms/cm^2) surface contamination following the ashing operation. The surface contamination was not removed following the non-rinse etch program. The control wafers did not show metallic contamination at the detection limit of the TXRF. This indicated that the surface heavy metal contamination was achieved as a result of either the coating with photoresist and/or the ashing process.

Wafers were "uniformly" contaminated with copper and/or iron as a result of coating the wafers with photoresist and following with an O_2 plasma ashing process. The iron surface contamination was removed below the TXRF tool detection limit ($\approx$5 E12 atoms/cm^2) using the etch/rinse process. The etch/rinse process did not lower wafer surface copper contamination below detection limits.

Table 6. Metals removal capability of anhydrous HF process

Wafer Type	Iron	Copper
Control (No Resist)	< Det. Lim.	< Det. Lim.
Ashed Photoresist	1.6	1.0
Ashed Resist/Etch	2.7	0.8
Ashed Resist/Etch/Rinse	< Det. Lim.	0.7

All Values E12 Atoms/cm^2; Detection limit approximately 4E11 atoms/cm^2

Experiment #2. The objective of this experiment was to compare the surface iron and copper contamination removal capability of the wet and dry pre-gate clean processes. The same experimental procedures (coating and ashing) were followed as in the previous experiment; in this case six virgin bare silicon wafers were used. Two wafers were processed in the Anhydrous HF/ISR process module using only the rinsing portion of the pre-gate clean recipe. Table 7 shows the results of this experiment. It can be seen that the levels of iron and copper do not change with the rinse only process.

Table 7. Metals removal capability of rinse process

Wafer Type	Iron	Copper
Ashed Photoresist	0.5	0.7
Ashed Resist/Rinse Only	0.5	0.3

All Values E12 Atoms/cm^2; Detection limit approximately 4E11 atoms/cm^2

Experiment #3. The objective of this experiment was to evaluate the surface chromium removal capability of both wet and dry pre-gate clean processes. Five wafers were processed through a chromic acid bath in an automated wet bench. Two

wafers were processed in the anhydrous HF/ISR process module: one using the etch/rinse pre-gate recipe and one using the etch portion of the recipe. An additional wafer was processed in an acid spray tool using the standard RCA wet cleaning process. The fifth chromic acid processed wafer was used as a control. The wafers were analyzed on the Perkin-Elmer Atomika XSA 8000 TXRF using the same procedure as in the previous experiments.

Table 8 shows the results which were obtained from the five wafers. The values represent the mean of three measurements taken per wafer and are given in the units of E12 atoms/cm^2.

Table 8. Chrome removal capability of anhydrous HF process

Wafer Type	Chromium
As Contaminated	10.9
Contaminated/Etch	15.3
Contaminated/Etch/Rinse	< Det. Lim.

All Values are E12 Atoms/cm^2; Detection limit is approximately 4E11 atoms/cm^2

Both the spray tool and the anhydrous HF etch/rinse processes were able to lower the surface chromium contamination (10.9 E12 atoms/cm^2) to below the detection limits of the tool (< 1 E11 atoms/cm^2). An unexplained result similar to that observed with the previous iron surface contamination experiments (increase in concentration) was seen with the chromium when using the etch only recipe in the HF/ISR module. This is believed to be an anomaly with the TXRF measurement since we observed this on many other experiments we ran using etched silicon wafers.

Both the etch/rinse process and the acid spray pre-gate clean processes are capable of lowering the chromium surface contamination levels to below the detection limit of the measurement tool.

The wet and anhydrous HF/ISR cleans were similarly efficient in lowering chromium, zinc, and iron wafer surface concentrations to levels similar to those on an incoming virgin wafer. The dry clean chemistry was not as efficient as the wet in removing wafer surface copper contamination.

Experiment #4. The objective of this experiment was to evaluate the wafer surface aluminum removal capability of the gas phase etch and etch/rinse pre-gate clean recipes.

Five wafers were immersed in an ammonium hydroxide and hydrogen peroxide bath mix for 10 minutes. The wafers were subsequently rinsed (5 cycle dump/rinse) and spun dry for 5 minutes at 2000 rpm. Two wafers each were processed using etch only and etch/rinse pre-gate clean recipes. The fifth wafer was left as a control. The wafers were then analyzed using the Perkin-Elmer PHI 6300 Quasi-Static SIMS. The experimental results are given in Table 9. Each value is given as the ratio of the aluminum to silicon peaks obtained from each respective SIMS analysis.

Table 9. Aluminum removal capability of anhydrous HF process

Wafer Type	Aluminum:Silicon Peak Ratio
As Contaminated	6.36 E-03
Contaminated/Etch	9.41 E-04
	5.76 E-04
Contaminated/Etch/Rinse	5.04 E-03
	4.30 E-04

The results indicate a reduction in aluminum wafer contamination as a result of using the anhydrous HF/ISR tool. Greater Al reduction was observed with the etch/rinse rather than with the etch only recipe. The latter observation may indicate that aluminum fluoride, formed in the etch step, was lightly bound to the surface and removed via the rinse application.

Metals Removal Summary. The etch/rinse process was comparable to the RCA spray clean process for surface metal removal capability. The rinse capability was necessary for the complete removal of most inorganic wafer surface contamination. Figure 9 shows a graph summarizing the metal removal capability of the gas phase etch/rinse process for selected metals. The graph shows that copper appears to be the only metal which the anhydrous HF/ISR process does not remove to below detection limits. Additional process development may be necessary for the etch/rinse process to sufficiently lower the copper contamination.

Surface Photovoltage (SPV) Measurements

Surface photovoltage (SPV) has been previously used as a process control monitor for oxidation and diffusion furnaces.[8] The surface photovoltage test can determine the minority carrier recombination lifetime via the direct measurement of the minority carrier diffusion length. For this study, the calculation of lifetime was avoided; the extracted diffusion length (L or L^2) was used as the figure of merit.

An objective of this work was to determine the efficiency of the cleaning process in removing metals and hence changing the diffusion length. A second objective was to establish a correlation between the surface iron concentration and the diffusion length using the SPV technique. The surface iron concentrations were measured using both TXRF (Total X-Ray Fluorescence) and SIRIS (Sputter-Initiated Resonance Ionization Spectroscopy) techniques. The correlation (if any) would enable an understanding of the ability of the SPV technique to detect very low levels of surface contaminants.

The experiment required the use of samples which were intentionally contaminated with iron at various, tightly controlled surface concentrations. This was done by two methods: the first method employed spin coating of wafer front sides with a spiked solution of iron chloride of varying concentration; the second method was to spin coat commercially available photoresist on the wafers and then follow it by an oxygen plasma ashing operation. The level of iron contamination was controlled by controlling the initial thickness of the photoresist on the wafer.

The iron concentration on the surface was determined using the Perkin-Elmer Atomika 8000 XSA TXRF and Technos TREX 610 TXRF tools; these were then used as secondary standards to correlate the Atom Science SIRIS tool. The detection limits for iron as quoted by both tool suppliers and as determined through SEMATECH experiments were 4 E11 atoms/cm^2 for the Atomika, 4 E10 atoms/cm^2 for the Technos, and ~1 E10 atoms/cm^2 for SIRIS.

The samples were pre-treated twice prior to the SPV measurements. The pre-treatment step involved a rapid thermal anneal at 1100°C for 2 minutes. This step was assumed to uniformly distribute the iron throughout the wafer. Another assumption was that the iron was monatomic (no Fe clusters) throughout the wafer. The second pre-treatment step involved a 200°C anneal for 1.0 minute. The purpose of this treatment was to annihilate the iron-boron pairs that are known to form in the boron doped silicon[9]. The trap level of these pairs is believed to be closer to a band edge than that of iron itself; hence the Fe-B pairs are less electrically active. The SPV measurements were then carried out at the University of South Florida using a commercially available constant photon flux SPV tool manufactured by Semiconductor Diagnostics Incorporated.

The results of the correlation are shown in Figure 10. The correlation coefficient was

found to be -0.98 indicating a strong relationship between the two variables. This result indicated that the SPV technique can give an estimate of the surface iron concentration on a wafer.

The SPV method can be used to evaluate iron removal during cleaning processes (see Figure 10). The data points that are indicated as "AHF/ISR cleaned" were pre-treated with the photoresist ashing technique previously outlined; the initial surface iron concentration was ~ 6 E12 atoms /cm^2. Following the anhydrous HF etch/rinse process, the surface iron concentration level was reduced to 5 E10 atoms/cm^2. The iron diffusion length also changed following this cleaning process.

The SPV measurement technique was shown to correlate well with the surface iron concentration measured by TXRF and SIRIS. The SPV signal on intentionally contaminated wafers was also shown to change following treatment in the anhydrous HF/ISR tool. The change was believed to result from the iron removal that occurred in the etch/rinse process. This ability of the anhydrous HF etch/rinse process to remove surface iron was also shown via TXRF measurements.

Mobile Ionic Contamination

The triangular voltage sweep (TVS) method[10] was used to characterize wafers for alkali metal contamination. The TVS method of detecting alkali metals is sensitive to contaminant levels in the 1 E09 atoms/cm^2 level. This is better than an order of magnitude improvement over the standard bias-temperature-stress method of detecting mobile ions in oxides. TVS analyzes the displacement current response of a MOS capacitor vs. a ramped voltage at an elevated temperature. The area beneath the current displacement curve is directly related to the quantity of mobile ionic contaminants residing in the oxide. The objective of this experiment was to determine whether there existed a difference in mobile ionic contamination resulting from etch/rinse process vs. acid spray process.

One lot of MOS capacitors was fabricated using aluminum gates. The silicon dioxide thickness was 1050Å and the gate area was approximately 5.3 mm^2. The TVS measurements were done using a Hewlett-Packard 4140B Picoammeter/Voltage Source with an Alessi R16 2500 semi-automatic probe stage. The TVS measurement temperature was 300 $\pm$ 5°C. Two TVS scans were done by ramping the voltage from -5 V to 5 V and then back to -5 V at 0.1 Volts per second. A deflection of the baseline towards higher current would indicate the presence of mobile alkali metal contaminants.

Figure 11 shows two typical TVS scans for wafers fabricated with anhydrous HF pre-oxidation clean and a standard HF/SC1/SC2 wet cleaning sequence. The slight deflection towards lower current near zero volts results from depletion region spreading and was not indicative of mobile ions present.

Due to the lack of noticeable deflection of the current-voltage curves, it was concluded that there was no detectable difference between the anhydrous HF and wet cleans. It was also concluded that the anhydrous HF tool was not adding any alkali metals from the materials of its construction.

Thin Oxide Growth

The purpose of this study was to determine whether there was a difference in the thermal oxide growth rate and/or non-uniformity between the acid spray HF/SC1/SC2 and anhydrous HF tool (etch/rinse recipe) pre-clean processed wafers.

Three sets of five wafers were pre-cleaned in the anhydrous HF tool using the 200Å etch/rinse recipe. An additional three sets of five wafers were pre-cleaned in the on-center spray acid processor using a 200Å etch RCA recipe.

One set from each type of pre-cleaned wafers was then processed in a horizontal furnace. Each set of wafers was processed using a dry oxidation process recipe that did not contain HCl. One cassette each was processed using dry oxidation times of 8, 34, and 50 minutes. The oxide thicknesses were then measured using a Gaertner two-wavelength L125B ellipsometer. Measurements were taken at nine points on a wafer.

A two factor analysis of variance (ANOVA) was performed on oxide thickness and uniformity data. The pre-clean process and the oxidation time were the two factors used for the ANOVA.

Table 10 shows a comparison of the thermal oxide thickness and uniformity data that was obtained for both pre-cleaned processes at the various oxidation times. The oxide thickness values given represent the mean values from the nine point measurements. The uniformity values correspond to a three sigma standard deviation from the mean. Table 11 shows the analysis of variance results obtained from the oxide thickness and uniformity data. The second uniformity analysis of variance shown was done without taking into account the 13 angstrom value for the 50 minute oxidation time.

The oxide grown on the anhydrous HF pre-cleaned wafers achieved better within-wafer uniformity than the RCA pre-cleaned wafers. This observation was confirmed from the analysis of variance results which indicated that there was a significant difference in both oxide growth and within-wafer oxide uniformity as a result of the pre-cleans and oxidation times.

The significant difference in the within-wafer oxide uniformity results became more apparent when the 50 minute oxidation time anhydrous HF wafer data was not taken into account in the analysis of variance calculations (uniformity 2 results in Table 11).

Table 10. Thermal Oxide Growth Measurements

Oxidation Time (Min.)	Wafer #	Anhydrous HF Thickness	Anhydrous HF Uniformity	Spray Process Thickness	Spray Process Uniformity
	1	76	5	76	4
	2	76	3	76	7
8	3	77	2	76	5
	4	77	4	75	5
	5	76	4	76	5
	1	145	5	143	6
	2	145	4	148	8
34	3	145	4	148	7
	4	145	3	148	7
	5	146	3	148	7
	1	170	13	169	6
	2	169	6	174	8
50	3	170	8	173	6
	4	169	6	173	4
	5	170	6	173	7

Table 11. ANOVA table for oxide uniformity and growth

Parameter	DF	SS	MS=SS/DF	F value	Sig.
1. Uniformity					
Clean	1	8.53	8.53	3.39	0.078
Time	2	34.40	17.20	6.83	0.004
Interaction	2	29.87	14.93	5.93	0.008
Error	24	60.40	2.52		
Total	29	133.20			
2. Uniformity					
Clean	1	16.20	16.20	14.01	0.001
Time	2	17.94	8.97	8.97	0.003
Interaction	2	14.74	7.37	6.37	0.006
Error	23	26.60	1.16		
Total	28	76.55			
3. Oxide Growth					
Clean	1	13.33	13.33	8.16	0.009
Time	2	48420	24210	14822	0.000
Interaction	2	15.27	7.63	7.63	0.019
Error	24	26.60	1.63		
Total	29	48487			

The preliminary results from this work statistically indicate that better thermal oxide within-wafer uniformity was achieved by pre-cleaning with anhydrous HF/ISR over that with the conventional RCA clean.

XPS Analysis

The objective of the experiment was to compare the wafer surface fluorine concentration levels between etch, etch/rinse and HF-last wet processed wafers using XPS and SIMS analysis.

For the XPS analysis, five virgin wafers were processed in the following manner:

1. Wafer #1: gas phase etch/rinse
2. Wafer #2 and #3: gas phase etch
3. Wafer #4 and #5: HF-last wet clean

The HF-last wafers were processed in an automated wet station. The wafers were rinsed in an overflow cascade rinse tank and were subsequently dried using a vertical, on-axis spin-rinse dryer. All wafers were placed in cassettes and then sealed in an air-tight bag and sent for ESCA analysis at the Center for Materials Chemistry at the University of Texas at Austin.

The XPS analysis was performed using a vacuum generator ESCA Lab MKI system equipped with a 263 W, Mg K-alpha (1253.6 eV) x-ray source. Photoelectrons were energy analyzed using a hemispherical analyzer operated at a constant pass energy of 20 eV. The operating pressure of the spectrometer chamber was 1 E-10 torr. XPS data was collected with the plane of the sample at angles of 10°, 15°, 20°, 30°, 50°, and 75° to the axis of the analyzer entrance aperture. The approximate depth of analysis, d, for each profile was based on the mean free path, λ (λ = 32Å) of Si 2p photoelectrons (kinetic energy = 1386 eV) in silicon dioxide. Percent concentration values and precise binding energies were determined for each profile using a quadratic/cubic 25 point interval smoothed curve, synthesized peak areas and VG calibrated atomic sensitivity factors. The data was collected at six sampling depths to determine residual surface and bulk fluorine concentration levels.

For the SIMS comparison, a three-wafer study was conducted. The wafers were immersed in a megasonic bath containing an ammonium hydroxide and hydrogen peroxide solution. Two wafers were then processed in the anhydrous HF tool, with the remaining wafer acting as a control.

Table 12 shows the XPS results which were obtained from the five wafer sample set. The fluorine concentration is given as a percent concentration relative to the total SiO_2, Si, C, and O species. The relative fluorine concentration is given for various

sampling depths. The SIMS results are shown in Figure 12. The aluminum and fluorine values shown in the graph are given as a ratio of their respective peak to that of silicon obtained from the SIMS analysis.

Table 12. XPS Results

	Etch/Rinse	Etch Only		Wet "HF Last"	
Depth (A)	Relative Fluorine % Conc.	Relative Fluorine % Conc.		Relative Fluorine % Conc.	
	Wafer 1	Wafer 1	2	Wafer 1	2
5.6	1.14	1.18	1.38	0.43	0.00
8.3	1.15	1.02	1.27	0.53	0.00
10.9	0.93	1.02	1.06	0.30	0.00
16.0	0.79	0.96	0.80	0.22	0.00
24.5	0.58	0.68	0.68	0.00	0.00
30.9	0.44	0.58	0.54	0.00	0.00

The gas phase etch-processed wafers generally had higher fluorine relative percent concentration than the anhydrous HF etch/rinse processed wafers based on XPS data. These XPS analysis results did correlate with similar results obtained using SIMS techniques. A lower fluorine surface concentration was seen for the anhydrous HF-etch/rinse-processed wafers relative to the anhydrous HF-etch-only process (not statistically validated).

The HF-last wet clean nevertheless gave the lowest relative fluorine wafer concentration in relation to gas phase processing. This result was not correlated by SIMS measurements. The cause of the difference in fluorine levels between the HF "last" wet clean and the anhydrous HF processes has not yet been determined.

The gas phase etch/rinse process achieved a lower relative fluorine concentration level than the gas phase etch-only process. This result was confirmed by both ESCA and SIMS analysis data. The HF-last wet process gave a lower relative fluorine concentration than the gas phase etch/rinse process. This result was determined only from the XPS analysis.

FUNCTIONAL PERFORMANCE - GATE OXIDE INTEGRITY (GOI)

A two part gate oxide integrity (GOI) test was used in this study. The procedure utilized both a ramped voltage breakdown (RVBD) test and time-dependent dielectric breakdown (TDDB) test. The individual die were first tested using the ramped breakdown test which was immediately followed in series with the abbreviated TDDB test. That is, any capacitors which passed the ramped breakdown test at a specific electric field would then be tested by an abbreviated TDDB test.

The RVBD test consisted of a 0.5 MV/cm stepped ramp with each step lasting fifty milliseconds. The ramp began at 0 MV/cm and ended at 12 MV/cm. If the device under the RVBD test survived the full voltage ramp, it was subjected to an extreme TDDB stress of 12 MV/cm for five seconds. Following the test, each die was binned according to its performance during the testing. These bins were defined as:

Bin	Definition
A	Initial failure of device between 0 MV/cm and 2 MV/cm;
B-	A device which failed at 2-4 MV/cm;
B+	A device which failed at 4-8 MV/cm;
C-	A device which failed at 8-12 MV/cm;
C+	A device which survived the full ramp to 12 MV/cm;
D-	A device which survived the full ramp to 12 MV/cm but failed the 5 second 12 MV/cm TDDB test;
D+	A device which survives both the full ramp and TDDB test.

The MOS capacitor processing sequence included the growth of a sacrificial oxide of 150 $\pm$ 15Å and an implanted, field-oxide-terminated polysilicon gate to form the MOS capacitor. The gate oxidation was carried out in a dry oxygen ambient. The nominal oxide thickness was 120Å. All wafers within any given lot were processed through the sacrificial oxidation process together. At the pre-gate clean step, the wafers were split into two groups: half the wafers were processed through the anhydrous HF/ISR 200Å etch/rinse, and the other half were processed through the acid spray processor with a HF/SC1/SC2 pre-clean designed to etch a nominal 200Å of oxide. Following the cleaning split, the wafers were recombined for gate oxidation and further processing.

Ten lots of epitaxial silicon wafers were used as starting material. The wafers were P/P+ type, 6-7 Ω-cm epi, with 6-10 mΩ-cm substrate resistivity. The epitaxial layer was 7.0 μm thick. Seven of the lots were processed using the process outlined above. Three of the lots were processed with a nominal gate oxide thickness of 90Å.

The active region of the device was 3.07 mm^2. The polysilicon plate overlapped the

field oxide by 5.0 μm around the entire periphery of the device.

Figure 13 shows the GOI yield for both the 120Å gate and 90Å gate oxide processes. The statistical analysis used for the hypothesis testing utilized a standard test of proportions with different sample sizes. The Z score for each of the individual bins is shown in the histogram. No significant difference was detected in the GOI yield for any of the bins on either of the gate oxides.

The second type of GOI testing was done on MOS capacitors fabricated on bulk silicon (non-epi substrates). The C+ yield obtained on these devices significantly varied within a lot or within a split. These large variations in bin yield forced an examination of the data in another way.

It was decided to use a different failure criteria for these devices. A 1.0 mA/cm^2 current density was used as the fail criteria versus passing a 12 MV/cm electric field. The cumulative probability of a device failing versus electric field was plotted. Figure 14 shows a plot of this type. The devices all failed at a field of ~10 MV/cm due to the Fowler-Nordheim tunneling current meeting the failure criteria. To further examine the differences between the two cleans, a χ^2 test of the entire distribution was performed. This type of test would detect any significant differences in the cumulative failure distributions. At a 95% confidence level, the χ^2 test did not detect a significant difference between the two distributions.

There was no significant difference between the standard wet cleaning process and the anhydrous HF etch/rinse pre-gate cleaning process with respect to the gate oxide integrity measurements that were performed. This pertains to MOS capacitors fabricated on both epitaxial silicon and bulk substrate material.

ENVIRONMENTAL

Hazardous waste generation is one of the areas of wafer cleaning that is often overlooked by process engineers. Hazardous wastes generated during wafer cleaning must be minimized according to the Resource Conservation and Recovery Act (RCRA). Not only is waste minimization mandated by RCRA, but it is also becoming cost efficient to reduce waste generation. For example, at the time of this paper, the cost of disposing one gallon of fluorinated waste in California was approximately $4.60 while in Texas the cost was $0.58.

There are several accepted methods available for minimizing the amount of hazardous waste generated. These methods include waste segregation, waste recycling, waste reclassification, and source reduction. As pointed out recently[11], the most effective and desired method is source reduction. Source reduction is most often achieved via process optimization, technology improvements/development of new technologies, or a combination of these. The use of gas phase or partial gas phase cleaning comes under the category of new technologies.

First, a comparison of the molar HF consumption rate of the anhydrous HF tool and the standard spray processor for a 200Å etch was made. Based on a five second etch in the anhydrous tool and a 15:1 D.I. water to HF dilution in the spray tool the calculated hydrogen fluoride consumption rate of 0.05 moles compared to 1.96 moles per twenty-five processed wafers, respectively. The use of the anhydrous HF tool provided approximately a **40x** reduction in the consumption of hydrogen fluoride.

The next part of this study was to determine if there was a notable increase in fluoride ion concentration in the effluent from the acid exhaust scrubber towers when running the tool. The etch/rinse process was run with twice the amount of HF flow and twice the etch time for each processed wafer. This was intended to simulate four units running simultaneously. Wafers were continuously processed for four hours with the fluoride levels in the waste stream sampled every 5.0 minutes. The scrubber system used at SEMATECH is typical of that used in the semiconductor industry. The system was designed to remove low levels of HF vapor from the exhaust stream.

Figure 15 shows the fluoride scrubber level data before and after the study. As can be seen, the baseline level of fluoride in the waste stream was not noticeably increased at any time during the simulation. Shown for reference purposes are the maximum acceptable limits for fluoride effluent allowed by the EPA, City of Austin, and the County of Santa Clara, California (excluding Sunnyvale and Palo Alto) at the time of the study.

The etch/rinse process did not alter the scrubber effluent fluoride waste stream concentration when the HF consumption rate was equivalent to that of four tools simultaneously running.

The use of the tool for 200Å oxide etching was shown to significantly reduce the molar quantity of HF used for processing, and hence significantly reduce the volume of waste generated.

COST OF OWNERSHIP

A cost of ownership comparison of the anhydrous HF in situ rinse tool was established for the pre-gate clean application. The tool cost of ownership comparison was performed using a comprehensive cost of ownership model[12]. The model thoroughly covers all aspects (tool characterization, defect density, throughput, cost of tool, test wafer etc.) associated with the ownership of a manufacturing tool, and is especially useful for comparisons between similar pieces of equipment.

Several assumptions were made in the generation of the tool cost of ownership:

- The production requirements (starts/week) were set equal to the maximum possible wafer starts/week for one tool (determined by the model to be 4300 starts/week). The purpose of this assumption was to determine the cost of ownership for one tool process module operating at full efficiency.

- Waste disposal amounts were determined assuming a 24 hours per day/7 days per week/52 weeks per year work period.

- Tool etch and particle qualification tests were assumed to be performed at the beginning of each three-shift period. Three test wafers were assumed to be used per test.

- Six inch wafers, processed on one in situ rinse process module.

- The rinse effluent was plumbed to the fluoride rather than the concentrated acid drain. This was done even though the rinse effluent fluoride concentration (6 ppm) was below that of the city of Austin and silicon valley limits.

A significant item when calculating the cost/wafer value for the anhydrous HF/ISR pre-gate clean application was the waste disposal cost. The cost/gallon of fluoride waste in Texas at the time of this report was $0.58. This value was low relative to the typical value in the silicon valley area of $4.60 per gallon. A study was then done to compare the tool cost/wafer as a function of the HF waste disposal costs per gallon. The study compares the anhydrous HF tool to the spray acid processor for the pre-gate clean application.

Figure 16 shows the relative cost/wafer versus HF waste disposal cost/gallon for both the anhydrous HF in situ rinse module and the spray processor. The comparison was done using each tool's known or assumed particle defect density.

The anhydrous HF/ISR tool cost/wafer was not as dependent upon the cost/gallon for fluoride waste disposal as was the spray processor's. It is important to note that the spray processor had a lower cost/wafer than the anhydrous tool when the per gallon cost of fluoride wa s was $0.50.

CONCLUSIONS

- The anhydrous HF/in situ rinse process tool was shown to be a robust manufacturing system for cleaning prior to 120Å and 90Å gate oxidation.

- The anhydrous HF etch/rinse process, like the RCA clean, was capable of removing most wafer surface metal contaminants below the detection limits of the TXRF tool; however the etch/rinse process was not able to remove copper from the wafer surface. Use of the etch by itself or the DI rinse alone did not remove metals from the wafer surface.

- The tool did not add any alkali metals from the materials of construction as determined by triangular voltage sweep (TVS) measurements. These results were comparable to that obtained with the RCA clean.

- XPS measurements indicated that the etch only process left a greater amount of fluorine on the wafer surface than did the etch/rinse process. HF last wet processing gave the lowest wafer surface fluorine values.

- A capable and robust 200Å etch process with a total etch nonuniformity (within-wafer, wafer-to-wafer, and run-to-run) of 2.7% (1σ) as determined from three week marathon runs was demonstrated.

- Results from both the ramp breakdown voltage and time dependent dielectric breakdown tests indicated that there was no difference between the pre-gate clean processes at a 95% confidence interval level. These results were obtained using a LOCOS-isolated MOS capacitor of area 3.07 mm^2 with a 120Å oxide with a polysilicon gate contact.

- Preliminary results obtained for a 90Å gate oxide using the identical test structure indicated no difference between either type of pre-gate clean process or technology.

- Gas phase processing significantly reduced the molar quantity of HF used and significantly reducing the volume of waste generated. This can provide a significant cost savings to the user.

ACKNOWLEDGEMENTS

The authors would like to thank the following for their contributions during the course of this project: Dan Syverson, Dan Gay, and Paul Merrill of FSI, Dr. Mike Gordon, Peter Nunan, Richard Lynch, and the Marathon Team at SEMATECH, and Professor Lubek Jastrzebski of the University of S. Florida.

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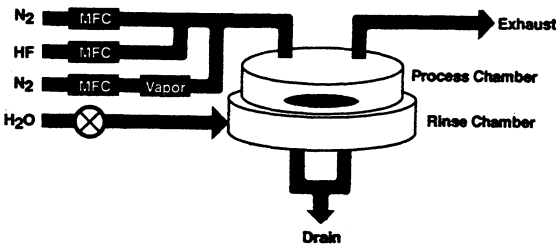

FIGURE 1 **Concept diagram of the anhydrous HF and in situ rinse module** (Used with permission - FSI International)

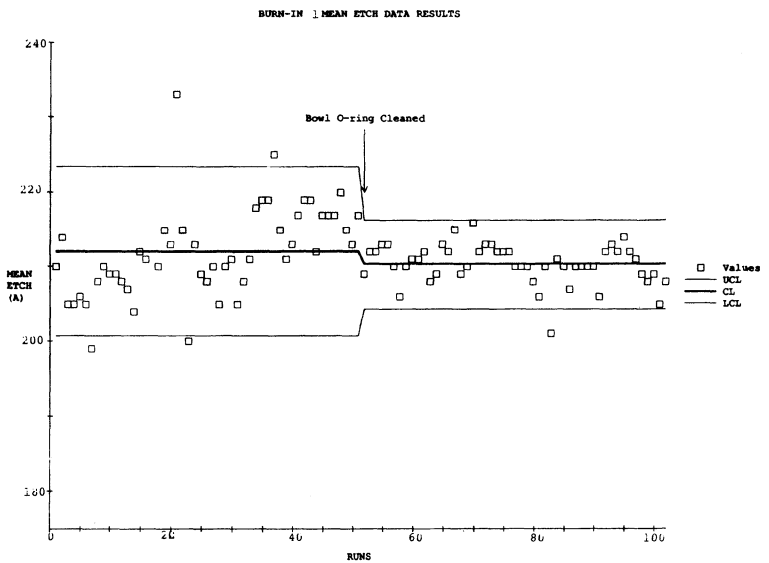

FIGURE 2 **Marathon 1 silicon dioxide etch vs. run number.**

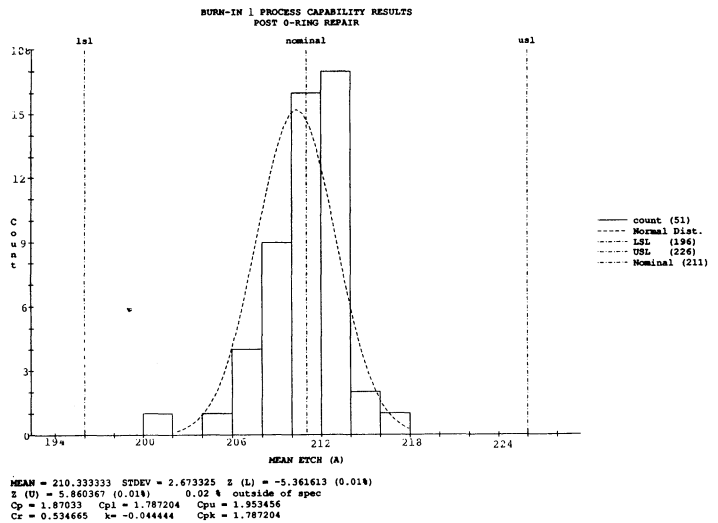

FIGURE 3 Oxide etch process capability chart for time following the O-ring clean.

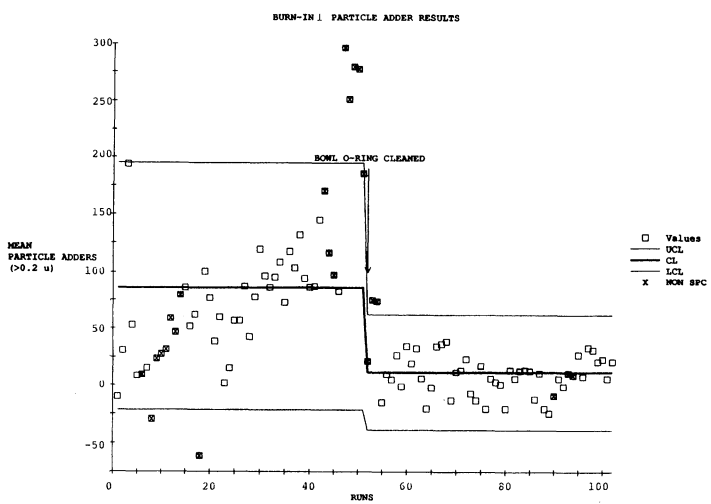

FIGURE 4 Particle performance of tool during marathon 1.

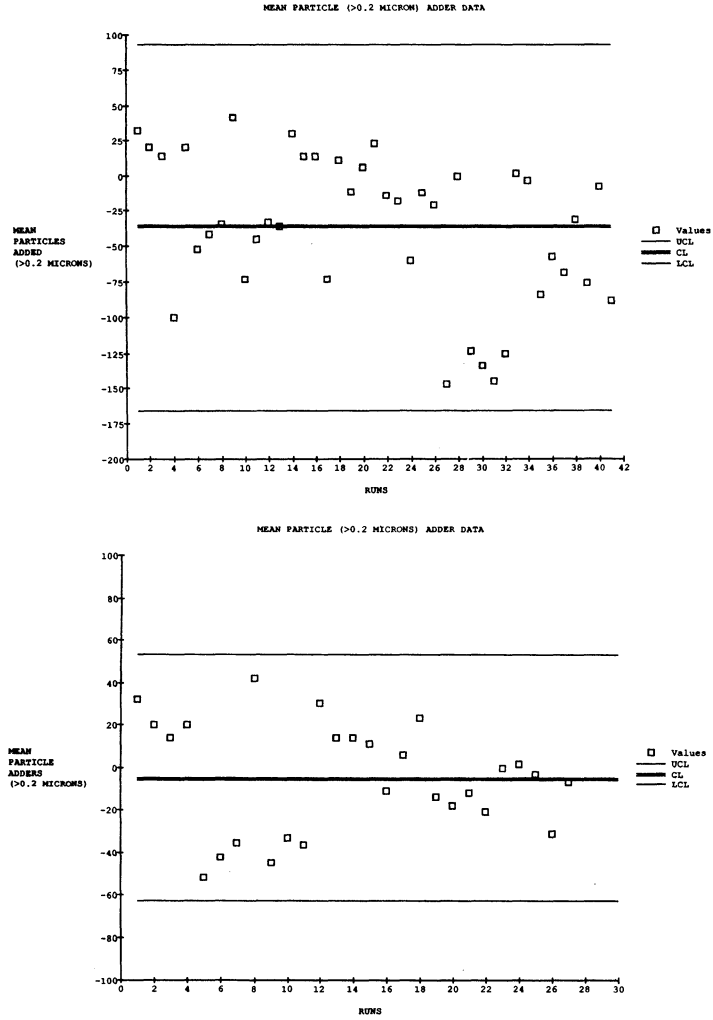

FIGURE 5 **a)** **Particle performance of all wafers during the second marathon.**
b) **Particle performance of wafers with initial levels less than 150 particles (>0.2μm) during marathon 2.**

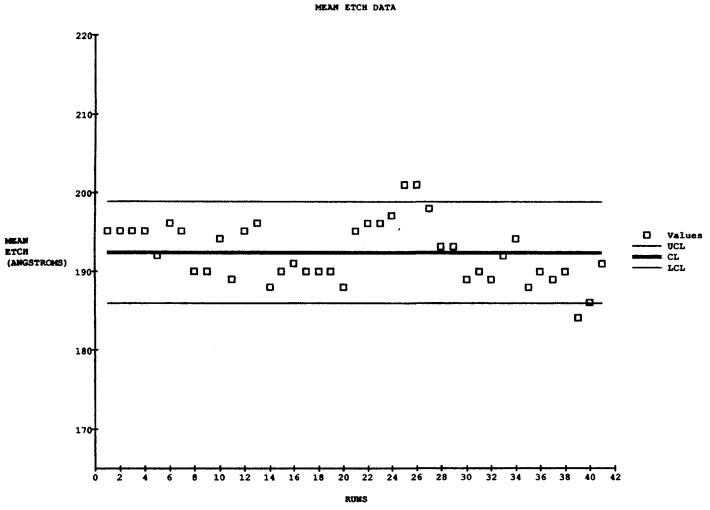

FIGURE 6 Marathon 2 silicon dioxide etch vs. run number.

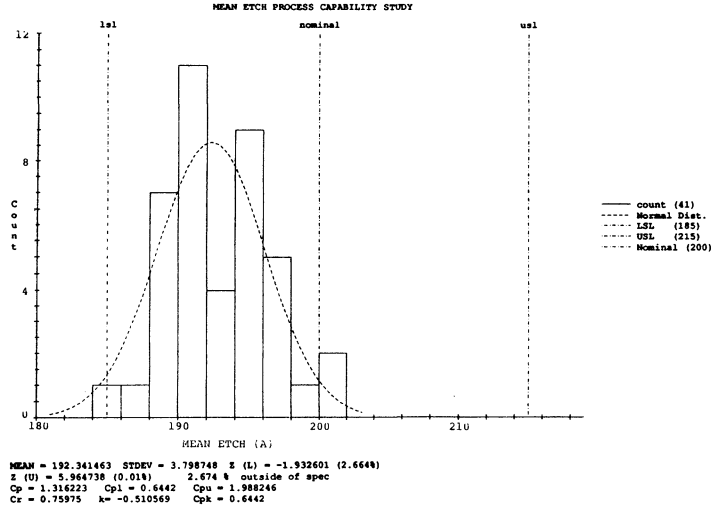

FIGURE 7 Oxide etch process capability chart for marathon 2.

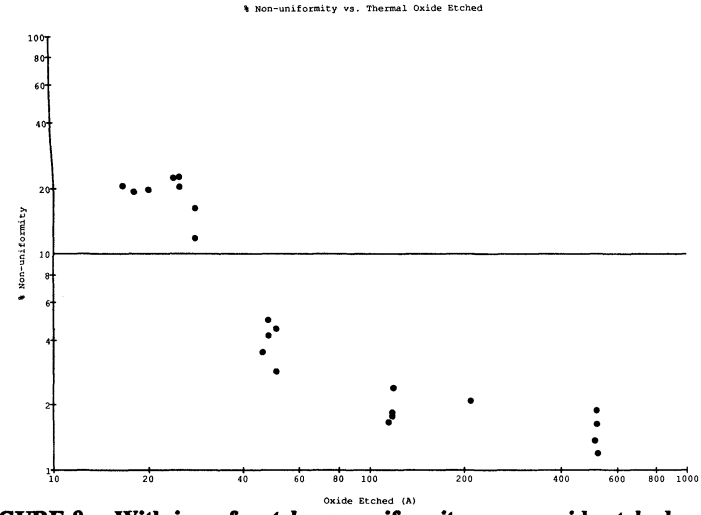

FIGURE 8 With-in wafer etch non-uniformity versus oxide etched.

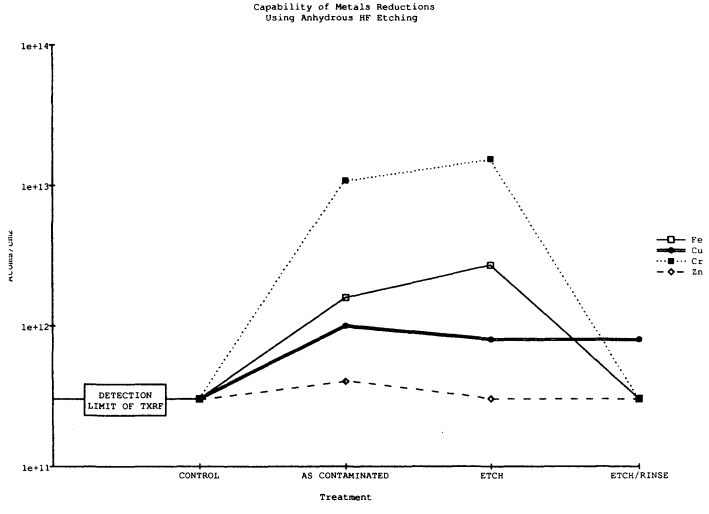

FIGURE 9 Metals removal capability of the anhydrous HF etch and rinse process.

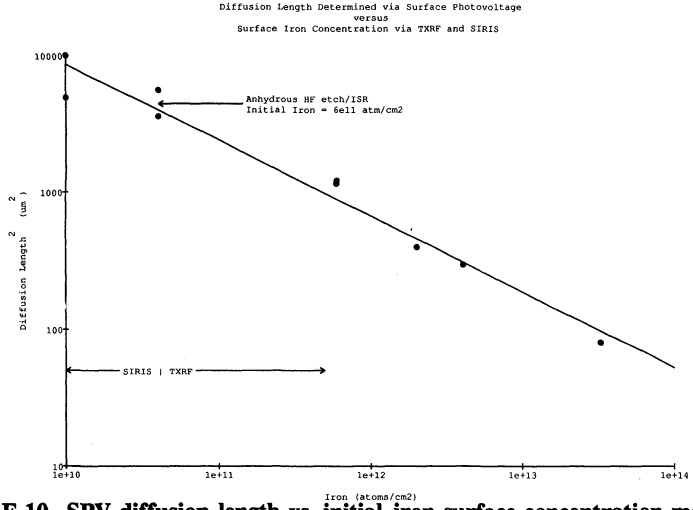

FIGURE 10 SPV diffusion length vs. initial iron surface concentration measured by TXRF and SIRIS.

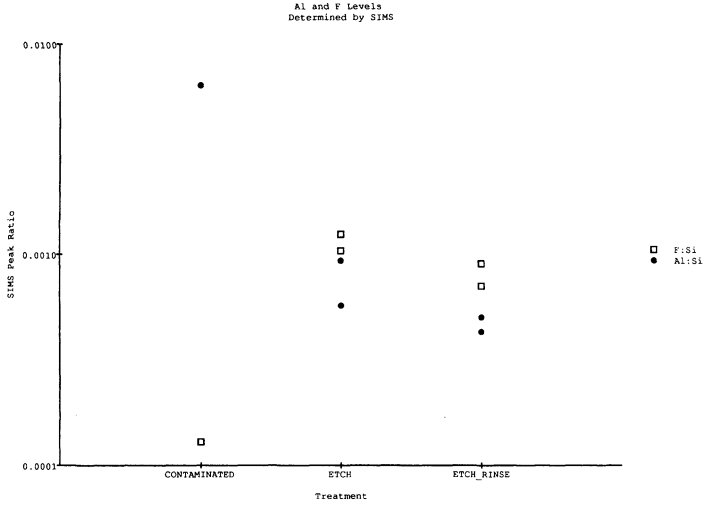

FIGURE 12 Aluminum and Fluorine surface levels measured by SIMS.

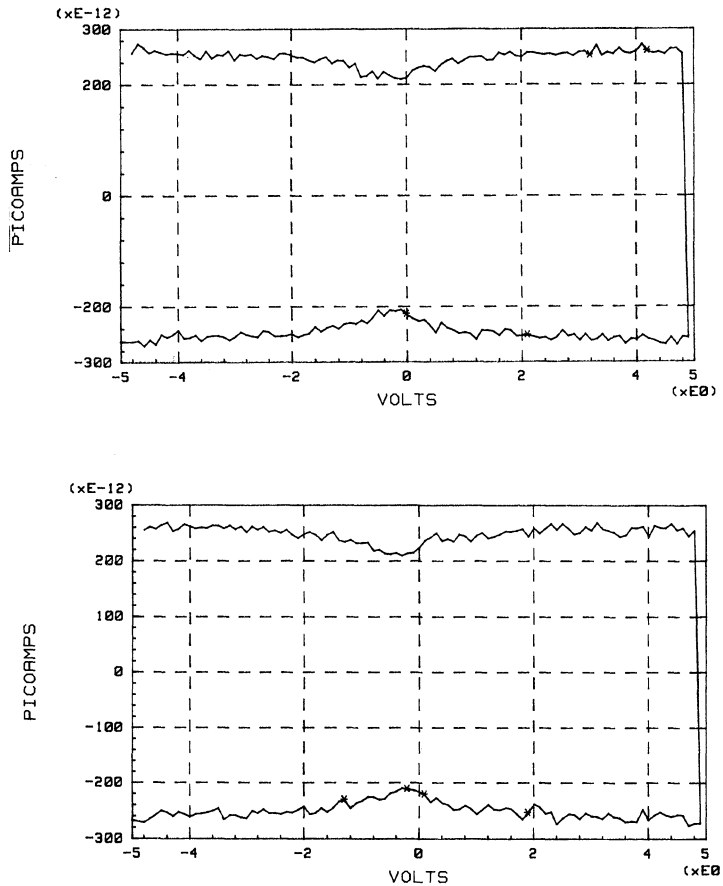

FIGURE 11 (top) **Typical TVS plot of standard cleaned wafer.**
(bottom) **Typical TVS plot of anhydrous HF/ISR cleaned wafer.**

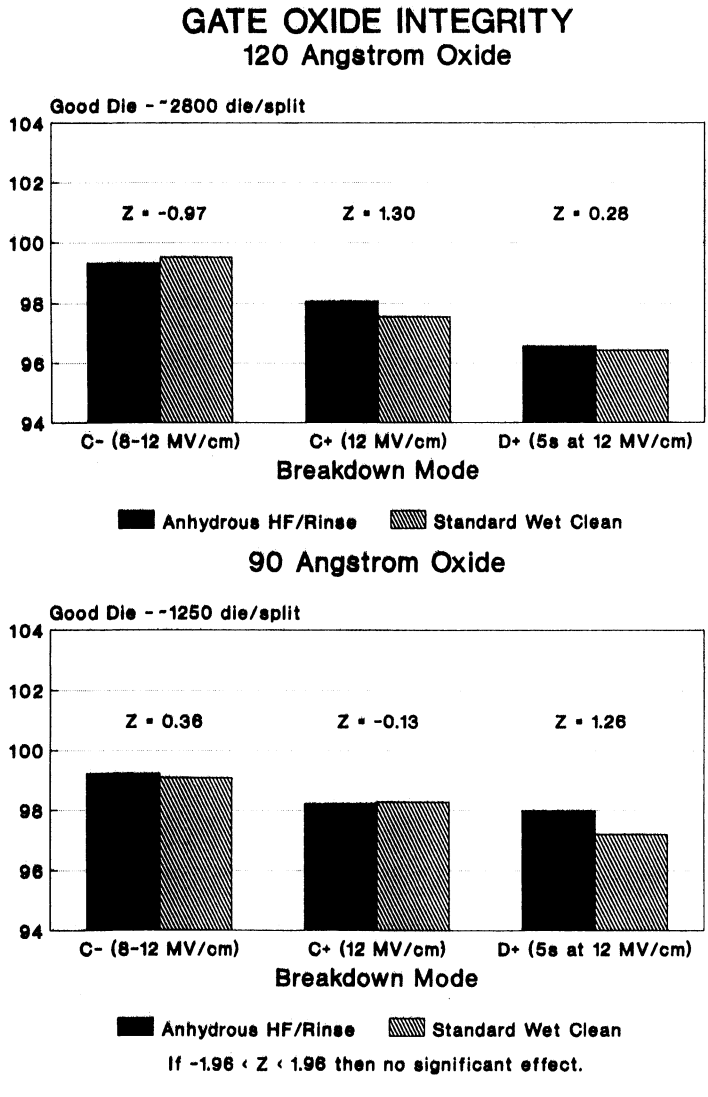

FIGURE 13 Gate oxide integrity test yield for 120Å and 90Å gate oxides.

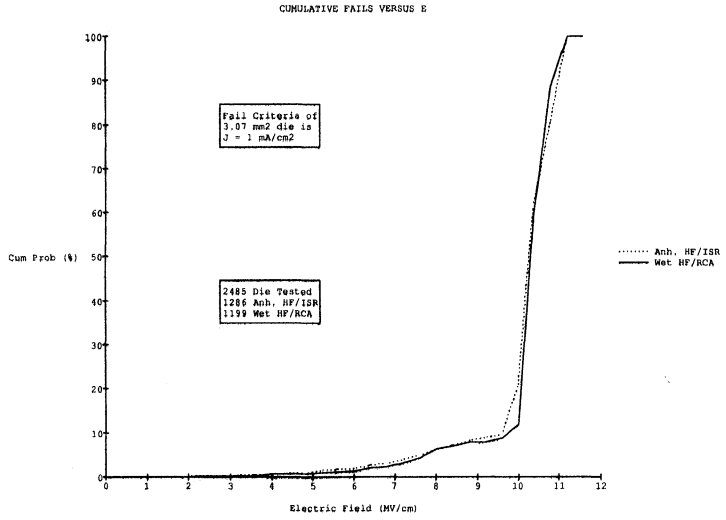

FIGURE 14 Cumulative probability plot for failure of GOI structure on non-epi material.

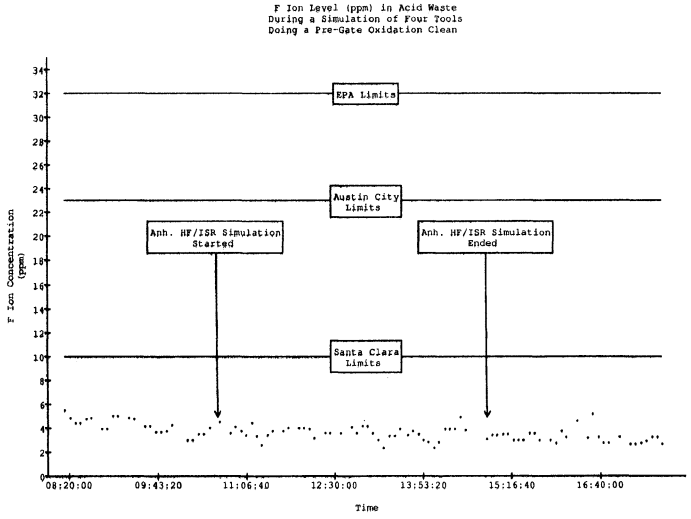

FIGURE 15 Fluoride ion levels in plant effluent before, during, and after process testing. HF flow was comparable to running four tools simultaneously.

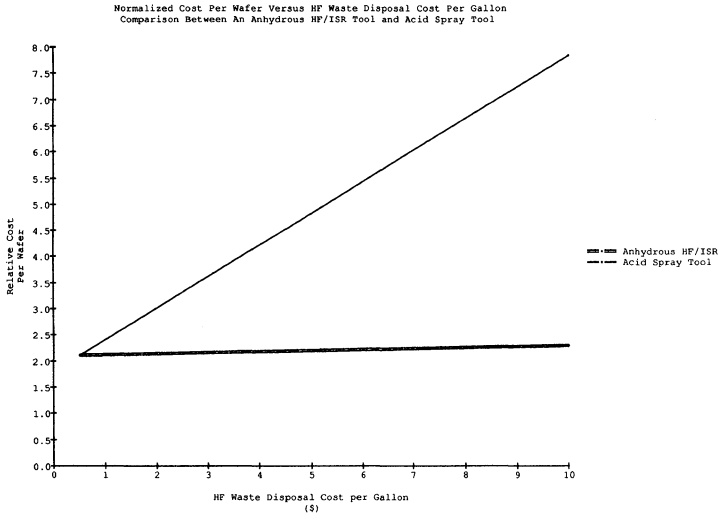

FIGURE 16 Relative cost per wafer of tool ownership versus HF waste disposal cost.

CONTAMINATION BY IMPURITIES IN CHEMICALS DURING WET PROCESSING

A.Tonti
SGS-Thomson Microelectronics
2,V.Olivetti
Agrate (Italy)

With the progress of technology,the issue of the purity of chemicals and its control takes on more and more importance.

The main conceptual control instrument,the specification, is however compiled in an empirical way.Even if there is a fair body of knowledge on the most dangerous impurities and their tolerable levels,very little is known on the relation between the impurity concentration in the chemicals and their effect on device quality and yield.

In this work a relation is given,in tabular form,between the impurity content in specific chemicals and the final residue on the device surface after wet processing.

Through comparison with accepted danger threshold values,a set of tolerable maximum levels of impurities in the most usual chemicals is derived. This allows one to compile the relevant specifications.

A MODEL FOR THE RESIDUE ON THE SURFACE AFTER TANK WET PROCESSING

An adherent film of solution remains on an hydrophilic surface after wet processing,the so-called carryover film (1,2,3).

In the case of a tank process the empirical formula for its thickness is (1,3):

$$b(cm) \approx \sqrt{0.02 U\nu} \qquad [1]$$

($\nu = \eta/\rho$ = kinematic viscosity
U = speed of extraction of the substrate from the solution)

The result,for reasonable values of U (1 cm/s) and ν (about 0.5 cs for SC-1 and SC-2 at 70°C;for 4:1 piranha about 3 cs at 75°C and 1.7 cs at 120°C,compared with 1 cs for water at 20°C) is 12 micron for SC-1 and SC-2 at 70°C,20 micron for water,30:1 HF at RT and piranha at 120°C,and 30 micron for piranha at 75°C;in excellent agreement with experimental data,17+/-7 micron for dilute solutions at RT (1,2).

TANK RINSING

In a tank rinse,at a water velocity of 1 cm/s,the average thickness of the boundary layer is given by (1,2,4):

$$\delta = \frac{2}{3} L \sqrt{\frac{\nu}{U \cdot L}} \qquad [2]$$

(L = wafer diameter,here 15 cm;
U = water velocity, 1 cm/s;
ν = kinematic viscosity,here 0.01 stokes).

In these conditions it amounts to 0.26 cm. Even under extremely strong mixing (nitrogen bubbling) it is always thicker than 300 micron, i.e. much thicker than b in any case.

This means that the carryover film is always well sheathed within,and protected by,the boundary film,even during the introduction in

the rinse bath:the rinse problem is essentially one of diffusion out of the carryover film.

This is a classical problem and may be treated rigorously (5) or also,approximately, by the method of instantaneous sources:

At time t=0 we have $c=c_o$ for 0,x,b and c=0 everywhere else. As long as b is small compared with the boundary layer thickness it may be approximated by a Dirac δ-function at x=0,with a strength

$$Q=\int_{-\infty}^{+\infty} c_o(x)\,dx=c_o b \qquad [3]$$

The subsequent evolution of diffusion in an homogeneous medium is that of a family of broadening gaussian profiles with constant area:

$$c'(x,t)=\frac{Q}{2\sqrt{\pi D t}}\exp\left(-\frac{x^2}{4Dt}\right)=\frac{c_o b}{2\sqrt{\pi D t}}\exp\left(-\frac{x^2}{4Dt}\right) \qquad [4]$$

If at x=0 we have an impermeable boundary,diffusion takes place only in the x>0 quadrant;and since the total area is always constant,the peak height must be twice that previously given by [4]:

$$c(x,t)=\frac{c_o b}{\sqrt{\pi D t}}\exp\left(-\frac{x^2}{4Dt}\right) \qquad [5]$$

and,therefore

$$c(0,t)=\frac{c_o b}{\sqrt{\pi D t}} \qquad [6]$$

Finally,

$$f=\frac{c(0,t)}{c_o}=\frac{b}{\sqrt{\pi D t}} \qquad [7]$$

where f is the fraction of contaminant left close to the surface after rinsing for a time t.

REMOVAL OF CONTAMINANTS FROM THE CARRYOVER FILM

After what said before the contaminant,which may be an impurity in the cleaning solution,stays incorporated in the carryover film during extraction from the cleaning tank.Upon introduction in the rinse tank the carryover is embedded into the boundary layer and the contaminant is carried away by diffusion.

The residue,at the end of rinse,is incorporated after extraction in a new carryover film of impure water and,at last,deposits on the surface after drying.

In tab.I residual fraction values (of the order of 1%) are tabulated, after a typical rinse cycle of 15',assuming a 17 micron carryover film thickness.

The initial carryover film content may be evaluated,in the case of Na at a 10 ppb concentration,at $4.4 * 10^{11}$ at/sqcm;and similarly for other contaminants.

Before evaluating the final content after rinsing,we must take into account another contribution,due to ions adsorbed on the surface.

SURFACE ADSORPTION:ALKALI METALS

The best presented data in literature are due to Kern (6).These have been reduced to a single surface and replotted in Fig.1.Kern states that the data taken after 60" desorption follow a Freundlich isotherm (Fig.1,curve 1)

$$Q = Q_0 * K\ c^n \qquad [8]$$

with n = 0.25 down to 70 ppm Na.It seems quite likely that also the initial,undesorbed values follow a parallel isotherm,which must allow extrapolation down to the lowest concentrations (Fig.1,curve 2).

Also the other available data are consistent with a band of values which represent the effective adsorption isotherm,with a scatter of a factor 4:in this band water and,presumably,H_2O_2 have a median position: acids are low,with HF lowest,while alkaline media rank highest.This fact may be simply explained by the competitive adsorption of hydrogen ion.

On the other side,HF generates a surface free from adsorption sites such as silanol groups,which has little affinity for sodium ions.

It must be reported that thermal oxides have a behavior similar to silicon surfaces covered with a "native" oxide layer,i.e. in contact with aqueous solution,except HF.On the other hand undensified CVD oxides seem to have a much higher adsorption power (about 1000 times more).This may be due to the much greater density of surface adsorption sites,like Si-OH (silanol) groups or nonbridging phosphorus-oxygen traps.

SURFACE ADSORPTION:COPPER AND GOLD

Literature data are again mostly due to Kern (9) and are collated in Fig.3,normalized to a single surface as before.

Summing up,it may be said that in general copper is deposited more than gold,but the trend is similar:obviously HF is the most dangerous environment, since it exposes a more or less "bare" surface to displacement plating of these metals,made possible by their noble electrochemical potential (see Fig 3,curve 1 for Cu and curve 2 for Au).

The contamination is very strong,easily more than a monolayer:recent data presented by Eichinger (10) line up very neatly in a position between copper and gold.It must be recalled that in this case we have no adsorption, but the deposition of true metal layers,more or less coherent with the substrate.These in any case cannot be removed only by rinsing:an etching clean is required.

The effective adsorption isotherm from HF is the whole band between curves 1 and 2,which are straight lines at low concentrations but tend to saturate at high ones (it must be remarked that the deposition is self-limiting to some extent).

It is strange to find also points for water in this band. Perhaps this means that the deposition may take place also in the breaks and pores of the "native" oxide layer,and that these are plentiful,in the deposition conditions.Until confirmation is given,we must treat also water as dangerous,only less so than HF and related chemicals.

SURFACE ADSORPTION:TRANSITION METALS

Data,due again to Kern (9),are incomplete in this case,since information is lacking on the effect of concentration.Chromium should be the most dangerous one,as it has a strong tendency towards adsorption from HF and also from H_2O_2.

These data should be confirmed,since the chemistry is open to discussion.The degree of adsorption is much greater than in the case of other transition metals,with the exception of copper and gold.Here it might be a matter of chemisorption,or complex ion adsorption,or even of deposition of colloidal hydroxide particles.The desorption behavior in water is unknown.

Iron has a much lower tendency to adsorption from acids,but ammonia seems to be a dangerous medium,as shown by recent measurement made in Japan by the method of lifetime measurement (16);the chemistry is again not understood.

Manganese,zinc and probably nickel have a similar behavior.If the slope of the curves for the effect of concentration were similar to the copper one,seen before,we might tentatively draw two adsorption bands,one for Cr (Fig.3,band 1) and one for Fe,Ni,Mn,Zn (band 2).

A recent datum by Eichinger (10) is consistent with this assumption.

Recent data by Takizawa (12) indicate a fair amount of adsorption for iron from nitric acid,notably at high concentrations:this fact is perhaps related to the well-known difficulty of removing iron with nitric acid cleans,but also in this case the chemistry is not well known.

THE EFFECT OF WATER RINSES

A good ultrapure water for VLSICs may still contain 0.5 ppb alkalis and 0.1 ppb transition metals.The effect of carryover thickness reduction during spin drying may roughly compensate probable accumulation effects at point of use.The ion content dries on the wafer when water evaporates,and we may calculate the deposited quantities of contaminants on the wafers (see Tab.II) in comparison with accepted danger threshold values. Even after a single rinse the levels of Na,K and Cu might have a very noticeable effect.Now in a modern 4 Mbit CMOS process there are about 20 prediffusion or predeposition cleaning steps,after which the rinse contaminants may potentially diffuse into the structure on subsequent thermal treatment.Some of these layers do not easily accept contaminants,some are etched away later on,but to be on the safe side we must multiply the deposited levels by a factor of the order of 10.Bearing in mind that the number of rinses during the whole process may be about 60 the total cumulative impact may become quite devastating.

The rinse process emerges from this treatment as potentially even more dangerous than wet processing,due to the deposition of the whole carryover content on the surface on drying.

The main remedies might be: the use of even purer water,switching to hot water or IPA drying,avoiding cleans and rinses on CVD oxides,above all undensified ones.

TOTAL RESIDUES AFTER WET PROCESSING AND RINSING

From the former consideration we may now construct tables of the total residual quantities like Tab.III,summing the carryover quantities and the adsorbed ones,and multiplying the total by the residual fraction from Tab.I.

The residue is dominated by the carryover down to a concentration of about 10 ppb,which is a typical impurity concentration of the so-called ULSI chemicals,supplied for the production of submicron ICs.

Purer chemicals are just being introduced to the market,with the exception of HF and H_2O_2 which are already available,so that the dominance of carryover is a general feature of today's chemicals.Adsorption seems to be much less important:things will probably be different in the future.

An exception is given by metals deposited in the metallic state (like Cu,Au and Pt) where the total residue is dominated by deposition and the deposited layer is not removed by rinsing,at least for deposited doses

greater than 10^{11} at/sqcm.

In this simple model we assume that desorption is in equilibrium with the rinsing process,without slow steps in series with diffusion,which would reduce the rinse efficiency.

A verification of rinse efficiency on Kern's data is in good agreement with the values reported in Tab.III.

Things become less certain when one finds strong and anomalous adsorption values (e.g.Cr from HF and H_2O_2) where,by the way,the desorption kinetics is wholly unknown).The best we can do,in the lack of new data,is to stick to the worst case (i.e. the highest values).

THE FINAL SURFACE CONCENTRATION OF CONTAMINANTS

In Tab.III a sample calculation of contamination (Na) quantities after an exposure to HF is shown.In the case of noble metal deposition the deposited quantity,generally much larger than the carryover one,is taken as resident on the surface.This calculation is extended,in Tab.IV,to all metals deposited from a typical SC-1 clean and a subsequent ideal rinse.

At this point some other factors must be taken into account.
First of all,the multiplicity effect already seen for water.
Then we must take a safety factor to account for such features as:

- accumulation at the point of use,due to contamination by the workload,corrosion,stagnation,contamination during filling up or recirculation;
- localized accumulation,like e.g. droplets on the corners of structures;
- non ideal substrate conditions,like e.g.the presence of CVD and P doped oxides,and even more so if not densified;of exposed heavily doped Si,and even of different doping types (possible cell effects),etc.
- non ideal rinse conditions (solution pockets,substrate roughness,etc).

The tank efficiency by itself (absence of dead zones) should not have a great importance,since its action is outside the boundary layer;at any rate practical experience suggests to take an additional safety factor of three in order to have an adequate operational margin.

Now it is possible to derive maximum allowable concentrations of contaminants,by multiplying the residual quantities by the proper multiplicity factor (10 to 30) and comparing the new levels with the accepted danger threshold levels for 1 to 4 Mbit CMOS technologies with 1.2 to 0.8 micron layout rules.

These are of the order of 3*E(10) at/sqcm for most metals (alkalis plus fast diffusers).Empirically gold and iron are regarded as the most dangerous ones,due to their effects on lifetime;Pt should behave like gold,with nickel less dangerous and copper also quite effective (14) in spite of its much smaller cross-section. These danger thresholds are consistent with a fairly recent specification limit for surface metal concentration on virgin wafers for VLSI, given as E(10) at/sqcm (15).

To account for the effect of real (impure water) rinses the residual contamination due to water is added to the wet process one,and it seems to mask the influence of chemicals at and below the 100 ppb level.

This cannot be accepted;the influence of water must be independently reduced by the measures already seen.

As the final example,in Tab.V the max impurity concentrations are given for NH_4OH,HCl,H_2SO_4,H_2O_2 and HF,considering single wet process steps and ideal (pure water) rinses.

In the case of complex processes,like an optimized RCA type clean,it may be shown it is the last step that matters,erasing all memory of the previous ones.This fact allows us to relax the specifications for H_2O_2 and

H_2SO_4 and to bring them to the level of ammonia and hydrochloric acid.

The values given seem reasonable and may be compared with current specifications for VLSI chemicals.They agree also with recent findings by Balazs (13) according to which "yield busts" have been recorded on advanced ICs for sodium and iron contnts above 100 ppb.

A sounder approach would be to specify not so much,or not only,the individual impurities,but the cumulative concentration for the whole group of impurities with a similar action:so,for instance,a cumulative maximum level for the mobile alkalies (Na+K+Li) might be 30 ppb.

It is also apparent that with the finer structures of the future the danger thresholds will go lower,and purer chemicals will be needed.

As a final remark,with better adsorption data it might be possible to model the total contamination on the whole structure,taking into account the etching away of some contaminated layers and the diffusion of contaminants at high temperatures.All this may be accomplished by modern simulation tools.

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TAB.I - RESIDUES AFTER 15' RINSING

Contaminant	D (cm^2/s)	f (900")
Na	$1.33 * 10^{-5}$	0.88 %
K	$1.96 * 10^{-5}$	0.72 %
Cu,Au,Fe,Ni,Cr,Zn,Mn	$0.7 * 10^{-5}$	1.21 %

Tab.II - METAL RESIDUES AFTER ONE REAL RINSE
Water purity: Na,K 0.5 ppb max each; metals 0.1 ppb max each

Metal	Carryover	Adsorbed/deposited	Total	Danger threshold
Na	$2.2*10^{10}$	$2 *10^{10}$	$4 *10^{10}$	$4 *10^{10}$
K	$1.3*10^{10}$	$1 *10^{10}$	$2.3*10^{10}$	$4\text{-}6*10^{10}$
Cu	$1.6*10^{9}$	$2.5*10^{10}$	$2.7*10^{10}$	$3 *10^{10}$
Au	$5 *10^{8}$	$1.5*10^{9}$	$2 *10^{9}$	$1 *10^{10}$
Fe,Ni	$1.8*10^{9}$	$2 *10^{9}$	$4 *10^{9}$	$5 *10^{10}$
Mn,Zn	$1.7*10^{9}$	$2 *10^{8}$	$1.7*10^{9}$	$>5 *10^{10}$

TAB.III - TOTAL SODIUM RESIDUES AFTER 9:1 HF ETCHING + IDEAL RINSE
solution makeup water purity Na,K 0.5 ppb,metals 0.1 ppb;rinse purity, absolute; Room Temperature; viscosity 1 cs; b=17 microns.The chemical residues on the wafer (scattered droplets clinging to defects and steps) have been arbitrarily equated to a continuous carryover film.

Concentration in HF	1 ppm	100 ppb	10 ppb	1 ppb
Concentration in sol.	100.4 ppb	10.4 ppb	1.45 ppb	0.55 ppb
Quantities:				
carryover	$4.4*10^{12}$	$4.6*10^{11}$	$6.4*10^{10}$	$2.4*10^{10}$
adsorbed	$8 *10^{10}$	$2.5*10^{10}$	$1 *10^{10}$	$8 *10^{9}$
total (before rinsing)	$4.5*10^{12}$	$4.8*10^{11}$	$7.4*10^{10}$	$3.2*10^{10}$
residue (.88% of total)	$4 *10^{10}$	$4.3*10_{9}$	$6.5*10^{8}$	$2.8*10^{7}$

Tab.IV - METAL RESIDUES AFTER ONE SC-2 CLEAN AND IDEAL RINSE
SC-2:13% HCl + 15.5% H_2O_2;water purity in SC-2 as above,in rinse absolutely pure;SC-2 temperature,75°C;viscosity 0.5 cs;carryover thickness 12 microns

Concentration in chemicals:	10 ppm	1ppm	100 ppb	10 ppb	1 ppb
Na,at/sqcm	$5.5*10^{11}$	$5.6*10^{10}$	$5.8*10^{9}$	$7.4*10^{8}$	$1.8*10^{8}$
K	$2.6*10^{11}$	$2.6*10^{10}$	$2.7*10^{9}$	$3.5*10^{8}$	8.6*107
Cu	$2.8*10^{11}$	$2.9*10^{10}$	$3.1*10^{9}$	$3.7*10^{8}$	$5.4*10^{7}$
Au	$8.5*10^{10}$	$8.5*10^{9}$	$8.5*10^{8}$	$9 *10^{7}$	$1.2*10^{7}$
Cr	$5.8*10^{11}$	$4.9*10^{10}$	$4.5*10^{9}$	$5.9*10^{8}$	$9.3*10^{7}$
Fe,Mn,Ni,Zn	$3.1\text{-}2.5*10^{11}$	$3.2\text{-}2.5*10^{10}$	$3.3\text{-}2.5*10^{9}$	$5.5\text{-}2.8*10^{8}$	$2\text{-}0.4*10^{8}$

Tab.V - MAX METAL IMPURITY LEVELS IN CHEMICALS (PPB)

Chemical Contaminant	NH_4OH	HCl	H_2O_2	HF	H_2SO_4
Na	25	20	20	30	1 to 20
K	50	50	40	60	2 to 40
Cu	25	20	20	0.03	1 to 20
Au	40	40	35	0.1	1.5 to 30
Fe	50	50	30	40	1.5 to 30
Ni	60	55	40	80	2 to 40
Cr,Mn	60	55	30	80	1.5 to 30
Zn	65	65	40	150	1.5 to 30

These values apply to the individual clean/rinse step.Piranha is seldom used alone as a cleaning step:the tighter values apply to H_2SO_4 ,but these may be relaxed if it is incorporated in an RCA clean.NH_4F and BHF have specifications similar to the HF one (1:9 dilution).

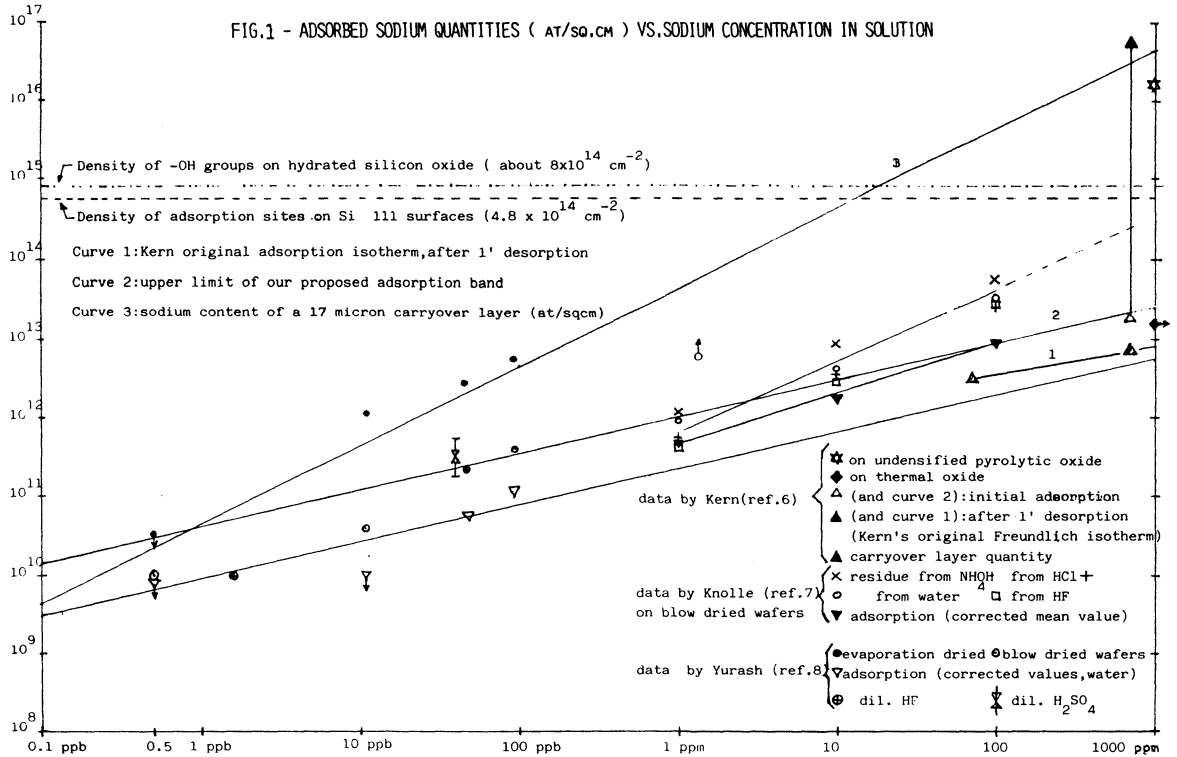


FIG.1 - ADSORBED SODIUM QUANTITIES (AT/SQ.CM) VS.SODIUM CONCENTRATION IN SOLUTION
Density of -OH groups on hydrated silicon oxide (about 8x10^14 cm^-2)
Density of adsorption sites on Si 111 surfaces (4.8 x 10^14 cm^-2)
Curve 1:Kern original adsorption isotherm,after 1' desorption
Curve 2:upper limit of our proposed adsorption band
Curve 3:sodium content of a 17 micron carryover layer (at/sqcm)
data by Kern(ref.6)
on undensified pyrolytic oxide
on thermal oxide
(and curve 2):initial adsorption
(and curve 1):after 1' desorption
(Kern's original Freundlich isotherm)
carryover layer quantity
data by Knolle (ref.7) on blow dried wafers
residue from NHOH from HCl
from water from HF
adsorption (corrected mean value)
data by Yurash (ref.8)
evaporation dried blow dried wafers
adsorption (corrected values,water)
dil. HF
dil. H2SO4
0.1 ppb
0.5
1 ppb
10 ppb
100 ppb
1 ppm
10
100
1000 ppm

FIG.2 - ADSORBED AU AND CU VS CONCENTRATION IN SOLUTION

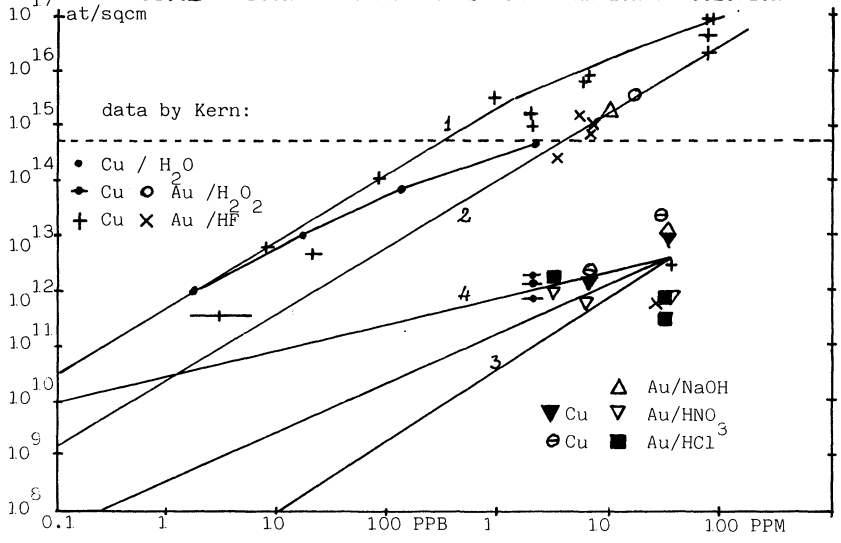
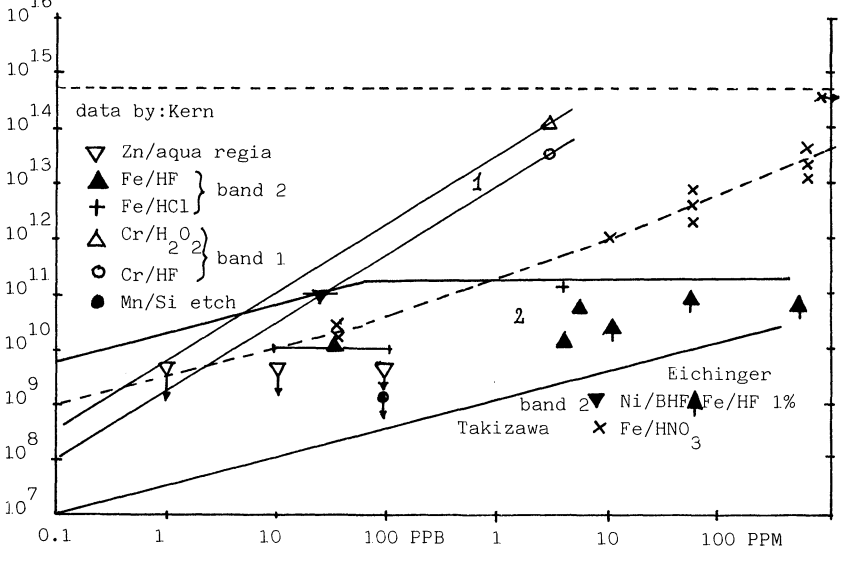


FIG.3 + ADSORBED TRANSITION METALS VS CONCENTRATION IN SOLUTION



LOW TEMPERATURE *IN SITU* CLEANING OF SILICON BY REMOTE PLASMA HYDROGEN

A.Tasch, S.Banerjee, B.Anthony, T.Hsu, R.Qian, J.Irby and D.Kinosky
Department of Electrical and Computer Engineering, University of Texas, Austin, Texas 78712

ABSTRACT

This paper reviews our recent results of *ex situ* wet chemical cleans and *in situ* low temperature remote plasma hydrogen cleans in an Ultra-High Vacuum (UHV) chamber to achieve a hydrogenated Si surface with minimal O, C and N contamination, which is critical for successful low temperature Si epitaxy. *Ex situ* wet chemical cleaning consists of ultrasonic degreasing and a modified RCA clean, followed by a final dilute HF dip, generally followed by a De-Ionized (DI) water rinse. The *in situ* clean is achieved by remote plasma excited H, where H introduced through the plasma column is r-f excited such that the plasma glow does not engulf the wafer. Using Auger Electron Spectroscopy (AES), Transmission Electron Microscopy and Reflection High Energy Electron Diffraction it is seen that a defect-free, H-terminated Si surface with C and O levels below the detection limits of AES can be achieved by this technique. The effectiveness of the various Si-H terminations as a passivation layer against re-adsorption of contaminants is also discussed. A novel electron-beam-induced adsorption of C and O on the hydrogenated Si surfaces, as determined by AES analysis, is discussed. Finally, since the best test for successful surface cleaning is the quality of the epitaxial films, results of Si homoepitaxy and Si/Si_xGe_{1-x} hetero-epitaxy under a variety of surface cleaning conditions are presented.

INTRODUCTION

Low temperature processing is extremely important for next-generation Si Ultra Large Scale Integration (ULSI) in order to minimize the thermal exposure and maintain compact dopant profiles and abrupt hetero-interfaces. A particularly critical and difficult step is low temperature Si epitaxy. Epitaxial growth places stringent demands on the cleanliness of the substrate surface, and this is especially difficult to achieve at low temperatures. It is necessary to remove carbon, oxygen and metallic impurities in order to allow nucleation of Si adatoms on the proper surface sites. This paper presents techniques for successful *ex situ* and *in situ* cleaning of the Si surface in order to achieve single crystal growth at very low temperatures (~150-480 C) by r-f Remote Plasma-enhanced Chemical Vapor Deposition (RPCVD) [1-3]. RPCVD has several advantages over conventional plasma CVD for low temperature Si homoepitaxy. Unlike a conventional plasma CVD chamber, a noble gas (argon or helium) r-f plasma is generated remotely from the wafer so that the plasma-induced damage is minimized or avoided, and the deposition reaction pathways are more controlled. The plasma generates excited species, such as long-lived noble gas metastables and energetic electrons, which are transported to the sample where they interact with and selectively excite the reactant gas species (silane) which is responsible for epitaxial deposition. Therefore, in this technique the downstream plasma excitation rather than elevated temperature is used to provide the energy needed for the deposition reaction and to increase the adatom mobility on the surface of the substrate, thereby allowing excellent control over layer thicknesses, and sharpness of interfaces and doping transitions. Hydrogen passivation of the Si surface has been found to be capable of preventing or reducing readsorption of oxygen by satisfying Si dangling bonds on the surface at low temperatures [4-6]. Actually, the H-terminated Si surface is stable only at low temperatures; for temperatures above 460°C, hydrogen will thermally desorb from the Si surface [7]. We have developed a remote hydrogen plasma clean at 250°C which effectively removes carbon, nitrogen and oxygen from a pre-treated silicon surface [5], and produces a hydrogen terminated surface with very few crystalline defects.

In RPCVD as well as in several other low-temperature epitaxy techniques such as Ultra-High Vacuum CVD developed by Meyerson [8], the final step in the wet chemical treatment is a dilute HF dip in order to remove as much of the native oxide as possible which has formed during the cleaning process. This approach leaves the surface protected by hydrogen such that little carbon and oxygen is observed after samples are loaded into the vacuum system, and such that this contamination is removable via remote hydrogen plasma cleaning at low temperatures. Chabal *et al.* [9] have analyzed silicon wafers prepared using an RCA clean followed by an HF dip and found the resultant surface to be extremely clean (i.e. little carbon, oxygen, and metallic contamination), and to be hydrogen terminated. The passivating effects of the HF treatment on silicon surfaces have been studied by several researchers. Takahagi et al. [4] found that contamination of a UV/HF treated surface increased by less than 10% after 10 min. exposure to air. Ruzyllo has reviewed some of these approaches [10]. Fenner *et al.* [11] have studied carbon and oxygen contamination of silicon surfaces cleaned using a spin etch technique by

spinning the samples at 3000 rpm while cleaning the surface with a few drops of alcohol and then etching with a few drops of an HF/alcohol solution. Fenner *et al.* have shown that after an HF spin etch and 1 minute exposure to air, total carbon and oxygen contamination is less than 1/10 of a monolayer. Kunitsugu et al. have been able to demonstrate oxygen removal from a Si surface, but with Electron Cyclotron Resonance (ECR) excitation of hydrogen at much lower pressures [12]. Tu et al. have used hydrogen plasma to remove carbon from InP but have not demonstrated it on Si [13]. Fountain and his co-workers have used Ar-excited plasma hydrogen to clean Si surfaces but have inferred the efficacy of the clean indirectly from RHEED reconstruction patterns because of the lack of *in situ* Auger analysis capability in their system [14].

EXPERIMENTAL PROCEDURE

The schematic of the RPCVD system used for the *in situ* remote hydrogen plasma clean and low temperature epitaxial growth is shown in Fig.1. The system consists of three interconnected Ultra High Vacuum (UHV) chambers: a load lock chamber for sample loading with a base pressure of 1X10-9 Torr, a surface analysis chamber with a base pressure of 1X10-10 Torr, equipped with an AES system for *in situ* monitoring of surface contamination, and a process chamber with a base pressure of <1X10-9 Torr equipped with an r-f plasma source in which the remote hydrogen plasma clean and low temperature epitaxial growth are performed. The deposition chamber is equipped with a Residual Gas Analyzer (RGA) to allow monitoring of the background levels of oxygen and water in the ambient, as well as to monitor the various species during processing using a differential pumping scheme. A RHEED system in the process chamber allows *in situ* diagnostics of surface crystallinity. The deposition is carried out using ultra-high purity gases in the process chamber, in which the partial pressures of water and oxygen are 1X10-9 Torr and 5X10-11 Torr, respectively. To further reduce the oxygen and water vapor in the process gases, all gas lines are equipped with Nanochem gas purifiers which reduce the oxygen and water vapor to the parts-per-billion level [15]. The wafers used are (100) p-type Si. Before wafers are loaded into the system, they are cleaned using a wet chemical treatment consisting of an ultrasonic degrease in TCA, acetone, and methanol. A subsequent ultra-high purity water rinse is followed by a modified RCA clean for removal of organic and metallic contamination. Finally a 60s 40:1 H_2O:HF dip is used to remove the oxide grown during the RCA clean. After the final HF dip, wafers are rinsed for 30 s in ultra-high purity water, spun dry, and immediately placed in a nitrogen purged glove box and loaded into the load lock chamber. Prior to epitaxial deposition, the wafers are cleaned *in situ* using a remote hydrogen plasma clean to remove carbon and oxygen contamination. For a typical clean, 200 sccm of hydrogen is introduced at the base of the plasma column at a pressure of 45 mTorr and inductively excited with 9 W of r-f power (13.56 MHz). During the clean, which typically lasts 45 minutes, the substrate is heated to 250°C from the back using two quartz infrared bulbs.

REMOTE HYDROGEN PLASMA CLEANING AND PASSIVATION

The r-f excitation of molecular hydrogen generates ions, electrons, neutral hydrogen atoms, vibrationally excited H_2 molecules, and electronically excited hydrogen atoms and molecules. During remote hydrogen plasma cleaning, the substrate is separated from the glow region by approximately six inches. Langmuir probe measurements between the glow and the wafer show ion and electron concentrations to be below the detectable limits (10^8 cm^{-3}) [3]. This is consistent with the large collision cross section for low energy electrons in hydrogen [16]. Since electronically excited species are short lived and the concentration of charged species is low, we conclude that the wafer cleaning due to the remote hydrogen plasma treatment is due to neutral species, either atomic H or vibrationally excited H_2, and we therefore consider the wafer to be remote from the plasma. We believe that the hydrogen plasma produces atomic hydrogen which, in turn, produces a reducing environment and has an etching effect on Si and SiO_2 by converting them to volatile byproducts. Indeed, Kunitsugu et al. have demonstrated etch rates of 123 A/ hr and 47 A/hr for Si and SiO_2, respectively, for ECR hydrogen plasma cleaning [12]. Carbon removal by this method has been shown to be very repeatable.

RHEED analysis of wafers cleaned using the remote hydrogen plasma clean at 250°C shows 1/3-order streaks (Fig. 2a) indicative of a (3x1) reconstruction pattern. This (3x1) pattern is consistent with the observations of Chabal and Raghavachari [17] for a silicon (100) surface exposed to atomic H. We therefore conclude that atomic H is responsible for passivating the wafer surface. The (3x1) reconstruction pattern has been found to be due to alternating monohydride and dihydride units [18] as shown in Fig.3a. The (3x1) reconstruction pattern can be transformed to a (2x1) reconstruction pattern by heating the wafers to or above 305 °C (Fig.2b). This results in desorption of some of the hydrogen,

which we believe produces a surface characterized by only monohydride coverage (Fig.3b). The (2x1) reconstruction pattern shown in Fig.3b is the same reconstruction pattern expected for a hydrogen free surface, in which case, the surface dimer atoms share two bonds. The (2x1) reconstruction pattern also results if the remote H plasma clean is performed in the temperature range of 305 - 400°C. In this case, the stable hydrogen termination of the surface is again the (2x1) reconstruction pattern (monohydride coverage). We have found the (3x1) and (2x1) reconstructed surfaces resulting from the remote H plasma clean to be very stable under UHV conditions. RHEED analysis shows that the (3x1) and (2x1) patterns are maintained when the samples cool to room temperature, and wafers that are allowed to remain in vacuum for 24 hours after cleaning show no increase in carbon or oxygen based on AES analysis. A (1x1) diffraction pattern is observed for wafers analyzed using RHEED after the *ex situ* treatment (Fig.2c), and for wafers subjected to the remote H plasma clean at temperatures less than 190°C regardless of the surface reconstruction before cleaning. This (1x1) hydrogen terminated surface is attributed to dihydride termination by Boland from Scanning Tunneling Microscope studies. As was the case for the (3x1) reconstruction pattern, if a (1x1) reconstructed sample is heated to >305°C, the surface reconstruction is transformed to the (2x1) reconstruction pattern.

The results of *in situ* AES analysis of the Si surface cleaned by remote plasma H at various temperatures are shown in Fig.4. The oxygen AES peak (KLL: 511 eV) from the wafer cleaned at room temperature shows the largest PPH. The oxygen PPH decreases with increasing substrate temperature and completely disappears below the AES detectability limit of 0.1-1 atomic% at temperatures above 250°C. This result indicates that the cleaning capability of the remote hydrogen plasma treatment increases with substrate temperature. However, it is important to examine defect generation such as the formation of dislocation loops on the Si surfaces cleaned at different temperatures. The mechanism for carbon and oxygen removal is believed to be atomic hydrogen combining with adsorbed species to form volatile molecules which in turn desorb into the gas phase. It is not expected that this method will create significant surface damage since we expect ion bombardment to be at relatively low energies and minimal, and since we do not observe a significant silicon etch rate. We have measured the thickness of a polysilicon layer before and after a typical 45 minute clean and found no detectable thickness change using a "Nanospec" spectrophotometer. Since our Nanospec measurements have been found to be repeatable to within +/- 15Å, the H plasma clean has an etch rate of less than 0.7Å/min. A low silicon etch rate suggests that the clean is not very effective in breaking silicon-silicon bonds which is necessary to create damage. Indeed, wafers cleaned at 250°C and 12 W r-f power show no observable defects under Nomarski microscopic examination after a dilute Schimmel etch, or using plan view Transmission Electron Microscopy (TEM). However, on some occasions crystalline defects such as dislocation loops are observed using TEM, but their cause has not yet been determined. TEM analysis of the Si surface as a function of cleaning temperature is shown in Fig.5. As can be seen, a defect density below the sensitivity limit of TEM analysis (~10^5 cm^{-2}) can only be achieved at 305°C under this cleaning condition with 12W plasma power (Fig.5(a)). As the cleaning temperature is lowered, the defect density appears to increase, and the size of the defects tends to decrease. The type of defect shown on the Si surface due to remote hydrogen plasma clean at various temperatures is predominantly dislocation loops or faulted dislocation loops as shown in Fig.5. It is believed that the formation of dislocation loops is primarily due to agglomeration of point defects such as vacancies or extra atoms [19]. Therefore, the TEM results suggest that the remote hydrogen plasma locally etches the Si surface, which, in turn, creates vacancies on the surface and results in dislocation loop formation. The increase of defect size and decrease of defect density at higher temperatures, as observed from Fig.5, may be due to the enhancement of vacancy mobility at higher temperatures. If the mobility of vacancies on the surface is higher, then the vacancies would tend to agglomerate, forming larger dislocation loops. On the other hand, vacancies with lower mobility would tend to form smaller, scattered defects. To achieve a defect-free Si surface, the substrate temperature needs to be high enough to provide the necessary mobility to "heal" the Si surface. Following the same argument, if the vacancy density is increased, then it will require higher substrate temperatures to provide higher mobility in order to achieve a defect-free Si surface. Indeed, from TEM analysis of the Si surface cleaned at 250°C with various plasma powers (15, 12, and 9 W), which are expected to give decreasing vacancy concentrations, it is found that 250°C substrate temperature, in combination with 9 W plasma power, is high enough to achieve a defect-free Si surface as shown in Fig.6(c). Since either 9W/250°C or 12W/305°C is capable of providing a defect-free Si surface as seen from Fig.6(c) and Fig.5(a), and either condition has good cleaning capability as seen from AES analysis (Fig.4), 9W/250°C was chosen as the optimal cleaning condition for subsequent passivation experiments.The passivating effect of exposure of a Si (100) surface to atomic H was studied previously by Hirayama and Tatsumi. [20]. It was found that H exposure at temperatures less than 200°C resulted in significantly less adsorbed oxygen than for wafers

without this treatment when the wafers were exposed to air for 12 hours. We have studied the passivating effect of the remote H plasma clean at 250°C by exposing cleaned wafers to room air and observing the change in carbon and oxygen contamination using AES analysis. Auger spectra taken immediately after the H plasma clean showed no detectable carbon or oxygen. Secondary Ion Mass Spectroscopy (SIMS) analysis of films deposited after the H plasma clean shows carbon and oxygen concentrations to be ~$1x10^{12}$ and $5x10^{12}$ cm^{-2} respectively.

To investigate the temperature dependence of hydrogen passivation, three wafers were passivated at 250°C, 150°C, and room temperature for 20 minutes after cleaning under the optimal conditions described above. The results of AES analysis on the Si surfaces before and after a 2-hour air exposure are shown in Fig.7. No detectable oxygen (KLL:511 eV) peaks are observed on any of these three wafers before air exposure (i.e. after cleaning/passivation), indicating an effective cleaning step. After a 2-hour air exposure, oxygen peaks are seen on all three wafers with different PPHs as shown in Fig.7. The largest oxygen PPH is observed on the wafer passivated at 250°C. The decrease of the oxygen PPH with passivation temperature suggests that lower the passivation temperature, better the Si passivation. The amounts of oxygen readsorbed on the Si surfaces passivated at different temperatures were quantified using SIMS analysis as shown in Fig.8. The Si surface passivated at room temperature shows an oxygen coverage as low as $1.2x10^{14}$ cm^{-2} which corresponds to ~0.1 monolayer if we note that a monolayer of coverage is $1.4x10^{15}$ $atoms/cm^2$ for a (100) Si surface. The fact that lower temperatures give better passivation as observed in this experiment may be explained by the lower hydrogen desorption rate at lower temperature [21,22], which, in turn, results in higher hydrogen coverage, and hence better passivation. This result is also supported by RHEED analysis. The surface reconstruction patterns of the wafers passivated at various temperatures were analyzed using RHEED, the results of which are shown in Fig.2. The Si surface passivated at 250°C shows a (3x1) surface reconstruction, while the surfaces passivated at 150°C and room temperature show a (1x1) pattern. The (3x1) hydrogen-passivated Si surface is believed to be due to an alternating monohydride and dihydride termination [17,18], while the (1x1) surface can be attributed to a dihydride coverage according to Boland [18] and Schaefer et al. [23]. The superiority of the passivation capability of the (1x1) surface over the (3x1) surface observed in this experiment suggests that the (1x1) surface observed here is due to an ordered dihydride coverage, since the hydrogen coverage is greater for a dihydride surface than for an alternating monohydride and dihydride surface (which causes a (3x1) reconstruction). The surface structures of these H-passivated Si surfaces are found to be stable even under air exposure as indicated by the RHEED patterns taken from these three wafers after 2 hours air exposure.

ELECTRON-BEAM-INDUCED ADSORPTION OF O AND C

As mentioned before, the H-passivated Si surface inhibits adsorption of O and C. It has been found, however, that a high energy (~keV) electron beam as in an AES system impinging on the hydrogenated surface desorbs the H and thereby enables O and C to be adsorbed, which is in striking contrast to electron-beam-stimulated O and C desorption reported in the literature. The AES experiments were conducted on H-terminated Si(100) surfaces with (1x1), (2x1), and (3x1) surface reconstruction in a system with a background pressure below $5x10^{-10}$ Torr. During the experiments, an electron beam with a diameter of approximately 1mm was irradiated on the H-terminated Si(100) surfaces at 2, 3 and 5 keV beam energies and various beam current densities. The Peak-to-Peak Heights (PPH's) of the Si *LVV* transition, O *KLL* transition, and C *KLL* transition were monitored every 20 s over a 4 hour period. Fig.9 shows the typical evolution of the Si(92eV), C(272eV) and O(511eV) PPH's as a function of electron beam irradiation time. The normalized Si(92eV) PPH increases gradually for a duration of 1.9-32 minutes, and then decreases exponentially with irradiation time. The normalized O(511eV) PPH appears to remain constant during the incubation period, and then increases. Although AES analysis cannot directly detect hydrogen on the Si surface, the behavior of surface hydrogen is indirectly revealed by investigating the Si PPH because of the excellent surface sensitivity of AES analysis. The increase in the Si PPH during the incubation period, as determined from AES analysis, is believed to be due to the desorption of surface hydrogen, which results in a reduction of surface coverage and hence an enhancement of the Si signal. The Si(92eV) Auger signal is very sensitive to the overlayer thickness because the inelastic mean free path of Auger electrons at 92 eV is less than 10Å[24]. The ratio of PPH at t=0, PPH(0), to PPH at the end of the incubation period, $PPH(t_{max})$ is equal to

$$PPH(0)/PPH(t_{max}) = \exp\{(-b\cdot\theta_0/D)\cdot[1-\exp(-j\cdot\gamma\cdot t_{max}/e)]\}$$

where θ_0 is the surface coverage at t=0, b is the monolayer thickness, and D is the inelastic mean free path of the Auger electrons with the energy of a specific Auger transition. The incubation period appears

to represent the amount of time required to desorb sufficient surface hydrogen such that subsequent surface reactions such as oxygen adsorption can occur. The Si PPH(t_{max}) represents the surface condition or hydrogen coverage at the end of the incubation period, which should be independent of the initial surface condition or hydrogen coverage. The Si PPH(0) represents the surface condition or hydrogen coverage at the beginning of the irradiation, which should have smaller values when the initial hydrogen coverage is greater. Hence, for the three H-terminated Si surfaces under study, the (1x1) surface should have the smallest Si PPH(0)/PPH(t_{max}) ratio, and the (2x1) surface the largest, since the (1x1) surface has been shown to have a dihydride termination, the (2x1) surface a monohydride termination, and the (3x1) a mixture of dihydride and monohydride [17]. From the experimental data of Si PPH(0)/PPH(t_{max}) ratios for various H-terminated surfaces at 2, 3 and 5 keV beam energies (Table I), the order of the Si PPH(0)/PPH(t_{max}) ratio for (1x1), (2x1) and (3x1) surfaces follows the trend predicted by the hydrogen desorption model. The incubation time is found to decrease with increasing beam current density. Since a higher current density should enhance the hydrogen desorption rate, as predicted from equation (1), the incubation time, which is the time required for the hydrogen to desorb sufficiently to allow C and O adsorption, is reduced. The values of the desorption cross sections determined using this model range from $4x19^{-19}$ to $8x10^{-18}$ cm^2 for various current densities and beam energies. After the incubation period, significant adsorption of O and C occurs, as shown in Fig.9. A power law fit to the oxidation rate indicates a dependency that lies between $\sqrt{t}$ and t (Fig.10). This could be due to a room temperature oxidation process that is due to surface reaction limited and diffusion limited behavior. Two possible sources of O are the typically present residual H_2O and CO in the vacuum chamber.

Si and $Si_{1-x}Ge_x$ EPITAXY

The acid test of successful surface cleaning is the success of low temperature epitaxy on the substrate. Silicon epitaxial growth by RPCVD can be sustained on surfaces subjected to a remote hydrogen plasma clean at temperatures down to 150°C, as confirmed by RHEED, plan view TEM and selected area diffraction analyses. Growth conditions were optimized in the range 150°C-450°C to yield a dislocation density in the epitaxial films below the sensitivity of the TEM analysis (~10^5 cm^{-2}). SIMS analysis was performed on these epitaxial Si films. The oxygen concentration in RPCVD films when a Nanochem gas purifier is used, is more than an order of magnitude lower than when the gas purifier was not in use. An oxygen concentration as low as $3x10^{18}$ cm^{-3} and a carbon concentration as low as $5x10^{17}$ cm^{-3} has been achieved in the epitaxial Si film grown at 150°C by RPCVD. *In situ* boron-doped epitaxial Si films have also been grown at 450°C. SIMS analysis results show the capability of RPCVD to achieve boron concentrations as high as $3X10^{20}$ cm^{-3}, increasing linearly with B_2H_6 partial pressure during epitaxy. The abruptness of the boron profiles have also been determined to be ~50Å/decade by SIMS. Mesa diodes with different boron doping concentrations (10^{17}-10^{19} cm^{-3}) show good forward bias characteristics with an ideality factor of 1.2-1.3. The leakage current density at -1 V reverse bias for various doping levels is in the range of 0.2-20 μA/cm^2 for a diode structure with 0.001 cm^2 junction area.

Epitaxial growth of $Si_{1-x}Ge_x$ films with Ge mole fractions as high as 0.7 has been achieved at 450°C substrate temperature by RPCVD. The $Si_{1-x}Ge_x$ films with thickness below the critical layer thickness were confirmed to have excellent crystallinity with defect density below the sensitivity of TEM analysis (10^5 cm^{-2}). It has been reported that the Ge mole fraction in $Si_{1-x}Ge_x$ films grown by thermal CVD may not be easily controlled due to the catalytic reactions between Ge and the Si surface. It has been proposed that Ge can react with the Si surface and reduce the activation energy for hydrogen desorption, which is the rate-limiting step, thereby causing growth rate enhancement [25]. The Ge mole fraction in the $Si_{1-x}Ge_x$ films grown by RPCVD increases linearly with the GeH_4 mole fraction, indicating a well controlled Ge mole fraction in the film. The relative incorporation efficiency of Ge and Si is 1.3:1, presumably due to the weaker Ge-H bond in GeH_4 than the Si-H bond in SiH_4. A pseudomorphic superlattice structure with 24 pairs of $Si/Si_{0.8}Ge_{0.2}$ layers has been grown at 450°C by RPCVD. The thickness of each Si and $Si_{0.8}Ge_{0.2}$ layer is ~60Å, as confirmed by SIMS and cross-sectional TEM analyses. Fig.11 shows the cross-sectional TEM micrograph of the superlattice structure. No extended defects such as dislocation loops and stacking faults are observed. The interfacial Ge transition layer width at the $Si/Si_{1-x}Ge_x$ interface is 30Å/decade or less, based on SIMS analysis.

CONCLUSIONS

We have discussed a technique for cleaning and passivating a silicon surface at very low temperatures (250°C), which is highly important for low temperature epitaxial growth. This technique

consists of an initial *ex situ* wet chemical treatment with a final dilute HF dip which removes most of the oxygen from the surface and passivates the surface with H. After the wet chemical treatment, wafers are transferred to the vacuum system where they are subjected to an *in situ* remote H plasma clean which supplies atomic hydrogen to volatilize and remove carbon, nitrogen and oxygen from the surface leaving behind different hydrogen terminated surfaces depending on the substrate clean temperature. We observe a (1x1) RHEED pattern at clean temperatures below 190°C, which we believe corresponds to a silicon dihydride termination, a (3x1) pattern between 200°C and 280°C, corresponding to ordered monohydride and dihydride coverage, transitioning to a (2x1) pattern with exclusively monohydride termination around 300°C. These results are consistent with the observations of Chabal and Raghavachari [17] for exposure of Si to atomic H in a UHV chamber. Wafers prepared in this manner are found to have very little carbon, nitrogen, and oxygen contamination and are adequately clean to support epitaxial growth of silicon films at temperatures between 150°C and 480°C. We have compared the surface conditions and passivating effect of an *ex situ* dilute HF treatment and the remote plasma hydrogen clean described in this paper. Both methods provide good passivation for short periods of time (~15 minutes), but the remote hydrogen plasma clean appears to provide slightly better passivation. In addition, the remote hydrogen plasma clean provides excellent passivation in a UHV environment over very long periods of time so that it is not necessary to initiate epitaxial growth immediately after the *in situ* clean.

This work was supported by ONR/SDIO Contract N00014-87-K-0323, and by the NSF Science and Technology Center at the University of Texas Contract CHE8920120.

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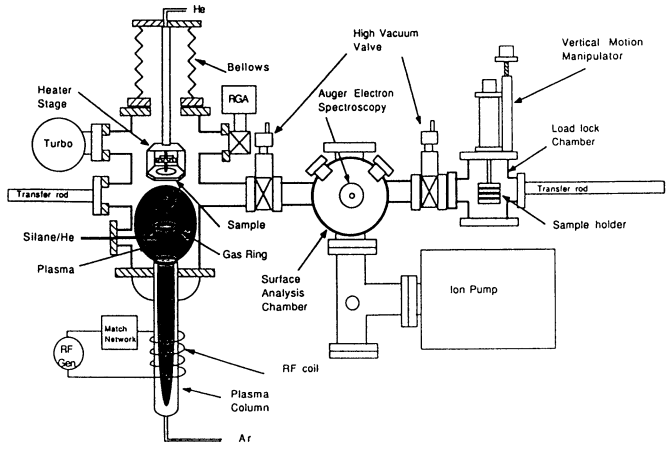


Fig.1 Schematic of the RPCVD system.

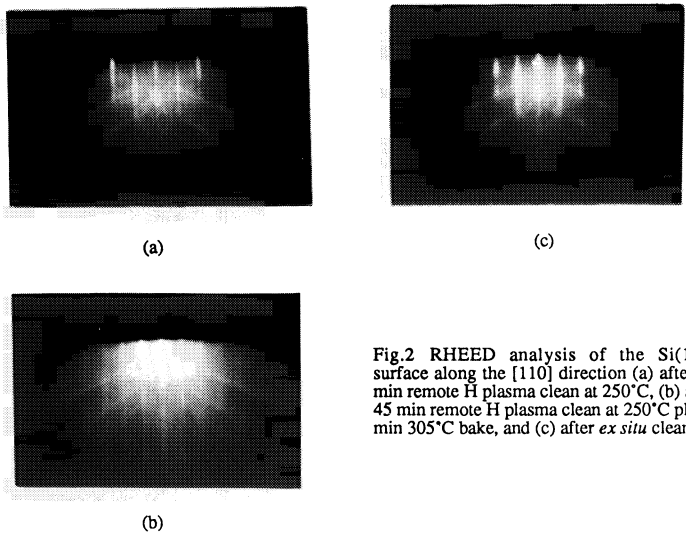


Fig.2 RHEED analysis of the Si(100) surface along the [110] direction (a) after 45 min remote H plasma clean at 250°C, (b) after 45 min remote H plasma clean at 250°C plus 5 min 305°C bake, and (c) after *ex situ* clean.

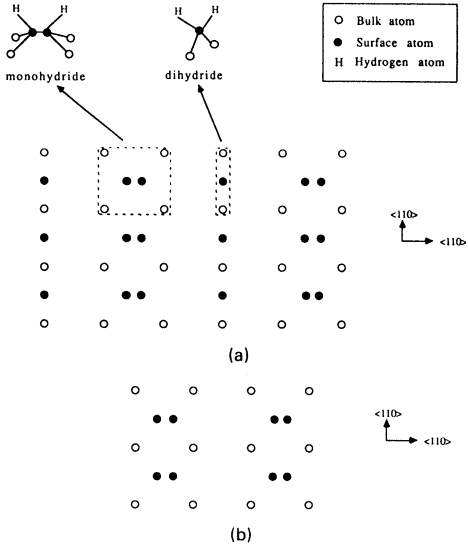


Fig.3 Schematic of H coverage for various reconstruction patterns of Si(100) surface. (a) (3x1) and (b) (2x1) reconstruction pattern.

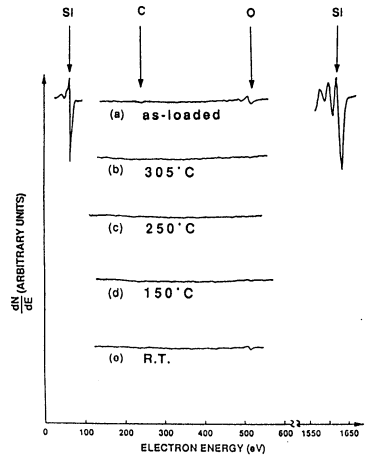


Fig.4 AES analysis of a Si(100) surface after (a) a 40:1 H2O:HF(49%) dip, and remote plasma clean at (b) 305°C, (c) 250°C, (d) 150°C, and (e) room temperature for 45 min.

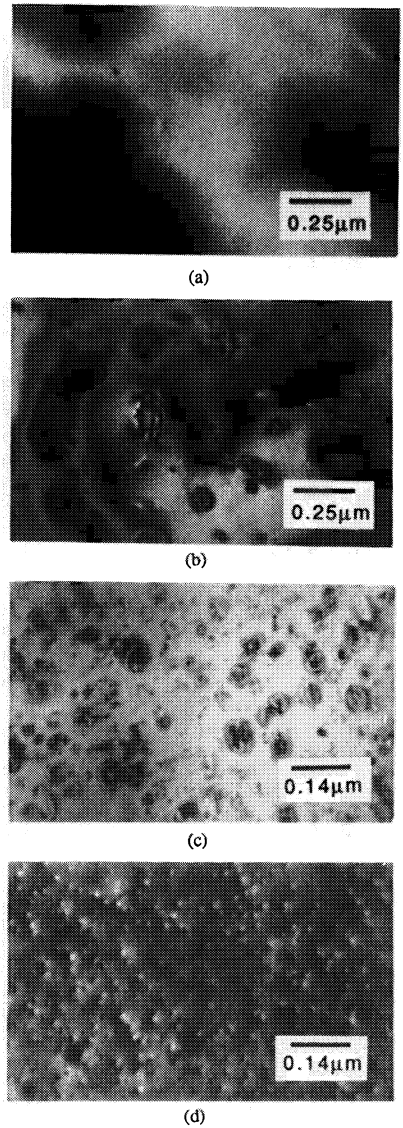
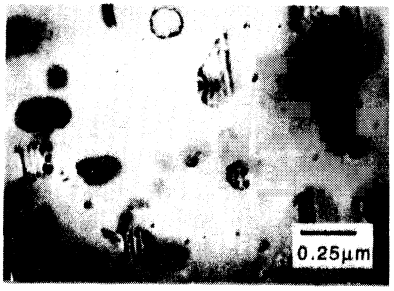
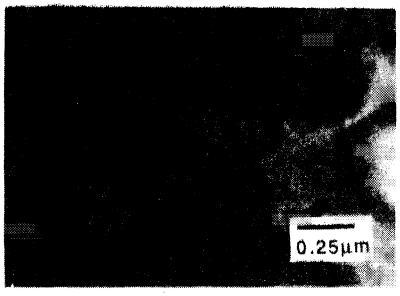


Fig.5 TEM analysis of the Si surface after the remote hydrogen plasma clean for 12 W r-f power at (a) 305°C, (b) 250°C, (c) 150°C, and (d) room temperature.



(a)

(b)



(c)

Fig.6 TEM analysis of the Si surface cleaned at 250°C and a plasma power of (a) 15W, (b) 12W, and (c) 9W by the remote hydrogen plasma clean.

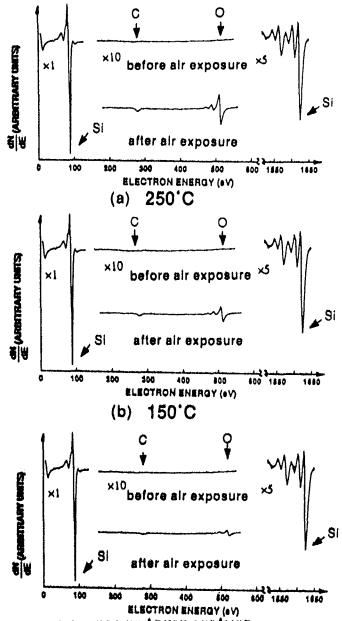


Fig.7 AES analysis of Si (100) passivated (a) 250°C, (b) 150°C, and (c) room temperature before/after 2 hour air exposure.

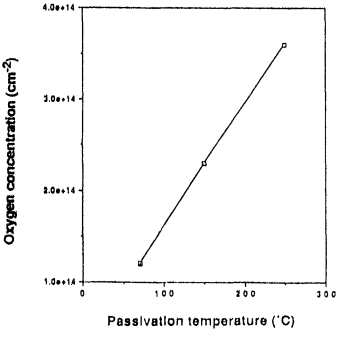


Fig.8 Readsorbed oxygen surface concentration after 2 hour air exposure as a function of passivation temperature. The data is deduced from SIMS analysis of oxygen peaks observed at the epi/substrate interface.

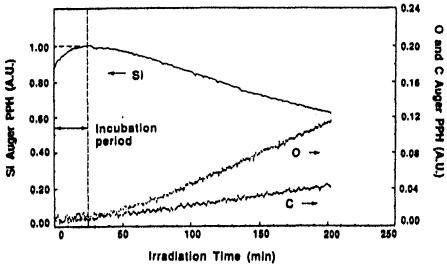


Fig.9 Time evolution of normalized Si(92eV), O(511eV), and C(272eV) Auger PPH's as a function of electron beam (3keV) irradiation time for a (3x1) H-terminated Si(100) surface.

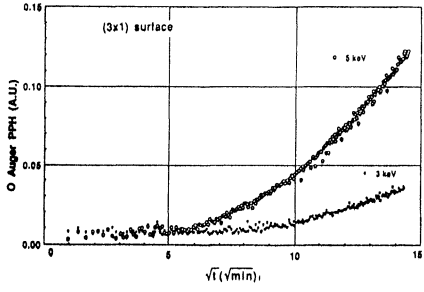


Fig.10 O Auger PPH's vs. square root of electron beam irradiation time for a (3x1) H-terminated Si(100) surface.

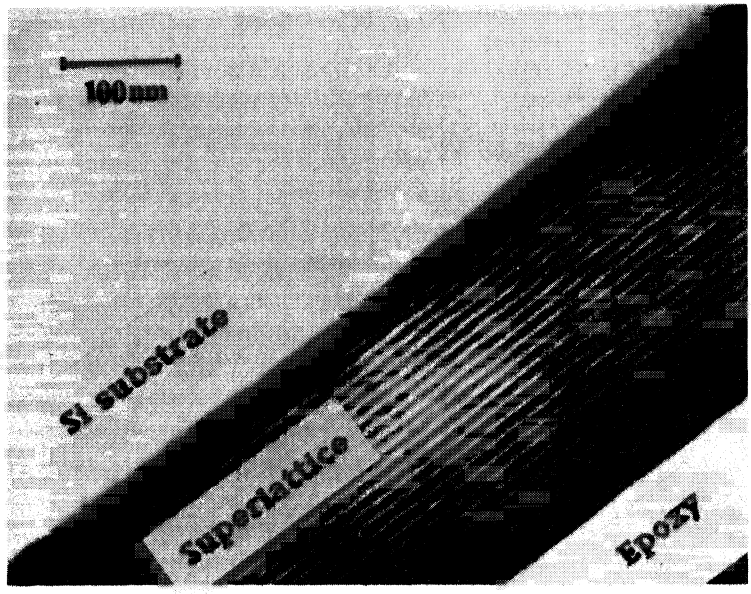


Fig.11 Cross-sectional TEM of a superlattice structure with 24 pairs of $Si/Si_{0.8}Ge_{0.2}$ layer

PRE-EPITAXIAL Si SURFACE CLEANING

James H. Comfort
IBM Research Center
Yorktown Heights, NY 10598

The advancement of epitaxial deposition techniques, in particular the extension to lower process temperatures, depends critically upon the preparation of the substrate (Si) surface immediately prior to epitaxial deposition. The fundamental issues involved include **both** the preparation and **maintenance** of a contaminant free surface prior to epitaxial growth, the most characterized of which is the presence or absence of oxygen (or oxide). In this paper we will consider the thermodynamics of the oxide/silicon system in order to set boundary conditions for maintainence of an oxide free surface. We will then consider the kinetics of in-situ surface cleaning (oxide removal) for a variety of processes including desorption, physical sputtering and chemical etching at both high (850- 1100 °C) and low (250-800 °C) processing temperatures. The kinetics of oxide removal balanced against the kinetics of oxide regrowth determine the regime of successful surface preparation for a given system while the resultant deviation from equilibrium conditions is related to the ability to maintain the clean surface. We will also consider the ex-situ preparation of a hydrogen passivated silicon surface which eliminates the need for an in-situ surface preparation step under certain processing conditions, notably those practiced in Ultra-High-Vacuum Chemical Vapor Deposition.

THERMODYNAMIC CONSTRAINTS

The thermodynamics of the $Si/O_2/H_2O/SiO_2$ system may be used to determine the fundamental limits for maintenance of an oxide-free Si surface once formed [1,2]. At any given temperature there are critical pressures of water and hydrogen above which silicon dioxide will grow. Below this critical pressure, volatile SiO will be formed and the silicon surface will effectively be etched and thus remain oxide free. Figure 1 from Lander and Morrison shows this behavior for oxygen over a wide range of temperatures. From this curve one may readily determine the partial pressure of oxygen which must be maintained in an epitaxial reactor to prevent oxide formation in the absence of kinetic barriers. Note that for 0.1 ppm oxygen in an atmospheric pressure system one would predict a minimum working tempmerature of roughly 900-950°C for defect free epitaxial growth. As discussed by Smith and Ghidini the measured critical pressures of oxygen and water reflect the balance between oxide etching and growth velocities. The balance observed for the Si(100) surface in the presence of oxygen [2].

HIGH TEMPERATURE THERMAL DESORPTION

In practice, most of the literature assumes, apriori, that there is a thin "native oxide" present on all silicon surfaces which must be removed prior to epitaxy. Figure 3 presents data from Kunii et al. on the rate of SiO2 etching observed in a hydrogen ambient such as is typically used for "prebaking" in commercial epitaxial silicon reactors [3]. The fact that the etching rate becomes negligible as the temperature nears 900°C reflects not only the sublimation kinetics but also oxidation kinetics in that particular reactor. Sedgwick and Agnello demonstrated that ppb impurity levels in an APCVD reactor allow one to reduce the oxidation rate sufficiently to allow high quality growth at temperatures as low as 700°C following a high temperature desorption step [4]. Figure 4 shows oxygen related defect densities as a function of oxygen exposure time with oxygen partial pressure as a pa-

rameter for growth from dicholorsilane at 750 °C. This illustrates the impact of background impurity levels on oxide formation in a given epitaxial reactor.

LOW TEMPERATURE OXIDE REMOVAL

At temperatures below 900°C (including "prebake") oxide sublimation becomes less effective. One may suppress oxide regrowth and utilize surface chemical treatments to produce a more volatile "native oxide" as described by Shiraki et al. but thermal cycle reduction below 800°C is limited [5]. Plasma enhancement has been explored for low temperature oxide removal by either physical (sputtering) or chemical (etching) means. Figure 5 presents data indicating that significant sputter yields are observed at elevated temperatures under conditions of low energy (< 300 eV) Ar ion bombardment [6]. In this work, however, a balance exists between the rate of damage generation induced by ion bombardment and the self-annealing rate of the Si substrate which ultimately limits this technique although some success has been reported at 250-300°C [7].

The most effective means of plasma enhanced surface cleaning at low temperatures appears to be hydrogen plasma etching [8,9]. The data shown in Figure 6 indicate that measurable quantities of silicon bearing silanes desorb at extremely low temperatures [10]. The steady stream of reactive, atomic hydrogen produced in a plasma may then be expected to etch silicon at a finite rate although the ability to actually remove oxide is not clear. Tasch et al. have recently demonstrated the ability to remove both carbon and oxygen from silicon surfaces using a hydrogen plasma preclean [9]. The Auger analysis shown in Figure 7 illustrates the effectiveness of this process for both oxygen and carbon removal.

Chemical enhancement of oxide removal using Ge has also been explored since GeO is more volatile than SiO [11,12]. Figure 8 demonstrates the efficacy of this technique by looking at the evolution of the photoemission spectrum of a heated silicon surface in the presense of water vapor for various Ge exposures. Curves (h) and (i) indicate the removal of oxide from the Si surface through Ge oxide sublimation.

HYDROGEN PASSIVATION

As noted earlier, almost all of the literature on pre-epitaxial surface cleaning assumes that a native oxide is present on any silicon surface. It is not clear, however, that this conclusion is based on direct analysis. Often times ellipsometric data taken immediately following HF exposure is used to ascertain the "native oxide" thickness. Raider et al. showed in 1975 that there is some ambiguity in the time zero oxide thickness that one might explain by proposing that there is a non-oxide adsorbed surface layer impacting the ellipsometric data. While under
many reactor conditions one may have to contend with a "native" oxide, in recent years it has become clear that a silicon surface exposed to an aqueous hydrofluoric acid (HF) treatment is hydrogen terminated and, in fact, nearly oxide free. This is demonstrated in the photoemission spectra shown in Figure 10 for both a HF treated Si surface and Si surface with a "native oxide" [13]. The lower portion of the figure indicates that the Si surface is terminated by hydrogen, not fluorine. Trucks et al. consider the chemical basis for hydrogen termination and suggest that although the HF treated surface is initially fluorinated, the polarization of the Si-F bond is strong enough to render it susceptible to displacement by hydrogen [14]. This displacement process is depicted schematically in Figure 11 and is a kinetically limited process where the forward reaction is nearly three orders of magnitude faster than the reverse (F for H) reaction.

Having prepared an oxide free surface, the second requirement for a preclean procedure is the **maintenance** of such a surface up to the onset of epitaxial growth. Takahagi et al. have examined the reactivity of a hydrogen passivated surface and shown (Figure 12) that no oxidation is detected

on the passivated surface after 2 hour air exposure [15] Meyerson et al. point out that the reactivity of the hydrogen terminated surface is nearly 13 orders of magnitude lower than a bare Si surface. They look at the thermal desorption of hydrogen from silicon (Fig. 4) and state that this surface is stable up to 400°C.

To the extent that one has a reactor which preserves hydrogen termination then the need for an in-situ cleaning procedure for oxide removal can be eliminated but one must still consider the thermodynamic arguments governing maintenance of an oxide free surface once the kinetic barrier imposed by the hydrogen is removed.

SUMMARY

The key to development of a successful pre-epitaxial Si surface treatment for oxide removal lies in understanding the thermodynamics of the Si/O2/H2O/SiO2 system as well as the kinetic barriers which govern oxide removal and formation. All of the pre-cleaning procedures proffered in the literature may be understood and characterized within this framework. Moreover, the limitations of any given technique are also defined even though the temperature regime of interest for Si epitaxy extends from near room temperature almost up to the melting point of Si.

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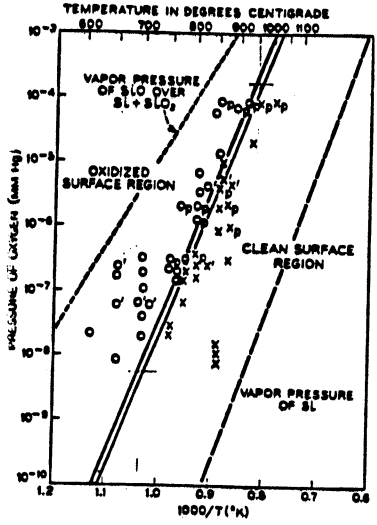

Figure 1 Oxidized and clean surface regions of silicon as a function of pressure and temperature [1].

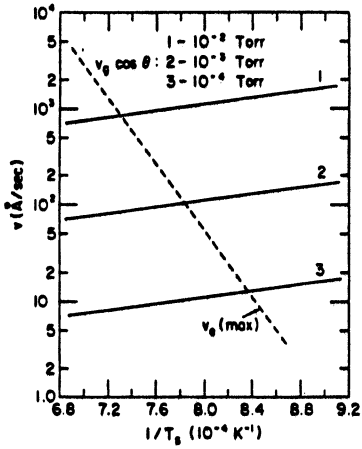

Figure 2 Growth and etching velocities, $v_g \cos \Theta$ and v_e, respectively, as functions of $1/T_S$, where T_S is the Si(100) substrate temperature. The critical conditions for growth of SiO_2 on Si(100) are determined by the intersections of the straight lines for $v_g \cos \Theta$ and v_e, yielding the critical oxygen pressure $P_c(T_S)$ above which growth of SiO_2 occurs on Si(100) as a function of T_S [2].

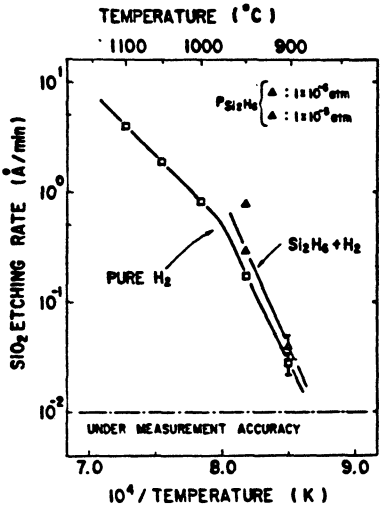

Figure 3 Dependence of the SiO_2 etching rate on temperature in pure H_2 or $SiH_6 - H_2$ ambient [3]

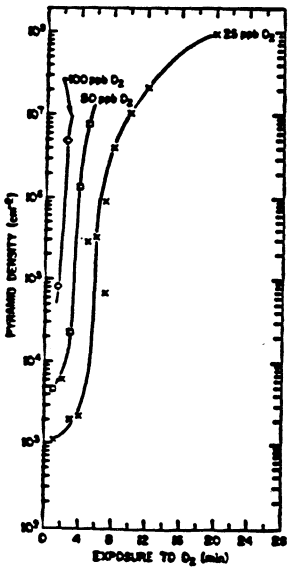

Figure 4 Oxygen related defect density as a function of exposure time to oxygen prior to epitaxial growth, with oxygen partial pressure as a parameter. Films deposited at 750 °C and 10 slm H_2 flow with 1% dichlorosilane [4].

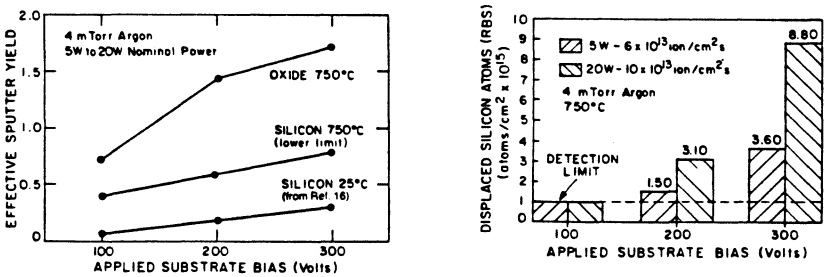

Figure 5 Left: Effective sputter yields at 750 °C for oxide and silicon vs. applied bias. Also shown are room temperature yields for silicon. Right: Areal density of displaced silicon atoms detected by RBS in near-surface region of substrate after sputtering [6].

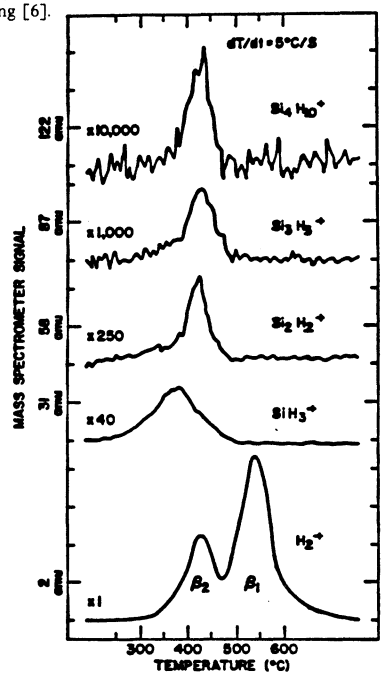

Figure 6 TPD of H_2, SiH_3, Si_2H_2, Si_3H_8, and Si_4H_{10}, measured in one esperiment in which the Si(100)-(2X1) surface at 80 °C was exposed to 10,000 arbitrary units of H atoms. This produces the (1X1) bulk terminated surface. The sample temperature was then programmed at 5 °C second and the signals were recorded using an electron impact energy of 70 eV in the QMS ionizer [10].

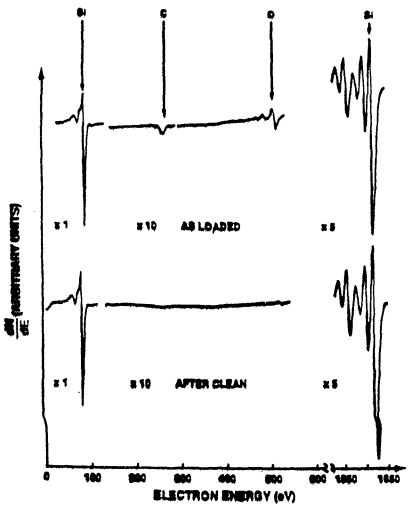

Figure 7 Auger analysis of effectiveness of a hydrogen plasma Si surface clean; 45-100 mTorr, 250-300 °C, 30-45 min, 7-12 Watt, 200 sccm H_2 flow.

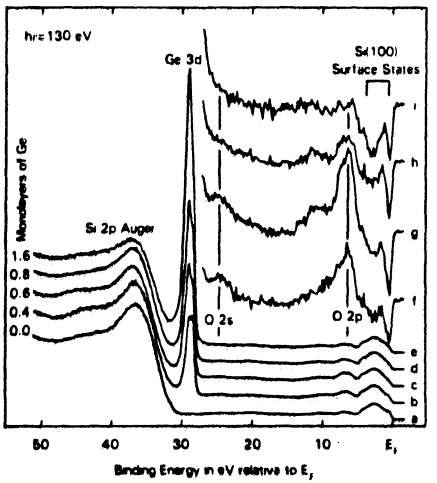

Figure 8 Curve (a) is a broad sweep photoemission spectrum of a clean well ordered Si (100) surface. Curves (b) through (e) show the same surface with increasing amounts of Ge deposited on a heated sample surface in the presence of water vapor. Curves (f) through (i) were obtained after subtraction of curve (a) from curves (b) through (e). These spectra illustrate the removal of oxygen from a heated silicon surface via reaction with adsorbed Ge, and the subsequent sublimation of resulting Ge oxides [12].

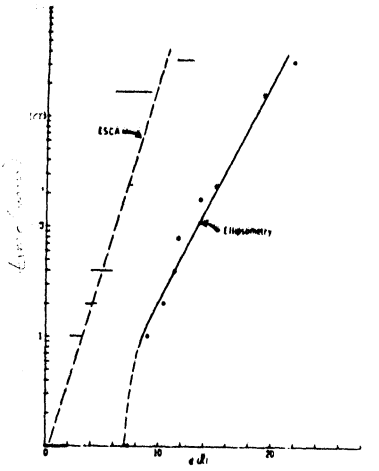

Figure 9 Ellipsometric and ESCA data plotted as a function of the logarithm of the time of exposure of etched samples to air at room temperature [16].

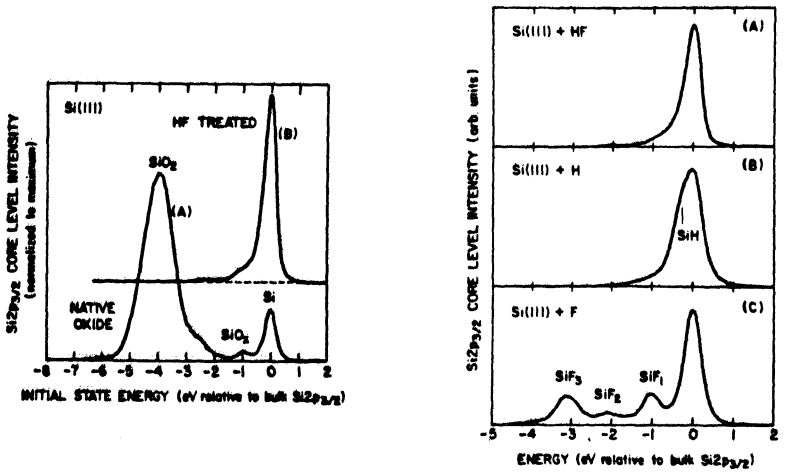

Figure 10 Left: Si 2p core level photoemission spectra for the case of: (a) Si (111) in as-received condition, (b) 10:1 dilute HF etched Si (111) after 10 min in air. Data were taken at a photon energy of 130 eV where the surface sensitivity is greatest. The $2p_{1/2}$ spin-orbit component and secondary electron background is subtracted. Similar results are obtained for Si (100). Right: Si $2p_{3/2}$ core level spectra from HF-etched Si (111), compared with Si (111) covered with a monolayer of hydrogen and fluorine. These spectra show that Si is mainly bonded to hydrogen (not to fluorine) on the HF passivated surface [13].

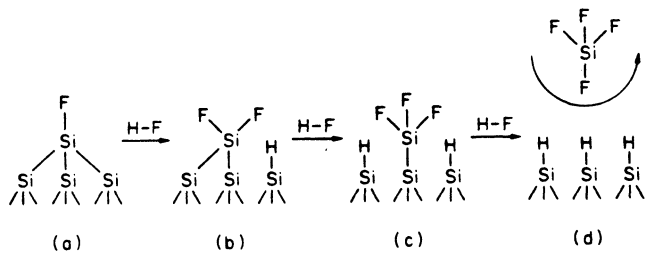

Figure 11 Schematic representation of the mechanism of H passivation [14].

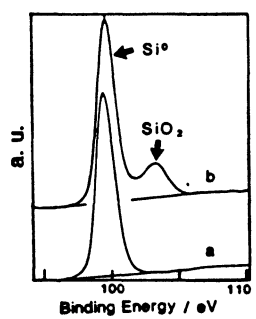

Figure 12 Si2p spectra of silicon crystals exposed to the air for 2 *h* after (a) UV HF cleaning and (b) conventional high temperature treatment in UHV [15].

CLEANING EFFECTS OF MOLECULAR PRE-SHOWERING ONTO SILICON SURFACE ON LOW-TEMPERATURE Si EPITAXY

K.Yamada, T.Ohmi, M.Morita, H.Suzuki and C.M.Soh.

Department of Electronics, Faculty of Engineering,
Tohoku University
Sendai 980, Japan

ABSTRACT

Gas molecules pre-showering onto a Si substrate surface right before low-temperature Si epitaxy using Si_2H_6 is experimentally demonstrated to suppress oxide growth caused by H_2O and O_2 gas molecules in chemical vapor deposition (CVD) reactor. Using Si_2H_6 molecular-flow pre-showering, high-quality in-situ phosphorus-doped Si films are obtained at a low temperature of 550 °C. PH_3 molecular-flow pre-showering is also effective to suppress the oxide growth on the Si surface and the epitaxial growth of in-situ phosphorus-doped Si films is also achieved at a low temperature of 535 °C.

INTRODUCTION

The precise control of dopant impurity profiles in fine structures is required for realizing high-performance ultra-large-scale integrated (ULSI) devices, such as high speed bipolar transistors having a thin base layer and abrupt doping profiles. In-situ doped Si epitaxy at low temperatures is one of the attractive technologies (1),(2). In Si epitaxy, it is essential to keep a Si substrate surface clean, especially to suppress the oxide growth on the Si surfaces prior to Si epitaxial growth, because the oxide impedes the epitaxial growth (3),(4). Thermal cleaning of the Si substrate surface at temperatures of 800 °C or higher is usually employed to eliminate the oxide before Si epitaxial growth. However, thin and abrupt doping profile is difficult to achieve because of impurity diffusion at high temperatures. Thus, low-temperature pre-cleaning is required.

Si epitaxial films are reported to be grown at the temperature as low as 550 °C using the ultrahigh vacuum chemical vapor deposition technique (1),(3). Low-temperature epitaxial growth requires ultrahigh vacuum to remove oxide but it may induces Si etching and surface

roughening (5). The surface microroughness before the epitaxial growth is well reflected on the surface after epitaxial growth (6). It is, therefore, necessary to suppress oxide growth and to keep the substrate surface smooth in the pre-cleaning process.

In this paper, we propose a cleaning method using molecular pre-showering onto Si substrate surfaces and describe the effects of Si_2H_6 or PH_3 gas molecules pre-showering on the suppression of oxide growth and low-temperature Si epitaxy.

EXPERIMENTAL

Si film formation was carried out with the CVD system using Si_2H_6 molecular flow (7),(8). This system is characterized as follows : source gas is introduced into the reaction chamber at free-jet molecular-flow through a gas nozzle with a diameter of 500μm and a length of 1mm. Si substrate surface is preferentially heated with the irradiation of Xe short-arc lamp set above the chamber. A high-vacuum pumping system, an ultraclean-gas supplying system and substrate transporting by the loadlock mechanism with electrostatic chuck make possible the process environment clean.

Si substrates used in these experiments were boron-doped p-type(100) CZ Si wafer (33 mm in diameter) with the carrier concentration of 10^{15} cm^{-3}. The Si substrate was set face-up on the Si susceptor in the reaction chamber after wet chemical cleaning, which had been newly improved to keep Si surface smooth (9). The Si substrate was heated by Xe short-arc lamp irradiation to the substrate surface. Si film formation was carried out under the condition as shown in Fig.1. A solid line shows deposition process with Si_2H_6 gas molecular-flow pre-showering and a dotted line shows that without the pre-showering. Film deposition temperatures were 535 and 550 °C. Si_2H_6 and PH_3/Ar(2%) gas pressures were 0.40 mTorr and 0.25 mTorr, respectively. Deposited film quality was evaluated by reflection high energy electron diffraction (RHEED). Thickness of thin oxide layer was measured by x-ray photoelectron spectroscopy (XPS) (10). Microroughness of Si substrate surface was observed by a scanning tunneling microscope (STM) right after removal of oxide using diluted HF etching. Partial pressures of H_2O and O_2 gas molecules were monitored by a quadrupole mass spectrometer.

RESULTS AND DISCUSSION

Oxide growth on Si surfaces before epitaxy

Figure 2 shows the thickness of oxide layer grown on the Si surface in high vacuum for the heating-up period, where the heating process was carried out as follows :

1. the substrate was heated up from room temperature to 535, 600 or 700 °C for 20 minutes.
2. the substrate temperature was kept constant for 10 minutes.
3. the substrate was cooled down to room temperature for about 90 minutes.

The oxide is thicker as the substrate temperature is higher. This result means that the oxide grows on the Si surface placed in the high vacuum (base pressure:8×10^{-9} Torr) during heating the Si substrate up to deposition temperatures between 535 and 700 °C. The oxide growth is considered to be caused by H_2O (partial pressure:10^{-9} Torr) and O_2 (10^{-11} Torr) (11). Figure 3 shows STM images of the Si substrate surface (a)placed in the high vacuum without heating and (b)heated up to 700 °C in the high vacuum. The microroughness of the Si surface increases with an increase of the temperatures. From the results shown in Figs.2 and 3, it is seen that the heating process at temperature between 535 and 700 °C in high vacuum causes quality degradation of the Si surface.

Si_2H_6 gas pre-showering

Figure 4 (a) and (b) show RHEED patterns of phosphorus-doped Si films deposited with and without Si_2H_6 gas molecular-flow pre-showering, respectively. The temperature starting Si_2H_6 pre-showering is 520 °C, which is almost thermal desorption temperature of hydrogen terminating Si atoms on an Si substrate surface (12), and the Si_2H_6 pressure was about 10^{-5} Torr at the pre-showering stage. The deposition temperature and the deposited film thickness were 550 °C and 0.2μm, respectively. It is obvious that the quality of the Si film formed with the pre-showering is improved in contrast with that of no pre-showering. This is considered to be due to suppressing the oxide growth on a clean Si surface right before film deposition stage by pre-showering. The suppression of the oxide growth is supposed to come from that Si_2H_6 gas molecule adsorption onto an Si surface is dominant compared with H_2O molecule adsorption because partial pressure of Si_2H_6 (10^{-5}Torr) is larger than that of H_2O (10^{-9}Torr) during the pre-showering.

Figure 5 shows RHEED patterns of phosphorus-doped Si films for various temperatures starting Si_2H_6 pre-

showering. The deposition temperature, the gas pressure and the film thickness were the same as above condition. The Si_2H_6 pre-showering starting at lower temperatures contributes little improvement of the film quality. This result indicates that several atomic layers of Si films having an imperfect crystallinity grows on the substrate surface during the pre-showering in the low temperature region, such as temperatures between 410 and 520 °C. It is adequate that Si_2H_6 pre-showering is started at the temperature at which thermal desorption of hydrogen terminating Si atoms on substrate surface occurs.

PH_3 gas pre-showering

Figure 6 shows the thickness of oxide grown on the Si substrate surface during PH_3 or H_2 gas showering throughout the heating process mentioned above. The thickness of oxide for PH_3 showering is thinner than that for H_2 showering. This result shows that PH_3 showering is very effective to suppress the oxide growth while H_2 showering is not effective. This is considered to be caused by that PH_3 gas molecules easily adsorb onto an Si surface compared with H_2 molecule, because PH_3 molecule has a dipolemoment of 1.935×10^{-30} C·m and a thermal decomposition temperature as low as 375°C (13).

Figure 7 shows Si film formation process with PH_3 gas pre-showering to suppress oxide growth on the Si surface before Si film deposition. A dotted line indicates PH_3 gas pressure and a solid line indicates Si_2H_6 pressurre. Figure 8 (a) and (b) shows RHEED patterns of the phosphorus-doped Si films deposited at 535 °C with and without the PH_3 pre-showering, respectively. The pattern of the film deposited with the PH_3 pre-showering indicates Kikuchi line weakly. The crystallinity of the deposited film is improved by the PH_3 pre-showering. This result comes from suppressing the oxide growth by PH_3 gas molecule pre-showering right before film deposition.

CONCLUSIONS

We have demonstrated that the molecular-flow pre-showering onto a Si substrate surafce makes pre-cleaning and growth temperatures of Si epitaxy lower, because the pre-showering is effective to suppress the oxide growth on the Si surface. High-quality epitaxial Si films are obtained at a low temperature of 550 °C employing Si_2H_6 molecular-flow pre-showering. PH_3 molecular-flow pre-showering enables the epitaxial growth of Si films at a low temperature of 535 °C.

ACKOWLEDGEMENTS

The authors wish to thank Associate Professor T. Shibata and Associate Professor J. Murota for useful discussions and suggestions. This study was carried out in the Superclean Room of Laboratory for Microelectronics, Research Institute of Electlical Communication, Tohoku University.

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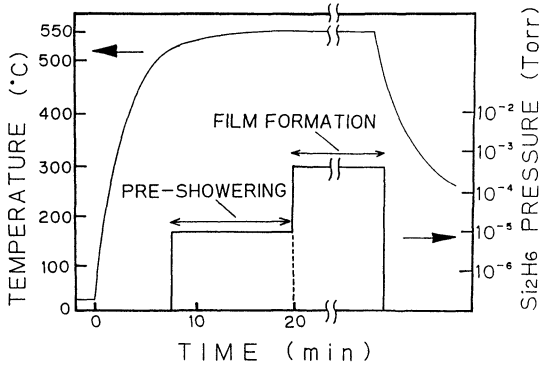

Fig.1 Temperature and Si_2H_6 pressure profiles of film formation process. The solid line (——) in the Si_2H_6 pressure profile shows the deposition process with pre-showering and the dotted line (---) shows deposition process without it.

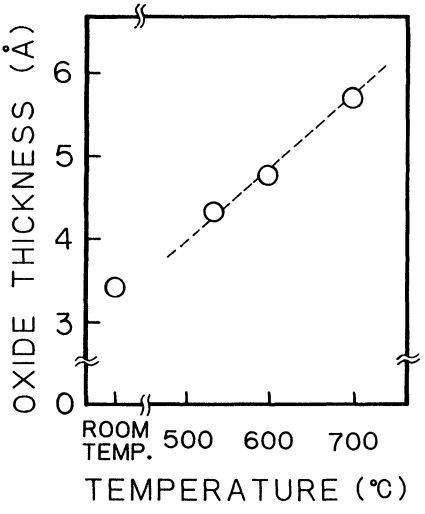

Fig.2 Thickness of oxide layer grown on Si surface during heating Si substrate up to film formation temperature in high vacuum.

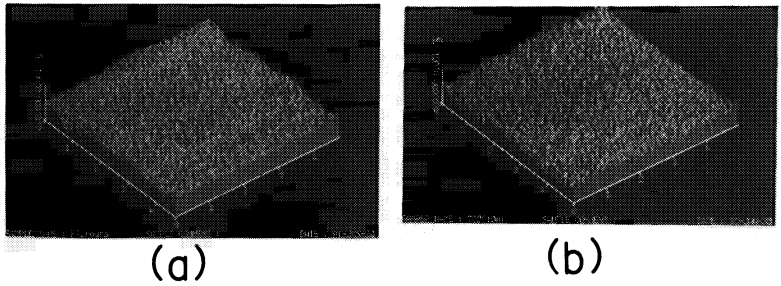

Fig.3 STM images of Si substrate surfaces (a) placed in high vacuum ($8x10^{-9}$Torr) at the room temperature for 2 hours and (b) heated up to 700°C in high vacuum ($3x10^{-8}$ Torr) for 10 minutes.

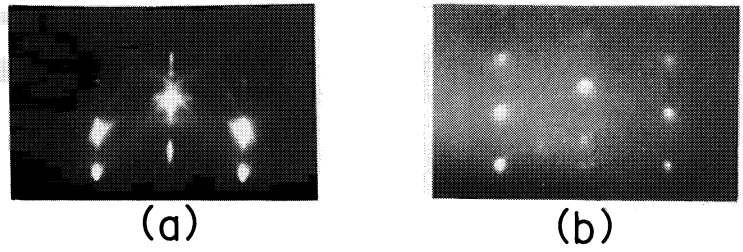

Fig.4 RHEED patterns of phosphorus-doped Si films deposited (a) with pre-showering at Si_2H_6 molecular-flow and (b) without pre-showering. The deposition temperature is 550°C.

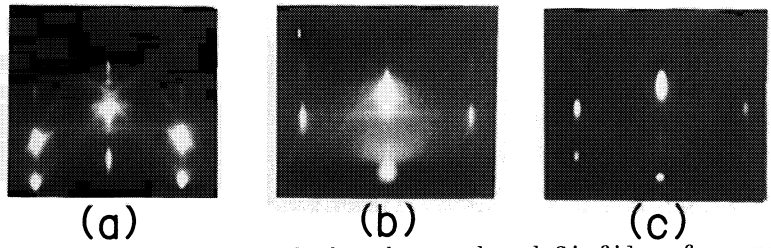

Fig.5 RHEED patterns of phosphorus-doped Si films for pre-showering start temperature of (a) 520°C (b) 450°C and (c) 410°C. The deposition temperature is 550°C.

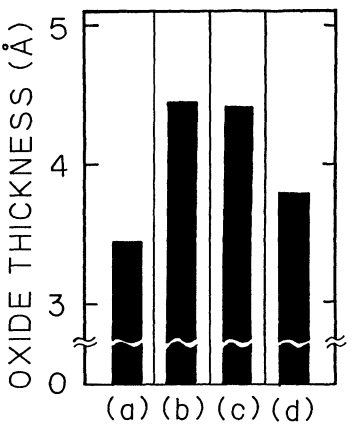

Fig.6 Thickness of oxide layer grown on the Si substrates (a) in high vacuum at room temperature for 2 hours, (b) in high vacuum during heating up to 535 °C, (c) with H_2 gas showering during heating up to 535 °C and (d) with PH_3 gas showering during heating up to 535 °C.

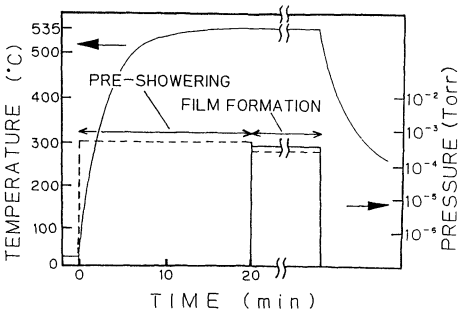

Fig.7 Temperature and pressure profiles of film formation process. A dotted line (---) indicates PH_3 gas pressure and a solid line (——) indicates Si_2H_6 pressure.

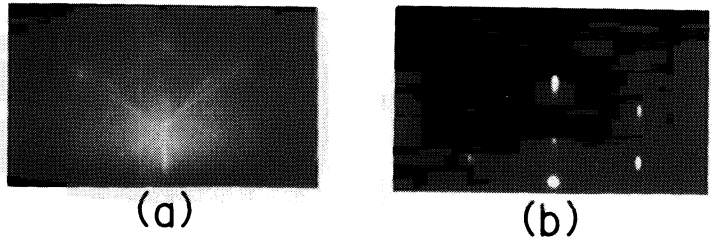

Fig.8 RHEED patterns of phosphorus-doped Si films formed at 535 °C (a) with and (b) without PH_3 gas pre-showering.

THE HYDROGEN-TERMINATED SILICON (100) SURFACE AND ITS ROLE IN THE SUCCESSFUL ACHIEVEMENT OF SILICON EPITAXY AT LOW TEMPERATURES

D. Kinosky, B. Anthony, T. Hsu, R. Qian, J. Irby,
S. Banerjee, and A. Tasch
Department of Electrical and Computer Eng., University of Texas,
Austin, TX 78712

The hydrogen-terminated Si(100) surface is shown to play a critical role in the achievement of low temperature Si epitaxy by Remote Plasma-enhanced Chemical Vapor Deposition (RPCVD). The remote hydrogen-plasma treatment is employed in the dual role of cleaning and passivating the Si surface. We have studied both the effectiveness of the remote H-plasma clean in establishing a clean surface on (100) Si, and the inertness of the H-terminated surface after exposure. The H-passivated surface prevents contamination by oxygen and carbon under Ultra High Vacuum (UHV) conditions and for up to 2 hours in air.

INTRODUCTION

The establishment and maintenance of a clean, defect-free surface is a critical requirement for successful epitaxial growth. In conventional Si epitaxy this is achieved by heating the substrate to high temperatures at which surface oxygen desorbs as volatile SiO. This oxygen-free surface can be maintained indefinitely at high temperature due to the thermodynamic instability of SiO_2 under the conditions of low oxygen partial pressure. However, at low temperature an initially clean Si surface is highly reactive and will quickly adsorb oxygen, even under UHV conditions. In order to develop a true low-temperature epitaxial growth process, one must also develop a low-temperature *in situ* cleaning technique consistent with the Ghidini-Smith curves [1]. Hydrogen passivation of the Si surface has been found to be capable of preventing or reducing readsorption of oxygen by satisfying Si dangling bonds on the surface at low temperatures [2]. Actually, the H-terminated Si surface is stable only at low temperatures; for temperatures above approximately 460°C, hydrogen will thermally desorb from the Si surface [3]. We have developed a remote hydrogen plasma clean at 250°C which effectively removes carbon, nitrogen and oxygen from a pre-treated silicon surface [4], and produces a hydrogen terminated surface with very few crystalline defects. The H-terminated surface is resistant to the adsorption of oxygen and other contaminants. In RPCVD, wafers are prepared with a two-step clean which takes advantage of the H-passivated surface. Wafers are given an *ex situ* RCA clean and HF dip followed by an *in situ* remote H plasma clean. After the *ex situ* clean, the Si surface is almost free of oxygen, and the surface is dihydride terminated with a (1x1) reconstruction as observed by Reflection High Energy Electron Diffraction (RHEED). The HF treated surface is sufficiently clean to support the growth of epitaxial films without any other treatment. However, some oxygen and carbon are adsorbed during transport of the wafers to the RPCVD system. An *in situ* remote H plasma clean is therefore used in addition to the HF dip to reduce the C and O contamination, as confirmed by Auger Electron Spectroscopy (AES) analysis. The degree to which the (100) Si surface is passivated against oxygen adsorption depends on the nature of the H bonding and on the surface reconstruction. It has been found that these parameters can be reproducibly established by controlling the substrate temperature at which the H-passivation occurs. For cleans performed below 300°, the surface is (1x1) or (3x1) indicating dihydride or a

mixture of di- and monohydride termination, respectively. For cleaning temperatures above 350°C the surface is (2x1), indicating monohydride termination only. We find lower temperature H plasma treatment to result in better passivation.

EXPERIMENTAL

The RPCVD system in which the remote hydrogen plasma treatment is performed has been described elsewhere [5]. This system consists of three chambers: a load-lock chamber, a surface analytical chamber equipped with an AES system used for *in situ* measurement of surface contamination, and a process chamber for wafer surface cleaning and epitaxial deposition. Background oxygen and water partial pressures in the cleaning and deposition chamber are $1x10^{-10}$ and $2x10^{-9}$ Torr, respectively, or lower. A RHEED system is located in the process chamber for *in situ* measurement of surface crystallinity after completion of the process. The remote H plasma treatment is accomplished by generating atomic hydrogen via excitation of 200 sccm hydrogen flow passing through an inductively-coupled rf plasma (13.56 MHz). The wafer is not in the glow region, and Langmuir probe measurements reveal a negligible ion concentration, (below 10^8 cm^{-3}). Typically, the plasma power is 9 W, and the process pressure is 45 mTorr. During the clean, the wafer temperature is maintained at 250°C by heating from the backside using a pair of quartz infrared lamps. The duration of a typical clean is 45 min. *Ex situ* preparation of the wafers consisted of ultrasonic solvent degrease, RCA clean, and a 30 sec. 10:1 H_20:HF dip. The wafers were then immediately loaded into the load-lock via a nitrogen-purged glove box, and the load-lock chamber was subsequently evacuated to UHV without requiring bakeout. The total time between HF dip and chamber evacuation is about 10 min. The wafers used were p-type (100) Si with resistivities of 10-15 ohm-cm.

RESULTS and DISCUSSION

The efficiency of the removal of adsorbed O and C by the remote H-plasma has been found to increase with wafer temperature in the range of room temperature to 305°C. The oxygen AES peak (KLL: 511 eV) from the wafer cleaned at room temperature showed the largest peak-to-peak height (PPH). The oxygen PPH decreased with increasing substrate temperature and completely disappeared below the AES detectability limit of 0.1-1 atomic% at temperatures above 250°C. Additionally, wafers cleaned using 9W plasma power at substrate temperatures lower than 250°C have been observed by Transmission Electron Microscopy (TEM) to have dislocation loops at the surface. If the wafer temperature during clean is raised to 250°C or greater (for 9W power), the occurrence of these defects fell below the TEM detection limits (10^5 cm^{-2}). However, as is demonstrated in this study, passivity of the cleaned surface varies inversely with the temperature at which the H-plasma treatment takes place. For routine cleaning of wafers prior to RPCVD epitaxy, 250°C is considered as the optimal temperature for producing a clean, defect-free, well-passivated surface. Further details of the H-plasma clean can be found in references [4] and [6].

RHEED analysis of wafers cleaned using the remote hydrogen plasma clean at 250°C shows third-order streaks (Figure 1a) indicative of a (3x1) reconstruction pattern. This (3x1) pattern is consistent with the observations of Chabal [7] and Boland [8] for a silicon (100) surface exposed to atomic H. If the wafer is then heated to 305°C or above, desorption of some of the hydrogen occurs, and the (3x1) reconstruction pattern transforms to a (2x1) reconstruction pattern (Figure 1b). The (2x1) surface also results if the clean is performed at 305-400°C. The (3x1) hydrogen-passivated Si surface is due to an alternating monohydride and dihydride termination [8,9]. The (2x1) reconstruction pattern shown in Fig. 1b is the pattern expected for a monohydride-terminated surface, in which case, the

surface dimer atoms share two bonds. RHEED analysis showed that the (3x1) and (2x1) patterns do not change when the samples cool to room temperature, and that these reconstructed surfaces resulting from the remote H plasma clean were stable under UHV conditions. Wafers that were allowed to remain in vacuum for 24 hours after cleaning showed no increase in carbon or oxygen based on AES analysis. As mentioned in the introduction, the *ex situ* HF dip results in a (1x1) RHEED pattern (Figure 1c). The same diffraction pattern is observed if the remote H plasma clean is performed at temperatures less than 190°C. This (1x1) hydrogen terminated surface is attributed to dihydride termination by Boland from Scanning Tunneling Microscope studies [8]. As is the case for the (3x1) reconstruction pattern, if a (1x1) reconstructed sample is heated to >305°C, the surface reconstruction is transformed to the (2x1) pattern.

The passivating effect of the remote H plasma clean at 250°C has been studied by exposing cleaned wafers to room air and observing the change in carbon and oxygen contamination using AES analysis. Auger spectra taken immediately after the H plasma clean showed no detectable carbon or oxygen. Figure 2 shows Auger spectra for wafers subjected to the remote H plasma clean and subsequently exposed to air for (a) 15 minutes, (b) 2 hours, and (c) 10 hours. The carbon and oxygen contamination were seen to increase steadily with the duration of exposure to air, and the best results were obtained when exposure time is limited to a few minutes. RHEED analysis after air exposure showed that the third-order streaks were maintained for the samples exposed for 15 min. and 2 hours, but only integral order streaks were apparent for the sample exposed to air for 10 hours.

By contrast, the HF dipped samples showed a (1x1) RHEED pattern after 15 minutes, 2 hours, and 10 hours air exposure. Again, the carbon and oxygen contamination were seen to increase with the time of exposure to air. Comparison of AES spectra for wafers exposed to air after the remote H plasma clean and after the HF dip is complicated by the fact that the silicon peaks for the wafers analyzed after the *in situ* clean/air exposure are smaller than for the wafers analyzed after the HF dip/air exposure wafers. However, taking the relative peak heights into account, the remote H plasma clean appears to be slightly more effective than the HF dip in passivating the surface. After AES analysis was performed on the wafers, they were cleaned *in situ* using the remote H plasma clean to determine if the accumulated contamination could be removed. Auger spectra after the *in situ* clean are shown in Figure 3 for exposure times of (a) 15 min, (b) 2 hrs, and (c) 10 hrs. In all cases the *in situ* clean was effective in removing carbon contamination caused by the air exposure, but only for the wafer exposed to air for 15 minutes was the clean effective in significantly reducing the oxygen contamination.

In order to investigate the temperature dependence of hydrogen passivation, a two-step H-plasma treatment was used for *in situ* wafer preparation. The wafers were first cleaned by remote H-plasma at 250°C for removal of O and C. The wafers were then subjected to a passivation step in which the nature of the H-termination of the surface was varied by changing the substrate temperature at the end of the clean, while maintaining the hydrogen plasma. Three wafers were passivated at 250°C, 150°C, and room temperature for 20 minutes. An additional sample was prepared by remote plasma H-clean followed by complete desorption of the hydrogen by heating the wafer to 500°C in UHV for 10 min. After the cleaning and passivation treatment, the wafers were removed from the chamber and exposed to air in a laminar flow clean hood for 2 hours. The results of AES analysis on the Si surfaces before and after a 2-hour air exposure are shown in Fig. 4. No detectable oxygen (KLL:511 eV) peaks were observed on any of the three passivated wafers before air exposure (i.e. after cleaning/passivation), indicating an effective cleaning step. After a

2-hour air exposure, oxygen peaks were seen on all four wafers with different PPHs. As expected, the largest oxygen PPH was observed on the H-desorbed, unpassivated wafer (heated to 500°C). Small carbon and nitrogen peaks were also seen. The rapid appearance of these contaminants under UHV conditions, in particular nitrogen, demonstrates the high reactivity of the unpassivated Si surface. Background partial pressures of H_2O, O_2, CO_2 and N_2 are $2x10^{-9}$, $1.5x10^{-11}$, $1.4x10^{-10}$, and $5x10^{-10}$, respectively. As can be seen in Fig. 4, the LMM:92 eV Si peak has decreased in amplitude substantially with respect to the higher energy Si peak (KLL:1619 eV). This is consistent with the minimum mean free path for inelastic scattering of electrons near 100 eV of electron energy. The peak did not shifted in energy indicating that the oxygen was adsorbed only, and that the suboxide has not formed. A comparably large oxygen PPH was found on the wafer passivated at 250°C. The decrease of the oxygen PPH with passivation temperature suggests that better H passivation is achieved at the lower passivation temperature. This trend is in agreement with an earlier study on the passivating effect of exposure of a Si (100) surface to atomic H by Hirayama and Tatsumi. [10]. It was found that H exposure at temperatures less than 200°C resulted in significantly less adsorbed oxygen than for wafers without this treatment when the wafers were exposed to air for 12 hours. The superiority of the passivation capability of the (1x1) surface over the (3x1) surface observed in this experiment suggests that the (1x1) surface observed here is due to an ordered dihydride coverage, since the hydrogen coverage is greater for a dihydride surface than for an alternating monohydride and dihydride surface (which causes a (3x1) reconstruction). The surface structures of these H-passivated Si surfaces are found to be stable even under air exposure as indicated by the RHEED patterns taken from the three wafers after 2 hours air exposure.

Secondary Ion Mass Spectroscopy (SIMS) analysis was used to quantify the amount of oxygen at the substrate-film interface of films deposited after a H plasma treatment and air exposure. Figure 5 shows oxygen concentration for a typical RPCVD epitaxial Si film deposited on a wafer prepared by an RCA clean, dilute HF dip, and *in situ* remote H plasma clean at 250°C. Carbon and oxygen concentrations at the film/substrate interface were found to be $\sim 1x10^{12}$ and $5x10^{12}$ cm^{-2}, respectively. As in the AES study, three wafers were cleaned with the remote H-plasma at 250°C, then passivated via remote H-plasma at temperatures of 75°C, 150°C, and 250°C. A fourth wafer was H-plasma cleaned, then desorbed of hydrogen by heating to 500°C for 10 min. under UHV. The wafers were removed from the vacuum system and exposed to room air for 2 hours. The wafers were then reloaded into the system, and 1000Å Si films were deposited by RPCVD at 305°C without any additional cleaning. The oxygen content at the substrate-film interface as evaluated by SIMS for the passivated films is shown in Fig. 6. The interfacial oxygen concentration was seen to increase monotonically with passivation temperature. The Si surface passivated at room temperature showed an oxygen coverage as low as $1.2x10^{14}$ cm^{-2} which corresponds to ~0.1 monolayer if we note that a monolayer of coverage is $1.4x10^{15}$ atoms cm^{-2} for a (100) Si surface. The fact that lower temperatures give better passivation as observed in this experiment may be explained by the lower hydrogen desorption rate at lower temperature [3], which, in turn, results in higher hydrogen coverage, and hence better passivation. This result was also supported by RHEED analysis. The Si surface passivated at 250°C showed a (3x1) surface reconstruction, while the surfaces passivated at 150°C and room temperature show a (1x1) pattern. For the H plasma clean performed at 250°C, it was found that the interfacial O concentration was $3.6x10^{14}$ cm^{-2} (~0.5 monolayers) after 2 hours exposure in air. This corresponds to an average O adsorption rate of $\sim 5x10^{10}$ $cm^{-2}s^{-1}$. The passivating effect of surface hydrogen

is also observed by the routine procedures used in RPCVD. After loading the wafers into the load-lock chamber it is common for the wafers to be stored for as long as 4-5 days before processing. There is insignificant buildup of O or C contamination on the as-loaded surface even upon extended storage in the load-lock chamber. Also, after wafers are prepared with the remote H plasma treatment, they are transferred to the surface analysis chamber for AES and then transferred back to the deposition chamber. This process can take up to 30 minutes, and the wafer temperature is ~100-200°C. Wafers prepared in this manner have been found to have interfacial O concentrations of ~$6x10^{12}$ cm^{-2} (Fig. 5), or 0.01 monolayers. We can therefore conclude that the H passivated surface is highly resistant to O and C adsorption.

The effect of the the H-passivation temperature on the crystallinity of films grown on substrates which had been exposed to air for 2 hours.is shown in Fig. 7. RHEED patterns of the Si films deposited for the SIMS study showed a tendency for the pattern to change from streaks to spots with increasing passivation temperature, indicating a roughening of the surface. In contrast to the single crystal films grown on passivated substrates, the film grown on the substrate desorbed of hydrogen at 500°C was polycrystalline, demonstrating the negative effect on epitaxy exercised by contaminants.

At temperatures above 550°C, it has been found by temperature programmed desorption that all of the H is removed from the Si (100) surface [3]. Therefore, epitaxy processes which operate in the 550°C-750°C temperature range have no intrinsic means of protecting the film-substrate interface once the wafer is at the growth temperature. Indeed, it has been reported that the UHV-CVD approach does not work in the 650°C - 750°C temperature range since the contamination of the interface occurs before growth is initiated [11]. The protection afforded by the H termination of Si surfaces below 450°C makes this temperature range very attractive for low-temperature Si epitaxy by CVD. Figure 8 illustrates the temperatures and conditions which minimize the adsorption of oxygen and carbon (100) Si wafers. Using RPCVD, single crystal growth rates as high as 50Å/min at 450°C have been achieved, indicating that even at these low temperatures there is sufficient adatom energy to grow single crystal films.

CONCLUSION

The low-temperature (250°C) remote plasma hydrogen clean that we have developed has been shown to serve an additional, highly important purpose of passivating the silicon surface. The wafers receive an *ex situ* wet chemical clean followed by a dilute HF dip. After the HF dip, the wafers are immediately transferred to the processing system via a UHV load-lock chamber. After the HF dip, a (1x1) reconstruction of the surface is observed which we believe to result from dihydride termination. This surface has been found to be resistant to absorption of O and C during transfer and loading of the wafers from the wet clean area to the load-lock chamber. Prior to processing, the wafers are subjected to an *in situ* remote H-plasma clean and passivation in which the wafer is exposed to atomic hydrogen. The passivated surface is found to be most resistant to adsorption of O and C when the passivation occurs at room temperature. We believe this to be correlated to the greater hydrogen coverage established at the lower passivation temperature. Additionally, the remote H-plasma passivated surface was found to be slightly more resistant to adsorption of contaminants onto a clean surface when compared to the surface resulting from the HF dip.

This work was supported by ONR/SDIO Contract N00014-87-K-0323, and by the NSF Science and Technology Center at the University of Texas Contract CHE8920120.

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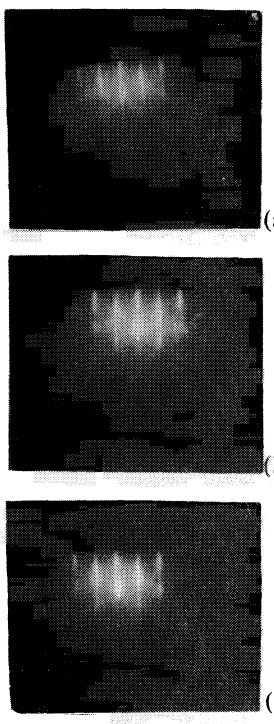
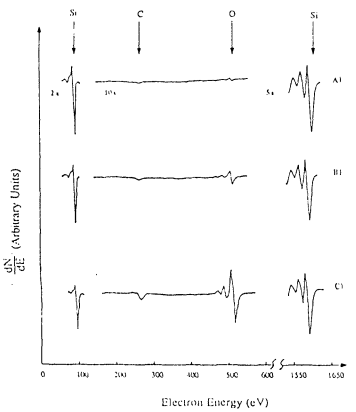


Figure 1. RHEED patterns of (100) Si surface after remote H-plasma clean at (a) 250°C (3x1), (b) 305 °C (2x1), and (c) room temperature (1x1).

Figure 2. AES of Si (100) after H-plasma clean and subsequent air exposure of (a) 15 min., (b) 2 hr. and (c) 10. hr. The oxygen peak is seen to increase with exposure time.



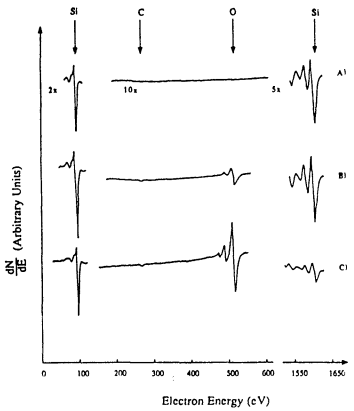


Figure 3. AES of Si after HF dip and subsequent air exposure of (a) 15 min., (b) 2 hr. and (c) 10. hr., then H-plasma cleaned at 250°C.

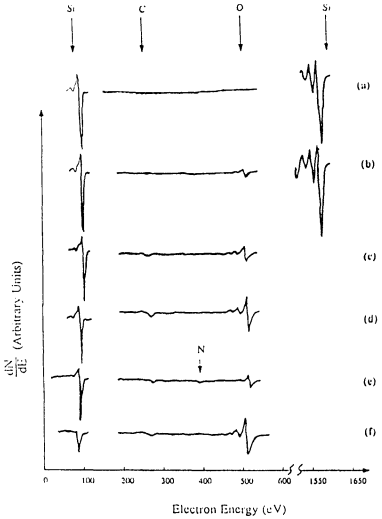


Figure 4. AES analysis of Si (100) (a) after H-plasma clean at 250°C and after subsequent 2 hour air exposure following clean plus passivation at (b) room temperature, (c) 150°C, (d) 250°C, and (e) before and (f) after 2 hour air exposure for wafer desorbed of H under UHV at 500°C.

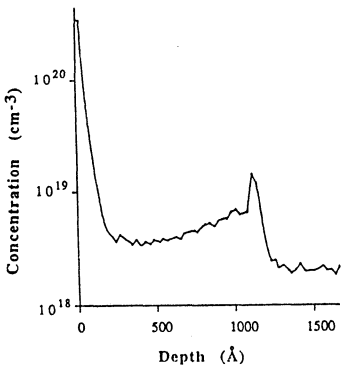


Figure 5. SIMS data showing oxygen incorporation for a typical RPCVD wafer. The surface preparation includes RCA clean, dilute HF dip, and *in situ* remote H plasma clean. The AES was performed after the *in situ* clean and before deposition.

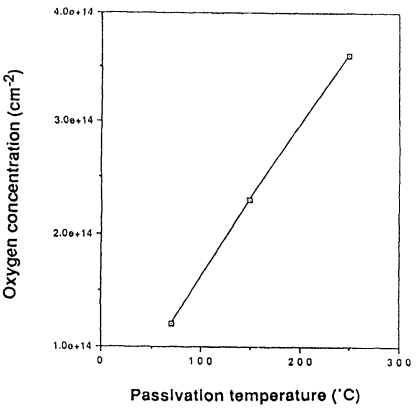


Figure 6 SIMS oxygen surface concentration after 2 hr. air exposure as a function of temperature of passivation. The wafer preparation was the same as in Fig. 6.

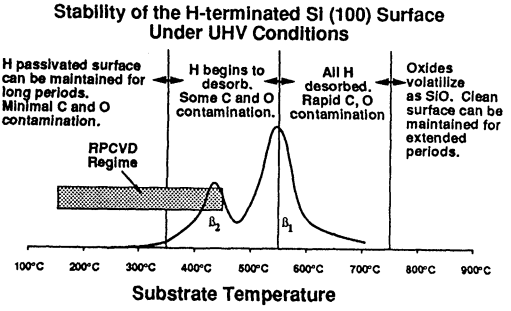


Figure 8. Ilustration of stability of (100) Si surface versus temperature superimposed with hydrogen temperature programmed desorption (TPD) curve. Temperature range for RPCVD epitaxy is also shown. TPD data is from Gates *et al* [3].

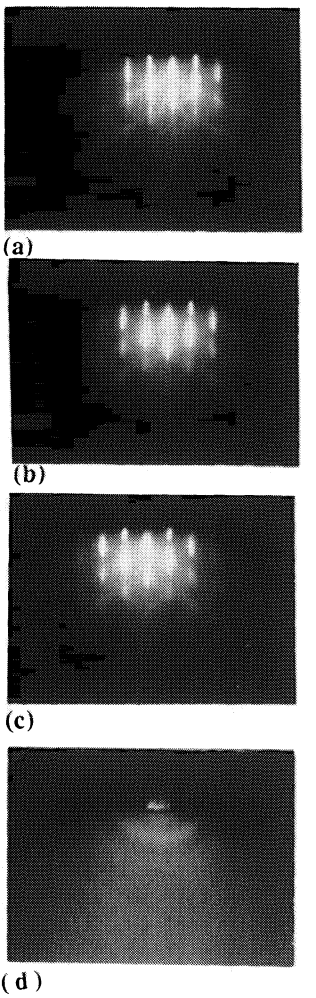


Figure 7. RHEED patterns of films grown after 2 hour air exposure following passivation at (a) room temperature, (b) 150°C, (c) 250°C and (d) desorbed of H at 500°C. Film growth temperature was 305 °C.

OPTIMISING HYDROPHILIC WAFER CLEANING FOR SILICON EPITAXY

A.J.Pidduck, R.Jackson, D.J.Robbins, W.Y.Leong and M.Wheeler
DRA Electronics Division, RSRE, St. Andrews Road, Malvern, Worcs., WR14 3PS, U.K.

Controlled etching in dilute HF is used to decrease the thickness of oxide formed during wafer precleaning, in order to lower the temperature required for oxide desorption prior to vapour phase silicon epitaxy. Low levels of interface carbon and epilayer dislocations can be achieved so long as the cleaned surface remains uniformly hydrophilic. This appears to require the presence of an outermost SiO_2 layer, leading to a minimum desorption temperature of about 860°C in 130 Pa H_2 for the cleaning strategy examined.

INTRODUCTION

High quality surface cleaning is an essential requirement for silicon epitaxy. Residual substrate surface contaminants, whether particulate or molecular, can lead to extended defects in the epilayer or to point defects or precipitates at the interface, and these can degrade electronic performance if present in the active region of devices. Two precleaning strategies are widely used. The first uses a final HF exposure to create a hydrophobic hydrogen-terminated surface (1,2), and requires no further in-situ cleaning step in the epitaxial reactor so long as deposition is started below about 550°C in order to preserve the hydrogen passivation at all times prior to epitaxy (2). The second uses an oxidising chemical preclean to form a thin hydrophilic carbon-free oxide (3,4) which must then be removed in-situ to expose the crystalline Si surface for epitaxy. Oxide removal can be achieved by reactive etching, for instance with Si(5), Ge(6), anhydrous HF(7), or by thermal desorption during a pre-epitaxial bake (prebake) period (4). As epitaxial temperatures are reduced in line with other processing steps, and still further to enable heteroepitaxy, it is desirable to minimise the prebake temperature. In this paper we study the hydrophilic preclean approach to find the lowest prebake temperature consistent with good epitaxial quality, through an understanding of the mechanisms involved.

Firstly we examine the links between surface morphology during prebake, the level of residual substrate contamination and epitaxial layer quality. We apply laser light scattering (LLS) (8-10) to follow the surface roughness changes in-situ in the epitaxial reactor, and use ex-situ atomic force microscopy (AFM) to interpret these changes. Secondly we study the effect of minimising oxide thickness by controlled etchback of a UV-exposed oxide in aqueous HF. The oxide surface chemistry, characterised using X-ray photoelectron spectroscopy (XPS) and a 'cold plate' moisture nucleation test, can be correlated

with the changes in LLS behaviour observed during prebake as the HF exposure time is increased. This is used to draw conclusions about the limits of suitablility of this process for high quality epitaxy.

EXPERIMENTAL

Wet chemical cleaning was performed in a spray cleaning system (FSI "Mercury"). For the HF-only clean, 1:30 HF/H_2O was diluted in-situ to 1:150 using UPDI water, and dispensed under atomisation conditions for various times up to 90s. This was immediately followed by cold water rinsing for 105s and hot water rinsing (80°C) for 45s before N_2 spin dry. The 'B' clean uses a modified RCA chemistry (3), namely a sequence of 4:1 H_2SO_4/H_2O_2 (45s), 30s 1:120 HF/H_2O, 120s 0.5:1:4 $NH_4OH/H_2O_2/H_2O$ and 120s 1:1:5 $HCl/H_2O_2/H_2O$ interspersed by cold and hot water rinses, and followed by final water rinse and N_2 spin dry. Chemicals used were Merck VLSI Selectipur or Micro Image Technology Memory grade. UV exposures were carried out in air mixed with N_2 and O_2 in a stainless steel reactor (UVOCS T0606B or T16X16E). Wafers used were (100) and (111) CZ or epi, of 76mm or 100mm diameter.

Cleaning quality was assessed by laser particle counter (Tencor Surfscan 160) sensitive to particles $\geq 1\mu m$ dia., and by total reflection X-ray fluorescence (TXRF model XSA 8000 or 8010 with Mo anode and He-purge, Atomika GmbH). No transition metal contamination was detected on cleaned wafers (detection limit $\sim 10^{11}$ atoms/cm^2 for $25<Z<40$). A cold plate, temperature programmable to ~0°C, was used to inspect the uniformity of atmospheric moisture nucleation and evaporation, in a fumehood. This is a variant of the steam test described by Vig (11). XPS measurements of cleaning chemistry were made using a hemispherical analyser (VSW HA150) with multichannel detector and MgKα incident radiation (1253.6eV, 300W) at fixed normal take-off angle.

Epitaxial growth was carried out by pyrolysis of SiH_4 in a stainless steel ultrahigh vacuum (UHV)-compatible chemical vapour deposition (CVD) apparatus (12). Wafers were placed into the UHV loadlock as soon as possible after cleaning. Substrates were the only unbaked component introduced to the growth chamber from air, and were warmed in UHV for several minutes before admitting H_2 for the prebake. For this work, prebake was carried out in 133 Pa H_2 for 7-10 mins at 860-920°C, followed immediately by epitaxial growth in 13 Pa H_2 and 2.5 Pa SiH_4 at 850°C (~0.1μm/min growth rate). The LLS intensity was monitored continuously during prebake and growth. In the fixed geometry used, LLS is sensitive to those Fourier components of the surface roughness autocorrelation function with ~0.5μm period, and has subnanometre vertical sensitivity (8-10). Epilayers were characterised by SIMS profiling for $^{12}C^-$ and $^{16}O^-$, using a Cameca 3f or 4f spectrometer with 50-300nA 10kV Cs^+ beam rastered over a 125-200μm square area, and by wet chemical defect etching using diluted Schimmel etchant (13) for 3 minutes, removing ~1μm Si. Surface roughness was imaged using a contact mode AFM (Digital Instruments Nanoscope II) with 30-100nN constant net stylus force.

RESULTS & DISCUSSION

Surface Morphology and Epitaxial Quality

In-situ LLS has shown that three roughening processes occur during prebake and epitaxial growth when residual carbon contamination is present (at levels of $>10^{12}$ cm^{-2}, as detected by subsequent SIMS profiling of the epilayer) on the substrate surface. The LLS features occuring are (a) a peak associated with inhomogeneous oxide removal (b) continued roughening of the surface whilst held at prebake temperature after the bulk of the oxide has been removed ("thermal roughening") and (c) an intense peak during initial epitaxial growth. Previous work (10) has shown a direct correlation between the intensity during thermal roughening, the LLS initial growth peak height and the integrated concentration of carbon impurity at the epilayer-substrate interface, C_{int}. An additional trend for epilayer dislocation densities to increase with increasing LLS initial growth peak height, and hence C_{int}, was also observed. This emphasises the strong link between surface morphology, residual substrate contamination (especially carbon) and epilayer quality.

Fig.1 shows AFM images corresponding to the three LLS features above. Fig.1(a) shows the circular pits observed on a specimen where heating was stopped after partial (30% complete) oxide decomposition at 850°C. The pits are the result of radial solid phase reduction of SiO_2 by exposed substrate Si. In this mechanism, holes of bare Si form at weaknesses in the oxide, and increase in diameter by reduction of SiO_2 to volatile SiO at their edges (14,15) A maximum in the LLS signal is expected when their diameter is ~1μm (9). The pit depth, 2nm, agrees with the oxide thickness measured by XPS. Small lumps are present at the pit centres. The additional candle-shaped features are however believed to be artefacts associated with aging of the Si surface in air. Fig.1(b) is from a surface exhibiting enhanced LLS thermal roughening after extended anneal (30mins) at 900°C. It appears that the thermal roughening phenomenon is due to the growth of pyramidal features, probably (from the similar number density, ~$5x10^7$ cm^{-2}) mostly nucleated at the oxide removal pit centres. Transmission electron microscopy (TEM) shows that though the pyramidal features contain small impurity microparticles, they are almost entirely crystalline Si (10). This is consistent with their formation by immobile impurities pinning atomic misorientation steps during surface annealling, as observed at an early stage by scanning tunnelling microscopy (16). Fig.1(c) shows the surface of a specimen where epitaxy was stopped during initial growth near to the LLS maximum. The surface pits observed, again ~$5x10^7 cm^{-2}$, result from the disruption of step-flow during epitaxy by the impurity microparticles (10). The pits overgrow after the first ~200nm epitaxy, leading to an epilayer which is cosmetically indistinguishable from that grown on a carefully prepared surface where initial growth disruption was absent.

Fig.2 shows AFM images for the case of prebake and epitaxial growth on substrates where no thermal roughening or initial growth disruption was detected by LLS. Fig.2(a) shows the surface of a polished (111) wafer with peak-to-valley roughness of 2-3nm over 2-3μm areas. Fig2(b) is from a similar wafer after prebake at 915°C for 8 mins, showing an overall roughness level below 1nm. No particulate features were observed. Fig.2(c) is the surface of a 3μm thick (111) epilayer grown at 850°C, also with peak-to-valley roughness below 1nm. Thus in the absence of contamination, the roughness occuring during inhomogeneous oxide removal is purely transient, and both annealling and epitaxial growth have a subsequent smoothing effect. Step lines can be seen running vertically in both (b) and especially (c), regularly spaced by about 60nm. The step height was measured to be ~0.3nm, which is close to the Si (111) monolayer height (0.314nm). The separation and direction of these steps are fully consistent with the 0.30° vicinal angle determined by X-ray diffraction. This suggests that the smoothing action occurs by misorientation step flow, in a reverse direction during annealling, and forward during epitaxy. We did not observe step lines on (100) surfaces, though roughness was within similar overall limits, and the same step-flow mechanisms are believed to occur.

UV/HF Surface Chemistry and Effect on Prebake

Fig.3 shows XPS measurements of surface O and C coverages, calculated from the relative O_{1s}, C_{1s} and Si_{2p} peak areas, after treatment of a UV-exposed chemical oxide (termed UV-O_3 in the following) with aqueous HF for different times t_{HF}. Surface F coverages were below 0.04ML (1ML = $7x10^{14}$ atoms.cm^{-2}) in all cases. The 10 minute UV exposure builds up an oxide of 1.1nm initial thickness, measured from the relative areas of the O-bonded and Si-bonded components of the Si_{2p} peak (17). Data from the 0.5nm-thick 'B'-cleaned oxide are shown for comparison. The oxide etching rate is initially ~10 ML oxygen/min, but decreases after about 20s (an apparent decrease may result if reoxidation occurs during H_2O rinsing). Particle levels (also in fig.3) become high after about t_{HF}=30s, and so longer HF exposures are not practical as a cleaning process. This effect is associated with a tendency for the surface to become hydrophobic, as determined from spreading of UPDI water droplets. Contact angles were estimated to be <20° for times less than 24s, and >30° after 30s HF, which is similar to previous results (17). The surface C data in fig.3 also increases with increasing t_{HF}, first rising above the background level (represented by the level after UV-O_3 cleaning) at t_{HF}=18s. A more dramatic effect is observed in the cold plate water vapour condensation pattern. This shows an abrupt and repeatable transition from high quality interference fringes, after 15s HF, to clear (no fringes) or mist after 18s HF. This change corresponds to a surface which is still hydrophilic (contact angle ⟨10° (11)). Hence the cold plate test pattern is a sensitive measure of the degree and uniformity of surface hydrophilicity.

Fig.4 shows the XPS Si_{2p} peak in detail to examine the oxide bonding state. The distinct symmetrical peak shifted by 3.6-4.0eV in the case of the UV-O_3 and FSI 'B' oxides can be assigned to SiO_2 layers, containing approximately 2-3 ML and 1-2 ML Si respectively. Initial etching of the UV-O_3 oxide reduces the height of this peak but does not alter its shape, as expected for simple removal of the outermost SiO_2 layers. After 18s HF however, the peak starts to shift to lower binding energy, until after 90s there remains only a shoulder extending to about 3eV from the Si_{2p}^{Si} peak, and which can be primarily assigned to silicon in suboxide states (18). Fig.4 (lower) shows that at t_{HF}=18s, although there are a similar number of oxidised surface Si atoms to that after FSI 'B' cleaning, a larger proportion are in suboxide states. The higher suboxide coverage may be a result of the UV-O_3 exposure.

Fig.5 shows the oxide behaviour during prebake, as determined by LLS. The LLS oxide removal maximum is seen after or during the initial rise in thermal background radiation when the temperature is ramped to 880°C. The LLS peak occurs after 3mins at 880°C for the 'B' cleaned oxide, compared to at ~860°C after 15s HF and ~840°C after 18s HF. Thus the oxide decomposition temperature decreases with decreasing O coverage. The parallel decrease in LLS peak height is consistent with a smaller oxide removal pit depth. This depends on the SiO_2 thickness, which determines the amount of surface Si consumed in the solid phase reduction reaction. Fig.5 also shows that thermal roughening can occur after 18s HF, though is not significant after 15s HF or the 'B' clean itself. This correlates with the transitions in both the level of surface C and hydrophilicity described above, and we conclude that the 15s HF treatment represents the optimum compromise between oxide passivation and stability for this UV/HF cleaning method. Layers grown at 850°C using this method after in-situ oxide removal at 860°C for 10mins consistently have undetectable interface carbon and oxygen, and dislocation densities of order $10^3 cm^{-2}$ or below.

The requirement to retain an SiO_2 layer limits the minimum prebake temperature to the region of ~850°C. This is because the rate of solid phase reduction decreases rapidly below this temperature due to its high activation energy (E_a~3.5eV(5)). Significant lowering of the prebake temperature may have been possible were a sufficiently hydrophilic suboxide formed by the UV/HF cleaning process. Whilst Si-OH groups are strongly hydrophilic surface sites (19), termination by Si-H groups (1,2), Si-O-Si linkages (19) and adsorbed hydrocarbons (11) are all known to produce hydrophobic surfaces. It is therefore probable that the transition in the cold plate test is due to a significant decrease in the available surface OH coverage as the final SiO_2 layer is removed. This would also coincide with initial exposure of suboxide by the HF etch, which may allow Si-H species to be formed by HF attack of Si-Si linkages (20). Additionally, remaining OH groups may be screened by adsorption of organic species. This is evidenced by the increased tendency of the surface to accumulate carbon contamination and exhibit thermal roughening during prebake.

CONCLUSIONS

We have examined both the mechanism and optimisation of the oxide passivation preclean / thermal desorption prebake approach to surface preparation for low temperature epitaxy. We have shown that care is required to reduce surface carbon contamination such that interface levels remain below 10^{12} cm^{-2}, but that if this is achieved, then roughening during prebake is a purely transient phenomenon, and device quality epitaxy results. For the case of an oxide formed by a final chemical reduction step in HF, it appears necessary to retain an outermost SiO_2 layer in order to reduce the attractiveness of the surface to accumulate carbon. This requirement for an SiO_2 layer however restricts the minimum prebake temperature in 1 Torr H_2 to the region of a few minutes at 850-860°C. The cold plate test gives a powerful indication of whether the surface is sufficiently hydrophilic for succesful epitaxy. This may depend strongly on the surface hydroxyl group concentration.

ACKNOWLEDGEMENTS

We thank G.Blackmore for SIMS profiling data, W.Berneike (Atomika GmbH) for TXRF results, and M.Lunt for defect etching. We also gratefully acknowledge the assistance of D.Rodway with XPS measurements, and K.Kjoller (Digital Instruments) with AFM imaging.

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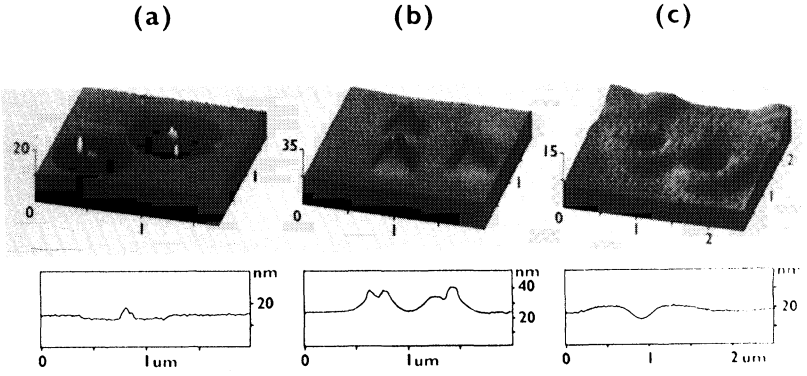

FIGURE 1. AFM images and cross-sections from (001) Si surfaces after (a) partial oxide decomposition at 850°C in UHV (b) 30 minutes anneal at 900°C in 130 Pa H_2 and (c) ~100nm epitaxial growth at 850°C. The circular pits in (a) are the bare silicon areas exposed during oxide removal. The hillocks in (b) and pits in (c) are roughening due to residual contamination (especially carbon) on the substrate surface.

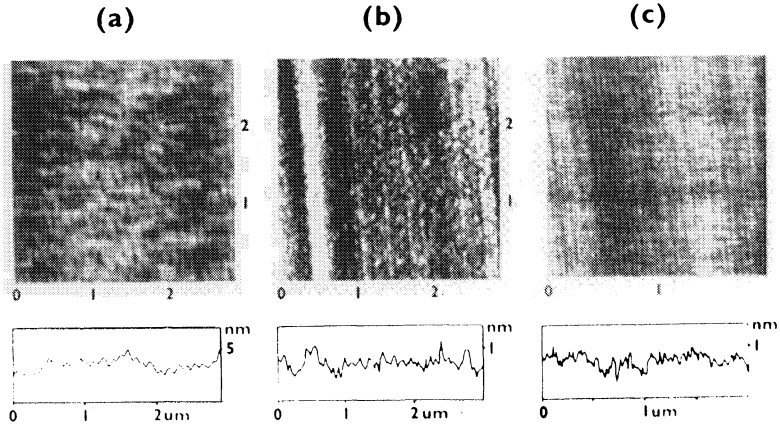

FIGURE 2. AFM images and cross-sections from (111) Si surfaces in the absence of detectable contamination-related roughening. (a) is the as-received wafer surface, (b) is after prebake for 8 minutes at 915°C in 130 Pa H_2 and (c) is after 3μm epitaxial growth at 850°C.

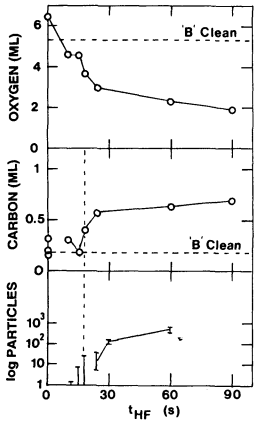

FIGURE 3. XPS surface O and C coverages, and added particles (per wafer, $\geq 1\mu m$ diameter), as a function of HF etching time t_{HF} following UV-ozone cleaning. The dotted line at t_{HF}=18s marks the change in cold plate test pattern.

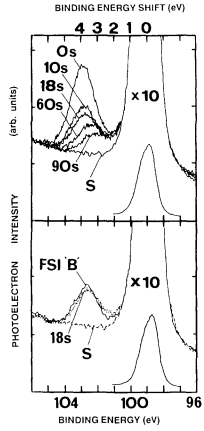

FIGURE 4. Superimposed Si_{2p} XPS spectra as a function of t_{HF} after UV-O_3 clean, compared with sputter-cleaned Si ('S') and (lower) FSI 'B' cleaning.

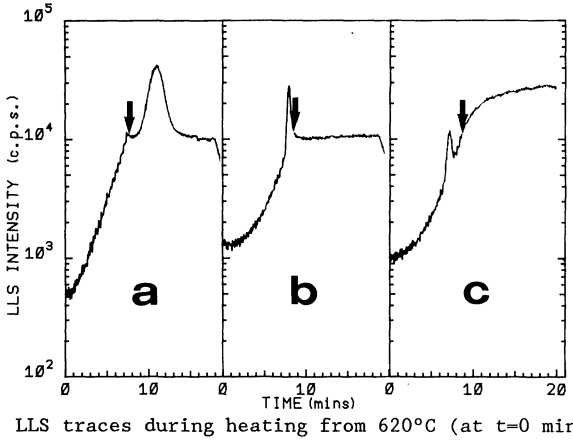

FIGURE 5. LLS traces during heating from 620°C (at t=0 minutes) to the 880°C prebake temperature in 130 Pa H_2 for the cases of oxides formed by (a) FSI 'B' cleaning (b) UV-O_3 + 15s HF and (c) UV-O_3 + 18s HF. The initial rise in intensity is due to increased thermal radiation background, and the arrow indicates when 880°C is reached. A prominent LLS oxide removal peak is seen in all three cases.

KINETICS OF THERMAL CLEANING FOR SILICON AND GERMANIUM-SILICON EPITAXY

M. Racanelli
Advanced Technology Center
Motorola, Incorporated
220 West Broadway Street
Mesa, AZ 85202

and

D.W. Greve
Department of Electrical and Computer Engineering
Carnegie Mellon University
Pittsburgh, PA 15232

ABSTRACT

The oxygen surface concentration on a heated silicon wafer is determined by the balance between chemisorption of oxygen and evolution of SiO. We show that the oxygen surface coverage can be predicted as a function of time, water vapor partial pressure, and temperature. The predicted values are in agreement with those measured for Ge_xSi_{1-x} and silicon epitaxial layers grown by UHV/ CVD.

INTRODUCTION

The recent interest in germanium- silicon/ silicon heterojunction bipolar transistors has provided a new driving force for the reduction of epitaxial growth temperatures, since relaxation of metastable strained layers causes generation of misfit dislocations which degrade transistor performance. A variety of growth techniques have been studied which provide adequately low growth temperatures, including MBE (1), limited reaction processing (LRP) (2), ultra- high vacuum chemical vapor deposition (UHV/ CVD) (3,4), and most recently atmospheric pressure CVD (5,6). Surface preparation is critical in all of these growth techniques, as any contaminants which are adsorbed on the surface are likely to be incorporated in the growing film.

In this paper, we will explore the use of thermal cleaning as a surface preparation technique for epitaxial growth. We will place particular emphasis on relating the oxygen surface concentration to the competing processes of adsorption and desorption. Experimental results reported will be for films grown by UHV/ CVD, although many of the conclusions will be relevant to other growth techniques as well.

SURFACE REACTIONS

We consider here the removal of an initial thin oxide layer (of order one monolayer) from a silicon wafer in a UHV/ CVD reactor. In our growth system (7) the partial pressure of oxygen is negligible ($< 10^{-13}$ torr) and the partial pressure of water vapor is of order 10^{-10} torr. The amount of oxygen on the surface of a wafer is then determined by the competition between chemisorption of water vapor

$$H_2O + * \overset{k_1}{\Rightarrow} SiO^* + H_2 \uparrow \qquad [1]$$

and the desorption of SiO

$$SiO^* \overset{k_2}{\Rightarrow} * + SiO \uparrow \qquad [2]$$

where * represents an empty surface site. These reactions lead to a rate equation for the fraction of surface sites occupied by oxygen Θ_{SiO}

$$\frac{d\Theta_{SiO}}{dt} = k_1 Z_{H_2O} - (k_1 Z_{H_2O} + k_2)\,\Theta_{SiO} \qquad [3]$$

where Z_{H_2O} is the incident flux of water vapor molecules. The solution of [3] is

$$\Theta_{SiO}(t) = \Theta_{SiO}^{\infty} + [\Theta_{SiO}(0) - \Theta_{SiO}^{\infty}]\, e^{-t/\tau} \qquad [4]$$

where $\Theta_{SiO}^{\infty} = k_1 Z_{H_2O}/(k_1 Z_{H_2O} + k_2)$ and $\tau = 1/(k_1 Z_{H_2O} + k_2)$. Values for k_1 and k_2 can be estimated from the work of Ghidini and Smith (8) who measured the critical pressure of water vapor p_C which represents the boundary between an oxygen- covered and oxygen-free surface in equilibrium. At that pressure the adsorption rate of water vapor is equal to the desorption rate of SiO, so we can write

$$k_2 = k_1 Z_{H_2O}(p_C) = k_1 (N_A/2\pi M_{H_2O})^{1/2} p_C \qquad [5]$$

where N_A is Avogadro's number and M_{H_2O} = 18 gm/ mole is the molar mass of water. The critical pressure p_C has been measured as a function of temperature by Ghidini and Smith, who found (8)

$$p_C(T) = 5.6 \times 10^7 \text{ torr } e^{-3.0 \text{ eV/kT}} . \quad [6]$$

Knowledge of $p_C(T)$ only fixes the ratio of the two reaction constants; in order to determine the magnitudes individually we need additional information. We can obtain values suitable for a worst- case calculation of the oxygen coverage if we assume that the water vapor sticking coefficient $s_{H_2O} = Nk_1 = 1$ (where $N = 6.78 \times 10^{14}$ cm^{-2} is the density of surface sites).

We discuss now the implications for epitaxial growth. Using the results above, we see that the equilbrium oxygen surface coverage $\Theta_{SiO}^{\infty} \approx 0$ provided $p_{H_2O} << p_C$. This condition is readily satisified in our growth system at 600 °C since at this temperature $p_C \approx 3 \times 10^{-10}$ torr and therefore it is expected that a clean surface will be obtained in equilbrium. However, as pointed out by Meyerson (9), the time constant for removal of surface oxygen is impractically long at this temperature. The predicted time constant τ (assuming $p_{H_2O} = 0$ and using the critical pressure of Ghidini and Smith) is plotted as a function of temperature in Fig. 1 (curve A). The time constant is predicted to be of order hours at 600 °C. It is more practical, then, to prebake at an elevated temperature at which the time constant is much reduced followed by cooling to the growth temperature. For example, at 800 °C the time constant is predicted to be of the order of a few seconds.

Assuming that a prebake is performed at an elevated temperature, we must also consider the possibility that oxygen may accumulate on the surface while cooling to the growth temperature. This is particularly a concern at very low growth temperatures where we cannot assure that $p_{H_2O} << p_C$. The oxygen surface coverage as a function of time is then predicted by eq. [4]; the results for various p_{H_2O} are plotted in Fig. 2 for a growth temperature of 600 °C. We see that acceptably small interfacial oxygen concentrations are expected even for cooling times of 20 minutes.

At this point, it is interesting to compare the predictions above with other studies of SiO desorption. Tuppen et al. (10) measured the oxygen concentration of MBE- grown silicon layers doped from a B_2O_3 source as a function of boron concentration and growth temperature. Oxygen- free layers were obtained only at higher growth temperatures where the desorption of oxygen as SiO was sufficiently rapid. Tuppen and coworkers calculated the desorption rate of SiO using the SiO partial pressure as determined from thermodynamic data. The predicted oxygen content was in good agreement with their measurements over the temperature range from 550 to 700 °C. The calculated time constant using their partial pressure expression is plotted in Fig. 1 as curve C. Finally, D' Evelyn et al. (11) have conducted a comprehensive study of the adsorption of O_2 and desorption of SiO from (100) silicon surfaces. The time constants they measured for

desorption from surfaces with an initial oxygen coverage of one monolayer are plotted in Fig. 1 as curve B. The results from these two other studies are in very good agreement with predictions based on the work of Ghidini and Smith, particularly for the temperature range of interest here (≈ 600 °C).

D' Evelyn et al. also studied desorption from surfaces with very small oxygen coverage, and obtained dramatically different results. For coverages in the range 10^{-3} to 10^{-7} monolayer, they found that the desorption process involved two steps

$$\text{Si–O–Si} \xrightarrow{k_s} \text{SiO(a)} \xrightarrow{k_d} \text{SiO(g)} \uparrow \qquad [7]$$

where Si–O–Si indicates an oxygen in a bridging site and SiO(a) an SiO molecule adsorbed onto the surface. They concluded that the first step was rate- limiting; the measured time constant $\tau = 1/k_s$ is also plotted in Fig. 1 as curve D. According to their measurements, then, the desorption of SiO from a nearly clean surface is roughly three orders of magnitude more rapid than for surface coverages of a monolayer or more. This was attributed to differences in the chemical bonding; for submonolayer coverages the oxygen is incorporated as isolated atoms bridging two silicon atoms, while for larger coverage SiO_3 and SiO_4 species predominate.

These observations have important implications for low temperature epitaxy. The conclusion to be drawn is that Fig. 2 may considerably overestimate the rate at which a clean surface becomes contaminated. It is interesting to note recent reports (5,6) of low temperature APCVD epitaxy under conditions where $p_{H_2O} > p_C$. While there are other complicating factors (such as the presence of large partial pressures of H_2 and the use of reactants such as SiH_2Cl_2 which produce a variety of other species in gas phase reactions) the enhanced rate of SiO desorption from nearly clean surfaces may partly explain these recent results.

COMPARISON WITH RESULTS OF UHV/ CVD GROWTH

The details of our growth system have reported elsewhere (7). Briefly, the UHV/ CVD technique uses a load- locked, hot- wall reaction chamber capable of attaining UHV conditions ($P_{total} < 10^{-9}$ torr; $P_{H_2O} < 10^{-10}$ torr; and $P_{O_2} < 10^{-13}$ torr). Epitaxial layers are grown at temperatures ranging from 500 to 600 °C using hydride sources (SiH_4 and GeH_4) at pressures of approximately 10^{-3} torr. Under these growth conditions, the reactive sticking coefficient of the reactants is relatively low (≈ 10^{-3}) and as a result uniform layers can be grown on a large number of closely spaced wafers (12,7).

We used 75 mm diameter (100) wafers which had been thermally oxidized followed by definition of an oxide stripe (for step height measurements of the epitaxial layer thickness). The wafers were cleaned by boiling in solvents followed by a DI water rinse and immersion in 3:1 H_2SO_4/ H_2O_2. Immediately before loading, the wafers were rinsed, etched briefly in ≈ 3% HF, rinsed again in DI water and blown dry with nitrogen. The wafers were pushed into the main chamber under a flow of hydrogen after the load lock pressure dropped below 10^{-5} torr. The main chamber was then raised to 150 °C and after a 10 minute pause ramped up to the growth temperature (600 °C). The chamber was pumped overnight in order to reach the base pressure. All wafers were thus exposed to vacuum at 600 °C for an extended period.

We first consider growth of $Ge_{0.05}Si_{0.95}$ layers. Layers grown with no additional in situ cleaning treatment showed an interfacial oxygen concentration of about 1.59 x 10^{15} cm^{-2} (13). The interfacial oxygen concentration was only slightly decreased to 0.83 x 10^{15} cm^{-2} when the sample was prebaked in hydrogen for 10 minutes at 700 °C. In contrast, a sample which was prebaked at 800 °C (5 minutes in hydrogen and 5 minutes in vacuum) showed no detectable interfacial oxygen by SIMS. Accounting for the oxygen background level of the SIMS instrument, this indicated that the interfacial oxygen concentration was less than 3.7 x 10^{12} cm^{-2}.

In the samples discussed above, we cannot rule out possible beneficial effects of exposure to hydrogen or GeH_4. In order to study this issue, we grew silicon epitaxial layers and performed the entire 800 °C prebake in vacuum. The measured SIMS profile for a 1500 Å thick layer is shown in Fig. 3 (14). Here the SIMS oxygen background is lower and the absence of the oxygen peak allows us to place an upper limit on the interfacial oxygen concentration of 4.4 x 10^{11} cm^{-2}. In another sample even lower values are observed and the upper limit on oxygen concentration could be placed below 1.7 x 10^{11} cm^{-2}. We conclude, then, that the vacuum prebake by itself accounts for the excellent results obtained.

The SIMS profile of Fig. 3 also shows the presence of a substantial boron peak at the substrate- epitaxial- layer interface. This boron peak has been also observed in CVD- and MBE- grown epitaxial layers and has been attributed to boron contamination from a variety of sources including atmospheric $B(OH)_3$ (15). The boron peak can be reduced by doing part of the prebake in hydrogen (15) or by protecting the wafer during loading with a hydrogen- passivated surface (9).

CONCLUSIONS

We have studied the use of thermal cleaning for growth of silicon and germanium-silicon layers by UHV/ CVD. Previous measurements of the water vapor critical pressure have been used to make predictions of the temperature required for removal of surface oxygen. The predictions are consistent with observations; a vacuum prebake at 800 °C for 20 minutes is sufficient to obtain an oxygen- free surface. Under the conditions prevailing in a UHV/ CVD reactor, a negligible amount of oxygen accumulates while cooling to the growth temperature. These results show that thermal cleaning is a practical alternative to the use of a hydrogen- passivated surface as described by Meyerson (9).

ACKNOWLEDGEMENTS

The authors wish to acknowledge support from AFOSR (equipment grant AFOSR-89-0144) and NSF (grant ECS-8814267). We also thank Westinghouse STC for additional support and M. Bevan for the providing the SIMS data shown in Fig. 3.

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13. SIMS measurements by Charles Evans Inc.; for this sample only the pause at 150 °C was omitted.
14. Data provided by M. Bevan; measurements performed at Charles Evans East.
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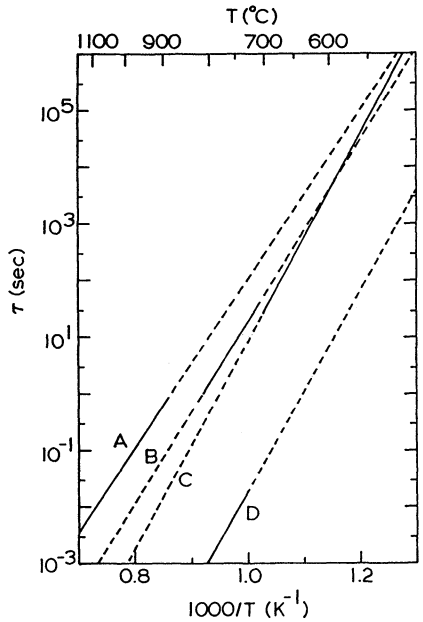

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Figure 1. Predicted time constant for approach to equilibrium surface condition: curve A, calculated from critical pressure data of Ghidini and Smith (8); curve B, single monolayer desorption data of D' Evelyn et al. (11); curve C, SiO partial pressure expression of Tuppen et al. (10); and curve D, submonolayer desorption data of D' Evelyn et al. The solid portion of the lines indicates the temperature range over which experiments were performed.

Figure 2. Predicted oxygen coverage as a function of time and water vapor partial pressure. A water vapor sticking coefficient of unity was assumed.

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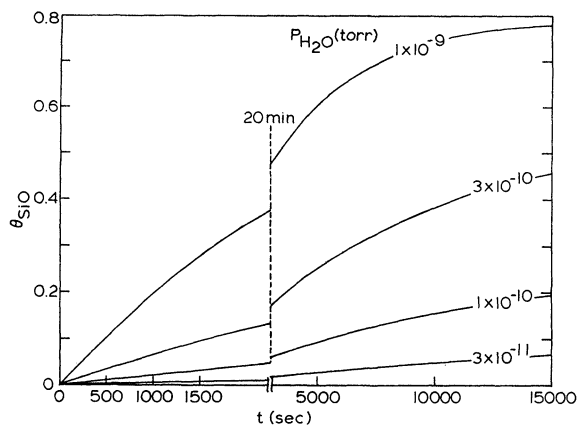

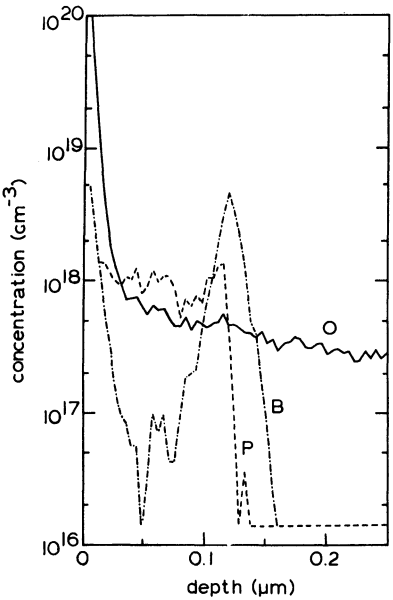

Figure 3. SIMS profile of silicon epitaxial layer grown at 600 °C. The sample received a prebake at 800 °C in vacuum for 20 minutes.

Rapid H_2 Pretreatment for Low-Temperature Silicon Epitaxy

A. Tsukune, H. Miyata, F. Mieno,
A. Shimizu, and Y. Furumura

Fujitsu Limited
Process Development Division
1015 Kamikodanaka, Nakahara-ku
Kawasaki 211, Japan

Abstract

We have developed a rapid-prebaking process and a single-wafer reactor for low-temperature silicon epitaxy. A wafer treated with diluted HF was directly placed on a specially designed SiC-coated graphite heater maintained at 600°C. After loading, the wafer was rapidly heated to a set temperature. Disilane (Si_2H_6) was used as a source gas and diborane (B_2H_6) was used as a doping gas. We grew silicon epitaxial layers with smooth surfaces and without contaminants (C, O, and F) at the epi/substrate interface. The epitaxial layer was grown, without high temperature prebaking, at 750°C and 15 Torr by blowing hydrogen (H_2) vertically against the wafer at a high flow-rate (50 slm) during ramping to the growth temperature. It was also grown at a low temperature of 660°C with prebaking at 795°C for the short time of 1 min.

Introduction

Studies have been done of the use of low-temperature epitaxy to form shallow junctions and heterostructures [1-3]. For an epitaxial process on a patterned wafer, with SiO_2 and polysilicon for example, a low thermal budget of prebaking is helpful. This suppresses undercutting formation at the SiO_2/Si interface [4], melting of high boron-doped polysilicon (Fig. 1), and autodoping.

H_2 prebaking and a prebaking with a small amount of reduction gas, such as SiH_4 and Si_2H_6, using a conventional reactor at low temperature (<900°C) have been unable to removing thick native oxide (~10Å) effectively. Several methods are considered to accomplish a low thermal budget of prebaking [5-7]. A treatment used an diluted HF, one of the methods, etches native oxide easily, and can give a non-oxidized pre-epitaxy surface provided that the substrate is not reoxidized in air or in the growth chamber. An ultrahigh vacuum (UHV) chamber with a load lock is generally used to prevent reoxidation. A drawback is that current UHV chambers for production need careful maintenance.

This paper describes a rapid-prebaking process for low-temperature epitaxy and describes a new reactor suited to the process.

Experimental

We developed a single-wafer reactor with a load-lock chamber and a SiC-coated graphite resistance heater (Fig. 2). A 100-mm-diameter wafer is placed on the heater. The heater is able to hold a maximum wafer diameter of 200-mm. Gas flows vertically onto the wafer from a showerhead. The growth-chamber wall is made of stainless steel and cooled by water. In the growth chamber, an SiC-coated graphite inner jacket protects the chamber wall against heat radiated by the heater. A Roots pump and dry pump system is used for the growth process, and a turbomolecular pump and dry pump system is used for wafer loading. The base pressure is 1×10^{-6} Torr.

The heater temperature is measured by a quartz covered thermocouple in contact with the heater. The heater is controlled by an AC-power-supply voltage. The wafer temperature was previously measured using an thermocouple attached to a wafer. Figure 3 shows the relationship between heater temperature and wafer temperature for an H_2 flow rate of 50 slm and 15 Torr.

We used n-type 4-Ω·cm (100)-oriented silicon wafers as substrates. Before growth, we treated a wafer with wet chemicals followed by diluted-HF treatment without a water rinse. We then placed the wafer in the load-lock chamber within 10 sec, and loaded it into the growth chamber whose heater temperature was 600°C. H_2 began to flow from the showerhead when a wafer was loaded on the heater and the gate valve was shut. The H_2 flow rate during ramping was varied from zero to 50 slm. Prebaking was done at 705-795°C, an H_2 flow rate of 50 slm, and 15 Torr for 1 min. We grew epitaxial layers at 615-750°C and 15 Torr for 10-20 min. During growth, the Si_2H_6 flow rate was 20 sccm, the 9 ppm B_2H_6 diluted with H_2 flow rate was 50-500 sccm, and the H_2 flow rate was 50 slm.

We measured the concentration of contaminants (carbon (C), oxygen (O) and fluorine (F)) and a dopant (boron (B)) with secondary ion mass spectrometry (SIMS). We examined crystal quality using reflection high energy electron diffraction (RHEED).

Results and Discussion

Figure 4 shows the concentration of contaminants, measured with SIMS, for samples grown at different H_2 flow rates during ramping to the growth temperature. Boron concentration was measured at the same time. The epi/substrate interface was obtained from the SIMS depth profile of B. The wafer was treated by 5%-diluted HF for 10 sec before epitaxy. There was no prebaking, and the growth conditions of 750°C and 15 Torr were constant. The calculated H_2 flow velocity at the exit of the showerhead was 1000 cm/sec. The zero-H_2-flow sample (Fig. 4a) has high intensity peaks of C, O, and F at the epi/substrate interface. We used fluorine-contained resin as an insulator between the heater electrodes and the chamber in this experiment only (Fig. 4). In the other experiments, we used quartz as the insulator. We considered that these contaminants (C, O, and F) evaporated from fluorine-contained resin and were adsorbed onto the substrate surface during ramping in the chamber. As the H_2 flow rate increases, the peak intensity at the interface decreases. On the 50-slm-H_2-flow sample (Fig. 4d), the peaks disappear. An H_2 flow rate of 50 slm was enough to lower the partial pressure of contaminants and prevent contaminants adsorbing onto the substrate surface. At an H_2 flow rate of 50 slm, the H_2 flux intensity at the substrate surface is calculated,

assuming ideal conditions, to be 7×10^{19} $cm^{-2} \cdot sec^{-1}$. Since the surface-Si-atom density is 7×10^{14} cm^{-2} at the Si (100) surface layer, H_2 refreshes the substrate surface at a calculated rate of 10^5 sec^{-1} in terms of atomic layer.

We observed the effect of the growth temperature without prebaking. The growth temperature was varied from 660°C to 750°C. Figure 5 shows SIMS depth profiles. The wafer was treated with 1%-diluted HF for 30 sec. The H_2 flow rate during ramping to the growth temperature was 50 slm. For 660°C and 705°C growth samples (Fig. 5a and 5b), contaminant peaks appear at the interface. Figure 4 suggested that contaminants are not easily adsorbed onto the substrate surface during ramping at an H_2 flow rate of 50 slm. So, we considered that C, O, and F were adsorbed before 50-slm-H_2 flow. From results and several researches on Si-wafer surfaces after HF treatment [8-10], it seems that C, O, and F were adsorbed during HF dip, that C and O were adsorbed between HF dip and loading of the wafer into the chamber, and that O was mostly adsorbed between loading of the wafer onto the heater and starting the flow of H_2, for the partial pressure of O during loading is 1.5×10^{-7} Torr. For the 750°C growth sample (Fig. 5c), the peaks disappear. This suggests that contaminants were removed by heating in H_2 between 705°C and 750°C, or by the effect of Si_2H_6 reduction at the first stage of growth.

The effect of prebaking temperature was examined. Figure 6 shows SIMS depth profiles for prebaking temperatures of 705-795°C. The 1%-diluted HF treatment time was 30 sec and the growth temperature was 705°C. 705°C prebaking sample (Fig. 6a) has peaks of contaminants similar to Fig. 5b. Also, with the 750°C prebaking sample, the peaks do not disappear. Figure 6b and previous Fig. 5c suggest that the contaminants adsorbed onto the substrate surface is completely removed at the first stage of 750°C growth with Si_2H_6, while H_2 prebaking at 750°C is not enough to remove contaminants. When the prebaking temperature is 795°C, the peaks disappear (Fig. 6c). It appears that most of contaminants are removed during prebaking. With this prebaking at 795°C and 15 Torr for 1 min, there is no undercutting formation at the SiO_2/Si interface and no melting of high boron-doped polysilicon.

Next, we examined the effect of the growth temperature with prebaking at 795°C. Figure 7 shows SIMS depth profiles for growth temperatures from 615 to 705°C. The 1%-diluted HF treatment was done for 30 sec. With the 660°C growth sample (Fig. 7b), there is no peak at the interface. A small peak of O is seen with the 615°C growth sample as shown in Fig. 7a. These results suggest that reduction by Si_2H_6 at 615°C does not effectively remove contaminants which remain after prebaking at 795°C. Further purification before epitaxy will be needed to remove oxygen at the interface. For example, the purity of diluted HF or gases is improved by using ultra-pure water or a purifier. Also, the base pressure of the reactor is reduced by decreasing chamber leaks and degassing the chamber wall and SiC-coated graphite parts.

Figure 8 shows an RHEED pattern for a sample grown at 615°C with prebaking at 795°C for 1 min. The RHEED pattern shows that the film grown at 615°C is epitaxial layer with a satisfactory crystal quality. With selective poly- and epitaxial-silicon growth (SPEG) at 705°C, the epitaxial layer connects smoothly enough with the polysilicon layer at the SiO_2/Si boundary of the substrate (Fig. 9).

From our results, we conclude that a high-flow-rate of H_2 lowers the partial pressure of contaminants and prevents their adsorption onto the substrate surface. And

although the reduction reaction of Si_2H_6 at 750°C and H_2 at 795°C has difficulty removing a native oxide, prebaking at 795°C for 1 min and the first stage of 750°C growth with Si_2H_6 effectively remove contaminants adsorbed onto a substrate surface after etching the native oxide by diluted HF, resulting in a clean surface.

Summary

We have developed a rapid-prebaking epitaxial process and a suitable reactor. We grew silicon epitaxial layer, without contaminants (C, O, and F) at the epi/substrate interface, on an HF-treated wafer. The layer was grown at 750°C without prebaking by vertically injecting H_2 gas at a high flow rate (50 slm) and a high flow velocity (1000 cm/sec). We also grew an epitaxial layer without contaminants at 660°C with prebaking at 795°C for 1 min.

Acknowledgment

We thank H. Tokunoh for SEM photography, M. Kimura for performing the SIMS analysis, T. Kanno for performing the RHEED analysis, and M. Takeda for his assistance and advice. We also thank H. Tsuchikawa, K. Yanagida, and S. Asuma for their encouragement.

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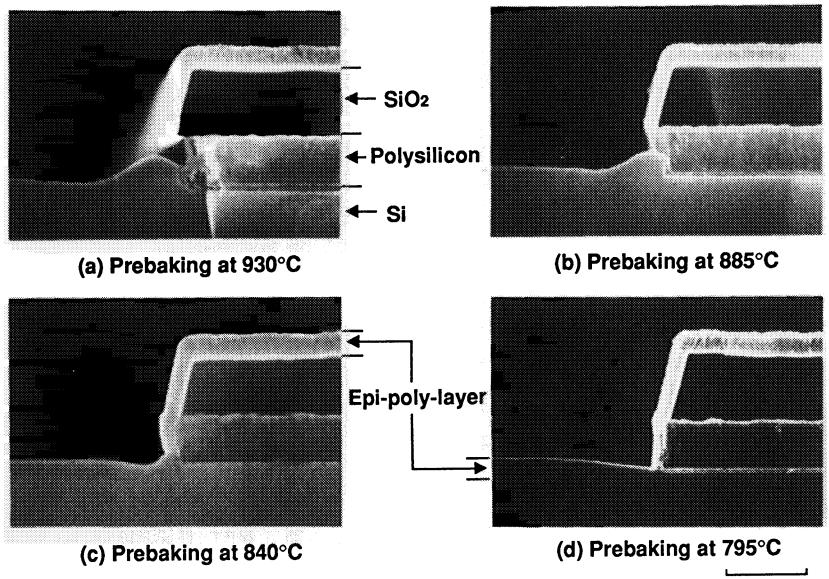

Fig. 1 Cross sectional SEM images. A selective poly- and epitaxial-silicon layer was grown at 705°C with prebaking at 15 Torr for 5 min.

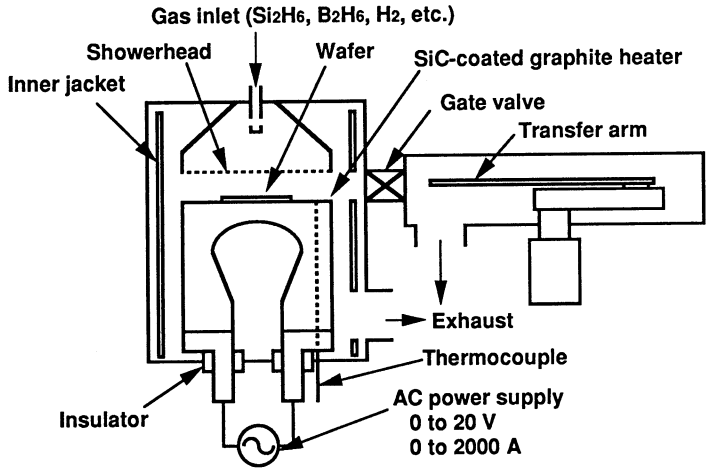

Fig. 2 Schematic of our reactor.

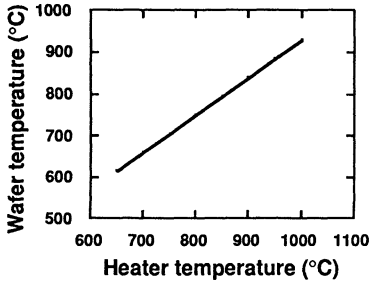

Fig. 3 Heater temperature versus wafer temperature.

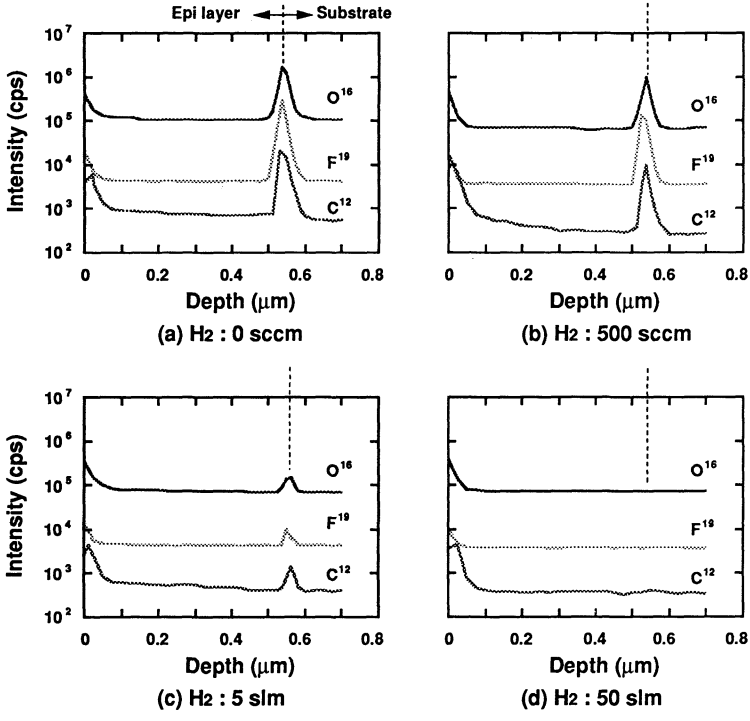

Fig. 4 SIMS depth profiles of C, O, and F in epitaxial layers grown at 750°C without prebaking.

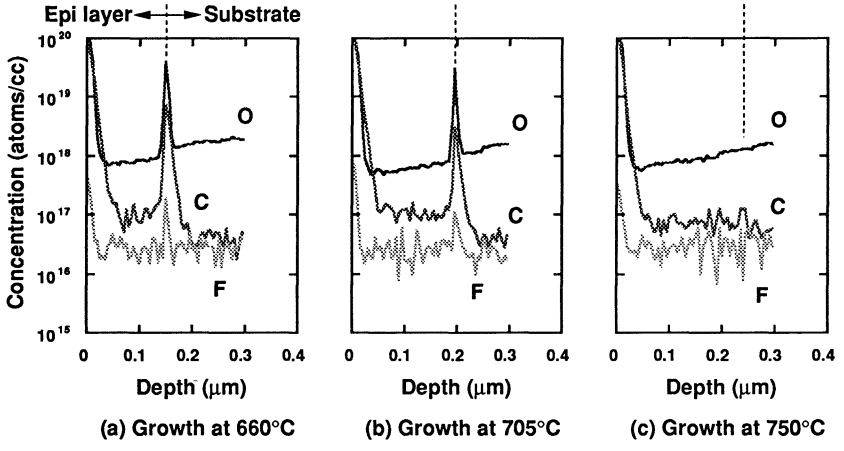

Fig. 5 SIMS depth profiles of C, O, and F in epitaxial layers grown without prebaking.

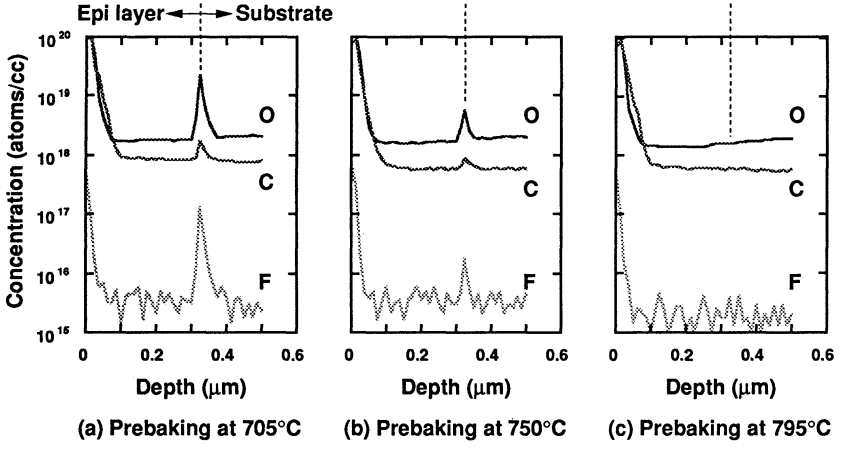

Fig. 6 SIMS depth profiles of C, O, and F in epitaxial layers grown at 705°C with prebaking for 1 min.

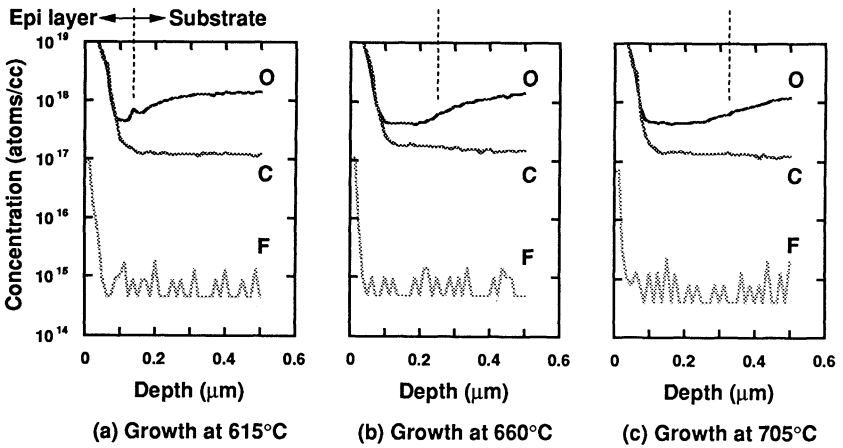

Fig. 7 SIMS depth profiles of C, O, and F in epitaxial layers grown with prebaking at 795°C for 1 min.

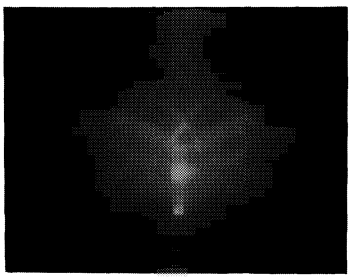

Fig. 8 RHEED pattern of an epitaxial layer grown at 615°C with prebaking at 795°C for 1 min.

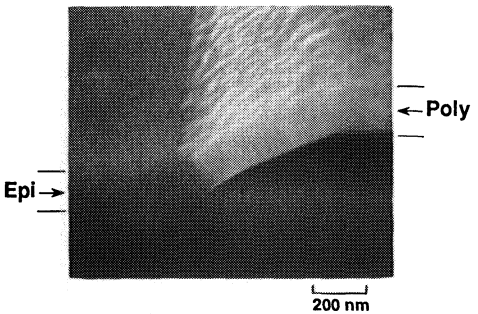

Fig. 9 SEM image of a selective poly- and epitaxial-silicon layer grown at 705°C.

UV/OZONE REMOVAL OF INTERFACIAL CARBON FROM GaAs PRIOR TO METAL ORGANIC MOLECULAR BEAM EPITAXY

S. J. Pearton, F. Ren, C. R. Abernathy, W. S. Hobson and H. S. Luftman
AT&T Bell Laboratories
Murray Hill, NJ 07974

ABSTRACT

Interfacial carbon and oxygen concentrations can be reduced by several orders of magnitude by UV/ozone cleaning of GaAs substrates prior to Metal Organic Molecular Beam Epitaxy (MOMBE). This removal of contamination leads to Metal Semiconductor Field Effect Transistors (MESFETs) with superior I-V saturation characteristics. These results are contrasted with Metal Organic Chemical Vapor Deposition (MOCVD) in which the higher growth temperature and presence of atomic hydrogen generated at the growth surface leads to very low interfacial C and O without the need for a separate ozone-cleaning step. The trend to lower growth temperatures during all types of epitaxy will require the use of some form of substrate cleaning.

INTRODUCTION

A contaminated interface between epitaxial GaAs layers and the underlying semi-insulating substrate will lead to the presence of leakage current and cross-talk between neighbouring devices.[1-3] This has been a common problem over the years in both MESFET and HEMT (High Electron Mobility Transistor) structures. In recent times there have been a number of reports describing the use of ultra-violet/ozone cleaning to remove contaminants from semiconductor surfaces.[4,5] This has particular application to the cleaning of GaAs substrates prior to subsequent epitaxial growth by Molecular Beam Epitaxy[2,6,7] and some reports have shown that UV/ozone cleaning leads to better device isolation properties because of removal of impurities such as carbon which can lead to the presence of a conducting layer at the epi-substrate interface.

While one might expect the UV/ozone cleaning techniques to the effective in preparing substrates for MBE growth, where the deposition of elemental Ga and As species take place in an ultrahigh vacuum environment, it is not clear what will occur on wafers during the initial stages of growth by gas-source techniques like metalorganic MBE (MOMBE) and metalorganic chemical vapor deposition (MOCVD). In both of these growth methods the group V species is derived from AsH_3, so that there is a source of hydrogen at the growth surface. In MOCVD, atomic hydrogen is released via the decomposition of AsH_3. In MOMBE, the AsH_3 is cracked to As_2 and H_2 prior to

injection into the growth chamber. The carbon levels in the epitaxial layer are usually well characterized by electrical and optical methods, and it is generally known how much carbon is expected for a given set of growth parameters. However, little attention has been paid to the level of interfacial contamination with these methods, the role of hydrogen in removing this contamination and whether UV/ozone cleaning is as effective as it is has proven to be for conventional solid-source MBE. In this paper we report secondary-ion mass spectrometry (SIMS) measurements of the interfacial carbon and oxygen concentrations in GaAs/GaAs field-effect transistor (FET) structures grown by both MOMBE and MOCVD, and the effect of UV/ozone cleaning of the GaAs substrate prior to growth. The saturation current-voltage (I-V) characteristics of these FETs are used to assess any contribution of interfacial contamination of leakage current in a typical device structure.

EXPERIMENTAL

The UV/ozone system uses passage of 184.9 nm wavelength light through air to generate ozone and additional use of 253.7 nm wavelength light in the presence of this ozone oxidizes and desorbs carbon and other organic species. All experiments were performed using standard undoped, semi-insulating GaAs substrates. Prior to growth some of the substrates were exposed to UV radiation from a grid of low-pressure mercury vapor lamps. This lamp array produces the two wavelengths of light mentioned above (184.9 and 253.7 nm) necessary for ozone generation and subsequent absorption by surface hydrocarbons. Each exposure was for 5 min (sample to lamp distance was ~5 mm) and then the substrates were immediately loaded into either of the growth systems. For both MOMBE and MOCVD experiments the control GaAs substrates were not given any chemical treatment at all. The epitaxial layers grown by MOCVD at 675 °C consisted of a 1500 Å undoped GaAs buffer layer, followed by a 1500 Å Si-doped ($n \sim 3.4 \times 10^{17}$ cm^{-3}) channel layer for the FET. The structure grown by MOMBE was 1000 Å of undoped GaAs capped with 1500 Å of Sn-doped ($n \sim 3 \times 10^{17}$ cm^{-3}) GaAs, and was deposited at 500 °C using TEGa, TESn, and AsH_3. SIMS measurements were performed using a 5 keV Cs^+ ion beam in a PHI system, with a sputtering rate of 40-80 Å s^{-1}. The secondary ions C^-, O^-, Ga^-, and As^- were collected. The concentration of carbon was derived from a comparison with an ion-implanted standard and is accurate to a factor of 2 and the depth scales were established by Dektak stylus profilometry of the resultant crater. The metal-semiconductor FETs (MESFETs) had a gate length of 1 μm, gate width of 30 μm and were fabricated using a standard lift off technique. TiPtAu was used for the gate metallization and alloyed AuGeNi for the source and drain contacts. The source-drain spacing was 3.5 μm. The doping profiles in the channel layer were obtained from 10 kHz capacitance-voltage (C-V) measurements using a Hg-probe contact.

RESULTS AND DISCUSSION

Figure 1 shows SIMS data on the C and O interfacial concentrations for samples consisting of a total of 3000 Å of epitaxial GaAs on a GaAs substrate. For the MOMBE-grown layers, substrates which had not been UV/ozone cleaned prior to growth display substantial ($\sim 10^{20}$ cm^{-3}) C levels at the interface and substantial oxygen in this region as well. Thus, it does not appear that molecular hydrogen is effective in reducing this surface contamination, as reported previously (8). By sharp contrast, ozone cleaning prior to growth reduces the carbon concentration at the interface to below the SIMS detection limit ($\sim 4 \times 10^{17}$ cm^{-3} in this instrument). A small amount of residual oxygen remains at the interface. It is not clear what the chemical nature of this oxygen is, but it may be in the form of metallic (As or Ga) oxides which are desorbed by the cleaning procedure or possibly small quantities of silicates as reported by Kanber et al.[9] Clearly the ozone cleaning treatment is extremely effective in removing carbon from the substrate surface and there is no recontamination prior to growth.

Figure 1 also shows that MOCVD grown layers do not suffer from detectable interfacial C and O contamination regardless of whether UV/ozone cleaning was used. We assume this stark difference from the situation with MOMBE is a result of the strongly reducing ambient of the growth surface due to the decomposition of AsH_3. This tends to desorb the substrate surface contamination more completely than the As_2 and H_2 generated from the precracking of the AsH_3 in MOMBE. This suggests that *in situ* wafer cleaning procedures in MOMBE will require generation of atomic hydrogen by thermal or plasma techniques.

Following this point, we found in MOMBE that higher temperatures were required to desorb the oxide formed by the ultraviolet radiation on the GaAs substrate surface than when using as-received wafers. In some cases incomplete removal of this oxide prevented initiation of growth of the epitaxial layer itself. Typically, heating to 600 °C under a beam of cracked AsH_3 completely removes the surface oxide. For wafers treated with ozone, however, this pregrowth step was not adequate. Annealing the wafer at 625 °C for 5 min was found to be sufficient for growth on ozone cleaned wafers. This increased difficulty in oxide removal may be due either to a thicker oxide layer on the ozone cleaned surface, or may suggest that the oxide formed by the ozone is of a slightly different character i.e., stoichiometry, than the oxides found on chemically cleaned or polished wafers (10).

The results of C-V measurements on the MOMBE-grown FET channel layers are shown in Fig. 2. Within the resolution of the measurement there is not difference in the sharpness of the profiles in the ozone-cleaned or untreated samples. Therefore, back depletion from the presumably p-type conducting GaAs layer formed at the interface is not affecting our results (2). Similarly, Hall measurements showed 300 K electron mobilities of 1846 and 1768 cm^2/V s, respectively for ozone-cleaned and untreated samples, indicating that the presence of interfacial contamination has little effect on the electrical quality of the epitaxial overlayers themselves. Gray *et al.* (2) only found

significant improvements in MBE-grown samples containing much thinner (~500Å) buffer layers than used here.

A striking improvement, however, was observed in the pinch-off characteristics of the MESFETs fabricated on these layers. Figure 3 (at left) shows the drain current (I_D)/source-drain voltage (V_{DS}) characteristics for the MOMBE-grown samples. The untreated samples display poor saturation behavior because of interfacial layer conduction. By contrast, the UV/ozone cleaned sample has excellent saturation behavior. Since we have seen that the carrier profiles in the channel are identical in both cases, it is clear that the ozone cleaning eliminates parallel conjunction from the interface. The extrinsic transconductance of MOMBE-grown devices was ~110 mS mm^{-1}.

Figure 3 also shows that the ozone cleaning had no detectable effect on the dc characteristics of MOCVD-grown MESFETs. The I_D-V_{DS} characteristics display excellent and identical saturation behavior for both untreated and cleaned samples, in agreement with the expectation from the SIMS measurements. The g_m of these devices grown by MOCVD was ~120 mS mm^{-1}, marginally higher than those on the MOMBE material because of the slightly higher doping in the former.

SUMMARY AND CONCLUSIONS

It is likely that either UV/ozone cleaning or in-situ hydrogen plasma cleaning of GaAs (and InP) substrates prior to epitaxial growth will become necessary in many MOMBE and MBE systems because of the push to lower growth temperatures. We have found that UV/ozone cleaning of GaAs substrates prior to MOMBE growth is a necessity for obtaining MESFET performance undegraded by parallel conduction from the substrate-epitaxial layer interface. This indicates that the molecular hydrogen generated from the decomposition of the AsH_3 prior to injection into the growth chamber does not assist in removal of hydrocarbons from the as-received wafer surface. In contrast, the atomic hydrogen generated at the surface during MOCVD growth is conducive to the removal of the carbon contamination without the need for UV/ozone pretreatment of the substrate.

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5. See, for example, the papers in Semiconductor Cleaning Technology 1989, edited by J. Ruzyllo and R. E. Novak, (Electrochemical Society, Pennington, NJ, 1990).

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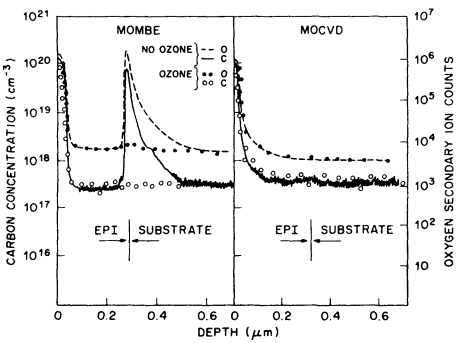

FIG. 1. SIMS profiles of carbon and oxygen in 3000-Å-thick GaAs layers grown by MOMBE (at left) or MOCVD (at right) on GaAs substrates, some of which had been UV/ozone cleaned prior to growth.

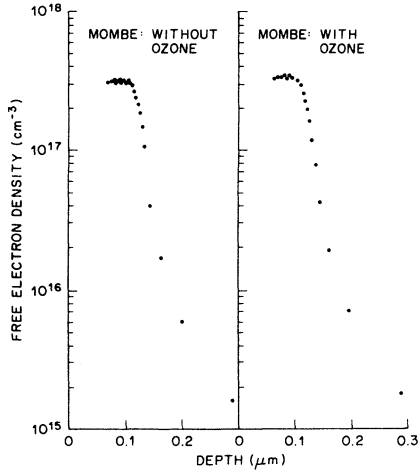

FIG. 2. Free-carrier profiles in GaAs MESFET structures grown by MOMBE on ozone or nonozone cleaned GaAs substrates.

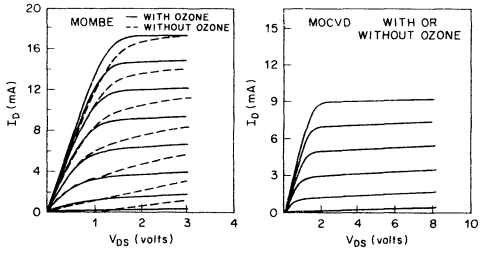

FIG. 3. I_D-V_{DS} characteristics of GaAs MESFETs grown on ozone or nonozone cleaned GaAs substrates by MOMBE (left) or MOCVD (right). In the former case the gate voltage (V_g) starts at $+0.5$ V and changes in -0.5 V steps to -3.5 V. In the latter case V_g goes in -0.5 V steps from 0 to -4.5 V.

STRIPPING OF PHOTORESIST IN SPRAY PROCESSOR

Vinh Thanh Nguyen
FSI International
322 Lake Hazeltine Drive
Chaska, Minnesota 55318-1096

ABSTRACT

The enhancement of photoresist stripping rate using a Sulfuric acid and Hydrogen Peroxide Mixture(SPM) in a spray processor was studied. Several techniques including the use of hot nitrogen for atomization, increasing the temperature of the SPM by optimizing the chemical mix ratio and preheating the chemicals was found to reduce chemical consumption. The higher temperature during stripping also greatly reduced the residual particles and mobile ion contaminants on the wafers.

INTRODUCTION

The removal of photoresist after its use for patterning wafers is an unavoidable step in the lengthy process of manufacturing solid state devices. In the past, photoresist stripping has received little attention. Today, state-of-the-art microcircuit devices are extremely sensistive to both ionic and particle contamination and this sensitivity requires more stringent results from the stripping operation. There are three classes of strippers: Inorganics (oxidizing types), Organics (solvents) and Dry (ash), with the inorganic chemistry presently the major way of removing photoresist[1].

Inorganic chemistries can remove most resist. However, there are occasions where partial plasma ashing is required prior to wet chemical removal to burn through the carbonized layer of photoresist created by heavy ion implantation.

Inorganic strippers usually consist of sulfuric acid mixed with an oxidant such as hydrogen peroxide or ammonium persulfate heated to 120°C [2]. They are normally used to strip resist from non-metallized wafers.

Immersion stripping has been widely used in the past. However this method suffers from drawbacks such as loss in chemical activity of the strip bath with time due to its high operating temperature or the contamination of the bath by photoresist residues (i.e. sodium). These drawbacks make it difficult for the process engineer to achieve the necessary strip and clean performance.

Spray stripping is another method of removing photoresist in which the stripping solution is distributed onto the wafers in the form of a fine mist. The capability of the spray tool to blend the sulfuric acid and hydrogen peroxide mixture just prior to stripping and discard it right after use helps alleviate the problems present with the immersion technique. The SPM solution on the wafer surface is always fresh thus eliminating contamination, both ionics and particles.

In the present study, a spray tool was used to perform the stripping process using mixtures of sulfuric acid and hydrogen peroxide (SPM). This paper reports the different techniques evaluated to minimize chemical consumption and maximize cleaning performance compared to a typical immersion method.

BACKGROUND

It is generally known that the temperature of any photoresist stripper greatly influences the efficiency and rate of photoresist removal. This is not surprising since chemical reaction rates approximately double for every 10°C increase in temperature. Most IC manufacturing companies capitalize on this fact by heating their SPM bath for stripping photoresist to high temperature, sometimes up to 150°C. In the immersion strip process, the wafers are allowed to reside in the bath for 10-15 minutes. Eighty per cent of this duration is redundant since all of the resist on the wafers is stripped within the first 3 minutes.

When an acid spray processor is used to perform the strip, the strip time is an important factor to be considered because it is directly related to the stripping solution consumption. Figure 1 shows the cross section of the process chamber in a standard FSI Multi Position spray processor. In this equipment the stripping solution is delivered onto the wafers directly from the mixing manifold at a fairly low flow rate. Since only a small amount of strippant to strip the four (or more) cassettes of wafers that the process chamber can contain, the SPM solution is broken down into a fine mist using a jet of high purity Nitrogen. This atomizing action unfortunately robs a portion of the heat generated by the exothermic reaction of mixing sulfuric acid and hydrogen peroxide. Cooling of the SPM solution reduces the strip rate of the photoresist, forcing the use of a larger amount of acid through longer chemical dispense time.

In order to minimize the chemical consumption and maximize the strip rate, the temperature of the SPM solution needs to be raised to as high a level as possible. Several techniques can be used to boost the temperature and prevent the heat loss of the stripping solution. First is optimum formulation of the SPM, second is preheating of sulfuric acid prior to mixing and third is the use of hot Nitrogen for atomization. All of these methods were evaluated in this study.

EXPERIMENTAL

Test wafer preparation:

The test wafers used in this study are divided into five separate groups to suit the different experiments.

Group A: 4" diameter silicon wafer.
1000 Å thermal oxide.
1.5 µ KTI 850 photoresist.
Hardbake in Blue M oven, 30 min, 120°C, N_2 ambient

Group B: 5" diameter silicon wafer.
Unknown thickness of thermal oxide.
1.5 µ Shipley 1813SP15, patterned
Phosphorous implanted @ 4 $10E^{14}$ atoms/cm^2, 140 KeV

Group C: 5" diameter bare silicon wafer
Megasonic clean with RCA chemistry
Quick dump rinse, Spin dry

Group D: 5" diameter bare silicon wafer
1000 Å thermal oxide
Megasonic clean with RCA chemistry
Quick dump rinse, Spin dry

Group E: 5" diameter bare silicon wafer
1000 Å Thermal Oxide on Silicon
1.2 µ positive photoresist
Hardbake, 30 min, 160°C

Optimization of the Sulfuric Peroxide Mixture:

The blending of sulfuric acid and hydrogen peroxide is an exothermic reaction with temperature rise dependent upon the mix ratio. Therefore, the H_2SO_4/H_2O_2 ratio was varied to determine the hottest mixture. In this test, sulfuric acid (96%) and hydrogen peroxide (30%) were mixed in a Teflon®beaker to a total volume of 1000 milliliters. The temperature was measured with a mercury thermometer and the highest temperature recorded. The maximum temperature typically occurs 10-15 seconds after the blending.

In order to determine the effect of mix ratio on strip rate, test wafers in group A were stripped in a beaker filled with H_2SO_4/H_2O_2 mixed at different volume ratios. The strip rate was determined by visually observing the dissolution of photoresist and measuring the time elapsed. In all experiments the test wafers were kept motionless in the SPM bath to prevent the effect of agitation.

Process modification in spray processor to increase wafer temperature:

In these tests Nitrogen gas was preheated to 100°C before atomization. The apparatus to heat the Nitrogen was an FSI in-line gas heater. The pressure of the nitrogen gas was regulated to 20 PSI during atomization. The temperature of the chemicals prior to mixing was kept at room temperature. The SPM solution had a volume ratio of 4:1. The temperature on the monitor wafers was measured by wedging a thermocouple between two wafers during the SPM dispense.

The tests were performed with an FSI acid processor (TITAN®Multi-Position). Sulfuric acid was heated prior to blending with hydrogen peroxide, then atomized with nitrogen onto bare silicon monitor wafers. The volume ratio of this mixture was chosen to be at 2:1 instead of 3:2 for the convenience of operating the flowmeters on the Titan MP. The temperature of the nitrogen was set at 25°C and 100°C. A Teflon®coated thermocouple was wedged between 2 adjacent wafers and the maximum temperature recorded.

The sulfuric acid was heated to a different temperature with an FSI on-line chemical heater. The temperature was varied from 25°C to 90°C. Experiments were performed both with and without nitrogen heating using the optimum mix ratio.

Application of modified process to stripping resist:

In these experiments a standard strip process and the optimized strip process were compared using wafers from group B. The implant dosage of $4X10E^{14}$ was chosen for this experiment because this medium range implant energy does not necessitate a plasma ash operation before stripping but still represents a challenge for wet stripping.

Two runs were performed. In Run 1, 25 test wafers were stripped with a 4:1 mixture of sulfuric peroxide without any preheating of the chemicals or with hot nitrogen. In Run 2, 25 test wafers are stripped in a 2:1 mixture with the sulfuric acid preheated to 90°C and nitrogen heated to 100°C.

Comparison of residual contamination following immersion and spray stripping:

Monitor wafers were run in both the acid processor and immersion bath to determine the addition/removal of particles. The particle counter used was a Tencor model 5500. Particles greater than 0.3 μm diameter were measured before and after the test.

In the immersion test the silicon monitor wafers were dipped in a 5:1 bath of sulfuric peroxide heated to 120°C for 10 minutes, followed by a rinse and spin dry.

In the spray process the monitor wafers were subjected to a 5 minute spray of sulfuric peroxide mixture followed by a 5 minute DI rinse and spun dry. The ratio of the mixture is either 4:1 or 2:1. Neither the sulfuric acid nor the nitrogen is heated in this case. Wafers with both a native oxide (Group C) and 1000Å thermal oxide (Group D) were used in the study.

Ionic contamination after stripping in the spray tool was studied by the CV (Capacitance-Volyage) test method. Sodium ion is the most common contaminant in MOS processing and a trace amount of Na+ in the gate oxide causes a CV shift [3]. To determine the CV shift a simple MOS capacitor was built on the stripped wafers. The structure of this capacitor consisted of a gate electrode (a circular dot of metal) deposited over the gate oxide. A capacitance meter was used to measure the capacitance of the structure while allowing the application of DC bias. By allowing the DC bias to change and plotting the capacitance as a function of the DC bias, a CV plot results. The CV shift is the difference between the CV plot of the initial MOS structure and the CV plot of the heat-stressed MOS structure. A shift of 0.1 V typically corresponds to a density of $<10E^{10}$ ions/cm^2. A 1.0V shift correspond to a density of $>10E^{12}$ ions/cm^2.

Hot sulfuric and hot nitrogen were used in the test to determine ionic contamination. The test wafers from Group E were used. The SPM dispense time was varied from 4.5 minutes to 17 minutes.

RESULTS AND DISCUSSIONS

Immersion strip experiments:

Figure 2 shows the temperature achieved when the SPM mix ratio was varied along with a theoretical curve. It indicates that a sulfuric-peroxide ratio of 3:2 respectively yielded the highest temperature. This ratio corresponds to the theoretical ratio that produces the most heat. Figure 3 shows that the highest strip rate was achieved with a 3:2 SPM ratio. It was not surprising to note that this 3:2 ratio is the most efficient mixture since it has the highest temperature.

Spray processor experiments:

Figure 4 compares the wafer temperatures achieved with and without Nitrogen heating. It shows that hot Nitrogen achieves a temperature increase on the surface of 10°C. A 4:1 SPM with room temperature H_2SO_4 and room temperature nitrogen yielded a temperature of 77°C on the wafers.

The effect of preheating the sulfuric acid is shown in Figure 5. Heating of the sulfuric to 90°C resulted in a 15-20°C temperature rise on the wafer surface. A combination of a 2:1 mix, hot atomization and hot sulfuric acid resulted in a wafer temperature of 115°C. This is an increase of about 40°C over the standard process using a 4:1 mix ratio with unheated sulfuric and nitrogen.

Table I compares the strip times and chemical consumptions of the standard and optimized process. It shows the optimized process reduced processing time and chemical consumption by 67% and 64%, respectively.

Table II shows that the spray tool used with an SPM ratio of 2:1 yielded the best particle performance. It also implies that fresh, clean SPM at high temperature does not add particles to the wafers. It was speculated that the higher temperature of the SPM and the relative higher dilution of sulfuric acid render the stripper less viscous, thus much easier to rinse off.

Table III shows that minimal ionic contamination resulted from the use of hot SPM, and over-stripping to remove these contaminations after the photoresist was completely disolved is not necessary. The CV shift averaged out to be less than 0.05 Volt. We can conclude that the level of ionic contamination left on the wafer after stripping was less than $10E^{10}$ ions/cm^2.

CONCLUSION

The most effective formulation of the Acid-Hydorgen Peroxide solution for stripping photoresist in a TITAN Multi-Position was found to be 2:1 by volume, respectively. The strip rate can be further enhanced by preheating the sulfuric acid before mixing with hydogen peroxide and by using heated nitrogen for atomization. A combination of optimized mix ratio, hot sulfuric and hot nitrogen atomization was found to decrease solution consumption by 64%. This process does not add particles and leaves the surface of the wafer with ionic contaminant density of less than $10E^{10}$ ions/cm^2.

ACKNOWLEDGEMENTS

The author would like to thank Craig Baldwin from IDT Corporation and Lup Yee from Motorola for supplying valuable data on CV and Particle tests; Don Grant from FSI for fruitful discussions and for reading the manuscript.

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	SPM Dispense (minutes)	SPM Consumption (liters)
Standard Process (4:1 SPM with room temperature N_2 & H_2SO_4)	15	11.25
Optimized Process (2:1 SPM with hot N_2 & H_2SO_4)	5	4

Table I: Comparisons of Dispense Times and Solution Consumption Using Standard and Optimized Strip Processes

Change in Particles Per Wafer (> 0.3 μm) for Various Strip Processes

	Immersion	4:1 SPM	2: SPM
Native Oxide	-	6 ±5	2 ± 8
1000 Å Oxide	40 ± 20	152 ± 90	-7 ± 17

Note: Results presented as mean ± 1 standard deviation

Table II: Comparison of Particle Additions for Three Stripping Processes

Sample #	CV Shift (v)	Strip Time (minute)
CV 1	0	4.5
CV 2	-0.2	4.5
CV 3	0	4.5
CV 4	0	4.5
CV 5	-0.13	9.0
CV 6	0	9.0
CV 8	-0.15	17.0
BPE 1	0	9.0
BPE 2	-0.04	4.5
BPE 3	0	4.5
BPE 4	0	9.0
Mean ± 1 SD	-0.05 ± 0.07	

Table III: CV Shifts Resulting Following an Optimized Strip Process

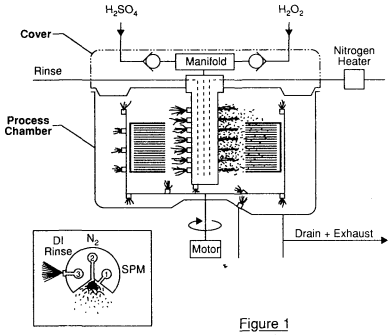

Figure 1

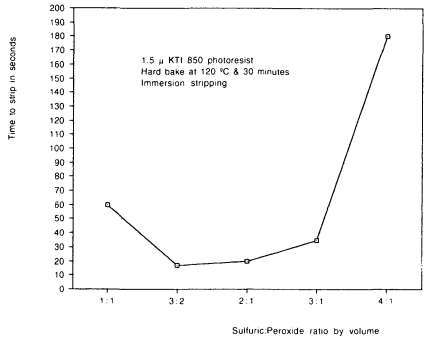

Figure 3: Strip time of photoresist in Sulfuric Peroxide Mixtures

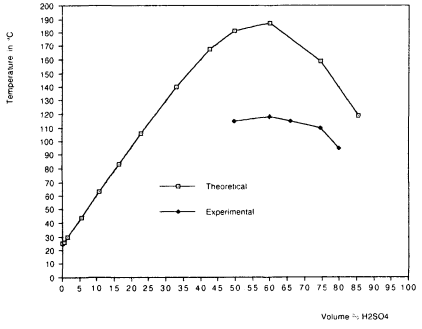

Figure 2: Temperature rise Due to Blending of 96% H2SO4 and 30% H2O2

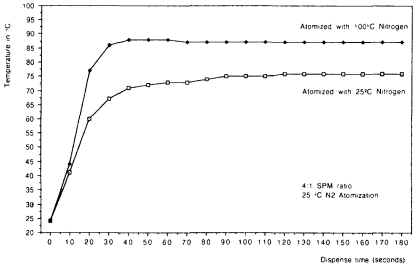

Figure 4: Effect of hot Atomization on Wafer Surface Temperature

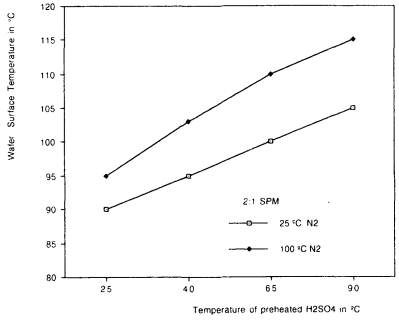

Figure 5: The effect of preheating N2 and H2SO4 on Wafer Surface temperature

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