PROCEEDINGS OF THE THIRD INTERNATIONAL SYMPOSIUM ON

CLEANING TECHNOLOGY IN SEMICONDUCTOR DEVICE MANUFACTURING

Edited by

Jerzy Ruzyllo
Pennsylvania State University
University Park, Pennsylvania

Richard E. Novak
SubMicron Systems, Inc.
Allentown, Pennsylvania

Assistant Editors

A. Bowling
B. Chung
B. Deal
M. Heyns
T. Ohmi

ELECTRONICS AND DIELECTRIC SCIENCE AND TECHNOLOGY DIVISIONS

Proceedings Volume 94-7

THE ELECTROCHEMICAL SOCIETY, INC., 10 South Main St., Pennington, NJ 08534-2896

Library of Congress Catalog Number: 93-72867

ISBN 1-56677-038-6

Printed in the United States of America

PREFACE

The First and Second International Symposia on Wafer Cleaning Technology in Semiconductor Device Manufacturing were held during the Society's Fall Meetings in October of 1989 in Hollywood, Florida, and in October of 1991 in Phoenix, Arizona. The attendance was beyond expectation, and the number and quality of papers presented during these symposia confirmed that meetings devoted solely to wafer cleaning technology are both needed and timely. This success prompted the Electronics and Dielectrics Science and Technology divisions to continue joint sponsorship of this series. Consequently, "cleaning symposia" are organized on the biannual basis during the Fall Meetings of the Electrochemical Society.

This softbound proceeding volume contains the papers presented during the Third International Symposium of Cleaning Technology in Semiconductor Device Manufacturing held during the Electrochemical Society Fall meeting in New Orleans, Louisiana, October 15-20, 1993. The number of papers submitted to this symposium was almost twice the number of papers submitted to the previous symposium in this series. Also, the number of people involved in this last meeting as the authors and co-authors of papers was almost as high as during the first two meetings combined. These observations, as well as excellent attendance during all eight symposium sessions testify to the deep reaching interest wafer cleaning technology currently enjoys.

It is readily noticeable from the content of the papers presented in this volume that the degree of scientific sophistication and technical complexity of the state-of-the art wafer cleaning methods are very high. Our understanding of surface reactions involved in both liquid-phase and gas-phase cleaning is continuously improving. Also, new processing methods and process characterization techniques are certain to have a positive impact on production yield and improved device reliability. As a result, we are now better than ever before prepared to extrapolate correctly the future role of wafer cleaning operations in high-end microchip manufacturing. In order to reach the next phase in terms of device complexity, new manufacturing

methods will have to be implemented. More than any other operation performed on the wafer, wafer cleaning will have to go through major changes to meet these future requirements. The organizers hope that the Electrochemical Society's "Cleaning Symposia" will continue having a noticeable contribution to this process.

We would like to take this opportunity to thank all symposium authors and participants who turned this symposium into a very informative and productive meeting. In particular, we would like to thank all our colleagues who assisted us in editing this volume and who chaired the symposium sessions. Moreover, our thanks are due to the invited speakers for their excellent contributions and to all the participants for their encouragement and support which makes us look toward the next symposium in this series in October 1995 with great enthusiasm and excitement.

Jerzy Ruzyllo
Richard E. Novak

TABLE OF CONTENTS

FACTS ABOUT THE ELECTROCHEMICAL SOCIETY, INC.

The Electrochemical Society, Inc., is an international, nonprofit, scientific, educational organization founded for the advancement of the theory and practice of electrochemistry, electrothermics, electronics, and allied subjects. The Society was founded in Philadelphia in 1902 and incorporated in 1930. There are currently over 6000 scientists and engineers from more than 60 countries who hold individual membership; the Society is also supported by more than 100 corporations through Patron and Sustaining Memberships.

The Technical activities of the Society are carried on by Divisions and Groups. Local Sections of the Society have been organized in a number of cities and regions.

Major international meetings of the Society are held in the Spring and Fall of each year. At these meetings, the Divisions and Groups hold general sessions and sponsor symposia on specialized subjects.

The Society has an active publications program which includes the following:

JOURNAL OF THE ELECTROCHEMICAL SOCIETY - The JOURNAL is a monthly publication containing technical papers covering basic research and technology of interest in the areas of concern to the Society. Papers submitted for publication are subjected to careful evaluation and review by authorities in the field before acceptance, and high standards are maintained for the technical content of the JOURNAL.

THE ELECTROCHEMICAL SOCIETY INTERFACE - INTERFACE is a quarterly publication containing news, reviews, advertisements, and articles on technical matters of interest to Society Members in a lively, casual format. Also featured in each issue are special pages dedicated to serving the interests of the Society and allowing better communication between Divisions, Groups, and Local Sections.

EXTENDED ABSTRACTS - Extended Abstracts of the technical papers presented at the Spring and Fall Meetings of the Society are published in serialized softbound volumes.

PROCEEDINGS VOLUMES - Papers presented in symposia at Society and Topical Meetings are published from time to time as serialized Proceedings Volumes. These provide up-to-date views of specialized topics and frequently offer comprehensive treatment of rapidly developing areas.

MONOGRAPH VOLUMES - The Society has, for a number of years, sponsored the publication of hardbound Monograph Volumes, which provide authoritative accounts of specific topics in electrochemistry, solid state science, and related disciplines.

LIQUID-PHASE CLEANING

ADVANCED WET CHEMICAL CLEANING FOR FUTURE ULSI FABRICATION

Tadahiro OHMI
Department of Electronics Faculty of Engineering
TOHOKU UNIVERSITY
Aza Aoba, Aramaki, Aoba-ku,
Sendai, 980 JAPAN

Realizing ultra clean wafer surfaces has become increasingly important for ULSI fabrication. In this paper some new wet chemical cleaning technique are introduced. Particles adhesion in the liquid can be prevented by adding surfactant into the solution. Organic impurities can be removed by ozonized ultrapure water at room temperature. The anion species in the solution strongly affect the noble metal adhesion onto silicon wafers. Finally, a new wet chemical cleaning sequence and a newly developed wafer spin cleaner featuring high cleaning performance and low cost are proposed.

INTRODUCTION

Reduction in minimum dimensions of semiconductor devices and the resultant enhancement in the integration density have been continuously advancing. The rate of growth of integration density has never been reduced, but it seems likely that the growth is even accelerated toward the deep submicron era. The problem now is how to construct manufacturing lines for the production of such ULSI circuit chips that preserve high manufacturing yields under moderate investment costs for the line. As many as 10 million to 100 million active devices are to be integrated on a single chip of a deep submicron design rule ULSI. A huge number of transistors on a wafer must behave exactly as they are designed, and such a tight control in manufacturing must be preserved from wafer to wafer, from lot to lot during a long period of production operation. Perfect uniformity and perfect reproducibility must be guaranteed for deep submicron wafer manufacturing lines.

We have claimed that the simultaneous fulfillment of the following three principles is most essential to establish high performance processes that assure both perfect uniformity and perfect reproducibility. The three principles are:

1. ULTRA CLEAN PROCESSING ENVIRONMENT;
2. ULTRA CLEAN WAFER SURFACE;
3. PERFECT-PROCESS PARAMETER CONTROL.

The importance of these three principles have been demonstrated by various experimental data[1-4]. In order to create *ultra clean processing environment* tremendous efforts have been devoted to the development of Ultra Clean Technologies such as super cleanroom

technology[5], ultra clean gas technology[6-9], ultra pure water technology[5,10-12], ultra clean chemicals technology[13-17] and so forth. As a result, we have achieved extremely high levels of cleanliness and purity in a cleanroom system, gases, ultra pure water and chemicals. This is quite important because they directly affect the quality of wafer processing. In spite of the remarkable advancement in these clean technologies, there still exist difficulties in realizing *Ultra Clean Wafer Surface* which, we believe, is most essential in establishing high performance processes.

The *Ultra Clean Wafer Surface* is characterized as a surface of following conditions.

1. PARTICLE FREE
2. ORGANIC CONTAMINATION FREE
3. METALLIC CONTAMINATION FREE
4. NATIVE OXIDE FREE
5. COMPLETELY HYDROGEN TERMINATED
6. SURFACE MICROROUGHNESS FREE

The particle, organic materials, and metallic elements are the well-recognized "classical" contaminations. The elimination of such contaminations has been greatly improved owing to the advancement of *ultraclean processing environment technologies*, namely ultrapure water technologies and ultra clean chemicals technologies. It is important to note that we have included *native oxide* in the category of contamination in a sense that it severely deteriorates the processing integrity. It was found that the native oxide growth occurs only under the coexistence of O_2 and H_2O[18]. This is why the dissolved oxygen(DO) concentration in ultrapure water must be reduced to a level as low as possible. It is shown that the growth of native oxide is suppressed when wafers are rinsed in ultrapure water with reduced DO concentrations. The silicon surface removed of native oxide by diluted HF, for instance, is very active and easily contaminated by adsorbed air molecules. The molecular adsorption on a cleaned Si surface also degrades the processing quality[19]. In order to prevent such degradation, the cleaned silicon surface must be perfectly hydrogen-terminated. Finally silicon surfaces must be perfectly flat at an atomic level. The improvement in the surface microroughness has great impacts on the integrity of thin gate oxide as well as the channel electron mobility[20-22].

The RCA cleaning method, which was established by W.Kern et al., has been helped us for a long time, since it is very effective to remove the three classical contaminations such as particle, organic impurities, and metallic elements[23]. However, as active scientific investigations has been conducted to reveal the interaction between various contaminations and substrates, it is necessary to develop a new cleaning process which can simultaneously realize the six conditions for ultra clean wafer surface. The purpose of this paper is to establish the advanced wet chemical cleaning method based on solid/liquid interface science. Firstly I wish to show some of our latest experimental results to understand how to realize ultra clean wafer surface. Secondly I wish to introduce *an Advanced Wet Chemical Cleaning Process* which is devised as the conclusion of the experimental results for the purpose of reducing the cost of wet chemical cleaning.

STRATEGIES FOR ULTRA CLEAN WAFER SURFACE

1. Prevention of Particle Deposition by Adding Surfactant in Cleaning Solution

In the RCA cleaning method, particles are mainly removed by $NH_4OH/H_2O_2/H_2O$ cleaning (APM or SC-1 cleaning). In this cleaning solution, the chemical oxide layer on a wafer, which is formed by H_2O_2 oxidation, is etched by NH_4OH. Particles on a wafer are lift off and separated from the wafer surface. The separated particles cannot readhere onto the surface due to the electrical repulsion between particles and the wafer surface, because most of the particles and silicon substrate are charged the same polarity (negative) in alkaline solution. Then particles are removed. This is the reason why the APM cleaning is very effective to remove particles from silicon wafer surface*(24)*. However, in the case of silicon nitride (SiNx) surface, APM solution rather promotes particle adhesion than removal, because the silicon nitride surface charges positive even in alkaline solution. The negative charged particles easily adhere on the positive charged surface. Therefore APM cleaning cannot be used for silicon nitride surface. This means that there is no effective cleaning solution which can clean the wafers on which the silicon surface and the silicon nitride surface coexist. Moreover, this problem often happens as a cross contamination problem that the particles which are removed from the contaminated back wafer surface adhere onto the front wafer surface when the back and front surface have different layers (e.g., silicon, silicon oxide, and silicon nitride), because the back surface is often more contaminated than the front surface.

In order to overcome this basic problem, we propose the addition of surfactant in the cleaning solution[25]. Table 1 shows the zeta potential of various substrates (silicon, silicon oxide, and silicon nitride) and poly-styrene latex particles with and without surfactant in the acidic solution. In this experiment, PSL particles were used as the representative particles due to their uniformity and chemical stability. The surface charge of substrates and particles is described by the zeta potential. The polarity of the zeta potential can be made equal by adding a surfactant to the solution. It is therefore expected that the particle deposition in the liquid is prevented by the addition of surfactant.

Table 1 Zeta Potential Change by Adding Surfactant (pH3.3HCl)

	without surfactant	anionic surfactant	cationic surfactant
Si	-23mV	-32mV	63mV
Si_3N_4	43mV	-52mV	45mV
SiO_2	7mV	-7mV	55mV
PSL	39mV	-67mV	78mV

Figure 1 shows the effect of the addition of surfactant applied to the silicon surface in acidic solution. The wafers were immersed in the HF solution with surfactant

contaminated by PSL particles (10^5/ml). The anionic surfactant completely prevents the particle deposition. On the other hand, the cationic surfactant reduces the particle deposition but about 1,000 PSL particles still deposit onto the surface. We have considered that the reason of the limited effect of the cationic surfactant is because some PSL particles adhered on negative charged silicon surface faster than the cationic surfactant changed the polarity of silicon surface from the negative to the positive. Therefore, PSL particles deposit immediately at the initial stage of the immersion, but no more PSL particles deposit on the wafer after that. This is different from the case of "without surfactant" where the number of the PSL particles on the silicon wafer increases with time. In the experimental result shown in Figure 2, where the silicon wafer was immersed in the clean HF solution with the cationic surfactant to change the polarity (pre-treatment) before it was immersed in the HF solution contaminated with PSL particles, the particle deposition was completely eliminated. In the case of the anionic surfactant applied to silicon surface, pre-treatment is not necessary, because the silicon surface is already negatively charged.

Figure 3 shows PSL particle deposition on the silicon and silicon nitride substrates where the anionic surfactant is added to the HF solution. When the pre-treatment is applied for silicon nitride surface, PSL particle deposition was eliminated on both substrates.

We will propose the surfactant adding method (Figure 4) to prevent particle deposition onto the wafers where the substrate materials having opposite zeta potential coexist. For example, addition of the anionic surfactant makes silicon, silicon oxide, silicon nitride, and particles charged negative resulting in a reduced particle deposition by the electric repulsive force. It is important to make sure that surfactant molecules cover the wafer surface before particles start depositing. Therefore, particles in cleaning solution must be reduced to an extremely low level, especially when this method is applied to prevent cross contamination from wafer back surfaces to front surfaces.

2. Organic Contamination Removal Using Ozone-Injected Ultrapure Water

Organic material is one of the most difficult contaminations on wafer surfaces. Organic contamination seriously deteriorates the wet chemical cleaning efficiency for other contaminations, because the adsorbed organic molecules often prevent the chemical cleaning solution from contacting with the wafer surface, resulting in a low cleaning efficiency and non-uniform etching which results in surface microroughness. Therefore, organic contamination must be removed from wafers at the first stage.

We have developed a new method to remove organic contamination using the combination of oxidation by ozonized ultrapure water and etching by diluted HF solution featuring low temperature processing[26,27]. In this cleaning method, ozonized ultrapure water contributes not only to the direct decomposition of organic contamination but also to the formation of silicon oxide layer which is removed together with contaminations on it by following diluted HF etching. From the experimental results using various surfactant as representative organic impurities, we have found that ozonized ultrapure

cleaning works effectively regardless of molecular weight (Figure 5) and hydrophobic degree (Figure 6) of organic molecules. Besides, this cleaning method does not increase surface microroughness.

3. Understanding the Anion Effects on Metallic Contamination

It has been revealed that metallic atoms get adsorbed onto the silicon surface in aqueous solution by two different mechanisms[28]. Metals featuring higher electronegativity than Si such as Pb, Cu, Hg, Ag, Pt, and Au, when being ionized, are reduced at the silicon surface and get directly adsorbed in a chemical manner (Table 2). On the other hand, metals featuring lower electronegativity than Si such as Sn, Ni, Fe, Zn, Al, Na, and K do not directly form any chemical bond with the silicon surface. Many of these metals featuring lower electronegativity than Si are included in the chemical oxide, which is formed on the silicon surface during the wet cleaning process, in the form of metal oxides because they are oxidized more easily than Si.

Table 2 Electronegativity of various metals

Element	Electronegativity (Pauling)	Electron Attraction Capability
Au	2.4	
Pt	2.2	
Ag	1.9	higher than Si
Hg	1.9	
Cu	1.9	
Pb	1.8	⇑
Si	**1.8**	
Sn	1.8	
Ni	1.8	
Fe	1.8	
Zn	1.6	lower than Si
Al	1.5	
Mg	1.2	
Ca	1.0	
Na	0.9	
K	0.8	

The metallic atoms which are included in the chemical oxide can be removed in the diluted HF cleaning together with the oxide. However noble metals such as Cu are not removed in the diluted HF cleaning because they directly form a chemical bond with the silicon surface. We have found that the Cu contamination which is directly adhered onto the silicon surface depends on the kind and the concentration of the anion species in the solution[29,30]. In Figure 7, the level of Cu contamination is compared by using various anion species of Cu salts which are added into diluted HF. Among them $CuCl_2$ results in the largest amount of Cu adhesion. From this result, it is thought that Cu contamination is promoted by chloride ions in the solution. Then we evaluated the effect

of the concentration of chloride ions and bromide ions, which are expected to facilitate Cu adhesion. This was carried out by spiking HCl and HBr into the diluted HF solution which was contaminated by 1ppm Cu using CuF_2 salt. Figure 8 (n-type wafer) and 9 (p-type wafer) indicate that Cu adhesion is promoted by chloride ions and bromide ions on both type of wafers. We can learn from these experimental results that chloride and bromide ions must be eliminated from the cleaning solution. The $HCl/H_2O_2/H_2O$ (HPM) cleaning solution may be the most dangerous source of chloride contamination. The HPM cleaning has been used to remove the alkaline metals from the silicon surfaces, but alkaline metals can be removed by a diluted HF solution. The HPM cleaning functions as an accelerator for Cu contamination if chloride ions are not rinsed completely. Therefore, the HPM cleaning must be eliminated from wet chemical cleaning processes. In order to remove Cu from silicon wafers, $HF/H_2O_2/H_2O$ (FPM) cleaning has been found to be effective[31,32]. Besides, in the FPM solution, Cu does not adhere onto silicon wafers even when the solution is contaminated with Cu and chloride (Figure 10).

ADVANCED WET CHEMICAL CLEANING

1. Cost-Effective Wet Chemical Cleaning - Simple Cleaning Sequence

Table 3 shows the typical wet chemical cleaning sequence based on RCA cleaning method. The original RCA cleaning cycle consists of 2 steps (APM and HPM cleaning). Some SPM and DHF steps are usually applied before and after RCA cleaning. After every step a ultrapure water rinse is performed.

Table 3 Conventional Wet Chemical Cleaning Sequence Based on RCA Cleaning

	mixing ratio	temperature	cleaning targets
H_2SO_4/H_2O_2 (SPM)	4:1	120°C	organic
HF/H_2O (DHF)	1:100	room temp.	native oxide, metal
$NH_4OH/H_2O_2/H_2O$ (APM)	1:1:5	70-90°C	particle, organic, metal
$HCl/H_2O_2/H_2O$ (HPM)	1:1:6	70-90°C	alkali metal
HF/H_2O (DHF)	1:100	room temp.	native oxide

This RCA cleaning has helped us greatly over the past 25 years. However, we would like to propose that it should be changed now for the purpose of improving the cleaning performance and reducing the cleaning costs. Concerning cleaning performance, we have shown that HPM cleaning promotes the contamination of noble metals when followed by diluted HF cleaning and that $HF/H_2O_2/H_2O$ (FPM) cleaning is effective. Moreover, the purity of chemicals and ultrapure water have improved dramatically in 25 years. Furthermore, the situation around semiconductor device manufacturing industry is becoming more and more stringent. One must consider to reduce the total cost of

manufacturing, including the cost of wet chemical cleaning. Specifically, future wet chemical cleaning must satisfy following three principles.

1. The number of the process steps should be decreased.

2. The chemical consumption should be reduced to an ultimately low level.

3. The entire wet process should be conducted at room temperature.

We will propose *Advanced Wet Chemical Cleaning Sequence* for future ULSI fabrication shown in Table 4[4].

Table 4 Advanced Wet Chemical Cleaning Sequence

	mixing ratio	temperature	cleaning targets
Ozonized Ultrapure Water	2ppm O_3	room temp.	organic
HF/H_2O (DHF)	1:100	room temp.	native oxide, metal
$NH_4OH/H_2O_2/H_2O$ (APM)	0.05:1:5	80°C	particle, organic, metal
$HF/H_2O_2/H_2O$ (FPM)	1:35:65	room temp.	native oxide

Organic impurities can be sufficiently removed by the ozonized ultrapure water cleaning. This process can be performed at room temperature. Unfortunately APM cleaning still requires a high temperature. As a final step of this advanced wet chemical cleaning sequence, we would like to propose $HF/H_2O_2/H_2O$ (FPM) cleaning. In this step, heavy metals featuring higher electronegativity than Si are removed together with chemical oxide formed by H_2O_2. HPM cleaning which was mainly conducted for the removal of alkali metals will not be performed, because HPM solution enhances the adhesion of heavy metals onto silicon wafers, and alkali metals can be removed by FPM cleaning. This simple cleaning sequence is enough to sufficiently fulfill the six conditions for *ultraclean wafer surface*.

2. Dynamic Wet Chemical Cleaning – Spin Cleaning

The essential functions of wet chemical cleaning can be listed as the following three functions.

1. The function to SEPARATE contaminants from wafer surfaces.

2. The function to PREVENT READHESION of contaminants onto wafer surfaces.

3. The function to TRANSPORT contaminants away from wafer surfaces.

For example, when the $NH_4OH/H_2O_2/H_2O$ (APM) cleaning is used to remove particles, firstly, Due to the etching by NH_4OH, particles are lift off and separated from the wafer surface together with chemical oxide formed by H_2O_2. This is the *function 1*. The separated particles cannot readhere onto the surface due to the electrical repulsion between particles and the wafer surface in an alkaline solution. This is the *function 2*. However, the conventional "liquid chemical waiting – wafer transiting" method, that is the *static* method in which wafers are immersed into chemicals, can hardly work for

function 3 except the slow diffusion during the immersion period or only at the moment when wafers are pulled out of chemicals. The following ultrapure water rinse does not work for *function 2* and *3* resulting in readhesion. Therefore, in order to realize rapid and complete cleaning efficiency, simultaneous fulfillment of the three functions is necessary.

On the other hand, when the *dynamic* "wafer waiting – liquid chemical transiting" method is introduced, the complete cleaning efficiency can be obtained within a short time. Practically speaking, we will propose the *spin cleaning* method, where fresh chemicals are continuously introduced onto the center of a rotating wafer[33]. The appearance of the newly developed spin cleaner is shown in Figure 11. In the spin cleaner, wafers are sealed by nitrogen in order to realize native oxide free processing. The cleaning efficiency of $HF/H_2O_2/H_2O$ cleaning for Cu removal is compared between spin cleaning method and batch cleaning method. Figure 12 indicates that Cu is removed to less than 5×10^{10}atms/cm^2 within 10 seconds by spin cleaning while it takes an hour by batch cleaning. The spin cleaning method requires less time and smaller chemical volume to remove Cu from the silicon surface completely. Moreover, spin cleaning is free from the cross contamination from back surfaces to front surfaces that is the most difficult problem of batch cleaning. Furthermore, in spin cleaning the chemical reaction can remain uniform because the fresh chemicals are supplied continuously and there is no change in chemical proportion.

CONCLUSION

The improvement for higher cleaning performance and lower cost are continuously requested to the wet chemical cleaning. Only the scientific investigation of solid/liquid interfaces can realize these demands simultaneously. Particles adhesion in the liquid can be prevented by adding surfactant into the solution. Organic impurities can be removed by ozonized ultrapure water at room temperature. The anion species in the solution strongly affect the noble metal adhesion onto silicon wafers. A new wet chemical cleaning sequence and a newly developed wafer spin cleaner are proposed based on the experimental results. We believe that these new technologies will contribute to future ULSI fabrication.

REFERENCES

1. T.Ohmi, Microcontamination, Vol.6 No.10, 49–58 (1988).
2. T.Ohmi, Tech.Dig., 1989 IEDM, Washington D.C., 49–52 (1989).
3. T.Ohmi, in Automated Integrated Circuits Manufacturing/1990, V.Akins, ed., PV90–3, p.3–18, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1990).
4. BREAK THROUGH FOR SCIENTIFIC SEMICONDUCTOR MANUFACTURING IN 2001, Realize INC., Japan, (1992).
5. T.Ohmi, N.Mikoshiba, and K.Tubouchi, in ULSI Science and Technology/1987,

S.Broydo and C.M.Osburn, eds., PV87-11, p.761-785, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1987).
6. T.Ohmi, J.Murota, Y.Mitsui, K.Sugiyama, T.Kawasaki, and H.Kawano, in ULSI Science and Technology/1987, S.Broydo and C.M.Osburn, eds., PV87-11, p.805-821, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1987).
7. K.Sugiyama, T.Ohmi, M.Morita, Y.Nakahara, and N.Miki, J.Vac.Sci.Technol.A8(4), 3337-3340 (1990).
8. T.Ohmi, M.Nakamura, A.Ohki, K.Kawada, and K.Hirao, J.Electrochem.Soc., Vol.139, 2654-2658 (1992).
9. T.Ohmi, A.Ohki, M.Nakamura, K.Kawada, T.Watanabe, Y.Nakagawa, S.Miyoshi, S.Takahashi, and M.S.K.Chen, J.Electrochem.Soc., Vol.140, 1691-1699 (1993)
10. T.Ohmi, Proc. 10th Semiconductor Pure Water Conference, Santa Clara, 251-273 (1991).
11. Y.Yagi, T.Imaoka, Y.Kasama, and T.Ohmi, IEEE Trans.Semicond.Manufact., Vol.5, 121-127 (1992).
12. T.Ohmi, T.Isagawa, T.Imaoka, and I.Sugiyama, J.Electrochem.Soc., Vol.139, 3336-3345 (1992).
13. N.Miki, H.Kikuyama, I.Kawanabe, M.Miyashita, and T.Ohmi, IEEE Trans.Electron Devices, Vol.37, 107-115 (1990).
14. H.Kikuyama, N.Miki, K.Saka, J.Takano, I.Kawanabe, M.Miyashita, and T.Ohmi, IEEE Trans.Semicond.Manufact., Vol.3, 99-108 (1990).
15. H.Kikuyama, N.Miki, K.Saka, J.Takano, I.Kawanabe, M.Miyashita, and T.Ohmi, IEEE Trans.Semicond.Manufact., Vol.4, 26-35 (1991).
16. H.Kikuyama, M.Waki, I.Kawanabe, M.Miyashita, T.Yabune, N.Miki, J.Takano, and T.Ohmi, J.Electrochem.Soc. Vol.139, 2239-2243 (1992).
17. K.Kimura, Y.Ogata, F.Tanaka, T.Imaoka, J.Takano, T.Isagawa, T.Kezuka, M.Kogure, T.Futatsuki, and T.Ohmi, in Contamination Control and Defect Reduction in Semiconductor Manufacturing I/1992, Dennis N.Schmidt, ed., PV92-21, p.347-360, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1992).
18. M.Morita, T.Ohmi, E.Hasegawa, M.Kawakami, and M.Ohwada, J.Appl.Phys., Vol.68, 1272-1281 (1990).
19. T.Ohmi, T.Ichikawa, T.Shibata, K.Matsudo, and H.Iwabuchi, Appl.Phys.Lett., Vol.53, 45-47 (1988).
20. T.Ohmi, K.Kotani, A.Teramoto, and M.Miyashita, IEEE Electron Device Lett., Vol.12, 652-654 (1991).
21. T.Ohmi, M.Miyashita, M.Itano, T.Imaoka, and I.Kawanabe, IEEE Trans. Electron Devices, Vol.39, 537-545 (1992).
22. M.Miyashita, T.Tsuga, K.Makihara, and T.Ohmi, J.Electrochem.Soc., Vol.139, 2133-2142 (1992).
23. W.Kern and D.A.Puotien, RCA Review, 31, 187-205 (1970).
24. M.Itano, F.W.Kern,Jr., R.W.Rosenberg, M.Miyashita, I.Kawanabe, and T.Ohmi, IEEE Trans.Semicond.Manufact., Vol.5, 114-120 (1992).
25. T.Kezuka, M.Ishii, T.Hosomi, M.Suyama, S.Maruyama, M.Itano, and M.Kubo, Proc.

Semiconductor Pure Water and Chemicals Conference, Santa Clara, 144–158 (1993).
26. T.Ohmi, T.Isagawa, M.Kogure, and T.Imaoka, J.Electrochem.Soc., Vol.140, 804–810 (1993).
27. K.Kogure, T.Isagawa, T.Futatsuki, N.Yonekawa, and T.Ohmi, Proc. 39th Meeting of Institute of Environmental Sciences, Vol.1, 380–385 (1993).
28. T.Ohmi, T.Imaoka, I.Sugiyama, and T.Kezuka, J.Electrochem.Soc., Vol.139, 3317–3335 (1992).
29. H.Aomi, F.Derouin, and T.Ohmi, Extended Abstracts of Electrochem.Soc., Spring Meeting, Vol.93–1, 1144–1145 (1993).
30. F.Derouin, H.Aomi, and T.Ohmi, Proc. 39th Meeting of Institute of Environmental Sciences, Vol.1, 460–465 (1993).
31. T.Shimono and M.Tsuji, Extended Abstracts of Electrochem.Soc., Spring Meeting, Vol.91–1, 278–279, Washington D.C. (1991).
32. T.Ohmi, T.Imaoka, T.Kezuka, J.Takano, and M.Kogure, J.Electrochem.Soc., Vol.140, 811–818 (1993).
33. F.Kunimoto, T.Ohmi, and F.W.Kern Jr., Proc. 39th Meeting of Institute of Environmental Sciences, Vol.1, 245–254 (1993).

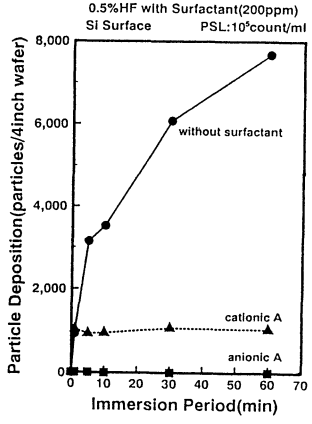


Figure 1 The effect of the addition of surfactant

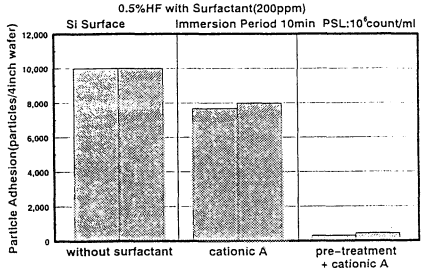


Figure 2 The effect of "pre-treatment"

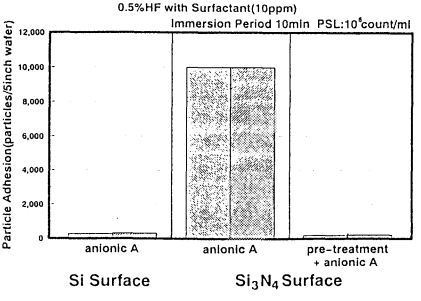


Figure 3 Prevention of particle deposition by surfactant for Si and Si_3N_4 surfaces

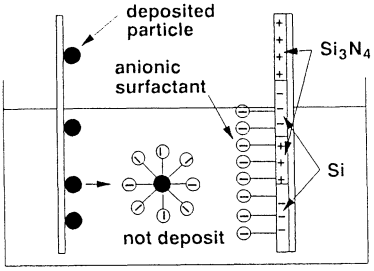


Figure 4 Proposed method to prevent particle deposition for different surfaces

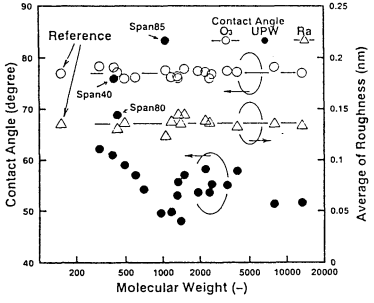


Figure 5 Cleaning efficiency of ozonized ultrapure water for organic contaminations with various molecular weight

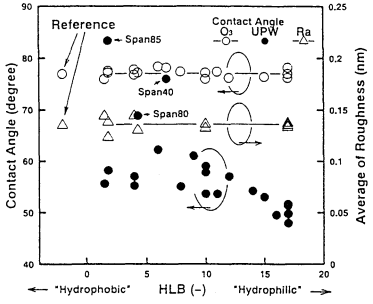


Figure 6 Cleaning efficiency of ozonized ultrapure water for organic contaminations with various hydrophobic degree

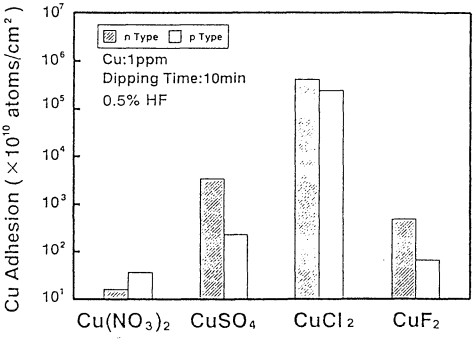


Figure 7 Cu contamination by various salts

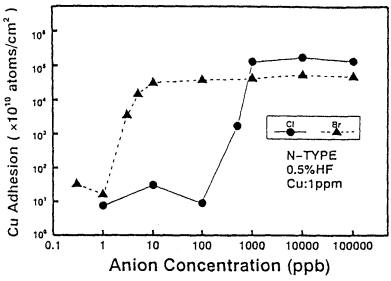


Figure 8 The relationship between the halogen concentration and the Cu adhesion onto n–tyte Si surface

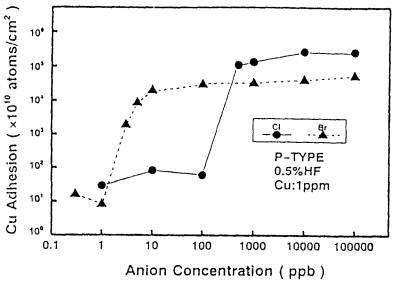


Figure 9 The relationship between the halogen concentration and the Cu adhesion onto p–tyte Si surface

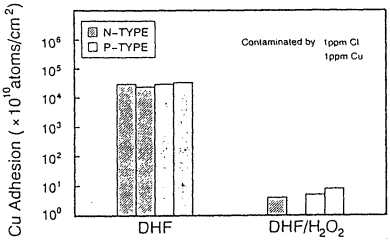


Figure 10 The effect of $HF/H_2O_2/H_2O$ (FPM) cleaning

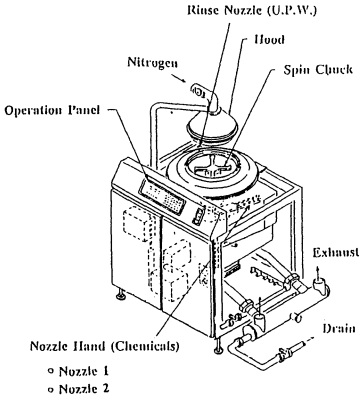


Figure 11 Nitrogen gas sealed spin cleaner

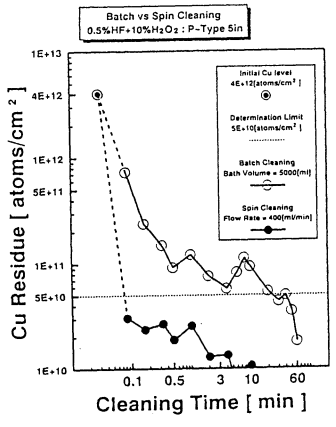


Figure 12 The cleaning time dependence on Cu removal efficiency with the spinning method and the batch method

A NEW CLEANING CONCEPT FOR PARTICLE AND METAL REMOVAL ON Si SURFACES

M. Meuris, S. Verhaverbeke[1], P.W. Mertens,
H.F. Schmidt, A.L.P. Rotondaro, M.M. Heyns,
IMEC, Kapeldreef 75, 3001 Leuven, BELGIUM, E.C.

and A. Philipossian[2]
Digital Equipm. Corp., 77 Reed Road, Hudson, MA, U.S.A.

In this study the IMEC Clean Concept will be proposed. It is a simple two-step cleaning, based on a oxidation step and an oxide removal step. It is demonstrated that this clean performs excellent regarding the particle and metal removal efficiencies, combined with a minimal surface roughness. Electrical breakdown measurements show also very good performance of the gate-oxide integrity after this clean.

1. Introduction.

The RCA-clean (SC1+SC2) [1] is the most widely used cleaning recipe in silicon processing. Since its original publication in 1970 several modifications were introduced to improve its cleaning efficiency. During last years most research effort concentrated on a better understanding of the SC1-step of the RCA-clean, which originally consisted of a $NH_4OH/H_2O_2/H_2O$ mixture of a (1/1/5) ratio at 85-90°C.

Although the particle removal efficiency of the SC1 step is excellent, it was revealed that this SC1 step may cause several problems. The metal contamination resulting from this step may be very high and a one-to-one correlation between the metal concentration of the SC1 bath and the metal contamination of the silicon surfaces was found [2,3]. A second problem is caused by the continuous etching of this step resulting in the roughening of the silicon surface [4–6]. Recently a correlation between some specific metal contamination and the decomposition of hydrogen peroxide in this mixture was revealed [7]. This decomposition will lead to the formation of light point defects measured with laser scattering (LPDs) on the wafer and can be correlated with reduced gate oxide integrity in the LPD regions.

To prevent these problems, the control of the SC1 treatment regarding the ratio, temperature and metal contamination needs to be extremely stringent to make it a

[1]present address: Prof. Ohmi's Lab., Tohoku Univ., Sendai, Japan.
[2]present address: Intel Corporation, Santa Clara, CA.

reliable cleaning mixture in todays silicon circuit manufacturing. The control of this cleaning step becomes a serious manufacturability issue. Further, it increases the cost of the cleaning of silicon wafers, by the necessity of sub-ppb metal contamination specifications of chemicals. This also implies that extreme care should be taken not only to the chemicals, but also to prevent metal contamination sources in the SC1 bath from the tank and cassette material and even from the silicon wafers itself.

Therefore, micro-electronic industry is searching for new chemical mixtures, which makes the cleaning sequence in a manufacturing line more cost effective. This can be achieved by reducing the chemical cost (more dilute chemical mixtures and/or less stringent specifications) or by reducing the time of the cleaning (more effective use of the baths). In this study it will be shown that by the understanding of the particle removal mechanism on silicon wafers it is possible to formulate more cost-effective cleaning recipes.

2. The IMEC Clean Concept.

During last years, the ratio and temperature of the SC1 step were optimised by balancing the reduction of the silicon surface roughening (decreasing the etch rate) and keeping an equal particle removal efficiency (minimal etch rate necessary). A (0.05/1/5) NH_4OH/H_2O_2 ratio at 85-90°C [4] and a (0.25/1/5) ratio at 70-75°C [6] were proposed. In Fig. 1 the amount of thermal oxide etched during 10 min. for the two different ratios as a function of the temperature is plotted. For both "optimised" SC1 mixtures the etch speed of thermal SiO_2 is equal and approximately 0.2 nm/min [6]. From these data the question arises if the particle removal is caused by a minimal etch rate or if only a certain etched depth is required to undercut the particles and lift off from the silicon surfaces into the chemical liquid.

In Fig. 2 the particle removal efficiency is shown as a function of thermal oxide etched depth for various SC1 mixtures. The etch rates of thermal oxide varied from 0.2 nm/min down to 0.05 nm/min in this experiment. The etch rate was measured on thermal oxide wafers by ellipsometry. At various immersion times wafers were taken out of the SC1 bath and measured for particle removal efficiency of controlled particle contaminated wafers. A non-optimised HF-last procedure was used for the particle contamination. Note that the total immersion time to reach a thermal oxide etched depth of 3 nm for the lowest etch rate was 60 min. Anyhow, the particle removal efficiency is independent on the etch speed. It reaches a value of 0.80-0.90 as soon as 1.5-2 nm is removed.

In the SC1 mixture particles are removed by the continuous oxidising effect of the H_2O_2 and dissolution or etching effect of the NH_4OH. Due to this action, the particles are undercut and lift-off. Because oxidation and etching takes place at the same time in the same bath, it is difficult to control the roughening effect of this

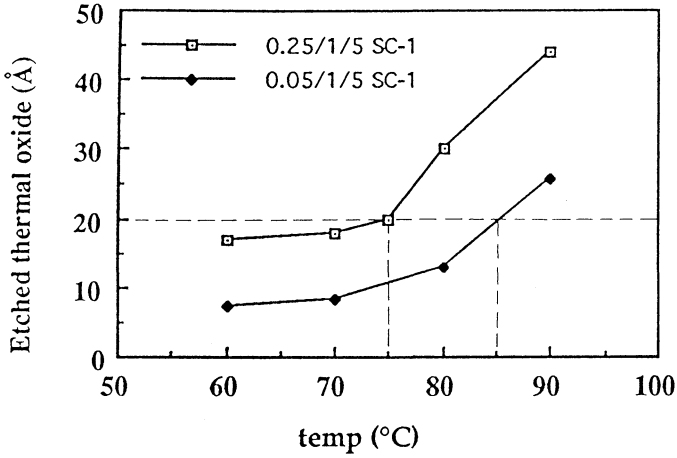


Figure 1: etched thermal oxide per 10 minutes immersion time for two different $NH_4OH/H_2O_2/H_2O$ mixtures as a function of temperature.

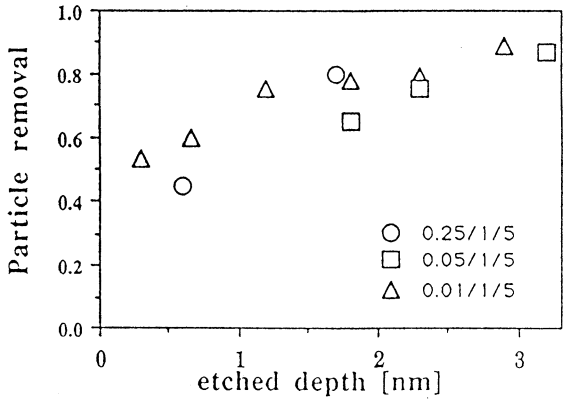


Figure 2: Particle removal efficiency (øLSE >0.5 μm) as a function of etched thermal oxide depth for different $NH_4OH/H_2O_2/H_2O$ mixtures at 70°C. Etch speed: (○) (0.25/1/5) ratio, 0.2 nm/min; (□) (0.05/1/5) ratio, 0.1 nm/min; (△) (0.01/1/5) ratio, 0.05 nm/min.

Table I: The IMEC-Clean Concept *Step 1:* growth of about 1.5 nm chemical oxide; *step 2:* removal of the oxide; *optionally step 3:* make a hydrophilic Si surface before drying; *drying* procedure.

step 1 oxide growth	step 2 oxide removal	(step 3) optional	drying
• H_2SO_4/H_2O_2 • H_2SO_4/O_3 • H_2O/O_3 • UV-O_3	• wet DHF • HF vapour + rinsing	• clean chemical oxide growth	• IPA-vapour • Marangoni • spin dry • hot DI-water

mixture.

On the basis of this knowledge, we propose a new cleaning concept. In the IMEC-clean concept the oxidising and the etching action of the silicon surface is separated. This is summarized in Table I. In step 1 an oxide is grown. In step 2 this oxide is etched away selectively versus the silicon. The total etched depth should be sufficient to remove the particles. This means that the chemical oxide grown in step 1 should be sufficiently thick. The advantage of separating the cleaning in two steps is that formation of the oxide layer is a self-limiting process. So, the thickness of the chemical oxide will be very uniform. In step 2 this chemical oxide is etched selectively versus the silicon, resulting in an easy control of the Si surface roughness.

The only requirement for step 1 is the growth of an oxide of a minimal thickness (about 1.5-2 nm). For step 1 a H_2SO_4/H_2O_2 mixture can be used. Also ozonated mixtures are possible: H_2SO_4/O_3, H_2O/O_3 [8] or UV-O_3. Another benefit of step 1 is the removal of organic contamination by the oxidising power of the mixture.

In step 2 this chemical oxide is removed selectively. The most logical choice is an HF based etchant. This step has to be optimised in such a way that a high passivation of the silicon surface is obtained (high contact angle, delayed regrowth of native oxide), that the silicon surface is not roughened (use of surfactans or other additives) and that high selectivity vs. thermal or deposited oxide layers is obtained (cleaning of patterned wafers).

After the cleaning the wafers have to be dried. When a good drying technique is available for hydrophobic surfaces, no pretreatment of the silicon surface is required and one can proceed to the drying step immediately.

In the other case, when hydrophilic wafers are preferred, a very clean chemical oxide can be grown by using e.g. ozonated DI-water, or an H_2O_2 based mixture. Note, that this optional step is very critical regarding roughening and metallic contamination. So, this optional step has to be optimised in such a way that a low

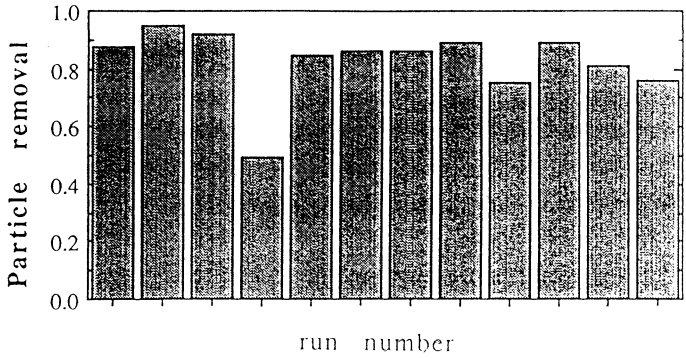


Figure 3: Particle removal efficiency (øLSE > 0.5 μm) for different runs of a $NH_4OH/H_2O_2/H_2O$ (0.25/1/5) mixture at 70°C.

particle and metal contamination and small roughening occur. A diluted SC1 mixture and a short immersion time was very suitable to grow a clean chemical oxide on the silicon surface and maintain a low particle density in our experimental set-up.

3. Results.

3.1 Particle removal

Our particle removal model of silicon surfaces predicts that every cleaning mixture, which etches about 2 nm of thermal oxide will result in sufficient particle removal. Experiments were designed with different etching treatments of the silicon surface. Controlled particle contamination of 125mm wafers was performed. *HF-last:* Wafers with particles from an HF-last treatment followed by a non-optimised rinse dry procedure (wafer surface is hydrophobic); *Latex spheres:* Wafers were contaminated with latex spheres of the size of 0.2, 0.3 and 0.63 μm in diameter (wafer surface is hydrophilic); *silica:* Wafers were contaminated with 0.2 μm diameter silica particles. Particle densities were measured with a Censor ANS100 instrument. Particle removal efficiencies were calculated as
$(Particles_{before} - Particles_{after}) / Particles_{before}$.

A. SC1 mixture: The SC1 mixture is in the first place used for particle removal. Therefore a particle removal efficiency base line was established by performing several SC1 cleans. In Fig. 3 the particle removal efficiency (øLSE >0.5 μm) is plotted for a SC1 (0.25/1/5) mixture at 70 °C for 10 minutes, each datapoint is taken from a separate cleaning experiment. The average particle removal efficiency of the SC1

Table II: Particle removal efficiency of particle contaminated wafers as a function of the particle type and size after SPM-DHF treatment.

type	diameter LSE (μm)	original number per wafer	removal efficiency
latex	0.18-0.24	690 $\pm$ 10	0.90 $\pm$ 0.02
spheres	0.27-0.33	698 $\pm$ 5	0.98 $\pm$ 0.03
	0.55-0.70	24 $\pm$ 2	0.95 $\pm$ 0.05
HF-last	0.18-0.7	1130 $\pm$ 120	0.92 $\pm$ 0.05
silica	0.18-0.24	750 $\pm$ 50	0.97 $\pm$ 0.02

step is 0.86 $\pm$ 0.06 (one excursion excluded). The etched thermal oxide depth of this treatment is about 2 nm.

B. IMEC Clean concept: Step 1 of the IMEC clean was taken as a variable. Step 2 consisted of a 2 min 0.5%HF/0.1%IPA in H_2O mixture at room temperature, followed by 10 min rinsing. No dry was used. The hydrophilic wafers were transferred into a dry cassette and measured.

B1. H_2SO_4/H_2O_2 mixture: As step 1 we used a 2 min H_2SO_4/H_2O_2 (4/1) mixture at 90°C, followed by a 10 min DI-water rinsing in an overflow bath. In Table II the particle removal is shown for different types of particles. The particle addition of this experiment was 32 $\pm$ 8 particles per 125mm wafer (øLSE >0.18 μm). The particle removal efficiency of this cleaning is at least performing as good as an optimised SC1 clean. The chemical oxide of a H_2SO_4/H_2O_2 mixture is about 1.3 nm measured with AFM [9]. Spectroscopic ellipsometry indicates 2.0 nm for the chemical oxide thickness.

B2. UV/O_3: UV/O_3 was used as a dry alternative for step 1 of the IMEC clean concept. The particle removal efficiency of (øLSE > 0.3 μm) is 0.83 $\pm$ 0.05. The chemical oxide thickness of the UV/O_3 is 2.2 nm measured with spectroscopic ellipsometry. The apparent lower particle removal efficiency compared with a SPM treatment we attribute to the fact that during the UV/O_3 step in our experimental set-up a few hunderd of particles were added. It decreases the calculated particle removal efficiency.

C. SC2+DHF clean: The importance of the chemical oxide thickness grown in step 1 is illustrated by experiments with a SC2 + DHF sequence. In this case we used (1/1/5) $HCl/H_2O_2/H_2O$ mixture at 70 °C for 10 minutes followed by an equivalent DHF treament of paragraph B. The particle removal efficiency was only 0.25 $\pm$ 0.15. This can be easily explained because since only a 0.6 nm thick chemical oxide is grown in the SC2 mixture [9].

D. Spray processor: The question of the difference between a cleaning in a wet

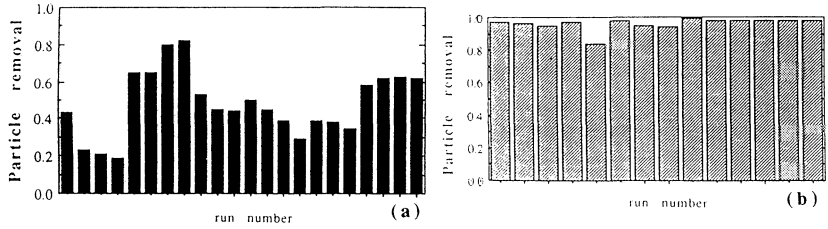


Figure 4: Particle removal efficiency (øLSE $>$ 0.5 μm) for different runs of a spray processor (a) RCA-clean (SC1-SC2), (b) SPM-DHF-SC1-SC2 cycle

bench (tank) and a spray cleaning tool often arises. In Fig. 4a the particle removal efficiency is given for a RCA cleaning (SC1-SC2) in a spray processor. It is not very high and also not reproducible. Similar data were also measured when using a SC1-only recipe in the spray tool. This can be understood since the SC1 step is short ($<$ 120 sec) and, more important, the temperature of the mixture when it reaches the silicon wafer is below 50 °C. This results in a etched depth of thermal oxide of about 0.5 $\pm$ 1.5 nm. The observation that this etching is very non-uniform over the silicon wafer further explains the irreproducibility of the particle removal efficiency of this cleaning sequence in the spray processor. However, in Fig. 4b it is shown that the particle removal efficiency of a SPM-DHF-SC1-SC2 cycle in the same equipment results in very reproducible and high particle removal efficiencies. The etched depth of this particular 4-step cycle is 4.4 $\pm$ 0.5 nm of thermal oxide. The particle removal efficiency is $>$ 0.95. It confirms the particle removal model explained in section 2.

Further, in Fig. 5 the particle removal efficiency is shown for two cleaning sequences. One sequence consists of a SPM-DHF cycle. It is well known that HF-last cycles in a spray tool equipment result in very high particle addition. In this particular experiment the treatment was stopped before the drying cycle. The wafers were taken out of the equipment in the wet cassette and transferred to a dry cassette. After this treatment low particle densities and a high particle removal efficiency were measured as indicated in Fig. 5. Although this procedure is not suitable for manufacturing, it proves again the validity of the IMEC clean concept. However, the problem of the spray tool is to dry hydrophobic surfaces without particle addition. As a second cleaning sequence a SC1 cycle was added to the SPM-DHF cleaning cycle and now the wafers were dried with a conventional spin-dry recipe of the spray tool. In this case the spray processor can dry the wafers with low particle densities and so, high particle removal efficiencies were found. Note that the conventional

Table III: Metal contamination (in 10^{10} at.cm^{-2}) after IMEC vs. RCA+HF clean.

cleaning treatment	Ca	Fe	Cu	Zn
original metal level	15	1	2	1
IMEC	0.7	0.3	<0.1	0.7
RCA+HF	2.5	0.8	0.5	4.9
5×(IMEC) + HF	<0.1	<0.1	<0.1	0.1
5×(RCA) + HF	4.5	0.3	<0.1	0.3

SPM-DHF-SC1-SC2 cycle of a spray tool is infact a SPM-DHF cleaning cycle and the SC1-SC2 cycle is only necessary to grow a clean chemical oxide (step 3 of the IMEC clean concept, Table I), whereafter the wafers are spin-rinse-dried.

3.2 Metal removal

In a previous study [10] a HF-last procedure before gate oxidation was proven to be very effective for removing the metallic contamination. In Table III the metallic contamination after a RCA+HF-clean and after an IMEC-clean is shown. Less metallic contamination is present after the IMEC-clean. When the cleaning sequence is repeated five times similar results are observed, but the repeated cleaning cycles result in lower metal contamination. The reason that a SPM-DHF cycle has the lowest metal contamination can be understood since in this clean only acid mixtures are present and these tend to keep metals in solution. Note also that after the IMEC-clean a lower Cu contamination is measured compared with the RCA+HF clean. This is consistent with the observation reported by F. Derouin et al. [11].

3.3 Roughness

For the roughness measurements the cleaning treatments were repeated 5 times to increase the roughening effect of the cleaning. Note that also the drying step is performed after each cleaning sequence [in total 5 x (clean+dry)] Following cleaning cycles were used.

IMEC: As step 1 we used a 2 min H_2SO_4/H_2O_2 (4/1) mixture at 90°C, followed by a 10 min DI-water rinsing in an overflow bath. Step 2 consisted of a 2 min 0.5%HF/0.1%IPA in H_2O mixture at room temperature, again followed by 10 min rinsing and no dry.

IMEC+1minSC1: a second cleaning sequence consisted of this IMEC clean and a 1 min SC1 treatment was added as the optional step 3 to obtain a hydrophilic surface before drying. The wafers were spin dried.

RCA: The RCA-clean consisted of a 10 min SC1 treatment [(0.25/1/5) ratio at 70°C] + 10 min SC2 treatment [(1/1/5) ratio at 70°C] with rinsing equal to the IMEC-clean. Note that especially for this RCA-cleanings great care was taken not to introduce any metal contamination in the baths. Wafers were dried in the spin

Table IV: *Silicon surface roughness measured with AFM. The r.m.s. value and Δz (peak-to-valley) value were measured on 4 different areas. Area = 1 × 1 μm^2.*

cleaning treatment	rms-z (nm)	Δz (nm)
no clean	0.15 ± 0.02	1.5
5 × (IMEC) + HF	0.19 ± 0.02	2.9
5 × (IMEC+1min.SC1) + HF	0.23 ± 0.02	2.6
5 × (RCA) + HF	0.36 ± 0.01	4.2
5 × (SPRAY) + HF	0.24 ± 0.01	3.1

Table V: *Defect density of 15 nm gate-oxide capacitors grown on EPI-wafers (0.15 cm^2; voltage ramp breakdown; breakdown field > 12 MV/cm). After the cleans all wafers went to the same HF-last, rinsing and drying procedure and underwent the same processing.*

cleaning treatment	defect density (cm^{-2})
IMEC	1.3 ± 0.3
RCA+HF	1.4 ± 0.3
5×(IMEC) + HF	2.1 ± 0.6
5×(IMEC+1min.SC1) + HF	1.7 ± 1.1
5×(RCA) + HF	3.0 ± 1.8
5×(SPRAY) + HF	2.8 ± 2.1

dryer.

SPRAY: A conventional SPM-DHF-SC1-SC2 cycle was used in a spray processor.

After the 5 × four different cleanings all wafers underwent a DHF treatment, identical to step 2 of the IMEC-clean. The chemicals used in all these cleanings were of a <1 ppb metal content specification (except HCl and H_2SO_4 < 10 ppb).

Table IV summarizes the AFM measurements. As can be derived from these results, the IMEC-clean has a small effect on the Si surface roughness even after 5 repeated cleans.

3.4 Electrical results

Finally, in Table V the defect density of capacitor structures (0.15 cm^2) with 15 nm gate oxides are shown. The cleaning cycles were equal to the ones used for the AFM measurements. Note that the yield definition is very severe, since only capacitors surviving fields of 12 MV/cm are taken as good capacitors. Gate oxides were grown at 950°C in dry oxygen with no chlorine addition. The IMEC-clean shows equivalent or better breakdown properties compared with RCA+HF-clean. Also when the cleaning is repeated 5 times the gate oxide integrity of the IMEC-clean remains excellent.

4. Conclusions - Advantages of the IMEC Clean Concept.

It was shown that the IMEC Clean Concept results in high particle and metal removal efficiencies and low Si surface roughening (even after repeated cleans).

Since only acid mixtures are used, the lattitude of the clean regarding metallic contamination of the baths is less severe compared with the SC1 step.

An important issue is the total cleaning time. Step 1 and step 2 can be performed within 1 or 2 min. By using a combination of megasonic and quick-dump DI-water rinsing, the rinsing time can also be reduced to 2 to 3 minutes. This opens the perspective of a clean with a total time of less than 15 minutes.

Another advantage is that the cleaning concept reduces the consumption of chemicals and in this way also the chemical waste.

Last but not least, it was shown that the IMEC Clean Concept result in excellent breakdown properties of gate oxides.

Acknowledgments

Digital Equipment Corporation, Wacker-Chemitronic, ASM, BOC (Airco), Ashland Chemicals, Texas Instruments and INTEL Corporation are greatly acknowledged for scientific and financial support. Part of the work was supported by the European Community (ESPRIT). The work at Wacker-Chemitronic was supported by the F.R. Germany under contract M 2793 F. A. Opdebeeck, M. Dulst, K. Kenis, P. Boelen, H. Van de plas, J. Van den Berghe, J. Mattheesen (KIH De Nayer) and J. Ballings (KIH Limburg). are acknowledged for technical assistance. Professors R. Van Overstraeten and G. Declerck are acknowledged for their continuous support of the IMEC Ultra Clean Processing group. L. Hellemans and J. Snauwaert of the Katholieke Universiteit Leuven are acknowledged for the AFM work.

References

[1] W. Kern and W. Puotinen, RCA Review **31**, 187 and 207 (1970).
[2] R. Takizawa, and A. Ohsawa, Proc. 1st Int. Symp. Cleaning Technol., 176th ECS Meeting 1989.
[3] M. Meuris, M. Heyns, W. Küper, S. Verhaverbeke, and A. Philipossian, Proceed. 178th ECS Meeting, Washington, DC (1991), p. 488.
[4] T. Ohmi, M. Miyashita, M. Itano, T. Imaoka, and I. Kawanabe, IEEE Trans. on El. Dev. **39**, 537(1992).
[5] M. Meuris, S. Verhaverbeke, P.W. Mertens, M.M. Heyns, L. Hellemans, Y. Bruynseraede, and A. Philipossian, Jpn. J. Appl. Phys. **31**, L 1514 (1992).
[6] M. Meuris, M.M. Heyns, P.W. Mertens, S. Verhaverbeke, and A. Philipossian,

Microcontamination, May 1992, p.31 (1992).
[7] H. F. Schmidt, M. Meuris, P.W. Mertens, S. Verhaverbeke, M. Kubota, M.M. Heyns, and K. Dillenbeck, Proceed. IES Annual Techn. Meeting, Las Vegas, Nevada (1993), p. 238.
[8] T. Isagawa, T. Imaoka, M. Kogure, H. Shimada, and T. Ohmi, Proceed. IES Annual Techn Meeting, Nashville, Tennesee (1992), p. 466.
[9] S. Aoyama, Y. Nakagawa, and T. Ohmi, Proc. 16th Symp. on UCT, Tokyo, July 1992, p. 19 (1992).
[10] S. Verhaverbeke, M. Meuris, M. Schaekers, L. Haspeslagh, P.W. Mertens, M.M. Heyns, R. De Blank, A. Philipossian, Proc. of 1992 Symp. on VLSI Techn., Digest of Techn. papers, p. 22 (1992).
[11] F. Derouin, Proceed. IES Annual Techn. Meeting, Las Vegas, Nevada (1993), p. 460.

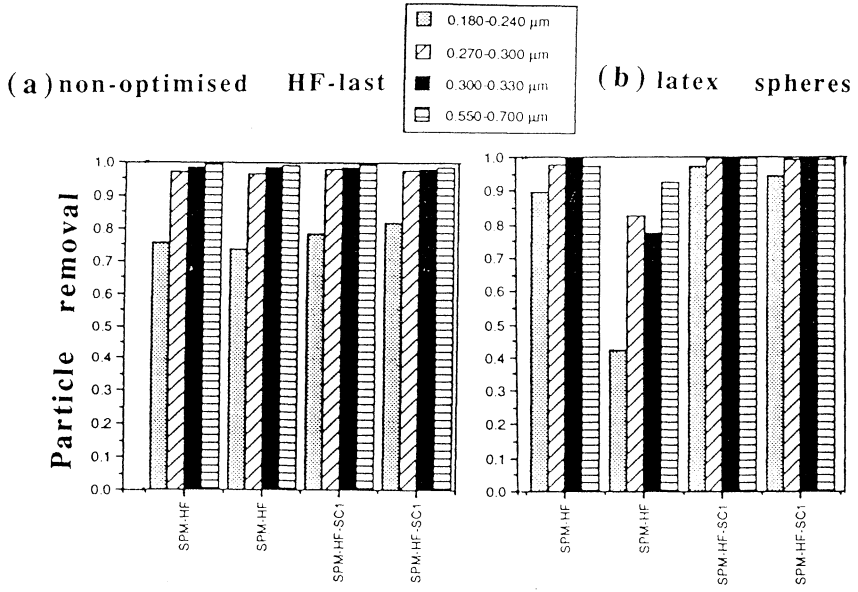


Figure 5: Particle removal efficiency of a spray processor (a) particle contamination from HF-last followed by a non-optimised drying; (b) contamination from latex spheres. SPM-HF: After the SPM-HF cycle the wafers were taken out of the tool without drying. SPM-DHF-SC1: a SC1-step was added after the SPM-DHF cycle and the conventional drying cycle was used.

ELECTROCHEMICAL EQUILIBRIUM OF Fe IN ACID/BASE/PEROXIDE SOLUTIONS RELATED TO Si WAFER CLEANING

C. R. Helms and Heungsoo Park
Department of Electrical Engineering, Stanford University, Stanford, CA 95305

In this paper we show that the equilibrium properties of Fe dissolved in water in the presence of oxidizing agents such as H_2O_2 lead to instabilities that can explain the deposition of Fe on Si surfaces during SC1 cleaning as well as during rinse cycles. The wafer surface acts as a heterogeneous nucleation site for the precipitation of Fe_2O_3 from supersaturated solutions of Fe^{3+} ion. It can also be shown that the tendency to produce Fe^{3+} leads to another instability where the decomposition of H_2O_2 to O_2 and H_2O is catalyzed.

INTRODUCTION

The process of removing various types of contamination from a wafer surface is highly dependent on the chemical nature of the contaminant and its physical location, both in macroscopic as well as nanoscopic terms. We have shown [1-4] that a metals chemical nature is critical in determining how effective a particular clean will be in removing it. For example, metals contained in metal salts or oxides on the surface are relatively easy to remove, whereas those bonded directly to the surface Si require a more extensive chemical sequence and are generally more difficult to remove. Possible locations, and therefore chemistries, of metals are illustrated in Fig. 1. Two cases are shown in the two columns, the left for a "clean" Si surface, such as might be expected for an HF-last surface (possible hydrogen termination left out for simplicity), and the right for a surface with a native oxide present. For metal atoms on the surface for these two cases, two very different bonding configurations might be expected, an intimate metal/Si bonding for the clean surface case or a metal/oxygen bonding for the case of the native oxide. To remove the metal from the clean surface, the metal/Si bond must be broken; to remove the metal from the native oxide surface, the metal may be already oxidized and therefore easily dissolved in a low pH solution or one containing an appropriate complexing agent. For metal in but near the surface, similar bonding issues need to be considered. In addition it is clear from the diagram that some Si must also be removed to access the metal atoms. This is an indication of the value of alternate sequences that oxidize the Si in a first step and then strip the oxide in the second step; this last step therefore will always require HF or other SiO_2 etch. The final type of chemistry that we encounter is shown at the bottom of the figure, where the metal is depicted as being present as a metal salt. This is the case we might expect for many metals deposited on the Si surface out of solution such as Fe_2O_3 A guide to understanding metal surface bonding can be obtained from the bulk metal/oxygen/Si ternary phase diagrams. One such phase diagram for Fe is shown in Fig. 2 [2,3] along with a diagram illustrating where different forms might be expected. Note in this diagram the existence of silicates has been included; in past publications we have neglected the silicates for simplicity. Possible distributions of Fe and the corresponding region of the phase diagram are also shown in the figure. An effective clean must be capable of removing all of the chemical forms shown. This is only part of the cleaning problem; the remainder is determining under what conditions the Fe will dissolved in solution and be stable enough to resist plateback. The remainder of the paper will deal with this issue for Fe in solution as a function of pH and peroxide concentration in solution.

CHEMICAL CONCEPTS

In very simple terms the removal of metals from the Si surface can be described by the following "reaction":

$$(\text{Metal})_{\text{adsorbed}} + \text{Reactants} \Leftrightarrow (\text{Metal})_{\text{dissolved}} + \text{Reaction Products} + \text{Surface Residue} \quad (1)$$

The chemistry of the metal adsorbed on the Si surface is determined by its bonding to the surface region as discussed above. It can be in the form of the element, its oxide, hydroxide, other salts, silicides, silicates, or organometallic compounds and carbides. Since we are dealing with individual atoms in many cases, the concept of a compound, such as a silicide, may not be entirely correct. However, for numerous cases in surface science, the binding of an "adsorbate" can be closely associated with a similar bulk compound [5]. In the case of "silicide-bonded" metal, we refer to the metal with Si nearest neighbors, whose binding energy might be expected to semi-quantitatively determined by the bond strengths in the corresponding silicide.

The goal of a cleaning process, of course, is to convert the adsorbed metal into its soluble form. High solubility's normally are found only for oxidized forms of metals, typically as the metal ions, hydroxylated ions ($HFeO_2^-$, $Fe(OH)_2^+$, ...), and complexes ($CuCl_2^-$, TiF_6^{-2}, ...) [6,7]. Therefore a major role of the reactant must be to oxidize the metal or provide an environment to keep it in an oxidized, soluble form. This is in competition with the equilibrium between insoluble oxides (hydroxides) and the soluble oxidized forms. Thus low pH solutions (high oxide solubility) coupled with oxidizing agents (H_2O_2, HNO_3, ...) are commonly employed for metal removal.

We will now present an analysis of the electrochemical properties of Fe in solutions as a function of pH and dissolved oxygen concentration (or H_2O_2). From this analysis it is easy to see why the reaction above is driven to the left in all situations except for very low pH. In addition, the analysis predicts that the deposited Fe should be in an oxidized from (probably as a Fe^{3+} ion). This also indicates that the deposited Fe should be easily removed in a subsequent low pH step, since the Fe^{3+} ion is quite soluble in these solutions.

The discussion in this paper will relate to the thermodynamics of the system. The kinetics of the chemical process is also critical. For example, if a metal is buried in or under a native oxide, favorable thermodynamics, although necessary, may be unimportant; the effectiveness of the cleaning chemistry may be determined by the kinetics of the leaching of the metal through the oxide or the removal of the oxide entirely. This is the reason that HF has been demonstrated to be effective for metal removal [1,2,8,9]. On the one hand HF can provide a low pH environment leading to high metal ion solubility and on the other it provides a mechanism to dissolve the native oxide that may be passivating not only the Si but adsorbed metal. In addition although we will show that Fe is thermodynamically stable dissolved in many cleaning solutions, the rate at which it precipitates is obviously quite slow. It seems likely that the Si surface provides a heterogeneous site for the nucleation of the precipitated phase, leading to the strong plateback effect observed in the literature [10].

The solubility of Fe

In contact with aqueous solutions Fe will exist as an oxide or hydroxide. Although there are other possible oxides, we will limit this discussion to Fe_2O_3 (Fe^{+3}) and $Fe(OH)_2$ (Fe^{+2}), the most stable forms in contact with water and oxidizing agents. Given one of

these solid forms the solubility of the Fe^{+2} and Fe^{+3} can be determined by the following reactions [6,7]:

$$1/2Fe_2O_3 + 3H^+ \Leftrightarrow Fe^{+3} + 3/2H_2O \quad (2)$$

$$Fe(OH)_2 + 2H^+ \Leftrightarrow Fe^{+2} + 2H_2O \quad (3)$$

This leads to equilibrium concentrations at room temperature given by:

$$[Fe^{+2}] = 1.95 \times 10^{(13-2pH)}$$

$$[Fe^{+3}] = 0.19 \times 10^{(-3pH)}$$

Unfortunately there are additional forms of Fe that must also be considered. These are $HFeO_2^-$, $FeOH^{+2}$, and $Fe(OH)_2^+$, the first being in the +2 oxidation state the last two in the +3 state. The appropriate equilibrium reactions are:

$$HFeO_2^- + 3H^+ \Leftrightarrow Fe^{+2} + 2H_2O \quad (4)$$

$$FeOH^{+2} + H^+ \Leftrightarrow Fe^{+3} + H_2O \quad (5)$$

$$Fe(OH)_2^+ + 2H^+ \Leftrightarrow Fe^{+3} + 2H_2O \quad (6)$$

These lead to equilibrium relationships:

$$\frac{[HFeO_2^-]}{[Fe^{+2}]} = 2.63 \times 10^{(3pH\ -32)}$$

$$\frac{[FeOH^{+2}]}{[Fe^{+3}]} = 3.7 \times 10^{(pH\ -3)}$$

$$\frac{[Fe(OH)_2^+]}{[Fe^{+3}]} = 7.59 \times 10^{(2pH\ -8)}$$

The total Fe concentration in solution can be determined by the sum of the concentration of the various forms. This is shown in Fig. 3 as a function of pH. For trivalent Fe the Fe^{+3} form dominates for the range of pH shown. For the divalent case, high solubility for low pH is obtained for Fe^{+2} itself, whereas at high pH the $HFeO_2^-$ form dominates. In looking at these curves we might therefore expect that Fe has a solubility greater than 1 ppb for all conditions (minimum in the Fe^{+2} curve). However we must also include the equilibrium between the Fe^{+2} and Fe^{+3} forms themselves.

Fe Solution Equilibrium

The equilibrium between the Fe^{+2} and the Fe^{+3} forms is determined by the concentration of available oxidizing agents and can be represented by the following reactions for cases of interest:

$$Fe^{+2} + H^{+} + 1/2H_2O_2 \Leftrightarrow Fe^{+3} + H_2O \quad (7)$$

$$2Fe^{+2} + 2H^{+} + 1/2O_2 \Leftrightarrow 2Fe^{+3} + H_2O \quad (8)$$

$$2Fe^{+2} + 2H^{+} + O_3 \Leftrightarrow 2Fe^{+3} + O_2 + H_2O \quad (9)$$

Note the equilibrium depends on the concentration of an appropriate oxidizing(or reducing) agent for the system to be completely specified. In aqueous solutions we must use the appropriate free energy for the dissolved species in equilibrium with the appropriate partial pressure of the species in the gas phase. In equilibrium one reaction can be easily converted to anther. However, these reactants are seldom in equilibrium. H_2O_2 for example is thermodynamically unstable except in equilibrium with enormous O_2 partial pressures. For simplicity we will deal exclusively with the first reaction; this is appropriate since many cleaning solutions contain H_2O_2 in any case. The effect of dissolved O_2 will be quantitatively similar. The relationship between concentrations and free energies for the first reaction can be written as:

$$\frac{[Fe^{+2}][H_2O_2]^{.5}}{[Fe^{+3}]} = 1.5 \times 10^{(pH\ -17)}$$

The ratio of Fe^{+2} and Fe^{+3} is shown in Fig. 4 as a function of pH for various H_2O_2 concentrations. It is seen that the Fe^{+3} is favored down to extremely low H_2O_2 concentrations for all ranges of pH. Applying this to Fig. 3 we see that the Fe^{+2} form will tend to be converted to the Fe^{+3} form by even minute amounts of peroxide present. The solubility of the Fe overall is therefore much better described by the Fe^{+3} curve by itself. This being the case the solubility of Fe in typical cleaning solutions above pH of about 4 is quite low leading to a driving force for the precipitation of Fe_2O_3. The kinetics of the process may however lead to reaction rates that are so slow as to effectively stop the equilibration. In this case it is likely to find Fe^{+2} in supersaturated concentrations for peroxide (or dissolved O_2, or dissolved O_3) containing solutions.

Peroxide Decomposition Effects

Give the above analysis there is an additional effect to be considered, peroxide decomposition. H_2O_2 is, of course, thermodynamically unstable with regard to decomposition to H_2O_2 and O_2. The presence of the Fe3+ ions predicted above can lead to an acceleration of this decomposition as has been observed in recent work [11]. The reaction of interest is:

$$Fe^{+3} + 1/2H_2O_2 \Leftrightarrow Fe^{+2} + H^{+} + 1/2O_2 \quad (7)$$

This reaction is thermodynamically driven to the right, especially at high pH. If we compare to reaction (7) above we see that one scenario is the catalytic decomposition of the

H_2O_2 by the presence of Fe in solution. This points out the difficulty of analyzing a system that is fundamentally unstable (H_2O_2) using equilibrium analysis. In the present case there will be a competition between the precipitation of Fe and the catalytic decomposition of the H_2O_2 to H_2O and O_2.

Relationship to Cleaning

To see how these effects may be important in cleaning we will consider a few examples. First let us imagine we start with NH_4OH with 10 ppb Fe impurity; this would be in the form of $HFeO_2^-$. This is now mixed with H_2O and H_2O_2 to form a cleaning solution. The addition of the H_2O_2 leads to a driving force for the conversion of the $HFeO_2^-$ to Fe^{+3}. The Fe^{+3} is itself unstable with respect to the precipitation of Fe_2O_3 at the high pH's present. Kinetics however may limit the conversion of Fe^{+2} to Fe^{+3} as well as the precipitation of the Fe_2O_3. The immersion of Si wafers into the solution now provides for the possibility of heterogeneous nucleation of the Fe_2O_3 form on the Si surface. This explains the Fe plateback effect without the need to invoke an additional chemical iteraction with the Si itself; the Si for this mechanism serves only as a catalyst for the precipitation reaction.

As another example let us consider an $HCl:H_2O_2:H_2O$ solution with 1 ppb Fe present. For pH< 2 the Fe will be stable in solution in the Fe^{+3} form. Now we expose wafers to the solution, remove and attempt to rinse. The rinse will cause the pH of any carried over chemical to be driven to near 7; in the process the solubility of the Fe is considerably reduced, leading to the possibility of precipitation driven plateback.

CONCLUSIONS AND RECOMMENDATIONS

A detailed understanding of the metal cleaning problem defined by equation (1) requires a knowledge of the Si metal interaction as well as the solution chemistry. In this paper we have presented a model by which the solution chemistry side of the problem can be understood for Fe. It suggests that high pH solutions with oxidizing agents present can lead to Fe plateback through simple heterogeneous precipitation of Fe_2O_3. To alleviate this effect altogether, Fe concentrations in the bases must be kept to a value below what is practical. Some Fe plateback from these solutions must therefore be expected. To remove this metal such cleans must be followed by a low pH treatment which redesolves the Fe_2O_3. Even in this case some Fe plateback due to the pH swing caused by a subsequent rinse may be expected. This leads to a scenario whereby sequential dilution's of the dissolved Fe by low pH cleans followed by rinses will lead to lower and lower surface concentrations as more clean/rinse cycles are added.

An additional mechanism suggested by other workers is the electrochemical replacement of a Si atom on the surface by the metal atom with oxidation and dissolution of the silicon. although this is possible and probably occurs in some cases, our analysis shows an additional channel for metal plate back that does not require dissolving Si. In this regard, however, a few comments are appropriate concerning the use of electronegativity and/or half cell potentials to predict such effects. It has been suggested that metals that are more electronegative than Si (or have larger half cell reduction potentials) will tend to plate out due to a simple oxidation/reduction reaction [12]. This would be true if the dominant soluble species are the elemental ions. This is not the case for Si or the more electronegative metals; the typical soluble species for some of these are: $AuCl_4^-$, $PtCl_4^{-2}$, $HgCl_4^{-2}$, $HCuO_2^-$, $CuCl_2$, SiF_6^{-2}, $HPbO_4^-$, and $HSnO_4^-$ [5,6]. A prediction of the details of the plating reaction must consider the equilibrium and kinetics of the set of

reactions involving these species. The kinetics are particularly important as the Si surface may catalyze the plating reaction even though it is not directly involved in the overall reaction itself.

Unfortunately, the process of cleaning a Si wafer requires not only the removal of metals but also organics, particles, and in some cases native oxide. The particle issue is particularly perplexing with regard to metal contamination, since the use of high pH SC1-type solutions for particle removal lead to conditions conducive to metal plating as discussed above. Even at today's ppb chemical purity levels, effects of Al and Fe deposition from SC1 solutions are still observed. We are left with the situation of the undesirability of SC1-last surfaces due to metal contamination, but the undesirability of anything else due to particle contamination. It is however becoming more necessary for modern processing to replace SC1-last sequences with others (SC2 if native oxide is acceptable or HF or HF/H_2O_2 if native oxide free surfaces are required).

For metal removal water rinses can play an important role, as discussed above. This might be particularly critical in deep trenches. In addition water normally contains dissolved oxygen which can rapidly oxidize HF-last surfaces. This has led to a recommendation of adding 10-100 ppm HF to a rinse (especially after an HF-last clean) providing a low pH, and sufficient HF, to mitigate the possible effect of the dissolved oxygen. Clearly much work is still needed to develop more effective rinsing and drying approaches for sub 0.35μm device structures.

ACKNOWLEDGMENTS

This work was supported by Stanford's Center for Integrated Systems (CIS) and gift funds from Texas Instruments, Inc. (Sean O'Brien and Mehrdad Moslehi, mentors); the authors would also like to thank Baylor Triplett for his support and making the facilities on Intel's Componennt's Research Laboratory available for some of these studies.

REFERENCES

1. M. L. Kniffin, T. E. Beerling, and C. R. Helms, J. Electrochem. Soc., **139**, 1195 (1992).
2. C. R. Helms, in *Microcontamination '92 Proceedings*, p. 555 (1992).
3. C. R. Helms & H.-S. Park, in *Chemical Surface Preparation*, G. Higashi, Ed., MRS Proc. in press.
4. H.-S. Park, C. R. Helms, D. Ko, M. Tran, B. B. Triplett, in *Chemical Surface Preparation*, G. Higashi, Ed., MRS Proc. in press.
5. See for example: A. Zangwill, *Physics at Surfaces*, Cambridge University Press (1988) and references therein.
6. W. M. Latimer, *The Oxidation States of the Elements and their Potentials in Aqueous Solutions*, Prentice-Hall, New York (1952).
7. M. Pourbaix, *Atlas of Electrochemical Equilibria in Aqueous Solutions*, Pergamon Press, Oxford (1966).
8. D. S. Becker, W. R. Schmidt, C. A. Peterson, and D. C. Burkman, in *Microelectronics Processing: Inorganic Materials Characterization*, L. A. Casper Ed., p. 366, American Chem. Soc. Symposium Series **295** (1986).
9. W. Kern, *J. Electrochem. Soc.* 137: p. 1887 (1990), and references therein.
10. P. Gupta, in *Microcontamination '92 Proceedings*, p. 580 (1992).
11. H. F. Schmidt, M Meuris, P. W. Mertens, S. Verhaverbeke, M. M. Heyns, K. Dillenbeck, Microcontamination, **11**, p. 27 (1993).
12. T. Ohmi, T. Imaoka, I. Sugyiama, and T. Kezuka, J. Electrochem. Soc., **139**, p. 3317 (1992).

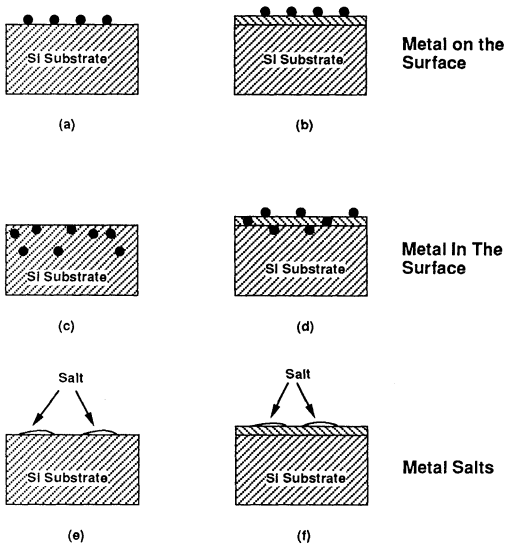


Figure 1. Schematic diagram of the possible locations of metals on a silicon surface. (a) represents metal atoms on a "clean" surface, which would be encountered if metal were deposited in ultrahigh vacuum; (b) represents the same case if a native oxide were present; (c) and (d) represent the case of a metal just below the surface; (e) and (f) represent the case of a metal salt deposited from solution.

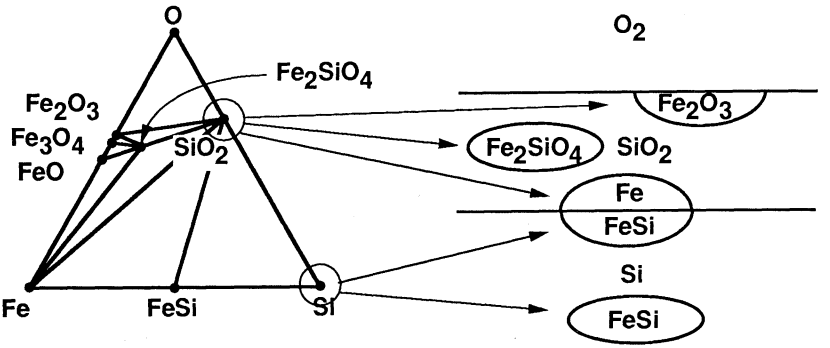


Figure 2. The phase diagram for the Fe/Si/O system is shown (other silicides neglected for clarity). The likely chemical forms of Fe in an MOS structure are shown on the right. The substrate is best represented by the lower right corner of the phase diagram in equilibrium with SiO_2 and FeSi, whereas the oxide in an oxidizing ambient would be in equilibrium with Fe_2O_3 and Fe_2SiO_4.

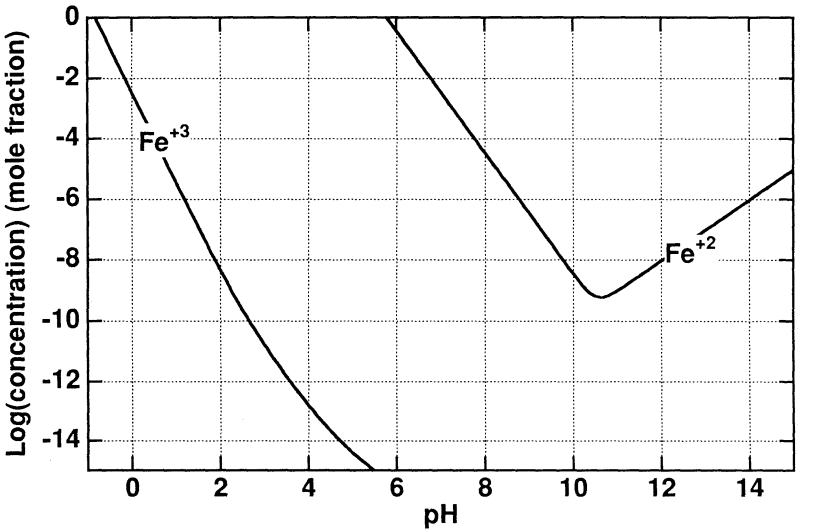


Figure 3. Diagram showing the relative solubilities of the various forms of Fe^{+3} and Fe^{+2} as a function of pH, neglecting any equilibrium between the 2 forms.

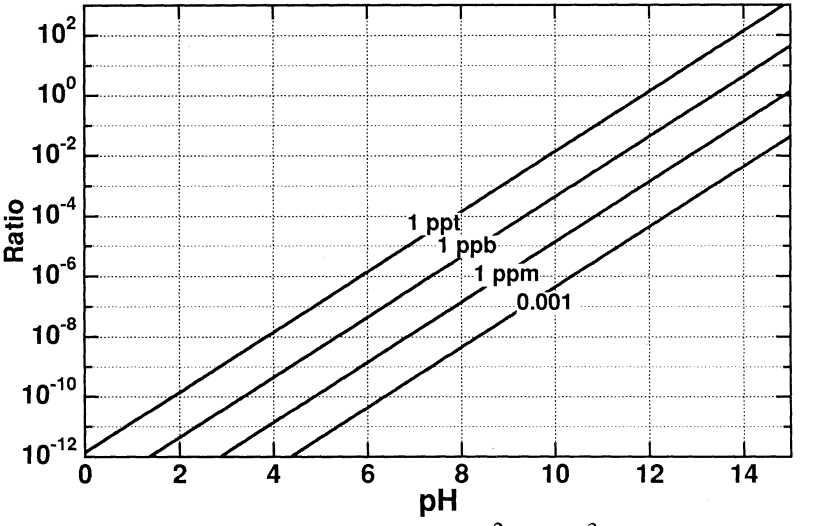


Figure 4. Diagram showing the ratio between total Fe^{+2} and Fe^{+3} as a function of pH for various concentrations of H_2O_2.

APPLICATION OF THERMODYNAMIC ELECTROCHEMICAL POTENTIAL-pH AND ACTIVITY-ACTIVITY DIAGRAMS IN WET CLEANING OF Si: $M:H_2O$, $M:NH_4OH:H_2O$ AND $M:Cl^-:H_2O$ {M= Fe, Cu} systems.

K. Osseo-Asare and Dawei Wei
Department of Materials Science and Engineering,
The Pennsylvania State University, University Park, PA 16802

Kamal Mishra
MEMC Electronic Materials, Inc.,
St. Peters, MO 63132

Thermodynamic stability diagrams for the systems $M-NH_3-H_2O$, $M-Cl^-H_2O$ and $M-H_2O$ { M= Fe, Cu} have been generated using the DIAGRAM computer program. The open circuit potential (OCP) and the current-potential measurements were made using p-type silicon electrodes in the presence of various electrolytes. Electrochemical measurements indicate the presence of an oxide-related passivating film on the silicon electrode in HCl electrolyte under the open circuit condition. On the other hand, in the presence of HF electrolyte, no passivation region was observed even at high potentials. A detailed electrochemical interpretation for the contamination/cleaning of Fe and Cu on/from silicon surface has been presented.

INTRODUCTION

It is believed that future technologies with sub 100A gate oxides will require metallic contamination significantly below 10^{11} atoms/cc(1). As a result numerous studies aimed at lowering the concentration of surface metals by wet cleaning have been reported (2-5). However, rather limited studies have focussed on gaining a detailed understanding of the mechanism of deposition/ removal of metals from silicon wafers using wet cleaning(6-7). The processes involving deposition/ removal of metals across a semiconductor/ aqueous interface as well as etching/ microroughening of the silicon surface are electrochemical in nature. In this study, thermodynamic aspects of Fe and Cu cleaning are studied first in detail using electrochemical potential-pH diagrams and activity-activity diagrams. Electrochemical measurements, such as the open circuit potential(OCP) and current-potential(i-V) relationship, were made to elucidate the mechanism of metallic contamination on silicon surface.

EXPERIMENTAL

A standard three-electrode cell configuration was used for electrochemical measurements. The conventional three-electrode system consisted of a saturated calomel electrode (SCE), a p-type Si working electrode and a Pt counter electrode. The working electrode was made using a p type CZ sample with resistivity of 4 to 6 ohm cm. The

ohmic contact was made by rubbing the electrode with Ga-In eutectic. An EG&G Princeton Applied Research Model 273 electrochemistry system was used for electrochemical measurements. All potentials reported in this study were converted to the SHE scale (SHE = 0.241 + SCE).

The minority carrier diffusion length was measured using the Surface Photovoltage (SPV) method(8). The SPV method utilizes a very low level of excitation. The method of determining Fe using SPV is described elsewhere(9). The following cleaning systems with varying compositions were used:

$NH_4OH:H_2O_2:H_2O$
$HCl:H_2O_2:H_2O$
$HF:H_2O$.

RESULTS AND DISCUSSION

Thermodynamic Data

To construct stability diagrams, the equilibrium constant data for the reactions of interest were culled from the literature(10-12). Representative thermodynamic data used in the construction of these diagrams are shown in Table I. The data analysis and the generation of predominance diagrams were accomplished using the Diagram computer program. The computer program has been discussed elsewhere(13).

Figs. 1(a) and 1(b) present equilibrium Eh-pH diagrams for the $Fe-H_2O$ and $Fe-NH_3-H_2O$ systems, respectively. The activity of dissolved iron-containing species is assumed as 10^{-10}. The ammonia-ammonium activity {N} is 1.0. These values were selected to represent typical compositions of cleaning solutions used in the semiconductor industry. These thermodynamic road maps delineate the stabilities of various solid and dissolved aqueous species. The upper and lower dotted lines in these figures correspond to the oxygen evolution and the hydrogen evolution reactions, respectively. In general, the stability of a phase, and hence cleaning or contamination would depend upon the pH and electrode potential, Eh of a cleaning solution. In the case of SC1 cleaning, with a pH value between 10 and 11, FeOOH enjoys a large stability field. On comparing the Eh-pH diagrams in Figs.(1a) and (1b), it is clear that the presence of ammonia introduces a ferrous ammine stability field in the Fe_3O_4 and FeOOH regions centered around pH 9.3. Thus under certain oxidation conditions, it is possible to dissolve/ clean Fe from a solid silicon wafer surface. However, on increasing the oxidation potential, iron-oxides, FeOOH/ Fe_2O_3 become stable. Thus Fe is predicted to precipitate out from the SC1 cleaning solution onto a solid surface such as silicon wafer (eqs. 2 and 3). Further, the rate of Fe contamination would depend upon the Fe concentration in the chemicals and the rinse time. On lowering the pH to the neutral regime, iron-oxide continues to be the stable product. This indicates that rinsing with de-ionized water following SC1 does not remove any iron oxide from the wafer surface. On further lowering the pH, aqueous species such as Fe^{2+} and Fe^{3+} predominate. Iron cannot deposit as elemental Fe as the oxidation potential at the silicon/ electrolyte interface falls in the stability field of Fe^{2+} and Fe^{3+}. This explains the dissolution of iron-oxide-related contamination from silicon surfaces by cleaning using acid media such as HF, HCl and sulfuric acid.

Figs. 2(a-b) present Eh-pH diagrams for the systems $Cu:H_2O$ and $Cu:NH_3:H_2O$ respectively. Again it is clear from comparing Figs. 2(a) and 2(b) that the presence of ammonia under basic pH introduces a copper-ammine-related stability field. In order to examine the effect of the concentration of ammonia on the predominance diagram, Fig 2c presents a plot of $Log\{NH_3 + NH_4\}$ vs. pH at a fixed $\{Cu^{2+}\}$ activity of 10^{-2} and an Eh of 0.1V. It can be seen that Cu contamination can occur by forming Cu- oxides at higher pH. On the other hand at lower pH, contamination is due solely to the formation of elemental copper. To avoid the deposition of elemental copper at lower pH values, the electrochemical potential of the solution needs to be raised. In practice, this is achieved by the addition of H_2O_2 so that the Eh falls above the Cu/Cu^{2+} boundary line (Figs. 2a and 2b).

Potential Determining Reactions and Contamination

In order to predict the thermodynamic stability of a phase, both pH and Eh need to be defined. The important potential determining reactions in aqueous phase across the silicon/ electrolyte interface can be summarized as follows:

$$2H^+ + 2e = H_2 \quad [24]$$
$$O_2 + 4H^+ + 4e = H_2O \quad [25]$$
$$H_2O_2 + 2H^+ + 2e = 2H_2O \quad [26]$$
$$Si + 2H_2O + 4(+) = SiO_2 + 4H^+ \quad [27]$$

Further, in reaction 27, silicon oxides, other than stoichiometric SiO_2 have been reported to form (14). The open circuit potential, OCP or mixed potential, i.e., the potential at which net current density is zero, is determined by the electron accepting hydrogen evolution reaction 24 and the hole consuming silicon oxide formation reaction 27. This has been schematized in Fig. 3. Oxygen and H_2O_2 reactions raise the OCP to a higher potential, if present in significant amounts. The other reactions which donot affect the OCP due to the negligible concentration of the relevant ions, could result from trace metallic impurities, such as,

$$Cu^{2+} + 2e = Cu \quad [28]$$
$$Fe^{2+} + 2e = Fe \quad [29]$$

Thus, as shown in Fig.3, the efficiency of contamination causing reactions 28 and 29 is controlled by the OCP which in turn is determined by the rate of reactions 24-27. In Table 2, experimentally measured OCP values, in various solutions, are presented. On comparing these values with Figs. 1-2, it can be seen that the OCP values of-0.03V (SC1), 0.25V(SC2) and 0.27 V (HF) fall in the stability regime of FeOOH, Fe^{2+} and Fe^{2+} respectively. In a set of experiments, samples were cleaned with these chemicals and the surface metals were driven in by heat treatment at 1000C for 30 min. in nitrogen ambient. The Fe concentration was determined using the SPV method. These results are shown in Figure 4. As expected from the consideration of the Eh-pH diagram, the Fe contamination resulting from SC1 bath cleaning is 1-2 orders of magnitude higher than that depositing from SC2 or HF bath. The band energy diagram in relation to the standard redox levels and the OCP is presented in Fig. 3b. A value of 0.64 V for the flat band potential, V_{FB} in HF electrolyte has been used(19). The deposition of copper and the removal of Fe from silicon surface can be easily explained on the basis of the

semiconductor-electrochemical model(16). In brief, electroreduction of copper by electrons from the conduction band is energetically favorable. On the other hand, the unfilled levels of the Fe^{2+} /Fe redox couple lies well above the conduction band and is not energetically favorable for the deposition of Fe from HF. Further, p-Si is reverse biased under the open circuit condition($OCP < V_{FB}$). As a result, enhanced copper contamination of p-Si under the band gap illumination is observed (6,16).

Effect of Anions on Copper contamination

In Figs. 5a and b, experimentally determined Log i vs. E relationships are shown for a p-Si electrode in the presence of 1M HCl and 25% HF solution. Figure 5a shows three distinct regions, i.e., hydrogen evolution region, active dissolution region and a passive region. Such behavior is also seen in basic pH electrolytes(14-15). Electrochemical reactions related with etching, microroughening and metal contamination are dependent upon the value of OCP(16). At lower potentials, hydrogen evolution is the predominant reaction. The sharp increase in the current in region 2 is due to the anodic dissolution of Si. The reaction products of dissolution donot inhibit the reaction. On further increase in the potential, a drop in the current is indicative of the surface passivation (reduction in the current was found to increase at lower potential scan rates than that used in Fig.5). However, on comparing Figs. 5a and 5b, the passive region is not observed in the log i-E plots in the presence of HF (Fig. 5b). Thus, in the case of HF, the silicon surface is free of oxides, thus facilitating the copper deposition reaction. In the case of HCl, the value of OCP falls in the passive regime of the Log i-E plot shown in Fig. 5a, indicating the presence of an oxide film. Thus a higher overpotential for the copper deposition than that in the presence of HF is required. Further, in the case of HCl the standard electrode potential for deposition reaction is shifted towards lower potentials. Consider the electrode potentials of the following reactions. The electrode potentials for these reactions have been calculated for the activity of dissolved Cu-related species at 10^{-10} .

$E\ Cu^{+}/Cu = \quad -0.07V$ [30]
$E\ CuCl_2^{-}/Cu = \quad -0.27V$ [31]
$E\ CuCl_4^{3-}/Cu = \quad -0.43V$ [32]

This explains why contamination of Cu from HCl solution is lower than that from HF based cleaning(17).

Effect of H_2O_2

It should be noted that the addition of H_2O_2 raises the OCP, which reduces the copper contamination in acidic medium. In SC1 condition, the addition of H_2O_2 brings the OCP in the passive dissolution regime (-0.36V in the absence of hydrogen peroxide vs. a value of -0.03V in the presence of H_2O_2). Since the dissolution current density is several fold lower in the passive regime than that in the active dissolution regime in the absence of H_2O_2, the roughness decreases significantly(4). However, Fe and Cu contamination is not reduced as the OCP is further pushed in the stability regime of Fe and Cu oxides.

SUMMARY

The application of thermodynamic electrochemical potential-pH diagram in wet cleaning of silicon has been demonstrated. The deposition of Fe and Cu at higher pH is caused by the precipitation of metal oxides. Under acidic pH, the open circuit potential as well as the potential corresponding to the E_c (conduction band edge) lie well above the Fe/ Fe^{2+} boundary, thus keeping the Fe in the electrolyte. On the other hand, the position of E_c and the Cu/Cu^{2+} boundary are energetically favorable for the deposition of elemental copper on oxide-free silicon surface. The i-V behavior of silicon in HCl indicates that the OCP falls well within the passive regime. This passivating film results in a large overpotential for the copper deposition reaction.

REFERENCES

1. W. B. Henley, L. Jastrzebski, and N. F. Haddad in Defect Engineering in Semiconductor Growth, Processing and Device Technology, S. Ashok, J. Chevallier and E. Weber, Editors, MRS Symposium Proceedings, Vol. 262,993(1992).
2. W. Kern and D. A. Puotinen, RCA Rev., 187 (June 1970).
3. W. Kern, J. Electrochem. Soc.,137,1887(1990) and references therein.
4. M. M. Heyns, L. Hellemans, Y. Bruynseraede and A. Philipossian, Jpn. J. Appl. Phys., 31,L1514(1992).
5. M. Itano, F. W. Kern, Jr., M. Miyashita, I. Kawanabe and T. Ohmi, IEEE Trans. Semicond. Manufact., SM-5, 114(1992).
6. T. Ohmi, T.Imaoka, I. Sugiyama, and T. Kezuka, J. Electrochem. Soc.,139,3317(1992).
7. R. W. Rosenberg, M. Itano, I. Kawanabe, F. W. Kern Jr., M. Miyashita, and T. Ohmi, in Microcontamination '90 Conf. Proc., p.273, Santa Clara, CA(1990).
8. J. Lagowski, P. Edelman, M. Dexter and W. Henley, Semicond. Sci. Technol. 7A,185(1992)
9. G. Zoth and W. Bergholz, J. Appl. Phys., 67,6764(1990).
10. G. B. Naumov, B. N. Ryzhenko and I. L. Khodakovsky, Handbook of Thermodynamic Data(Moskow: Atomizdat,1971).
11. C. F. Baes and R.E. Mesmer, The Hydrolysis of Cations (New York: Wiley, 1976), p328.
12. L. G. Sillen and A. E. Martell, Critical Stability Constants of Metal-ion Complexes, Spec. Publ. Chem. Soc. Lond.no 17, 1964; R. M. Smith and A. E. Martell, Critical Stability Constants(New York, Plenum 1977) Vol. 4.
13. K. Osseo-Asare and T. H. Brown, Hydrometall.,4(1979)217.
14. O. J. Glembocki, R. E. Stahlbush and M. Tomkiewicz, J. Electrochem. Soc.132,145(1985).
15. H. Gerischer and W. Mindt, Electrochimica Acta, 13,1329(1965).
16. Kamal Mishra, Dawei Wei and K. Osseo-Asare, unpublished research.
17. P. Gupta, "Silicon Surface Contamination: Identifying and Correlating the Source of Metal Contamination with Process Chemicals", Microcontamination Conf. Proc.,1992.
18. J. W. Faust and E. D. Palik, J. Electrochem. Soc.,130,1413(1983).
19. P. de Mierry, D. Ballutaud, M. Aucouturier and A. Etcheberry, J. Electrochem. Soc.,137,2966(1990).

TABLE 1 Selected equilibrium constants for the Fe-NH_3-H_2O, and the Cu-NH_3-H_2O systems at 25 C.

Reaction	Log K
1. $Fe = Fe^{2+} + 2e$	16.16
2. $Fe_2O_3 + 2e + 6H^+ = 2Fe^{2+} + 3H_2O$	26.93
3. $FeOOH + e + 3H^+ = Fe^{2+} + 2H_2O$	13.37
4. $Fe_3O_4 + 2e + 8H^+ = 3Fe^{2+} + 4H_2O$	36.81
5. $FeO + 2H^+ = Fe^{2+} + H_2O$	14.77
6. $Fe(OH)_3 + e + 3H^+ = Fe^{2+} + 3H_2O$	15.63
7. $Fe(OH)_2 + 2H^+ = Fe^{2+} + 2H_2O$	12.90
8. $Fe(NH_3)^{2+} + H^+ = Fe^{2+} + NH_4^+$	7.84
9. $Fe(NH_3)_2^{2+} + 2H^+ = Fe^{2+} + 2NH_4^+$	16.28
10. $Fe(NH_3)_4^{2+} + 4H^+ = Fe^{2+} + 4NH_4^+$	33.26
11. $NH_4+ = H^+ + NH_3$	-9.24
12. $Fe(OH)_3^- + 3H^+ = Fe^{2+} + 3H_2O$	31
13. $Fe(OH)_4^{2-} + 4H^+ = Fe^{2+} + 4H_2O$	46
14. $CuO + 2H+ = Cu^{2+} + H_2O$	7.34
15. $Cu = Cu^{2+} + 2e$	-11.48
16. $Cu_2O_+ 2H^+ = 2Cu^{2+} + H_2O + 3e$	-7
17. $Cu(NH_3)^+ + H^+ = Cu^{2+} + NH_4^+ + e$	0.75
18. $Cu(NH_3)_2^+ + 2H^+ = Cu^{2+} + 2NH_4^+ + e$	5.22
19. $Cu(NH_3)^{++} + H^+ = Cu^{2+} + NH_4^+$	5.06
20. $Cu(NH_3)_2^{++} + 2H^+ = Cu^{2+} + 2NH_4^+$	10.76
21. $Cu(NH_3)_3^{++} + 3H^+ = Cu^{2+} + 3NH_4^+$	17.06
22. $Cu(NH_3)_4^{++} + 4H^+ = Cu^{2+} + 4NH_4^+$	24.12
23. $Cu(NH_3)_5^{++} + 5H^+ = Cu^{2+} + 5NH_4^+$	33.87

TABLE 2 Open circuit potential (OCP) values for p-type silicon electrodes.

Resistivity	Electrolyte	OCP, SHE, Volts	References
4-6 Ohmcm	1M HCl	0.17	This work
4-6 Ohmcm	1M HCl + H_2O_2	0.25	This work
4-6 Ohmcm	1M NH_4OH	-0.36	This work
4-6 Ohmcm	1M NH_4OH+ H_2O_2	-0.03	This work
1.3 Ohmcm	1M KOH	-1.07	18
4.2 Ohmcm	1M KOH	-1.25	18
0.5 Ohmcm	5% HF	-0.11	19
4-6 Ohmcm	25%HF+0.1MKCl	0.28	This work

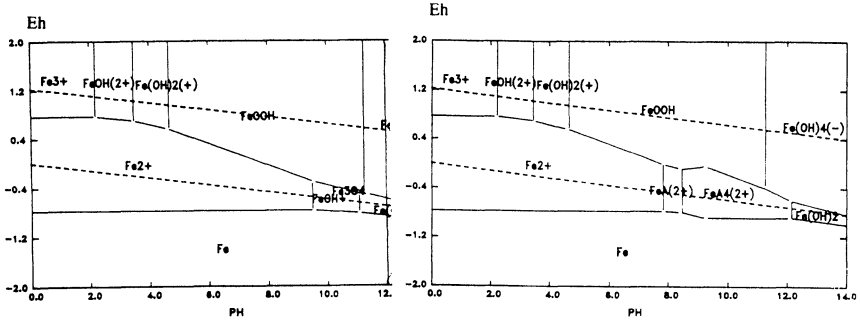


Fig. 1 Equilbrium Eh-pH diagrams for the system (a) Fe-H_2O and (b) Fe-NH_3-H_2O $\{Fe\} = 10^{-10}$, $\{NH_3 + NH_4^+\} = 1$. $A = NH_3$

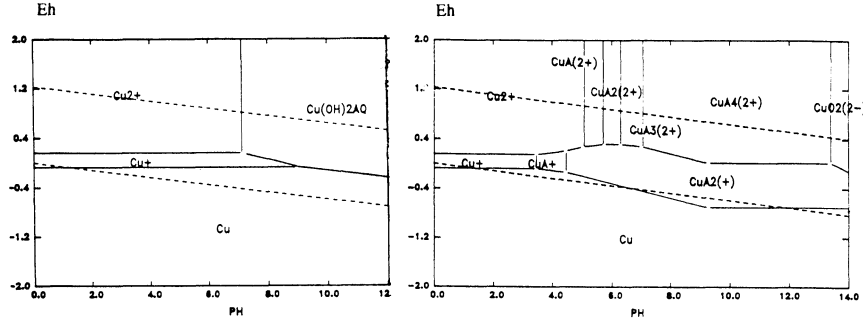
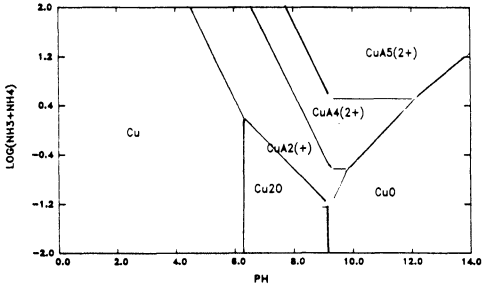


Fig. 2 Equilibrium Eh-pH diagrams for the system (a) Cu-H_2O and (b) Cu-NH_3-H_2O $\{Cu\} = 10^{-10}$, $\{NH_3 + NH_4^+\} = 1$;
Fig2(c) Activity-Activity, Log $\{NH_3 + NH_4^+\}$ vs. pH, plot for $\{Cu\} = 10^{-2}$, Eh = O.1V



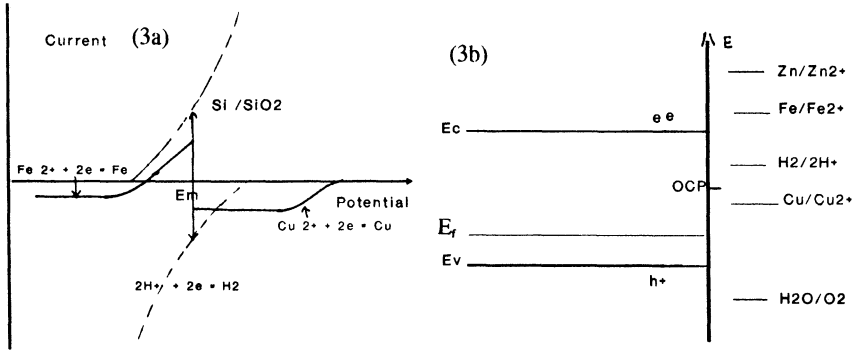


Fig.3a. Schematic mixed potential model for the metallic contamination of silicon.
Fig.3b. Band energy diagram of p-Si in HF in relation to the redox levels and the OCP.

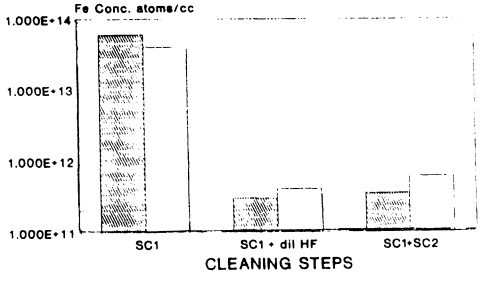


Fig. 4 The effect of various cleaning steps on the bulk contamination in p-type silicon following 1000C, 30 min. drive-in treatment in the nitrogen ambient.

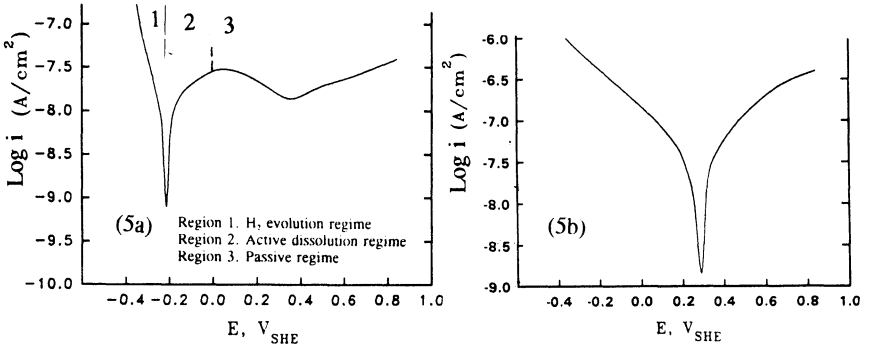


Fig. 5 Log i- E relationship for p-Si in (a)1M HCl and (b) 25% HF

AN ELECTROCHEMICAL PERSPECTIVE OF SILICON CONTAMINATION DURING PROCESSING

Yaw S. Obeng
AT&T Bell Laboratories
555 Union Boulevard
Allentown, PA 18103

Copper contamination of silicon wafers during etching in HF, and the consequent pitting of the substrates are described. The observations are discussed in terms of oxidation-reduction processes at the silicon-solution interface. A guide for identifying potential metallic contaminants, and contamination extents are proposed. Strategies for preventing metallic contamination are also discussed.

INTRODUCTION

Transition metal contamination continues to plague the IC industry; electrodeless plating of noble metals is considered a nuisance in substrate cleaning by wet chemical etching. The metal contaminants in wet chemical cleaning can be traced to a number of sources such as equipment (metal components of wafer handlers), process materials (Si materials), cleaning chemicals, as well as cross contamination from metal deposition processes. Transition metals tend to diffuse rather quickly via interstitial lattice sites and form deep level traps which can readily affect the electrical and optical properties of Si. Metal contaminants are known to passivate dopants, create generation-recombination centers in Si, increase reverse-bias junction leakage currents, affect the dielectric properties of oxides, decorate dislocations and induce stacking fault formation. Furthermore, transition metal contamination can degrade devices to an extent well beyond what would be expected from the contamination levels. For example, an initially deposited submonolayer of Cu can induce other metals that will not normally deposit, such as Mo and Pb, to deposit from solution through the phenomenon of underpotential deposition (UDP) of metals.

Kern et al. have identified three basic mechanisms by which metals contaminate wafers: physisorption, precipitation of insoluble metal complexes, and deposition of free metal species (1). The latter mechanism is difficult to control even in the purest commercially available solutions. It is also well known that 1 ppb levels of Cu in HF can plate out to yield 10^{11} - 10^{12} atom/cm^2 concentrations on Si surfaces (2).

EXPERIMENTS AND RESULTS

Silicon wafers etched in contaminated 49% HF emerge from the processing bath with a hazy dull appearance. Optical and scanning electron microscopies suggested the haze was formed by deposits on the Si wafer during chemical etching of dielectric films in the HF bath. Surface SIMS analysis of the hazed areas showed traces of fluorine (F), presumably from adsorbed HF or some fluoride salts, and large amounts of copper (Cu) contaminants. Auger microprobe analysis of the haze particles showed that the Cu contamination was confined to these plate-like particles. ICP-MS analysis suggest that the Cu deposits originated from the HF bath.

Figure 1 shows the SEM of the top surface of a Cu contaminated wafer that has been stored in an analytical laboratory ambient for about 4 months. The wafer surface developed pits at the sites that originally had Cu containing deposits, and surface area of the pits match the foot prints of the original deposits. Atomic force microscopy (AFM, Figure 2) shows the pits to be ~ 900Å deep. Auger analyses within the pits showed Cu and traces of chlorine (Cl) as the only contaminants, while the areas adjacent to the pits show only carbon (C) and oxygen (O) contaminants. These observations suggest that the pitting may be a consequence of Si and F loss, possibly as volatile SiF_4. The pit sizes and their distribution suggest that the pitting process is limited by the amount of F available locally in the initial Cu-rich deposits.

DISCUSSION

The bare Si surface is a fairly strong reductant (Efb = -0.7V/NHE), with a small band gap (1.1ev). Thus,

for metallic ions with redox potentials negative of E_{fb} both oxidation and reduction will occur through the conduction band of the Si, irrespective of dopant type and level, although ion reduction rate on p-type Si is expected to be slower than on n-type. This suggests that p-type Si should be less susceptible to noble metal contamination; Cachet et al. have demonstrated that in the presence of a p/n junction, Pt and Pd deposit selectively on n-type areas (3).

The observed pitting is the net result of Cu catalyzed formation of volatile SiF_4 from reaction of the Si substrate, atmospheric humidity, and fluorine sources such as adsorbed HF. The proposed chemical processes are summarized in equations [1] and [2].

$$Si(s) + 2H_2O \longrightarrow SiO_2(s) + 2H_2 \qquad [1]$$

$$SiO_2(s) + 4HF \longrightarrow SiF_4(g) + 2H_2O \qquad [2]$$

Thermodynamics of Metal Contamination Process

The reduction of metal ions at the clean Si/electrolyte interface is accompanied by the oxidation of Si by hole injection. The surface contamination process can be summarized as

$$M^{n+}(aq) + ne \longrightarrow M(s) \quad E = E_M \text{ (reduction)} \qquad [5]$$

$$Si(s) + 2H_2O(l) \longrightarrow SiO_2(s) + 2H_2(g) \quad E_o = 0.84V/NHE \qquad [6]$$

The formal potential of the reduction step, E_M, is related to the solution concentration of the metallic ion, M^{n+}, of interest by the Nernst equation (equation [7])

$$E_M = Eo(M) + (RT/nF) \ln([M^{n+}]/[M]) \qquad [7]$$

where Eo(M) is the standard reduction potential of the M/M^{n+} couple, R the gas constant, F Faraday's constant, and $[M^{n+}]$ the molar concentration of M^{n+} (moles/cm^3).

Since the reduced metal goes out of solution as free metal, its activity ([M]) is effectively unity, and equation [8] reduces to

$$E_M = Eo + (RT/nF)\ln[M^{n+}] \qquad [8]$$

The driving force for the contamination process , E_C, is

$$Ec = E_M - 0.84\ V/NHE \qquad [9]$$

The metal ion reduction at the interface is feasible as long as Ec is a positive quantity. This restricts the reduction potential of possible metal contaminants to species with $E_M > +0.84$ V/NHE. E_C determines only the feasibility, but not the rate, of the reduction of M^{n+} on bare Si (in HF). In VLSI grade HF, the concentration of most divalent metal ions, e.g., Cu^{2+}, Zn^{2+}, and Pb^{2+}, is around 0.10ppb. At these concentrations positive E_C restricts potential direct contaminants to species of $E_O \geq$ 0.3 V/NHE, i.e., only metals below Co^{2+} or Cu^{2+} in the electromotive series.

Contamination Kinetics

The wafer surface concentration of electrodeposited metal after HF cleaning should be proportional to the reduction and deposition rates. For a M^{n+}/M couple, $E_{O(M)}$ does not change, but E_M floats as a function of [M] and $[M^{n+}]$. Define, ΔE as

$$\Delta E = (RT/nF)\ [\ln\ (\Delta([M^{n+}]/[M]))] \qquad [10]$$

where $(\Delta([M^{n+}]/[M])$ is the change in the ratio of reduced to oxidized metal ion concentrations. The rate of metal/contaminant deposition is described by

$$\Delta E/\Delta t = (RT/nF) \ln (\Delta[M^{n+}])/\Delta t \quad [11]$$

The slope of the metal deposition rate curve, (RT/nF), depends on the charge on the metallic species. Equation [11] also suggests that the electrodeposition will cease at the point when $\Delta E/\Delta t$ effectively approaches zero.

The total amount of metal deposited on the wafer surface is determined by the total charge passed (Q), equation [12]

$$Q = (RT/nF) \ln (\Delta[M^{n+}]).t \quad [12]$$

$$\rho = Q(1 + 1/A) = (RT/nFA)t.\ln[M^{n+}] \quad [13]$$

Under diffusion controlled conditions the density, (ρ), of free metal depends on the solution concentration of the reducible metal ions, their charges, and the duration of contact of the clean Si wafer with the contaminated solution, equation [13]. The form of equation [13] agrees with the empirical relationships derived for heavy metal contamination of Si wafers from deliberately contaminated HF solutions (2).

Strategies for Preventing Metallic Contamination

It has been demonstrated that the addition of H_2O_2 to HF cleaning solutions prevents the formation of metal deposits on the cleaned Si surface. The added peroxide presumably oxidizes the H-capped Si to SiO_2 by the reaction:

$$Si + 2H_2O_2 \longrightarrow SiO_2 + O_2 + 2H_2 \quad E_{rxn} \sim 2.1V/NHE \quad [14]$$

The E_{fb} of SiO_2 is such that there is no direct deposition of metals on the surface as the oxide film can not be further oxidized. The addition of the peroxide to the HF solution introduces a new dimension to the metal

contamination problem, as the passivating oxide is very susceptible to a wider range of metallic contamination. Many of the metal ions present in HF solution oxidize rather readily and are incorporated into the growing SiO_2 film. Thus, care must be taken to effectively strip off the *in-situ* grown oxide before further processing.

Another strategy to preventing metallic contamination during HF etching is the addition of surfactants to the HF cleaning solutions. For example, the addition of anionic perfluorocarbon surfactants to 5% HF etching solutions have been demonstrated to reduce Si surface Cu concentration by four fold, relative to neat 5% HF. The addition of surfactants has two potential benefits: (a) surfactant films adsorb on and passivate substrate surfaces, and (b the micelles immobilize the metal ions(4). The micelle immobilized ions tend to be more stable than the hydrated precursors, towards reduction as the efficiency of the electron transfer kinetics is decreased. Furthermore, the micelle-ion complexation drastically decreases the free metal concentration, thus pushing the formal potential of potential metallic contaminants to below the threshold of -0.3 V/NHE.

SUMMARY

The pitting of Cu contaminated Si wafers is attributed to Cu catalyzed Si loss as volatile SiF_4 from the Si substrate. In HF media, only metals with reduction potentials more positive than 0.3/NHE will deposit on Si wafers. The rate of deposition, and the wafer surface density of such metals, depend on the solution concentration of the reducible species. Hydrogen peroxide added to HF etching solutions oxidizes the cleaned Si surface, thus passivating it with an oxide film. The film prevents the Si from coming into direct contact with the reducible metal ions. The addition of surfactants prevents metallic contamination by drastically decreasing the free metal ion concentration.

ACKNOWLEDGEMENTS

We are grateful to Drs. Barry Miller, S. Nakahara, Karrie Hanson, Joyce Sapjeta , Ken Benson, Greg Higashi,

Juli Eisenberg; David Angst, Fred Stevie, Bill Knolle, Messieurs Kurt Steiner, David Brady, Bob Lebaron, Jim Cargo, Mark Sundahl, and Ms Judy Moore for helpful discussions and technical assistance. We are especially grateful to Dr. Susan Maher (Park Scientific Instruments, Mount Laurel, NJ) for technical assistance with the AFM

REFERENCES

1) F. W. Kern, M. Itano, I. Kawanabe, M. Miyashita, R. W. Rosenberg, and T. Ohmi, in *'Metallic Contamination of Semiconductor Devices from Processing Chemicals, the Unrecoginized Potential'*, presented at the 37th Annual IES Meeting, San Diego, CA, May 6-10, (1991), (b) Antilla, O. J. ; Tilli, M. V.; Scaekers, M.; Claeys, C. L. J. Electrochem. Soc., 139(4), 1180, (1992)

2) E. Hsu,*'Deposition Characteristics of Metal Contaminants from HF based solutions onto Wafer Surfaces'*, M. S. Thesis, University of Arizona, February (1992).

3) H. Cachet, M. Froment, E. Souteyrand, C. Dening, *J. Electrochem. Soc.*, 139, 2920 (1992)

4) J. Ouyang, and A. J. Bard, Bull. Chem. Soc. Jpn., 61, 17, (1988) (b) G. L. Macintire, Am. Lab., 173, (1986), (c) G. L. Macintire, D. M. Chippardi, R. L. Casselerry, and H. N. Blount, J. Phys. Chem., 86, 2632, (1982)

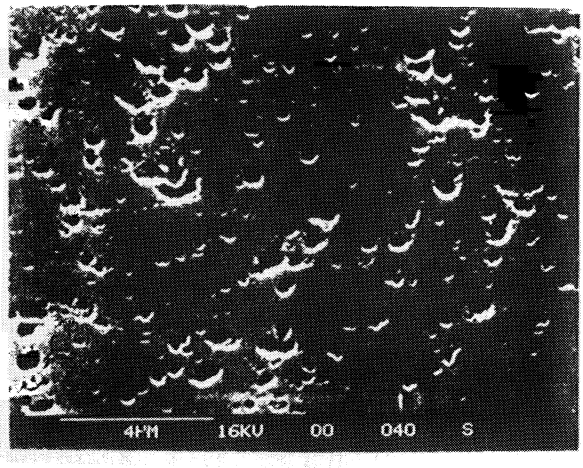


Figure 1: SEM of Pitted Si Surface of a Cu Contaminated Si wafer after 4 months in an analytical laboratory ambient.

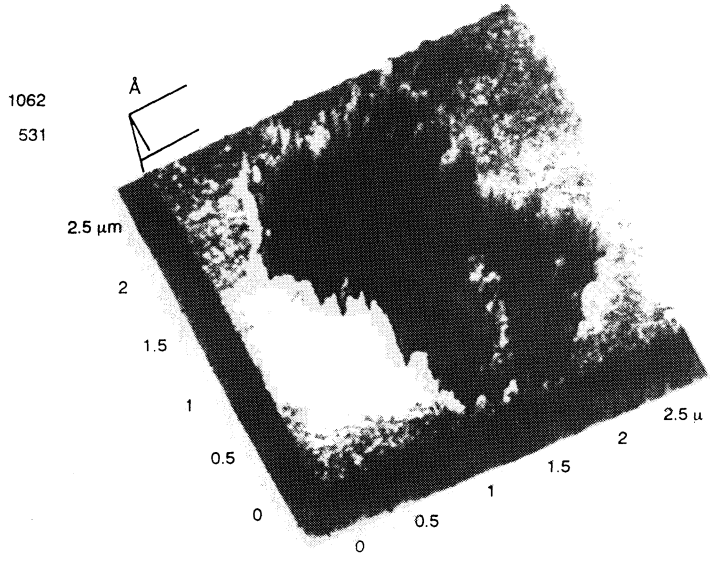


Figure 2: Atomic Force Micrograph of a 900Å deep pit on Si Surface of a Cu Contaminated Si wafer after 4 months in an analytical laboratory ambient.

EFFECTS OF SURFACE IRON ON RECOMBINATION LIFETIME AND ITS REMOVAL FROM SILICON SURFACES

Heungsoo Park and C. R. Helms
Solid-State Electronics Laboratory
Stanford University, Stanford CA 94305

M. Tran and B. B. Triplett
Intel Corporation, Santa Clara CA 95052-8125

Vacuum-evaporated iron caused a severe degradation in the lifetimes irrespective of the cleans used indicating lifetime degradation is related to initial iron concentration, not merely to final iron concentration after cleaning. We also found that it took at least three separate steps (within the RCA-based cleans) to effectively remove iron from hydrofluoric acid solution (HF)-last surfaces.

INTRODUCTION

The current metal-oxide-silicon (MOS) processing, the concentration of "process-induced" metallic impurities on the silicon surfaces is often higher than 10^{12} atoms/cm^2.(1) Iron in particular has been one of the impurities of greatest concern in wafer degradation, leading to reduction of the minority-carrier recombination lifetime as well as poor gate oxide reliability. Therefore, it is important to understand the behavior of iron in silicon and silicon oxides, and develop effective methods for the removal and control of metals from the silicon surface.

In this paper, we report effects of surface iron contamination on the photoconductivity recombination lifetime of p-type silicon and its removal from silicon surfaces.

EXPERIMENTAL

For this study, 4"(100) p-type Czochralski (CZ)-grown wafers were used in most cases. We prepared iron-contaminated wafers by vacuum-evaporating sub-monolayer concentrations of iron atoms on wafers precleaned with either an ammonium hydroxide-hydrogen peroxide solution (SC1)-last step or an HF-last step at a very low rate ($< 10^{13}$ atoms-cm^{-2}-sec^{-1}) for about 2-3 sec to give a

contamination level of less than about $3x10^{13}$ atoms-cm^{-2}. The relative efficiency of various chemical cleans was determined, using Auger electron spectroscopy (AES) as well as total reflection X-ray fluorescence (TXRF).(2, 3)

The photoconductivity recombination lifetimes of the wafers were measured with a Semitex LIFETECH-88. For the lifetime measurement, both the uncontaminated and the contaminated wafers were cleaned with standard RCA cleans followed by HF solutions and were then oxidized at 920°C to an oxide thickness of 110 Å. In order to study its temperature dependence, the photoconductivity recombination lifetime of the wafers were measured from room temperature up to 250°C.

To see surface microroughness of iron-contaminated wafers and uncontaminated wafers, we assessed some of the wafers cleaned with standard RCA cleans followed by HF solutions by means of Tapping Mode™ atomic force microscopy (TMAFM). The measurements were done on an area of 1 μm x 1μm with 512 x 512 data points for the samples.

RESULTS AND DISCUSSION

Chemical cleaning efficiency of the removal of iron from silicon surfaces

Table I shows the efficiency of RCA-based cleans for the removal of iron on silicon surfaces. The cleaning efficiency here is defined as follows:

$$\text{Chemical Cleaning Efficiency} = \frac{100}{\text{the \% Fe remaining after the cleans}} - 1$$

As shown in the table, we found that it took at least three separate steps to effectively remove iron from HF-last surfaces. We also found that the SC1 was more effective in removing iron from HF-last surfaces than the hydrochloric acid-hydrogen peroxide solution (SC2). Note the sequence of HF + SC1 + HF is interesting because, even without an SC2 step, it effectively removed iron from silicon surfaces.

When wafers are contaminated, several possible situations can result and we can group them into two categories in terms of surface conditions: one with native silicon oxides, and the other without native oxides (HF-last surface). In the former case (SC1-last surface), we could remove iron from native oxide surfaces even with single-step cleans.(2, 3) The iron on HF-last surfaces was much more difficult to remove. To understand this behavior, we must consider the bonding between metals and silicon itself when we aim to dissolve metals in chemical solutions.

Most elemental metals tend to dissolve in acidic solutions containing moderate oxidants and/or suitable complexing agents.(4) According to the potential-pH equilibrium diagram of the iron-H_2O system (4), iron is not stable with H_2O. It dissolves in acid solutions but becomes gradually passive as the pH of the solution increases. The presence of oxidizing agents in the solution also can help the dissolution of iron in the solution when the pH of the solution is below about 8.

Table I
Efficiency of RCA-based cleans on the removal of iron either from SC1-last surfaces or from HF-last surfaces.

Chemical Cleaning	Cleaning Efficiency (Fe on HF-last surface)
HF only	6
SC1 only	2
SC2 only	0
SC1 + SC2	4
SC1 + HF	99
SC2 + HF	9
HF + SC1	49
HF + SC2	11
SC1 + SC2 + HF	24
SC1 + HF + SC2	> 99
HF + SC1 + HF	> 99
HF + SC1 + SC2	> 99

Therefore, we can expect that either an SC2 solution or an HF solution will be more effective to dissolve iron from silicon surfaces than an SC1 solution. When compared with the previous experimental results (2, 3), this is the case when iron is deposited on the SC1-last surfaces, but it is not the case when iron is on HF-last surfaces. Our model is that iron on HF-last surfaces exhibits silicide-like bonding to Si; therefore, it is possible that the etching of silicon is necessary for iron removal from HF-last surfaces. HF and HF-oxidizing-HF sequences are therefore effective for the removal of iron in this case due to the attack of silicon by the HF solutions.

Effect of chemical cleaning of surface iron on photoconductivity recombination lifetime

Table II shows the photoconductivity recombination lifetime of the uncontaminated p-type silicon wafers and the iron-contaminated wafers, with different chemical cleans prior to the oxidation step. As shown in the table, the chemical cleans before oxidation can strongly affect the lifetime of the wafers: a very low lifetime for the silicon wafer with SC1-last surfaces before oxidation and a high lifetime for the silicon wafer with HF-last surfaces before oxidation. However, for all of the cleans performed after iron deposition, the lifetimes were lower suggesting that the cleans still left iron that could dissolve into the silicon during oxidation.

Table II
Photoconductivity recombination lifetime on TCA-oxidized wafers having different chemical cleans prior to oxidation for the uncontaminated wafers, and for the iron-contaminated wafers.

Processes	Lifetime [μsec]	
	Uncontaminated	Contaminated*
HF + SC1	1	--------
HF + SC1 + SC2	180 - 250	4 - 6
SC1 + SC2 + HF	--------	5 - 10
HF + SC1 + SC2 + HF	400 - 500	5 - 10
SC1 + HF + SC2 + HF	--------	20 - 30

* The initial iron contamination level was about 3×10^{13} atoms/cm^2.

The use of the SC1 solution has been controversial due to the possible recontamination of metallic impurities like aluminum and iron from the solution to the silicon surfaces during cleaning. Since aluminum does not greatly affect the recombination lifetime (5), we consider iron the more likely cause for the low lifetime of the silicon wafers cleaned in the SC1 solution.(see Table II) Compared to the SC1 solution, the SC2 solution is believed to produce clean silicon surfaces passivated by chemical oxides, relatively free of metallic contamination. In fact, Atsumi et al. suggested that recontamination of the silicon surfaces by iron in the solution did not occur because iron became soluble (or rather stable) ion at the low pH of the solution.(5) Indeed, iron tends to be absorbed more by the silicon surfaces as the pH of the solution goes up.(6) Therefore, it is not surprising that

the silicon wafers with a final SC2 solution clean show a much higher lifetime than the silicon wafers with a final SC1 solution clean. The HF solution can produce very clean and flat silicon surfaces when compared with those produced by the other two solutions.(7) On the other hand, a silicon surface cleaned in the HF solution attracts particles and organic contaminants from the solution, deionized (DI) water, and ambient air.(8) It is not clear at this point how the vulnerability of the HF-cleaned silicon surfaces to particle and/or organic contamination before oxidation affects the recombination lifetime afterwards. However, it is the wafers cleaned in the HF solution that have the lowest iron contamination surfaces and that thus show the highest lifetime among the wafers cleaned in the three solutions.

Effect of Initial Fe Coverage on Photoconductivity Recombination Lifetime of Si

The lifetime is also dependent upon the concentration of surface iron: the higher the surface concentration, the lower the lifetime. However, it is surprising to see that the lifetime is also dependent on the initial concentration of surface iron before cleaning. Figure 1 shows the effect of the initial iron coverage on the lifetime of the wafers with different chemical cleans before oxidation. Likewise in Table II, the wafers with a HF-last surface before oxidation showed a higher lifetime than the wafers with a SC2-last surface before oxidation.

As shown in the figure, the initial iron concentration has an effect on the lifetime: the larger the lifetime as the lower the initial iron concentration. The TXRF measurements on the iron-contaminated-but cleaned silicon surfaces showed that the surface iron concentration of the contaminated wafers was the same as that of the uncontaminated wafers. Since the TXRF measurements can not tell iron atoms from iron complexes on the surfaces, the concentration of "effective" iron on the uncontaminated wafers may, in fact, be lower than that of the contaminated wafers. Besides, iron was deposited on the HF-last surfaces in this study, which means some of surface iron atoms can survive during cleaning and later diffuse into the bulk during oxidation. Therefore, we suspect that the concentration of the "effective" iron atoms on the surfaces after cleaning is proportional to the initial concentration of iron deposited to a certain extent and thus that the lifetime is dependent upon the initial concentration of surface iron.

However, we can not exclude the possibility that the dependency of the lifetime on initial surface iron coverage might be related to the surface microroughness of the wafers. As mentioned earlier, iron on HF-last surfaces is believed to have silicide-like bonding with surrounding silicon atoms, and those silicon atoms could be taken off with iron during cleans. If it is the case, then the surfaces of the iron-contaminated wafers becomes much rougher locally than those of the uncontaminated wafers after cleans: the more iron on the surfaces, the more roughened spots on the surfaces. We, then, can expect that the surface recombination velocity will be higher for the contaminated wafers than for the uncontaminated, resulting in lower lifetimes for the contaminated wafers than for the uncontaminated wafers. Table III shows the root-mean-square (rms) roughness

of an iron-contaminated wafer and a uncontaminated wafer, measured by AFM. They were cleaned through standard RCA cleans with HF solutions. For the contaminated wafer, only its center region was contaminated with iron. As shown in the table, the center of the contaminated wafer shows a slightly higher rms roughness than other areas of the same wafer and the center of the uncontaminated wafer, which does not seem to suggest that there was a large difference in surface microroughness between the contaminated wafer and the uncontaminated wafer after cleans. Since the table only shows the average values, it is not clear at this moment whether there were much roughened local regions on the contaminated wafer related with iron—if any, they should be the ones that deteriorates the lifetime severely.

Table III
Root-mean-square (rms) roughness of an iron-contaminated wafer and a uncontaminated wafer, measured by atomic force microscopy (AFM), after cleans

Samples	RMS Roughness [nm]
Center of the iron-contaminated wafer	.104
Edge of the iron-contaminated wafer	.095
Center of the uncontaminated wafer	.082

* The initial iron contamination level was about 1 x 10^{14} atoms/cm^2.

Figure 2 shows the lifetime of an iron-contaminated-but-cleaned wafer as a function of temperature for both ramp-up and ramp-down of the sample. As shown in the figure, the lifetime exhibits the same trend for both cases. Since we were measuring the lifetime of the top layer of about 10 μm from the silicon surfaces due to the limitation from the penetration depth of the laser, we believe that the Fe_i's freed from the iron-born pairs at elevated temperatures did not diffuse far away, and thus that the reverse reaction to the formation of the iron-boron pairs became available as temperature went down. In fact, the diffusion coefficient of iron in silicon is not high at temperatures up to 250°C.(9)

CONCLUSION

Experiments on photoconductivity recombination lifetime of the wafers showed a very low lifetime for silicon wafers with SC1-last surfaces, a relatively high lifetime for silicon wafers with SC2-last surfaces, and a high lifetime for silicon wafers with HF-last surfaces. In addition, vacuum-evaporated iron caused a severe degradation in the lifetimes irrespective of the cleans used indicating lifetime

degradation is related to initial iron concentration, not merely to final iron concentration after cleaning.

ACKNOWLEDGMENTS

The authors would like to thank Dr. K. Gupta for total reflection X-ray fluorescence measurements. They also would like to thank Dr. Y. Strausser and Mr. Richard Lee for atomic force microscopy measurements. This work was supported by Stanford Center for Integrated System (CIS) and Gift Funds from Texas Instruments.

REFERENCES

(1) N. Anzai, Y. Kureishi, S. Shimizu, and T. Nitta, in 1st Workshop on ULSI Ultra Clean Technology, p. 75 (1989).
(2) M. L. Kniffen, T. E. Beering, and C. R. Helms, J. Electrochem. Soc., 139, 1195 (1992); conditions for cleaning solutions used here are specified in this paper.
(3) H. Park, C. R. Helms, D. Ko, M. Tran, and B. B. Triplett, Materials Research Society Conference, San Francisco, 1993.
(4) M. Pourbaix, Atlas of electrochemical equilibria in aqueous solutions, p. 307, Pergamon Presss, Oxford (1966).
(5) J. Atsumi, S. Ohtsuka, S. Munehira, and K. Kajiyama, in Semiconductor Cleaning Technology/1989, J. Ruzyllo and R. E. White, Editors, PV 90-9, p. 59, The Electrochemcal Society Softbound Proceedings Series, Pennington, NJ(1990).
(6) H. Hiratsuka, M. Tanaka, T. Tada, R. Yoshimura, and Y. Matsushita, in 11th Workshop on ULSI Ultra Clean Technology, p. 5 (1991).
(7) Y. J. Chabal, G. S. Higashi, K. Raghavachari, and V. A. Burrows, J. Vac. Sci. Tech., A 7, 2104 (1989).
(8) W. Kern, J. Electrochem. Soc., 137, 1887 (1990).
(9) K. Graff, in Aggregation Phenomena of Point Defects in Silicon, E. Sirtl and J. Goorissen, Editors, PV 83-4, p. 121, The Electrochemcal Society Softbound Proceedings Series, Pennington, NJ(1990)..

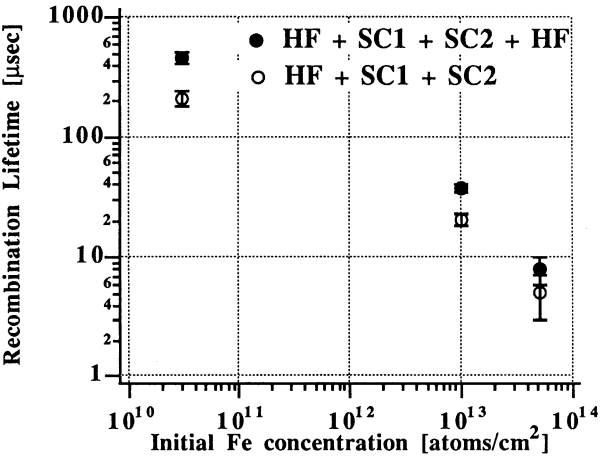


Figure 1. The plot of photoconductivity recombination lifetime of Si versus initial surface Fe coverage

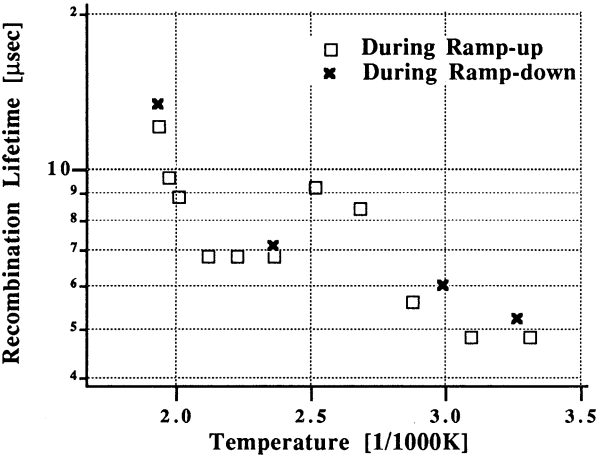


Figure 2. The photoconductivity recombination lifetime of an iron-contaminated-but-cleaned wafer as a function of temperature for both ramp-up and ramp-down.

THE RELATION BETWEEN SODIUM AND ALUMINUM CONTAMINATION AND DIELECTRIC BREAKDOWN IN MOS STRUCTURES

B. Vermeire, A. L. P. Rotondaro, P. W. Mertens, S. Verhaverbeke and M. M. Heyns
IMEC
Kapeldreef 75, B-3001 Leuven, Belgium

ABSTRACT

The effect of sodium and aluminum contamination on the dielectric behaviour of gate oxides is investigated for concentrations in the order of 10^{11} atoms/cm^2. No degradation of the breakdown field distribution has been observed for sodium and aluminum contaminated wafers. However, the presence of a tail in the charge-to-breakdown analysis of both the Na and Al contaminated samples indicates that both elements can be very detrimental to the reliability characteristics of thin gate oxides.

INTRODUCTION

The effect of metal contamination on the characteristics of thin gate oxides is a field of study that has received an increasing amount of attention in the last years (1-3). In this study, sodium and aluminum were selected to be investigated as both are supposed to get incorporated into the oxide layer (3). It has been demonstrated (4,5) that Na can cause a reduction in the breakdown field as a result of barrier height lowering. However, relatively high levels of sodium contamination were used in these cases. Moreover, it has been reported that aluminum contamination introduced prior to oxidation does not affect the recombination lifetime of silicon substrates (6). Unfortunately, the effect of the aluminum contamination on the characteristics of thin oxides was not investigated in detail. In this paper the effect of sodium or aluminum contamination on the dielectric behaviour of thin gate oxides is presented for contamination levels in the range of 10^{11} atoms/cm^2.

EXPERIMENTAL

Sodium or aluminum was introduced at a typical level of 10^{11} atoms/cm^2 by spinning on the wafers a NaCl or Al spiked HNO_3 solution (6). Reference wafers without intentionally introduced contamination were oxidised separately in order to avoid cross-contamination. For all wafers the typical background contamination level for elements with atomic number from 16 (Sulphur) to 36 (Krypton) and from 47 (Silver) to 83 (Bismuth) was determined using a combination of Vapour Phase Decomposition (VPD), Droplet Surface Etching (DSE) and Total reflection X-Ray Fluorescence (TXRF). In all cases the background contamination level is below 10^{10} atoms/cm^2.

The effect of Na contamination on the oxide characteristics was investigated for a contamination level of 10^{11} atoms/cm^2 which is introduced at two stages of the MOS capacitor fabrication process: just prior to oxidation and after the gate oxidation is performed *i.e.* just prior to the poly-Si electrode deposition. In this way the effect of the gate oxidation process on the Na contamination can also be investigated. The Al contamination was only introduced prior to the oxidation but at two levels: 10^{11} and 10^{12} atoms/cm^2. Both n-type Cz and p on p+ type epitaxial Si-wafers were used. Gate oxides of 15 or 60 nm were grown in dry O_2 (no Cl added) after ramp-up in argon ambient to an oxidation temperature of 900 °C in a double wall furnace. Standard n+ poly-Si gate capacitors were fabricated for electrical evaluation.

The Na or Al levels on the various wafers after processing were determined using SIMS measurements. Breakdown histograms are constructed using a ramp-voltage breakdown test until destructive breakdown occurs. The capacitors were measured with the top plate grounded and the silicon substrate biased in accumulation. The defect density (d_d) was obtained from the field breakdown yield determined at 12 MV/cm. The charge-to-breakdown distributions were determined with a constant-current stressing using a current density of 100 mA/cm^2. The amount of mobile charge on the Na samples was calculated from the voltage shift of the CV characteristics of the capacitors after a Bias-Temperature-Stress (BTS) at a temperature of 250 °C and a field of 2 MV/cm. The total oxide charge of ($Q_{ox,SCA}$) the Al samples was determined by Surface Charge Analysis (SCA) performed with a Semitest SCA2000 immediately after oxidation and also after the removal of 2 nm of the oxide layer in a 5% HF solution.

RESULTS AND DISCUSSION

The Na concentration results (Table I) indicate that the contamination level on the reference wafers is at least one order of magnitude lower than on the contaminated ones. The Na concentration after processing on the 15 nm gate oxide samples is close to the targeted value of 10^{11} atoms/cm^2 for contamination introduced before or after the oxidation (Table I). However, for the 60 nm gate oxide samples it can be noticed that part of the Na has been removed during the oxidation step as the final Na concentration of the pre-oxidation contaminated wafers is lower when compared to the values detected on the post-oxidation contaminated ones (Table I). This loss of Na atoms can most likely be explained by the sodium evaporation during the oxidation step.

The fixed oxide charge (Q_{ox}) and interface state density (D_{it}), as determined from CV measurements, and the mobile charge (Q_m) obtained from the voltage shift of the CV characteristics after BTS are also shown in Table I. These values can only be determined for capacitors with 60 nm oxides since the voltage shifts of the CV characteristics of the 15 nm samples are too small to be measured. There is no apparent correlation between the fixed charge and the sodium contamination. Also very little influence of the sodium contamination on the interface state density can be noticed. As expected, a relatively good agreement between the mobile charge and the sodium content determined by SIMS is found suggesting that all the sodium is mobile in the oxide.

The SCA results (Table II) indicate that the total oxide charge ($Q_{ox,SCA}$) is shifted to negative values due to the Al contamination. The shift in $Q_{ox,SCA}$ is found to be proportional to the Al contamination level introduced on the wafers (Table II). However, if 2 nm of all the oxide layers are removed by a dip in 5%HF a negative charge even for the reference material can be measured probably due to the high concentration of F atoms at the etched oxide surface (Table II). On these samples the effect of the Al contamination on $Q_{ox,SCA}$ is not observed anymore (Table II).

Analysing the oxide charge shift introduced by the Al contamination on the non etched oxides it is possible to notice that either each Al atom corresponds only to a partial charge or only a fraction of the Al atoms get incorporated in the oxide layer (Fig1). The latter assumption is supported by the SIMS data, as less aluminum is detected when the thermal budget is increased (Fig 1). However, the Al contamination introduced on the wafers that have only received poly deposition (no gate oxidation performed) is close to the targeted values (Fig 1).

The defect density (d_d) Na contaminated Cz and Epi wafers is shown in Fig. 2 for capacitors with 15 nm gate oxide. No significant change in defect density is observed for Na introduced before or after the gate oxidation on Epi wafers. No clear trend can be seen for capacitors fabricated on Cz material since for these wafers a substrate related breakdown mode is dominating (7). This can be observed in the breakdown histograms of Fig. 3 where a dominant breakdown mode in the mid-field region (6-10 MV/cm) is observed even for the reference Cz material which is not seen on the Epi wafers.

As in the case of Na, the aluminum contamination has no significant effect on the defect density (d_d) of the 15 nm gate oxide capacitors (Fig 4) fabricated on Epi wafers. Also in this case the performance of the Cz material is determined by a substrate effect which renders the results non-significant for the contamination effect analysis.

Charge-to-breakdown (Q_{BD}) plots for Cz and Epi wafers are shown in Fig 5 for Na contaminated samples. The substrate related defect mode dominates the Q_{BD} plots for the Cz wafers and no effect can be seen from the sodium contamination (Fig 5a). However, on the Epi wafers a large tail is observed in the Q_{BD} plots for the Na contaminated samples, which is not present for the uncontaminated ones (Fig 5b). This leads to the conclusion that Na contamination levels as low as 10^{11} at/cm^2 can present an important reliability problem, especially when the Na is introduced after the gate oxidation. Therefore, great care should be taken to avoid Na contamination prior to the electrode deposition.

The Q_{BD} analysis of the Al contaminated samples present similar results to what has been observed for the Na contaminated ones (Fig 6). The behaviour of the Cz wafers is strongly dominated by the substrate effect (Fig 6a) which has masked the possible influence of the Al contamination on the results. On Epi material such substrate related problems do not occur and a good correlation between the Al contamination introduced before the oxidation and the degradation of the Q_{BD} characteristics of the oxides can be noted (Fig 6b). This indicates that Al contamination can have a strong detrimental effect on the reliability properties of thin gate oxides.

CONCLUSIONS

The effect of a low level of sodium and aluminum contamination on the gate oxide characteristics was investigated. The amount of sodium and aluminum contamination after processing are dependent on the thermal budget applied to the wafers. In both cases by increasing the thermal budget the final concentration on the wafers is reduced. The sodium concentration after processing correlates well with the mobile charge observed in the oxide. Aluminum introduces a negative shift proportional to the Al concentration on the gate oxide charge detected by SCA. Both elements have no significant influence on the breakdown field distribution of the capacitors for the contamination levels under study. A tail in the charge-to-breakdown (Q_{BD}) plots is found for the Na and Al contaminated epitaxial wafers, which indicates that both elements can cause reliability problems. It should be noted, however, that contamination of other elements (*i.e.* Ca) at the same level (10^{11} atoms/cm^2) can have a much greater detrimental effect on the gate oxide characteristics (8).

ACKNOWLEDGMENTS

A. L. P. Rotondaro would like to thank CNPq (Conselho Nacional de Desenvolvimento Científico e Tecnológico) Brazil, for financial support. The authors would like to acknowledge Prof. G. Declerk for supporting this work.

REFERENCES

1. M. Meuris, M. Heyns, W. Küper, S. Verhaverbeke and A. Philipossian, in ULSI Science and Technology 1991, J. M. Andrew and G. K. Celler, Editors, PV 91-11, p., The Electrochemical Society Softbound Proceedings Series, Pennington, NJ, 1991.
2. S. Verhaverbeke, P. W. Mertens, M. Meuris, M. M. Heyns, A. Schnegg and A. Philipossian, Technical Conference SEMICON Europe 92, Zürich, March 10-11, 1992, in Progress in Semiconductor Fabrication, SEMI Europe, Brussels, 1992.
3. T. Ohmi, T. Imaoka, I. Sugiyama and T. Kezuka, J. Electrochem. Soc., 139, 3317 (1992).
4. T.H. DiStefano, J. Appl. Phys., 44, 527 (1973).
5. C.M.Osburn and S.I. Raider, J. Electrochem. Soc., 120, 1369 (1973).
6. M. Hourai, T. Naridomi, Y. Oka, K. Murakami, S. Sumita, N. Fujino and T. Shiraiwa, Jpn. J. Appl. Phys., 27, L2361 (1988).
7. P.W. Mertens, M. Meuris, H. F. Schmidt, S. Verhaverbeke, M. M. Heyns, D. Gräf, A. Schnegg, M. Kubota, K. Dillenbeck and A. Philipossian in IES 39th Annual Technical Meeting 1993 Proceedings Vol. 1, p. 238, IES, Mount Prospect, Illinois, (1993).
8. P.W. Mertens, H. F. Schmidt, M. Meuris, S. Verhaverbeke, D. Gräf, K. Dillenbeck, S. S. Salem and M. M. Heyns in Tech. Dig. 1993 Symp. on VLSI Technol. p. 111, JSAP, Tokyo, (1993).

Table I: Na concentration on wafers determined by poly-encapsulated SIMS measurements; fixed oxide charge (Q_{ox}), interface state density (D_{it}) and mobile charge (Q_m) as determined by CV and BTS measurements.

Na contamination (10^{11} atoms/cm^2)	Gate oxide thick. (nm)	Na conc. (10^{10}/cm^2)	Q_{ox} (10^{10}/cm^2)	D_{it} (10^{10}/cm^2)	Q_m (10^{10}/cm^2)
No	-	2.7	-	-	-
No	15	1.5	-	-	-
Pre-oxidation	15	10	-	-	-
Post-oxidation	15	12	-	-	-
No	60	0.8	4.1	3.5	1.6
Pre-oxidation	60	3.5	0.2	5.5	3.6
Post-oxidation	60	13	12	4.0	11

Table II: Al concentration on wafers determined by SIMS measurements and fixed oxide charge ($Q_{ox,SCA}$) determined by surface charge analysis for fresh and 2 nm HF etched oxides. (d.l.) stands for detection limit.

Targeted Al contamination	Wafer processing	Al conc. (10^{10}/cm^2)	$Q_{ox,SCA}$ fresh (10^{10}/cm^2)	$Q_{ox,SCA}$ HF (10^{10}/cm^2)
No	Poly	<d.l.	-	-
No	Oxide	<d.l.	+14.9	-63
No	Poly + Oxide	<d.l.	-	-
1E11	Poly	15	-	-
1E11	Oxide	-	+7.6	-58
1E11	Poly + Oxide	3	-	-
1E12	Poly	45	-	-
1E12	Oxide	-	-4.3	-59
1E12	Poly + Oxide	11	-	-

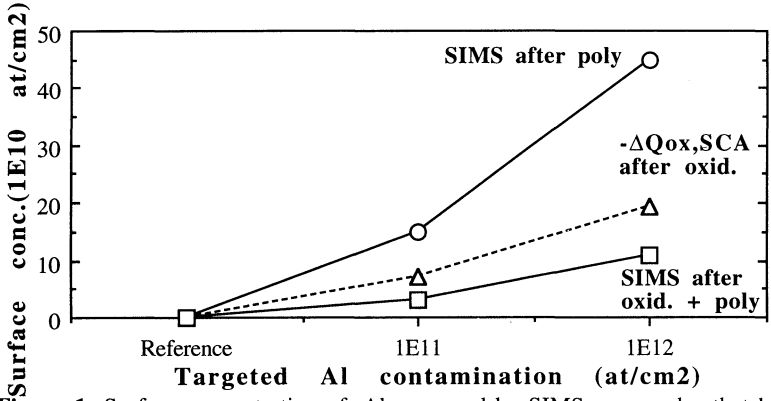


Figure 1: Surface concentration of: Al measured by SIMS on samples that have received poly deposition direct on silicon (o); Al measured by SIMS on samples that have received poly deposition on 15 nm oxide (□) and absolute fixed oxide charge shift measured by SCA on 15 nm oxides (Δ).

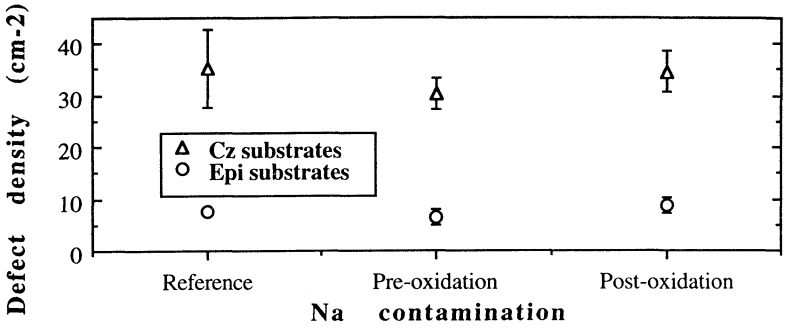


Figure 2: Defect density extracted from the field breakdown (E_{BD}) yield defined at 12 MV/cm for 15 nm gate oxide capacitors fabricated on Cz and Epi substrates that have received no, pre and post oxidation Na contamination.

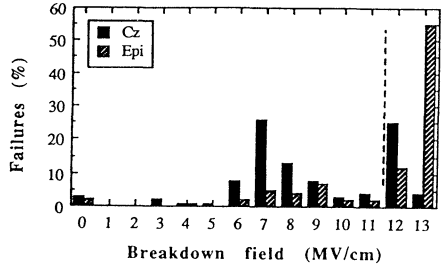


Figure 3: Breakdown field (E_{BD}) histograms for 15 nm gate oxide capacitors fabricated on Cz (full bars) and Epi substrates (dashed bars). The dashed line indicates the yield criteria of 12 MV/cm.

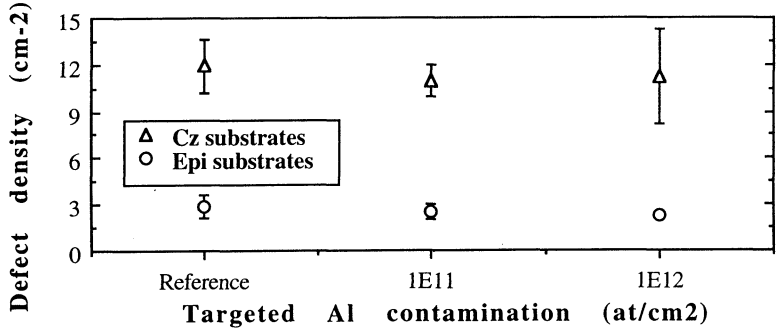


Figure 4: Defect density extracted from the field breakdown (E_{BD}) yield defined at 12 MV/cm for 15 nm gate oxide capacitors fabricated on Cz and Epi substrates that have received no, 10^{11} and 10^{12} atoms/cm^2 pre-oxidation Al contamination.

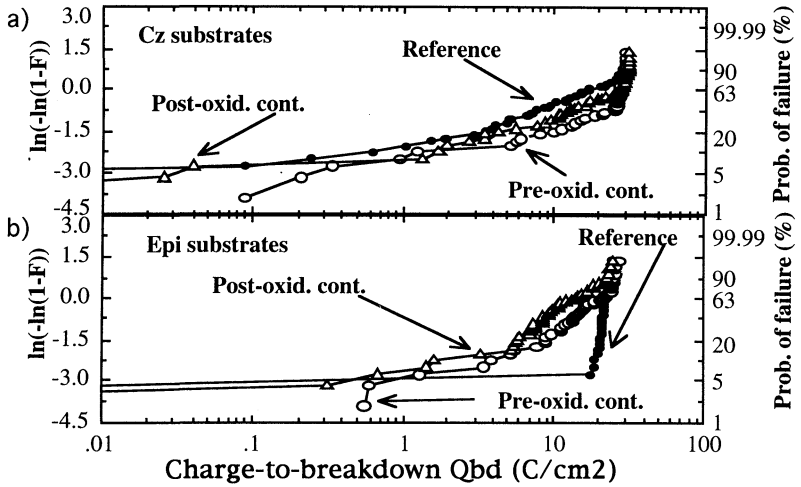


Figure 5: Charge-to-breakdown (Q_{BD}) plots obtained with a current density of 0.1A/cm^2 for 15 nm gate oxide capacitors that have received Na contamination. The results of (•) reference, (o) pre-oxidation and (Δ) post-oxidation contaminated samples are shown for (a) Cz and (b) Epi substrates.

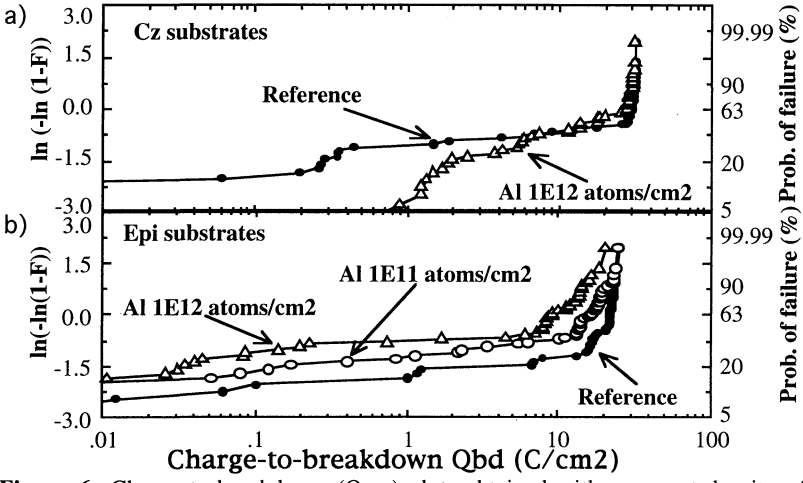


Figure 6: Charge-to-breakdown (Q_{BD}) plots obtained with a current density of 0.1A/cm^2 for 15 nm gate oxide capacitors that have received Al contamination. The results of (•) reference, (o) 10^{11} atoms/cm^2 and (Δ) 10^{12} atoms/cm^2 nominal contaminated samples are shown for (a) Cz and (b) Epi substrates.

CONTROL OF NATIVE OXIDES ON DEEP-SUBMICRON CONTACT-HOLE-BOTTOM SURFACES

N.Aoto, M.Nakamori, H.Hada, T.Kunio*, Y.Teraoka**, I.Nishiyama** and E.Ikawa

ULSI Device Development Laboratories,
*Microelectronics Research Laboratories,
**Optoelectronics Research Laboratories,
NEC Corporation

1120 Shimokuzawa, Sagamihara, Kanagawa 229, Japan
**34 Miyukigaoka, Tsukuba, Ibaraki 305, Japan

The effects of cleaning and treatments on contact-hole-bottom Si surfaces were investigated by x-ray photoelectron spectroscopy (XPS) and thermal desorption spectroscopy (TDS). Suboxide-rich native oxides are formed on dry-etch-damaged Si surfaces and still exist after DHF treatment, resulting in high contact resistance. The suboxide-rich native oxide layers are removed by chemical dry etching (CDE). After the oxide removal, native oxidation of the bottom Si surfaces immediately occurs under clean-room air exposure, while oxidation is suppressed in N_2 atmosphere. Therefore low resistance and high reliability of contacts can be achieved by the suboxide removal and by keeping contact-holes in less-oxidizing atmospheres.

INTRODUCTION

The down-scaling of current VLSI yields a minimum interconnection dimension of 0.2 μm with high aspect ratios. In cleaning and treatments of contact-holes having such deep-submicron dimensions, there are some problems to be solved in order to achieve low resistance and high reliability of the contacts. The most essential subject is the elimination of native oxides at the interface between contact-hole-bottom Si surfaces and plugging materials. For the native oxide elimination, it is necessary to satisfy the following requirements: first the complete removal of oxides on the contact-hole-bottom Si surfaces, and secondly the suppression of re-oxidation of oxide-removed Si surfaces.

In the present work, cleaning and treatment effects on characteristics of contact-hole-bottom Si surfaces are investigated in order to meet the requirements. Native oxides on Si surfaces under contact-hole processing are analyzed by using x-ray photoelectron spectroscopy (XPS) for non-patterned surfaces. Suppression of native oxides on the contact-hole-bottom Si surfaces by exposing to an N_2 atmosphere is also examined by thermal desorption spectroscopy (TDS).

EXPERIMENTS

Figure 1 shows a schematic diagram of treatment processes for contact-holes and non-patterned Si surfaces. Non-patterned Si surfaces of ion-implanted n^+ layers were treated in the same way as contact-holes after etch-back of HTO layers. The non-patterned Si surfaces simulate the properties of contact-hole-bottom Si surfaces.

O_2 plasma treatment and wet cleaning in a H_2SO_4 and H_2O_2 mixture (SPM) were performed for removing carbon-polymer deposition films. Chemical dry etching (CDE) was used for removing dry-etch damaged layers. For comparison, a part of samples was not treated by CDE. Wet cleaning in both a NH_4OH, H_2O_2 and H_2O mixture, and a HCl, H_2O_2 and H_2O mixture (HPM) were used for removing particles and metal contaminations. Dipping in a diluted HF solution (DHF) was used for native oxide removal.

Non-patterned Si surfaces were analyzed using XPS after each treatment step. The non-patterned Si surfaces can roughly simulate the properties of the contact-hole-bottom Si surfaces. Contact-hole-bottom Si surfaces were analyzed by TDS after exposing to clean-room air or to an N_2 atmosphere.

RESULTS AND DISCUSSION

Figure 2 shows compositions, analyzed by XPS, of non-patterned n^+ layers after each treatment. Contaminations of C and F, which form CF_x polymers as indicated in C(1s) spectra, were removed by O_2 plasma treatment. The surfaces treated by CDE showed an increase in Si composition and a decrease in O composition after the last DHF dipping step. In contrast, the surfaces without CDE showed considerable O composition even after DHF dipping. The measurement of contact resistance for contact arrays showed that CDE lowered the resistance corresponding to the O composition decrease.

It has previously been reported that CDE improves the electronic properties of contacts by removing dry-etching damage on contact-hole-bottom Si surfaces (1). The effect of CDE was precisely examined in the present work by means of Si(2p) XPS spectra. Figure 3 shows the Si(2p) spectra for n^+ layers after each treatment. The spectra show chemical shifts, which are assigned to SiO_x as follows. As shown in Fig.2, the F compositions after treatments are small in comparison with O composition. The C compositions after treatments are less than 10%. It has been reported that the C composition of less than 29% in SiC_x cause the Si(2p) chemical shifts of less than 0.4 eV (2). Thus the influence of F and C on the Si(2p) chemical shifts is negligible. Therefore chemical shifts shown in Fig.3 after treatments are mainly due to Si oxides. The shifts are deconvoluted to Si suboxide peaks.

In Fig.3, the CDE-treated surfaces show low amounts of suboxides after APM and HPM, and show no oxides except Si^{1+} after the last DHF dipping step. On the other hand, the Si(2p) spectra for surfaces without CDE show higher amounts of the suboxides after every treatment step. On the suboxide-rich surfaces, even Si^{4+} is not easily dissolved by DHF dipping.

The Si_{4+} persistence on the suboxide-rich surfaces after DHF-dipping is considered as follows. The Si^{4+} on non-CDE surfaces are mixed with suboxides. The Si-Si bonds of the suboxides are not dissolved by DHF dipping. Thus the Si^{4+} located deeper than the suboxides cannot be dissolved by DHF dipping. Such suboxide-rich layers is considered to be caused by dry-etching damage such as crystalline defects.

Based on the above mentioned experimental results, the contact-hole-bottom Si

surface conditions can be schematically illustrated in Fig.4. After etching, the contact-hole-bottom Si surface contains CF_x polymers on dry-etch-damaged defect layers. After the removal of CF_x by O_2 plasma treatment and SPM cleaning, the surface becomes suboxide-rich. CDE completely removes the damaged layer, resulting in a native oxide of a low suboxide density after APM and HPM cleaning. On the other hand, a surface without CDE still contains the damaged layer, whose top becomes the suboxide-rich native oxide. After the last DHF dipping step, the suboxide-free native oxide is dissolved, while the suboxide-rich native oxide stays on the surface.

After the oxide removal on the contact-hole-bottom Si surfaces, it is necessary to prevent re-oxidation of the bottom surface before plugging in order to avoid the increase of contact resistance. Native oxidation of bare-Si surfaces easily occurs in a humid air environment, while oxidation is prevented in a dry N_2 atmosphere (3). Thus, the control of surrounding atmospheres is needed for the prevention of contact-hole bottom oxidation.

In this point of view, TDS analysis was employed for the examination of the effect of oxidation prevention under exposure to an N_2 atmosphere. Figure 5 shows TDS spectra of ^{30}SiO (m/e=46) for 0.4 μm-diameter contact-holes which are formed on p-Si surfaces with contact-walls of thermal oxide. The ratio of peak intensities for the desorption spectra of m/e = 44, 45 and 46 are in good agreement with the existence ratio of Si-isotopes, ^{28}Si, ^{29}Si and ^{30}Si. Therefore it is indicated that the influence of the background CO_2 (m/e=44) on the TDS peak intensities is negligible. Since SiO desorption was not observed from the thermal oxide films, the peaks are due to SiO desorption from the hole-bottom Si surfaces. On samples after APM and HPM cleaning following etching and treatments (see Fig.1), the spectrum of SiO desorption shows a peak which indicates the existence of the native oxide layer on the contact-hole-bottom Si surface. The peak disappears after DHF dipping, indicating that the oxide layer is removed. After exposure to clean-room air for 43 hours, a SiO desorption peak appears again, while no peak is observed on the spectrum for a sample exposed to a 1 atm N_2 atmosphere for the same period.

In the TDS analysis, the temperature of SiO desorption reflects the thickness and the quality of the oxide films on Si surfaces. Figure 6 shows TDS peak temperature of SiO desorption for contact-hole-bottom Si surfaces of n^+ and p^+ as a function of exposure time to clean-room air and 1 atm N_2. Oxidation of contact-hole-bottom Si surfaces of both n^+ and p^+ is prevented in N_2 for less than 43 hours. In contrast, oxidation easily occurs on both surfaces under exposure to clean-room air. In order to prevent oxidation of contact-hole bottoms for obtaining low resistance, therefore, it is necessary to keep contact-holes in a N_2 atmosphere or to plug them immediately after oxide removal.

CONCLUSION

Thin oxide layers formed on contact-hole-bottom Si surfaces were investigated by XPS and TDS. The effects of cleaning and treatments on the surfaces were also examined. Suboxide-rich native oxides are formed on dry-etch-damaged Si surface and still exist after DHF treatment, resulting in high contact resistance. The suboxide-rich native oxide layers are removed by chemical dry etching (CDE). After oxide removal on contact-hole-bottom Si surfaces, native oxidation of the bottom Si surfaces immediately occurs under clean-room air exposure, while oxidation is suppressed in N_2 atmosphere. Therefore low resistance and high reliability of contacts can be achieved by the suboxide removal and by keeping contact-holes in less-oxidizing atmospheres. The results obtained here can be effectively applied to designing the integrated

processes of contact-hole treatments, from dry etching to contact-hole plugging, in the fabrication of deep-submicron contacts for future devices.

ACKNOWLEDGMENTS

The authors wish to thank Drs. N.Endo, M.Sakamoto, A.Ishitani, T.Kikkawa, and K.Kasai for their helpful discussions. We also thank S.Yamasaki, T.Hukase, M.Komuro and J.M.Drynan for their supports and discussions. We thank Dr. S.Hoshino for his cooperation in the XPS analysis.

REFERENCES

1)M.Sekine et al.,in Extended Abstract of the 1992 International Conference of Solid State Devices and Materials, Tsukuba, Japan,p.184(1992).
2)W-Y.Lee, J.Appl.Phys.,**51**,3365(1980).
3)M.Morita et al., Appl.Phys.Lett.,**55**,562(1989).

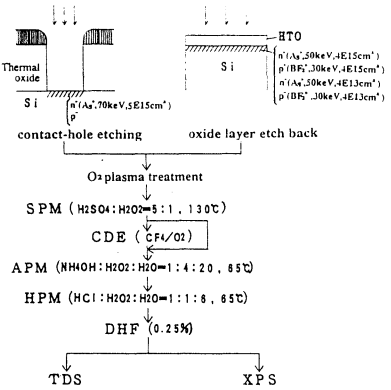


Figure 1 A schematic diagram of Si-surface treatment processes for contact-holes and non-patterned Si surfaces.

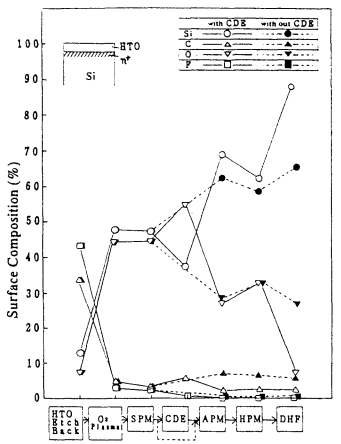


Figure 2 Variance of composition on n^+-Si surfaces through treatment steps.

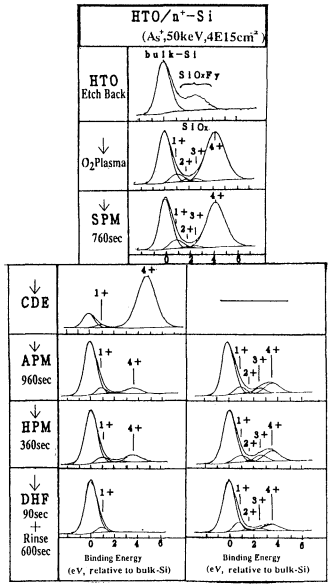


Figure 3 Si(2p) XPS spectra of n^+-Si surfaces after each treatment step.

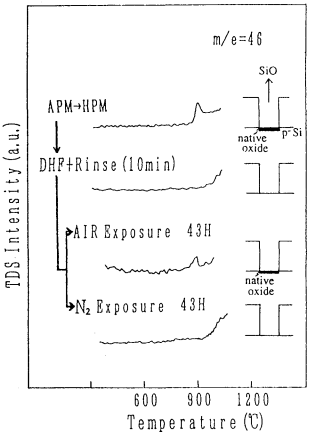


Figure 5 TDS spectra of SiO (m/e=46) for contact-hole-bottom p^--Si surfaces after cleaning, DHF dipping and preservation in one of two atmospheres.

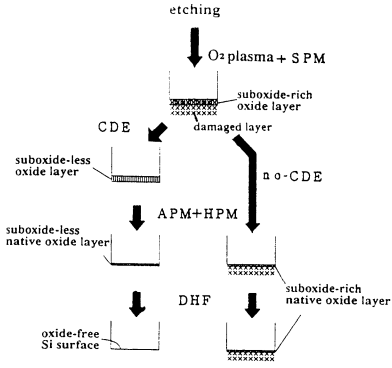


Figure 4 A model of variation of contact-hole-bottom Si surfaces through treatment processes.

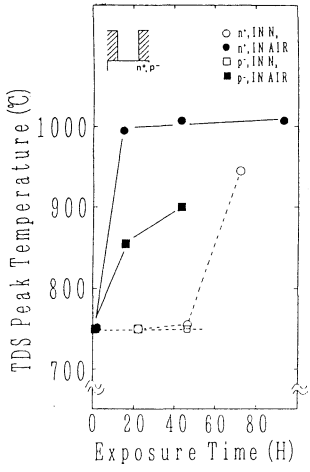


Figure 6 Temperature change of TDS peaks as a function of the exposure time periods to clean-room air and N_2.

ULTRA THIN OXIDE FORMATION USING CHEMICAL OXIDE PASSIVATION

K. Nakamura[1], T. Futatsuki[1,2], K. Makihara[1] and T. Ohmi[1]

[1] Department of Electronic Engineering, Faculty of Engineering, Tohoku University, Sendai 980, Japan.
[2] Laboratory for Microelectronics, Research Institute of Electrical Communication, Tohoku University, Sendai 980, Japan.

ABSTRACT

We have investigated electrical characteristics of MOS devices with the gate oxide films incorporating the chemical oxides used as a passivation film of silicon surface. The gate oxide films incorporating the chemical oxides formed in H_2SO_4/H_2O_2, O_3/H_2O and hot H_2O_2 are superior to those incorporating the chemical oxides formed in $NH_4OH/H_2O_2/H_2O$ and $HCl/H_2O_2/H_2O$ in reliability. In the characteristics of charge to breakdown(Q_{BD}), the gate oxides with the chemical oxide formed in O_3/H_2O is superior to the gate oxides with other chemical oxides. We suggest using the chemical oxide formed in O_3/H_2O as a passivation film.

INTRODUCTION

Future ultra large scale integrated (ULSI) devices demand ultra thin oxide films with high reliability for the scaling down of the minimum device dimension. Perfect control of silicon surface condition is essential to form highly reliable oxide films. It has been reported that the increase of silicon surface microroughness and impurities adsorbed on silicon wafer cause the degradation of the reliability of thin gate oxide films[1-4]. During device fabrication, the silicon wafer is treated with various chemical cleaning. Before gate oxidation, the silicon wafer is treated with RCA cleaning and which is followed by the treatment in the diluted HF solution and rinsed in ultrapure water. After this, the silicon wafer is transported in air ambience and loaded into the oxidation furnace. At this stage, the silicon surface is subject to various contaminations such as adsorption of impurities in air and native oxide growth. As a result, this is one reason that device performances is degraded.

Furthermore, the wafer may be maintained in inert gas ambience during the wafer heating up to oxidation temperature, because an oxide layer must not be formed during the wafer heating up[5]. However, heating the wafer in an inert gas ambience leads to an increase in silicon surface microroughness, because the silicon surface is etched by trace moisture and oxygen in the inert gas[6]. Therefore, a passivation film is necessary. The

growth of the passivation film must also be controlled before gate oxidation, because the current density level through the gate oxide with a thick passivation oxide film is enhanced in the low electric field region[5]. Because of these reasons, the passivation films formed on silicon surface are required to be as thin as possible. Accordingly, we use the chemical oxides formed in various chemicals at the final step of wafer cleaning for the passivation films, because the thin oxide film is easily formed in chemical and because impurity concentration in chemicals is extremely low[7]. In this paper, we describe electrical characteristics of the gate oxides using chemical oxide films.

EXPERIMENTAL

In this experiment, we used Cz, B-doped p-Si(100) wafers with 0.4-0.6 ohm·cm resistivity. MOS devices were fabricated after field oxide was formed by wet oxidation. Table 1 shows the experimental procedure and the condition for passivation film formation. Before gate oxidation, the silicon wafer was treated with RCA cleaning, HF/H_2O_2 solution, and ultrapure water rinsing. At this point, the control wafer in Table 1 was transported in air ambience and loaded into the oxidation furnace. It was heated up to 300°C in ultraclean argon gas, and oxidized at 300°C in ultraclean oxygen gas in order to form a 0.4nm oxide passivation layer. The wafer was heated to oxidation temperature of 900°C in ultraclean argon gas in the oxidation furnace and was oxidized at 900°C in ultraclean oxygen for gate oxidation. In Other samples, after chemical cleaning, silicon wafer was treated with one of various chemicals such as SPM, O_3/H_2O, hot H_2O_2, APM and HPM, to form the chemical oxide on the silicon wafer. After this, the silicon wafers were transported in air ambience and loaded into the oxidation furnace. The wafers were heated to oxidation temperature of 900°C in ultraclean argon gas in the oxidation furnace and were oxidized at 900°C in ultraclean oxygen for gate oxidation. The control and gate oxides were formed in the ultraclean oxidation system characterized by extremely low moisture and extremely low metal impurity concentration due to investigate the effects of chemical oxides[5,8]. The gate electrodes for the MOS devices were n^+-polycrystalline silicon. The forming gas annealing was performed at 400°C for 30min in H_2/N_2(10% hydrogen 90% nitrogen).

The quality of chemical oxide was evaluated by etching rate. As etchant, BHF solution with 0.1nm/min etching rate for thermal oxide at 25°C was used. The chemical oxide thickness was measured by X-ray photoelectron spectroscopy(XPS)[9,10].

RESULTS AND DISCUSSION

Figure 1 shows the etching rates of various chemical oxides. The etching rate of all the chemical oxides is higher than that of thermal oxide (etching rate 0.1nm/min). The chemical oxide quality is different by the forming method. Also the etching rate varies with time, presumably because the oxide quality is not uniform across the film.

Figure 2 shows dielectric breakdown characteristics of MOS(n^+-polycrystalline $Si/SiO_2/p-Si$) diodes with 5nm thick gate oxide films incorporating chemical oxides formed by various chemicals. Breakdown field events concentrate in the range of 12-13MV/cm in the case of the gate oxide films with the passivation oxide formed by control, SPM, O_3/H_2O and hot H_2O_2 method. While the breakdown fields of the gate oxides with the chemical oxides formed in APM and HPM are distributed in the lower electric field region. This result indicates that the chemical oxides formed in APM and HPM cannot be used as the passivation film for 5nm thick gate oxide film.

Figure 3 shows cumulative failure of MOS(n^+-polycrystalline $Si/SiO_2/p-Si$) diodes with 6nm thick gate oxide films incorporating chemical oxides formed by various chemicals. The gate electrode is negatively biased, the current density is $-100mA/cm^2$. The gate area of measurement device is $1\times10^{-3}cm^2$. The characteristics of the gate oxide incorporating the chemical oxide formed in HPM is inferior to the others. This is thought to be because of the chlorine and hydrogen, which are taken in the chemical oxide formed in HPM, diffuse and combine with silicon in the gate oxide[11], therefore many traps are formed in the gate oxide. On the other hand, the characteristics of the gate oxide incorporating the chemical oxide formed in O_3/H_2O is superior to the others. This result indicates that the reliability of the 6nm thick gate oxide incorporating the chemical oxide formed in HPM is lower.

Figure 4 shows current density-average oxide field characteristics of MOS (n^+-polycrystalline $Si/SiO_2/p-Si$) diodes under the negatively biased metal electrodes for 5nm thick gate oxide films incorporating the chemical oxides formed by various chemicals. The current level through the gate oxide incorporating the chemical oxide formed in APM is higher than that through the others in the low electric field range. This is thought to be because silicon surface is deeply etched during APM cleaning. As a result, the leakage current at a low electric field increases due to the electric field concentration near the gate electrode edge. It is also possible that the metal impurities in the APM solution, such as Fe and Al, are taken in the chemical oxide during the formation of the chemical oxide[12] and diffuse in the gate oxide. It is believed that this influence of the gate oxide reliability is great even when the metal impurity concentration in the gate oxide is low.

The above indicates that the chemical oxide formed in O_3/H_2O is the most effective film as a passivation film. That chemical oxide is formed at room temperature in a solution in which only H_2O and O_3 exist. Therefore it is easy for the chemical oxide to be controlled. We suggest using the chemical oxide formed in O_3/H_2O as a passivation film. We will call the chemical oxide formed in O_3/H_2O the ozonized ultrapure water preoxide.

Figure 5 shows the threshold voltage(Vth) shift of n-MOSFET with 9nm thick gate oxides as a function of the number of injected electrons. The hot electrons are injected from the substrate into the gate oxide[13,14]. The current density into the gate oxide is $1mA/cm^2$, the oxide field is 5MV/cm and the substrate bias is -10V. The threshold voltage(Vth) is defined as the gate voltage at which the channel current of MOSFET is $1\times10^{-6}A$. The threshold voltage(Vth) shift for the sample having the gate oxide with ozonized ultrapure water preoxide is the same as that of the control sample.

Therefore, the number of electron traps in gate oxide is also the same level. It has been reported that electron traps are caused by the water-related trap[15,16]. So it is considered that the water-related traps inducing by ozonized ultrapure water preoxide are rare in the gate oxide though the passivation film is formed in ultrapure water.

Figure 6 shows the gate voltage(Vg) shift of MOS(n^+-polycrystalline $Si/SiO_2/p$-Si) diodes with 6.6nm thick gate oxide films. The gate electrode is negatively biased, the current density is $-1mA/cm^2$. The gate area of measurement device is $1\times10^{-4}cm^2$. The gate voltage(Vg) shift of the sample having the gate oxide with ozonized ultrapure water preoxide is smaller than that of the control sample. Therefore, it is considered that the gate oxide with ozonized ultrapure water preoxide has lower hole traps.

CONCLUSION

We have investigated the electrical characteristics of MOS devices with the gate oxides incorporating the chemical oxides formed in various chemicals. The gate oxide films incorporating the chemical oxides formed in SPM, O_3/H_2O and hot H_2O_2 are superior to those incorporating the chemical oxides formed in APM and HPM in reliability. This indicates that the reliability of gate oxides depends on passivation oxide film formation method. We feel that the chemical oxide films formed in SPM, O_3/H_2O and hot H_2O_2 are effective to protect silicon surface for the formation of the gate oxide film with high reliability. Among those chemical oxides, the chemical oxide formed in O_3/H_2O is the most effective film as a passivation film. The chemical oxide thickness and quality are influenced by the chemical concentration in the solution. In the hot chemical solution, the chemical concentration is continuously changing because of evaporation and decomposition. While ozonized ultrapure water preoxide is formed at room temperature. So the O_3 concentration in the solution is easy to control. As a result, high quality passivation film is formed reproducably. Therefore, we suggest the use of a chemical oxide formed in O_3/H_2O as a passivation film before gate oxidation.

ACKNOWLEDGEMENT

The majority of this work was carried out at the Super Clean Room of the Laboratory for Microelectronics, Research Institute of Electrical Communication, Tohoku University.

REFERENCES

[1] M. Miyashita, M. Itano, T. Imaoka, I. Kawanabe and T. Ohmi, in Digest, Technical Papers, 1991 VLSI Symposium, Oiso, 1991, p.45.

[2] T. Ohmi, M. Miyashita, M. Itano, T. Imaoka and I. Kawanabe, IEEE Trans. Electron Devices, **39**, 537(1992).
[3] M. Miyashita, T. Tsuga, K. Makihara and T. Ohmi, J. Electrochem. Soc., **139,** 2137(1992).
[4] T. Ohmi, J. Takano, T. Tsuga, M. Kogure, S. Aoyama, K. Matsumoto and K. Makihara, in Digest, Technical Papers, 1992 VLSI Symposium, Seattle, 1992, p.24.
[5] K. Makihara, A. Teramoto, K. Nakamura, M. Y. Kwon, M. Morita and T. Ohmi, Jpn. J. Appl. Phys. **32**, 294(1993).
[6] M. Offenberg, M. Liehr, G. W. Rubloff and K. Holloway, Appl. Phys. Lett. **57**, 1254(1990).
[7] K. Kimura, Y. Ogata, F. Tanaka, T. Imaoka, J. Takano, T. Isagawa, T. Kezuka, M. Kogure, T. Futatsuki and T. Ohmi, in Contamination Control and Defect Reduction in Semiconductor Manufacturing I/1992, edited by D. N. Schmit, (The Electrochemical Society, Pennington, NJ, 1992), p.347.
[8] T. Ohmi, M. Morita, A. Teramoto, K. Makihara and T. S. Tseng, Appl. Phys. Lett. **60**, 2126(1992).
[9] M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami and M. Ohwada, J. Appl. Phys., **68**, 1272(1990).
[10] M. Morita and T. Ohmi, Mat. Res. Soc. Symp. Proc., 259, 19(1992).
[11] H. Ogawa and T. Hattori, IEICE Trans. Electron., Vol.E75-C, 774(1992).
[12] T. Shimono, M. Morita, Y. Muramatsu and M. Tsuji, Proceedings of 8th Workshop on VLSI Ultra Clean Technology, 59(1990).
[13] C. A. Bosselear, Solid-State Electron., **16**, 648(1973).
[14] J. F. Verwey, J. Appl. Phys., **44**, 2681(1973).
[15] E. H. Nicollian, C. N. Berglund, P. F. Schmidt and J. M. Andrews, J. Appl. Phys., **42**, 5654(1971).
[16] M. Morita, K. Nakamura, A. Teramoto, K. Makihara and T. Ohmi, in Extended Abstracts in The 183rd Electrochemical Society Meeting, Hawaii, 1993, 589.

Table 1 Experimental procedure and condition of chemical oxide formation

RCA cleaning → HF/H_2O_2 cleaning → Ultrapure water rinse→Sample formation

$NH_4OH:H_2O_2:H_2O$=0.05:1:5

$HCl:H_2O_2:H_2O$=1:1:6

$HF:H_2O_2:H_2O$=1:30:60

Samples	Method
Control	Preoxidation in dry O_2 for 20 min and annealing in Ar for 20min at 300°C.
SPM	Chemical oxide formed in SPM solution ($H_2SO_4:H_2O_2$=4:1) for 5 min at 120°C.
O_3/H_2O	Chemical oxide formed in Ultrapure water injected O_3 (concentration: 2 ppm) for 10 min at R.T.
hot H_2O_2	Chemical oxide formed in 30%H_2O_2 solution for 10 min at 80-90°C.
APM	Chemical oxide formed in APM solution ($NH_4OH:H_2O_2:H_2O$=0.05:1:5) for 10 min at 80-90°C.
HPM	Chemical oxide formed in HPM solution ($HCl:H_2O_2:H_2O$=1:1:6) for 10 min at 80-90°C.

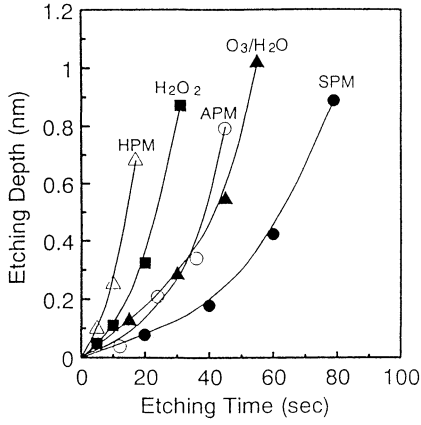


Figure 1. Etching rates of various chemical oxides. The etchant is BHF with 0.1nm/min etching rate for thermal oxide at 25°C.

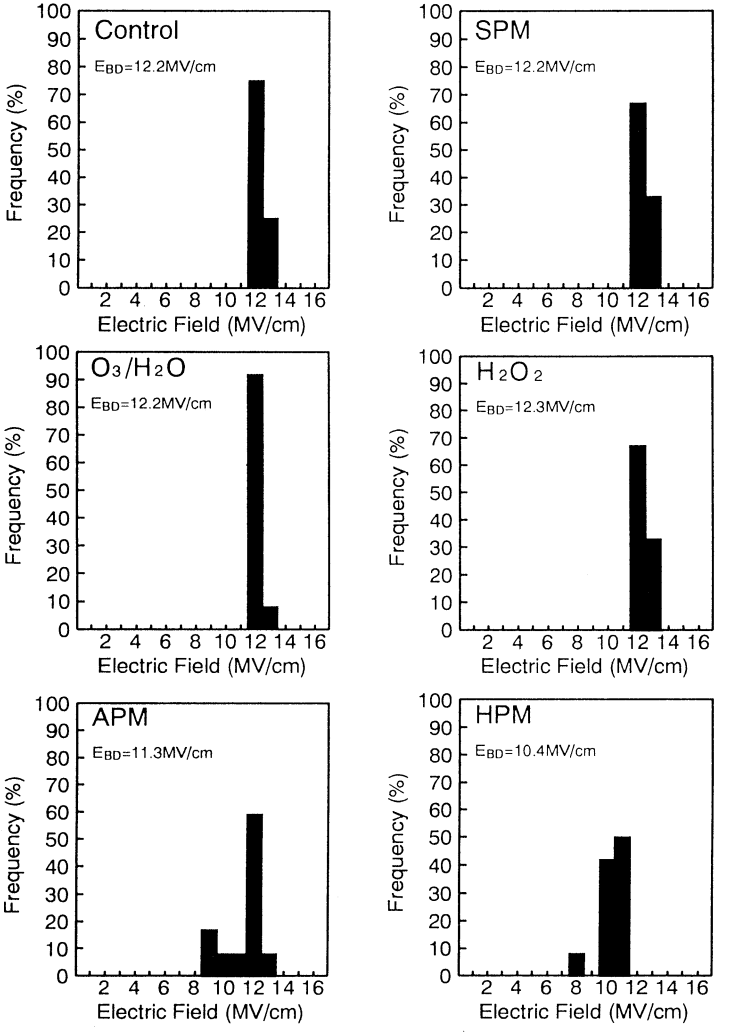


Figure 2. Dielectric breakdown characteristics of MOS diodes for 5nm thick gate oxide films incorporating chemical oxides formed by various chemicals.

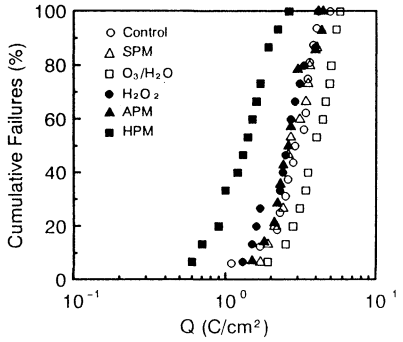


Figure 3. Cumulative failure under the negatively biased metal electrodes of MOS diodes with 6nm thick gate oxide films incorporating chemical oxides formed by various chemicals, as the current through the oxide is kept constant.

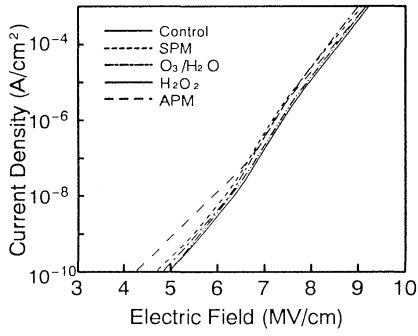


Figure 4. Current density-average oxide field characteristics of MOS diodes with 5nm thick gate oxide films incorporating the chemical oxides formed by various chemicals.

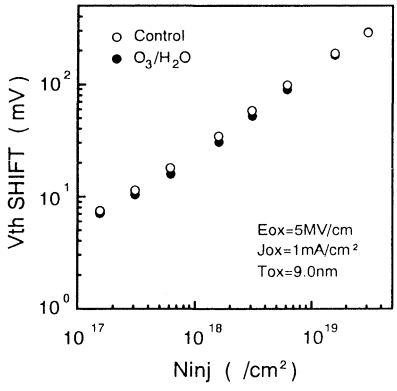


Figure 5 Threshold voltage(Vth) shift of n-MOSFET with 9nm thick gate oxides as a function of the number of injected electrons.

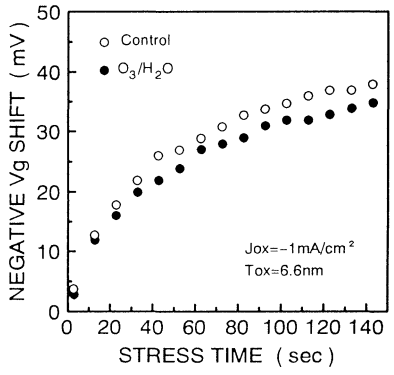


Figure 6 Gate voltage(Vg) shift of MOS diodes with 6.6nm thick gate oxide films, as the current through the oxide is kept constant.

PECULIARITIES OF HOT PHOSPHORIC ACID USED IN ETCHING SILICON NITRIDE

W. Syverson, M. Fleming
IBM Microelectronics
Essex Junction, Vermont 05452

The process of etching silicon nitride with hot phosphoric acid is commonly used by many semiconductor producers. Although the process appears fairly straightforward, knowledge of its peculiarities and actual mechanics is typically fairly limited. This paper details the aspects of chemical transformations during heating, the importance of DI water makeup, nitride and oxide etch rates, acid contaminant levels and wafer foreign-material levels, as well as the importance of adequately rinsing the wafers with DI water after phosphoric acid exposure.

Introduction

Hot phosphoric acid is commonly used in the semiconductor industry to remove silicon nitride (Si_3N_4) from patterned wafer surfaces. As with any process, many diverse factors must be considered simultaneously to adequately control the phosphoric-acid silicon-nitride etch process:

1) A chemical transformation begins at 154°C during heating and water is given off as a by-product of the reaction.

2) The silicon nitride (Si_3N_4) etch rate is stable over a typical bath: however, the silicon dioxide (SiO_2) etch rate is not.

3) For etch-process stability, makeup water must be continuously added to the phosphoric acid.

4) The manufacturer of the acid can play a major role in minimizing wafer foreign-material levels.

5) A time-dependent wafer-hazing phenomenon post-phosphoric has been observed and characterized.

This paper identifies and describes several findings relative to the process intricacies of removing silicon nitride from semiconductor wafer surfaces using hot phosphoric acid.

Phosphoric-Acid Dynamics During Heating

Ortho-phosphoric acid (H_3PO_4), as purchased from most suppliers, is received at about an 85% standard concentration. But, during heating, the acid concentration increases due to the evaporation of excess water and a chemical reaction begins to occur within the phosphoric acid. When a temperature of 154°C is reached, the ortho-phosphoric acid transforms to pyro-phosphoric acid ($H_4P_2O_7$) and water is given off as a by-product of the reaction. Pyro-phosphoric acid will begin to form at 154°C per the equation:

$$2H_3PO_4 <==> H_4P_2O_7 + H_2O$$

Further heating of the phosphoric acid to its typical processing temperature range of 165°C to 185°C will extend that chemical reaction. Additional water produced in the reaction will slow the heating of the acid bath (Figure 1). Heating a phosphoric-acid bath to a standard processing temperature of up to 185°C can take up to three hours. At that temperature, the phosphoric acid concentration will reach 93%. Continued heating of the acid well beyond 200°C would result in a second chemical transformation where meta-phosphoric acid (HPO_3) would be formed and, eventually, solid phosphate (P_2O_5). Once again, water is the by-product of these chemical reactions.

Phosphoric-Acid Etch Rates

As with any semiconductor manufacturing process, a stable and predictable operating condition is highly desirable. Etching silicon nitride with phosphoric acid is extremely useful in that regard because at a steady-state operating condition, the nitride etch rate of phosphoric acid is very stable. In addition, the etch rate is stable when measured for both duration of the bath life and wafer throughput through the bath. The nitride etch rate is also very repeatable with each successive bath.

Although phosphoric acid etch-rate selectivity of nitride to silicon dioxide is typically very good (e.g., >20:1), the oxide etch rate itself is not very stable. In particular, the number of wafers processed through a given bath largely determines the oxide etch rate. Figure 2 shows how the oxide etch rate decreases as wafer-throughput levels in a bath increase. Although the oxide etch rate appears to decrease predictably, the rate of etching never quite reaches zero over the life of the bath. The oxide etch rate does not vary over the bath life and is repeatable bath-to-bath.

Importance of Makeup Water

A stable phosphoric acid concentration is very important because it determines the stability of nitride and oxide etch rates over the life of the bath. But, maintaining a stable acid concentration is very difficult due to the very high operating conditions of the phosphoric acid. To maintain etch-rate stability, there must be a continuous, controlled replenishment of the bath DI water lost through evaporation when the tank temperature was at its operating temperature. The constant introduction of sufficient makeup DI water plays an important role in etching both nitride and oxide films. Without an excess of water, the etch rates for both nitride and oxide films are not easily controllable or predictable.

From a steady-state condition of sufficient DI water addition, the nitride etch rate is directly related to the amount of makeup DI water added to the acid bath. A prolonged deficiency of DI water will significantly DECREASE the nitride etch rate and increase the oxide etch rate.

Two methods are commonly employed to compensate for the loss of water: a condensing tank lid and injecting makeup DI water. When a condensing tank lid is used to trap escaping water vapor, a portion of the escaping DI water vapor, or steam, is condensed and allowed to drain back onto the surface of the acid bath. But, when trapped in this manner, a large portion of the condensed water vapor again flashes to steam before it can be reabsorbed by the acid. Therefore, this technique is generally insufficient to capture all of the escaping water vapor and efficiently return it to the acid.

However, when makeup DI water is injected well below the acid surface, additional time is allowed for the water to be effectively absorbed into the acid. Any excess DI water will merely result in a more vigorous boiling of the acid due to steam generation. An excess of DI water also insures that both nitride and oxide etch rates are stabilized.

Turning off a DI water injection system that supplies makeup water to a bath will not cause an immediate change in nitride or oxide etch rates. It takes time for enough water to evaporate due to the viscous nature of the acid. However, in as little as two hours after turning off the water injection system, the change in etch rates is measurable.

Wafer Contamination Levels

The hot phosphoric acid nitride etch process is inherently one of the dirtier processes used today in semiconductor processing. The contamination is widely known to derive from two primary sources -- acid viscosity and high processing temperatures, which make effective filtering of the acid difficult. However, two lesser known sources

can also play a significant role in controlling contamination. Both have been identified as originating from the acid manufacturer.

Phosphoric acid suppliers can be a first-order contributor to device defect density. Figure 3 compares wafer foreign-material (FM) levels measured on flat, thermal-oxide monitor-wafer wafer surfaces using a standard wafer-surface FM measurement tool with a 0.5-μm detection sensitivity threshold. Both acid suppliers were site-qualified to supply standard VLSI phosphoric acid. However, when wafer-surface FM levels were measured, Vendor 'A' averaged 1,580 FM adders, and Vendor 'B' averaged 58 FM adders. Although the reason for these differences was never pursued, the dedication to the best-of-breed supplier of the phosphoric acid was an easy decision.

The second finding is that phosphoric acid supplied by various vendors can contribute to alpha-particle emission levels as measured on wafer surfaces; emissivity levels also appeared to be wafer-surface film dependent. Wafers were prepared with either a nitride:oxide:silicon, oxide:silicon or just a bare silicon wafer surface and the following process was performed for each of the three vendor acids. Groups of wafers were immersed for 20 minutes in 185°C phosphoric acid from each vendor. Next, the wafers received a standard set of DI water rinses and centrifuge dry. Finally, the wafers were measured using a very sensitive zinc-sulfide alpha-particle scintillation counter. The results were significant (Figure 4). Not only were there vendor-to-vendor differences in alpha-particle emissivity levels, there were also differences between wafer-surface types. The vendor results should not be surprising. Phosphoric acid is manufactured from raw materials from various sources that possess natural levels of radioactivity. The wafer-surface results should be of minimal concern as long as an oxide remains on the wafer surface after processing to protect the underlying silicon.

Phosphoric Acid Tank Material

The construction materials used for phosphoric acid tanks also need to be considered. The semiconductor industry commonly uses quartz material to fabricate hot phosphoric acid tanks. However, repeated thermal stresses caused by the high operating temperatures of phosphoric acid can cause a quartz tank to rupture during use; to design and construct an adequate spill-containment facility would be very costly and cumbersome. Also, quartz, or silicon dioxide, is consumed by the phosphoric acid during processing. With all of the process variables that can affect a process, a variable that includes consumption of the very material intended to contain a process, is highly questionable. Both of these facts are cause for considering a material other than quartz for the phosphoric acid tanks.

Time-Dependent Wafer Hazing

When wafers are exposed to hot phosphoric acid, they become extremely difficult to rinse clean. Although very hygroscopic, the acid is also very viscous and highly hydrophilic, making it very difficult to preclude wafers from developing a haze. Even with extensive DI water rinsing, oxide wafer surfaces can retain as much as 0.5 atomic-weight percent of phosphorous, as measured by electron spectroscopy for surface analysis (ESCA).

An artifact of this residual phosphoric acid on oxide wafer surfaces is an observed time-dependent wafer-hazing phenomena. Although not visible immediately after processing wafers through the acid-rinse-dry process, the haze can be seen after 8 to 24 hours subsequent to acid exposure and when the wafers are stored in an ambient fabricator room air environment. The more aggressive the subsequent DI water rinses, the longer it will take for the haze to develop.

The haze is best observed with either dark-field or phase-contrast optical microscopy. Figure 5 is an optical dark-field photograph of the haze. The haze is comprised as a field of high-density light-point wafer surface defects. However, bright-field optical microscopy and scanning electron microscopy (SEM) are of limited value in identifying the haze. Figure 6 is an SEM micrograph of the haze; a thin gold film was evaporated on the sample to highlight the shape and size of the haze defect itself. Monochromatic light can used to detect the haze, but only when the haze is fully developed several days after exposure to the acid.

Two physical properties can be used to characterize the haze: (1) Simple heating of the wafer to at least 150°C for several minutes can eliminate the visual appearance of the haze; however, the haze will reappear within several hours; and (2) Once the haze is present, it can be rinsed from the wafer surface with DI water and will not return. In this case, the surface phosphorous concentration can be reduced to as little as 0.07 atomic-weight percent, as measured by ESCA surface analysis. These physical properties, coupled with the ESCA analysis, imply that haze is a manifestation of the residual hygroscopic phosphoric acid which will absorb atmospheric moisture over an extended period of time.

Conclusion

Silicon nitride etching with hot phosphoric acid is one of the more common wet chemicals used in semiconductor manufacturing today. The phosphoric acid process is very cost effective and traditionally has been as good or better than available alternatives. However, for many of the those same reasons, phosphoric acid is also one of the most overlooked and least understood wet chemicals. Under closer examination, phosphoric

acid has been shown to be much more dynamic than it would first appear. A myriad of factors from etch-rate control to source of the acid, to residue rinsability needs to be considered to adequately control the process. As with any wafer process, the unique aspects of phosphoric acid must be thoroughly understood for the silicon nitride etch process to be truly optimized and effectively applied.

Acknowledgments

The authors would like to thank D Bouldin, E. Fisch, E. Gabriel, F. Kern, M. Lavoie, E. White and W. Zorn for their contributions to this paper.

References

1. A. W. van Gelder and V.E. Hauser, J. Electrochemical Soc., *Solid State Science*, **Vol. 114**, No. 8, pp. 869-872, August 1967.

2. B. Kirk-Othmer, *Encyclopedia of Chemical Technology*, **volume 17**, Third edition

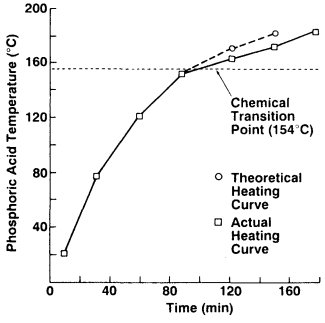


Figure 1. Phosphoric acid heating characteristics.

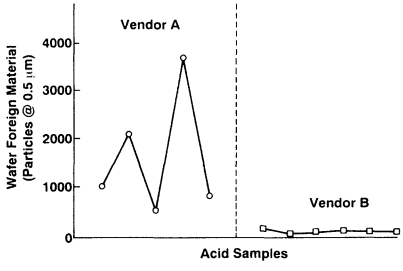


Figure 3. Comparison of phosphoric-acid vendors and corresponding wafer foreign material levels.

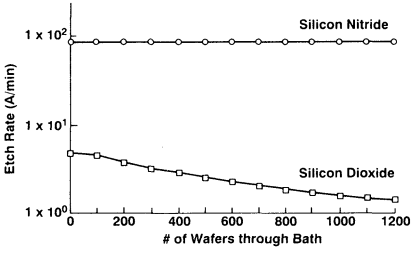


Figure 2. Silicon nitride and silicon etch rates as a function of number of wafers through the phosphoric acid bath.

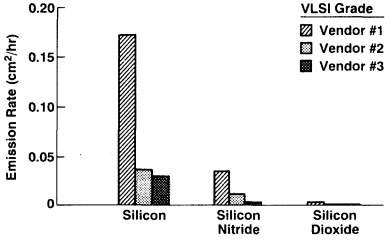


Figure 4. Comparison of alpha-particle emission rates from three wafer-surface types and acid from three different vendors

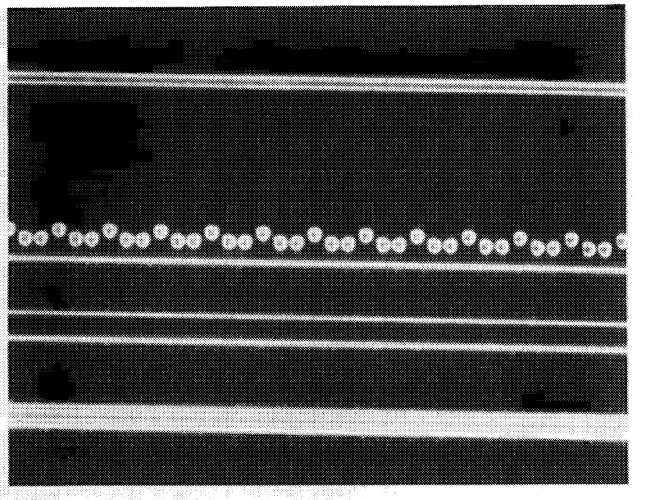


Figure 5. Optical dark-field microscopy photograph showing phosphoric acid haze.

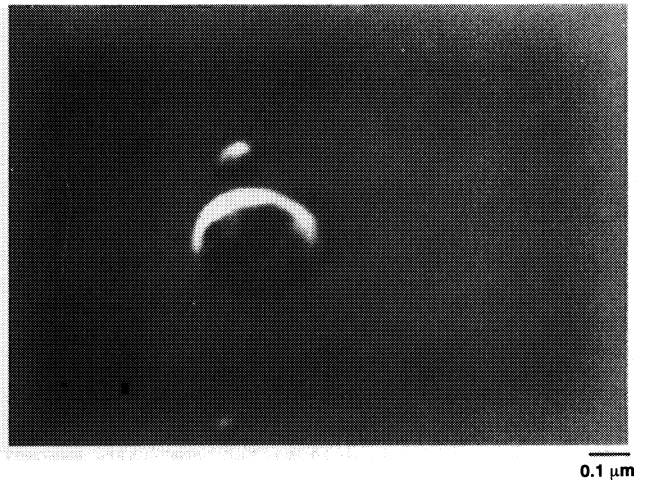


Figure 6. Gold-decorated SEM micrograph of phosphoric acid haze.

IMPACT STUDY OF THE USE OF ULSI, VLSI AND MOS GRADE CHEMICALS IN THE RCA CLEANING PROCESS ON MOS AND BIPOLAR DEVICES

F. Tardif, J.P. Joly, T. Lardin
LETI (CEA - Technologies Avancées)
MEL - CEN/G - 85 X
F38041 Grenoble Cedex

A. Tonti, P. Patruno, D. Levy
SGS / THOMSON
F38190 Crolles

W. Sievert
RIEDEL-de HAËN
D3016 Seelze-1

ABSTRACT : The use of commercial MOS, VLSI and ULSI grade chemicals in the RCA cleaning process are evaluated here in terms of minority carrier lifetimes (Bipolar or DRAM applications) and of 7 nm dry gate oxide yield (MOS application). In these tests, the generation lifetime of minority carriers measured on MOS capacitors is clearly correlated to the purity of the chemicals used during the last cleaning step before oxidation (SC2). The key element is Iron.

The results obtained on 7 nm thin dry oxide and 17 mm^2 large capacitors show that at the contamination levels reached after RCA cleaning using chemicals available from the market, defectivity is affected in the first order by the particles present before oxidation. These particles generate pin-holes. Metallic contamination levels greater than about 10^{11} to 10^{12} at/cm^2 have to be artificially reached to measurably degrade dry thin oxides (mean breakdown field drop of 1MV/cm).

INTRODUCTION

In integrated circuit manufacturing, cleaning processes play a particularly important role in the critical steps of advanced technologies and represent up to a quarter of elementary operations. If the purity of the chemicals used during these cleaning processes is considered as one of the key points which conditions the final residual contamination of silicon wafers, its real impact on actual devices is unfortunately not yet very well quantified.

As high-grade chemicals are of course expensive, the real interest of their use before critical process steps in terms of yield or reliability improvement has to be demonstrated.

The practical consequences linked with the use of commercial MOS, VLSI and ULSI grade chemicals in the RCA cleaning process are evaluated here in terms of minority carrier lifetimes (Bipolar or DRAM applications) and of 7 nm dry gate oxide yield (MOS application).The results are correlated with the more academic ones obtained by intentional contamination of silicon wafers.

EXPERIMENTAL

After a high/low/high thermal treatment, 100 mm p-doped [1.0.0] silicon wafers are etched with a 1% HF dip followed by RCA cleaning : diluted SC1 [0.25,1,5] and SC2 [1,1,5] both processed at 70°C for 10'. The baths are constituted with NH_4OH, H_2O_2 and HCl chemicals of MOS, VLSI and two ULSI grades : ULSI-1 and ULSI-2 all available on the market. In order to minimize wafer-related defects and to better simulate actual wafer processing which includes a sacrificial oxidation, a high/low/high thermal treatment under partial oxygen pressure was performed prior to any other steps. All the different cleanings are carried out sequentially in the same vessel, after intensive preconditioning. This point is particularly critical. After cleaning, the actual contamination of each bath is analyzed by ICPMS. Reference wafers are measured by TXRF and VPD-AAS for light elements (Na, Al). A particle count is performed on TENCOR 4500 equipment (particles > 0.2µm) just before a 7 nm dry thermal oxidation at 900°C.
A 420 nm thick polysilicon layer is then deposited on oxide and patterned. A final 450 °C anneal under oxygen and hydrogen is carried out to get rid of interface states.

CHEMICAL BATH CONTAMINATION

The specifications of MOS, VLSI and ULSI grades may be different from one supplier to another. Nevertheless, it is commonly assumed that metallic and alkaline contaminations should each not exceed 1 ppb for S-ULSI grade, 10 ppb for ULSI grade, 50 ppb for VLSI grade and 100 ppb for MOS grade. Generally, the concentrations actually measured are often better than specifications, in particular for the low grades. This is what can be observed in table 1 which gives the measured contamination of the SC1 and SC2 baths after wafer cleaning. Indeed, in this studied case, the MOS quality, taking the DI dilution into account, could be sold as a VLSI chemical, apart from the particulate criterion. Bath contamination as a general rule follows the expected order, especially for Iron and Zinc. (SC2 ULSI-1 does however present an anomaly for Sodium, Potassium, Magnesium and Calcium, probably due to accidental pollution of the bath).
It is interesting to note that as bulk chemicals are diluted with ultra-pure DI water , bath contaminations are lower. This represents a further advantage in using diluted SC1 or diluted HF_{last} based chemistry.

WAFER CONTAMINATION

Although alkaline treatments such as SC1 or Choline today appear to be a must to remove particles from silicon wafers by under-oxide etching, they do however deposit a large amount of chemical contaminants (see table 2). This contamination reaches an equilibrium with the bath concentration when the adsorption mechanism is predominant[1] (in the case of Iron, Zinc and to a lesser extent Copper and Nickel) or is added by hydroxide precipitation which can in a certain ratio coagulate in the form of particles.
The latter phenomenon can be demonstrated for example by observation of particle deposition on wafers processed in a Calcium-contaminated SC1 (see figure 1).

To obtain a very clean surface, it therefore seems difficult to finish off a cleaning process by an alkaline treatment even with ultra-pure or highly diluted chemicals.
The results obtained show the efficiency of SC2 acid treatment in dissolving Iron and Zinc. In these tests, the final residual metallic wafer contamination depends only on the purity of the last RCA bath : SC2.
The purities of the Hydrochloric acid and Hydrogen peroxide are therefore determinant factors for the final chemical cleanliness of wafers after RCA cleaning.
We can conclude that the different commercial purities of the chemicals available today used in the RCA cleaning process have a measurable impact on wafer surface cleanliness.

IMPACT OF RCA BATH PURITY ON MINORITY CARRIER LIFETIME (BIPOLAR AND DRAM APPLICATIONS)

Several metals such as Gold, Copper, Iron, etc. induce particularly active generation recombination centers in Silicon since their energy level is very close to that of the middle of the silicon bandgap(2) and their cross section is high.
In these tests, the generation lifetime of minority carriers measured on MOS capacitors is clearly correlated to the quality of the chemicals used for the last cleaning step before oxidation. Indeed, it can be seen in figure 2 that a clear correlation exists between the Iron concentration left on the surface after cleaning and the lifetime.
A general dependence on a larger scale has been obtained between surface Iron concentration and lifetime after intentional Iron wafer contamination in polluted SC1 as depicted in figure 3. For an Iron concentration higher than $3\ 10^{11}$ at/cm^2 the lifetime decreases with a slope of -1 in log-log scale as expected from the Shockley-Read-Hall theory where Lifetime = 1/(A x [Fe]). In this relationship, A depends on carrier thermal velocity and recombining center capture cross section(2). This result is also well known in literature(3). For a lower Iron concentration a smaller variation is obtained. It is expected to be due to parasitic phenomena such as surface generation lifetime, initial wafer purity or contaminants coming from the other processes.
The variation of lifetime with the quality of the chemicals (figure 2) and with the Iron concentration which is clearly obtained for the low Iron contamination range does not follow the same 1/(A x [Fe]) law obtained for high concentration. We have not come up with a full satisfactory interpretation for the moment.

An attempt was made to establish a correlation between lifetime and other contaminants present such as Nickel, Zinc or Copper but this was unsuccessful.
However, to act as traps, the elements must be present as point defects in silicon. Since the solubility of heavy metals is very low at room temperature(3), they must therefore be quenched in a metastable state after the last thermal treatment.
Very fast diffusing elements such as Nickel, Copper or Zinc moreover precipitate very easily and rapidly even at low temperature.
On account of the low quenching rate used in our experiment (usual cooling under laminar flow), these elements were not expected to be present as point defects. On the contrary, Iron is less mobile in Silicon and does not precipitate easily : α-$FeSi_2$ requires a large consumption of interstitial silicon which means that a large proportion can therefore be quenched as interstitial or Fe-B complexes at room temperature.

IMPACT OF RCA BATH PURITY ON THIN GATE OXIDE DEFECTIVITY (MOS APPLICATION)

The results obtained on 7 nm thin dry oxide and 17mm^2 large capacitors show that at contamination levels reached after RCA cleaning using chemicals available from the market, defectivity is first affected primarily by the particles present before oxidation. These particles generate pinholes as shown in figure 4 where all the points are averaged on each split of 10 wafers. The VLSI grade used in this experiment was particularly clean in terms of particles and gave the best results.
The linear relationship between defect rate and particle density before oxidation is usually observed in the case of very thin oxides and when the particle distribution at the wafer surface is relatively homogeneous.
The sensitivity of 7 nm dry oxide to particles counted before oxidation depends on their size and chemical nature as depicted in figure 5, and also on the kind of the cleaning process : see figure 6. This phenomenon is particularly enhanced for hydrophobic wafers when thermal ramping is performed without oxygen. For wafers with initial native oxide like those used in the tests described in figures 5 and 6, the influence of oxygen during ramping is not so critical.
The metallic contaminations observed on wafers after RCA cleaning with MOS, VLSI or ULSI grade chemicals remain too low to enable a statistical identification of any effect on breakdown distribution (see figure 7). The mean breakdown fields obtained are 10 MV/cm and 13 MV/cm respectively for 17mm^2 and 1mm^2 capacitors. (However in the evaluation performed with the ULSI-1 grade accidentally contaminated with Alkalines and Magnesium, the electrical performances of the oxide are lower. Action of the Magnesium is suspected here).
Reliability tests probably have to be performed in order to expect a measurable effect.

To highlight the action of metallic impurities in terms of thin oxide defectivity, silicon wafers have to be intentionally polluted to reach sufficient contamination levels.
Two examples are given for Calcium and Iron where the wafers are contaminated in intentionally polluted SC1 baths.
On the contrary, no defectivity effects were detected even for very large amounts of Sodium, Zinc or Copper deposited at the surface of the wafers before oxidation
The two cases of Iron and Calcium are interesting as they are representative of two possible contaminant behaviours during oxidation. Indeed, as shown by figure 8, the Iron remains at the oxide surface (and partially inside) whereas the Calcium like the copper or zinc segregates to the Si/SiO_2 interface.

This result was obtained by TXRF measurement ($\theta = 0.1°$) on a 25 nm oxide etched step by step in a 1% HF bath.
The silicon surface before 25 nm dry oxidation at 900°C was intentionally contaminated with Iron, Copper and Zinc in the 10^{12} at/cm^2 range and with Calcium in the 10^{11} at/cm^2 range.
TXRF analysis performed at different points of the wafers also reveals that segregation to the Si/SiO_2 interface occurs non-homogeneously in the contamination range studied. The values shown on curve 8 are therefore averages.
The insulator integrity loss mechanisms for these two contaminants are probably very different (a polysilicon fog is observed in the case of Iron) but they lead to the same macroscopic behaviour in terms of defectivity.

Curves 9 and 10 give the evolution of the mean breakdown fields obtained with 7 nm dry oxide for Iron and Calcium contamination. Similar results have already been obtained on 15 nm dry oxide by Verhaverbeke and al [4].
The major conclusion is that metallic contamination levels greater than about 10^{11} to 10^{12} at/cm^2 have to be reached to measurably degrade dry thin oxides (mean breakdown field drop of 1MV/cm). This conclusion was already established by Ohsawa and al[5].

CONCLUSION

The use of ultra-pure chemicals in RCA cleaning processes results in an appreciable improvement of minority carrier lifetime (Bipolar and DRAM applications). The major contaminant to be taken into account is Iron.
The critical chemicals are Hydrochloric acid and Hydrogen peroxide (SC2).

The thin oxide yields are probably mostly degraded by particles present before oxidation rather than by the low residual metallic contamination levels usually encountered after RCA cleaning. Bath particulate cleanliness is therefore a critical parameter for MOS technologies.

To measurably degrade dry tin oxidees in term of meanbreakdown field (drop of 1 MV/cm), metallic contamination has to be greater than 10^{11} to 10^{12} at/cm^2.

REFERENCES

(1) J. Ryuta and al, J. Appl. Phys., 31 (1992).

(2) S.M. Sze: Physics of Semiconductor devices, John Wiley and Son.

(3) K. Graaf, in Semiconductor Silicon/1986, PV 86-4 p 751, The Electrochemical Society Proceedings Series, Pennington, NJ (1986).

(4) S. Verhaverbeke and al, in IEDM 1991, p 71, The IEEE, Piscataway, NJ (1991).

(5) A. Ohsawa and al, in Semiconductor Silicon/1990, PV 90-7 p 601, The Electrochemical Society Proceedings Series, Pennington, NJ (1990).

ACKNOWLEDGEMENTS

The autors would like to thanks the electrical tests team at Leti for their active contribution and Riedel-de Haën analysis specialists for their decisive support.
This study was carried out within the scope of the JESSI European programmes (E2A project) and was partly presented at the SEMICON/EUROPA 93 Technical Conference, Geneva, Switzerland. This Conference was sponsored by SEMI.

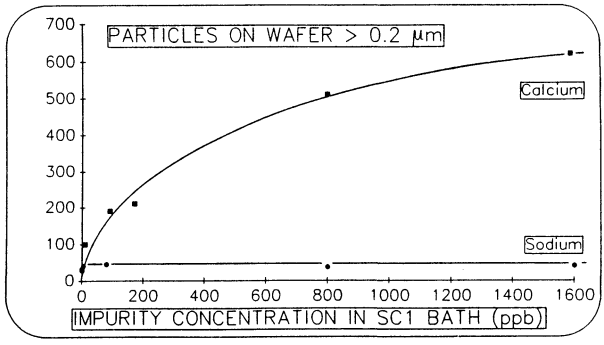


Figure 1: Calcium deposit in SC1, in particulate form

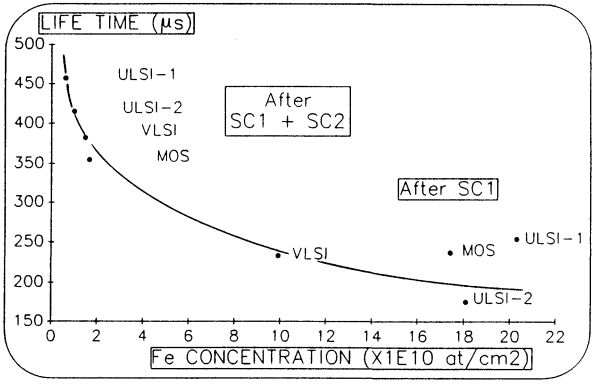


Figure 2 : Correlation between minority carriers MOS lifetime and Iron surface contamination after different RCA cleaning processes : MOS, VLSI and ULSI.

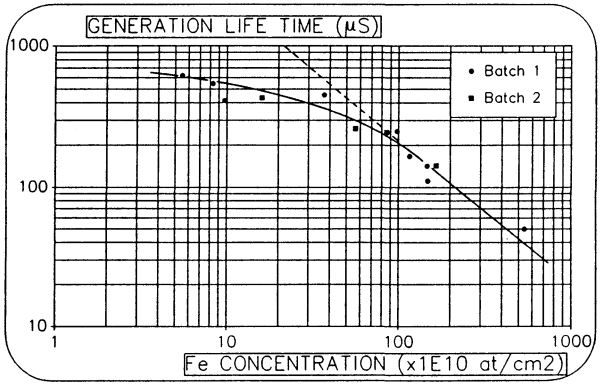


Figure 3 : Correlation between minority carriers MOS lifetime and Iron surface contamination after different SC1 baths intentionally contaminated with Iron.

	SC1				SC2			
	ULSI-1	ULSI-2	VLSI	MOS	ULSI-1	ULSI-2	VLSI	MOS
Fe	**0.4**	**0.5**	**0.6**	**1.8**	**1.3**	**4.8**	**3.8**	**6**
Ni	<0.2				<0.2			
Cu	<0.1				<0.3			
Zn	**1**	**0.4**	**0.6**	**0.7**	**1**	**1.2**	**2.8**	**3.8**
Cr	<0.2				<0.4			
Al	0.2	0.3	0.3	0.3	**0.6**	**1**	**0.6**	**2.1**
Na	1.6	2.2	2	2	330	4.2	3.2	4
K	<0.2				12	1.4	0.6	3.8
Mg	0.4	1	0.2	0.5	58	1.2	0.3	3.2
Ca	8	6	2.3	6.8	100	11	3.8	42

Table 1 : Impurities concentration of SC1 and SC2 baths (ppb)

	SC1				SC2			
	ULSI-1	ULSI-2	VLSI	MOS	ULSI-1	ULSI-2	VLSI	MOS
Fe	**20**	**18**	**10**	**17**	**0.6**	**1**	**1.4**	**1.6**
Ni	1.6	1.4	1.1	0.6	1.7	1.4	2.4	3.0
Cu	1.9	1.4	1.2	1.8	1.9	2.8	2.6	4.4
Zn	**247**	**40**	**34**	**39**	**1.6**	**1.9**	**1.2**	**2.9**
Cr	0.2	1.2	0.5	1.3	0.6	1.7	0.4	1.2
Al	34	29	16	34	1.2	3.7	3.2	2.1
Na	**0.2**	**0.6**	**0.8**	**0.2**	**6**	**0.4**	**0.1**	**0.06**
K	**1**	**2.2**	**1.3**	**3**	**2,4**	**1.3**	**0.8**	**3**
Mg	0.4	3.4	1.5	7.1	120	1.6	1.2	1.2
Ca	23	24	18	26	17	19	23	18

Table 2 : Residual surface contamination after SC1and SC1 followed by SC2 (10^{10} at/cm^2)

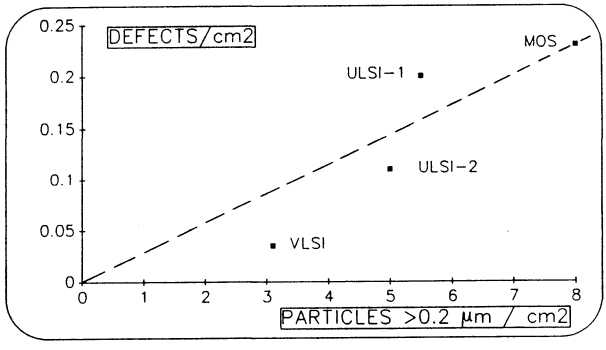


Figure 4 : Impact of particles before oxidation on pinhole generation in a 7 nm dry oxide

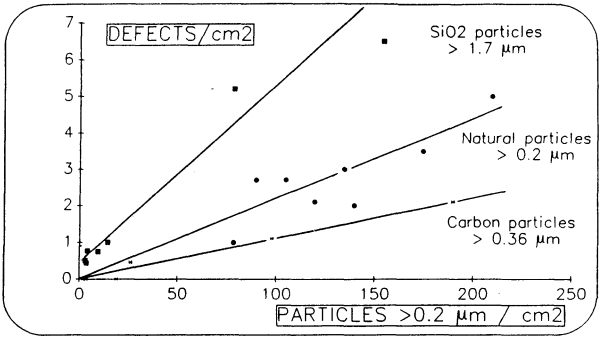


Figure 5 : Example of relationship between the nature of particles before oxidation and pinholes obtained on a 7 nm dry oxide

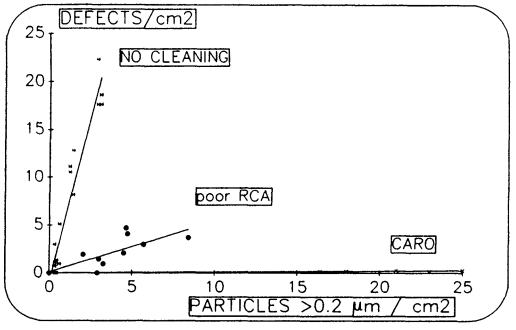


Figure 6 : Example of 7 nm dry oxide sensitivity to "natural" particles for different pre-gate cleanings

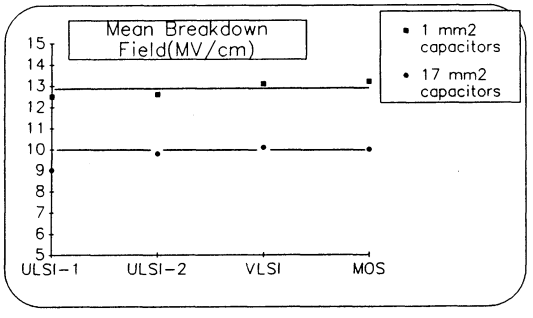


Figure 7 : Mean breakdown fields of 7 nm dry oxide obtained with the different grades of RCA cleanings

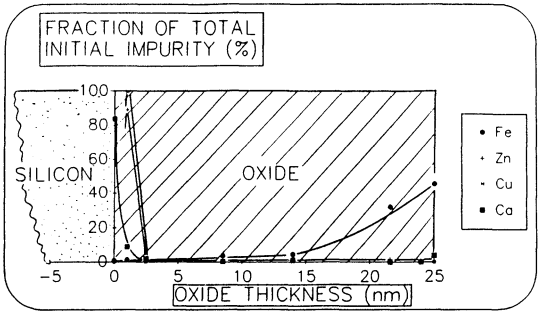


Figure 8 : Distribution of contaminants initially present at the Silicon surface after a 25 nm dry oxidation

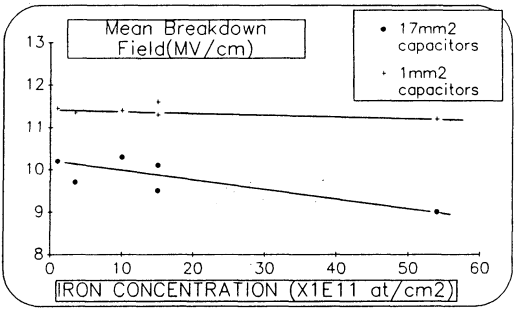


Figure 9 : Evolution of mean breakdown fields versus wafer Iron contamination present before 7 nm oxidation

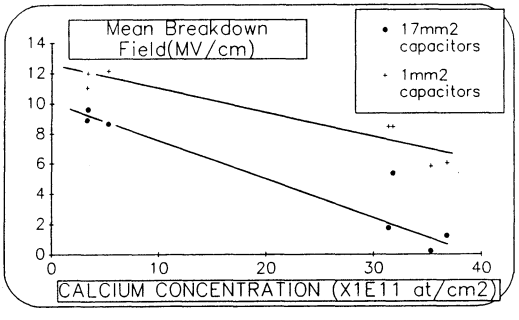


Figure 10 : Evolution of mean breakdown fields versus Calcium contamination present before 7 nm oxidation

CONTAMINATION REMOVAL BY WAFER SPIN CLEANING PROCESS WITH ADVANCED CHEMICAL DISTRIBUTION SYSTEM

N.Yonekawa , S.Yasui , F.Kunimoto and T.Ohmi
Department of Electronics, Faculty of Engineering, Tohoku University
Aza Aoba, Aramaki, Aoba-ku, Sendai, Japan, 980

Frederick W.Kern, Jr
IBM Corporation
General Technology Division in ESSEX Junction, Vermont, USA

In this report we studied the metallic impurities removal and the organic impurities removal during spin cleaning. We show the use of Ozonized Ultra Pure Water for the removal of organic impurities. From the simulation tests, we optimized rotation speeds and cleaning time. The simulation test result were confirmed by Fourier transform infrared spectroscopy (FT-IR). The experimental results demonstrate that the spinning method is more effective in removing organic impurities and metallic impurities from the wafer surface than the immersion type of cleaning in batch mode. The cleaning time could be greatly reduced. This is because the reaction is accelerated by chemical mixing and reaction products formed by the cleaning reaction are removed immediately by the constant flow of chemicals induced by the centrifugal force of Spin Cleaning System.

INTRODUCTION

In the semiconductor manufacturing field, We have claimed that the simultaneous fulfillment of the following three principles is essential to establish high performance processes that assure both perfect uniformity and perfect reproducibility. These three principles are: 1) ULTRA CLEAN PROCESSING ENVIRONMENT, 2) ULTRA CLEAN WAFER SURFACE, 3) PERFECT-PROCESS PARAMETER CONTROL. The importance of these three principles have been demonstrated by various experimental data.(1) It has been shown that when a wafer is exposed to cleanroom air, a native oxide layer grows. Cleanroom air is nothing more than dustless air and contains oxygen and water, along with other impurity gas molecules. Therefore, wafers should never be exposed to air in the advanced manufacturing process, and this is why the closed manufacturing is essential.(2) We propose here a closed manufacturing scheme in which wafers are processed in a nitrogen gas sealed wet station. The clean nitrogen gas seal processing has been proven to be very effective at performing high quality processes. The establishment of the ultra clean wafer surface requires the complete elimination of the following six contaminant sources; 1) Particles, 2) Organic Contaminants, 3) Metallic Impurities, 4) Native Oxide, 5) Molecules adsorbed on the surface, 6) Surface Microroughness

However, the conventional batch treatment method will not meet the requirement of high-precision process control essential for ULSI manufacturing primarily due to cross-contamination in the batch process.

The variation in chemical composition occurring in the batch process also limits its performance. Furthermore, the increase in consumption of chemicals due to the increase in wafer diameter is also an important issue. In an attempt to solve the problems of the conventional batch cleaning method, we have developed a system which fully controls process parameters which we will report here. In this system, we introduced single wafer cleaning process which does not allow cross-contamination to occur or composition to change, and it also performs very accurate and uniform etching. Furthermore, we have found that we can reduce both cleaning time and the chemical consumption by using the new high-precision Spin Cleaning System.

In this report we studied the metallic impurities removal and the organic impurities removal during spin cleaning. From the simulation tests, we discovered the correct rotation speeds and cleaning time. The simulation test result was confirmed by Fourier transform infrared spectroscopy (FT-IR). The experimental results demonstrate that the spinning method is more effective in removing organic impurities and metallic impurities from the wafer surface than the batch method. The cleaning time was greatly reduced. This is because the reaction is accelerated by chemical mixing and reaction products formed by the cleaning reaction are removed immediately by the constant flow of chemicals induced by the centrifugal force of Spin Clean System.(3)

SYSTEM DESCRIPTION

We employed a newly-developed chemical delivery system to uniformly distribute chemicals, ozonized ultra pure water and ultra pure water immediately after they are filtrated. As shown in Figure 1, filtrated chemicals are introduced into funnels placed at an elevated position. When the diaphragm valve is opened the chemicals are gravitationally delivered due to the height difference between the funnel and nozzle. This system makes it possible to perform the circulation filtration without affecting the volume of delivered chemicals. In this way if the tank gets contaminated, it is possible to continue the chemical delivery because the tank can be cleaned while delivering only newly-filtrated chemicals. The air-driven pumps employed in this system can withstand high temperature. The filters in this system have an absolute rating down to 0.05 micron. Bubbles generated during the circulation filtration are automatically removed by the tank/funnel arrangement. Figure 2, shows the ozonized ultra pure water line. Ultra pure water line is diverged from the main line introduce into the ozonizer. Generated ozone is injected into ultrapure water, which is returned to the main line. All these lines are made of PFA. We cleaned these lines to remove the organic and the metallic impurities by SPM solution. Ever afterwards, we were flowing ultra pure water into the tubes. The cleanliness was confirmed by an ozone concentration meter. Figure 3, shows the structure of the wafer spinner. The maximum wafer size that this spinner can handle is 6-inch. Since the wafers are rotated at a high speed during the chemical cleaning, a special chuck is mounted on the spinner to making use of centrifugal force

with increasing rotation speed.(Figure 4) Nitrogen gas is continuously introduced into the cleaning chamber to prevent air contamination from the environment. Chemicals are introduced onto the center of wafers from a nozzle having a uniform end. The chuck, cleaning chamber, and the nozzle arm feature a self-cleaning function which allow them to be cleaned with chemicals or ultra pure water at any time.

NITROGEN GAS SEAL PROCESS

In the case of the conventional wet station which are exposed to the cleanroom air, even if the particulates are completely removed, there are still a lot of impurity atoms and/or molecules. If the wafer surface is exposed to air this causes the formation of a native oxide, resulting in device characteristics degradation. In Figure 5, the native oxide thickness on n, n^+, and p^+ substrate surfaces is plotted as a function of the air-exposure time, where the clean room air is maintained at 23°C and RH (relative humidity) at 42%. Native oxide thickness was measured by XPS. It should be noted that the native oxide grows in the air in a layer-by-layer manner, and the native oxide growth on the highly doped n^+ region is very fast compared to that on the n or p^+ region. It is quite interesting to note that no native oxide grows in moisture-free air which was created by mixing ultra clean oxygen and nitrogen at a volume ratio of 1 : 4 .
The coexistence of oxygen and moisture is essential for native oxide growth. Figure 6, shows native oxide growth in UPW with three concentrations of dissolved oxygen 9, 0.6, and 0.04 ppm. The thickness of native oxide increases with time and with increasing dissolved oxygen concentration. The surface roughness of a wafer decreases with the growth of native oxide. The initial native oxide growth on the n^+ surface is faster than that on the n surface, but saturates at a thickness of 10 Å.
A decrease in dissolved oxygen concentration slows the native oxide growth in pure water, again demonstrating that the coexistence of oxygen and water is essential for native oxide growth. So, we must decrease oxygen or water. If possible, we have to decrease both parameters. Therefore, in our tests, dissolved oxygen concentration has been less than 1 ppb and an wet chamber isolated from the atmosphere was used. The existence of native oxide has been shown to degrade high-quality film growth, highly selective reactive etching, and highly selective film deposition such as silicon, germanium, and aluminum deposition.

One of the easiest ways and the most economical way to realize a closed manufacturing scheme, is to perform all wafer processing in a clean nitrogen ambient. Since the native oxide grows only under the coexistence of oxygen and moisture, native oxide-free processing is possible only in a closed manufacturing system in which wafers go through all fabrication processes completely isolated from the ambient air.

Our tests needed to decrease both parameters. Therefore, we controlled that dissolved oxygen concentration has been less than 1 ppb and that we have an isolated wet chamber from the atmosphere. Figure 7 shows FT-IR data of wafer surface after spin cleaning. Native oxide grows very slow. Figure 8, shows the XPS spectrum of a n^+ silicon surface which shows that the native oxide is not formed on an n^+ surface wafer. In this spinning cleaning test the n^+ surface wafer is spin cleaned with $HF-H_2O_2$

solution (HF:0.5%, H_2O_2:10%), the flow rate is 300ml/min and the rotation speed is 200 rpm for 2min to remove the native oxide, followed by rinsing with ultra clean water for 5 min by the spinning method in a nitrogen gas sealed process.

IMPURITIES REMOVAL WITH SPIN CLEANING METHOD

1. Removal of metallic impurities

Two mechanisms are considered to explain the metallic impurity segregation on the Si surface. The first mechanism is the direct precipitation as a result of the charge exchange between metallic ions and Si atoms or hydrogen atoms terminating the Si surface. The second mechanism is the precipitation caused when the metal oxides formed from the metallic impurities are included in the oxide film as it grows on the Si surface. The metallic impurities included in the SiO_2 film can be removed as the SiO_2 film is etched in a diluted HF solution. However, the noble metallic impurities binding directly with the bare Si surface, such as Cu, can not be removed easily. Usual, these metallic impurities need to be ionized by the $HCl-H_2O_2-H_2O$ cleaning in the cleaning process to be removed. It is also possible to remove them to some extent by etching the Si substrate in the $NH_4OH-H_2O_2-H_2O$ cleaning. However in either method, the solution needs to be heated to around 90°C.

The dilute $HF-H_2O_2$ cleaning has recently been proposed as a method to remove metallic contamination on the Si surface at room temperature(4). It is considered that, in this method, H_2O_2 induces the formation of oxide film on the Si surface while the oxide film is then etched with HF. Eventually the metallic impurities adhering on the surface are removed by slightly etching the Si substrate.

To test this cleaning method similar to the actual service operation, the following experiment was performed. The 5-inch wafers were immersed in a 0.5% HF solution for 1 minute to remove the native oxide, followed by rinsing with ultra clean water for 10-minutes. Then the wafers were immersed into pure water, with Cu of 0.1ppm added, for 10-minutes and then they were rinsed in ultrapure water for 10-minutes. After going through the above treatments, the entire surface of the wafers was contaminated with Cu at a level of 10^{13} - 10^{14} atoms/cm^2. These contaminated wafers were then treated with a dilute $HF-H_2O_2$ solution (HF:0.5%, H_2O_2:10%) to remove Cu on the silicon wafer surface by different methods, the spinning method and the dipping method. The Cu removal efficiency of each treatment was evaluated with Total Reflection X-ray Fluorescence Spectroscopy (TRXRF). As shown in Figure 9, the dilute $HF-H_2O_2$ solution was found effective in removing Cu from bare silicon surface. It was also observed that the spinning method required shorter time than the dipping method to completely remove Cu from the silicon wafer surface. This means that, compared with the conventional dipping method, the spinning method can save both cleaning time and chemical consumption.

2. Removal of organic impurities

The removal of organic impurities can be performed in two ways. One method is the conventional SPM cleaning. The mechanism is the oxidation of organic impurities

and native oxide growth on the Si wafer surface. Native oxide and decomposed organic impurities are separated from the surface by a following diluted HF solution. But the SPM solution contains sulfuric acid which is environment contaminating. Therefore, we have used high concentration ozonized ultra pure water. The removal mechanism is the same as in the SPM solution. The decomposed organic impurities included in the SiO_2 film and adhered on the wafer surface can be removed as the SiO_2 film is etched in the DHF solution. However, some organic impurities can not be removed easily from surface in the immersion cleaning method.

The Spin cleaning method has two important additional features for removal, one is the supply of fresh ozonized ultra pure water, the second is the centrifugal force. Organic impurities are removed immediately , after decomposition.

To test this cleaning method similar to the actual operation, the following experiment was performed. The sample wafers were immersed in 0.5% HF solution for 1 minute to remove the native oxide, followed by rinsing with ultra pure water for 10-minutes. Then the wafers were immersed into surfactant solution of 0.001mol/l, for 10-minutes and then they were dried by ultra pure N_2 gas. We used surfactant which is n-Octylamine Hydrochloride ($CH_3(CH_2)_7NH_2HCl$). After going through the above treatments, wafers were contaminated with surfactant. Figure 10, shows the FT-IR spectrum of the contaminated and the cleaned wafers. The contaminated wafers were treated with 10ppm ozonized ultra pure water, followed by rinsing with ultra pure water. Then the samples were treated with a 0.5% dilute HF solution and rinsed to remove the reaction products and the native oxide on the surface. In these experiments the rotation speed was used as a variable. We can see the organic contamination removal efficiency for each rotation speed. The Removal efficiency is increasing with rotation speed. And so, 3000 rpm and 1500 rpm can remove the organic contaminants in 5 minutes. 3000r.p.m. can remove the impurities in just only 3 minutes.

In Figure 11, the FT-IR spectrum of the Si surface by each treatment is shown when performed in immersion mode. The Ozonized ultra pure water and the SPM solution can decompose the organic impurities, but are not able to completely remove them. This figure demonstrates Hydrogen termination peaks after each treatment. However, besides the Hydrogen peaks also hydrocarbon peaks can be observed. Therefore, the O_3 dipping and SPM solution performed in immersion mode do not achieve the complete removal. On the other hand, the spin cleaning can remove organic contamination from the Si surface.

CONCLUSION

It has been found that the spinning method is more effective than the batch (dipping) method for removal of various impurities from the wafer surface, metal impurities such as Cu, organic impurities and native oxide. Since the fresh chemicals are constantly supplied to the wafer surface, the reaction remains uniform, which enables the wet processing to be conducted in a predetermined and controlled manner.

We have developed the chemical delivery system, ozonized ultra pure water injection system and the spinner system to secure a high cleanliness level. The

following results have been obtained in the simulation test with pure water, the spinning metal cleaning test and the spinning organic cleaning test ;

1.The spinning system improves the cleaning performance : the spinning method requires shorter time and smaller chemical volume to completely remove the Cu and organic impurities. Moreover, it does not need high temperature and the system enables continuous processing.

2.The atmosphere has to be kept clean : comparison of the Nitrogen sealed system with the batch method proved that pure environment is of utmost importance.

3.We believe that advanced wet cleaning process must be made in a dynamic mode in a single chamber. Because conventional batch cleaning limits the cleaning performance. Those limits are contamination from the environment and transit from chamber to chamber.

4.Combination of Ozone and the spinning method is very effective and environment friendly.

ACKNOWLEDGMENTS

The research reported in this article was conduced in the Mini Super Clean Room at the Faculty of Engineering and in the Laboratory for Microelectronics attached to the Electric Communication Laboratory in Tohoku University.

The authors would like to express their sincere thanks to Nisso Engineering Co., Ltd. and M.T.C Japan Co., Ltd. for supplying "Advanced Chemical Distribution System" and "Advanced Spinner System" respectively.

REFERENCES

1. T.Ohmi, BREAK THROUGH FOR SCIENTIFIC SEMICONDUCTOR MANUFACTURING IN 2001, p.36,Realize INC, Japan (1992).
2. M.Morita, T.Ohmi, E.Hasegawa, M.Kawakami, and M.Ohwada, "Growth of silicon surface," J.Appl.Phys., Vol.68, No.3, pp.1272-1281 (1990).
3. F.Kunimoto, F.W.Kern and T.Ohmi, "Characterization of Wafer Spin Cleaning Process with Advance Chemical Distribution System", Proceeding of IES 38th Annual Technical Meeting, May (1992)
4. T.Shimono and M.Tsuji "A New Cleaning Solution for Metallic Impurities on the Silicon Wafer Surface" Extended Abstracts of Electrochem. Soc., Spring Meeting , Vol.91-1, pp.278-279, Washington DC, May 5-10 (1991

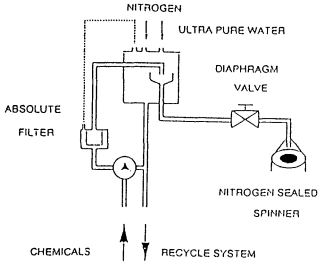


Figure 1 Advanced Chemical Distribution System

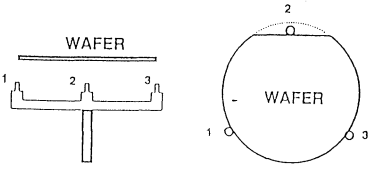


Figure 4 Teflon Chuck for Wafer

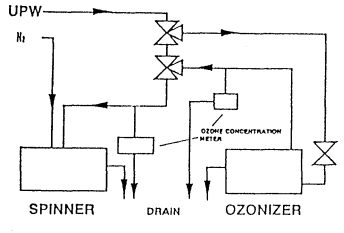


Figure 2 Ozonized Ultra Pure Water Line

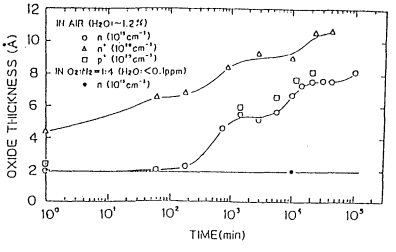


Figure 5 Thickness of native oxide grown in the airat room temperature as a function of time

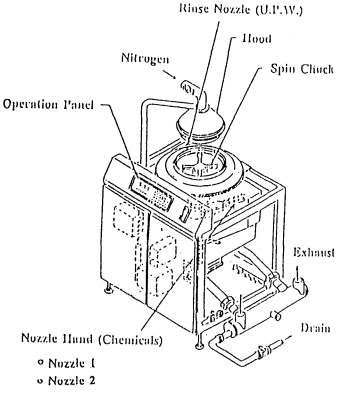


Figure 3 Nitrogen Gas Sealed – Advanced Spinner System

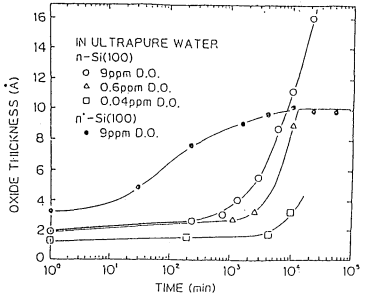


Figure 6 Native Oxide growth in ultra pure water under various dissolved oxygen concentration

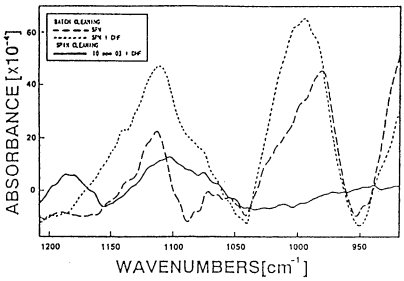


Figure 7 Native Oxide growth by spin cleaning and batch cleaning

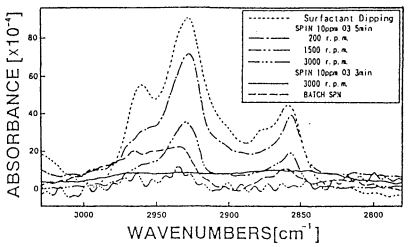


Figure 10 Comparison of adhering of organic impurities on each treatments

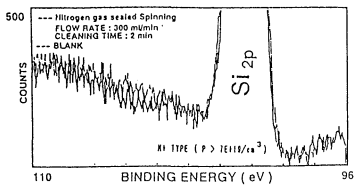


Figure 8 XPS spectrum of n^+ silicon wafer surface after cleaned with HF-H_2O_2 solution (HF:0.5%, H_2O_2:10%) by spin method in nitrogen gas sealed process.

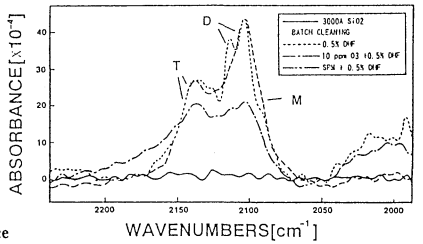


Figure 11 Hydrogen Termination on contaminated

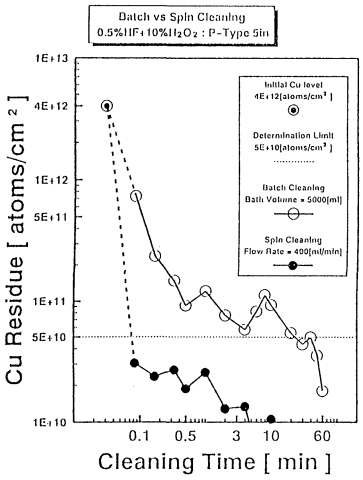


Figure 9 The cleaning time dependence on Cu removal efficiency with the spinning method and the batch method

SILICON SURFACE ROUGHENING BY THE DECOMPOSITION OF HYDROGEN PEROXIDE

H.F. Schmidt, M. Meuris, P.W. Mertens, S. Verhaverbeke, M.M. Heyns,
IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, E.C.

L. Hellemans, J. Snauwaert,
Lab. Chem. Biolog. Dynamics, KUL, Celestijnenlaan 200D, B-3001 Heverlee, Belgium, E.C.

K. Dillenbeck
Ashland Chemical Inc., P.O. Box 2219, Columbus, Ohio 43216, U.S.A.
presently at Pacific Scientific, Hiac/Royco division, 11801 Tech Road, Silver Spring, Maryland, U.S.A.

Abstract

The decomposition of H_2O_2 is a well known problem for the stability and therefore the suitability of H_2O_2 based cleaning solutions in the semiconductor industry. It was found, that this decomposition plays an important role especially for the NH_4OH - H_2O_2 mixture, which is known as the SC1 step in the RCA cleaning procedure. This paper will describe recent progress in correlating H_2O_2 decomposition to microroughening of silicon surfaces and will provide some information on the nature and the mechanism of this roughening effect. Also a direct correlation between Gate Oxide Integrity (GOI) and surface roughening by the decomposition of H_2O_2 will be shown.

INTRODUCTION

Metal contamination, particles and silicon surface roughness are important causes for defect related gate-oxide breakdown in MOS technology. It was found that a major part of these impurities and defects are introduced to the wafer surface during the wet pre-gate cleaning steps, due to the use of an unsuitable quality of chemicals [1]. Certain trace metal impurities in standard wet cleaning solutions were identified to have detrimental impact on gate oxide integrity in two ways: first directly through contaminating the silicon surface [2,3] and second indirectly through degradation of the chemical mixture [4,5]. The SC1 step in the RCA cleaning procedure [4], where a $NH_4OH/H_2O_2/H_2O$ mixture is applied to the silicon wafer surface, could be identified to be one of the most critical ones, because of its slight etching of silicon to remove particles and because of its low solubility of metal impurities. The low solubility of the metal impurities results in the above mentioned surface contamination through precipitation and inclusion into the SiO_2 film, while the slight etching of silicon can

result in an increase in surface roughness. It was found that silicon surface roughening depends on the mixing ratio of $NH_4OH/H_2O_2/H_2O$ [6,7]. NH_4OH, in particular the OH^-, acts as a catalyst for the dissolution of SiO_2 [8], and has the chemical attribute to etch silicon. Because this etching has a strong anisotropic character and forms (111) facets on the (100) surface, it is necessary, that the oxidation is done by a slightly faster concurrent reaction to achieve a homogeneous removal of Si. This is the role of H_2O_2 in the SC1 mixture, which acts in this way as an inhibitor of the etching of silicon.

Recently it was found that the decomposition of H_2O_2, where gaseous oxygen becomes liberated, has a strong impact on the roughening of silicon wafer surfaces in the SC1 cleaning bath [9].

DECOMPOSITION OF HYDROGEN PEROXIDE

The overall decomposition reaction of H_2O_2 is given by the equation

$$2H_2O_2 \rightleftharpoons 2H_2O + O_2 \,. \tag{1}$$

To investigate decomposition rates in real time, a gasometric technique has been used to measure the amount of O_2, generated through the decomposition of H_2O_2 as a function of time. In this way the decomposed mol H_2O_2 per unit time can be determined and normalised to the residual mol H_2O_2 in the solution. The decomposition rate is defined accordingly as a fraction of H_2O_2 decomposed per unit time. A special tool has been constructed to avoid errors from the evaporation of water and ammonia. The accuracy of temperature control was ± 1 °C.

It was found, that the decomposition rate of H_2O_2 in a SC1 solution initially increases and reaches a constant value after a certain time (Fig. 1). The time t=0 is defined as the time, when the components of the test solution are mixed together and between t=0 and t=15 min, the sample is heated up to 70 °C. Because of the time dependence of the H_2O_2 decomposition in a SC1 solution, all measurements were carried out until a constant decomposition rate was achieved. H_2O_2 (30 w-% ± 2) with different impurity levels were used for the experiments, two without a stabiliser ($<$ 1ppb and $<$ 10ppb grades) and one with stabiliser ($<$ 100ppb grade), while the NH_4OH quality was always of the same high purity ($<$ 1ppb for all metals). For selectively spiking of H_2O_2 with Fe and Cu, Fe(III)-nitrate and Cu(II)-nitrate AAS standards were used.

Fe and Cu are two of the most investigated catalysts for the decomposition of H_2O_2 [10]. In Fig. 2 it is shown that already low ppb levels of Fe and Cu are influencing the decomposition rate of an ultra pure H_2O_2. The impact of metal impurities, which originate mainly from the applied H_2O_2 becomes also obvious from Fig. 3, where the decomposition rates of different grades of H_2O_2 are plotted versus the SC1 mixing ratio. A very strong initial dependence of the decomposition rate on the NH_4OH concentration was found, especially in the case of the low grade H_2O_2. Because it

contains a very effective stabiliser, the decomposition rate without adding NH_4OH is comparable to the ultra pure one. When NH_4OH is added, the stabiliser becomes inactive and the decomposition rate increases by around three orders of magnitude.

The decomposition of hydrogen peroxide is extremely sensitive to catalysis, both homogeneous and heterogeneous. In a basic solution, especially an NH_4OH environment, a very active colloidal form of $Fe(OH)_3$ is mentioned to be involved into the catalysis [10]. In the case of Cu its tetrammine complex is believed to be mainly responsible for the high activity as H_2O_2 decomposition catalyst [11]. This can explain why H_2O_2 decomposes so much faster in a SC1 mixture. This can also be an explanation why the decomposition rate in the beginning is time dependent. The chemical environment for the catalytic active species changes when H_2O_2 is mixed with NH_4OH. By coming from a weak acid environment (H_2O_2) with high oxidising potential into a basic environment, where the oxidising potential of H_2O_2 is reduced [12], the impurities are changing their chemical status. On the other hand, the so-called base catalysed decomposition of H_2O_2 is proposed to take place in a basic environment [10]:

$$2H_2O_2 + HO_2^- \rightleftharpoons H_2O + OH^- + O_2. \qquad (2)$$

The next figure (Fig. 4) shows the temperature dependence of the decomposition rate of H_2O_2 in two different, so called modified SC1 solutions. Both mixtures give the same particle removal efficiency when applied to silicon wafers for 10 minutes, but the more or less small variation in temperature results in a significant change in the decomposition rate, because of the Arrhenius type behaviour of the H_2O_2 decomposition [13]. Therefore, to increase the stability of the SC1 bath, it is necessary to lower the temperature. The resulting decrease in the particle removal efficiency can be compensated by increasing the NH_4OH concentration or the cleaning time [14].

ROUGHENING OF THE SILICON SURFACE

Silicon surface roughness, generated by the decomposition of H_2O_2 in a SC1 mixture shows up in form of small Light Point Defects (LPDs) in sensitive light scattering maps (Censor ANS100). In most cases, this kind of roughening is identifiable through typical patterns in which the LPDs are arranged. Also the size of the LPDs, mainly in the range of 0.1 to 0.3 μm LSE (Latex Sphere Equivalents), is characteristic. In Fig. 5 three examples are shown. Entire area damage on the surface can occur if the silicon wafer is exposed to that region of a strong decomposing cleaning bath, where assembly of the O_2 bubbles occurs (Fig. 5a). Nucleation centres of O_2 bubbles in front or beneath the wafer surface can cause patterns shown in Fig. 5b and Fig. 5c. In the second case, (c), decomposition occurred at the contaminated backside of the front wafer (Cu contamination from a vacuum tweezers). Fig. 6a shows another typical pattern, which arises from the decomposition of H_2O_2 at a metal contaminated part

of the PFA carrier. All these wafers had initially a hydrophobic surface before they were immersed into SC1 mixtures of different quality.

The result of AFM (Atomic Force Microscopy) investigations on the damaged part of the wafer (square, marked with an arrow) is represented in Fig. 6b. This plot shows significant spikes, which were measured to be around 2nm in height and can not be found on the "good" part of the wafer (square without an arrow). By applying SEM (Scanning Electron Microscopy) on wafers with similar patterns, also spikes of a diameter between 0.1 and 0.3 μm can be observed. The impact of this decomposition roughening on GOI was investigated by testing the electrical breakdown of thin SiO_2 capacitors, which were produced on wafers with such typical patterns. A comparison between the light scattering map (Fig. 7a) and the E_{bd} (Electrical breakdown) wafer mapping of the test wafers, results in a direct correlation between LPDs and Low Field breakdown (Fig. 7b).

To investigate the effect of the surface pre-treatment of a silicon wafer on roughening through H_2O_2 decomposition, an experiment was carried out using an ultra pure SC1 mixture (0.25/1/5) which was selectively spiked to 1 w-ppb Fe. All wafers (p- and n- type, 125mm) got initially a full clean (Piranha + RCA) in a spray tool. A part of the wafers got a supplementary HF-dip before they were immersed into the SC1 solution to obtain hydrophobic surfaces. Then two PFA carriers, each containing hydrophobic and hydrophilic wafers were immersed one after each other into the same Fe spiked SC1 cleaning bath at 70 °C for 10 minutes. After the SC1 step, the wafers were rinsed in DI water and dried in a spin drier. The surface quality of the wafers were then evaluated using sensitive light scattering. As it can be seen from Fig. 8, the surface roughness increases with the age of the bath only on wafer surfaces which were hydrophobic and not on wafers which were covered with a chemical oxide (hydrophilic) before they were immersed into the Fe spiked SC1 solution. Hydrophobic wafer surfaces are critical, because O_2 bubbles, which are present in the mixture will adhere on the bare silicon. While these bubbles are sticking on the surface, the silicon beneath is shielded against the etching action of the SC1 mixture. The surrounding silicon surface will be etched. In general the shielding effect is determined by the growth rate and shape of the bubble and also by the parameters influencing its adhesion to the silicon surface. It has been reported [15], that the detachment diameter of O_2 bubbles decreases with increasing hydrophilic character of a heterogeneous catalyst surface for H_2O_2 decomposition. Because silicon itself does not act as a catalyst for the decomposition of H_2O_2, the bubbles, which are sticking on the surface are not growing and therefore they are not reaching the so-called detachment diameter. The bubbles will stay on the surface until the end of the cleaning. An additional indication for this mechanism is the height of around 2nm of the spikes. This correlates with the etch depth of silicon in the used SC1 mixture [14].

The Fe concentration on the wafers, measured with TXRF (Total X-ray Reflection Fluorescence) after the 1 w-ppb Fe spiked SC1 treatment was typically 10^{12}

at./cm^2 [16]. All other elements were below detection limit (around 10^{10} at./cm^2) except Zn, which reached some 10^{10} at./cm^2. Applying an additional SC2 cleaning ($HCl/H_2O_2/H_2O$) on wafers which are showing decomposition roughening patterns, reduces all metal levels to below 10^{10} at./cm^2 but does not change the picture of roughness.

CONCLUSIONS

A direct correlation between the decomposition of H_2O_2 in a SC1 mixture and roughening of hydrophobic silicon surfaces was found. Through atomic force and scanning electron microscopy it could be shown, that this roughness is caused by spikes. The formation of these spikes seems to occur through micro masking effects. O_2 bubbles, which are formed during the decomposition of H_2O_2 and which adhere very easily to hydrophobic surfaces shield the bare silicon beneath against the slow etching action of the SC1 mixture in the surrounding. It was also found, that this kind of roughness has a direct impact on gate oxide integrity and causes low field breakdown of thin gate oxide capacitors. This experiments and observations made in other studies [3, 7, 9, 17], allow to conclude, that the pre-treatment of wafers before SC1 and the SC1 quality itself is much more important than the post-treatment by SC2. Metals are removed by the SC2 but indirectly they have already contributed to surface damage.

ACKNOWLEDGEMENT

The technical assistance of K. Kenis and S. Geboers is greatly acknowledged.

References

[1] M. Meuris, M. Heyns, W. Küper, S. Verhaverbeke and A. Philipossian, presented at the Electrochem. Soc. Spring Meeting, Washington D.C., 5-10 May 1991, published in the proceedings.

[2] S. Verhaverbeke, M. Meuris, P.W. Mertens, M.M. Heyns, A. Philipossian, D. Gräf and A. Schnegg, Technical Digest of the International Electron Devices Meeting, Washington, D.C., Dec. 8-11, 1991, p. 3.6.1.

[3] P.W. Mertens, M. Meuris, H.F. Schmidt, S. Verhaverbeke, M.M. Heyns, D. Gräf, A. Schnegg, M. Kubota, K. Dillenbeck and A. Philiposian, 39th Annual Technical Meeting of the Institute of Environmental Sciences, Las Vegas, Nevada, May 2-7, 1993, pp. 231-237.

[4] W. Kern and D.A. Poutinen, RCA Rev. 31, pp. 187-206 (1970)

[5] Y. Oshida, in Chemical Proceedings of the 1992 Semiconductor Pure Water and Chemicals Conference, Editor M.K. Balazs, pp. 63-82 (1992).

[6] T. Ohmi, M. Miyashita, M. Itano, T. Imaoka, and I. Kawanabe, IEEE Trans. Electron Devices, Vol. 39, No./ 3, pp. 537-545, March (1992).

[7] M. Meuris, S. Verhaverbeke, P.W. Mertens, M.M. Heyns, L. Hellemans, Y. Bruynseraede and A. Philipossian, Jpn. J. Appl. Phys. Vol. 31 (1992) pp. L 1514-L 1517, Part2, No. 11A (1992).

[8] R.K. Iler, The Chemistry of Silica, John Wiley and Sons, (1979) p. 4.

[9] H.F. Schmidt, M. Meuris, P.W. Mertens, S. Verhaverbeke, M.M. Heyns, M. Kubota, and K. Dillenbeck, 39^{th} Annual Technical Meeting of the Institute of Environmental Sciences, Las Vegas, Nevada, May 2-7, 1993, pp. 238-244.
Remark: The decomposition rates in this reference are wrongly defined as fraction per unit time. The graph values are in percent per unit time.

[10] D.F. Evans and M.W. Upton, J. Chem. Soc. Dalton Trans. 1985, 2525-2529.

[11] H. Weisz, S. Pantel and W. Meiners, Analytica Chimica Acta, 82 (1976), 145-153.

[12] G. Vierke, Z. Naturforsch. 29b, 135-136, 1974.

[13] J.E.A.M. van den Meerakker and M.H.M. van der Straaten, J. Electrochem. Soc., Vol. 137, No.4, 1990, pp. 1239-1243.

[14] M.Meuris, S. Verhaverbeke, P.W. Mertens, H.F. Schmidt, M.M. Heyns, M. Kubota, A. Philipossian, K. Dillenbeck, D. Gräf, A. Schnegg and R. de Blank, Microelectronic Engineering 22 (1993) 21-28, Elsevier.

[15] I.I. Vasilenko, Russian Journal of Physical Chemistry, 55 (2), 1981, 269. Translation from Zhurnal Fizicheskoi Khimii, 55 (1981), 487-488.

[16] H.F. Schmidt, P.W. Mertens, M. Meuris, S. Verhaverbeke, M.M. Meuris and K. Dillenbeck, *First International Symposium on Ultra Clean Processing of Silicon Surfaces*, Sept. 17-19 1992, Leuven, Belgium.

[17] H.F. Schmidt, M. Meuris, P.W. Mertens, S. Verhaverbeke, M.M. Heyns, and K. Dillenbeck, Microcontamination 11-9 (1993) p.27-32.
Remark: The decomposition rates in this reference are wrongly defined as fraction per unit time. The graph values are in percent per unit time.

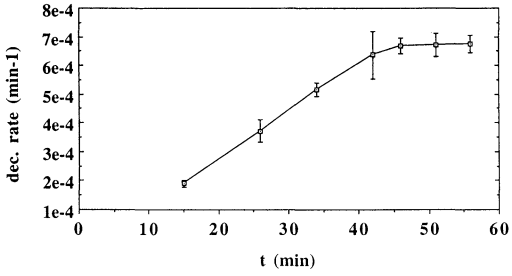


Figure 1: Decomposition rate of a SC1 mixture versus age of the solution (0.25/1/5 at 70 °C, metal levels: < 0.5ppb in total SC1).

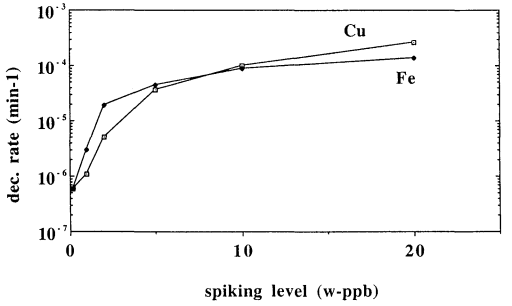


Figure 2: Dependence of the decomposition rate of an ultra pure H_2O_2 on the Fe and Cu contamination level at 70 °C (all other metals: < 0.4ppb).

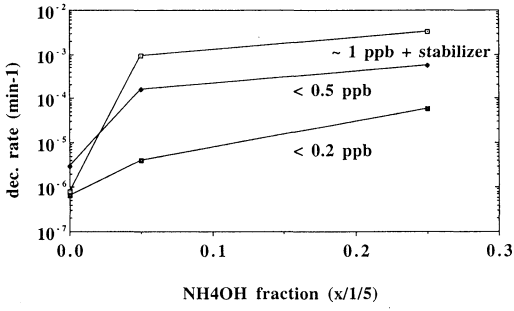


Figure 3: Decomposition rate of three different grades of H_2O_2 as a function of the $NH_4OH/H_2O_2/H_2O$ ratio at 70 °C (metal concentrations in total SC1).

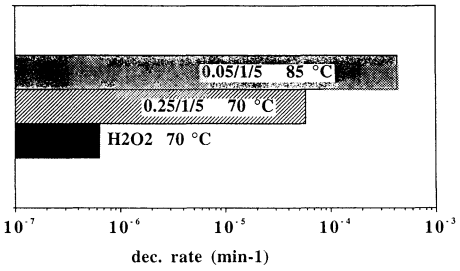


Figure 4: Decomposition rates of ultra pure SC1 mixtures: 0.05/1/5 at 85 °C and 0.25/1/5 at 70 °C compared to the ultra pure H_2O_2 itself (metal levels: < 0.2ppb in total SC1 and < 0.4ppb in H_2O_2).

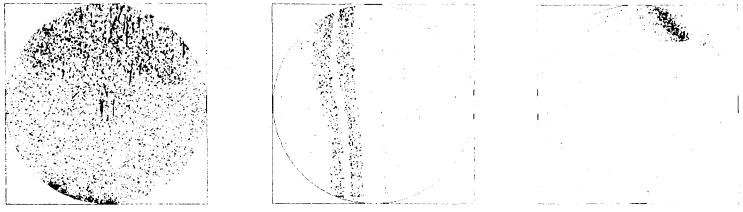


Figure 5: Typical LPD patterns (LSE: 0.14 - 0.24 μm, offzone 5mm):
a) after treatment in a low grade SC1 mixture (metal levels: $\sim$ 1ppb),
b) after treatment in an ultra clean SC1 mixture (metal levels: < 0.2ppb),
H_2O_2 decomposition occured at two bubble sources in front of the wafer surface,
c) like b) but decomposition occured at the contaminated backside of the front wafer.

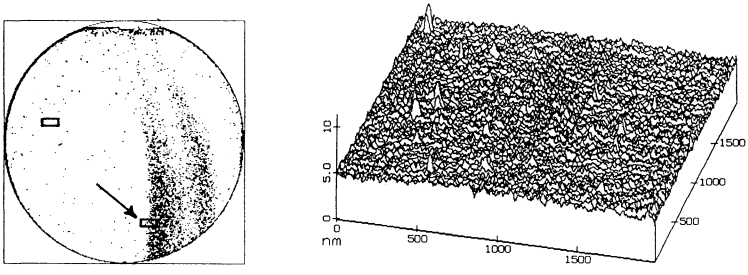


Figure 6: Decomposition-LPDs and their atomic nature: a) Light point defects (LSE: 0.15 - 0.30 μm, offzone 0mm) after treatment in an ultra clean SC1 solution (metal levels: < 0.2ppb); typical patterns when decomposition of H_2O_2 occurs at the PFA carrier, b) AFM plot from the roughened area of this wafer (arrow).

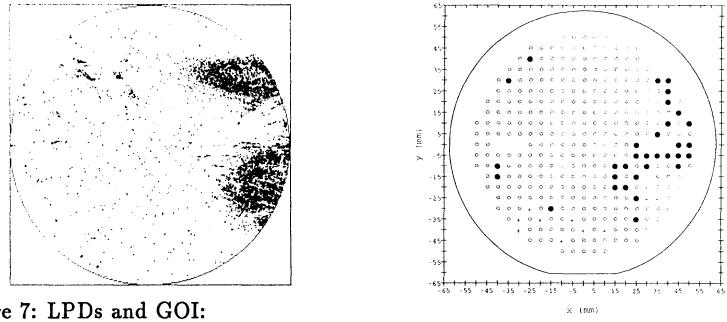


Figure 7: LPDs and GOI:
a) Light point defects (LSE: 0.11 - 0.14 μm, offzone 5mm) after treatment in an ultra clean SC1 solution (metal levels: < 0.2ppb); typical patterns from decomposition of H_2O_2 at the bottom of the cleaning bath,
b) E_{bd} wafer mapping, 15nm gate oxide, cap.area=15.8 mm^2, black dots symbolise low field breakdown ($\leq$ 2MV/cm).

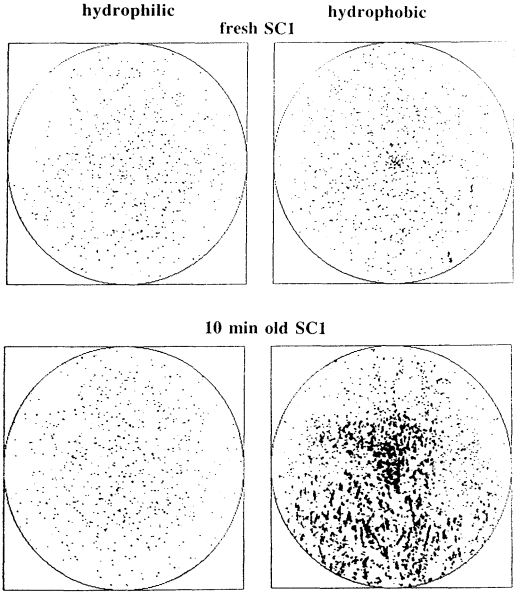


Figure 8: Light point defects (LSE: 0.10 - 0.19 μm offzone 5mm) after treatment in a 1 w-ppb Fe spiked SC1 solution (0.25/1/5 at 70 °C). The different wafers were taken out from 2 consecutively cleaned batches.

COMPARISON OF POST ASH CLEANING PROCESSES

Sylvia D. Hossain and Michael F. Pas
Texas Instruments,
0.5μm Productization
M/S 385
13353 Floyd Road
Dallas, TX 75243

ABSTRACT

SC1 ($NH_4OH:H_2O_2:H_2O$) is evaluated at 50°C, 60°C, and 80°C as one step in several sequences for post ash silicon wafer cleaning. The ratio of SC1 used is 1:2:10 for this work. A comparison is made of various wet cleaning sequences using defect density analysis, minority carrier lifetime (MCLT), and surface contamination analysis. Results indicate that the defect density using 60°C and 80°C SC1 for post ash cleaning is less than 0.25 def/cm^2. These results are an order of magnitude lower than those obtained using ozonated piranha. The MCLT values for SC1 alone are possibly low due to Zn contamination in the H_2O_2 as shown by Total Reflection X-ray Fluorescence. However, the MCLT recovers if followed by an HF step. The data shows that using heated SC1 followed by HF is an excellent choice for pre oxidation cleaning combined with a post ash process.

INTRODUCTION

Cleaning and particulate removal of silicon surfaces following ion implantation and/or plasma etch processes can be difficult. For Dynamic Random Access Memory (DRAM), the cleaning efficiency, from the point of view of both defects and of surface contamination, is critical. Defects, such as particles, immediately before gate oxidation growth may cause pin holes in the gate oxide, early oxide breakdown, reduced gate oxide integrity, etc. Surface contamination by metallics may cause degradation of gate oxide properties such as lower oxide capacitance and increased interface trap density as well as a reduction in minority carrier lifetime. Particles present on the silicon wafer surface before film deposition (such as silicon nitride, polysilicon, etc.) will result in higher particles in and under the film through decoration of the particulate,

thereby causing pattern and etch defects.

Resist which has been ion implanted can be much more difficult to remove than un-implanted resist. The difficulty of removal depends on the type of ion implanted, the ion implantation dose, and the energy and the beam current. An ashing process is almost always required in such cases before any cleaning using a wet process can be attempted.

An ashing process is used to oxidize organic surface residue or films such as photoresist. An oxygen plasma is generated and the surface of the substrate is exposed to the plasma. The organics volatilize in the chamber.

Plasma etching is used as a dry etching process. Certain gases are used to obtain selective or non-selective etching of surface films or the substrate itself. During the plasma etching process, a certain amount of contamination is generated by the simultaneous etching of particles and residue both in the chamber and on the substrate. The gases used may also generate defects on the wafer.

The combination of resist coating, ion implantation or plasma etching, and ashing is one of the more difficult wet cleaning processes due to the increased 'hardness' of the resist from ion bombardment during the implant and defects generated by the plasma etch process.

As a comparison to ion implantation with ash, results are also reported on work done using plasma etching and ashing of un-implanted resist. The plasma etch which is chosen is an SiO_2 etch and one which has been found to have a potential particulate problem in the past. In this case, using un-implanted resist, the resist coating, plasma etching, and resist ashing are the primary source of particles.

In a previous publication [3], the authors have reported on particulate removal efficiency of the heated SC1 solution. In this report, a more thorough study of particulate removal using different wet process sequences is done. This data is also combined with minority carrier lifetime and TRXRF data to provide an overall result of post ash wet cleaning of both implanted and un-implanted silicon wafers.

After processing test wafers through the post ash cleaning sequence, some wafers also continue processing through a typical pre diffusion wet cleaning sequence. Continuation of these wafers through a pre diffusion wet cleaning simulates normal wafer processing in the production

environment. Production wafers receive a post ash wet clean before continuing through a more stringent wet clean if the process to follow is a diffusion process such as thermal oxidation, annealing, or film deposition.

EXPERIMENTAL PROCEDURE

P-type, <100>, 1.6-1.9 ohm-cm, 150 mm silicon wafers are used for all studies, including particulate tests and TRXRF analysis. The starting defect density for silicon wafers is less than 0.09 defects/cm^2. For particulate removal studies, Si wafers are coated with 1.0-2.0 μm of resist. In the case of ion implanted wafers, particle counts reported are the total final particle counts over the wafer surface. The delta defect density from pre to post process is not reported because the combination of ion implantation and ashing causes very large numbers of defects on the surface. Using the ESTEK WIS-8500, these defects, due to the large quantity present, are reported as 'haze' and it is difficult to assign a true number to them. In the case of etch and ash only, there is no such issue and the delta values between pre and post wet process are reported.

Arsenic, boron, and phosphorus are ion implanted into bare silicon coated with photoresist. The arsenic and boron implant parameters for this work use high dose and high energy. The implanters used are high current implanters. Arsenic is implanted at a dose of 3.0E15 ions/cm^2 at 120 keV, phosphorus at a dose of 4.0E14 ions/cm^2 at 50 keV and boron at 2.0E15 ions/cm^2 at 20 keV. The resist is baked at 120°C for 60 min. before ion implantation.

For Minority Carrier Lifetime (MCLT) measurements, a thermal silcon dioxide of 150Å is grown on bare Si P<100> wafers. Silicon wafers used are high resistivity (8 to 12 ohm-cm). The oxidation process includes 6% HCl (standard gate oxidation conditions) flowing in the furnace during oxidation. MCLT evaluation is done using a Leo Giken Wafer Tau measurement tool.

A fresh bath of SC1 solution is mixed for each test. The control process is room temperature SC1 with megasonic (SC1 RT) -> 0.49% HF -> IPA VD. This process is referred to as 'HF*'. SC15 refers to SC1 at 50°C, SC16 to SC1 at 60°C, and SC18 to SC1 at 80°C. For SC15, SC16, and SC18, the process sequence is heated SC1 and spin dry. This sequence is then followed by an HF dip and dry using an IPA vapor dryer, where required. The 'HF -> IPA V/D' process will be referred to as 'HF'. The spin dry procedure prior to the HF clean is due to equipment limitations. 'O3P' refers to ozonated piranha in an autohood with two sequential

sulfuric acid tanks. The solution is heated to 130°C ± 10°C and ozone gas is bubbled through the solution to form piranha. The room temperature SC1 process is done in a manual stand-alone hood which is also commercially available. The megasonic transducers are located in the bottom of the process tank and are fixed in place. In this particular equipment setup, the wafers, which are placed in teflon cassettes, are automatically moved over the fixed transducers. The drying technique is an SRD for all processes other than 'HF' or 'HF*'. The sequences tested are listed below in Table I.

For pre diffusion cleaning processes such 'HF*' or 'HF', the equipment used is an autohood with recirculation and filtration for each chemical tank. All material transfer between load and unload is done by robotic transfer. An IPA V/D is used for drying wafers.

Table I. Process sequences used in this study.

PROCESS	DESCRIPTION
HF*	{SC1->H_2O->HF->H_2O->IPA V/D}
HF	{HF->H_2O->IPA V/D}
O3P	{PIRANHA->PIRANHA->H_2O->S/D}
O3P-HF*	O3P => HF*
SC15	{SC15->H_2O->S/D}
SC16	{SC16->H_2O->S/D}
SC18	{SC18->H_2O->S/D}
O3P-SC15	O3P => SC15
O3P-SC16	O3P => SC16
O3P-SC18	O3P => SC18
O3P-SC15-HF	O3P => SC15 => HF
O3P-SC16-HF	O3P => SC16 => HF
O3P-SC18-HF	O3P => SC18 => HF

The inspection tool used is an ESTEK WIS-8500. The WIS-8500 is used to detect particles on unpatterned Si wafers. The edge exclusion is 8 mm on the wafer. Defects of size 0.2μm and larger are detectable using this tool.

MCLT results are obtained using high resistivity (8 to 12 ohm-cm) wafers especially procured for this test. All oxidation is done using a horizontal furnace with 6% HCl (standard gate oxidation conditions) flowing during the oxidation process. The targetted oxide film thickness is 150 Å.

RESULTS. Defect Density Evaluation

The SC1 solution is heated to 50°C, 60°C, and 80°C. A new batch of chemicals is mixed for each test. The temperature range is set to ± 2°C for each of the temperatures tested. The solution is allowed to come to equilibrium for a minimum of 2 minutes.

In order to obtain optimum characterization and results, an autohood with recirculation and filtration for each chemical tank and with IPA V/D is an absolute necessity for optimum particle evaluation. The type of rinse is also important, whether heated or not, or quick dump spray, or overflow. The manual, bottle filled hood with spin dryer routinely results in particles added of an average defect density of 0.21 defects/cm^2. The autohood with robotic transfer and IPA V/D has a average defect density of 0.01 defects/cm^2. The defect size being measured is greater than or equal to 0.2μm in each case.

As mentioned previously, two types of samples are processed. One group of wafers is resist coated, ion implanted, and ashed. The other group is resist coated, plasma etched, and ashed. Figure 1 below shows the process flow for the test procedure.

Figure 2 shows the defect density for ion implanted wafers. It is important to note that defect density values reported here for the ion implanted wafers are the post wet process values. The delta in values between pre and post wet process are not valid due to the present of 'haze' as detected by the ESTEK WIS-8500.

Figure 2 contains data for O3/P, O3/P-HF*, O3/P-SC1 and O3/P-SC1-HF*. The 1-step process sequence of O3/P only results in the highest final remaining defect density as seen in the figures shown. For ion implanted wafers, the O3/P process also shows the presence of 'haze' as detected by the WIS-8500 and due, in this case, to defects too numerous to count. These defects are then categorized as 'haze'. Note as the temperature of the SC1 increases so does its defect removal efficiency. Regardless of the process which follows the O3/P, it results in a defect reduction.

Defect densities are much lower overall for these samples which are plasma etched and ashed than for the ion implanted samples. Figure 3 compares data for O3/P versus heated SC1. As for ion implanted samples, O3/P shows the highest defect density for the sequences investigated here.

Results. Chemical analysis

The average of the data is reported where applicable. The standard deviation of the data is also reported on the figures and can be seen by the smaller squares inset into the bar graph.

Chemical analysis of the Si surface is performed using Total Reflection x-Ray Fluorescence (TRXRF). The instrument used is a Rigaku 3726 TXRF system. The angle of incidence is a few minutes of arc such that there is total reflection from the sample. The elements capable of being detected by this system are Na to U. Some elements such as Al are more difficult to detect due to the limits of mass resolution. The spot size for detection is about 1 cm in diameter. The detection limits for the system and parameters used on the samples for which results are reported are listed below.

Table III. Detection Limits (atoms/cm^2) for TRXRF Analysis

ELEMENT	DETECTION LIMIT
Ni	3.50E+10
Fe	5.00E+10
Zn	5.00E+10

TRXRF analysis is completed on samples which have been processed through resist coat, ion implant or etch, ash, and wet processes. Figure 4 compares TXRF data for implanted versus un-implanted (or plasma etched) samples for several wet processes. Different wet process sequences are analyzed in each figure. It is important to note that the values reported are the average of 5 data points. Values below the detection limit for each element are set to the detection limit value.

Figure 4 compares the two types of samples using the O3/P and O3P+heated SC1 processes. 'I2' refers to ion implanted samples and 'Etch' refers to plasma etched only samples. There does not seem to be a significant difference due to

either the ion implant or plasma etch processes for metal contamination. Both types of samples show similar levels of Ni, Fe, or Zn. Differences which are noticeable seem more to be due to the wet processes themselves.

Results. Electrical Evaluation

To evaluate the possible impact of cross contamination and effective surface cleaning of ion implant, plasma etch, and O_2 ash processes, MCLT wafers are processed through the pre diffusion clean along with samples which have been resist coated, ion implanted or etched, and ashed. Due to the sensitive nature of the MCLT analysis, it is difficult to process the MCLT wafers themselves through processes such as ion implantation or plasma etching and still obtain minority carrier lifetime values which are sensitive to possibly small differences. MCLT also is affected by surface damage. In this case, ion implantation may confuse the issue of contamination with that of surface damage. The various process parameters are listed below.

The 'HF*' process in this case refers to room temperature megasonic SC1 (SC1 RT) - HF (75 seconds) - IPA V/D.

Table II. Evaluation of SC1 process for MCLT evaluation

PROCESS	HF TIME	SC1 TEMP	SC1 TIME
'HF*'	75 sec	NONE	NONE
O3P	75 sec	NONE	NONE
SC15	NONE	50°C	15 min
SC16	NONE	60°C	15 min
SC18	NONE	80°C	15 min
O3P->SC15	NONE	50°C	15 min
O3P->SC16	NONE	60°C	15 min
O3P->SC18	NONE	80°C	15 min

PROCESS	HF TIME	SC1 TEMP	SC1 TIME
'HF*'	75 sec	NONE	NONE
O3P->HF*	75 sec	NONE	NONE
SC15->'HF'	75 sec	40 C	15 min
SC16->'HF'	75 sec	50 C	15 min
SC18->'HF'	75 sec	60 C	15 min
SC15->'HF'	75 sec	60 C	15 min
SC16->'HF'	75 sec	80 C	15 min
SC18->'HF'	75 sec	80 C	15 min

A total of 9 points per wafer are taken. The data reported below is the average of all points from at least 2 wafers. MCLT depends quite heavily on the exact furnace, type of furnace, and oxidation conditions used. Trends provide information in this case where quantitative data is sensitive to many other parameters.

Figure 5 presents MCLT trends and includes all post ash cleaning sequences investigated. The process 'HF*' is used as a benchmark in this case. As can be seen from Figure 5, SC1 last processing at temperatures higher than room temperature show a much degraded MCLT value as compared to O3/P. It is important to note that if SC1 last processing is followed by an HF last step before gate oxidation, the MCLT trend recovers to values as high as those for O3/P or 'HF*'.

It appears that while heated SC1 last processing may degrade MCLT values, if the heated SC1 process is followed by an HF last step, MCLT recovers to optimum levels. Considering the results of the TXRF analysis, it may be that the presence of Zn detected on heated SC1 last processed wafers aids in degrading MCLT. The data has shown that heated SC1 is more efficient than the standard ozonated piranha process in removing defects. Because MCLT data shows that metallic impurities are removed by an HF last process following the heated SC1 process, the contamination resulting from the heated SC1 process should not be an issue. For these reasons, it is recommended that heated SC1 be used only for the purpose of reducing defect densities. Heated SC1 should be followed by another

sequence such as HF last for gate oxidation cleaning.

CONCLUSIONS

The heated SC1 solution heated to 50°C, 60°C, and 80°C is characterized using physical, chemical, and electrical criteria. Impurity analysis completed using the TRXRF analytical technique provides quantitative data on metallic impurity levels for heated SC1, heated SC1 + 'HF', and 'HF*' processes and correlates these results with MCLT. The data shows some reduction in metallic levels for SC1 + 'HF' processes.

The degradation in MCLT from SC1 last processing to either O3/P or 'HF*' last processing has not yet been completely explained. The investigation is ongoing using various analytical tools to understand the results obtained. Ongoing investigation includes the use of Time of Flight Secondary Ion Mass Spectroscopy (TOF-SIMS) to study further the possible effects of lighter mass metallic contamination and of organic contamination.

ACKNOWLEDGEMENTS

The authors would like to acknowledge valuable help by Dr. Leigh-Ann Files-Sesler of Central Research Laboratories at Texas Instruments for TRXRF analysis.

REFERENCES

[1] W. Kern, "The Evolution of Silicon Wafer Cleaning Technology", J. Electrochem. Soc., **137** (6), 1887-1892, (1990).

[2] T. Ohmi and T. Shibata, "Scientific ULSI Manufacturing in the 21st Century", The Electrochem. Soc., INTERFACE, **1**(1), Winter, 1992, pp. 32-37.

[3] S.D. Hossain and M.F. Pas, "Heated SC1 Solution for Selective Etching and Resist Particulate Removal", submitted, J. Electrochem. Soc., July, 1993.

[4] W. Kern, "Purifying Si and SiO2 Surfaces with Hydrogen Peroxide", Semiconductor International, (1984).

[5] N. Yabumoto, K. Saito, M. Morita, and T. Ohmi, "The Role of Hydrogen, Oxygen and Water in Oxidation of Hydrogen Terminated Silicon Surface", Extended Abs. of the 22nd Conf. on Solid State Devices and Mat., 1067-1070, Sendai (1990).

[6] C.Y Wong and S.P. Klepner, "X-ray Photoelectron Spectroscopy on Surface Oxidation of Silicon by Some Cleaning Procedures", Appl. Phys. Lett., **48** (18), 1229-1230, (1986).

[7] G. Gould and E.A. Irene, "The Influence of Silicon Surface Cleaning Procedures on Silicon Oxidation", J. Electrochem. Soc., 134, 1031 (1987).

[8] P.O. Hahn, M. Grundner, A. Schnegg, and H. Jacob, "The Si-SiO2 Interface Roughness: Causes and Effects", Phys. and Chem. SiO2 and Si-SiO2 Interface, Ed. C.R. Helms and B.E. Deal, Plenum Pub. Corp. (1988).

[9] T. Shimono and M. Tsuji, "A New Cleaning Solution for Metallic Impurities on the Silicon Wafer Surface", Electrochem. Soc. Spring Meeting, Wash., D.C., May 1991, Ext. Abstr. **91-1**, pp. 278-279.

[10] M. Miyashita, M. Itano, T. Imaoka, I. Kawanabe, and T. Ohmi, "Optimizing NH4OH/H2O2 Cleaning Process for Ultra-Clean Wafer Surface Preparation, Electrochem. Soc. Spring Meeting, Wash., D.C., May 1991, Ext. Abstr. **91-1**, pp. 709-710.

[11] S. Verhaverbeke, H.F. Schmidt, M. Meuris, P.W. Mertens, and M.M. Heyns, "HF-last Cleaning Cycles for Gate

Oxides", Tech. Conf., SEMICON/Europe '93, March 30-April 1, Geneva, Switzerland.

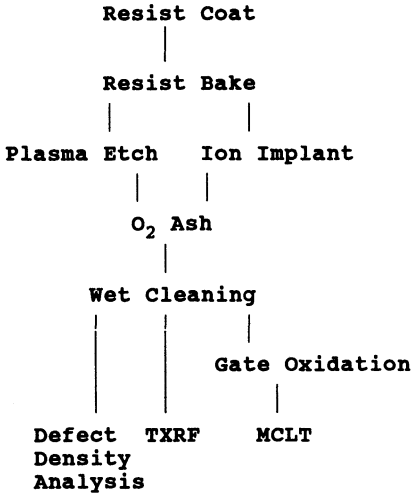


Figure 1. The test wafer process flow

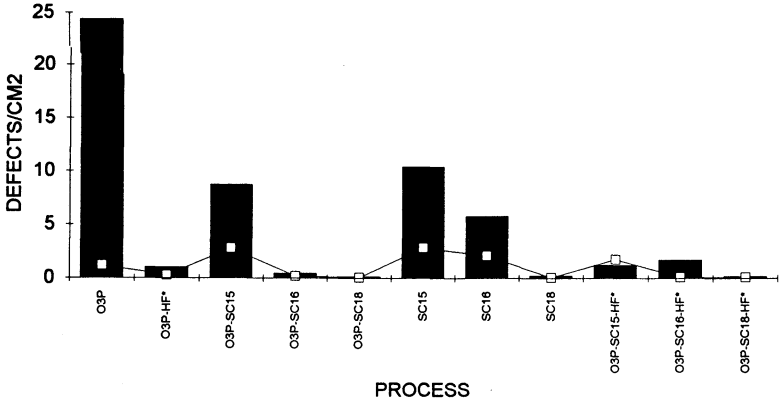


Figure 2. Defect density analysis of wet process sequences evaluated for ion implanted samples

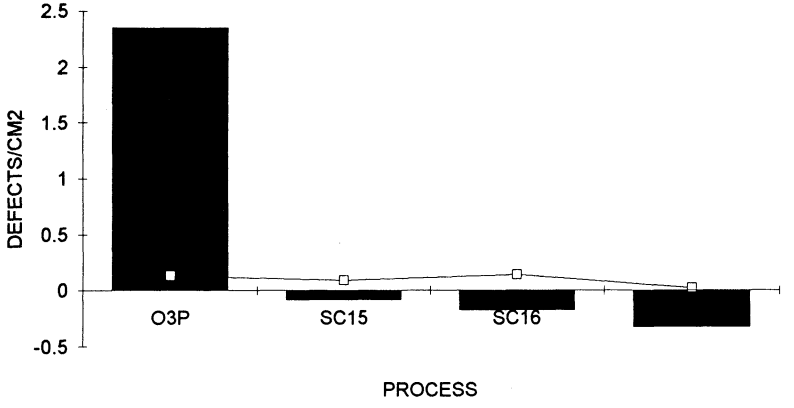


Figure 3. Defect density analysis of O3P versus heated SC1 processes for plasma etched samples

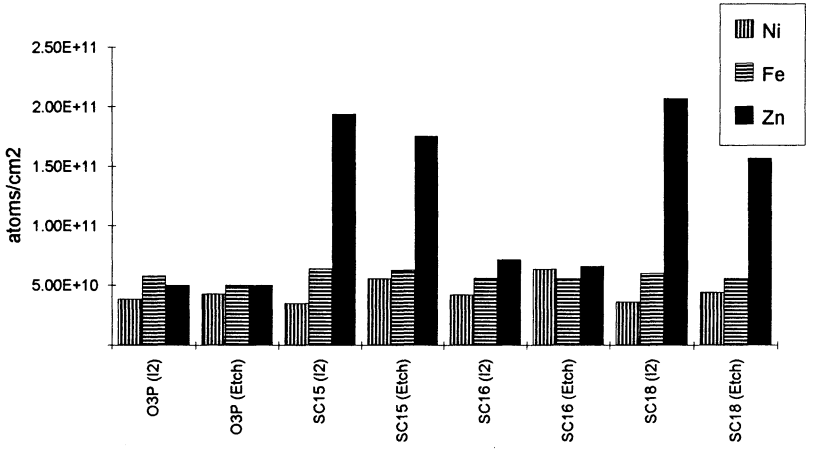


Figure 4. Surface contamination analysis using TRXRF for O3P versus heated SC1 processes

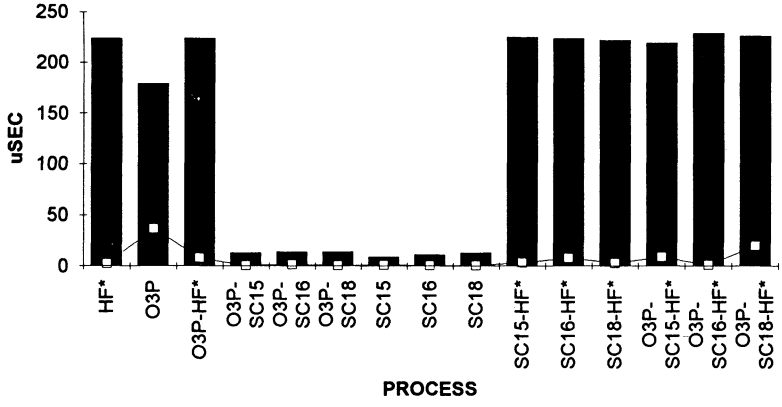


Figure 5. MCLT analysis for the cleaning processes contained in Table I

THE EFFECT OF DISSOLVED OXYGEN AND DISSOLVED OZONE IN ULTRAPURE WATER ON N^+ DOPED POLYCRYSTALLINE SILICON TO N^+ DOPED CRYSTALLINE SILICON CONTACT RESISTANCE

Michael J. Satterfield, Brian Anthony, Gary Huffman, and Fred Walczyk
Advanced Products Research and Development Laboratory
Motorola, Inc., Austin, TX 78721

ABSTRACT

The effect of dissolved oxygen and dissolved ozone has been studied on integrated N^+ doped polycrystalline to N^+ doped crystalline silicon contact resistance devices. Dissolved ozone in concentrations of 15 ppb or higher has been shown to sharply increase the contact resistance of this structure. Dissolved oxygen in concentrations as high as 3 ppm has been shown to have no statistical effect on the contact resistance of this structure.

INTRODUCTION

Fast Static Random Access Memory (FSRAM) lots utilizing self-aligned[1] bit cell contacts were being routinely run to exercise the process integration and make appropriate changes to the processes in order to develop a robust transferable process to a high volume manufacturing fab. It was found that most of the lots that were processed showed excessively high and variable arsenic implanted and diffused N^+ polysilicon to arsenic implanted N^+ monocrystalline silicon contact resistance. Figure 1 shows the self-aligned N^+ polysilicon to N^+ silicon contact. Analysis of the data led to the observation that the pre-clean, which utilized low level ozonated water ($\approx 40 \pm 5$ppb dissolved ozone) as the final rinse, prior to poly deposition, was causing the unacceptable contact resistance. Wafers pre-cleaned prior to polysilicon deposition using a special vapor HF process showed extremely low values for the contact resistance as compared to the conventional wet process[2]. In addition to the problems caused by the pre-clean, problems associated with rapid thermal annealing were also present such that furnace annealing was being utilized. Furnace annealing accentuated the contact resistance problem when the fully ozonated water process was used. Rapid thermal annealing showed much better contact resistance data even when the ozonated water was used at the poly pre-clean. Transmission Electron Microscopy (TEM) analyses of the interface showed that a thin oxide was formed on the monocrystalline N+ silicon when low level ozonated water was used. No discernible difference in oxide was present when unozonated water was used. This thin oxide acts as a diffusion barrier to arsenic. This explains why furnace annealing accentuates the problem and why RTA processed wafers gave much better contact resistance even with low level ozonated water. Rapid Thermal Annealing (RTA) will break up the oxide interface and arsenic can also diffuse through a thin oxide with the help of RTA.

The recent technical literature suggested that the excessive dissolved oxygen in the ultrapure water could be causing the high contact resistance due to native oxide growth studies.[3-6] More experiments were devised that split a contact resistance lot (fully integrated contact process) through water that had extremely low dissolved oxygen (no ozonation) and water that was ozonated at a low level. In addition, the rinse times were varied to see if this had a negative effect on contact resistance. The graphs in Figures 2 and 3 show dramatic differences between wafers rinsed in water containing approximately 20ppb dissolved oxygen and those rinsed in ozonated water containing 3500 ppb dissolved oxygen. Further, the longer rinses in ozonated water gave increased values of contact resistance. It was obvious from this data that the low level ozonated water process used was unacceptable for the polysilicon to N^+ contact process.

From the above experiment, it was not known if the cause of the high contact resistance was due to excessive dissolved oxygen in the water or to the low level of ozone in the water. Several more integrated short flow contact resistance experiments were devised that examined dissolved oxygen and ozone separately. When water is ozonated, low levels of ozone are present and extremely high levels of oxygen are present due to the inefficient conversion of oxygen to ozone through a corona discharge ozonation system. Therefore, dissolved oxygen in ultrapure water can either exist by itself or in conjunction with low level ozone.

PROCEDURE AND RESULTS

Low level ozonation of ultrapure water was accomplished by converting gaseous oxygen in to ozone through a corona discharge cell. The ozone is then pressurized above the pressure of the ultrapure water and injected into the ultrapure water stream as it flows into wet process tool. Figure 4 shows the schematic for the ozone injection apparatus.

One fully integrated contact resistance device experiment was split four ways at the polysilicon deposition pre-clean . The four splits consisted of a final rinse in water containing 20, 100, 550, or 3000ppb dissolved oxygen with NO ozone following the normal dilute HF pre-clean. Pure oxygen was bubbled into the water stream in the same manner that ozone is injected into the water as was depicted in Figure 4. A ball type flowmeter was utilized to control the amount of oxygen entering the water in order to keep the dissolved oxygen level constant for each of the four splits. Dissolved oxygen measurements were taken with a calibrated dissolved oxygen probe that sampled ultrapure water past the point of injection. The data in Figure 5 shows the contact resistances from these four splits are not statistically different via a students t-test at an alpha risk of 0.05. Therefore, dissolved oxygen levels as high as 3500ppb (3.5ppm) have no effect on the contact resistance of this integrated process. The second fully integrated contact resistance experiment was also split four ways at polysilicon deposition pre-clean by simply varying the electric current on the ozone generator's cell such that no ozone was present in the water (oxygen injection with I=0) for one split, followed by splits of 15, 30 and 45ppb dissolved ozone. The data in Figure 6 shows that the contact resistance increases an order of magnitude for rinse water containing as little as 15ppb dissolved ozone! The 30 and 45ppb splits showed similar contact resistances while the no ozone split showed very good contact resistance. All of these splits were processed at 3500ppb dissolved oxygen levels.

Therefore, the no ozone split in this experiment repeated the 3000ppb dissolved oxygen split in the first experiment and yielded the same results.

DISCUSSION

The experiments above were repeated several times and the same results were obtained each time. The dissolved oxygen in the water showed no statistical effect on the contact resistance of the fully integrated structure, but dissolved ozone concentrations as low as 15ppb raised the contact resistance of this structure by an order of magnitude. Therefore, it was clear that ozone, not dissolved oxygen, was the cause of the interfacial oxide growth enhancement and this increase in interfacial oxide was the cause the of the high contact resistance. The growth of native oxide by ozonated water is well known[7-8].

CONCLUSION

Dissolved ozone, in concentrations as low as 15 ppb, has a deleterious effect on N^+ doped polycrystalline to N^+ doped monocrystalline silicon contact resistance. The same work also indicates that much higher dissolved oxygen concentrations can be allowed (over two orders of magnitude higher than has previously been recommended in the literature) with no statistically significant effect on the contact resistance of this structure. We therefore conclude that dissolved oxygen in ultrapure water is not the major concern once believed.

ACKNOWLEDGMENTS

The authors would like to thank the many operators, technicians and engineers at APRDL for their contributions and help with this project. The authors would also like to thank the management of APRDL for their support of this project.

REFERENCES

[1] F. Walczyk, et. al., "Tailoring Interfacial Oxide for Polysilicon Bit-Cell Contacts and Emitters with In-Situ Vapor HF Interface Cleaning and Polysilicon Deposition in a 4MBit BiCMOS Fast Static RAM", Proceedings of the 1992 IEEE Bipolar/BiCMOS Circuits Meeting, October, 1992.

[2] C.J. Werkhoven, et. al., "Polysilicon Contact Resistance Control Using Cluster Tool Technology", Semiconductor International, To Be Published.

[3] Hashimoto, et. al., "Manufacturing Equipment for Ultrapure Water for 16MB Devices," Proceedings of the Ninth Annual Semiconductor Pure Water Conference, January, 1990.

[4] Tadahiro Ohmi, et. al., "Examining Performance of Ultra High Purity Gas, Water, and Chemical Delivery Subsystems," Microcontamination, Volume 8, Number 3, March 1990.

[5] Tadahiro Ohmi, et. al., "Advanced DI Water System With Low Dissolved Oxygen for ULSI Processing," 1990 Proceedings of the 36th Annual Technical Meeting of the Institute of Environmental Sciences, April 1990.

[6] Tadahiro Ohmi, et. al., "Foresightedness in RCA Cleaning Concept and Importance of Surface Microroughness in ULSI Device Performance," Proceedings of 1991 Microcontamination Conference and Exposition, October 1991.

[7] R.A. Craven, A.J. Ackermann, and P.L. Tremont, "High Purity Water Technology for Silicon Wafer Cleaning in VLSI Production, " Arrowhead Industrial Water Technical Paper, Microcontamination, November 1986.

[8] U.S. Patent # 4749640, Monsanto Electronic Materials Company, Patent rights assigned to Arrowhead Industrial Water, Inc.

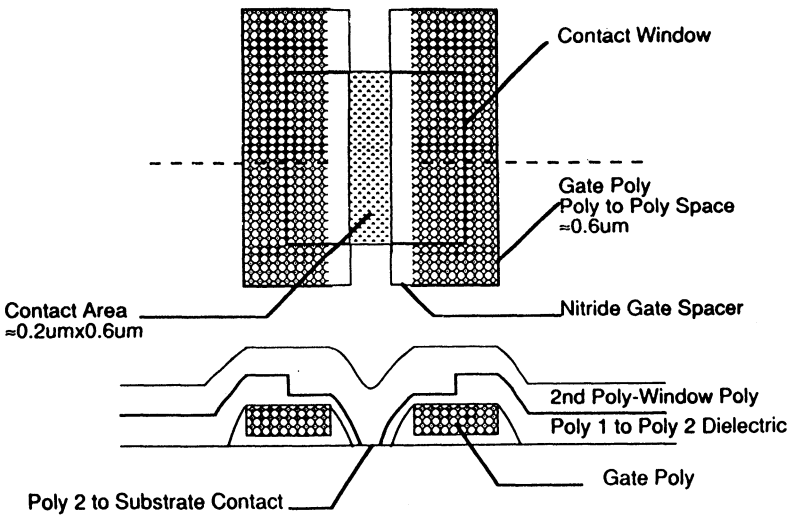


Figure 1. Self Aligned Bit Cell Contact

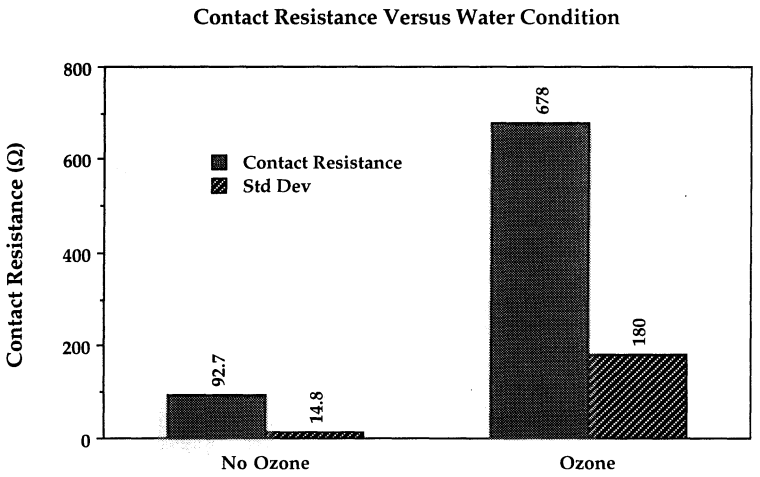


Figure 2. Effect of Rinse Water Type on Contact Resistance

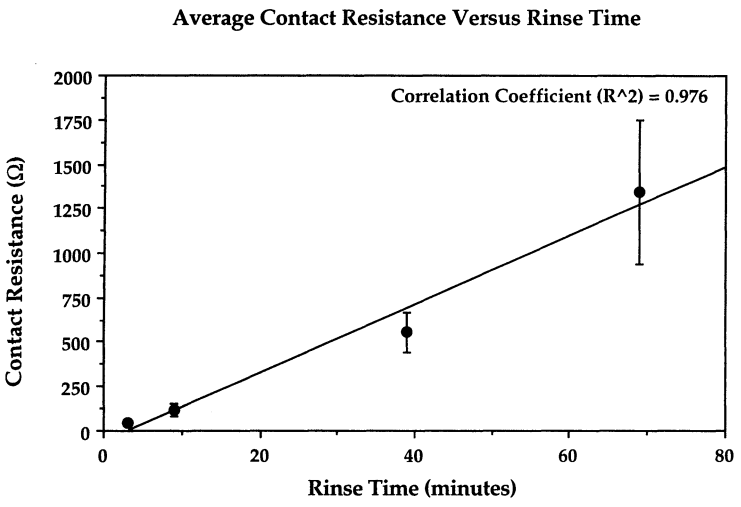


Figure 3. Contact Resistance Versus Rinse Time

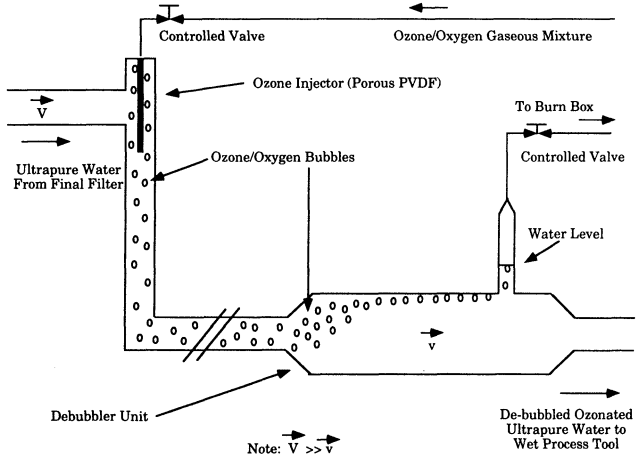


Figure 4. Ozone Injection Apparatus

Average Contact Resistance Versus Dissolved Oxygen Level (No Ozone)

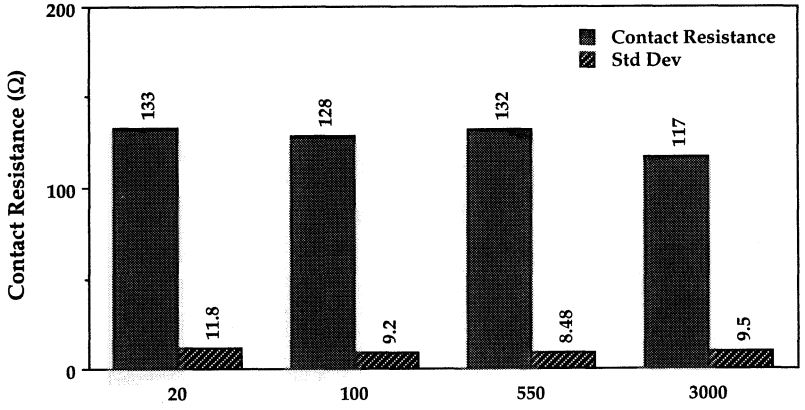


Figure 5. Contact Resistance as a Function of Dissolved Oxygen

Average Contact Resistance Versus Dissolved Ozone Concentration
(Dissolved Oxygen @ 3500ppb)

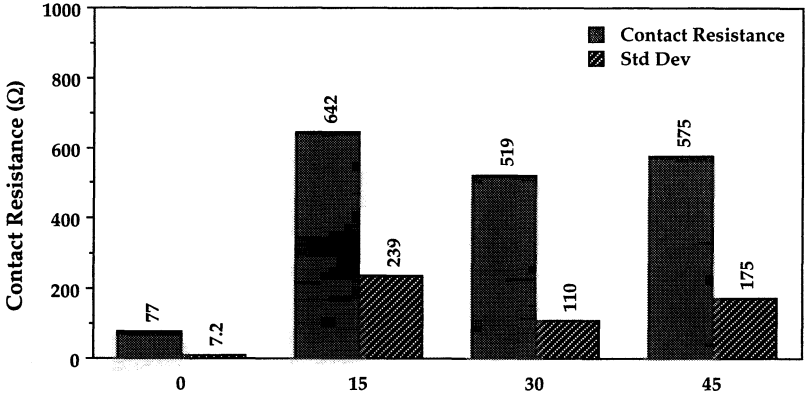


Figure 6. Contact Resistance as a Function of Dissolved Ozone Level

MEGASONIC CLEANER CHARACTERIZATION FOR VLSI PLANARIZATION RIE POST CLEAN PROCESS

Ping Wang and David Bell
Motorola
2200 W. Broadway Rd, M301, Mesa, AZ 85202

ABSTRACT

In this study, megasonic cleaning was applied to the multilevel metal planarization RIE etchback process. The characterization of a newly designed quick dump megasonic cleaner for VLSI post planarization RIE treatment was studied. It was found that the megasonic power during rinse cycle is the most significant parameter that affects the cleaning efficiency. A new megasonic cleaning process with optimized parameter conditions were obtained. The new process significantly reduced the planarization post cleaning defectivity level. The results were confirmed by patterned planarization monitor wafer inspection, and the yield of snake/comb wafers.

INTRODUCTION

The megasonic wafer cleaning technique has been widely used in the semiconductor industry in recent years, especially in front end wafer processes. The megasonic energy in a tank or in a DI jet spray has been found to greatly enhance the particle removal capability of the cleaning liquid (1-3). In this investigation, megasonic cleaning has been applied to a back end multilevel metal planarization RIE etchback process. It was observed that megasonic cleaning is very effective in the removal of planarization dry etch process particles. It was found that it is very important to turn on high power of megasonic energy during rinse cycle to keep particles from re-attaching to the wafer surface.

In this paper, the characterization of a newly designed quick dump megasonic cleaner for this RIE process will be described. The snake/comb and inline defectivity Inspex data comparing different types of megasonic cleaners will be presented.

EXPERIMENTAL

A newly designed Verteq quick dump megasonic cleaner was used in this study. In conventional megasonic cleaners, the megasonic transducer is flat. The megasonic energy propagates through a half-moon shaped quartz lens to the liquid in the tank. In this new cleaner, the transducer itself is half-moon shaped which increases the efficiency of propagation of the megasonic energy. The new equipment consists of only one tank for both cleaning and rinsing. The advantage of this arrangement is the availability of megasonic power during the rinse cycle. The equipment also features quick dump and filtration capabilities.

For the characterization of the new megasonic cleaner, Catalyst/DOE software from BBN was used to set up a test matrix of 30 runs. The key parameters investigated in this experiment were megasonic cleaning power and time, number of quick dumps after megasonic clean, as well as power and time during rinse cycle as shown in Table I:

Table I Parameter Settings For The Characterization Experiment

Parameters	Settings
Megasonic Cleaning Power	100 to 300 W
Megasonic Cleaning Time	5 to 15 Min
# Of Quickdumps Prior To Rinse	0 to 7 Times
Megasonic Power During Rinse	0 to 300 W
Rinse Time	8 to 15 Min

A fixed surfactant (NCW 601 from Wako Chemical) to DI water ratio of 1:2000 was used in the cleaning cycle. In order to simulate the planarization etchback RIE process, particle test silicon wafers were coated with 1000 Å of TEOS to create an oxidized surface. Fused silica particles ranging from 0.1 to 5.0 μm were mixed in a DI water solution with a 1: 500,000,000 ratio. The solution was sprayed onto the silicon wafer surfaces with resultant particle counts ranging from 1000 to 25,000 particles per wafer. Five wafers representing the above range of the particle counts were run in each test. The change in particle counts after megasonic clean was plotted versus the starting particle counts for each run. A simple curve was fitted to the data. The slope of the line was used as the figure of merit for comparing test results.

After the new equipment was characterized and optimized, the new process was compared with the standard process of the existing conventional Verteq Sunburst stand alone megasonic system. The megasonic transducer of the stand alone system is flat and did not have megasonic power capability during the rinse cycle. Patterned planarization monitor wafers and snake/comb wafers were used for this comparison study. The patterned planarization monitor wafers and snake/comb wafers were prepared by running silicon wafers through the metal and planarization module to simulate the real planarization process in the production flow.

The patterned planarization monitor wafer test flow is shown as follows:

1. Wafer mark
2. Metal deposition
3. Metal patterning
4. Metal etch
5. Planarization deposition
6. Planarization etchback RIE
7. Inspex
8. Planarization post megasonic cleaning
9. Inspex

The snake/comb wafer test flow is shown as follows:

1. wafer mark
2. Planarization deposition

3. Planarization etchback RIE
4. Planarization post megasonic cleaning
5. Metal deposition
6. Metal patterning for snake/comb structure
7. Metal RIE
8. Metal anneal
9. Snake/comb probe

Each of the patterned planarization monitor lot or snake/comb lot was split to be run in the new and the old machine at the post planarization megasonic clean step. The patterned planarization monitor wafers were inspected using an INSPEX EX3000 station both after planarization etchback RIE, and again after post planarization megasonic cleaning. The reduction of particle counts on the planarization monitor wafers after megasonic cleaning were calculated. The snake/comb wafers were tested for electrical opens and shorts at probe. Defect density was calculated using Poisson's model on these snake/comb wafers (4).

RESULTS AND DISCUSSION

For the new quick dump megasonic cleaner characterization, 30 tests were run with the conditions as shown in Table I. Figure 1 shows the particle removal as a function of pre-clean particle counts for one of the 30 Catalyst test runs. The set points were megasonic cleaning power of 100 Watts and time of 10 min., 7 quick dumps after megasonic clean and prior to rinsing, rinse power of 300 Watts and time of 15 min during rinse cycle. A simple curve was fitted with R^2=0.99. The slope of the resulting line (0.768) was used as the figure of merit for comparing test results. It is important to note that the figure of merit is not simply a particle removal efficiency of the run. Rather, it is considered as a function of average particle removal capability of each test within the starting particle range investigated.

The figure of merits for all of the 30 runs were entered into Catalyst experimental design worksheet as the response of the experiment. Figure 2 is the Catalyst model graph of this experiment. Two lines for each factor are displayed for the factor-response relationship when that factor interacts with other factors. The top

line for each factor shows the most positive effects that factor can have on the response. The bottom line shows the most negative effects that factor can have on the response (5). Rinse power stands out as the most influential of the five parameters investigated. Other parameters, on the other hand, did not appear to be as significant as rinse power for cleaning efficiency. It is noticed that for the rinse power, both of the two effect lines (positive and negative) show that cleaning efficiency (figure of merit) increases dramatically as rinse power increases. There is little interaction between rinse power and the other factors, since the two rinse power effect lines are almost parallel. It is believed that during the rinse cycle, it is very important to use high megasonic power to prevent the particles in the fluid re-attaching to the wafer surface.

The optimized conditions for this experiment were determined by applying the Catalyst interpretation tool, and maximizing the effects of all parameters. The maximum predicted average efficiency rating (figure of merit) is 0.78.

The optimized process using the new machine was compared with the old process using the old machine. Figure 3 shows the snake/comb defectivity boxplot versus post planarization RIE megasonic clean process for each of the machines. It is seen that the new megasonic process of the new equipment significantly reduces the snake defectivity level of post-planarization RIE treatment from 0.78 to 0.22 defects/cm^2. The distribution of the defectivity for the wafers run on the new megasonic cleaner was also tighter than that of the old machine. The Inspex results from patterned planarization monitor wafer were compared for new and old equipment. It is noticed that the new process in the new machine increases the mean particle removal rate from 68% to 77%.

SUMMARY

In this study, the characterization of a newly designed quick dump megasonic cleaner for post planarization RIE treatment was performed. It was found that the megasonic power during rinse cycle is the most significant parameter that affects the cleaning efficiency. A new process with optimized parameters was obtained. The maximum particle removal efficiency rating (Figure of merit) is about 0.78. The new

process significantly reduced the planarization post cleaning defectivity level. The results were confirmed by planarization patterned Inspex monitor wafers and snake/comb wafers.

ACKNOWLEDGEMENT

The authors would like to thank Mr. Tom Roche for his valuable suggestions about testing methodology and Mr. Mike Clayton for his help on Catalyst analysis. Thanks should also go to Mr. Chip Cope and his team for helping with teos wafer preparation.

REFERENCES

1. W. A. Syverson, M. J. Fleming, and P. J. Schubring, Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing, The Electrochemical Society, pp. 10-17, 1992.
2. V. B. Menon and R. P. Donovan, Microcontamination, pp. 29-34, Nov., 1990.
3. M. B. Olesen and E. R. Blome, Proceedings of KTI Microlithography Seminar, pp. 125-144, 1991.
4. P. Wang, B. Liu, M. May., and M. Granum, Proceedings of SPIE Microelectronics Manufacturing and Reliability, pp. 69-80, 1992.
5. BBN/Cataiyst Handbook, pp. 415-425, 1992.

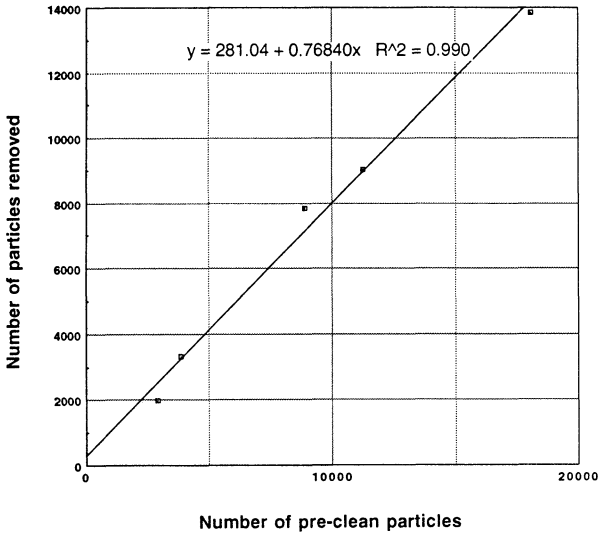


Fig. 1. Number of particle removed as a function of number of pre-clean starting particle counts for one of the 30 Catalyst test runs. The set points were megasonic cleaning power of 300 W and time of 10 min., 7 quick dumps, rinse power of 100 W and time of 15 min. The slope of the line was used as the Figure of Merit.

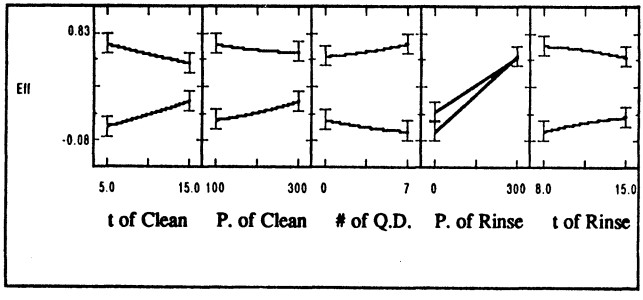


Fig.2. A model graph illustrates the factor-response relationship when each factor interacts with other factors. The top line for each factor shows the most positive effects that factor can have on the response. The bottom line shows the most negative effects that factor can have on the response.

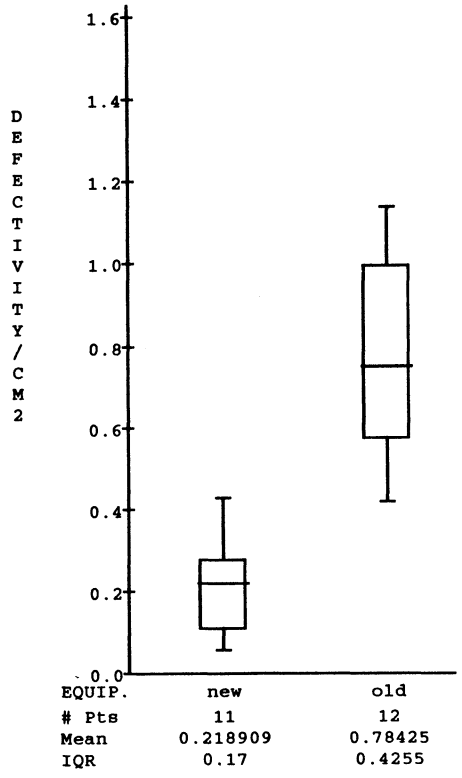


Fig.3. Snake/comb defectivity boxplot versus post planarization RIE megasonic cleaning processes using different machines.

STUDIES OF RINSE EFFICIENCIES IN WET CLEANING TOOLS

J.J. Rosato, R.N. Walters, R.M. Hall, P.G. Lindquist, R.G. Spearow
Santa Clara Plastics, 400 Benjamin Lane, Boise, ID 83704

C.R. Helms
Stanford University, Electrical Engineering Department, Stanford, CA 94305

ABSTRACT

The efficiency of the rinse process in automated wet cleaning stations is examined following HF-last cleans. Experimental results are presented showing the effects of tank geometry, flow parameters, cassette geometry, cassette materials, and wafer load. A theoretical model for the fluid dynamics in a rinse tank is developed which yields information regarding the flow distributions between and around wafers in a cassette. The time dependence of the tank resistivity during the rinse process is fitted to a second order mathematical model based on convective transport and ideal mixing assumptions. The effectiveness of the model confirms the importance of the fluid dynamics in the rinse process.

INTRODUCTION

The rinse process has received considerable attention in recent years. With the increasing complexity of semiconductor manufacturing technologies, the number of wet process and rinse steps has increased dramatically. Considering that typical rinses can consume up to 70 liters per minute of UHP DI water, and given the high throughput of automated wet cleaning stations, it becomes apparent that DI water consumption is a major cost issue. The problem is further compounded for large diameter wafers, which require larger tank volumes and even greater quantities of DI water. Recent cost of ownership models for automated wet stations show that the wafer cost component for DI water has increased from 13% for 150 mm wafers to 32% for 200 mm wafers (1). Clearly, there is considerable motivation to improve the efficiency and effectiveness of the rinse process in order to reduce DI water consumption.

The cleaning and rinsing of wafers can be limited by a number of factors, including: 1) the surface reaction kinetics; 2) thermodynamics; 3) diffusion of reactants, products, and contaminants; and 4) convective transport of reactants, products, and contaminants. The relative importance of these factors depends upon the prior wafer history, the chemistries involved, the fluid dynamics, and the design of the process vessels. For simple rinsing of soluble residues, the predominant mechanisms are convective and diffusive mass

transport of contaminants from the wafer surface. Any residues left on the wafer surface after the rinse process will be transferred to the next process step, or, in the case of drying, will ultimately deposit on the wafer as a surface contaminant.

Recent studies have attempted to address these phenomena from a theoretical point of view in order to determine the rate-limiting factors in rinsing (2,3,4). One theory maintains that the wafer is covered with a uniform carryover layer coming out of the chemical bath, and subsequently sheathed within a static boundary layer during the rinsing process. Therefore, the removal of surface residues requires diffusion through the boundary layer, and then convective transport in the bulk fluid (2). This paper will demonstrate that such models are not applicable to well-designed rinsing processes.

CARRYOVER OF RESIDUES INTO THE RINSE TANK

When wafers are removed from a chemical bath, there is a residual liquid which adheres to the wafer and cassette surfaces, and is subsequently carried over into the rinse tank. This total *carryover volume* will depend upon a number of factors, including: 1) the extraction rate from the chemical bath; 2) the transfer time between baths; 3) the immersion rate into the rinse tank; 4) the number of wafers; 5) the cassette surface area; and 6) the cassette material. The carryover volume may be categorized as either: 1) a *bulk carryover* in the form of liquid droplets or puddles which are nonuniform in nature; and 2) a *carryover layer* which is a somewhat uniform liquid film that remains on the surface due to viscous forces. Figure 1 shows a schematic representation of the carryover volume. The nature of the carryover volume depends upon the balance between gravitational, viscous, and surface tension forces. Gravitational and surface tension forces will tend to pull liquid off the surface during removal from the solution, whereas the viscous force will react against velocity gradients, holding a layer of liquid on the surface. For typical process conditions, this force balance seldom results in a uniform film of liquid on the surface. In fact, for hydrophobic surfaces, the surface tension forces are so dominant that the notion of a carryover layer is certainly not applicable.

Previous analyses of the carryover layer thickness have neglected surface tension effects (which can be significant for both hydrophilic and hydrophobic surfaces), and drainage of the fluid after extraction. A more accurate relationship for the carryover layer thickness h, accounting for viscous, gravitational, and surface tension forces during the removal process is given by (5):

$$h = \{\mu V/\rho g\}^{1/2}\, Ca^{1/6} \qquad [1]$$

where μ is the viscosity (0.01 g/cm-s for water), V is the extraction velocity, ρ is the density (1 g/cm^3 for water), g is the gravitational acceleration (980 cm^2/s), and Ca is the capillary number given by:

$$Ca = \mu V / \sigma \qquad [2]$$

with σ being the surface tension (70 dynes/cm for water). Substituting the values for water yields

$$h = (0.0007)\ V^{2/3} \qquad [3]$$

For slow extraction velocities V < 10 cm/s, this gives a carryover layer thickness of h < 30 μm. In the case of automated wet stations with robotic systems set for high throughput, the extraction velocities are in the range of 20 - 60 cm/s, giving a thickness range of 50 - 100 μm. Note that this analysis is only valid during the extraction phase, and is not applicable once the wafers have come to rest or have begun the lateral transfer to the rinse tank. During this phase, fluid drainage will occur, forming droplets and puddles which will drip off when a critical mass is reached. Thus, the value of the carryover layer thickness given above represents the upper limit, and is only applicable for hydrophilic surfaces with very fast pull rates and short transfer times. In most cases, the concept of a bulk carryover, with perhaps isolated regions of a carryover layer, is more accurate. Upon immersion into the rinse tank, this carryover will then be removed by diffusive or convective processes.

DIFFUSION OF RINSE RESIDUES

In the case of a static system, which is the limit of no convective mass transport, the rinsing of a wafer surface will be limited by the diffusion of chemical residues or contaminants from the wafer surface into the bulk solution. The problem becomes the classical one of diffusion from a limited-source, with a Gaussian solution for short times (2, 6). For longer times, the outdiffusion from the neighboring wafer must be considered. Assuming an initial concentration of residue C_0 (cm^{-3}) in a carryover volume of average thickness 20 μm, the fraction of concentration remaining as a function of time and distance from the wafer surface is shown in Fig. 2 for a 50 wafer load. Two items are apparent from the profile: 1) the surface concentration (at x = 0) decreases very quickly initially, and 2) the tail of the distribution advances at a much slower rate.

If we assume the case of a carryover layer sheathed in a static boundary layer (2), the overall rinse process would be limited by the time required for the diffusion front to reach the edge of the boundary layer, where convective transport would then be dominant. Using a value for the static boundary layer thickness of 0.26 cm, as suggested in reference (2), would result in a time delay of over 2 minutes. As will be shown below, this does not agree with the experimental evidence.

CONVECTIVE TRANSPORT OF RINSE RESIDUES

In order to determine the relative importance of the convective transport of rinse residues, the fluid dynamics in a rinse tank must be determined. In particular, the behavior of the wafer gap flow field within a rinse tank determines, to a large degree, the effectiveness and efficiency of the rinse cycle. In the following analysis, the fluid dynamics in an overflow rinse tank (OFR) will be modeled from first principles. More extensive computer simulations will be reported in a future publication.

Rinse Tank Geometry and Flow Field Regions

The geometry used for the analysis consists of fifty 200 mm diameter wafers in a cassette with 0.55 cm gap spacing (0.25 inch centerline spacing). This is the configuration used in the Santa Clara Plastics Advanced Automated Tool, which was used for experimental verification. Figure 3 shows a top view of the tank and wafer geometry (the wafer cassette is not shown). Typical DI flowrates range from 40 - 60 liters per minute, corresponding to an average velocity U_o of 0.85 cm/s at the tank inlet. The three flow regions of interest are 1) in the gaps between wafers; 2) in the short sidewall areas at the ends of the tank; and 3) in the long sidewall areas at the sides of the tank. Regions 1 and 2 consist of two flat parallel boundaries which can be treated as a 'channel' flow, while region 3 consists of only one flat boundary which can be treated as 'flat plate' flow (7).

Results of flow computations show that average velocities in the three regions of interest are comparable, suggesting that convective transport in the wafer gap region can be a significant factor in rinsing. These results have been confirmed by visual observations and testing. Therefore, for the sake of brevity, the analysis presented herein will be restricted to the wafer gap region, although results will be given for all regions.

Wafer Gap Flow Field Analysis - Channel Flow

A first order approximation to the flow field behavior begins with a Reynolds number calculation based upon a characteristic distance for the region of interest (7). This is used to determine the flow regime - laminar or turbulent - which then allows for a calculation of the flow boundary layer profile. Finally, the velocity profile within the boundary layer and the shear stress distribution along the boundaries are determined.

In the region between the wafers, a suitable characteristic length is the gap width. A Reynolds number based on the gap width has the form

$$(Re)_b = (U_o\, b) / \nu \qquad [4]$$

where U_o is the average entrance velocity, b is the spacing between wafers, and ν is the

kinematic viscosity (0.01 cm^2/s for water). Inserting values yields a relatively low Reynolds number of 47, indicating a laminar flow field between the wafers. In general, the flow between two flat parallel boundaries will experience an acceleration along the length due to the thickening of the two closely spaced boundary layers. The velocity increases until the boundary layers from both sides merge and the flow achieves a steady-state condition, at which point it is called 'fully developed' laminar flow. The length required to fully develop the inlet flow is given by (7)

$$L_e = (0.02)\,(b)\,(Re)_b \qquad [5]$$

which, upon inserting values, yields a distance of only 10 mm from the wafer leading edge. Therefore, the flow is undeveloped for the first 10 mm of the fluid inlet, and fully developed for the remaining 190 mm. The velocity distribution for fully developed plane flow moving in the x-direction (lengthwise) is obtained by simplifying the Navier-Stokes equation for 1-d parallel flow. For fully developed flow in the x-direction, this becomes:

$$d^2U/dy^2 = (1/\mu)\,(dp/dx) \qquad [6]$$

where U is the velocity, p is the pressure, and the y-axis represents the transverse direction across the wafer gap. Inserting the appropriate boundary conditions to satisfy the no-slip condition at the boundary (U = 0 at y = 0 and y=b), integrating, and solving for the integration constants yields the parabolic velocity distribution

$$U(y) = 6\,U_o\,(y/b)\,(1 - y/b) \qquad [7]$$

with a maximum velocity $U_{max} = U(\text{at } y=b/2) = {}^3/_2\,U_0$, where U_0 is the average entrance velocity. Figure 4 shows the boundary layers and the velocity profiles between the wafers for undeveloped flow (x < 10 mm) and fully developed flow (x > 10 mm). The most obvious feature of the velocity profile is the absence of a 'static' boundary layer region.

The effect of the fluid flow on the residue (carryover volume) at the wafer surface can be estimated by calculating the shear stress at the surface. Since the velocity for fully-developed flow is independent of x, the shear stress is constant and can be estimated from Newton's law of friction:

$$F_\tau = \mu\,(dU/dy)_{y=0} \qquad [8]$$

where F_τ is the shear stress, and (dU/dy) is the slope of the velocity profile at the boundary (y=0). This gives a constant value of $\tau = 0.1$ dyne/cm^2. The importance of the shear stress acting on the carryover layer cannot be overlooked. Due to the fluid viscosity and a no-slip (U = 0) condition at a given boundary, a shear stress exists at the boundary along its entire length. The shear stress initially acts upon the outermost lamina of the carryover

layer, resulting in a downstream motion, which subsequently generates a shear stress on the lower lamina (Fig. 4c). This viscous entrainment is repeated until a solid boundary, the wafer surface, is reached. The result is a streamwise transport of the carryover layer along the wafer length, and a very effective removal of wafer residues. Table I summarizes the important flow characteristics for the three regions in the rinse tank.

EXPERIMENTAL

Rinse evaluation experiments were carried out using 200 mm diameter wafers in two fully automated wet process stations manufactured by Santa Clara Plastics: 1) Automated Wet Station (AWS), designed to handle two standard cassettes of 25 wafers; and 2) Advanced Automated Tool (AAT), featuring a reduced cassette design capable of handling 50 wafers. The reduced cassette design of the AAT allows for smaller tank volumes and improved fluid dynamics, thereby reducing chemical and DI water consumption significantly. Wafer pitch in these experiments was held constant at 6 mm (0.25"), although results for reduced pitch experiments will be reported in a future publication.

All rinse processes were carried out on bare Si wafers following a typical native oxide removal process (50:1 HF at 25°C for 120 seconds), except where noted. Rinse efficiencies were monitored using standard resistivity and pH probes. For typical HF last processes, the resultant change in hydrogen ion concentration in a rinse tank, as monitored by resistivity or pH, is an accurate indicator of the HF concentration over the range of interest. For extreme high concentrations of HF, the incomplete dissociation of HF must be considered, while for very dilute concentrations, the hydrogen ion concentration due to the water must be accounted for.

IDEAL MIXING MODEL

In order to understand the time dependence of the rinse water resistivity following an HF clean, a second order mathematical model with relatively few parameters was developed. The model is based on the assumption that convective transport of the HF carryover volume is the dominant removal mechanism. The basic premise of the model is that upon immersion in the rinse tank, the entire carryover volume of HF is dissolved and ideally mixed in the DI rinse water volume.

The concentration of HF (or hydrogen ion concentration) in the rinse tank would then follow a simple exponential behavior given by:

$$C(t) = C_0 \exp(-t/\tau) \qquad [9]$$

where $C(t)$ is the concentration of HF in the rinse tank at a time t after the immersion at $t=0$; C_0 is the total volumetric concentration of the HF carryover (the total quantity of HF residue divided by the total volume of rinse water); and τ is a characteristic time constant

for the mixing process.

In the case of an overflow rinse tank, where DI water is continually flowing into the tank, the time constant τ will depend upon the flow rate and the tank geometry. For the simplest case with a uniform flow inlet at the bottom of the tank, and a probe mounted at the top of the tank, the time constant will be related to the bath turnover rate:

$$\tau = \text{(Volume of Tank)} / \text{(DI Flow Rate)} \qquad [10]$$

In order to compare the model to experimental data, the concentration values predicted by the model are converted to conductivity values, accounting for the conductivity of water and the dissociation constant of HF. For dilute concentrations, the conductivity can be expressed as:

$$G(t) = G_{H2O} + G_0 \exp(-t/\tau) \qquad [11]$$

where G(t) is the conductivity as a function of time t after immersion in the rinse tank (S/cm); G_{H2O} is the conductivity of the incoming DI water; G_0 is the conductivity of the total rinse volume; and τ is the bath turnover time constant. The resistivity is then simply the inverse of equation [11], after converting units to MOhm-cm.

The expected values of τ can be calculated based on the tank geometries and flow rates. For the AWS, with it's larger tank volume, the calculated bath turnover rate is 48 seconds, while the corresponding value for the AAT is 25 seconds. The parameter G_0 is related to the total carryover volume, and should therefore be dependent on the cassette area, the number of wafers in the cassette, the extraction rate from the chemical tank, the immersion rate into the rinse tank, and the total volume of DI.

The parameters of equation [11] can be extracted from the experimental resistivity vs. time data. The correlation of the model constants to physical values will give an indication of the validity of the model assumptions. If the time constant τ is approximately equal to the bath turnover rate, then the assumption of convective limited mass transport via ideal mixing is validated. A longer time constant would indicate a two-step process involving diffusive and convective mass transport.

RESULTS AND DISCUSSION

Results for the fitted vs. experimental values of rinse water resistivity for a post-HF overflow rinse are shown in Figs. 5-8. Data are shown for the AAT, with teflon and quartz reduced cassettes, in Figs. 5 and 6, respectively. Note that the rinse time to resistivity (RTTR) for the teflon cassette is highly dependent upon the wafer load. This suggests that the carryover volume is predominantly associated with the wafers (most

likely droplets and puddles). As such, the tank resistivity is an accurate indicator of the wafer rinse efficiency. In the case of quartz, there is considerably less wafer dependence, even though the quartz reduced cassette surface area is identical to the teflon reduced cassette. This is probably due to increased wetting of the quartz hydrophilic surface, and possible surface chemical reactions (quartz etching).

For comparison, a standard full cassette (Fluoroware PA-192) was run in the AAT with varying wafer loads. The results shown in Fig. 7 indicate very little rinsing dependence on the wafer load. The implication here is that the increased surface area and reduced drainage of the full cassette results in a carryover volume which is dominated by the cassette attributes. Therefore, the resistivity value in the rinse tank is probably more indicative of the cassette rinsing behavior than of the wafer rinsing efficiency.

Similar data are shown in Fig. 8 for the AWS. Here, a standard 25 wafer full cassette (Fluoroware PA-192) is compared to a 25 wafer cassette made of quartz. Again, the quartz cassette exhibits slower rinsing behavior.

The model time constants extracted from the experimental data are summarized in Table II. The excellent agreement with the bath turnover rates confirms the model assumptions of convective transport and ideal mixing. The time constant is shown to be dependent primarily on the bath turnover rates, and not on the cassette materials, cassette geometry, and wafer load.

CONCLUSIONS

The fluid dynamics in an overflow rinse tank were modeled analytically. The results show that fully developed laminar flow is prevalent in the region between the wafers. Calculations of the velocity profiles and shear stress forces indicate that the wafer gap flow fields are predominant in removing rinse residues via shear stress and convective transport. A model was developed to predict the time dependence of the rinse tank resistivity. The excellent agreement of the model with experimental data confirms the assumptions of convective transport and ideal mixing. An understanding of the removal mechanisms in the rinse process can be used to improve rinse efficiency and reduce DI water consumption in automated wet stations.

REFERENCES

1. G.D. Ching and R.B. Murtha, in Microcontamination 93 Proceedings, P205, p.378 (1993).
2. A. Tonti, in Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing, J. Ruzyllo and R.E. Novak, Editors, PV92-12, p.41 (1992).

3. A. Tonti, in Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing, J. Ruzyllo and R.E. Novak, Editors, PV92-12, p.409 (1992).
4. F.W. Kern et al, in Proceedings of the 37th Annual IES Meeting, p.23 (1991).
5. R.P. Spiers et al, Chemical Engineering Science, 29, p.389 (1974).
6. A.B. Glaser and G.E. Subak-Sharpe, Integrated Circuit Engineering, p.197, Addison Wesley, Massachusetts (1977).
7. H. Schlichting, Boundary Layer Theory, McGraw-Hill, New York (1968).

Table I. Rinse tank laminar flow field parameters

Region	Flow Regime	Characteristic Length x (cm)	Re_x	L_e(cm)	F_τ (dyne/cm²)
1	Channel Flow	0.55	47	1	0.10
2	Channel Flow	4.8	408	39	$0.026/\sqrt{x}$†
3	Flat Plate	25.4	2151	-	$0.026/\sqrt{x}$

† - Undeveloped channel flow

Table II. Ideal mixing model parameters extracted from experimental data

CASSETTE TYPE	TOOL	# WAFERS	Go(uS/cm)	TAU(sec)
Teflon Reduced Cassette	AAT	0	3.00E-05	21
Teflon Reduced Cassette	AAT	25	8.00E-05	21
Teflon Reduced Cassette	AAT	50	1.30E-04	21
Quartz Reduced Cassette	AAT	0	3.00E-04	20
Quartz Reduced Cassette	AAT	25	2.60E-04	20
Quartz Reduced Cassette	AAT	50	2.20E-04	20
Standard Full Cassette	AAT	0	6.50E-05	19
Standard Full Cassette	AAT	10	8.00E-05	19
Standard Full Cassette	AAT	25	8.00E-05	19
Standard Full Cassette	AWS	25	3.10E-05	45
Quartz Cassette	AWS	25	4.40E-05	45

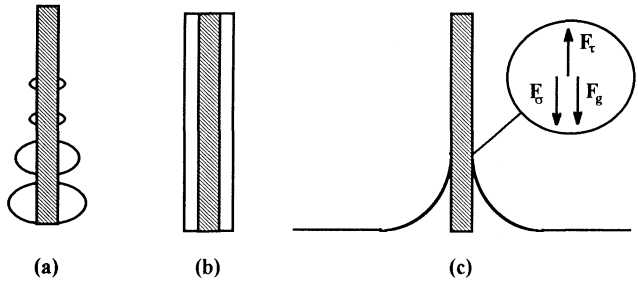


Figure 1. Physical representation of carryover volume. (a) Bulk carryover, (b) Carryover layer, (c) Force diagram

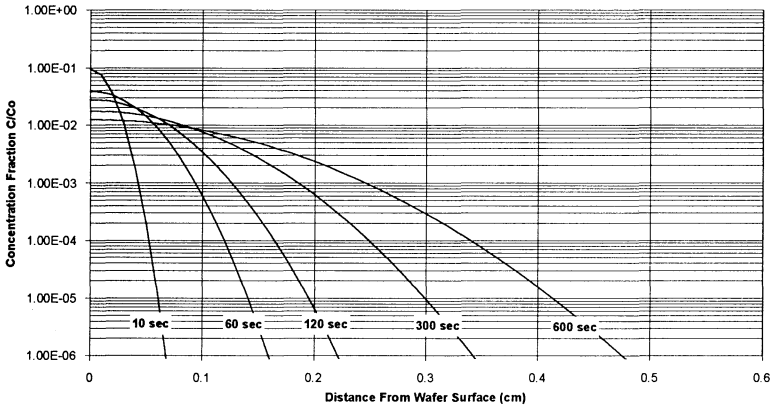


Figure 2. Fractional concentration profile $C(x,t)/C_0$ for diffusion of residues in a carryover volume of initial concentration C_0 and average thickness of 20 μm.

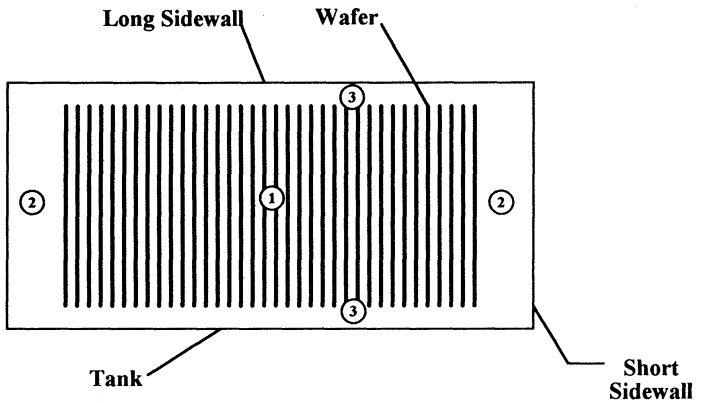


Figure 3. Rinse Tank and Wafer Geometry - Top View

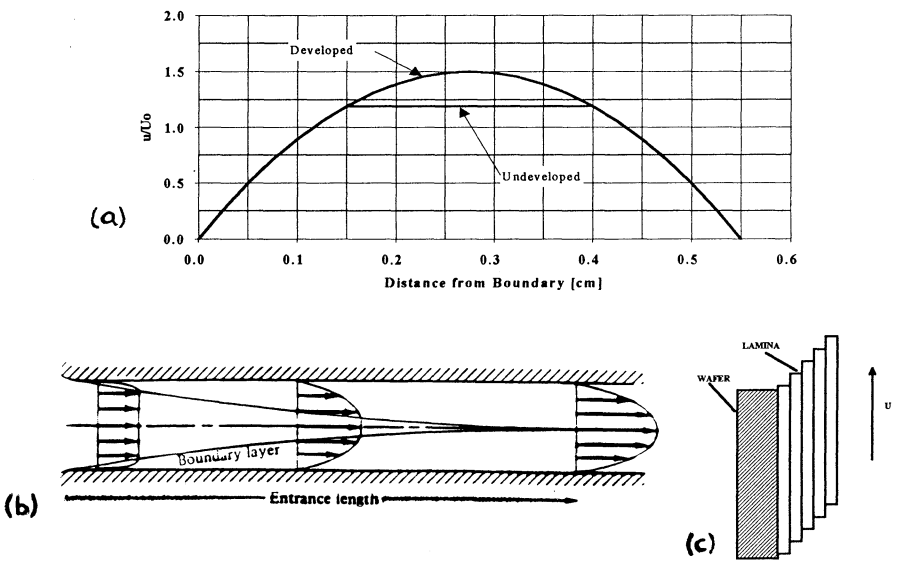


Figure 4. Wafer Gap flow field. (a) Velocity profiles, (b) Boundary layer profile, (c) Lamina shear diagram

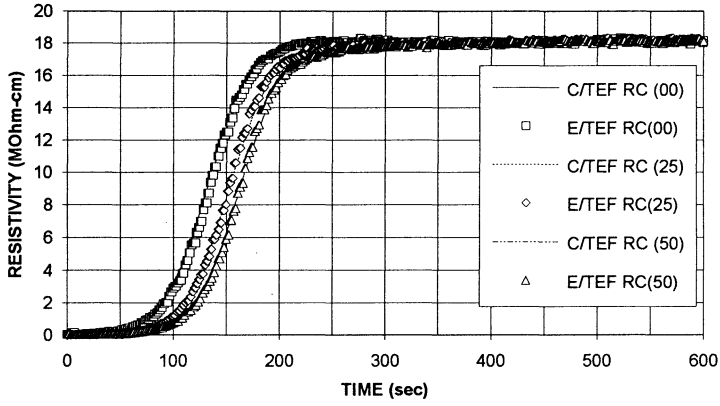


Figure 5. Experimental (points) and calculated (lines) rinse resistivity curves for the Teflon reduced cassette in the AAT with wafer load indicated in parentheses.

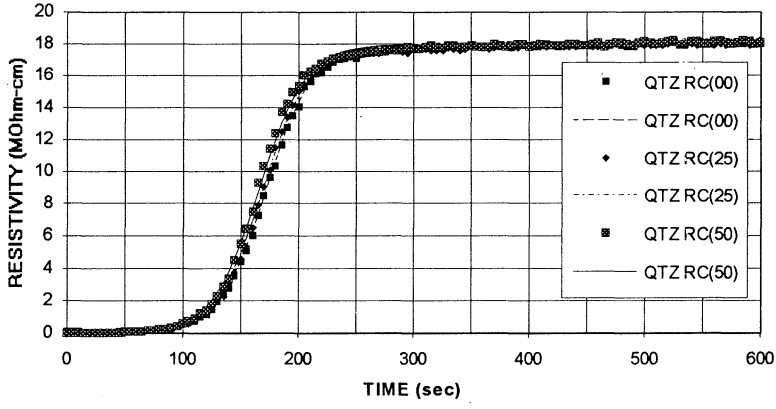


Figure 6. Experimental (points) and calculated (lines) rinse resistivity curves for the quartz reduced cassette in the AAT with wafer load indicated in parentheses.

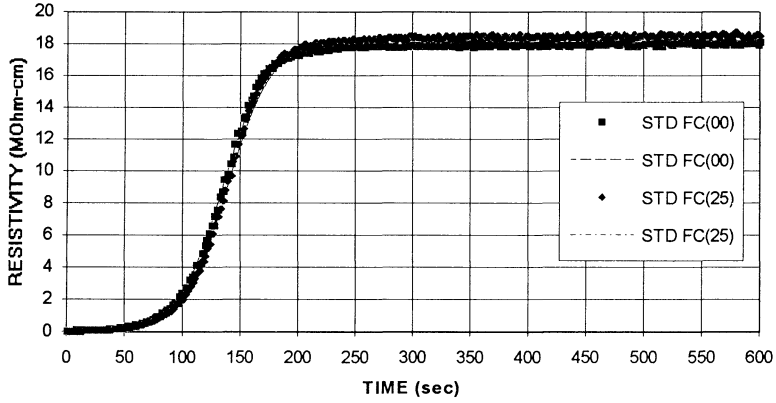


Figure 7. Experimental (points) and calculated (lines) rinse resistivity curves for the standard full cassette in the AAT with wafer load indicated in parentheses.

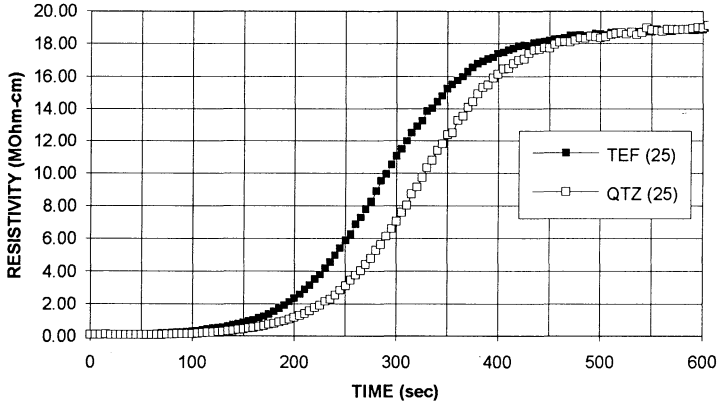


Figure 8. Experimental (points) and calculated (lines) rinse resistivity curves for the Teflon and quartz full cassette in the AWS with 25 wafers.

THE USE OF CENTRIFUGAL FORCE TO IMPROVE RINSING EFFICIENCY

Kurt K. Christenson

FSI International
322 Lake Hazeltine Dr.
Chaska, MN 55318 USA

ABSTRACT

The success of aqueous based cleaning of silicon wafers depends on the complete removal of both the residual contaminants and the cleaning solutions from the silicon surface by a water rinse process. The efficiency of rinsing in a bath is limited by the rate at which contaminates diffuse away from the silicon surface, through the nearly stagnant boundary layer, and into the bulk of the water. Typical reported rinse water requirements for 200 mm wafers range from 13 to 20 liters/wafer for each chemical step (1, 2). This paper reports the improvement in rinsing efficiency gained by repeatedly "ramping" the wafer to a high RPM to spin off this stagnant layer. The rinse efficiency is sufficient to allow complete rinsing with 0.75 liters/wafer for each chemical step, a 20x reduction in water usage compared to present immersion techniques.

INTRODUCTION

The success of aqueous based cleaning of silicon wafers depends on the complete removal of both the residual contaminants and the cleaning solutions by a rinse process. An analysis by Tonti indicates that after 15 minutes in an overflow rinse tank, 0.88% of the initial surface contamination is still carried over into the subsequent process bath or dry sequence in the 20 μm "carry over film" of water on the wafer (3). This poor rinsing performance is caused by a stagnant boundary layer near the surface of the wafer. Contaminants must diffuse through this boundary layer to reach the flowing rinse water and be swept away. Diffusion coefficients for dissolved ionic and molecular species are typically in the range of 10^{-5} cm^2/sec which allows an average diffusion length of approximately 1 mm during a 10 minute rinse (3, 4). Figure 1 shows the approximate distribution of small ionic and molecular contaminants in a stagnant water rinse bath 60, 300, 600 and 900 seconds after insertion of a contaminated wafer.

Rinse tanks are normally not stagnant, but have flow velocities parallel to the surface of the wafers near 1 cm/sec. The fluid motion in these "overflow" rinse tanks acts to sweep away contaminates that have diffused into the flow stream from the surface of the wafers. The water's velocity distribution between the wafers is parabolic; 1.5 times the average velvety half way between the wafers and zero at the surface of the wafer where the contaminants are concentrated. Figure 2 shows the velocity distribution near the surface of a 200 mm wafer for a 1 cm/sec average flow. Only at a distance of 0.55 mm from the wafer does the fluid reach 0.33 mm/sec, the velocity necessary to transit the wafer in one minute. As shown in Figure 1, 35% of the contaminants never diffuse to a distance of 0.55 mm during a 10 minute rinse cycle. Therefor, the flow of water between the wafers in an over flow rinser does little to help rinse the surface of the wafers.

"Dumping" and refilling the rinse tank periodically during the rinse cycle allows contaminants that have diffused some distance into the bulk of the boundary layer drain away. Only the contaminants in the "carry over film" remain on the wafer. The film's thickness is approximately 20 μm and is primarily determined by the drain time, viscosity and density of the water and the force of gravity (3). The thickness can be reduced by supplementing the force of gravity with centrifugal force by spinning the wafers either about their axis as in a spin rinse drier, or off axis as in a multiple position spray processor. The carry over thickness after a 10 second ramp at 500 RPM in a multiple position spray processor was measured to be less than 2 μm. Reducing the thickness of the carryover layer by 10x results in a 90% reduction in the residual contamination in the carry over film. Figure 3 shows the contaminant distribution in the rinse water after 40 seconds. The 2 μm (0.0002 cm) layer that remains after the 500 rpm ramp is approximately equal to the thickness of the "y" axis.

A highly efficient rinse sequence is as follows: At low rpm, the wafers are wetted and contaminants diffuse freely from the wafer surface into a thick layer of water. The bulk of this layer is then removed by centrifugal force. In a second rinse cycle, the wafer is rewetted and contaminants from the thin carry over layer are again allowed to diffuse into this fresh layer of water which is then ramped off... Figure 4 shows the calculated aerial concentration of contaminants in a 2 μm layer at the surface of the wafer for a stagnant bath and for a ramped rinsing sequence. These calculations indicate that ramped rinsing achieves a 175x reduction in the contamination levels at the surface of the wafer after each 1 minute rinse / spin cycle. A single, 1 minute rinse / spin cycle leaves 0.57% of the initial contaminates. A second one minute cycle would reduce the contamination level by another 175x to 0.003% of the initial contamination level. This should be compared to Tonti's calculation of 0.88% remaining after 15 minutes in an over flow rinse[1].

The situation is even more extreme for particles. Figure 5 shows the concentration profile for 0.3 μm particles for diffusion times of 60, 200, 600 and 900 seconds. The diffusion coefficient for these particles is near 1.4×10^{-8}, nearly three orders of magnitude

lower than for small molecular contaminants. Virtually no particles would diffuse into the flow stream during a 10 minute over flow rinse. Only 12% would diffuse out of the 20 μm carry over layer in 1 minute to be removed during a "dump" of the rinse bath. But 88% of the particles that are dislodged from the surface would be removed after each 1 minute ramped rinsing cycle. Ramped rinsing should have a strong, positive effect on particle removal efficiency.

EXPERIMENTAL

The process sequence in an FSI MERCURY® MP spray processor was modified such that the rinse sections after each chemical dispense included a series of 40 second, low speed rinses followed by 20 second, 500 RPM ramps to remove the boundary layer. The MERCURY was also mechanically modified to include an atomized rinse Side Bowl Spray Post (SBSP) in the side of the bowl to rinse the outside of the carriers. Additional fan jets were also included on the bottom of the bowl to better rinse the bottom of the turn table. The base process program was a standard FSI B Clean which consists of an SPM, dilute HF, APM, HPM chemical sequence. Experimental data was collected on 150 mm, <100>, p type wafers using "Semi" grade chemicals from Ashland chemical.

A sodium challenge was prepared by dipping clean wafers in a NaCl solution and spinning them dry without rinsing a SRD. The Na removal rinse sequences consisted of portions of the final rinse sequence of the modified B Clean. Sodium levels were measured by Static SIMS at Evans Central, Minnetonka, Minnesota. The metal challenge was added by plasma ashing 0.5 μm of photo resist on the wafer. VPD-ICP-MS analysis was performed at Balazs Labs, Sunnyvale, California and TXRF measurements were taken at Evans West, Redwood City, California. "HF Last" particle challenge wafers were prepared by dipping clean wafers in a 10% HF solution for 1 minute followed by a spin rinse dry. Pre and post measurements of particles larger than 0.15 μm were performed on an ESTEK™ 8500 Wafer Inspection System calibrated with NIST traceable latex spheres.

RESULTS

The improved rinsing performance allowed the total cycle time of the clean to be reduced from 43 minutes for the standard B Clean to 30 minutes for the optimized clean utilizing ramped rinsing and the Side Bowl Spray Post (SBSP). Figure 6 shows the results of rinsing the Na contaminated wafer for 30 and 120 seconds followed by a 500 rpm ramp and performing the entire final rinse sequence from the modified B clean. In the first 30 seconds the sodium levels dropped by a factor of 3000 to near background levels. This

experimental rinsing rate for ramped rinsing of over 6 LRV/min (Log Reduction Value) is above the 2.25 predicted by the theory. Apparently there is significant turbulence within the fluid during the ramp that acts to further dilute the contaminants in the 2 μm carry over layer. Figure 6 also shows the results of rinsing a soluble ionic salt in an overflow rinse tank (5). Overflow rinsing provided a 0.25 LRV/min in the surface concentration of the salt. The overflow rinsing appears to be 9x less efficient than the theoretical ramped rinsing models and 24x less efficient than the ramped rinsing experimental data.

The metals results were also encouraging. With the exception of nickel, all metal levels after both the standard and SBSP B Cleans were below the detection limits of TXRF and VPD-FIA-ICP-MS (Table 1). The plasma ashing may have transformed some of the nickel into nickel silicide which is insoluble in standard wafer cleaning chemistries. No nickel is normally detected after either clean on unashed wafers. Further research is needed in the area of nickel removal.

Table I. A series of experimental cleaning sequences utilizing the Side Bowl Spray Post and ramped rinsing. Surface concentration in units of $10^{10}/cm^2$.

Element Analysis Method	Na VPD	Al VPD	Ti TXRF	V TXRF	Cr BOTH	Fe TXRF	Ni TXRF	Cu TXRF	Zn VPD
Control / Prime	<10	25	<1	<1	<1	1	1	300	<2
Control / Ashed	570	102k	15	15	950	200	9	150	26
SBSP2 / Ashed	<10	26	<1	<1	<1	1	5	<1	<2
SBSP7 / Ashed	<10	<5	<1	<1	<1	2	5	<1	<2
SBSP8 / Prime	<10	<5	<1	<1	<1	<1	5	<1	<2
SBSP8 / Ashed	<10	<5	<1	<1	<1	<1	5	<1	<2
SBSP9 / Ashed	52	<5	<1	<1	<1	1	5	<1	2.2
SBSP10 / Ashed	<10	<5	<1	<1	<1	2	5	<1	<2
SBSP11 / Ashed	<10	<5	<1	<1	<1	1	4	<1	<2
SBSP13 / Ashed	<10	<5	<1	<1	<1	2	4	<1	<2
B Clean / Ashed	<10	<5	<1	<1	<1	<1	4	<1	<2

Surface roughness, as determined by "haze" measurements in a CENSOR ANS wafer inspection system, were 0.112 ppm for the control wafer, 0.117 ppm after the standard B Clean and 0.112 after the SBSP B Clean. The haze added by the SBSP clean is apparently less than 1/5 of that added by the standard clean.

Particle removal efficiency for two runs of 25 wafers each is shown in figure 7. The modified B clean with ramped rinsing averaged 98% removal of particles larger than

0.15 μm. The overall particle performance for 10 runs of 25 wafers each is shown in Figure 8. Overall, the cleans averaged removing 6 particles/wafer for each clean. In reality, the first clean removed the contamination from the "as received" wafers and subsequent cleans averaged particle neutral (neither adding nor removing particles).

SUMMARY

The use of centrifugal force to reduce the thickness of the carry over layer between rinse steps and improved distribution of the rinse sprays greatly improved the theoretical and experimental rinsing efficiency in an acid processor. These changes allowed a 25% decrease in process time and water usage while maintaining metal removal performance, improving particle performance and reducing surface roughening. Water usage in the process was less than 10% that used for immersion "over flow" rinsing.

ACKNOWLEDGMENTS

The author would like to thank Brent Carlson for helpful discussions and significant laboratory work in testing these ideas.

REFERENCES

1. G. Ching and R. Murtha, "Cost of Ownership Comparisons for 200 mm Versus 150 mm Immersion Wet Cleaning Equipment", Proc. Microcontamination 1993, San Jose, CA, 1993, p. 378.
2. R. Spearow, J. Rosato and C. Helms, "Studies of Rinse Efficiencies in Wet Cleaning Tools", Extended Abstracts of Semiconductor Cleaning Technology / 1993, J. Ruzyllo and R. Novak, Editors, Vol 93-2, p. 580, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1993).
3. A. Tonti, "A Simple Model For Rinsing", in Proc. 2nd Int. Symp. on Cleaning Technology in Semiconductor Device Manufacturing, Eds. J. Ruzyllo and R. Novak, The Electrochemical Soc., PV 92-12, pp. 41-47, 1992.
4. J.S. Kirkaldy and D. J. Young, "Diffusion In The Condensed State", The Institute of Metals, London 1987, p 5.
5. Ionic salt rinsing data courtesy of Marc Meuris, IMEC. To be published.

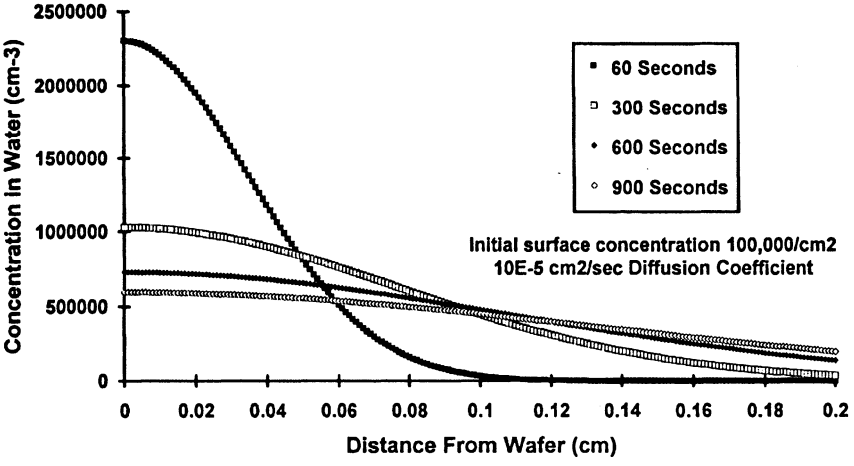


Figure 1. The calculated concentration distribution of molecular contaminants that have diffused away from the surface of the wafer into the rinse water for diffusion times of 60, 300, 600 and 900 seconds. The calculation assumes a stagnant bath and a diffusion coefficient of 10^{-5} cm^2/sec, typical of ionic and molecular species (4).

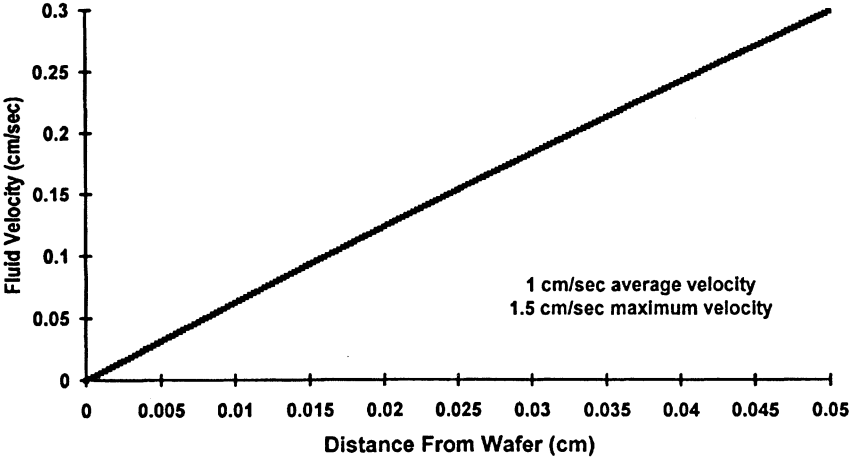


Figure 2. The fluid velocity profile near the wafer in an overflow rinse bath with an average fluid velocity of 1 cm/sec.

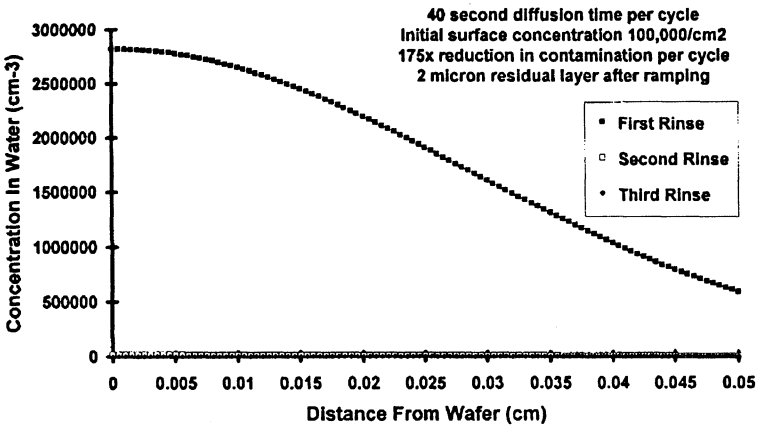


Figure 3. The calculated concentration of contaminants that have diffused away from the surface of the wafer in the rinse water for a diffusion time of 40 seconds. During a 20 second ramp at 500 rpm, all but 2 μm of this layer would be is spun off of the wafer by centrifugal force. The residual contamination in this 2 μm layer 0.57% of the initial surface contamination.

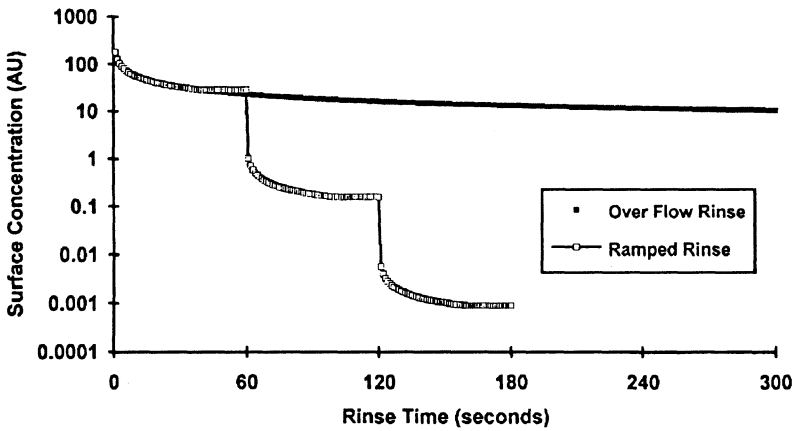


Figure 4. The aerial concentration in a 2 μm thick layer versus rinse time for a stagnant bath and ramped rinsing. Each 1 minute ramped rinsing cycle consisted of a 40 second period to allow contaminants to diffuse into the boundary layer followed by a 20 second ramp to remove the bulk of the boundary layer. Calculations were based on an initial surface concentration of 5000/cm^2, a diffusion coefficient of 10^{-5} cm^2/sec and a 2 μm residual layer remaining after the ramp.

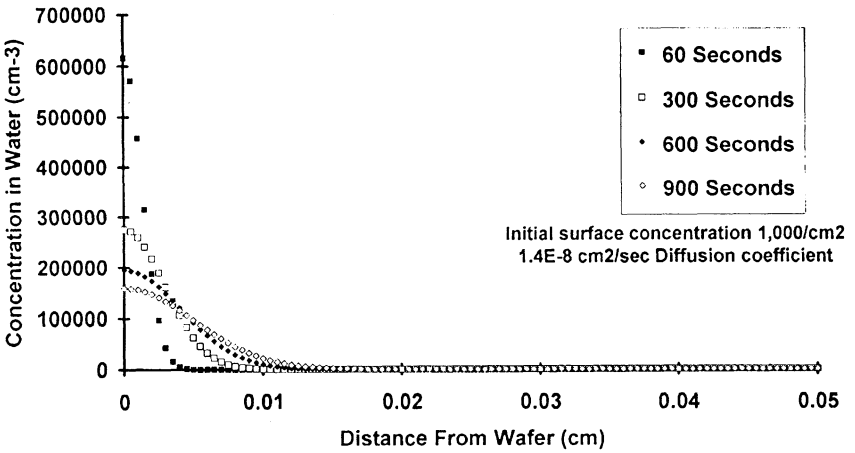


Figure 5. The calculated concentration of 0.3 μm particles that have diffused away from the surface of the wafer in stagnant rinse water for diffusion times of 60, 300, 600 and 900 seconds.

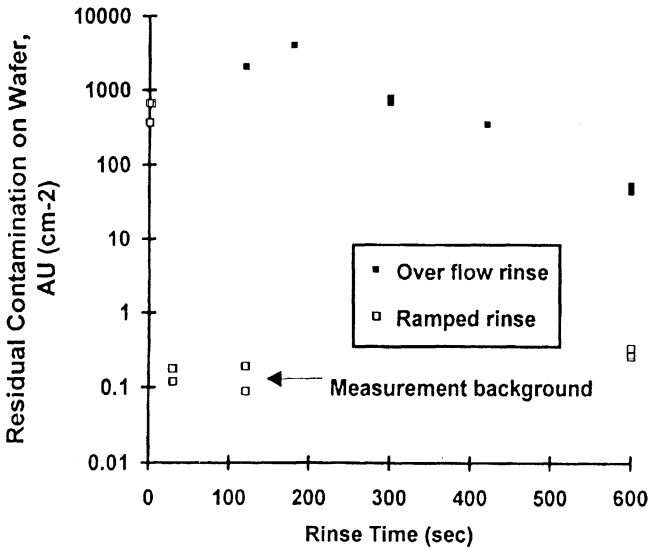


Figure 6. Experimental rinsing data for an ionic salt in an over flow rinse tank and for sodium in an acid processor utilizing ramped rinsing (5).

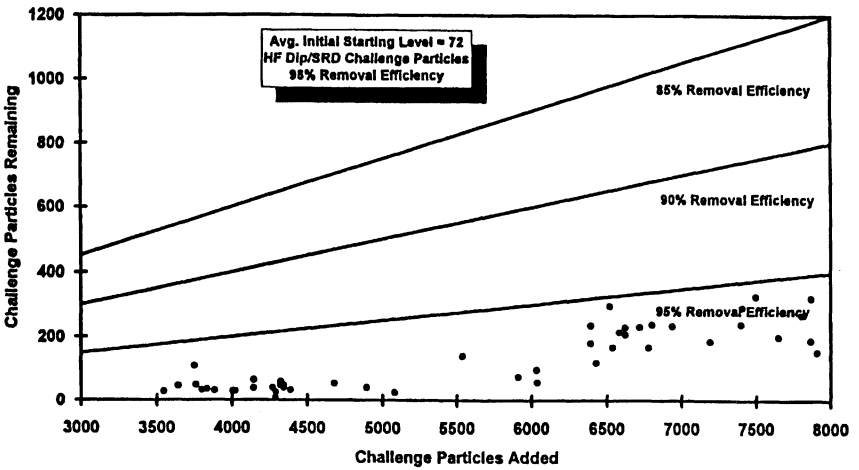


Figure 7. Particle removal efficiency of the MERCURY MP B Clean utilizing the Side Bowl Spray Post and ramped rinsing for 2 runs of 25, 150 mm wafers. The x axis indicates the number of "HF Last" challenge particles larger than 0.15 μm added to a wafer. The y axis indicates the number of these added challenge particles remaining on the wafer after the clean.

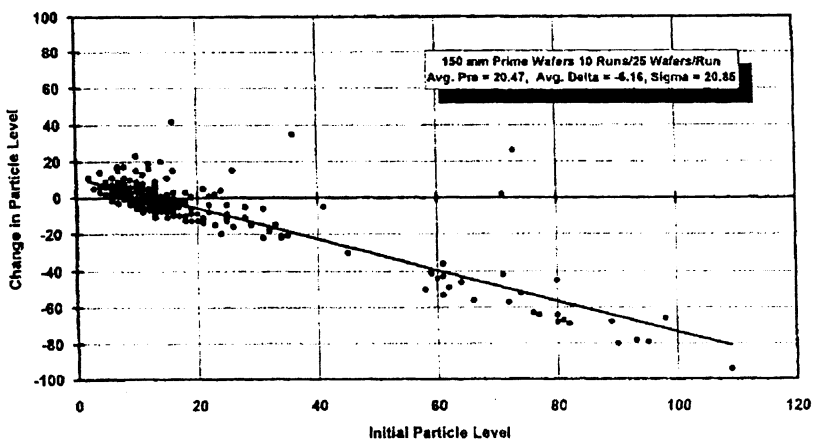


Figure 8. Particle performance of the MERCURY MP B Clean utilizing the Side Bowl Spray Post and ramped rinsing for 10 repeated runs on a lot of 25, 150 mm wafers. Large particle reductions in the lower right quadrant represent the removal of initial contamination during the first cleaning cycle.

LIQUID HF PROCESSING

ASPECTS OF THE ETCHING OF SILICON DIOXIDE IN FLUORIDE-BEARING SOLUTIONS

C. W. Pearce[1] and B. C. Chung[2]
AT&T Microelectronics, Allentown, PA 18103[1]
Bell Laboratories, Princeton, NJ 08542-0900[2]

This paper reviews existing literature and presents new data on certain aspects of the etching of silicon dioxide in fluoride bearing solutions. Specifically, the role of glass doping on the etch kinetics and the role of ammonium fluoride as a buffering agent are explored. For example, the etch rate of a BPSG film was found to decrease with increasing ammonium fluoride concentration.

INTRODUCTION

Because of its simplicity and versatility, wet etching is widely used and assumes an important role in IC fabrication. It is repeatedly used for the delineation of patterns and removal of impurities from wafer surfaces. The nature of the surface preparation, prior to the growth of oxides, is also of great importance, and is being extensively investigated for submicron devices and is affected by the nature of the HF solution. Depending on the etch requirements, various concentrations of HF or HF buffered with ammonium fluoride (NH_4F) are used. The etching reaction is sensitive to various parameters such as: temperature, etch time, and concentration of etchant. The etch process typically has a narrower window compared to other wet cleaning techniques used in IC processing, necessitating tighter process control. With increasing circuit density and decreasing feature sizes and in spite of recent extensive characterization of gas phase techniques involving anhydrous HF in the presence of water or alcohol vapors (1, 2), the etching of silicon dioxides in acidic, aqueous fluoride-bearing solutions will continue to play an important role in the IC manufacture.

Numerous papers are available in the literature regarding the characteristics of the etch when using different types of oxides, dopant levels, chemical concentrations and temperature; these include several excellent review articles (3, 4). Also several studies have been reported elucidating the etching reaction itself (5, 6, 7, 8, 9, 10, 11, 12). This paper gives an overview of the etching of doped and undoped silicon dioxides in hydrofluoric acid or mixed with ammonium fluoride.

PROPERTIES OF HF

Anhydrous HF

HF, a simple binary compound, is a strong acid and powerful solvent in the anhydrous state. It is extremely hygroscopic, dissolving readily in water with a large amount of heat evolution. The self ionization of anhydrous HF is approximated in its simple form as:

$$2HF = H_2F^+ + F^- \qquad [1]$$

Based on the conductivity measurements, the ionization constant is reported to be 1.0×10^{-12} and it is postulated that this value could be lowered through the further exclusion of moisture (13). It is interesting to compare this value to the ionization constant of water, which is 1.0×10^{-14}. As in most protonic acids, the ionized species are very likely stabilized by hydrogen bonding. In the gaseous phase HF molecules are associated as dimers, tetramers and hexamers. Comprehensive physical properties are published elsewhere (14).

Aqueous HF

Dissolved in water , HF becomes a weak acid and dissociates as:

$$HF = H^+ + F^- \text{ and} \qquad [2]$$

$$HF + F^- = HF_2^- \qquad [3]$$

The equilibrium constants for the dissociation are defined by the following equations:

$$[H^+][F^-] = K_1[HF] \qquad [4]$$

$$[HF][F^-] = K_2[HF_2^-] \qquad [5]$$

The dissociation constants have been measured by a number of different workers and, in the concentration range of 1 M solutions, K_1 and K_2 values are 1.3×10^{-3} and 1.04×10^{-1} respectively (15, 16, 17). Unlike most of the other protonic acids, the HF_2^- ion is formed in hydrofluoric acid at high concentrations and the F^- ion concentration is negligible. Several studies using IR, NMR and x-ray crystallography and phase-rule investigations point to the existence of higher polymeric $H_2F_3^-$ and $H_3F_4^-$ anions at high concentrations. In dilute solutions, F^- is dominant and the HF_2^- ion is negligible (6, 11). When the acidity of hydrofluoric acid is compared, as a function of concentration, to strong acids such as hydrochloric acid, the hydrofluoric acid behaves in a similar way to the hydrochloric acid solutions of lower concentration. For example, the acidity of 1

M hydrofluoric acid will be approximately the same as that of 0.1 M hydrochloric acid.

Buffered Hydrofluoric Acid Solutions

Hydrofluoric acid buffered with its conjugate base F^- in the form of NH_4F is commonly used for etching silicon dioxide. The NH_4F reacts with HF according to the following reaction, producing a high concentration of HF_2^- ions.

$$NH_4F + HF = NH_4^+ + HF_2^- \qquad [6]$$

A buffer solution is a mixture of a weak acid and its conjugate base. If hydrogen ions are generated, they react with F^- to increase the amount of HF and if hydrogen is consumed, hydrofluoric acid dissociates to give more hydrogen ions, thus minimizing a change in the hydrogen ion concentration (pH). The buffer capacity is a measure of the amount of strong acid or base that is required to change the pH by a given amount. The larger the buffer capacity, the larger the amount of acid or base is required. At high HF concentrations, the pH of the solution is not easily varied due to the buffering action of water.

The concentrations of HF_2^- vs. pH have been calculated for different concentrations of NH_4F (6). The pH of 7:1 NH_4F/HF mixtures is calculated to be approximately 4. The pH of 1 M HF solution is approximately pH 1.

ETCHING OF SILICON DIOXIDE

Anhydrous HF does not appreciably etch silicon oxide at room temperature. Weston and Mattox (18) investigated the etch process using gaseous HF at reduced pressures and found that the reaction did not occur until the temperature reached 80°C. An enhanced etching took place under negative photoresist. They postulated that HF_2^- was formed as a result of interaction of HF with carbonyl groups in the photoresist (18). More recently Wong et al (19) reported that as the temperature is raised, the etch rate of undoped oxides decrease, reducing to 50% of the original etch rate at temperatures above 40°C (19). It is known that the adsorbed layer of water on the surface is rapidly removed with a rise in temperature. The etching reaction observed with anhydrous HF gas in a nitrogen atmosphere is hypothesized to be due to the interaction with moisture adsorbed on the SiO_2 surface, resulting in the ionization of HF into HF_2^- ions (20, 1). All these observations indicate that anhydrous HF needs to form hydrofluoric acid with water, which then etches silicon dioxide. Thus, the presence of water (even in trace amounts) is considered to be necessary for the reaction of HF with silicon dioxide to occur.

Tertykh and his coworkers (21) observed by IR spectroscopy the etch reaction of gaseous HF at 650°C with silica surfaces and identified a four-center cyclic

complex as an intermediate species. The silanol group, complexed with HF, was stable at room temperature when in vacuum.

[7]

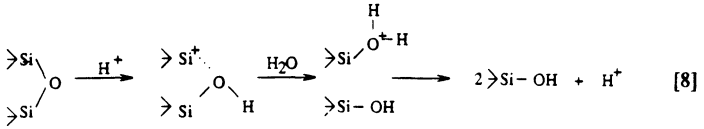
Depending on the required application, different thermal oxidation techniques are used. If sodium ion contamination is a concern, the oxidation is carried out in the presence of HCl. The oxidation in dry oxygen is slow and thus used to grow thin oxide layers. In contrast, steam or wet oxidation techniques are used to grow thick oxide layers.

The properties of oxides such as refractive index, density, hydrogen content, etc. are dependent on the experimental conditions used in the oxide growth. Figs. 1 and 2 illustrate the hydrogen content determined by SIMS for thermal oxides grown by high pressure oxidation (HIPOX) and by dry oxidation. These concentrations of bulk hydrogen are similar to the reported values in the literature (22). A higher hydrogen content is observed for the HIPOX oxide. It is well known that hydrogen, introduced in the form of water, remarkably affects thermal growth and the properties of silicon dioxide (22). However, there is a dearth of information about how the hydrogen in the silanol form affects the physiochemical properties of the oxide such as etch rate.. When the etch rates were compared in a buffered HF solution, a consistently higher etch rate was observed for the HIPOX oxide, as shown in Fig. 3.

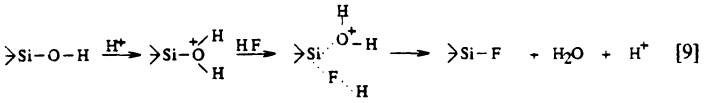
Numerous studies using IR spectroscopy, NMR, SIMS, and radioactive analysis demonstrate that the hydrogen atom is incorporated into the silicon dioxide network as SiOH and SiH (22, 23, 24, 25, 26,27).

The role of water in the etching process has been established and the presence of a silanol group preexisting in the oxide is considered to augment the etching reaction, thus explaining the dependence of etch rate on the manner of growth. Thus, it would appear that the etch rate is not simply related to the hydrogen content as summarized in Table I, but does depend explicitly on its form in the oxide (i.e. SiOH).

The etching mechanism of silicon dioxide in aqueous solutions has been postulated to be initiated by the cleavage of the siloxane bond, forming a silanol group. In acidic fluoride bearing solutions, the silanol group is to undergo a nucleophilic substitution by such nucleophiles as HF or HF_2^-, replacing the OH group with F.



[8]



[9]

Born, et al (11) considered the chemical adsorption of H^+ and first order rate dependence on HF_2^-, when they examined the etch rate in HF and HCl mixtures. In dilute solutions of hydrofluoric acid, an etch rate increase could not be confirmed by the addition of HCl. The work by Kline, et al indicates that the etch kinetics is of the first order dependence on HF concentration rather than HF_2^- (9). They propose a direct complex formation of the HF molecule with siloxane groups, similar to the gas phase etch reaction. On the other hand, the etch rate for thermal oxides is reported to be dependent on HF_2^- ion and HF (6, 10). The maximum etch rate is realized in a given HF and NH_4F solution, when the concentration range of HF and NH_4F is equimolar (10). As the following reaction equation indicates, any additional amount of NH_4F does not increase the formation of H_2F^- ion appreciably.

$$HF + NH_4F = NH_4^+ + HF_2^- \qquad [10]$$

For doped oxides, the etching is more complicated, and an additional etch mechanism appears to be present. The etch rate of P doped oxides, as shown in Fig. 4, increases with increasing phosphorus concentrations (28) in a given concentration of etch solution, and is much higher, compared to undoped CVD oxides (Table I). Solutions buffered with NH_4F differ from the aqueous case in that increased availability of the hydrogen difluoride increases the etch rate of undoped oxides by about a factor of one half to an order of magnitude depending on the HF concentration or HF_2^- concentration. The etch rate differences of a thermal oxide and a doped oxide, such as BPSG, in the same etching solution are illustrated in Fig. 5. While the etch rate for the thermal oxide remains constant after the equimolar additions of NH_4F, the etch rate for the BPSG continues to decrease. Unlike the thermal oxide the etch rate of the P doped oxide or BPSG film decreases as NH_4F is added to hydrofluoric acid.

The etch rate differences of P or B doped oxides have been hypothesized to be a result of an electron donating or withdrawing from P and B respectively (8). If the etching of silicon dioxides is initiated by the cleavage of siloxane groups, followed by the formation of a silanol group before the substitution of F occurs at the silicon atom, the concentration of water present and the acidity of the solution would affect the etching of doped oxides greatly. The higher etch rate of P doped glasses is believed to be related to the more easily cleaved Si-O-P bonds due to its strong affinity to water and protonation in strong acidic medium, resulting in rapid dissolution of the phosphorus pentoxide . The relatively weak acidity and high content of NH_4F that might affect the hydration and solubility of phosphorus oxide is believed to lead to the observed lowering of the etch rate for these glasses. There is at least one study linking the acidity to etch rate on P doped glasses (12).

DISSOLVED SILICA IN HF AND BHF SOLUTIONS

When silicon dioxides are etched in hydrofluoric acid or hydrofluoric acid solutions, buffered with ammonium fluoride, hexafluorosilicates are formed. The overall reactions are generally expressed as;

$$6HF + SiO_2 = H_2SiF_6 + 2H_2O \quad \text{and} \qquad [11]$$

$$NH_4F + 4HF + SiO_2 = (NH_4)_2SiF_6 + 2H_2O \qquad [12]$$

The stability of the hexafluorosilicate ion is not well known, especially in relation to hydrolysis and condensation into larger molecules. Aqueous reactions involving the etching solution and etch product are in equilibria, and these equilibria are affected by the concentrations of the chemical species and temperature. The hydrolysis of $SiF_6^{=}$ in hydrofluoric acid has been studied using NMR techniques (31). It is reported that $SiF_6^{=}$ is partially hydrolyzed into $SiF_4(OH)_2^{=}$

$$SiF_6^{=} + 2H_2O = SiF_4(OH)_2^{=} + 2HF \qquad [13]$$

In phosphorus-doped oxides, the majority of phosphorus is present in the pentavalent form as P_2O_5 and some in the trivalent form as P_2O_3. They are identified using ion chromatography (29). For boron doped oxides, the boron is likely to be present in the trivalent state as B_2O_3.

When etched in hydrofluoric acid solutions phosphorus oxides would result in the corresponding acids, and the boron as boric acid. Fluorinated phosphate ions are hydrolyzed in dilute acidic solutions (30).

SUMMARY

A brief overview of essential chemical properties of HF and BHF, relating to the etching aspects of doped and undoped silicon dioxides has been presented. The etching of silicon dioxides is hypothesized to be initiated by the cleavage of the siloxane group, followed by the replacement of the silanol group with a fluoride in a nucleophilic substitution reaction. Several kinetic models have been reported. However, little is known about the transition state of the etching reaction. One of the factors that affect the etch rate is the dopant concentration in the oxides which influences the etch rate both in HF and BHF. While undoped oxide etch rates are increased with an increase of NH_4F concentration, in contrast, the etch rate of phosphorus doped oxide decreases . This difference is considered to be associated with the difference in the acidity of the etching solution or the availability of water for hydration and protonation, playing a greater role for the doped oxides.

Etch selectivity and post etch cleanliness are important considerations to be made. One of the major contaminants in an etch process is the accumulation of hexafluorosilicates, which are known to hydrolyze in aqueous medium, and little is known about the fate of the hydrolyzed silicates in terms of colloidal particle generation.

REFERENCES

1. C. R. Helms, B. E. Deal and M. A. McNeilly, Extended Abstract, ECS Fall Meeting, 807 (1991).
2. J. Ruzyllo, K. Torek, C. Daffron, R. Grant and R. Novak., J. Eletrochem. Soc., 140, L64 (1993).
3. W. Kern, RCA Reviews 47, 186 (1986).
4. W. Kern, Symposium Proceedings, Electrochemical Society, H. G. Hughes and J. J. Rand, Editors,1-18 (1976).
5. A. A. Blumberg and C. S. Stravirinon, J. Electrochem Soc., 64, 1438 (1960).
6. J. S. Judge, J. Electrochem. Soc., 118, 1773 (1971).
7. H. S. Fogler, et al, Chem. Eng. Sci., 30, 1325 (1975).
8. H. H. Born and M. Prigogine, J. Chim . Phys., 76, 538 (1979).
9. W. E. Kline, and H. S. Fogler, Ind. Eng. Chem. Fund., 20, 155 (1981).
10. H. Kikuyama, N. Miki, K. Saka, J. Takano, I. Kwanabe, M. Miyashita and T. Ohmi, IEEE Transactions on Semiconductor Manufacturing, 4, 26 (1991).
11. S. Verhaverbeke, PhD Thesis, (1993), Katholieke Unversiteit, Leuven, Belgium.
12. D. J. Monk, D. S. Soane and R. T. Howe, J. Electrochem. Soc., 140, 2339 (1993).
13. H. H. Hyman and J. J. Katz, Non-aqueous Solvent Systems, p. 47, T. C. Waddington, Editor, Academic Press, London and New York, (1965).

14. Gmelin Handbook of Inorganic Chemistry, Springer-Verlag, New York, 1982.
15. S. Ahrland, R. Larsson, and K. Rosengren, Acta Chem. Scand.,10, 705 (1956).
16. E. W. Bauman, J. Inorg. Nucl. Chem., 31, 3155 (1969).
17. R. E. Mesmer, and C. F. Baes, Inorg. Chem., 8, 618, (1969).
18. D. F. Weston and R. J. Mattox, J. Vac. Sci. Technol., 17, 466 (1980).
19. M. Wong, M. M. Moslehi and R. A. Bowling, J. Electrochem. Soc., 140, 205 (1993).
20. N. Miki, H. Kikuyama, I. Kwanabe, M. Miyashita and T. Ohmi, IEEE Transactions on Electron Devices, 37 (1), 107 (1993).
21. V. A. Tertykh, A. A. Chuiko, V. V. Pavolov and V. M. Ogenko, Dokl. Chem. Proc. Acad. Sci., USSR, 202/207, 791 (1971).
22. A. G. Ravesz, J. Electrochem. Soc., 126, 122, (1979).
23. K. H. Beckman,and N. J. Harrick, J. Electrochem. Soc., 118 (4), 614 (1971).
24. C. W. Magee and E. M. Botnick, J. Vac. Sci. Technol., 19, 47 (1981).
25. M. A. Briere and D. Braunig, IEEE Trans. Nucl. Sci., 37, 1658 (1990).
26. D. H. Levy and K. K. Gleason, J. Electrochem. Soc., 140, 797 (1993).
27. N. Nagashima, J. Appl. Phys., 43, 3378 (1972).
28. A. S. Tenney and M. Ghezzo, J. Electrochem. Soc., 120, 1091 (1973).
29. M. C. Hughes and D. R. Wonsidler, J. Electrochem. Soc., 134, 1488 (1987).
30. J. R. Van Wazer, Phosphorus and Its Compounds, Vol. 1, Chapter 13, Interscience Publishers, Inc., New York (1966).
31. P. M. Borodin, and Nguen Kim Zao, Russian Journal of Inorganic Chemistry, 17 (7), 959 (1972).
32. R. A. Levy et al, J. Electrochem. Soc., 132, 1472 (1985).

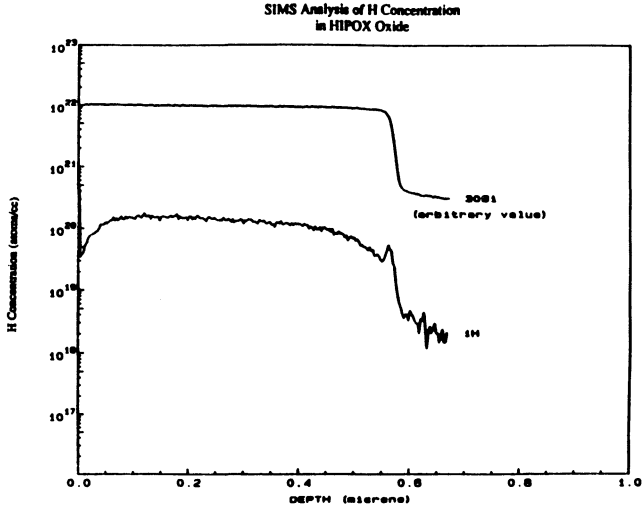

SIMS Analysis of H Concentration
in HIPOX Oxide
H Concentration (atoms/cc)
DEPTH (microns)
30Si
(arbitrary value)
1H

Fig. 1

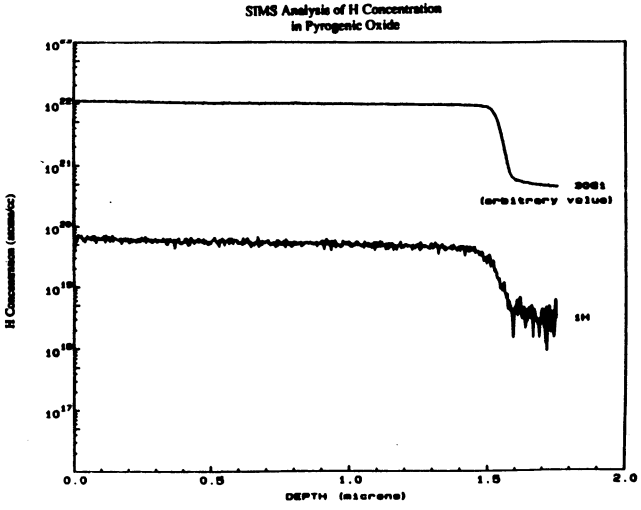

SIMS Analysis of H Concentration
in Pyrogenic Oxide
H Concentration (atoms/cc)
DEPTH (microns)
30Si
(arbitrary value)
1H

Fig. 2

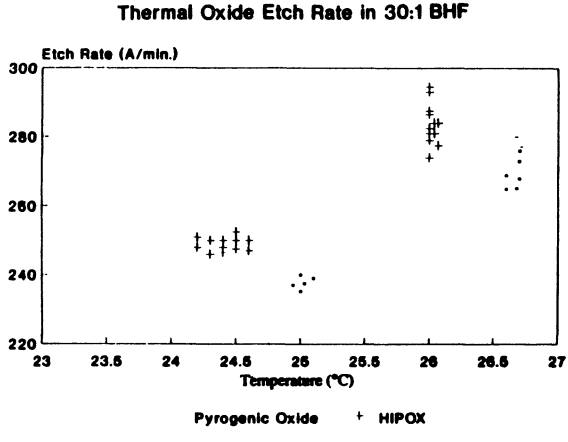

Thermal Oxide Etch Rate in 30:1 BHF
Etch Rate (A/min.)
300
280
260
240
220
23
23.5
24
24.5
25
25.5
26
26.5
27
Temperature (°C)
Pyrogenic Oxide
HIPOX

Fig. 3

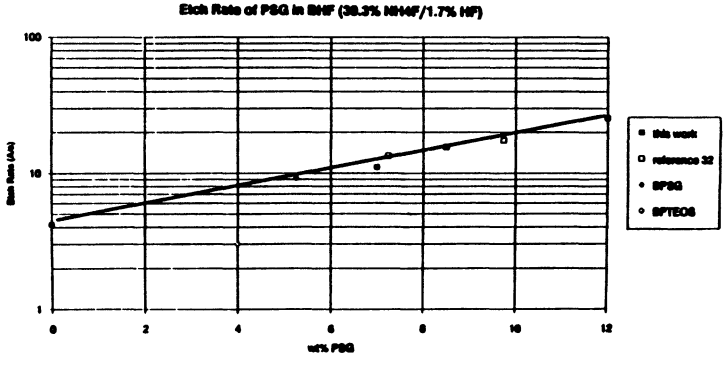

Etch Rate of PSG in BHF (30.3% NH4F/1.7% HF)
100
10
1
0
2
4
6
8
10
12
wt% PSG
this work
reference 32
BPSG
BPTEOS

Fig. 4

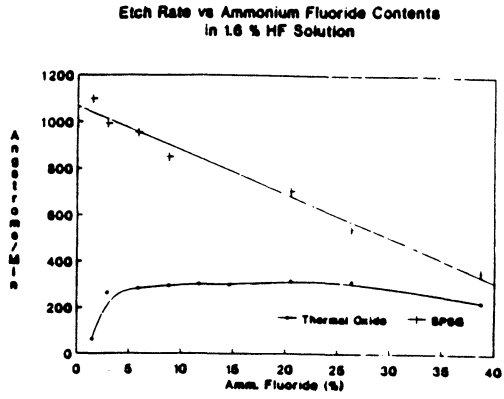


Fig. 5

Table I
H Content In Silicon Oxides

Type of Oxides	Oxid. Temp.	H^1 Conc. (atoms/cm^3) Bulk	Surface	Etch Rate^2 (Å/min.)
HIPOX Field Oxide	900°C	~2 x 10^{20}	~5x10^{21}	208.3±0.6
Standard Oxide	900°C	~2x10^{20}	~5x10^{21}	195.5±0.6
Pyrogenic Field Oxide	900°C	~7x10^{19}	~5x10^{21}	195.5±0.9
Dryox Field Oxide	900°C	~6x10^{19}	~8x10^{21}	185.8±4.0

Note: 1) Determined by SIMS analysis. 2) Etch Temp = 23.5°C

Table II
Etch Rates (angstrom/min) of Various Oxides
In Different HF and BHF Solutions

Type of Oxides	HF (0.6%)	HF (1.8%)	HF (39.3%:1.7%)	BHF (37.3%:6.8%)	BHF
Thermal Oxide	30	140	200	270	1075
TEOS (densified)	140	-	700	475	1950
3 % P-Glass	1864	-	4948	1969	17942
BPSG	225	850	1600	560	1680

MODELLING OF THE HYDROGEN PASSIVATION KINETICS OF SI IN DILUTE HF SOLUTIONS

S. Verhaverbeke* , M. Meuris, H. Schmidt, P. Mertens, M. Heyns

IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

Abstract

The kinetics of the H-passivation is modelled as a combination of the etching of the chemical oxide and the etching of the first monolayer of Si. From this, the increase in selectivity when using very dilute HF solutions can be explained.

Introduction

In a recent publication, we have shown that the etched thermal oxide and TEOS oxide thickness after complete native oxide removal is reduced when lowering the fluoride concentration (1). In this paper we have modelled the kinetics for removing the native oxide.

Model for the removal of the native oxide

The removal of the native oxide in HF solutions can be modelled as follows : first the native oxide is etched and subsequently, the first monolayer of Si is etched to obtain the H-passivation (2). This is schematically shown in fig. 1.
Therefore, the time needed to obtain the passivation of the Si surface can be modelled as :

$t_p = t_{ox} + t_{1Si}$

with t_p : time to passivation
t_{ox} : time to etch the native oxide
t_{1Si} : time to etch 1 monolayer of Si

In order to study the passivation kinetics, it is thus necessary to study the etching kinetics of both SiO_2 and Si.
Before studying the etching kinetics, it is necessary to investigate the equilibria in dilute HF solutions, in HF/HCl and in Buffered HF solutions.

Equilibria in HF solutions

In dilute HF solutions the following equilibria are well established :

$$HF = H^+ + F^- \qquad (r_1)$$

$$HF + F^- = HF_2^- \qquad (r_2)$$

For the equilibrium constants K_1 and K_2 of respectively reaction r_1 and r_2, the values of $6.85*10^{-4}$ mol/l and 3.963 l/mol will be used (3). These are the equilibrium constants at

---

* presently at Prof. Ohmi's Laboratory, Tohoku University, Sendai, Japan

25 °C and corrected for zero ionic strength. The ionic strength in dilute HF solutions is very low and therefore these values can be used.

In general, it has been well accepted that other equilibria exist as well, but usually it is thought that these other equilibria only come into play at higher concentrations of HF. However, L.J. Warren (4) already showed in 1971 that the dimerisation reaction of HF cannot be neglected and he found the equilibrium constant K_3 for the reaction

$$2HF = (HF)_2 \qquad (r_3)$$

to be K_3 = 2.7 l/mol.

From these known equilibrium constants, together with the mass law and charge conservation laws, the composition of the solutions can be calculated. The different species are HF, F^-, HF_2^-, $(HF)_2$ and H^+.

A fraction α can now be defined as the ratio of the molarity of each species divided by the total fluoride content $C_F = [HF] + [F^-] + 2[HF_2^-] + 2[(HF)_2]$:

$\alpha[HF] = [HF] / C_F$

$\alpha[F^-] = [F^-] / C_F$

$\alpha[HF_2^-] = [HF_2^-] / C_F$

$\alpha[(HF)_2] = [(HF)_2] / C_F$

$\alpha[H^+] = [H^+] / C_F$

In fig. 2 α of the various species is shown as a function of the molar concentration of fluoride (in mol/l). From these graphs we can see that the HF is indeed a very weak acid. Only below 0.05 M, HF becomes strongly dissociated, which is according to the Ostwald law, stating that a weak acid becomes strongly dissociated upon strong dilution. The dissociation becomes increasingly important once below 0.25 M HF. This is important in applications such as where HF is being reprocessed. Above 0.25 M the concentration of the F^- and the HF_2^- does not drastically change. However, the HF becomes now partially dimerised and shows a maximum at 0.05 M, which is 0.1 %-weight.

Equilibria in diluted HF/HCl solutions

When HCl is added to diluted HF solution, the equilibria of the various components in the HF solution shift drastically. In these calculations, always 0.5 M HCl was added to the HF solutions. In such solutions, the equilibrium of reaction r_1 is completely shifted to the left side, leaving only HF in the solution. Because the F^- concentration becomes negligible, also reaction r_2 is shifted to the left, preventing the formation of HF_2^- . Therefore, in case the dimerisation reaction is not taken into account, the solution will exist only of HF molecules regardless of the total fluoride atom concentration. If the dimerisation reaction is taken into account, the only 2 species present are HF and $(HF)_2$. Their fraction a as defined earlier, is given in fig. 3.

It can be concluded that the composition of HF/HCl solutions is simple and that it offers excellent possibilities to study the basic reaction phenomena of HF and $(HF)_2$ without the presence of HF_2^- or F^-.

Finally, in all these mixtures, since the HCl concentration is held constant, the pH is also constant and is equal to 0.3 .

Equilibria in HF solutions as a function of pH

The previous calculations the composition and the pH were calculated as a function of the fluoride atom concentration added to the solution. One can also perform the calculation of α, given a certain fluoride molarity, as a function of the pH. The total fluoride concentration was taken as the fluoride concentration in traditional buffered HF solutions.

The result of these calculations is shown in fig. 4.

From this graph it is seen that at low pH, the HF is not dissociated and is partially dimerised. At intermediate pH, the HF is mainly transformed into HF_2^- and at high pH, the mixture contains predominantly the F^- ion.

Etch rate study and modelling of SiO_2

From the etch rate measurements in HF/HCl solutions and in HF solutions as a function of the fluoride concentration, a general model of the etch rate of SiO_2 in HF can be derived by fitting the experimental data to the calculated species in the HF solution (5). The best fitting for the measured SiO_2 etch rate as a function of the calculated species in the HF-solution resulted in the following etch rate description (in nm/min !) :

$$R = 25.7[(HF)_2] + 5.53[(HF)_2]^2 + 99.2 \pm 62.5[HF_2^-] + 206.8 \pm 123.5 * [HF_2^-] * \log([H^+]/[HF_2^-])$$

The active etching species are thus the dimer of HF and the HF_2^- ion.

Kikuyama et al. (6) have studied the etching of SiO_2 in buffered HF solutions. Buffered HF solutions typically have a pH of around 4 to 5. From fig. 4, it can be seen that at these pH values almost uniquely HF_2^- and F^- are present in the solution. Therefore, since F^- does not etch SiO_2 (6), buffered HF solutions provide the best medium for determining the coefficients of $[HF_2^-]$. When taking the coefficients from Kikuyama et al. (6) for the etching by HF_2^- and the coefficients found by us from the HF/HCl solution (5), the following etch rate description results (in nm/min !) :

$$R = 25.7[(HF)_2] + 5.53[(HF)_2]^2 + 128.2[HF_2^-] + 38.88 * [HF_2^-] * \log([H^+]/[HF_2^-])$$

Both these fitting together with the measured data points is shown in fig. 5 on the relative etch rate graph. The relative etch rate graph is a graph of the etch rate per mole of fluoride as a function of the total fluoride concentration.

Etch rate study and modelling of Si

In order to understand more about the etching of the first monolayer of Si, the etching of Si in dilute HF was investigated. In order to do this, the etch rates of poly-Si layers on top of SiO_2 were measured. For these layers the thickness can be measured with light reflectance techniques. It is believed that even if the etching of poly-Si would not exactly be the same as the etching of monocrystalline Si, these measurements will certainly give an

indication on the Si etching mechanism. Moreover, even the etching of bulk monocrystalline Si will almost certainly not be the same as the etching of the first monolayer. However, it is thought that the etching of the first monolayer of Si is at least proportional to the etching of poly-Si.
The etch rate of poly-Si was measured in dilute HF mixtures with and without the addition of 0.5 M HCl.
The obtained etch rates are shown in fig. 6.

Also the etch rate of poly-Si in standard buffered HF (BHF) was measured. Standard buffered HF contains 7 parts NH_4F (40%-weight) and 1 part HF (48%-weight). This mixture has a pH of about 4.5. In this etch mixture, poly-Si has an etch rate of 0.265 nm/min, which is 7 times higher than the most concentrated HF solution which was investigated (6 M HF) as can be seen from the absolute etchrates in fig. 5. From this, we can conclude that the HF_2^- is certainly an important species in the etching of poly-Si, since at these pH values, the HF_2^- is the most abundant species in the BHF. When adding NH_4OH to the BHF, at first the etch rate increased, but upon further NH_4OH addition, the etch rate decreases again. From fig. 4, it can be seen that in such solutions, only F^- is left. Therefore, it can be concluded that the F^- is etching the Si at much reduced rates compared to HF_2^-.
The poly-Si etch rate can now again be modelled as a function of the species present in the solution. At first, the HF/HCl mixture was modelled. In this mixture, the etch rate can best be described by the following equation :

$$R = 0.0119\,[HF] + 0.0025\,[(HF)_2]$$

The measurement points and the modelled etch rate is shown in fig. 7 on the relative etch rate graph. It must be remarked that the uncertainty on these reaction rate constants is rather large due to the few measurement points.

The relative contribution of both etching mechanisms is shown in fig. 8. This graph is only meant to give an indication, since there exists a substantial uncertainty on the reaction rate constants. However, the trend which is given in this graph stays valid. From this graph we can see that the etching by $(HF)_2$ becomes more important at higher concentrations up to 40% at concentrations of more than 6 mol/l (=12 %-weight). For very dilute HF/HCl mixtures, the etching occurs exclusively by the HF molecule. In contrast to the etching of SiO_2 (5), it is seen that for the etching of Si, the HF molecule plays an important role.

Then, the HF solution was modelled, while taking the rate constants for the [HF] and the $[(HF)_2]$ from the HF/HCl solution. In this case, we have to do this because there are not enough measurement points to do the fitting with 5 independent species. In the HF solution, the etch rate can then best be described by the following equation :

$$R = 0.0119\,[HF] + 0.0025\,[(HF)_2] + 0.0356[F^-] + 0.267[HF_2^-]$$

The measurement points and the modelled etch rate is shown in fig. 9 again on the relative etch rate graph. The same remark on the reaction rate constants as above is also valid here.

The relative contribution of the different etching species is shown in fig. 10. This graph is also only meant to show the trends when changing the concentration. From this graph we can see that the etching at high concentrations occurs through HF, HF_2^- and $(HF)_2$. For very dilute HF solutions, the etching occurs also by the F^- ion.

Kinetics study of the etching of the native oxide until passivation

When complete passivation is obtained, the surface hydrophobicity is characterized by contact angles of more than 70° (1). The loss of thermal oxide and TEOS oxide (densified at 850°C) as a function of the process to obtain a hydrophobicity of over 70° after removing the chemical oxide (a RCA oxide) was investigated. The result is shown in fig. 11. From this graph, it is seen that when the concentration of HF is lowered to 0.1% HF at roomtemperature, the thermal oxide loss can be reduced to 1.0 nm. This is comparable to the thickness of the chemical oxide which is being removed. It can be remarked that it is less than what is removed during a SC-1 treatment, where typically 2.0 nm is removed! The TEOS loss is 6.5 nm at room temperature which is in the same range as the loss during a SC-1 treatment. The process time for this HF concentration at room temperature is at least 260s. When shorter process times are needed, higher temperatures can be used.
The etch rate of thermal SiO_2 and TEOS oxide in a 0.25/1/5 $NH_4OH/H_2O_2/H_2O$ SC-1 bath at 70°C is respectively 0.195 nm/min and 0.557 nm/min.
Increasing the temperature of the HF bath (shown for the 0.5% case and the 0.1% case in fig. 11) does not increase the selectivity.

When considering the fact that the etching of the native oxide involves the etching of the chemical oxide itself and the etching of 1 monolayer of Si to obtain the passivation, the increase in selectivity can be understood. The time to passivation can be modelled as shown earlier as :

$$t_p = t_{ox} + t_{1Si}$$

where t_{ox} is the time to etch the chemical oxide and t_{1Si} is the time to etch the first monolayer of Si until the passivation is reached. A chemical oxide is typically about 1.0 nm thick (7). Considering the fact that chemical oxides are expected to be etched much faster than thermal oxides and considering the etch rate difference between oxides and Si, in a first approximation the time to etch the chemical oxide can be neglected. The time to passivation is then mainly determined by the time needed to etch 1 monolayer of Si. Indeed, if we plot the etch rates of SiO_2 and poly-Si on the same graph, fig. 12 is obtained. We can see that there is roughly a factor 1000 difference in etch rate between oxide and Si. In figure 12, it is clear that for decreasing concentrations, the relative etch rate of the poly-Si increases while the etch rate of the thermal oxide decreases. This already explains the increase in selectivity for low concentration HF solutions.
When we then approximate the time to passivation as :

$$t_p = a^* t_{1Si}$$

for a 0.05 M, a 0.25 and a 1 M HF solution, we find the best fit for a = 1/30 (assuming the thickness of 1 monolayer to be 0.2 nm). This means that the etching of the first top-monolayer of Si in order to get the passivation still occurs 30 times faster than the etching of 1 monolayer of poly-Si during a prolonged etching process. Even so, this step will still be the time limiting step since the etching of the oxide will occur at least 30 times faster than the etching of 1 monolayer of Si, whereas its thickness is only 5 times larger, i.e. about 5 monolayers.

In the above reasoning the etch rates for the chemical oxide are taken as the etch rates of thermal oxide. It is however expected that the etching of the chemical oxide goes faster than the etching of the thermal oxide.

Finally, it must be remarked that this situation changes when going to the very low concentrations as can be seen from fig. 12. In this figure we can see that the ratio between thermal oxide and poly-Si becomes only about 180 instead of more than 1000 when going to the high fluoride concentratons. Taking into account the factor 1/30, the ratio betwen the etching of the first monolayer of the Si substrate and the etching of the oxide (taken as the etch rate of thermal oxide) becomes now only 6. This means that, because the thickness of the oxide is about 5 monolayers, the t_{ox} term in $t_p = t_{ox} + t_{1Si}$ is not negligible any longer.

The same comparison can now be performed for the HF/HCl mixture. This is shown in fig. 13.

The contact angle measurements of HF and HF/HCl mixtures for 0.5% HF content are shown in fig. 14. From this figure, it is seen that there is no marked difference when the HCl is added for this concentration, well in agreement with the graphs of fig. 12 and 13.

Until now the etch rate of the chemical oxides was always investigated on a RCA type grown chemical oxide. This chemical oxide was always grown in an automatic spray tool, which sprays the chemicals on the wafer. It can be expected that the etch rate is dependent on the actual structure of the chemical oxide and especially the last monolayer, since this determines the time to passivation. The effect of this was investigated by monitoring the contact angle as a function of time in a 0.1 % HF solution on several oxides. This is shown in fig. 15. It is clear from this figure, that the nature of the chemical oxide determines the time to passivation. Already after 1 to 2 min on all chemical oxides contact angles of at least 30 ° are found. These contact angles are typical for surfaces with submonolayer coverage of oxygen (8). However, depending on the exact structure of the chemical oxide, the remaining time to reach the high degree of hydrophobicity, characterized by contact angles of 70 ° can be widely different. This can be modelled by a different *a* factor. This *a* factor represents the proportionality between the etching of the first monolayer of Si after removing the chemical oxide and the etching of 1 monolayer of bulk Si and is dependent upon the exact structure of the chemical oxide.

The following order was found for the time to passivation of the different chemical oxides, starting with the easiest to remove oxide : SC-2 > SC-1 + SC-2 : spray-tool > SC-1 > H_2SO_4/H_2O_2. This order agrees remarkably well with the H-content of the chemical oxides (9,10). This difference was only observed for the very low concentration HF (0.1% = 0.05 M). This could be due to the fact that the etching mechanism of the first monolayer of Si in HF is depending on the concentration as shown in fig. 10.

Conclusions

From the modelling of the etching of SiO2 and Si, the kinetics of the hydrogen passivation after etching the chemical oxide could be derived. This provided the insight to explain the increase in selectivity when using very dilute HF solutions. Finally, a dependence of chemical oxide growth could be seen on the kinetics.

References

1. S. Verhaverbeke, M. Iacovacci, P. Mertens, M. Meuris, M. Heyns, R. Schreutelkamp, K. Maex, J. Alay, W. Vandervorst, R. De Blank, M. Kubota and A. Philipossian, "a high-selectivity native oxide removal process for native oxide free processes", Tech. Dig. IEDM '92, p.637.
2. Y.J. Chabal, G.S. Higashi and K. Raghavachari, J. Vac. Sci. Technol. A 7 (3), 2104 (1989).
3. IUPAC, "Stability Constants of Metal Ion Complexes", Part A, Pergamon Press, Oxford, p.188 (1982)
4. L.J. Warren, Anal. Chim. Acta, 53, 199 (1971)

5. S. Verhaverbeke, H. Bender, M. Meuris, P.W. Mertens, H.F. Schmidt and M.M. Heyns, MRS spring meeting 1993, April 13-15, Vol 315, Symposium Y, Y11.2.
6. H. Kikuyama, N. Miki, K. Saka, J. Takano, I. Kawanabe, M. Miyashita and T. Ohmi, IEEE Trans. Semiconductor Manufacturing, Vol. 4, No.1, Feb. (1991)
7. T. Ohmi et al., IEEE Trans. on El. Dev., Vol 39, No. 3, March 1992, p. 537.
8. S. Verhaverbeke, J. Alay, P. Mertens, M. Meuris, M. Heyns, W. Vandervorst, M. Murrell and C. Sofield, MRS Spring meeting 1992, April 27-29, Vol. 259, pp. 391-398.
9. T. Hattori et al., J. Vac. Sc. Tech. , August 1993, to be published.
10. H. Ogawa et al., Appl. Phys. Ltts., August 1992.

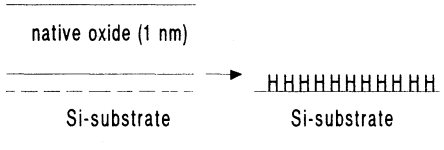


Figure 1 : Removal of the native oxide until the Si surface is passivated.

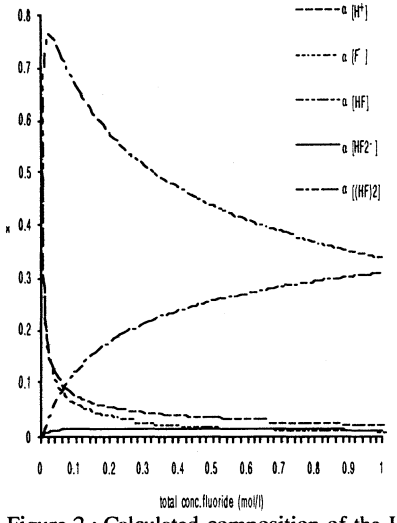


Figure 2 : Calculated composition of the HF mixture as a function of total fluoride concentration, when taking the dimerisation reaction into account.

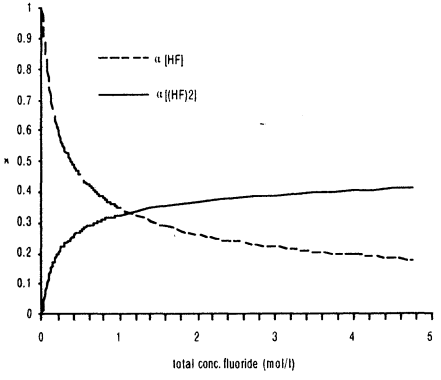


Figure 3 : Calculated composition of HF/HCl mixtures in the case the dimerisation reaction is taken into account.

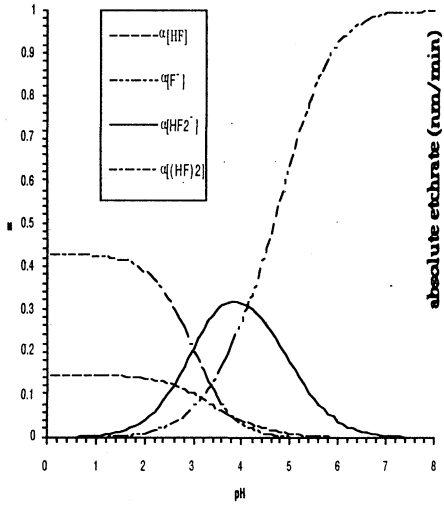


Figure 4 : Calculated composition as a function of pH for a fixed 7.5 mol/l fluoride concentration.

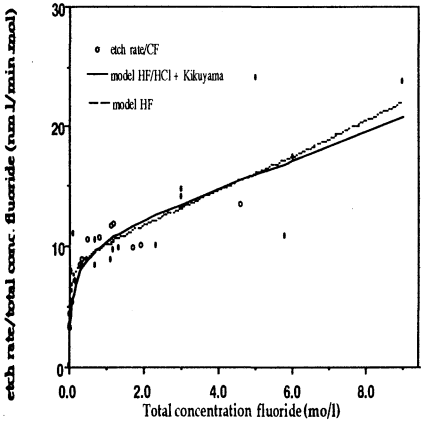


Figure 5 : Measured relative etch rate (dots) and fitted etch rates when the dimerisation reaction is taken into account.

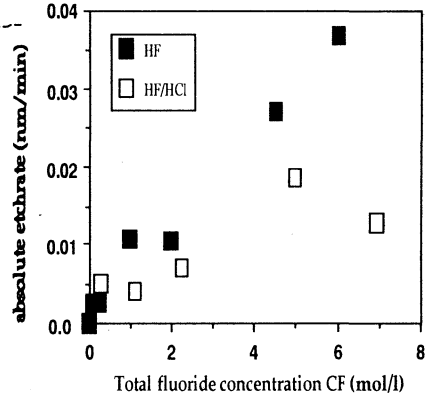


Figure 6 : Etch rates of poly-Si in HF and HF/HCl solutions as a function of the total fluoride concentration.

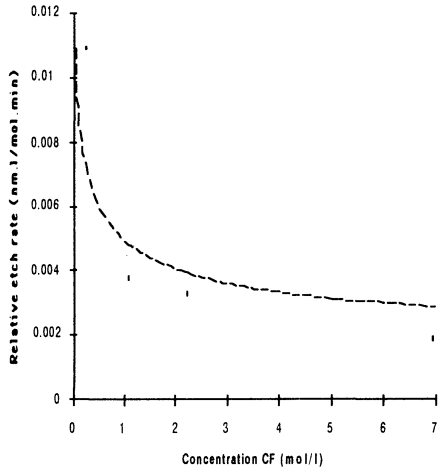


Figure 7 : Modelling of the relative etch rate of poly-Si as a function of fluoride concentration C_F in the case of a HF/HCl mixture.

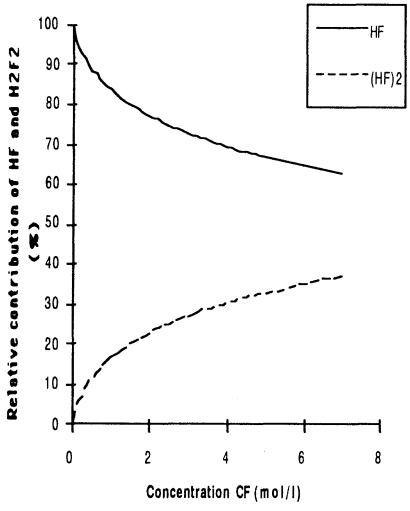


Figure 8 : Relative contributions to the etch rate of poly-Si as a function of fluoride concentration C_F in the case of a HF/HCl mixture.

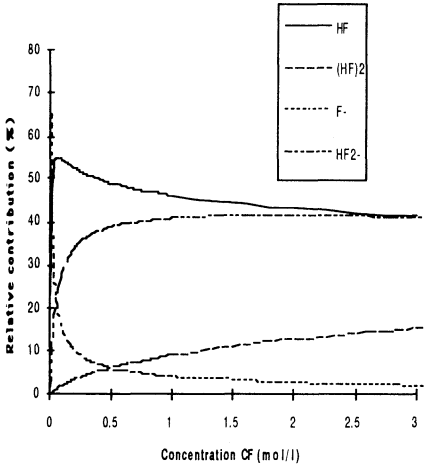


Figure 10 : Relative contributions to the etch rate of poly-Si as a function of fluoride concentration C_F in the case of a HF solution.

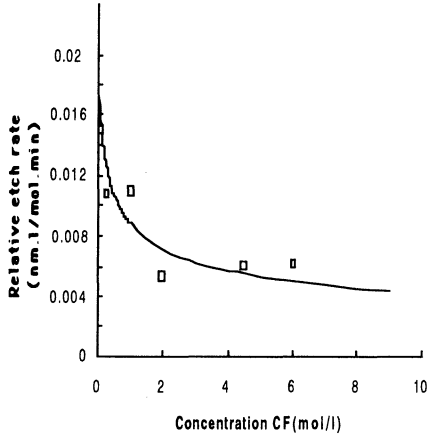


Figure 9 : Modelling of the relative etch rate of poly-Si as a function of fluoride concentration C_F in the case of a HF solution.

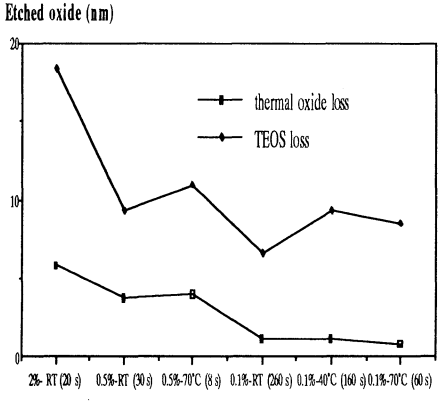


Figure 11 : Thermal oxide and TEOS oxide loss as a function of the process to remove the native oxide (concentration and temperature are varied).

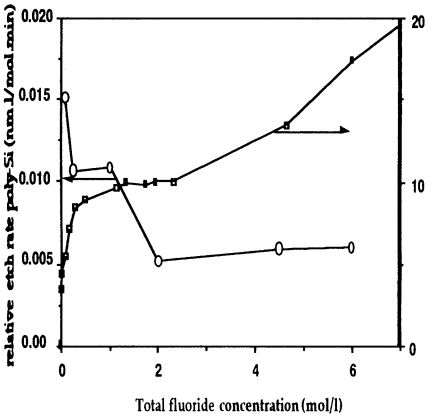


Figure 12 : Relative etch rates for thermal oxide and for poly-Si as a function of the total fluoride concentration for the HF mixture.

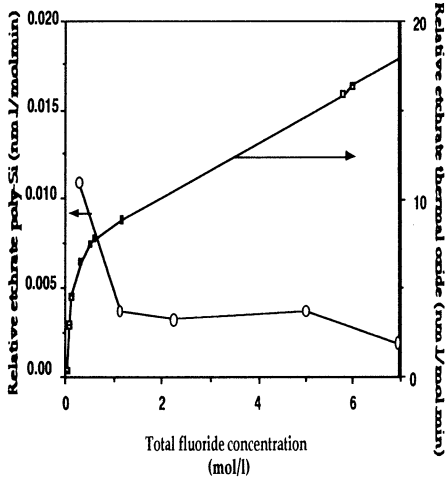


Figure 13 : Relative etch rates for thermal oxide and for poly-Si as a function of the total fluoride concentration for the HF/HCL mixture.

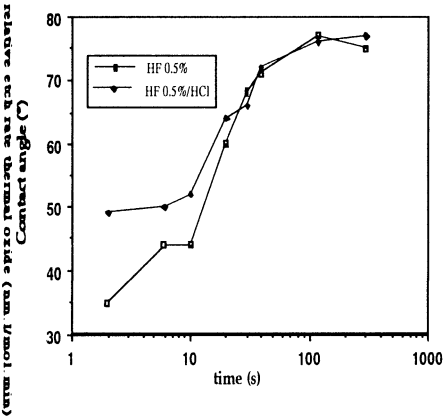


Figure 14 : Contact angle as a function of time for HF and HF/HCl mixtures.

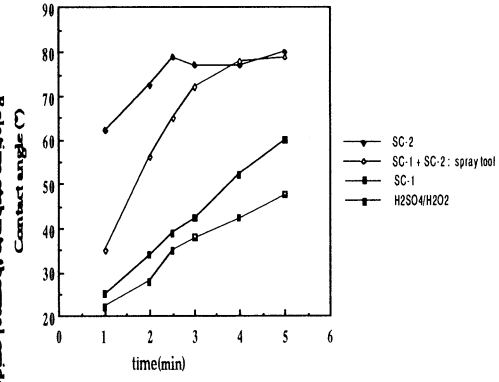


Figure 15 : Contact angle as a function of the dipping time in a 0.1 % HF solution for different chemical oxides.

HYDROGEN PASSIVATION OF HF-LAST CLEANED (100) SILICON SURFACES : A MIR-FTIR STUDY

H. Bender, S. Verhaverbeke, M.M. Heyns
IMEC
Kapeldreef 75
B-3001 Leuven, Belgium

The hydrogen passivation of (100) silicon surfaces is characterized as a function of the chemical treatment by means of Multiple Internal Reflection (MIR) Infrared Spectroscopy. The stability of the surfaces against oxidation and the build-up of a CH_x contamination layer are examined. A new feature is observed in the MIR spectra between the peak positions generally attributed to the di- and trihydrides and tentatively attributed to inclined dihydrides. This peak occurs for etchings with lower HF concentration and after DI water rinsing. Prolonged DI water rinsing results in facetting of the surface. A new Multiple Internal Reflection sample preparation method is proposed.

INTRODUCTION

It has recently been shown that HF-last cleanings of silicon result in superior dielectric characteristics [1]. The quality of thin gate oxides is strongly correlated with the interface flatness. Infrared spectroscopy can yield information on the surface micro-roughness through investigation of the relative amount of mono-, di- and trihydrides and their direction of polarization [2–8]. Indirectly it can yield information on surface reconstruction, as e.g. after H_2 annealing [9].

EXPERIMENTAL

Multiple Internal Reflection (MIR) infrared measurements are performed on a Mattson-Galaxy Fourier Transform Infrared spectroscope (FTIR) with polarized or unpolarized light. For this purpose a dedicated sample preparation technique is developed, based on standard device processing steps. Double side polished (100) silicon wafers are covered with a patterned nitride mask on both sides and subsequently etched in KOH at 80°C (Fig. 1). This results in (111) oriented sidewall planes which are used as IR entrance/exit planes. The silicon crystal is mounted in the MIR set-up so that the IR light is incident orthogonal to the sidewalls. For the 125 mm diameter silicon wafers with a standard thickness of 625 μm 132 internal reflections are thus obtained. The advantage of this sample preparation technique is that standard device quality (double side polished) silicon can be used so that the relationship between surface finishment, MIR spectral features and electrical properties can be studied on the same type of wafers. All spectra are acquired with N_2 purging of the FTIR analysis chamber. The resolution is set at 2 cm^{-1}. It is checked that using better spectral resolution does not reduce the peak width.

All samples are first wet chemically oxidized in a $NH_4OH/H_2O_2/H_2O$ (0.25/1/5) bath at 70°C ("SC-1"). One of these samples is used as reference for the MIR measurements. The period between preparation and measurements is kept as short as possible.

RESULTS

Aqueous HF solutions

MIR spectra with unpolarized light are acquired as a function of the etching time in an aqueous HF solution with 0.1, 0.5 and 5% HF with or without a subsequent rinse in DI water. A typical example is shown in fig. 2. The arrows indicate the peaks related to the coupled monohydride (M), dihydride (D) and trihydride (T). A very weak shoulder between the two monohydride peaks can sometimes be observed (not indicated on the figures). Although the exact peak position cannot be determined with certainty, this shoulder might be due to the 'ideal' monohydride peak (M') on (111) surfaces (peak position at 2083.7 cm^{-1} [5] - 2082.5 [6]). It would then be due to 'ideal' monohydride on (111) terminated surface steps. The positions of the M, D and T peaks are in accordance with the theoretical predictions [2,10]. It can be seen that the spectrum is dominated by the dihydride peak which has two maxima at respectively 2114 and 2106 cm^{-1} corresponding to the asymmetric and symmetric stretching vibrations. This type of spectrum is interpreted as due to a rough silicon surface [2,3]. The integrated intensity of the SiH_x stretching mode as a function of the etch time is represented on fig. 3. Saturation of the passivation is reached after shorter etching time for increasing HF concentration.

The intensity of the asymmetric dihydride peak depends on the HF concentration. This is illustrated in fig. 4 which shows spectra after etching with a 0.1%, 0.5% and 5% HF/H_2O solution (pH 2.5, 2 and 1.5 respectively). The intensity of D_{AS} increases for lower HF concentrations. Furthermore simultaneously with the increase of the intensity of the asymmetric dihydride peak a new feature (marked 'N') appears in the spectrum between the D and T peaks at 2123 cm^{-1}. This peak is also reported by other authors (e.g. on fig. 7 in [3]), but is inadequately explained.

Spectra acquired with polarized light show a partial polarization dependence of the dihydride peaks and a weak polarization dependence of the trihydrides, while the peaks of the monohydride and the one at 2123 cm^{-1} are almost independent of the polarization (Fig. 5). The degree of polarization of the dihydride peaks is independent of the HF concentration in the etch solution and is similar for both D peaks. The polarization dependence indicates that the dihydride groups are only partially oriented orthogonal to the surface as would be expected on an ideally hydrogen terminated (100) surface and that almost all the mono- and trihydrides are inclined with respect to the surface normal, i.e., present on surface steps and edges. Hence, the surfaces are rough on a microscopic scale.

The strength of the D_{AS} and the new peak at 2123 cm^{-1} further increases after rinsing in DI water independent of the fluoride concentration used during the etch step (Fig. 6). During the 5 minutes water rinse the monohydride concentration diminishes. The total hydrogen coverage (integrated absorbance) increases slightly during the rinse (Fig. 3). The polarized spectra of the samples after DI water rinsing show a similar polarization dependence of the peaks as for the unrinsed samples. During extended water rinsing a decrease of the dihydride peaks and an increase of the monohydride peaks is observed. Fig. 7 shows the polarized spectra after a 24 h DI water rinse. The ideal monohydride peak M' can now clearly be distinguished and the unstrained coupled monohydride peaks M show an important polarization dependence. No peak of O_xSiH can be observed. This result shows similarity with

the etching in buffered HF (see below) and indicates roughening of the (100) surface by formation of (111) facets during the long time DI rinse. Etching of (111) surfaces during treatment in boiling water has previously been reported [11].

HF/HCl/H_2O solutions

The probable dependence on the pH of the solution is further examined by adding HCl to the etch bath in a concentration of 0.5 mol/l. This solution has a pH of 0.3 independent of the HF concentration. In comparison with the spectra obtained without HCl, the intensity of the asymmetric dihydride peak is reduced for equal HF concentrations and the peak at 2123 cm^{-1} is absent in all cases. The spectrum for 0.5% HF with HCl is similar to the one for 5% HF without HCl. These observations indicate that the pH of the solution is not the most important factor influencing the strength of the D_{AS} and N peak, but that the HF concentration plays a major role. The HF/HCl solutions have the advantage compared to the aqueous HF bath that the uniformity of the SiO_2 etching is much improved [12]. On the other hand, the presence of Cl in the solution is generally believed to result in etching of the silicon surface and therefore in increased roughness. However, the MIR spectra show that the surface microroughness is not changed to any significant extent for the conditions investigated in this work.

HF/acetic acid solutions

Etching of the silicon can be avoided by using a more weak acid. A straightforward candidate for this purpose is acetic acid. Samples which are etched with 2% HF added to pure glacial acetic acid show again a SiH_x spectrum in which the symmetric D peak dominates similar as for the 5% HF etching. After rinsing in DI water again the asymmetric D peak dominates and also the peak at 2123 cm^{-1} is present.

HF/isopropyl alcohol/H_2O solutions

Adding isopropyl alcohol (IPA) to the HF/H_2O solution results in improved electrical characteristics and lower particle densities [13]. No effect on the MIR spectra can be noticed, i.e., the microroughness is not changed by the IPA so that the improved electrical characteristics should be related to the difference in particle density.

Buffered HF solutions

Etchings at a higher pH are performed in a buffered HF solution (pH = 4-5). As a function of the etch time a change of the spectrum from dihydride dominated to monohydride dominated is observed (Fig. 8). The integrated absorbance under the SiH_x peak is almost independent of the etch time. Without rinsing the asymmetric dihydride peak is more intense than the symmetric one. After rinsing this effect becomes more pronounced and also the peak at 2123 cm^{-1} can clearly be observed. The intensity of the latter peak decreases proportional with the decrease of the dihydride peaks. Up to 30 s etching in BHF, the polarization dependence of the different peaks is similar as for the aqueous HF solutions. Already for the 5 s etching the ideal monohydride (M') peak can be observed as a clear shoulder

peak. For longer etch times the intensity of the monohydride M peaks as well as of the M' peak increase (Fig. 9). The strength of the latter peak is independent of the polarization, i.e., corresponds to inclined monohydrides as is expected for ideal monohydrides on (111) facets. The monohydride peak at 2088 cm^{-1} shows an important polarization dependence, while the M peak at 2071 cm^{-1} has a weak inverse polarization dependence, i.e., it is the largest in the s-polarized measurements. It can be concluded that this coupled monohydrides are mainly oriented in a plane orthogonal to the surface. As their peak positions indicate that they are unstrained, they are likely situated at the [110] edges of intersecting (111) facets. Furthermore a peak is present at 2100 cm^{-1} which has a polarization dependence similar to the one for the 2088 cm^{-1} peak. Its peak position can be related to strained coupled monohydrides on (100) [4].

Stability of the H-passivation

The stability of the H-passivation is studied in time-resolved MIR measurements. The build-up of CH_x bonds starts immediately after the preparation of the samples and saturates after approximately 5-8 hours independent of the condition of the H-passivation (Fig. 10). Peaks can be distinguished of the stretch vibrations of the sp^3 configuration of CH (m), CH_2 (d) and CH_3 (t) at peak positions which are in accordance with those observed for hydrogenated hard carbon [14]. The spectrum is dominated by the d and t peaks. Only the dihydrocarbide shows a partial polarization dependence. It can be concluded that the hydrocarbides are mainly randomly oriented on the surface.

The build-up of this hydrocarbon contamination layer also occurs on the chemical oxide sample, with a similar time dependence. Therefore care should be taken to use a freshly prepared chemical oxide as reference and to minimize the time between preparation and measurement of the cleaned samples. It is important to realize that due to the measurement relative to the reference sample, equal amounts of hydrocarbon or other IR active contaminants initially present on the chemical oxide as well as on the cleaned samples cannot be investigated with MIR. Indeed some adsorbed carbon can be measured on the cleaned samples with XPS even when no carbon bonds are found by MIR [15].

The only samples which show in the MIR spectra initially no CH_x bonds, are those etched in a HF/acetic acid solution. This agrees with XPS measurements which indicate that the treatment with acetic acid results in the lowest C contamination on the surface [15].

The peak of O_xSi-H ($\sim$2260 cm^{-1}) is observed once the samples are kept for at least a few days in air. During this period the fine structure of the Si-H_x peak disappears. After 1 week still $\sim$50% of the passivation is present (Fig. 11). The remaining SiH_x slowly decreases further but partially remains present for more than 10 weeks. For the samples treated in BHF, the monohydride peak decreases much faster than the dihydride peak (Fig. 12), but the decrease of the integrated hydrogen peak intensity is slower than for samples treated in aqueous HF (Fig. 11).

DISCUSSION

The described experiments point out that the N peak arises for treatments in

solutions with lower HF concentrations and after rinsing in DI water. Its presence is also linked to an increase of the intensity of the D_{AS} peak. The peak separation between N and D_{AS} is 9 cm^{-1}, which is very similar to the experimental (8 cm^{-1}) and predicted (9 cm^{-1} [10]) separation between the two dihydride peaks. No explanation for the N peak is available in the literature. In view of the peak positions and the strength of the N peak, it seems unlikely that the N peak arises from a coupling between the dihydrides and monohydrides resulting in three dihydride peaks as reported for vicinal (111) surfaces [7]. Also a shift of the trihydride peak over more than 7 cm^{-1} or a new trihydride related peak seems to be unlikely for a (100) surface. It is *tentatively proposed that actually two new dihydride peaks are present after treatment in a solution with a lower HF concentration or after DI rinsing* : an asymmetric D" peak at 2123 cm^{-1} and a symmetric D" peak at 2114 cm^{-1}, i.e., at the same position as the asymmetric D peak. This explains the simultaneous occurrence of the N peak and of the increase of the D_{AS} peak. The polarization independence of the N peak indicates that the D" groups are inclined with respect to the surface. The decrease of the (inclined) monohydrides during the DI rinsing can then be related to the formation of the inclined D" dihydrides. This might imply some etching of the surface already during the 5 min DI rinse. This indeed agrees with observations that DI water can etch Si [16] and is also in accordance with *the (111) facetting during extended rinsing* which can be deduced from our MIR measurements and with the reported etching of (111) surfaces in boiling water [11].

The formation of the D" groups can probably also occur during the DI rinsing on those places where F terminates the surface after HF etching [17]. An indication for this process might be the increase of the integrated SiH_x absorbance during rinsing and also the fact that XPS measurements show a decrease of the F concentration after DI rinsing [15, 17]. This replacement of F groups by D" groups can then already occur during the HF etching itself when solutions with low HF concentration are used. For highly concentrated HF, the F termination is more stable than the D" group termination and thus no replacement takes place.

The dependence of the etch behaviour is related to the varying equilibria in the HF/H_2O solution [18,19]. At a pH below 1.5 the HF is not dissociated and only HF and the dimer $(HF)_2$ are present. At medium pH (3-5) the HF_2^- ions dominate and at a pH above 5.5 mainly F^- ions are present. Adding HCl to the aqueous HF solution lowers the pH and results in a mixture of HF and $(HF)_2$. It can be concluded from the results with the BHF and from the observation that low (this work and e.g. [3]) as well as very high pH's [3] give rise to dihydride dominated MIR spectra, that HF_2^- etches primarily along the (111) planes.

The capacitor yield is enhanced for a 5% HF cleaning compared to a 0.1% HF cleaning [20]. This difference is attributed to slight roughening in the latter case by HF_2^- etching, whereas in the case of the 5% HF solution the oxide etching occurs solely by HF and H_2F_2.

CONCLUSION

The peak at 2123 cm^{-1} which is present after aqueous HF cleaning with a low HF concentration and after DI rinsing is tentatively attributed to inclined dihydrides. Etching in BHF as well as long time rinsing in DI water result in facetting

of the (100) silicon surface. On all cleaned samples a fast build-up of a hydrocarbon contamination layer is observed. Oxidation of the passivated surfaces is a slow process so that even after more than 10 weeks some hydrogen passivation is left.

ACKNOWLEDGEMENTS

The authors greatly acknowledge P. Mertens, M. Caymax, W. Vandervorst and J. Alay for stimulating discussions and M. Dulst and H. Van de Plas for the skillful preparation of the cleaned samples.

REFERENCES

1. S. Verhaverbeke, M. Meuris, M.M. Heyns, P.W. Mertens, H.F. Schmidt, A. Philipossian, K. Dillenbeck, D. Gräf and A. Schnegg, in : *Proc ULSI Science and Technology*, Electrochem. Soc. spring meeting (1993), in press.
2. Y.J. Chabal, G.S. Higashi, K. Raghavachari and V.A. Burrows, J. Vac. Sci. Technol. **A 7**, 2104 (1989).
3. Y.J. Chabal, Mat. Res. Soc. Symp. Proc. **259**, 349 (1992).
4. Y.J. Chabal and Raghavachari, Phys. Rev. Lett. **53**, 282 (1985).
5. G.S. Higashi, Y.J. Chabal, G.W. Trucks and K. Raghavachari, Appl. Phys. Lett. **56**, 656 (1990).
6. S. Watanabe, N. Nakayama and T. Ito, Appl. Phys. Lett. **59**, 1458 (1991).
7. P. Jakob and Y.J. Chabal, J. Chem. Phys. **95**, 2897 (1991).
8. M. Hirose, T. Yasaka, M. Hiroshima, M. Takakura and S. Miyazaki, Mat. Res. Soc. Symp. Proc. **315**, in press (1993).
9. H. Bender, S. Verhaverbeke, M. Caymax, O. Vatel and M.M. Heyns, Appl. Phys. Lett. submitted
10. V.A. Burrows, Y.J. Chabal, G.S. Highashi, K. Raghavachari and S.B. Christman, Appl. Phys. Lett. **53**, 998 (1988).
11. S. Watanabe, M. Shigeno, N. Nakayama and T. Ito, Jpn. J. Appl. Phys. **30**, 3575 (1991).
12. S. Verhaverbeke, I. Teerlinck, G. Stevens, R. Cartuyvels, M.M. Heyns, J. Electrochem Soc. submitted (1993).
13. S. Verhaverbeke, M. Meuris, M. Schaekers, L. Haspeslagh, P. Mertens, M.M. Heyns, R. de Blank and A. Philipossian, in : *Proc. 1992 Symp. on VLSI Technology*, Digest of Technical Papers, p 22 (1992).
14. B. Dischler, A. Bubenzer and P. Koidl, Solid State Comm. **48**, 105 (1983).
15. J. Alay, S. Verhaverbeke and W. Vandervorst, unpublished.
16. M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami and M. Ohwada, J. Appl. Phys. **68**, 1272 (1990).
17. M. Hirose, T. Yasaka, K. Kanda, M. Takakura, S. Miyazaki, in : *Proc. 2nd Int. Symp. on Cleaning Technology in Semiconductor Device Manufacturing*, eds. J. Ruzyllo and R. Novak, The Electrochem. Soc., Pennington (1992) pp. 1-9.
18. S. Verhaverbeke, H. Bender, M. Meuris, P.W. Mertens, H.F. Schmidt and M.M. Heyns, Mat. Res. Soc. Symp. Proc. **315**, in press (1993).
19. S. Verhaverbeke, M. Meuris, H. Schmidt, P. Mertens and M. Heyns, these proceedings
20. S. Verhaverbeke, J. Alay, P. Mertens, M. Meuris, M. Heyns, W. Vandervorst, M. Murrell and C. Sofield, Mat. Res. Soc. Symp. Proc. **259**, 391 (1992).

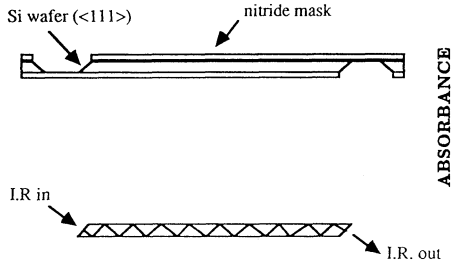


Fig. 1 : Preparation of the MIR silicon crystals by KOH etching of a double side patterned nitride masked wafer (a) and IR light path through the chamfered crystal (b).

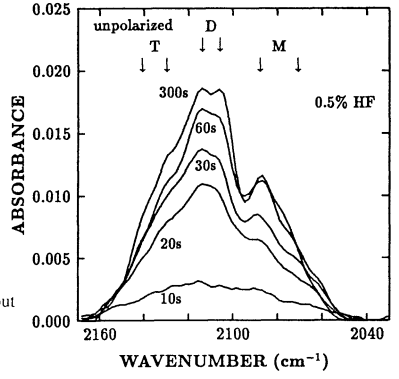


Fig. 2 : MIR spectra of the SiH_x stretching modes as a function of the etching time in a 0.5% HF/H_2O solution. Mono- (M), di- (D) and tri- (T) hydride peaks can be distinguished.

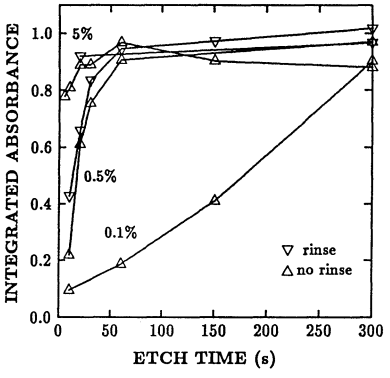


Fig. 3 : Integrated absorbance of the SiH_x stretching mode as a function of the etch time in different HF/H_2O solutions with and without rinsing.

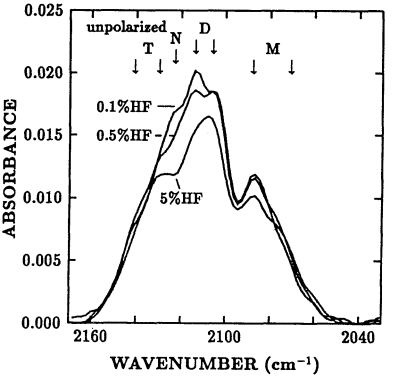


Fig. 4 : Unpolarized spectra after etching with a 0.1%, 0.5% and 5% HF/H_2O solution without DI water rinsing.

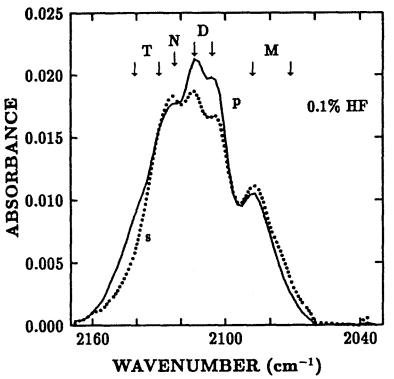


Fig. 5 : Polarized SiH_x spectrum for a 5 min etching in 0.1%HF/H_2O without DI water rinsing.

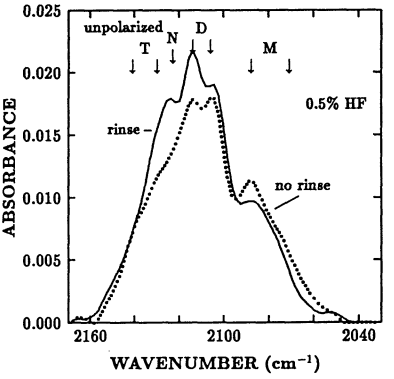


Fig. 6 : Comparison of the SiH_x absorption spectrum for a 5 min etching in 0.5%HF/H_2O with and without rinsing.

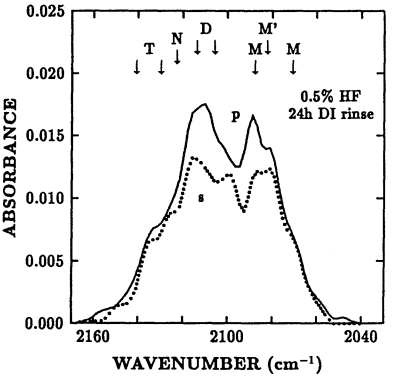


Fig. 7 : Polarized SiH_x spectra for a 24 h rinse in DI water after a 5 min etching in 0.5%HF/H_2O. The increase of the monohydrides indicates (111) facetting.

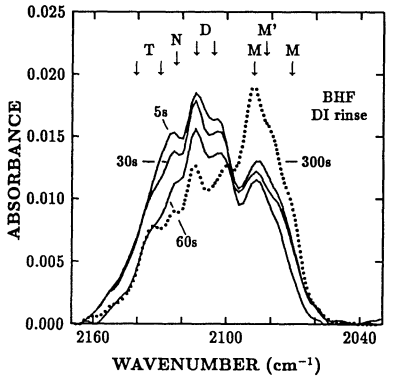


Fig. 8 : SiH_x spectrum as a function of etch time in a buffered HF solution showing the change of a dihydride to a monohydride covered surface.

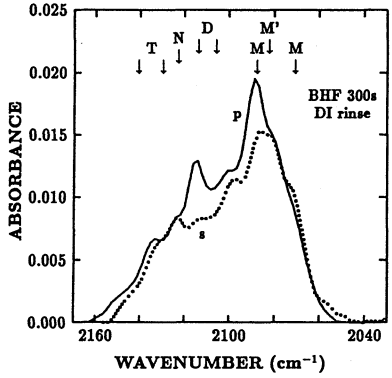


Fig. 9 : Polarized SiH_x spectrum for a 5 min etching in BHF with subsequent DI rinse.

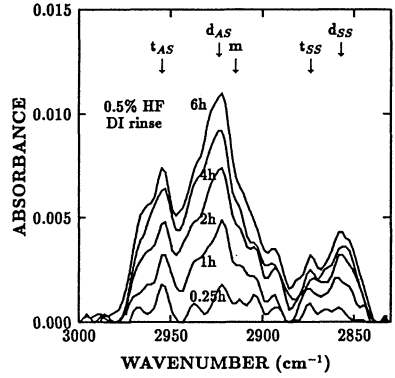


Fig. 10 : The CH_x bonds as a function of time after a H-passivation with 0.5% HF/H_2O and DI water rinse. CH (m), CH_2 (d) and CH_3 (t) peaks can be distinguished. Asymmetric and symmetric stretch modes are indicated by AS and SS respectively.

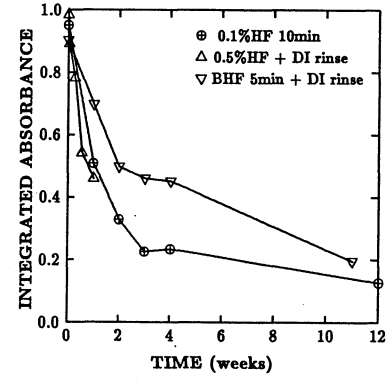


Fig. 11 : Decrease of the integrated SiH_x absorbance for different etchings when the samples are kept in cleanroom air for several weeks.

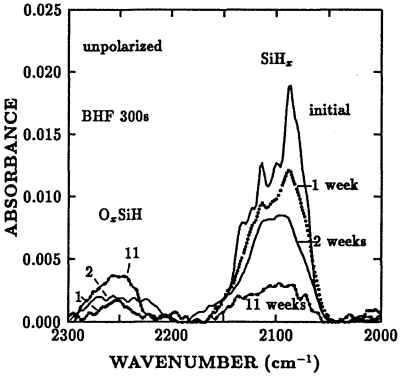


Fig. 12 : SiH_x and O_xSiH peaks as a function of storage time in air after a BHF 300s etching and subsequent rinsing in DI water.

HF *IN-SITU* TANK USED IN HF-LAST CLEANING.

Paul PATRUNO, Didier LEVY and Alain FLEURY
Centre Commun CNET - SGS-THOMSON Microelectronics, 38192 CROLLES, FRANCE
Allessandro TONTI
SGS-THOMSON Microelectronics, Via Olivetti, AGRATE BRIANZA, ITALY
François TARDIF
LETI(CEA-Technologies Avancées), Avenue des Martyrs, 38041 GRENOBLE, FRANCE

ABSTRACT

The effect of a wet chemical cleaning process used as HF-last cleaning in an automated wet bench is investigated in a special tank, which has the design capability for *in-situ* displacement of an extremely diluted solution of HF by DI water. The performance of this tank is compared to that obtained on a conventional acid tank with its dedicated rinse tank to which the wafers are transferred. Surface microroughness measurements by AFM, surface trace contamination measurements by TXRF, particle contamination measurements using a laser particle counter and contact angle measurements have been done in order to characterize this cleaning process. It has been found that by using HF *in-situ* tank we improve particle contamination as well as contact angle. Etch rate has been found to be usable for HF-last cleaning with very high HF dilution, when etch time is around 5 minutes. This range of long etch time is good for batch etching uniformity. A theoretical study of the *in-situ* rinsing conditions has also been done and a good correlation of its results with measured values of a specifically designed set of experiments has been obtained.

INTRODUCTION

A dilute HF mixture is increasingly being used as a final step, often referred to as "HF-last" because it is done as the end of the complete cleaning sequence, just before final rinsing and drying. This last step provides hydrogen passivated surface and removes metals that are still present. [1]

In this work, the effect of a wet chemical cleaning process used as HF-last cleaning in an automated wet bench is investigated, using a special tank design incorporating the capability of *in-situ* displacement of an extremely diluted HF solution by DI water. The performance of this tank (called *in-situ* rinse tank) is compared to that obtained on a conventional acid tank with its dedicated rinse tank to which the wafers are transferred. In such a case with conventional acid tank (called *standard* rinse tank) the transfer from the acid tank to the rinse tank causes hydrophobic wafers to be exposed to a liquid(acid)/air interface and to an air/liquid(water) interface. This is not desirable since particle contamination can occur from hydrophobic wafers being inserted into a liquid when the transfer is done. [2]

The benefits obtained from HF *in-situ* are evaluated and the influence of H_2O_2 added to dilute HF is also investigated. Surface microroughness is measured with a non-contact Atomic Force Microscope (AFM), chemical contamination is measured on the wafer using TXRF. Particle contamination is monitored with a laser particle counter and contact angle is used to monitor changes in surface stochiometry.

The complete study has been done using 200 mm wafers.

IMPROVING HF-LAST CLEANING

Transferring wafers after HF-last, from the acid tank to the next tank dedicated to rinse with DI water, causes hydrophobic wafers to be exposed to a liquid(acid)/air interface and to an air/liquid(water) interface. This phenomenon is well known and has been described and explained by several authors. Repeated experiments have shown that, in a single HF process batch, thick thermal oxide wafers (that stayed hydrophilic) will exhibit particle removal, while thin thermal or native oxide wafers that have been exposed to HF (turning hydrophobic) exhibit considerable particle addition. This finding has been attributed to the immersion of hydrophobic wafers; as the wafers are inserted into the DI water rinse tank, particles on liquid surface transfer and become attached to the wafers.

Improved particle contamination can be expected with a special tank design, in which HF solution is first mixed and blended in a dedicated vessel, then transferred through a dual parallel filter, to the process tank. A continuous recirculation/filtration loop can be used throughout an in-line heater, such that the process temperature is controlled, within better than $\pm$ 1°C.

After the HF cleaning process in the *in-situ* tank is finished, a couple of valves are switched such that dilute HF solution is displaced from the bottom of the tank with DI water. The wafers are finally transferred through a final rinse tank and to a final dry (Spin Rinser Dryer - SRD or IPA dryer).

EXPERIMENT BASELINE

Before starting the experiments, our drying process was referenced such that it would not lead to misinterpretation of contamination tests. Drying, as the last step is very critical, and an extensive study of the level of performance of a conventional IPA dryer, model FEL 281 supplied by S&K, has been done using a repeated series of measurements over more than 3 weeks. A single cassette fully loaded with 25 x 200 mm wafers, carried inside a special quartz carrier using a 2-axis robot installed in a fully automated wet bench supplied by SubMicron Systems Inc was used for this text.

The tests consisted of 5 minutes in an ambient temperature SC1 solution (NH_4OH:H_2O_2:H_2O - 0.5:1:5in a Turbo Sunburst Megasonic process tank supplied by VERTEQ, using 250 watts power) followed by a 5 minute rinse in an QDR/overflow rinse tank, a 10 minute final rinse in an overflow rinse tank before a 15 minute IPA dry step in the S&K dryer.

This allowed 33 test measurements to be made on the same set of wafers, only one set of particle count measurements (0.3 um and above particle size) were made per run. The difference between run n and run n-1 has been plotted versus the number of runs first (Fig 1), and finally in removal efficiency plot (Fig 2).

It shows extremely good neutral behavior in terms of particle contamination from the total cleaning, rinsing and drying process, demonstrating the effectiveness of the drying technique and of the actual setup of the IPA dryer.

EXPERIMENTS

Particle contamination and etch rate

In the first set of experiments particle contamination and thermal oxide etch rate resulting from both kinds of rinsing (standard rinse and *in-situ* rinse) after HF-last processing, are compared with different tank temperatures in the range of 20°C to 40°C.

HF process time of 300 seconds has been chosen for the HF process step. This condition has been found elsewhere to exceed the minimum time in order to reach a

stable and significantly high contact angle. [3]

Rinse after HF process time of 300 seconds has been chosen as well for both kinds of rinsing, standard rinse and *in-situ* rinse. This condition has been found as a reasonable rinsing time.

The HF dilution has been chosen for practical reason to be 50% HF:H_2O=1:208 in volume, assuming that a little more native oxide than already grown on the test wafers is to be removed.

Test wafers were 200 mm prime wafers from the box for the contamination test, and thermal oxide wafers for etch rate measurements. Oxide thickness is measured with a beam profile reflectometer, and the etch rate is obtained by averaging the difference before and after etch (based on 21 points per wafer).

Fig 3 presents the particle contamination results from this first set of experiments, for particle size 0.3 micron and above. One can see that a reduction on particle contamination is always observed when *in-situ* rinse is used. The temperature effect is also quite significant in particle contamination reduction.

Fig 4 shows the etch rate measured on this series of tests. The difference between standard and *in-situ* rinse etch rates, can easily be explained by the time required for the *in-situ* rinse to start up in the tank (different from the standard rinse). The mechanism of rinsing in the *in-situ* tank has been theoretically studied and the final experiments are described in this paper to support this work. The theoretical study is given in Appendix to this paper.

One can see from these etch rates that oxide thickness removed is higher than the normal target for native oxide removal, especially at high temperature. This suggests that a more dilute solution could be used reducing acid cost.

Surface characterization

In a second set of experiments AFM measurement, contact angle measurement, optical absorption and thermal oxide etch rate resulting from both kinds of rinsing (standard rinse and *in-situ* rinse) are compared for different tank temperatures in the range of 20°C to 60°C.

The same process conditions have been used, 300 seconds HF process time, 300 seconds rinse time and same type of wafers.

Fig 5 shows the etch rate measured on this series of tests, with the extended temperature range conditions of 20°C to 60°C. Non-uniformity top to bottom, not shown here is below 4% at 1 sigma, on the center wafers of the boat.

Surface microroughness has been measured using a non-contact Atomic Force Microscope from Digital Instruments. RMS value instead of Ra value which is often used, and peak-to-valley (6 sigma) value from the AFM measurement are plotted on the next graph. (Fig 6). RMS value is higher than Ra value.

Contact angle of the wafers resulting from the same experimental conditions have been measured using an accurate test bench specially designed by CNET. High contact angle means that the surface is well passivated. It is a very good measure of the degree of completeness of native oxide removal. This technique has been found to be well correlated to XPS measurement.

Fig 7 shows the contact angle measured on this series of tests, with an extended range of temperature from 20°C to 60°C with a reference value at 40°C to compare *in-situ* rinse and standard rinse. The maximum value one can get on a perfect silicon surface is 78.9 degree. Angles very closed to this value have been obtained on the HF *in-situ* rinse test at 40°C and above. It is worth noticing that these high contact angles have been measured 48 H after processing. This demonstrates the effectiveness of the surface passivation after HF *in-situ* rinse.

Spectroscopic ellipsometry has also been used on these test wafers, to characterize the silicon surface resulting from this set of experiments. The $\epsilon 2$ dielectric function (equivalent to the optical absorption) is used, which shows two intensity peaks, at 3.34 eV (representing the crystalline structure) and at 4.30 eV (Fig 8). The latter is representative of surface microroughness and indeed a good correlation is shown with the previous figure.

In order to characterize the wafer surface, TXRF measurements have been done on the same set of wafers. TXRF has been done on a RIGAKU TXRF, by LETI with a detection limit of $5x10^9$ at/cm^2. Measurements of a few species considered to be the most significant are reported. Average surface measurements for Fe and Cu on 2 wafers are plotted along with a non-processed reference wafer, for comparison (Fig 9). No significant differences in Fe or Cu contamination are observed for all cases, showing that the HF process is not creating contamination, within measurement limits, whatever the rinsing conditions may be.

Addition of Hydrogen Peroxide to the HF solution

In a third set of experiments, the above experiments have been repeated with addition of H_2O_2 to the dilute HF solution. The concentration used was 10 percent of the total dilute HF solution as Hydrogen Peroxide.

The same process conditions have also been used, 300 seconds dilute HF with H_2O_2 process time, 300 seconds rinse time, and the same type of wafers

Fig 10 shows the etch rate measured on this set of tests, using the extended temperature range of 20°C to 60°C.

In order to characterize the difference in wafer surface contamination, TXRF measurements have been made on the same set of wafers (especially looking at Cu) to demonstrate the effectiveness of H_2O_2 addition and the results of this test is presented. (Fig 11)

Again, only average values of Fe and Cu measured on 2 wafers at the surface are plotted with an unprocessed reference wafer for comparison. No significant differences are observed with Fe contamination. However, a slight improvement is observed with Cu contamination with H_2O_2 addition.

MODELLING OF HF *IN-SITU* RINSE PROCESS

Another set of experiments has been designed, in order to support the work presented in Appendix 1. The goal was to measure the time to effectively *in-situ* rinse between wafers inside the wafer carrier. Wafer position number 25 on the carrier is exposed to different rinsing conditions, comparison is done with wafers 13 and 14.

While the flow near a surface exposed to the liquid flow may be modelled with the help of the boundary layer concept for the wafers such as number 13 and 14 in a carrier, no such boundary develops between parallel surfaces for wafer number 25. In the first case it may be easily shown that the velocity profile is parabolic. (Fig 12) As an example, comparing the oxide removed 0.5 cm from the bottom of the wafer to the same distance from the top, the model shows a difference of 1.4 nm between these 2 points (1.1 nm have been measured in the same conditions).

One important comment arising from these results, concerns the cost of HF disposal when using an *in-situ* rinse tank. Since it is possible to rinse in quite short time without seeing a detrimental effect on oxide etch uniformity across the boat on field oxide (obviously exposed silicon zones being totally cleared off, are not concerned by this) only moderate quantities of very dilute HF effluents are sent to the drain.
A good estimation being around 250 liters per batch of 50 wafers when using optimized tank dimensions.

CONCLUSIONS

Both standard and *HF in-situ* rinse processes have been studied. The two techniques have been compared and characterized for 200 mm wafers processed in a state-of-the-art class 1 fab environment using advanced automated wet benches with an established IPA drying process. Very good results have been obtained for various concentrations and temperatures, both with and without addition of H_2O_2 to the dilute HF solution. High contact angle of the hydrogen terminated surface has been obtained with good passivation properties and an improvement in particle count by a factor of two has been achieved. AFM measurement has shown very low surface roughness while TXRF has shown low surface contamination and confirmed effectiveness of Cu removal by addition of the H_2O_2 to the dilute HF solution used. Rinsing has been achieved throughout the entire wafer carrier as demonstrated by the mathematical model given hereafter. The subsequent set of experiment has proven the validity of the theoretical study. The *in-situ* rinse process is relatively easy to implement. The very low concentration of HF required makes it inexpensive when using very precise quantities of 50% HF with DI water, even though HF solution is lost for every batch of wafers.

ACKNOWLEDGEMENTS

The authors would like to thank Jean-Louis BUEVOZ, Elie ANDRE, Frédéric FERRIEU and Emilienne FADDA from CNET, FRANCE TELECOM Laboratory in Meylan, FRANCE, for very useful support in doing measurements and for very valuable discussions about the results. This paper would have not been achieved without this support.

LETI, CEA France Laboratory has supported us as well for the TXRF measurements, thanks to Carole D'ASSENZA for her valuable contribution.

APPENDIX

Modelling of *in-situ* rinse process (by Dr Allessandro Tonti)

While we may model the flow field near a surface exposed to the liquid with the help of the boundary layer concept [4], no such boundary develops between parallel surfaces, such as between wafers in a carrier. In this case it can easily be shown [5] that the velocity profile is parabolic, and that it obeys the equation:

$$U(z) = \frac{\Delta p}{2\eta L}(d^2 - z^2) = U_{max}\left[1 - \left(\frac{z}{d}\right)^2\right] \qquad (1)$$

The average velocity is 2/3 U_{max} and may be set roughly equal to the normal, unimpeded fluid velocity in the tank. In our case 0.44 cm/s may be a realistic value. The Reynolds number for the flow between wafers, under these conditions is 17, i.e. the flow is completely laminar.

At the onset of the *in-situ* rinse phase, pure water is injected in the etch tank with the same flow geometry used for the recirculation of dilute HF. After a small delay pure water enters between the wafers and starts to displace upwards the dilute HF solution following the same streamlines; the disturbance to flow is minimal due to the similarity of physical properties between two liquids. The separation surface between pure water and dilute HF arches between two neighboring wafers, while the dilute HF

solution clings to the wafers as a layer of slowly decreasing thickness.

By very simple mathematics it may be shown, as in [5], that the HF layer thickness is given by :

$$x = U(z)*t = \frac{\Delta p}{2\eta L}(d^2 - z^2)*t = U_{max}\left[1 - \left(\frac{z}{d}\right)^2\right]*t = D \qquad (2)$$

This system may be solved for z, the distance of the interface from the mid-plane between wafers at a point removed by the length D from the leading edge. Of course the HF layer thickness is just $a_x=(d\text{-}z)_x$. Some representative figures related to the rinse process are given in Tab.I.

Tab.I- HF LAYER THICKNESS(cm) AND RESIDUAL CONCENTRATIONS

t	z_L	a_L $=(d\text{-}z)_L$	$a_{1/2L}$	$2(Dt)^{1/2}$	f_L	$f_{1/2L}$	f_0
0 s	0 cm	0.28 cm	0.28 cm	0 cm	1	1	1
15 s	0	0.28	0.28	0.024	1	1	0
30 s	0	0.28	0.081	0.037	1	1	0
45 s	0.16	0.12	0.051	0.043	1	1	0
60 s	0.2	0.08	0.036	0.049	0.90	0.54	0
90 s	0.23	0.05	0.024	0.060	0.59	0.33	0
120 s	0.244	0.036	0.018	0.069	0.41	0.23	0
180 s	0.255	0.025	0.013	0.085	0.26	0.14	0
240 s	0.262	0.018	0.009	0.098	0.17	0.09	0
300 s	0.266	0.014	0.007	0.110	0.12	0.06	0
360 s	0.268	0.012	0.006	0.120	0.09	0.05	0

Here the second column displays layer thickness values at the trailing edge of a diametral section; the third thickness values at the wafer center, and the fourth diffusion lengths for HF, taking a diffusion coefficient of about 10^{-5} cm^2/s.

We see at once that after 60 s the center values are practically one half those at the trailing edge, i.e. the interface is flat. After the same time the diffusion length becomes larger than the residual layer thickness a_L, and becomes increasingly larger towards the end of the rinse, i.e. 300 s in our case. The residual fraction of chemicals or contaminants may be computed by using a triangular approximation to the diffusion profile [5], which gives:

$$f = \frac{2a(x,t)}{4\sqrt{(Dt)} + a(x,t)} \qquad (3)$$

Some values given by (3) are listed in the last three columns of Tab.I, where $f_{x,t}$ is the residual fraction at a distance x from the leading edge and at time t. The fraction remaining on the surface may amount, in the worst case (trailing edge), to about 10%. Impurities therefore are not efficiently swept away by *in-situ* rinsing, also, the HF concentration and the related etch rate are not negligible during the rinse phase. The removal is practically nil for particles, which diffuse much more slowly. The indication is that a very pure filtered HF must be used on very clean wafers so that residual contamination is not a problem. Anyway at the end of the rinse stage impurities are drained away from the hydrophobic wafer surface with the very dilute HF, so that the only residual contamination, if any, is due to adsorbed ions or plated-on metal layers.

Referring to the etch rate data published by [3] and summarized in Tab.II we may approximatively model the etching during rinsing and the resulting oxide thickness non- uniformity.

Tab.II- HF ETCH RATE VS. CONCENTRATION AND TEMPERATURE

HF concentration	E.R. @ 24°C	E.R. @ 40°C	E.R. @ 60°C
10% wt	50 nm/min	110 nm/min	400 nm/min
6	30 "	90 "	210 "
2	10 "	30 "	60 "
1	4.6 "	14 "	20 "
0.4	1.5 "	3.3 "	6.5 "
0.2	0.6 "	1.5 "	2.2 "
0.1	0.2 "	0.4 "	0.5 "
0.06	0.09 "	0.1 "	0.2 "

For any point on the wafer the HF concentration and the related etch rate may be computed as a function of time, using the data in Table I and Table II; the total reduction in oxide thickness may be calculated by integration. (See Fig 13 and Fig 14).

As an example, comparing the etch process at point G' (0.5 cm from the bottom, i.e. the leading edge) and at point B' (same distance from the trailing one) at a starting etch rate [6], of about 0.8 nm/min for the initial 0.25% HF, we find the following situation:

point G': thickness loss during etching 4 nm, during rinsing 0.1 nm
Total 4.1 nm

point B': thickness loss during etching 4 nm, during rinsing 1.5 nm
Total 5.5 nm

Non-uniformity (Max-min)/2*ave = 15%.

Of course this figure can be considerably improved by rinsing at higher temperatures, which speeds up diffusion and causes the etch rate dependence on concentration to become steeper. This must be balanced with the effect of increasing the native oxide layer growth due to the increased temperature of the DI water during rinsing. A non-uniformity better than 10% may be also obtained. This oxide thickness non-uniformity is not observed after the wafer has become hydrophobic, but could in principle, be replaced by a subtler and less easily measurable non-uniformity in physical structure in this case. Therefore it is preferable to use high temperature *in-situ* rinsing.

BIBLIOGRAPHY

[1] Peter H. Singer, Semiconductor International, page 36-39, Dec. 1992.
[2] Christopher F. McConnell, UCPSS 92, Sept. 1992.
[3] Steven Verhaverbeke et Al, IEDM 92, page 637-640. Dec. 1992.
[4] A. Tonti, ECS 91, Oct. 1991.
[5] A. Tonti, revised paper submitted to Microcontamination
[6] C.A. Deckert, ECS journal, 127,11, page 2433. Nov. 1980.

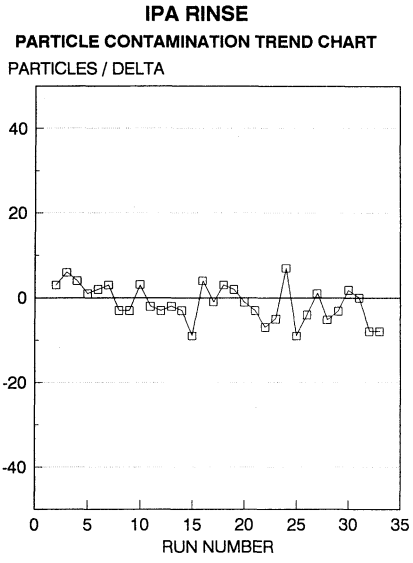


FIG 1

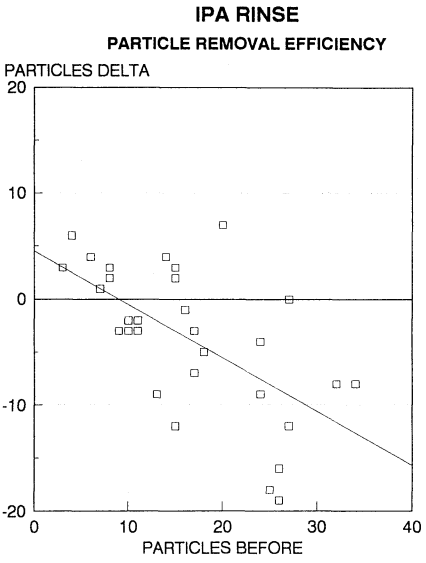


FIG 2

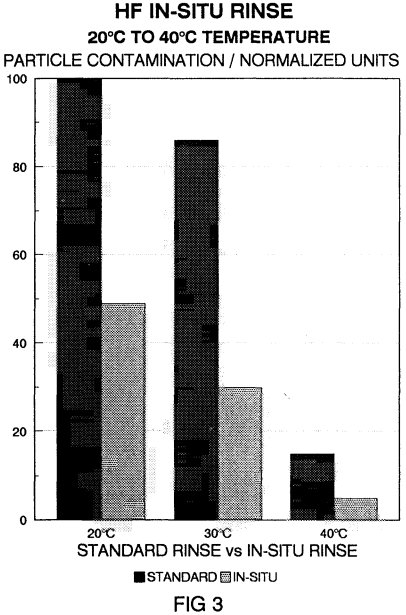


FIG 3

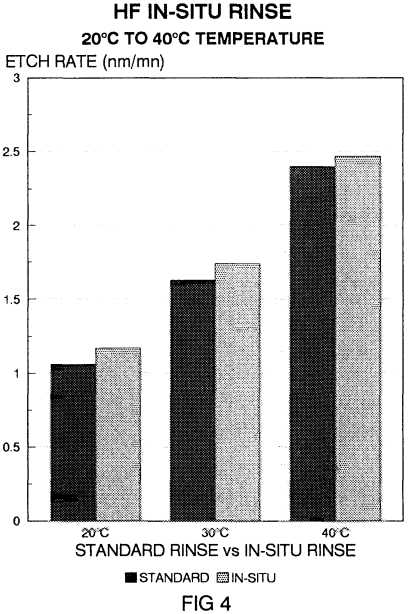


FIG 4

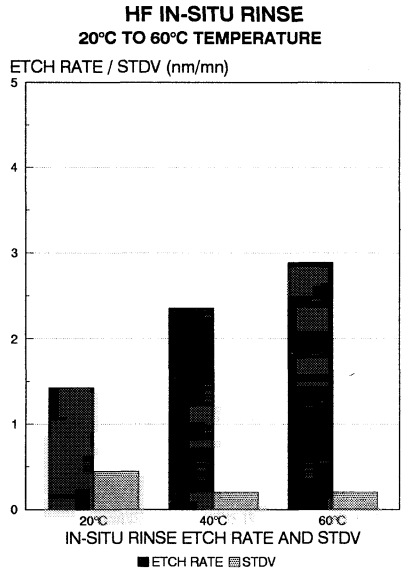


FIG 5

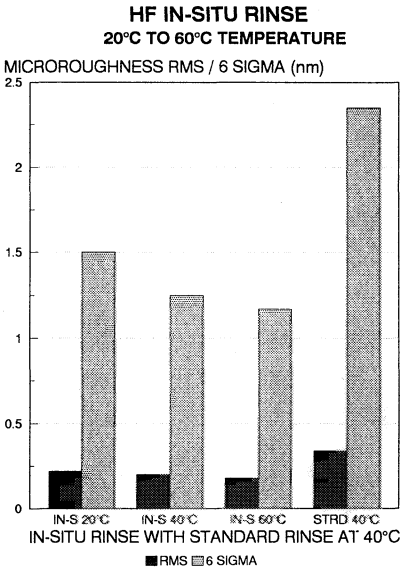


FIG 6

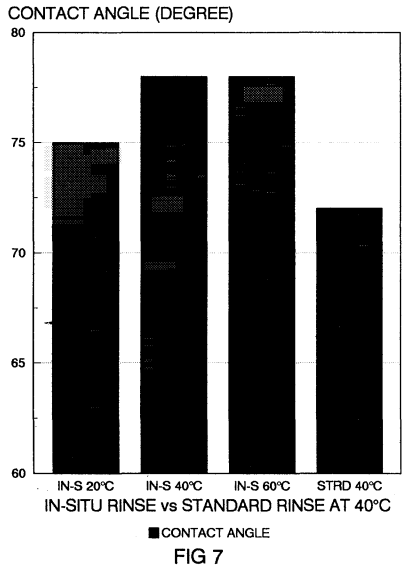


FIG 7

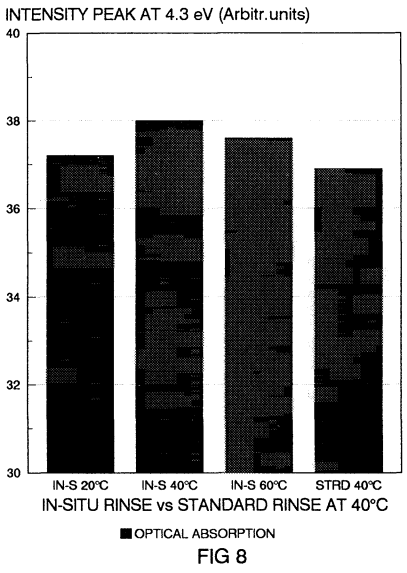


FIG 8

HF IN-SITU RINSE / TXRF
20°C TO 60°C TEMPERATURE

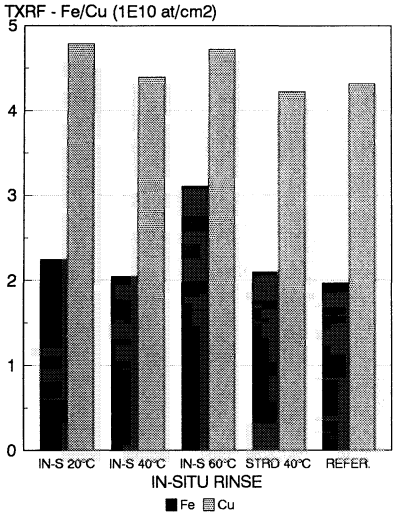


FIG 9

HF+10% H2O2 IN-SITU RINSE
20°C TO 60°C TEMPERATURE

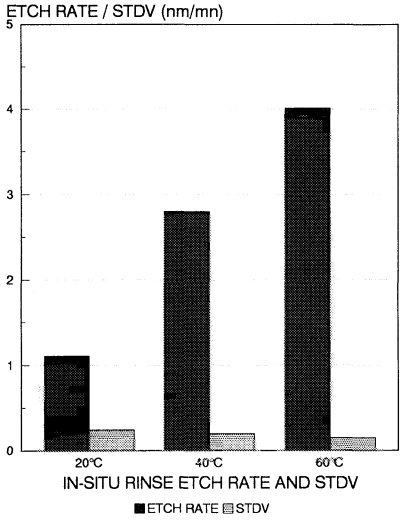


FIG 10

HF IN-SITU RINSE WITH 10% H2O2 / TXRF
20°C TO 60°C TEMPERATURE

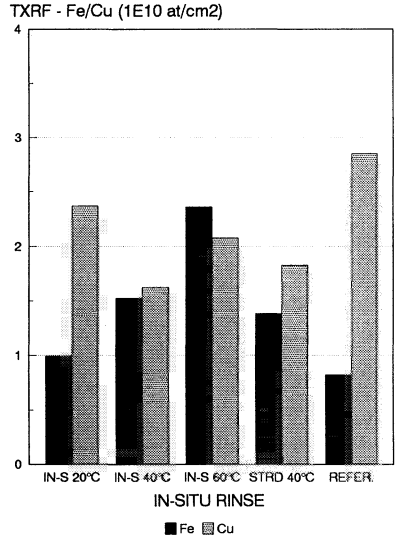


FIG 11

HF IN-SITU RINSE
IN-SITU RINSE BETWEEN WAFERS

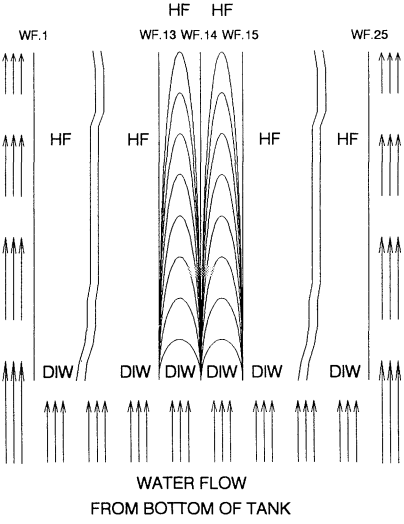


FIG 12

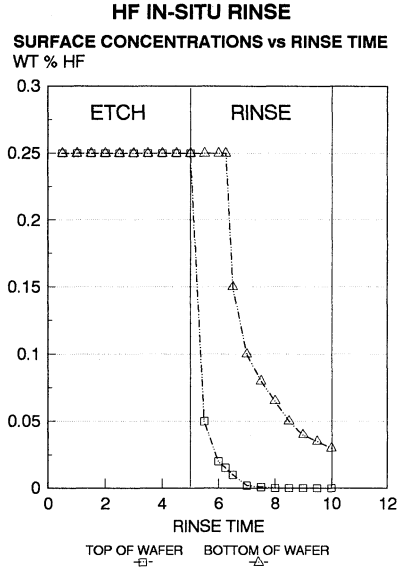

HF IN-SITU RINSE
SURFACE CONCENTRATIONS vs RINSE TIME
WT % HF
0.3
0.25
0.2
0.15
0.1
0.05
0
ETCH
RINSE
0
2
4
6
8
10
12
RINSE TIME
TOP OF WAFER
BOTTOM OF WAFER

FIG 13

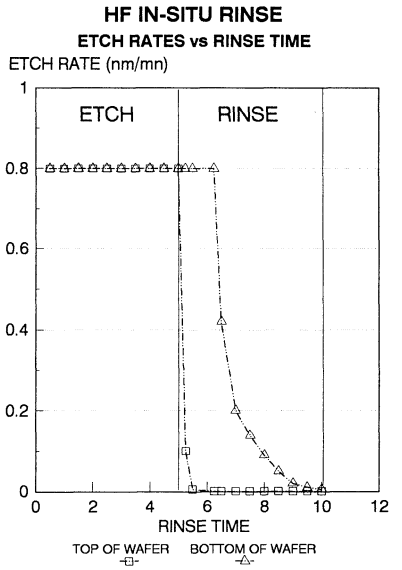

HF IN-SITU RINSE
ETCH RATES vs RINSE TIME
ETCH RATE (nm/mn)
1
0.8
0.6
0.4
0.2
0
ETCH
RINSE
0
2
4
6
8
10
12
RINSE TIME
TOP OF WAFER
BOTTOM OF WAFER

FIG 14

CONTAMINATION REDUCTION IN DILUTE HF BY ADDING HCl

I.Oki, H.Shibayama and A.Kagisawa

Sharp Corporation,VLSI Research Laboratories,
2613-1 Ichinomoto-cho Tenri City, Nara 632,
JAPAN

ABSTRACT

The influences of HCl addition in dilute HF to Si surfaces and the electrical characteristics of the thin oxide were investigated. It is shown that the adhesions of particles and metallic contaminants are reduced and the efficiencies of removing metallic contaminants are improved at the appropriate HCl concentrations in dilute HF, which results in the improvement of the electrical characteristics of the thin oxide. The formation of the unsoluble salts and the slight oxidation of Si surface by HCl are considered to be the main reasons of these advantages.

INTRODUCTION

In a wet chemical cleaning process of VLSI fabrication, wafer cleaning in dilute HF is especially important, since it is used as precleaning before the thin oxide formation. However, the bare Si surface is susceptible to particulate and metallic contaminations in dilute HF. In order to form the reliable thin oxide, it is indispensable to avoid such contaminations in a cleaning process in dilute HF. Several alternative cleaning methods, such as H_2O_2 added dilute HF cleaning [1], surface active buffered HF cleaning [2] and HCl added vapor HF cleaning [3] are investigated. In this paper, a new cleaning method of HCl added dilute HF is proposed, which results in low particulate and metallic contaminations and improves the electrical characteristics and reliability of the thin oxide [4].

EXPERIMENTAL

CZ, P(100) wafers with 150 mm in diameter were used in the following experiments.

The adhesions and removal efficiencies of particles

and metallic cntaminants on Si surface in dilute HF (1%,5%) with and without HCl addition were evaluated by means of the laser particle counting (ESTEC: WIS-850) and Total Reflection X-Ray Fluorescence (TECHNOS: TREX-610). HCl concentrations were varied from 0% to 5% in dilute HF.

The adhesions of particles and metallic contaminants to bare Si surfaces were measured after immersing wafers in dilute HF with and without HCl addition for one minute. In the case of evaluating metallic contaminations, each solutions were intentionally contaminated with impurity metals (Ni,Fe,Cu,Zn,Cr: 2000 ppb in the solution).

The removal efficiencies of particles and metallic contaminants on Si surfaces were evaluated after immersing the intentionally contaminated wafers in dilute HF, dilute HCl and HCl added dilute HF for one minute. The initial number of particles on Si surfaces were about 5000 (> 0.16 um), and the initial concentrations of Cu, Fe, Zn and Cr on Si surfaces were $2x10^{11}$, $1x10^{13}$, $2x10^{11}$ and $4x10^{14}$ atoms/cm^2, respectively.

The influences of HCl in dilute HF to the microroughness and the growth of native oxide on Si surfaces were evaluated by AFM (Degital Instruments: Nanoscope 3) and FTIR - ATR (Biorad : FTS-40).

The electrical characteristics of thin oxide (100 A) grown by the thermal oxidation after cleaning in dilute HF with and without HCl addition were evaluated by the minority carrier recombination life time measurement (REO: LTA-550), the dielectric breakdown measurement and the TDDB measurment of constant voltage stress (-16 MV/cm).

RESULTS AND DISCUSSIONS

The adhesion of particles on Si surface after immersing in dilute HF are decreased as the concentration of HCl increases as shown in Fig.1.

The adhesions of metallic contaminants on Si surface as a function of HCl concentration in dilute HF are shown in Fig.2. The surface concentration of Cu, Zn, Ni and Fe increases when 1% HCl added, however, above this concentration of HCl, the adhesions of these impurity metals starts to decrease drastically. The surface concentrations of Cu are $1x10^{14}$, $2x10^{14}$ and $2x10^{11}$ atoms/cm^2 after imersing in HF(1%), HF(1%)/HCl(1%) and HF(1%)/HCl(5%), respectively. It can be observed that the dependence of Cl adhesions to Si surface on the HCl concentration is identical to the adhesions of metallic impurities, as shown in Fig.3.

This indicates that the Cl on Si surface enhances the adhesions of impurity metals, so that the adequate HCl concentration is important to reduce the Cl termination on Si surface. The decrease of Cl termination at higher HCl concentration is explained that the Si surfaces are supposed to be oxidized in dilute HF when adequate HCl existed. Shown in Fig.4 are the FTIR-ATR spectra of Si surfaces after immersing in HF(1%), HCl(5%) and HF(1%)/HCl(5%). It can be observed that the backbond oxidation peaks of O_3SiH and O_2SiH_2 appears at HCl(5%) and HF(1%)/HCl(5%) treated surfaces.

The maximum removal efficiency of particles in dilute HF shows no improvement by HCl addition, however, the level of minimum removal efficiency is raised by adding HCl as shown in Fig.5, which indicates that the redepositons of particles washed off from Si surface are prevented.

On the contrary, the efficiencies of removing metallic contaminants on Si surface, especially Cu and Zn, are improved drastically by HCl addition in dilute HF, as shown in Fig.6. It should be noted that the HCl alone does not enough to remove metallic contaminants efficiently.

In a HCl added dilute HF solution, the oxidation process of Si surface by HCl and etching process of native oxide by HF are believed to be occuring repeatedly. The deposition of particles and impurity metal on Si surface are suppressed in the process of surface oxidation, because of passivation of active bare Si surface, and in the process of surface oxidation, metallic contaminants on Si surface are incorporated into native oxide and removed when native oxide is etched off. Furthermore, at higher HCl concentrations, the formation of unsoluble salts of impurity metals, such as CuCl, is considered to be suppressing the adhesion of the impurity metals.

Fig.7 shows surface roughness (Ra) of Si wafers after immersing in HF(1%) and HF(1%) / HCl(3%) for 10 minutes. HCl addition in dilute HF does not degrade the micro-roughness of Si surface.

Fig.8 shows the minority carrier recombination life times of P-type Si wafers, which oxides were grown after cleaning in dilute HF with and without HCl addition. It can be observed that the minority carrier life time increases about 10 % by HCl addition, which result is consistent with the suppression of impurity metal deposition on Si surfaces [5].

Fig.9 and Fig.10 show the oxide defect density and TDDB characteristics of thin oxide (SiO_2 = 100 A) grown by thermal oxidation after cleaning in dilute HF with and without HCl addition. The oxide defect densities were caluculated using -lnP/S, where P and S represent the yield (breakdown field > 8 MV /cm) and the electrode area (4 mm^2). The oxide defect densities are 0.6, 1.6 and 1.9 cm^{-1} in the case of cleaning in dilute HF, and 0.1, 1.0 and 2.3 cm^{-1} in the case of cleaning in dilute HF with HCl addition. A relatively large dispersion of the defect densities in the latter case could be improved by optimizing HCl concentrations. It can be observed that TDDB characteristics are improved by HCl addition in dilute HF. This may be due to the improvement of cleaning efficiencies in dilute HF by HCl addition.

CONCLUSIONS

We have shown the following advantages of Si wafer cleaning by HCl added dilute HF compared with the conventional cleaning of dilute HF.

(1) The adhesions of particles and impurity metals (Cu, Ni, Zn, Fe) from the solution are suppressed at the appropriate HCl concentrations.

(2) The cleaning efficiencies of metallic contaminants on Si surface are improved.

The formation of unsoluble salts and the repeated processes of the slight oxidation of Si surface by HCl and the oxide etching on Si surface by HF, are considered to be the main reasons of these advantages, which result in reliability improvement of the thin oxide.

ACKNOWLEGEMENT

The authors would like to thank to Mr. R.Miyake and T.Sakurai for their supports.

REFERENCES

1. T.Shimono and M.Tsuji : Spring Meeting of Electrochemical Society, Extended Abstracts, p 278 (1991)

2. T.Ohmi, M.Miyashita, M.Itano,T.Imaoka, and I.Kawanabe : IEEE Transactions on Electron Devices Vol.39 No.3 p 537 - 545 (1992)

3. D.B.Kao, B.R.Cairns and B.E. Deal : Cleaning Technology in Semiconductor Device Manufacturing (The Electrochemical Society, Proc. Vol 92-12) p 251 - 259

4. I.Oki, T.Miyata, T.Biwa, J.Kudo and H. Shibayama : Extended Abstracts (The 39th Spring Meeting 1992) The Japan Society of Applied Physics and Related Societies p 690 (in Japanese)

5. J.Atsumi, S.Ohtsuka, S.Munehira and K.Kajiyama : Semiconductor Cleaning Technology /1989 (The Electrochemical Society, Proc. Vol 90-9) p 59 - 66

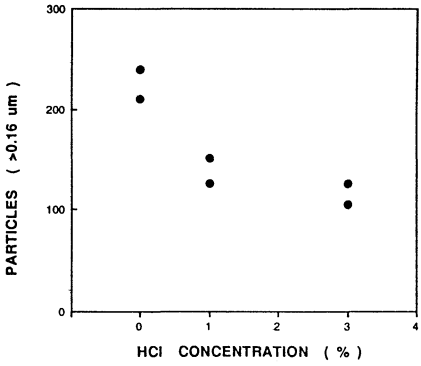


Fig.1
The number of adhered paricles on Si wafers as a function of HCl concentration in dilute HF (1%)

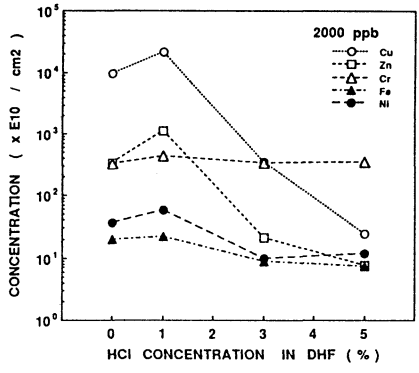


Fig.2
Surface concentration of adhered metallic contaminants on Si wafers as a function of HCl concentration in intentionally contaminated dilute HF (1%)

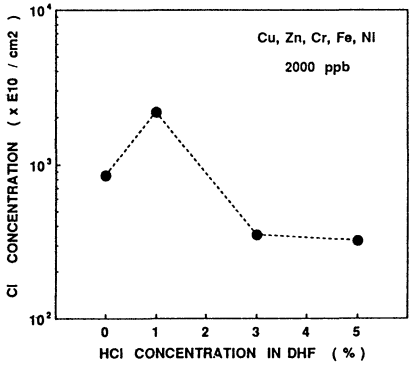


Fig.3
Chlorine concentration on Si wafers as a function of HCl concentration in intentionally contaminated dilute HF(1%)

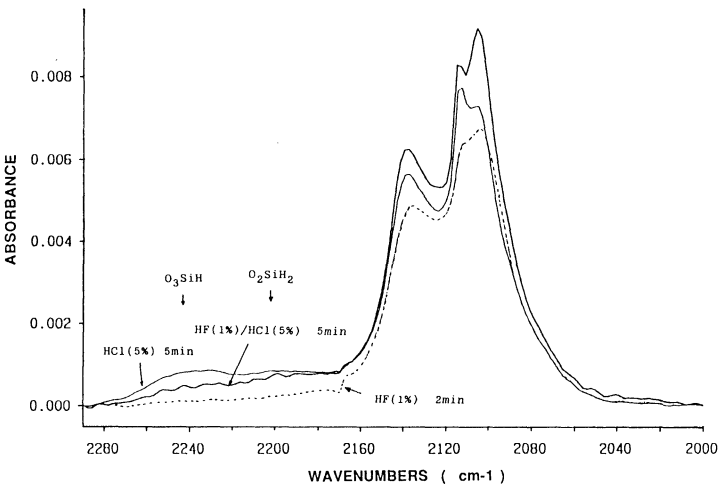


Fig.4
FTIR - ATR spectra of Si wafers after immersing in HF(1%), HCl(5%) and HF(1%) /HCl(5%)

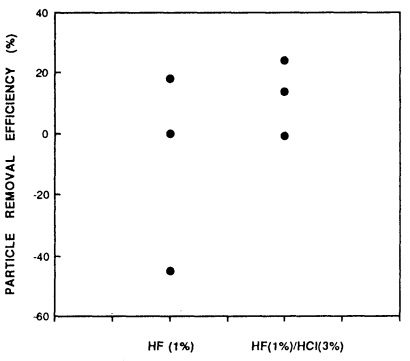


Fig.5
The efficiencies of removing particles on Si wafers after cleaning in HF(1%) and HF(1%) / HCl(3%)

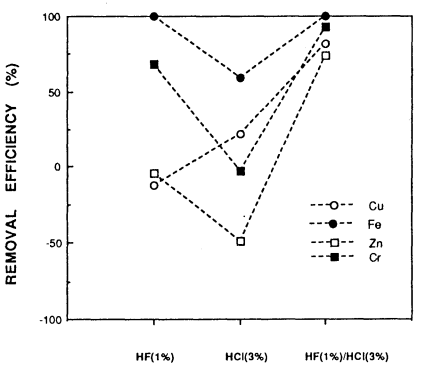


Fig.6
The efficiencies of removing metallic contaminants on Si wafers after cleaning in HF (1%), HCl(3%) and HF(1%) / HCl(3%)

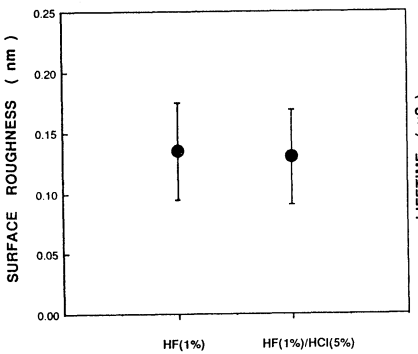


Fig.7
Surface roughness (Ra) of Si wafers after immersing in HF(1%) and HF(1%) / HCl(3%)

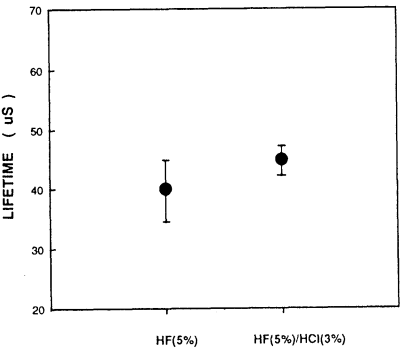


Fig.8
The minority carrier recombination lifetimes of P type wafers which oxide were grown after cleaning in HF(5%) and HF(5%) / HCl(3%)

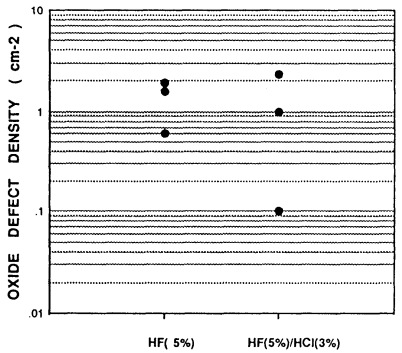


Fig.9
The oxide defect densities of thin oxide (100 A) grown after cleaning in HF (5%) and HF(5%) / HCl(3%)

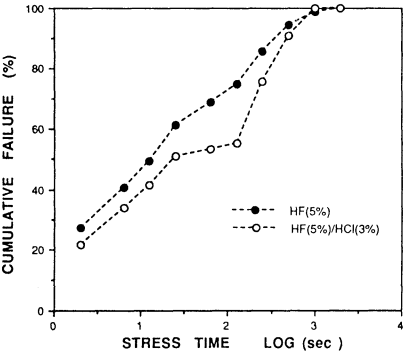


Fig.10
TDDB caracteristics of thin oxide (100A) grown after cleaning in HF (5%) and HF (5%) / HCl(3%)

Prevention of Microroughness Generation on the Silicon Wafer Surface in Buffered Hydrogen Fluoride by a Surfactant Addition

M. Miyamoto, N. Kita, S. Ishida, and T. Tatsuno
Morita Chemical Industries Co., Ltd;
3-12-10, Higashimikuni, Yodogawa-ku, Osaka 532, Japan

ABSTRACT

For the purpose of preventing the generation of microroughness on the Si wafer surface in buffered hydrogen fluoride(BHF), the effect of the surfactant addition into BHF was investigated. It was found that the microroughness generation was prevented by a several 10 ppm addition of the surfactants, which suppress the dissolution of Si into BHF from the Si wafer surface. It was also clarified that the microroughness generation was suppressed by lowering the NH_4F concentration in BHF and the dissolution of Si depended on the OH^- concentration rather than on the HF concentration in BHF. For a wide range of HF and NH_4F concentrations in BHF, the hydrocarbon anionic surfactant is effective for the suppression of the microroughness generation. The suppression of the microroughness generation is explained by the adsorption of the surfactant molecules on the Si wafer surface in accordance with the Langmuir type adsorption equation.

Introduction

In semiconductor device fabrication process, it is very important to clean the Si wafer surface for the performance and the reliability of devices. Wet cleaning process and etching process have been increasingly necessary in order to remove the contaminants such as inorganic ions, organic matters, particles, and native oxide on the Si wafer surface. Recently, very thin oxide films and very shallow junction have been more and more important for device fabrication with reduced dimensions. Therefore, it becomes essential to prepare the smooth Si wafer surface without any contaminant(1). Buffered hydrogen fluoride(BHF) which has been widely used in wet process of device fabrication is excellent for the removal of particles on the Si wafer surface besides etching of Si oxide films(2). However, it is reported that the microroughness is generated on the Si wafer surface by immersion in BHF for a long time(3). The generation of microroughness must be prevented in order to improve the performance and the reliability of devices. In the present work, the effect of the surfactant addition was investigated to prevent the microroughness generation on the Si wafer surface in BHF. The relation between the microroughness generation and both HF and NH_4F concentrations in BHF with and without surfactant addition was also investigated. Moreover, the suppression of Si dissolution by surfactant addition was explained by the adsorption of the surfactant molecules on the Si wafer surface according to the Langmuir type adsorption equation.

Experimental

There are many kinds of BHF with various combinations of HF and NH_4F concentrations. In the present work, 630BHF(HF=6wt%, NH_4F=30wt%), which has been widely used in wet process of device fabrication, was used. Also, there are many kinds of surfactants with various chemical structures and characteristics. However, the surfactants which are suitable for BHF are limited by the following 8 items: namely, (I)the etching rate of the Si oxide film by BHF does not change by the surfactant addition, (II)metal ions in BHF do not increase, (III)particles in BHF do not adhere on the Si wafer surface, (IV)the surfactants do not make BHF foam, (V)the surfactants are not trapped by filtering, (VI)the surfactants do not decomposed by BHF nor react with BHF, (VII)the resists are not attacked by surfactants (VIII)the surfactants dissolve in BHF. In this experiment, Three kinds of surfactants chosen by the pre-experiments were used: They are hydrocarbon anionic, hydrocarbon cationic and perfluorocarbon anionic surfactants [5wt% isopropyl alcohol(IPA) solution]. The three surfactants have the effect of improving the wettability of BHF. Moreover, it has been reported that the hydrocarbon anionic and perfluorocarbon anionic surfactants have the effect of preventing metal ion deposition on the Si wafer surface(4).

The substrates used in this experiment are CZ-P type Si(100), and CZ-N type Si(100) and Si(111) wafers with the resistivity of 1-2 Ω・cm. Each Si wafer was cleaned with H_2SO_4-H_2O_2 solution and the native oxide on the Si wafer surface was removed in 5% HF solution before the immersion experiment. The Si wafer was immersed in BHF for 24, 48 and 120 hours at 25 ℃. After immersion, Si wafer was rinsed in pure water and dried by N_2 blow. The microroughness on the Si wafer surface was investigated by scanning electron microscope(SEM). The concentration of dissolved Si in BHF after immersion was measured by induction coupled plasma atomic emission spectrometer(ICP-AES)(5). Thermal Si oxide film formed at 1000℃ in wet atmosphere, phosphosilicate glass(PSG) and borosilicate glass(BSG) films formed by the chemical vapor deposition(CVD) method and annealed at 1000℃ were used in order to investigate the influence of the surfactant addition on the etching rate of Si oxide films by BHF. The etching rate of Si oxide films by BHF was calculated from the etching time and the etching depth which was measured by the interference method. pH of BHF was measured by the glass electrode method.

Results and Discussion

Figure 1 shows SEM photographs of three types of Si wafer surface after immersed in 630BHF. The large microroughness is observed on every Si wafer. Etch-pits on Si(100) are circular and those on Si(111) are triangular. The surface of the N-type Si wafer immersed in 630BHF is rougher than that of the P-type Si wafer. Figure 2 shows SEM photographs of the wafer surface after immersed in 630BHF containing various surfactants. In case of perfluorocarbon anionic surfactant, 2000ppm IPA is added at the same time because it is dissolved in IPA as 5wt%. The addition of hydrocarbon cationic surfactant or IPA scarcely suppresses the microroughness generation. On the other hand, the addition of hydrocarbon or perfluorocarbon anionic surfactant prevents the microroughness generation on the Si wafer surface. In case of 25ppm addition

of hydrocarbon anionic surfactant, the microroughness is not observed after immersed for 24 hours, but is observed after immersed for 48 hours. In case of 50ppm addition, the microroughness is not observed after immersed for 48 hours.

Figure 3 shows the relationship between the surfactant concentration and (a) pH and (b) the amount of dissolved Si after immersed in 630BHF. In case of no addition, the dissolved Si from the N type Si wafer in 630BHF is more than that from the P type. Although pH of 630BHF scarcely changes by the addition of either anionic or cationic surfactant, the amount of dissolved Si decreases with the increase of the surfactant concentration and the addition of anionic surfactant is more effective for the suppression of Si dissolution than that of cationic surfactant. Accordingly, an addition of more than 50ppm hydrocarbon or perfluorocarbon anionic surfactant is very effective for both the prevention of the microroughness generation on the Si wafer surface and the suppression of the Si dissolution in 630BHF from Si wafer.

In general, Si is etched by OH^- in an alkaline solution as follows (6):

$$Si + 4OH^- \rightarrow Si(OH)_4 + 4e^-$$
$$4H^+ + 4e^- \rightarrow 2H_2\uparrow$$

In conventional BHF, Si is oxidized by OH^- in BHF and is dissolved by HF in BHF as follows (7):

$$Si(OH)_4 + 6HF \rightarrow 2H^+ + SiF_6^{2-} + 4H2O$$
$$2NH_4^+ + SiF_6^{2-} \rightarrow (NH_4)_2SiF_6$$
$$2H^+ + 2F^- \rightarrow 2HF$$

In BHF containing surfactants, however, the oxidation process by OH^- is considered to be suppressed by the adsorption of the surfactant molecules on the Si wafer surface. The reason why anionic surfactant is more effective for the suppression of Si dissolution than cationic surfactant is that the hydrophilic group of anionic surfactant molecule is negative and can prevent electrically the attack of OH^- in BHF to the Si wafer surface.

Figures 4 and 5 show the dependence of pH and the amount of dissolved Si on the NH_4F concentration and on the HF concentration in BHF, respectively. The amount of dissolved Si increases with the increase of the NH_4F concentration, and decreases with the increase of the HF concentration in BHF. Correspondingly, pH also increases with the increase of the NH_4F concentration and decreases with the increase of the HF concentration. However, the dissolution of Si is suppressed by the addition of hydrocarbon anionic surfactant independently on the NH_4F and HF concentrations. Figure 6 shows SEM photographs of the N type Si(100) wafer surface after immersed in 630BHF and in BHF with a low NH_4F concentration. The microroughness is suppressed by lowering the NH_4F concentration in BHF, and is also prevented by the addition of hydrocarbon anionic surfactant. Consequently, the effect of lowering the NH_4F concentration in BHF on suppressing the microroughness generation on the Si wafer surface can be explained by the suppression of the Si dissolution due to lowering the OH^- concentration in BHF with the change of pH. Anyway, the addition of hydrocarbon anionic surfactant is effective for the suppression of

Si dissolution and the prevention of microroughness generation.

Next, the etching rate of Si oxide film was investigated. The etching rate of various Si oxide films is affected by the NH_4F concentration in BHF as shown in Fig. 7. Figure 8 shows the relationship between the surfactant concentration in 630BHF and the etching rate of various Si oxide films. The addition of anionic surfactant does not affect the etching rate of thermal SiO2, PSG and BSG film, although the etching rate of each Si oxide film decrease by an addition of more than 200 ppm cationic surfactant. The uniformity of etching was also degraded by the addition of cationic surfactant. It is considered that the cationic surfactant adsorbs more easily on the Si oxide film surface than the anionic surfactant.

Here, we consider a possible mechanism of suppressing the microroughness generation on the Si wafer surface by the addition of the surfactants. Since the pH value scarcely changes by the surfactant addition, the ionic equilibrium in BHF solution is considered not to be affected by the surfactant addition. Therefore, the interruption of Si dissolution by the surfactant adsorption on the Si wafer surface is considered to be the mechanism. If the surfactant molecules are adsorbed on the Si wafer surface according to the Langmuir type adsorption equation(8), coverage(θ) of the surfactant molecule is given by

$$\theta = KC/(1+KC) \qquad [1]$$

where C is the concentration of the surfactant and K is the adsorption equilibrium constant. Moreover, if the dissolution of Si from the surface is suppressed where the surfactant molecules are adsorbed, the amount of dissolved Si(D_{Si}) is given by

$$D_{Si} = D_0(1-\theta) \qquad [2]$$

where D_0 is the amount of dissolved Si in case of no addition. From Eqs. 1 and 2, D_{Si} is given by

$$D_{Si} = D_0/(1+KC) \qquad [3]$$

Solid lines in Fig. 3(b) show the calculated value using Eq. 3. There is a very good agreement between experimental and calculated values. Used value of constant K is given in Table I. Accordingly, the adsorption of the surfactant molecules on the Si wafer surface can be described by the Langmuir type adsorption, and the effect of surfactants on suppressing the microroughness generation in BHF can be explained by the suppression of Si dissolution which is owing to the adsorption of the surfactant molecules on the Si wafer surface.

Conclusions

It was found that the generation of microroughness on the Si wafer surface in BHF was prevented by a several 10 ppm order addition of surfactant. It was confirmed that the effective prevention of the microroughness generation was observed by 50 ppm addition of hydrocarbon anionic and perfluorocarbon anionic surfactant. It was also found that the microroughness generation was suppressed by lowering the NH_4F concentration in BHF and the dissolution of Si which causes the microroughness generation on the Si wafer surface depended on the OH^- concentration rather than on the HF concentration in BHF. For the studied concentration range of NH_4F and HF in BHF, the hydrocarbon anionic surfactant is effective for the suppression of the

microroughness generation. The suppression of the microroughness generation is owing to the surfactant molecules which suppress the dissolution of Si into BHF from the Si wafer surface. The adsorption of the surfactant molecules on the Si wafer surface can be expressed by the Langmuir type adsorption equation.

Acknowledgment

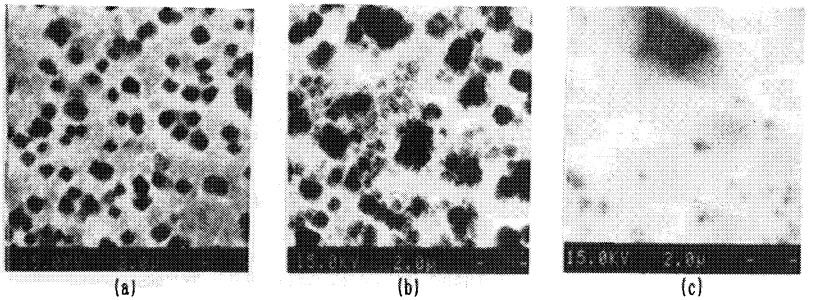
The authors wish to express their gratitude for the encouragement of Prof. S. Ono of Tohoku University in executing their study. They also would like to thank Assoc. Prof. J. Murota and Assoc. Prof. T. Matsuura of Tohoku University for their useful discussions and valuable advices.

References

(1) M. Miyashita, M. Itano, T. Imaoka, I. Kawanabe and T. Ohmi, 1991 Symposium on VLSI Technology, Oiso, p. 45 (1991).
(2) M. Miyamoto and T. Tatsuno, Extended Abstract, The 40th Spring Meeting of The Japan Society of Applied Physics and Related Societies, 29P-ZW-10 (1993).
(3) H. Kikuyama, N. Miki, K. Saga, J. Takano, I. Kawanabe, M. Miyashita and T. Ohmi, IEEE Trans. Semiconductor Manufacturing, 3, 99 (1990).
(4) Y. Kawazawa and T. Tatsuno, Extended Abstract, The 50th Autumn Meeting of The Japan Society of Applied Physics, 27P-B-15 (1989).
(5) Y. Nakamura, S. Shigemori, A. Watanabe, M. Matsubara and K. Okamoto, Extended Abstract, The 52th Annual Meeting of The Japan Analytical Chemical Society, 1A12 (1991).
(6) E. D. Palik, H. F. Gray and P. B. Klein, J. Electrochem. Soc., 130, 956 (1983).
(7) H. Nielsen and D. Hackleman, J. Elctrochem. Soc., 130, 708 (1983)
(8) I. Langmuir, J. Am. Chem. Soc., 38, 2221 (1916).

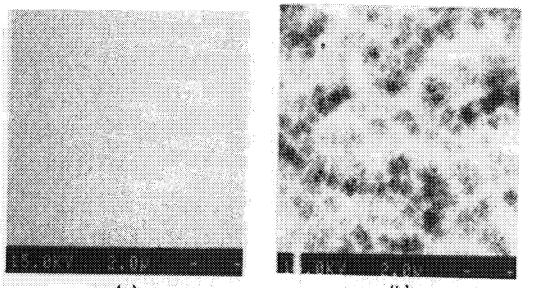
Table I. Adsorption equilibrium constant K in Eq. 3 used for fitting the data in Fig. 3 (b).

Kind of surfactant	Type of wafer	Value of K ($\times 10^6 cm^3/g$)
Perfluorocarbon anionic	P (100)	0.2349
Hydrocarbon anionic	P (100)	0.1875
	N (100)	0.1015
Hydrocarbon cationic	P (100)	0.0089
	N (100)	0.0072

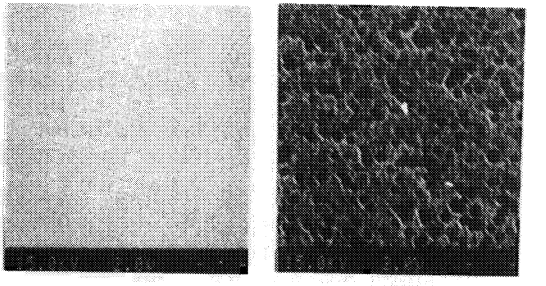


(a) (b) (c)

Fig. 1 SEM photographs of the Si wafer surface after immersed in 630BHF for 24 hours at 25 ℃. Wafer type is (a) P(100), (b) N(100), and (c) N(111).



(a) (b)



(c) (d)

Fig. 2 SEM photographs of the P type Si(100) wafer surface after immersed in 630BHF containing 100 ppm surfactant for 24 hours at 25 ℃. Surfactant type is (a) hydrocarbon anionic, (b) hydrocarbon cationic, (c) perfluorocarbon anionic with 2000ppm IPA, and (d) only . IPA(2000ppm) addition.

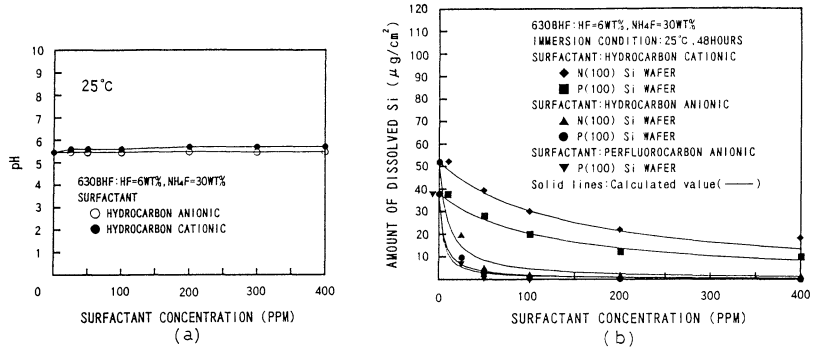


Fig. 3 Relationship between the concentration of surfactants and (a) pH and (b) the amount of dissolved Si in 630BHF.

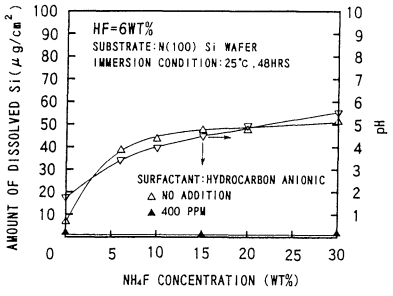


Fig. 4 Dependence of pH and the amount of dissolved Si after immersed in BHF on the NH_4F concentration in BHF.

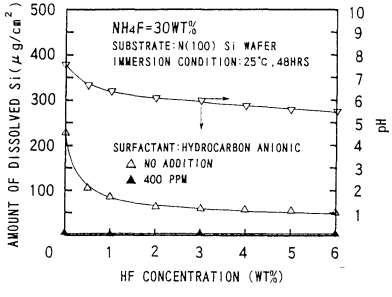


Fig. 5 Dependence of pH and the amount of dissolved Si after immersed in BHF on the HF concentration in BHF.

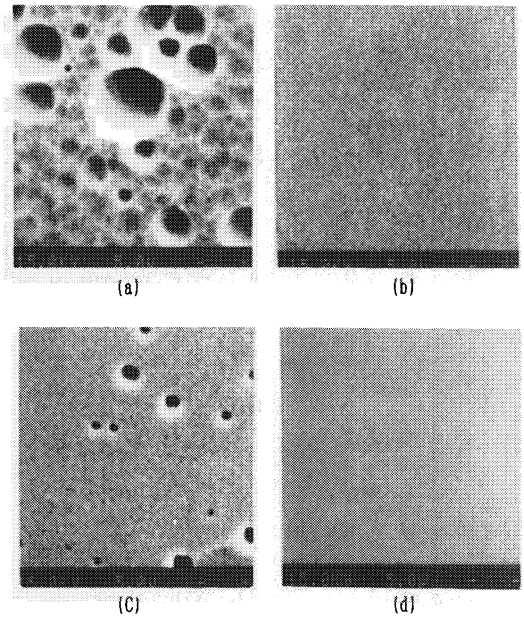


Fig. 6 SEM photographs of the N type Si(100) wafer surface after immersed in (a) 630BHF (HF=6wt%, NH_4F=30wt%), (b) 630BHF containing 400ppm hydrocarbon anionic surfactant, (c) BHF of low NH_4F concentration (HF=6wt%, NH_4F=15wt%), and (d) BHF of low NH_4F containing 400ppm hydrocarbon anionic surfactant for 120 hours at 25 °C.

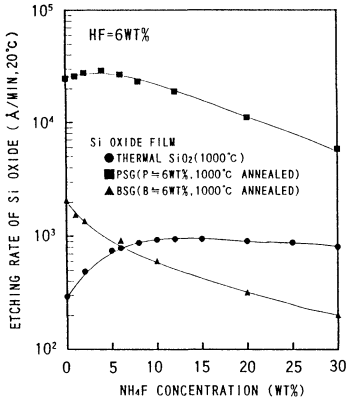


Fig. 7 Relationship between the etching rate of Si oxide films and the NH_4F concentration in BHF.

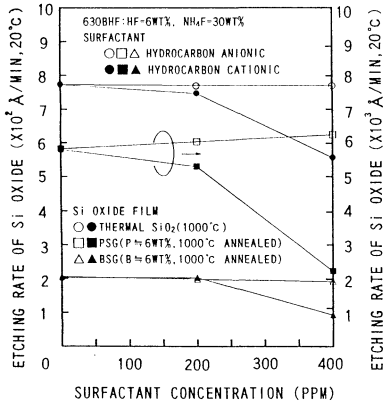


Fig. 8 Relationship between the etching rate of Si oxide films and the concentration of hydrocarbon anionic and cationic surfactants in 630BHF.

THE EFFECTS OF HF-CLEANING PRIOR TO SILICON WAFER BONDING

Karin Ljungberg, Ylva Bäcklund and Anders Söderbärg
Dept. of Technology, Uppsala University,
P.O. Box 534, S-751 21 Uppsala, Sweden

Mats Bergh and Mats O Andersson
Dept. of Solid State Electronics, Chalmers University of Technology
S-412 96 Göteborg, Sweden

ABSTRACT

The effects of different HF-cleaning solutions on silicon surfaces has been studied, by wafer bonding in room temperature together with surfaces analysis using AFM (Atomic Force Microscopy) and ESCA (Electron Spectroscopy for Chemical Analysis). The composition of the solution and the following water rinse, if any, have strong influence on the surface morphology, and hence the initial bonding. It was found that a solution of 10% HF in water gives an extremely smooth surface, and also the best bonding behaviour of the surfaces studied. A water rinse after the HF cleaning introduces surface particles, which are destructive for the bonding process.

INTRODUCTION

In the past few years there has been a growing interest in solid-state bonding of semiconductors. Bonding between surfaces of different materials can be achieved without external force, intermediate adhesives or applied electrical field. The process is amazingly simple; just press two surfaces, which however must be exceptionally clean and flat, together in room temperature, heat them to 500-1000°C, and the bond is completed. Since the first report on silicon wafer bonding, by Lasky and co-workers in 1985 [1], most bonding work published have dealt with hydrophilic surfaces, i.e. the wafers are covered by a thin, chemically grown oxide. It has been reported that hydrophilic surfaces are necessary for the initial, spontaneous bonding to occur, and that hydrophobic surfaces can only be bonded with the aid of an applied pressure [2,3]. In contrast, we have shown that spontaneous bonding occurs also for hydrophobic, oxide-free surfaces [4]. Bonding of silicon wafers without any interfacial oxide is important, e.g. for high power devices and as an alternative to epitaxial layers. Hydrophilic bonding always gives an interfacial oxide, resulting in an unacceptably high density of electron states at the interface [5].

OBJECTIVE

In this work, we have studied the effects of different HF-cleaning procedures on the initial bonding of silicon wafers. Since there are still different opinions regarding the possibility of achieving spontaneous hydrophobic bonding, we found a closer investigation of how the different cleaning processes affect the surfaces essential. As the initial bonding of hydrophobic surfaces is attributed to the relatively weak van der Waals forces [6,7], which do not reach very far, the bonding process is very sensitive to changes in the surface morphology and chemistry. Hence, room temperature bonding can be considered as a way to characterise surfaces. We have cleaned silicon wafers in a variety of HF-solutions prior to bonding, and related this to the spontaneity of the initial contact wave at room temperature. We have also characterised the cleaned surfaces with regard to surface roughness, chemical nature and particle density. The roughness was measured with an AFM (Atomic Force Microscope), and the chemical nature using ESCA (Electron Spectroscopy for Chemical Analysis). The particle density was estimated using dark field microscopy.

EXPERIMENTAL

The silicon wafers used in all experiments were 3-in, [100]-oriented wafers, with a thickness of 380±5 μm (Wacker, FZ, 10-12 Ωcm, n- and p-doped). All experiments were performed in clean-room environment. Prior to bonding, the wafers were etched for 1 minute in aqueous HF-solutions, having concentrations between 1 and 50%, or a HF-solution buffered with NH_4F to pH≈5 (BHF). Some of the wafers were carefully rinsed in DI water after the HF-etch, while others were not. All wafers were blown dry in N_2. As the wafers are contacted, the contact area spreads like a wave over the whole wafer. This "wave" was observed in transmitted IR-light, using an IR-camera and a video set-up, and the velocity of the wave front was determined. Normally, a slight pressure with the tweezers at the wafer edge was required to initiate the wave. If the contact area then grows without further help, the bonding is referred to as spontaneous.

An Atomic Force Microscope (AFM) was used to characterise the silicon surfaces regarding topography and roughness. In principle, the instrument acquires a picture of the sample surface by scanning a fine tip across it. The AFM (Park Scientific Instruments model SFM-BD2-210) operates at room temperature, under a flow of dry nitrogen gas. The instrument was used in the contacting mode, wherein the sample acts to deflect the Si_3N_4 tip and cantilever by a repulsive force. The topography of the sample is represented by the piezo driving voltage required to keep this deflection constant. The image processing behind the three-dimensional topographies in this paper is kept at a minimum, so that the pictures represent the surface topographies as closely as possible. The tip is scanned laterally across a 200x200 nm area of the surface, and the tip radius is nominally less than 40 nm. Each cleaning procedure were performed as described above immediately prior to the AFM measurement.

Chemical analysis of the surfaces was performed in a very sensitive ESCA-instrument (Scienta, ESCA-300), using Al Kα radiation [8]. The surfaces was again prepared as described above, and put into the vacuum chamber of the ESCA system within 30 seconds after blown dry. In this instrument the signal from glancing angles can be used, without loosing sensitivity [8]. The information thus originates from the outermost atom

layers only. In the measurements made in this work, a take off angle of 8° was used, corresponding to an information depth of 5-10 Å (i.e. 2-3 atom layers).

It has been shown [9] that the amount of particles on a hydrophobic, HF-etched, silicon surface increases if the wafer is immersed in either the HF-solution again, or in water. If so, repeated dipping would of course be deleterious to the bondability. To verify this theory, we estimated the particle density on an HF-cleaned silicon surface, immersed one or several times in H_2O. The liquid surface was intentionally contaminated with particles before immersing the wafers, to ensure that the particle density would be sufficient. The estimation was made using the dark-field mode of an Olympus BHT microscope.

Some bonding experiments were performed inside a bonding chamber, similar to the one described by Stengl et al [10]. In this set-up, the wafers to be bonded are placed over each other, with spacers in between, and then spin-rinsed, spin-dried, and bonded inside the chamber without opening it. Thereby neither the water nor the wafer surfaces will be exposed to the surrounding air (except for the small volume inside the chamber), and probably the particle contamination will be minimised.

RESULTS

Room temperature bonding

The spontaneity of the contact wave was strongly dependent on the cleaning procedure prior to bonding. The wafers which had not been rinsed in water after the HF-etch bonded spontaneously, while the rinsed wafers did not. These wafers could be pressed together, but they ended up with quite a large amount of voids (i.e. unbonded areas). In fig 1 are shown the measured contact wave velocities versus the concentration of the HF-solution for non-rinsed samples. As can be seen, the highest velocity was received for the 10% solution, while a concentrated (50%) solution gives surfaces that bond very slowly. The BHF-treated surfaces did not bond spontaneously.

AFM

In diagram 1 are the obtained RMS-values of the roughness before (black bars) and after (white bars) each treatment shown. It is obvious that increasing the concentration of the aqueous HF-solution will increase the resultant surface roughness. Between 10 and 50% this increase is larger than between 1 and 10%. A water rinse after the 10% HF-etch does not increase the surface roughness. The BHF-surface is also comparable to the one treated in 10% HF. The reproducibility of these results was found to be very good.

ESCA

The obtained spectra, taken in 8° take off angle, from the different surfaces are shown in fig 2 a-d. As can be seen, the chemical nature does not differ very much in the different cases. In good agreement with other researchers [11] we find the fluorine peak (F1S) at about 686 eV, the oxygen peak (O1S) at about 532 eV and the carbon peak (C1S) at 285 eV, for all concentrations. The strong HF-solution (fig 2a) yields a somewhat larger fluorine signal than the more diluted solution, which agrees with other reports [12]. The oxygen signal is large on the rinsed sample (fig 2c), due to native oxide growth. The carbon peak consists of signals from C-O, C-H and C-C. On the water rinsed samples the signal from oxygen bonded carbon (C-O) is considerably larger. Fluorine is mainly present as Si-F and O-F.

Particle contamination

Dark field micrographs of the surface cleaned in 10% HF before and after a water rinse, are shown in figure 3 a) and b). The particles were not homogeneously spread over the surface, why a representative part of the wafer area was chosen in each case. Nevertheless, it gives a fairly good picture of what happens during the cleaning steps. Remember though, that these are "artificial" particles densities, due to the particle addition. It is clearly visible that immersing the hydrophobic wafer into the H_2O-bath drastically increases the amount of surface particles. Covering the water surface with a thin layer of IPA (isopropanol) was found to substantially reduce this effect. After rinsing the HF-etched wafer in IPA/H_2O, the amount of particles was comparable to the non-rinsed hydrophobic surface. A hydrophilic wafer was found to be almost as particle-free after the rinse as before. These results are in good agreement with McConnel [9].

When using the bonding chamber, or "micro-cleanroom", the rinsed wafers were found to bond nicely, with no visible voids. This probably means that inside the chamber we can avoid particle contamination, which was not possible in the previous experiments. It also shows, that the particle contamination does not originate from the water itself.

DISCUSSION

HF-treated surfaces have been extensively studied, and are believed to be covered to about 90% by hydrogen [11, 12]. The initial bonding of hydrophobic surfaces is due to van der Waals forces [6,7]. As these forces do not reach far, the surface atoms must be brought very closely together for the room temperature bond to be possible. This makes extremely clean and smooth surfaces necessary. The chemical nature of the different surfaces studied in this work, as investigated with ESCA, do not differ very much. Hence, the variations in initial bonding behaviour cannot be explained by means of the surface chemistry.

The AFM results (diagram 1) show that the more concentrated the HF-solution, the rougher becomes the surface. This correlates well to the measured contact wave velocities (fig 1), measured for the aqueous HF-solutions, where the velocity is strongly dependent on the concentration. However, such a correlation cannot be seen for the non-spontaneously bonding, water rinsed, surfaces, for which the roughness was similar to that measured for non-rinsed surfaces.

The etch rate of silicon in an HF-solution is small, but measurable [13]. Our results, showing that the 10%-samples are smoother than the 50%-samples, may lead to the conclusion that the latter one is etched faster, thus ending up with a rougher surface. However, it has been found that the etch rate of silicon in a concentrated, strongly acidic, HF-solution is so small that it is basically inert and only the native oxide is removed [14,15]. An explanation based on the etch mechanism is given: The etching proceeds in two steps, oxidation of the hydrogen-terminated silicon surface by water molecules in the solution, and removal of this oxide by the HF-molecule [15]. Thus the etch rate is depending on the OH^--concentration, and therefore higher in a more diluted, or rather less acidic, solution. This might explain our observations: in a concentrated solution the etch rate is so small that the roughness of the original native oxide/silicon-interface is maintained, while etching in the diluted solution has a "polishing" effect. Another explanation might be that the higher concentration etches defects, such as dislocations, twins, etc. The rough surface after 50% might thus be a result of defect decoration.

The effects of treatment in HF and BHF-solutions on the silicon surface morphology have been studied by several researchers [14,15]. It has been found that an aqueous HF-solution, having a pH between 1 and 2 (corresponding to concentrations of 50 down to 1% HF), probably etches silicon in an isotropic way, while buffering the solution with NH_4F results in an etching anisotropy, which is increasing with pH [14,15]. For more alkaline solutions, this will result in atomically smooth (111)-surfaces, and consequently (111)-facets on a (100)-surface. The number of contact points between the BHF-treated (100)-surfaces will therefore become small, which might explain the observed non-spontaneous bonding of the surfaces treated in BHF. However, this could not be seen in the investigations made here.

A water rinse does not increase the roughness of the HF-etched surface, according to the AFM-measurements. The ESCA-measurements showed a larger oxygen signal, but this should not have any influence on the bonding behaviour, as hydrophilic, native oxide-covered surfaces can very well be bonded [e.g. ref.1]. Hence, there must be another reason for the observed non-spontaneous initial bonding. McConnel state, that particles stick to the surface when the wafer passes the air/liquid interface, due to the downwardly bent liquid surface [9]. The liquid surface is extended down with the wafer, so that surface particles, originating from the air, are transferred to the silicon wafer surface. One way to avoid this effect was shown to be a thin layer of IPA (isopropanol) on the water surface [9]. Our results confirm this, and thus the problem seems to be solved. The use of a bonding chamber like the one presented by Stengl et al [8], in which the wafers to be bonded are rinsed and spin-dried in a "micro-cleanroom", would also be a solution to the particle problem. The wafers will not pass an air/liquid interface like if dipped into a beaker, and any possible particles inside the chamber would probably be unable to stick to the rotating wafers. Our results, showing a very good room temperature bond after rinsing and bonding of hydrophobic surfaces in such a chamber, support these theories. There were no presence of voids, as have been observed in the case of "ordinary" water rinsing, and the surfaces bonded – as far as can be seen – spontaneously. This leads to the conclusion that the main reason to the observed non-spontaneous bonding of water-rinsed wafers is due to surface particles, but also that the problem quite easily can be avoided. Of course the application must be considered, since a water rinse will influence the electrical properties of the bonded interface [16].

CONCLUSIONS

The chemical nature and morphology of the silicon surface is strongly dependent on the HF-cleaning procedure, considering both the composition of the HF-solution and the subsequent water rinse, if any. Extremely smooth and clean surfaces are necessary for the initial room temperature bonding between hydrophobic surfaces. There are many surface parameters influencing the initial contact wave, mainly the surface roughness and presence of particles. The best surface preparation for achieving a spontaneous, voidless bond in room temperature, is etching in a solution of 10% HF in water, with no subsequent water rinse. A water rinse will introduce particles on the hydrophobic surfaces. As long as the electrical properties of the bond are not critical, this is however an avoidable problem, e.g. by using spin-rinse and -dry or adding isopropanol to the rinse bath. A buffered HF-solution (with a pH of about 5) gives surfaces that do not bond spontaneously.

ACKNOWLEDGEMENTS

This work was financed by a grant from the Swedish board for Industrial and Technical Development (NUTEK). The authors wish to thank Björn Wannberg and Prof. Ulrik Gelius at the dept. of Physics, Uppsala University, for making the ESCA analyses. Special thanks also to Stefan Bengtsson, at Chalmers University of Technology, for assistance in the laboratory work, and for fruitful discussions. Prof. Bertil Hök is acknowledged for encouragement and support.

REFERENCES

[1] J.B. Lasky, S.R. Stiffler, F.R. White and J.R. Abernathey, IEDM Tech. Dig. p. 684 (IEEE, New York, 1985)
[2] W.P. Maszara, J. Electrochem. Soc, **138**, p. 341 (1991)
[3] S. Bengtsson and O. Engström, J. Appl. Phys. **66**, p. 1231 (1989)
[4] K. Ljungberg, A. Söderbärg and Y. Bäcklund, Appl. Phys. Lett. **62**, p. 1362 (1993)
[5] S. Bengtsson and O. Engström, Proceedings of the 180th Electrochemical Society Meeting, edited by U. Gösele, T. Abe, J. Haisma, and M.A. Schmidt (The Electrochemical Society, Pennington, NJ, 1992) vol 92-7, p. 18
[6] Y. Bäcklund, K. Ljungberg and A. Söderbärg, J. Micromech. Microeng. **2**, p.158 (1992)
[7] G.A.C.M. Spierings and J. Haisma, in ref 5, p.18
[8] U. Gelius, B. Wannberg, P. Baltzer, H. Fellner-Feldegg, G. Carlsson, C-G. Johansson, J. Larsson, P. Münger and G. Vegerfors, J. Electr. Spectr. and Rel. Phen. **52**, p. 747 (1990)
[9] C.F. McConnel, First Int. Symp. on Ultra Clean Processing of Silicon Surfaces (UCPSS'92), 17-19 Sept 1992
[10] R. Stengl, K.-Y. Ahn and U. Gösele, Jpn J. Appl. Phys. **27**, L 2364 (1988)
[11] L.A. Zazzera, and J.F. Moulder, J. Electrochem. Soc. **136**, p. 484 (1989)
[12] J.M.C. Thornton and R.H. Williams, Semicond. Sci. Technol. **4**, p.847 (1989)
[13] W. Hoffmeister and M.Zügel, Int. J. Appl. Radiat. Isotopes **20**, p.139 (1969)
[14] H.E. Hessel, A. Feltz, M. Reiter, U, Memmert and R.J. Behm, Chem. Phys. Lett.186, p.275 (1991)
[15] G.S. Higashi, Y.J. Chabal, G.W. Trucks, and Krishnan Raghavachari, Appl. Phys. Lett. **56** (7), p.656 (1988)
[16] K.Ljungberg, A.Söderbärg, S.Bengtsson and A.Jauhiainen, Proceedings of the 183th Electrochemical Society Meeting, Honolulu, Hawaii, May 16-21, 1993

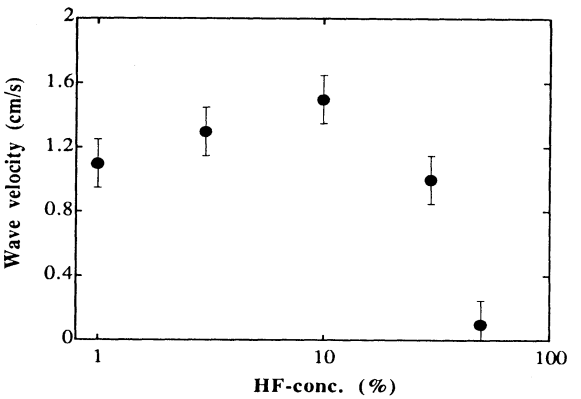


Figure 1. The contact wave velocity for room temperature, spontaneuos bonding, versus the concentration of the HF etch-solution prior to bonding.

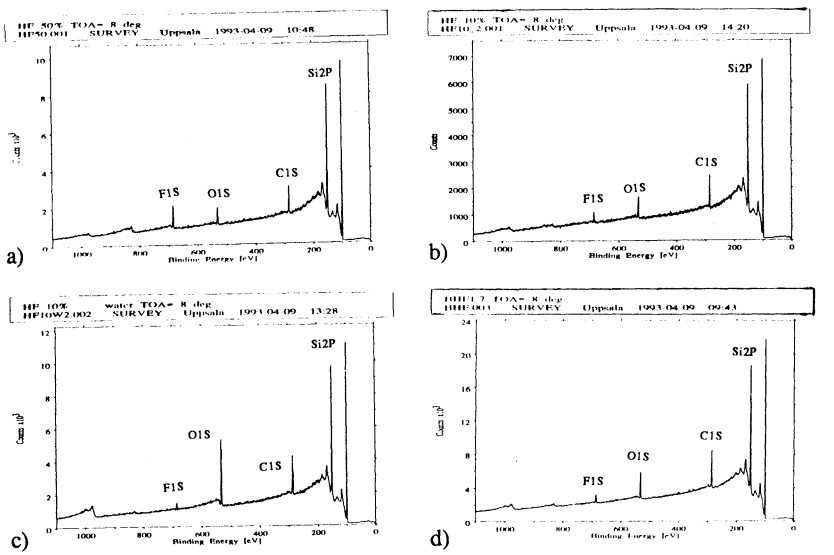
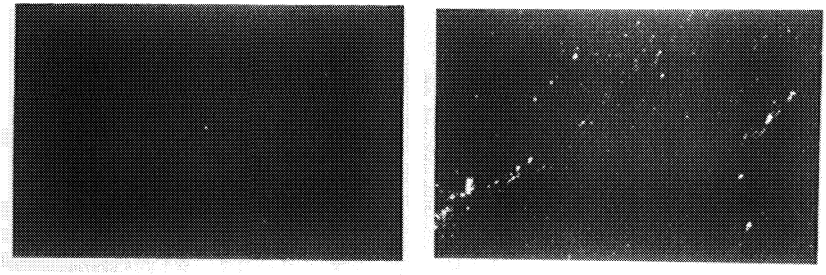


Figure 2. ESCA spectra of silicon surfaces treated in a) 50% HF, b) 10% HF, c) 10% HF plus a water rinse and d) buffered HF (BHF).



a) b)

Figure 3. Micrographs taken in dark-field of wafers etched in a) 10% HF and b) 10% HF with a subsequent water rinse. The surfaces of both the HF-solution and the rinse water where intentionally contaminated with particles.

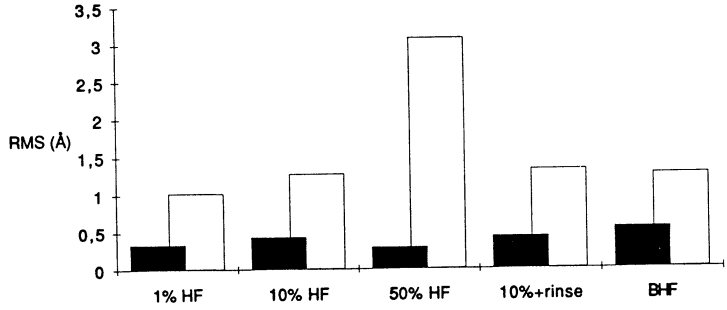


Diagram 1. The RMS-values of the surface roughnesses as measured in an AFM before and after each treatment.

GAS-PHASE CLEANING

VAPOR PHASE HF CLEANING IN CMOS PRODUCTION

Sean O'Brien, Brynne Bohannon, Marylyn Hoy Bennett,
Charlotte Tipton, and Allen Bowling

Texas Instruments,
Semiconductor Process & Design Center
PO Box 655012 MS 944,
Dallas TX 75265

Vapor HF processes replaced all aqueous HF processes required for the manufacture of the Microelectronics Manufacturing Science and Technology (MMST) single-wafer processing CMOS device. Traditional applications included removal of 1) sacrificial oxides 2) nitride formed between the sacrificial oxide and silicon substrate during the tank drive process and 3) oxynitride layer formed over nitride during the LOCOS isolation process. Vapor HF was also used as a post-etch residue removal eliminating the need for some acids and organic solvents. The MMST goals of single-wafer gas phase cleaning, fast cycle time and high equipment availability were all easily met by these processes. In addition, process enhancements such as elimination of subsequent process steps and reduced cost of ownership make vapor HF a beneficial alternative to aqueous HF processing.

Introduction

The elimination of wet chemical processing is a key goal for 21st century semiconductor processing. Process requirements for sub-half micron technology along with chemical consumption and waste disposal costs are driving us toward replacing liquids with gases. In addition the requirements of fast cycle time and single wafer cleaning set forth by the MMST program at TI (1) are best met with dry processing. Currently, most dry cleaning technology will not support manufacturing requirements, but vapor HF cleaning is an exception. Aqueous HF and most solvent processing can be eliminated today by implementing typical vapor HF cleaning processes.

Aqueous HF is one of the most common chemicals used for manufacture of CMOS devices. A typical CMOS device flow will have more than 15 HF process steps. While aqueous HF processes typically do not have batch loading effects that increase processing times, they usually require subsequent wafer cleaning to reduce unacceptable particle levels. The vapor HF process is so clean that additional particle removal processes can be eliminated, dramatically lowering cycle time. The net result is a fast, clean process free of liquid chemicals.

Equipment

The tool used for vapor HF cleaning is an FSI Excalibur ISR (in situ rinse). This is a single wafer process tool operating at atmospheric pressure. The wafer is loaded into a chamber in which HF, N_2, and H_2O vapors are introduced. All processes used for this work are essentially identical. First is a pre-treatment purge step with dry N_2. HF and H_2O vapor are then introduced into the chamber where the wafer is spinning at 100 RPM. HF, N_2, and H_2O vapor flow rates are adjusted to control oxide removal. After the etch is finished a post-treatment purge step with dry N_2 followed by a liquid water rinse is used to remove etch residue. The wafer is then dried with a combination of high spin speed and dry N_2 purging. HF concentration instead of exposure time is typically adjusted to control oxide removal. This is contrasted with aqueous HF where concentration is strictly controlled and exposure time is varied. A JEOL 845 scanning electron microscope was used for all micrographs contained within this paper.

Process time

Wafer processing with vapor HF is significantly faster than with aqueous HF due to the elimination of the subsequent SC1/megasonic clean, rinse, and spin-dry. These extra processes are required for wet HF processing to achieve comparable particle levels. Analyzing the cycle time and throughput of a single wafer cleaning tool is non-trivial (2) so the batch cycle time of a 24 wafer lot is given in Table 2 with no consideration of single-wafer processing.

Table II Cycle Time for HF Processing

Clean	Cycle Time (min)
Vapor HF	24
Aqueous HF - Megasonic - SRD	41

Cost of Ownership

For a cost of ownership analysis a comparison between vapor HF and aqueous HF processing is given in Table 3. Details are dependent on each facility, but clearly the elimination of procurement and disposal of wet chemicals makes vapor HF a much more economical and environmentally friendly process.

Table III Cost-of-Ownership for HF Processing

	Aqueous HF *	Vapor HF
Capital cost (k$)	500	400
Footprint (ft^2)	42	25
Chemical usage (gal/day)		
H_2O	3000	171
HF	12	1+
NH_4OH	12	0
H_2O_2	12	0
disposal	36	0

* Process flow is HF - rinse - SC1/megasonic - rinse - spin rinse dry
+ lbs per 1000 wafers

Implementation into MMST Processing

Oxide Strip

Stripping of sacrificial oxides is a standard process requiring little development for the switch to vapor HF. Several different oxide layers ranging in thickness from 90Å to 250 Å are used as diffusion barriers, polysilicon sticking layers, and dummy gate oxides. When the oxide thickness approaches a few monolayers the effective etch rate slows down, leading to a requirement of an over etch beyond the level needed to compensate for oxide thickness variation. This is best described as the difference in etch rates between thin sacrificial oxide and thick field oxide. These are equal until the thin oxide approaches 100 Å, where the field oxide etches faster than the thin sacrificial layer. Compensation for this is easily achieved by increasing the etch time. This can lead to excess removal of field oxide, so the grown field oxide thickness must take into account all oxide removed during sacrificial oxide stripping.

Gate Oxide Integrity (GOI) testing showed little significant difference between vapor and aqueous HF. Table 4 lists several different methods of measuring GOI. It is important to note that only the pre-gate clean was vapor HF. The 2 previous deglazes in the pilot wafer flow were run with aqueous HF which can distort the results of the pre-gate oxide deglaze. Subsequent GOI work confirms that vapor HF is superior to aqueous HF if done for all deglazes.

Table IV GOI for HF Processing

Clean	Def Density (cm^{-2})	VBD (Volts)	QBD (C/cm^2)	
			50 %	Best
Vapor HF	60.4 ± 24	7.41 ± 3.7	8 ± 2	25 ± 2
Aqueous HF	73.3 ± 41	6.68 ± 4.1	22 ± 3	33 ± 1

All GOI data is measured on 191 0.01 cm^{-2} 120 Å oxide capacitors. Defect Density is calculated from the turnover point in a Weibull distribution plot of Breakdown voltage (VBD). Charge to breakdown (QBD) is measured with exponential ramped current. 50% point is median of QBD values, Best point is highest value for a single capacitor.

Nitride Strip

The tank drive process for MMST wafers includes NH_3 in the process gas, which creates a 20 Å layer of silicon nitride between the sacrificial oxide layer and the substrate silicon. (3) After the vapor HF deglaze process small circular regions of nitride remain which interfere with the growth of the subsequent sacrificial oxide. As seen in Fig. 1 these defects resemble liquid residue or watermarks, but the root cause is incomplete removal of this thin nitride layer.

This nitride layer is easily removed with aqueous 10% HF, but the selectivity of oxide to nitride is much higher with vapor cleaning. The process occurs on unpatterned wafers and an extreme overetch has no deleterious effects on the wafers. The thin nitride layer is totally removed with this overetch.

Oxynitride Strip

Any sacrificial nitride layer must be cleared of its thin coating of oxynitride before stripping in either phosphoric acid or a dry plasma etch. (4) The nitride layer is not sensitive to overetch; however, the field oxide is exposed and any overetch must be carefully controlled.

A liquid residue problem may be found on vapor processed wafers where adjacent regions of nitride and oxide geometries intersect. At the interface region between the 2 films, large (100 μm) diameter rings are seen on most wafers. Figure 2 shows typical watermarks seen on patterned wafers. Adding a subsequent SC2-SC1 clean in a wet bench in addition to changing the rinse cycle eliminates the residue problem.

Polysilicon etch clean

Tight critical dimension (CD) control over polysilicon linewidths requires operation of the plasma etcher in a mode which deposits sidewall passivation polymer. (5) This deposited polymer is predominantly SiO_2 and is traditionally removed using a sulfuric acid (piranha) resist strip followed by an SC1 megasonic. Figure 4 shows residue typically found after an inadequate piranha clean. Extending the process time proved unacceptable due to lengthy process times and inconsistent removal of the polymer. Inserting a vapor HF process in between 2 short wet cleans gave a faster overall process time and consistent removal of the etch residue. Table 5 compares processes used for removing this polymer deposit.

Table V Process Time for Post Polysilicon Etch Clean

Process	Time	Total*	Process
Piranha + SC1 Strip		60	Marginal
Acid	20		
SC1	20		
Wet - HF - Wet		37	Excellent
Acid	15		
SC1	5		
Vapor HF	2		
Acid	3		
SC1	3		

All times in minutes
* Single wafer process time includes water rinses and spin dry.

Metal etch clean

For post-metal etch, HF vapor cleaning is preceded by an O_2 ash. The vapor HF process removes the etch residues providing a robust and efficient process while eliminating the need for traditional organic solvents. (6) Fig. 2 shows before and after SEM cross sections showing the impact of vapor HF on this residue.

Contact etch clean

Prior to Ti sputter deposition the exposed silicon substrate in the contacts must be deglazed to minimize resistance caused by native oxide and ash residues. This clean also removes any remaining traces of resist residue remaining after the contact plasma etch. A short vapor HF clean removes the last trace of ash residue, and deglazes the

substrate without significantly increasing contact CD's. Table 5 shows excellent contact resistance was achieved on several MMST lots indicating the process capability can support high yield.

Table V Contact resistance

Clean	Contact Resistance *
Aqueous HF	1.35 ± 0.094
Vapor HF	1.00 ± 0.12

* Resistance normalized, measured in ohms on chain with 280 polysilicon contacts

ACKNOWLEDGMENTS

We would like to thank James Cates, Steve Strattman, and Annette Walder for their support of the work described here. This work was supported in part by the Air Force Wright Laboratory and the ARPA Microelectronics Technology Office under contract F33615-88-C-5448.

REFERENCES

1 M. Moslehi, C. Davis, and R. Bowling, Texas Instruments Technical J., 9(5), 44 (1992).

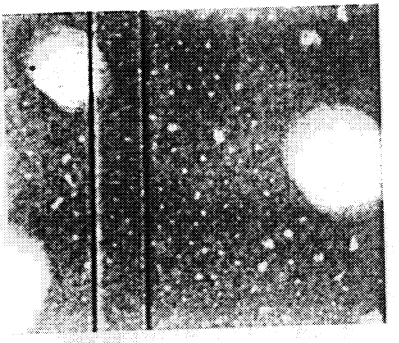
2 S. O'Brien, B. Bohannon, M. Bennett, C. Tipton, and R. Bowling, presented to MICROCONTAMINATION '93, Sept. 1993.

3 M. Moslehi, C. Han, K. Saraswat, C. Helms, and S. Shatas, J Electrochem. Soc., 132(9), 2191 (1985).

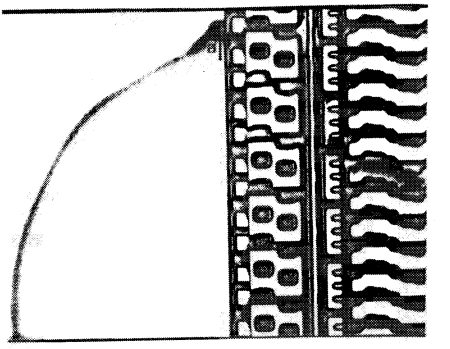
4 L. Loewenstein and C. Tipton, J Electrochem. Soc., 138(5), 1389 (1991).

5 H. Denton and R. Wallace, in Advanced Technology for Integrated Circuit Processing II, PV 1803, Proceedings of the SPIE - The International Society for Optical Engineering, San Jose, CA (1992).

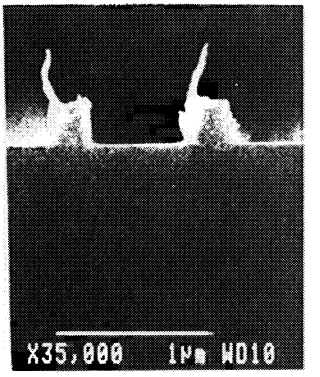
6 B. Bohannon, R. Bowling, B. Poarch, R. Wallace, and D. Syverson, submitted to IES (1993).



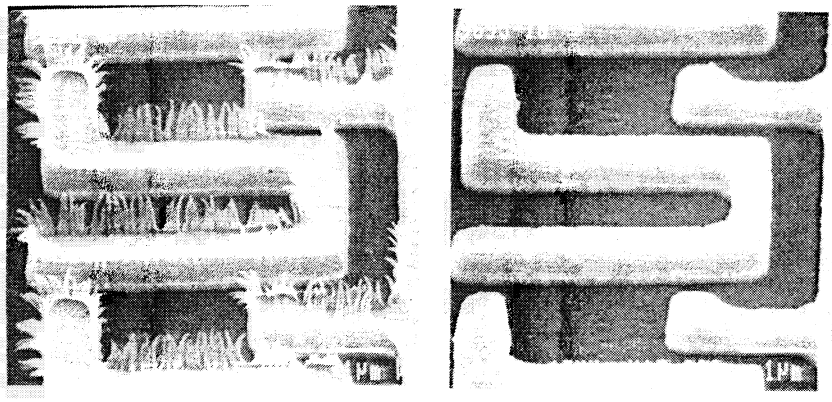
1. Spot defects found after tank oxide deglaze, root cause is incomplete removal of nitride film formed during tank drive.



2. Liquid residue defects seen on patterned wafers. Residue is probably a fluosilicic acid polymer.



3. Polymer residue seen after polysilicon etch. Piranha - vapor HF - piranha clean sequence efficiently removes this.



4. Scanning electron micrographs of TiN/AlSiCu/TiN metal stack after reactive ion etch, in situ resist ash, pre (left) and post (right) etch rinse using vapor HF process. Etch residue is seen as grassy form.

A HF VAPOUR ETCH PROCESS FOR INTEGRATION IN CLUSTER-TOOL PROCESSES: CHARACTERISTICS AND APPLICATIONS

W.J.C. Vermeulen, L.F.Tz. Kwakman, C.J. Werkhoven and E.H.A. Granneman
ASM International, Rembrandtlaan 2a, 3723 BJ Bilthoven, The Netherlands
and
S. Verhaverbeke and M. Heyns
IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

The effects of process parameters on the HF-H_2O vapour phase oxide etch characteristics have been studied. The most important factors, e.g. etch rate, inhibition and selectivity, turn out to be largely influenced by the selection of one of the three established etch regimes, viz. a gasphase, an enhanced adsorption or a condensation regime.
By integrating the HF vapour etch process with LPCVD processes in a load-locked, vacuum operated cluster tool, significant process improvements can be achieved in critical device fabrication steps such as the formation of poly-contacts, poly-emitters and NO capacitors, provided the proper etch regime is selected.

INTRODUCTION

For the successful fabrication of advanced IC's, adequate control over some of the critical production steps is a prerequisite. The continuous trend towards an increased level of integration and better device performance demands thinner films for the construction of active components. Since device characteristics have to be reproducible and well controlled, the need for thinner films not only puts more stringent requirements on the film properties themselves but also on the control of the interface of such films with the underlying substrate surface. In Bipolar and CMOS technologies, interfaces between silicon and thin films are amongst the most critical. For silicon surfaces, one effective way to improve the interface quality is to remove any unwanted native or chemical oxide prior to a LPCVD or oxidation process and to avoid re-contamination of the wafers during wafer transport and heat-up.

To achieve this, a low pressure gaseous HF etch process is developed in a reactor that is integrated in a vacuum operated cluster tool equipped with LPCVD and oxidation reactors. The vacuum integration of this HF vapour process prevents regrowth of the native oxide prior to subsequent processing. The HF etch process itself removes surface oxides at room temperature and reduced pressure using a mixture of anhydrous HF gas and H_2O vapour. The characteristics of this etch process are determined by the exact choice of the process parameters, viz. flow rate, flow ratio and total pressure.

While the target of the etch process is to render silicon surfaces hydrophobic, i.e. free from oxide and properly passivated, it has to meet other boundary conditions as well: first, for several applications, etching of other exposed oxides should be minimized to

avoid unwanted side effects such as undercutting and, eventually, circuit shorting. Therefore, etch selectivities, oxide specific etch-inhibition and (local) loading effects have to be optimized. Second, the process can only qualify for production if throughput, controllability and reproducibility are demonstrated. In this study the process parameter space is investigated in terms of above mentioned target and boundary conditions.

THEORETICAL CONSIDERATIONS

Etching of SiO_2 layers in liquid HF is a well characterized chemical process that is widely used in the fabrication of integrated circuits (1). Compared to the liquid based process, HF vapour phase etching of SiO_2 is a relatively new technique that only recently started to receive much attention. Although detailed knowledge on this new process is still lacking, several characteristics have been consistently reported by various groups. First, it is observed that exposure of SiO_2 to anhydrous HF yields etch rates that are very low and critically depending on the background moisture level in the etch ambient (2). It is found that a mixture of HF and H_2O is required to obtain higher and better controlled etch rates (3,4). Second, depending on the type of oxide and its treatment prior to HF etching, etch rates and etch inhibition times may vary significantly (5).

Explanations for these experimental observations are generally based on a differentiation between a true gas phase regime and a condensation regime. In the gas phase regime, etching is taking place via a slow gas-solid reaction that is catalyzed by adsorbed moisture on the oxide surface. In the condensation regime, the process conditions are such that the HF/H_2O vapour condenses as a liquid film onto the oxide surface, and etching actually proceeds in a similar way as for liquid solutions. A comprehensive study of the HF/H_2O vapour etch process is published by Helms and Deal (6).

Given the fact that sorption and condensation mechanisms are critical steps in the overall etch process, it can be concluded that a more in depth analysis of these phenomena is needed in order to be able to control the process to a level that meets the stringent industrial requirements. Below, the sorption characteristics of the binary HF/H_2O vapour mixture onto SiO_2 are reviewed from a theoretical point of view.

Physical adsorption

Independent of possible chemical reactions taking place, the HF/H_2O vapour can physically adsorb onto a SiO_2 surface. Whereas in many situations the thickness of the adsorbate is limited to one monolayer (Langmuir adsorption), this thickness can become a few monolayers (BET adsorption) when polar molecules such as H_2O or HF are involved (7). In equilibrium, the number of adsorbed molecules per unit area, N_s, is determined by the vapour pressure (p), the sticking coefficient (s), the vapour temperature (T_g) and the substrate temperature (T_s) and can be expressed as:

$$N_s = \text{Const.} \cdot p \cdot s \cdot \exp(Q/RT_s) \; / \sqrt{(M.T_g)} \qquad [1]$$

For sub monolayer coverages, the sticking coefficient (s) is a function of the number of

available adsorption sites. Furthermore, for Langmuir and BET adsorption the binding energy (Q) is determined by the existing adhesion and cohesion forces, respectively. In figure 1, typical Langmuir and BET adsorption characteristics are shown as a function of p/p_s, i.e. the ratio between the vapour pressure and the saturation pressure at which condensation occurs. From this figure it can be concluded that for pressures well below the saturation pressure adsorption is limited to sub monolayer coverage. On the other hand, for BET adsorption an appreciable amount of vapour can be adsorbed at pressures still below the condensation pressure.

Based on these considerations it is plausible that, indeed, the HF/H_2O vapour phase etching is impaired at very low HF and H_2O pressures due to a lack of adsorption. Using the same reasoning, it can be expected that, if multilayer BET adsorption is assumed, appreciable etching already starts at pressures still below the saturation pressure. This could be of practical importance since etching in the condensed phase is known to leave residues that are difficult to remove in the vapour phase (8).

HF/H_2O phase diagram

In order to arrive at etch conditions where multilayer adsorption is expected to take place, the saturation pressure needs to be known. The saturation pressure of the HF/H_2O vapour mixture is a function of temperature and the composition of the mixture. Due to the strong interaction between HF and water, the mixture does not behave as an 'ideal gas' but shows azeotropic behaviour with a maximum boiling point for a mixture containing $\approx$ 38 mol% HF. In figure 2, the HF/H_2O phase diagram, reconstructed from data published by Munter et al. (9), is shown for a temperature of 25 °C. In this diagram, the pressures at which condensation or evaporation takes place are indicated by the vapour and liquid lines, respectively.

Factors affecting etch rate / uniformity

So far, only adsorption of HF/H_2O has been considered, neglecting the effects of the etch reaction itself. In the absence of water the gaseous etch reaction is thought to occur via the following, overall reactions

$$SiO_2 + 6HF \Leftrightarrow 2H_2O + 6H_2SiF_6 \qquad [2]$$

$$SiO_2 + 4HF \Leftrightarrow 2H_2O + SiF_4 \qquad [3]$$

An important step in the overall etch reaction, the (dissociative) adsorption of HF onto SiO_2, is catalyzed by hydroxyl groups or traces of moisture present or created at the surface. Since water is liberated, the reaction is autocatalytic. Clearly, when no H_2O is added to the gas ambient, etch rates and inhibition times are strongly affected by the surface and bulk properties of the oxide being etched. Under such conditions, controllability of the etch process is difficult to achieve. By deliberately adding water to the vapour ambient, better control of the adsorption/desorption steps can be obtained. If the H_2O surface concentration is increased by adsorption from the vapour phase, HF adsorption is enhanced and less sensitive to the accidental presence of moisture on the SiO_2 surface. Furthermore, if the H_2O surface concentration is primarily determined by the adsorption from the vapour phase and not by the reaction, it does not increase significantly as etching proceeds, thus, the rate of the autocatalytic reaction is better controlled as well.

Although the addition of water may lead to a better controlled process in terms of inhibition and etch rate, one has to be careful in the selection of the etch conditions. When adding H_2O to the HF vapour, the saturation pressure of the mixture is significantly lowered and, depending on the choice of the process pressure and temperature (eq.[1]), etching may take place in a gas phase, multilayer adsorption or condensation regime. In the latter two regimes the etch rate may be much higher and, if so, sufficient supply of the reactants is required to minimize etch non uniformity due to depletion effects.

Because the etch characteristics in each of these regimes are difficult to predict from a theoretical point of view, experimental studies are required to explore the process window in more detail.

EXPERIMENTAL

Equipment description

For the characterization of the HF/H_2O vapour etch process, an ASM Advance 600/2 vertical reactor cluster system was used. The cluster system consists of a central wafer handling platform via which four process modules are integrated. Wafer transport from one process module to the next takes place in a reduced pressure ambient of high-purity nitrogen. Typical leak-in and desorption rates of 10^{-3} Pa.l/s, ensure the internal contamination background level to be better than 10^{-4} Pa.

All modules are batch type and for the LPCVD and oxidation processes, production-proven and well-characterized hot wall vertical reactors are used in which 100 wafers are stacked in a quartz boat positioned on a boat elevator.

The HF vapour etch module is a vertical batch reactor too, but cold wall and using a smaller number of wafers, typically 25, per process cycle. The reactor design includes a gas inlet section capable of delivering high vapour flows and a reactor geometry concept optimized for an uniform gas distribution across the wafers. Pressure control is realized by a closed loop system using a MKS throttle-valve in combination with a Baratron capacitance manometer for pressure readout. For this study, the H_2O and HF vapour flows were independently controlled by mass flow controllers. With this setup, the exact composition of the vapour mixture that is fed into the reactor can be easily varied over a wide range.

Experimental details

In this study, 150 mm p-type <100> silicon wafers were used as starting material. 100 nm thick thermal oxides were grown in the A600/2 oxidation reactor at 900 °C in a wet (83%) ambient. Thin chemical oxides were prepared by subjecting the silicon wafers to a full FSI-b clean (SP + HF + RCA). The thermal oxide wafers were used to monitor the etch process in terms of etch rate, uniformity and inhibition, while the FSI-b cleaned silicon wafers were used to monitor the effectiveness of native (chemical) oxide removal. The latter was checked by observing the dewet behaviour (hydrophobicity) of the etched surfaces after emerging in DI water. In some of the etch experiments undoped LPCVD TEOS oxide wafers, annealed for 30 minutes in N_2 at 850 °C, were included as well.

The amount of oxide removed in the HF vapour etch process was calculated from ellipsometric thickness measurements at a fixed refractive index of 1.46 before and after etching.

RESULTS AND DISCUSSION

Adsorption characteristics of HF/H_2O vapour mixtures

As mentioned earlier, multilayer adsorption might take place at pressures well below the saturation pressure. In order to verify this assumption experimentally, a number of simple adsorption experiments has been carried out for several HF/H_2O vapour mixtures. This was accomplished by feeding HF and H_2O vapour into the evacuated and isolated reactor chamber at a constant flow rate and recording the pressure increase ($\partial p/\partial t$). In figure 3, one of the experimentally determined $\partial p/\partial t$ curves is depicted. The curve can be interpreted as follows: the initial pressure increase is proportional to the filling time, i.e. $\partial p/\partial t = c$, in accordance with the ideal gas law if vapour adsorption is negligible. At the onset of enhanced adsorption (p_e), a significant amount of vapour is lost at solid surfaces as a consequence of which $\partial p/\partial t$ starts to reduce. Once the saturation pressure (p_s) is reached, $\partial p/\partial t$ becomes either zero for pure H_2O or an azeotropic mixture, or reaches a constant value again if the condensed liquid and the vapour have different compositions. As indicated in figure 3, the pressure interval where $\partial/\partial t\ (\partial p/\partial t) \neq 0$, has been defined as the enhanced adsorption regime.

The experimentally determined p_e and p_s values for several HF/H_2O mixtures are tabulated in table 1. Due to experimental constraints, these values are only accurate to within $\pm$ 10 %. The values found for p_s using this technique are in good agreement with those reported by Munter et al. Interestingly, for all vapour mixtures investigated, the onset of enhanced adsorption is observed at pressures around $(0.6 \pm 0.1)p_s$ which suggests that the enhanced adsorption regime is primarily related to the value of p_s and not to the exact vapour composition. This finding is visualized by the three regimes indicated in the phase diagram of figure 2. In regime I, the HF/H_2O mixture will not condensate nor adsorb to a large extend ($p < p_e$) whereas in regime III, the HF/H_2O mixture exists as a condensed liquid ($p \geq p_s$). In regime II, enhanced adsorption of the gaseous HF/H_2O mixture is expected ($p_e \leq p < p_s$).

It should be noted, though, that whereas both the reactor wall and 25 silicon wafers act as adsorption surfaces in this experiment, the actual p_e for SiO_2 surfaces might be different from the values reported in table 1: first, the sticking coefficients s_{wall}, s_{si} and s_{oxide} are not necessarily the same and second, since at the oxide surface etching occurs and, thus, SiF_x species are generated, the local adsorption conditions might be different due to the existence of a ternary system $HF\text{-}SiF_x\text{-}H_2O$. The latter effect, although insignificant at low HF concentrations, can not be ignored at higher HF concentrations.

Notwithstanding this limitation, the adsorption experiments have been useful to define the different etch regimes as will be demonstrated in the next sections.

Gas phase regime etching

If the etch process is intended to be used for native oxide removal on silicon, the target is to remove the native oxide completely while not etching other exposed oxides. In practice this means that the amount of other oxides etched should be controlled to a minimum (typically 5-20 nm). In this section the etch behaviour in the gasphase regime is presented in terms of etch rate, etch selectivity and inhibition effects.

First, the etch kinetics, i.e. the influence of p_{HF} and p_{H_2O} on the etch rate has been evaluated on thermal oxide. Although a detailed description of the reaction kinetics is beyond the scope of this paper, the experiments show that for total pressures < 0.4-0.5

p_s, the etch rate is proportional to both the HF and H_2O partial pressures. For total pressures approaching the value of 0.5-0.6 p_s, however, a transition to much higher etch rates is observed. This transition point for the etch rate corresponds well with the onset of enhanced adsorption ($p_e \approx 0.6\ p_s$) in the adsorption experiments.

The observed kinetics support the idea that in the gas phase regime, H_2O catalyzed adsorption of HF is the etch rate determining step. Since the etch rate is in first order determined by the reactant surface concentration, an increase of adsorbed HF will result in a higher etch rate. At low surface coverages, an increase of p_{H_2O} leads to a proportionally higher concentration of adsorbed water and of HF if adsorbed water acts as an adsorption site for HF. An increase in p_{HF} also leads to a higher reactant surface concentration. Therefore, the HF surface concentration and, thus, the etch rate, is proportional to both p_{H_2O} and p_{HF}.

As a next step, the etch behaviour on the TEOS and thin chemical oxides has been examined. For this, the etch parameters were fixed ($p_{HF} > p_{H_2O}$ and $p < 0.4\ p_s$) while the etch time was varied. Figure 4 shows the amount of oxide etched as a function of etch time for both thermal and TEOS oxides. Also indicated in this figure is the minimum etch time required to completely remove the chemical oxide. From the data several conclusions can be drawn. Firstly, although the etch rates for TEOS and thermal oxide differ significantly (4.5 nm/min vs. 0.2 nm/min), they are constant, indicating that the process is stabilized already in its initial stage. Secondly, the etch inhibition time for both types of oxide is approximately 60-90 seconds. Since the etch inhibition strongly relates to surface conditions, the inhibition time might vary from run to run. Repeat experiments show a variation of the inhibition time from 5-100 seconds. Finally, complete native oxide removal to a level where the silicon wafer shows immediate and complete hydrophobicity, can be achieved while only 3 nm of thermal oxide is etched.

Based on the experimental data, it is concluded that the HF vapour etch process in the gas phase regime can be used successfully for the removal of native oxides if thermal oxide is the only other oxide exposed to the etch. The process guarantees complete removal of the native oxide whereas only 3-4 nm thermal oxide is removed. The low etch rates and relatively short inhibition times make that the etch uniformity and reproducibility can be controlled to within ± 10%. In spite of the low etch rate, throughput, an important economical factor, is, given the batch processing capability, up to industrial standards (> 50 wafers/hour).

On the other hand, if other oxides such as TEOS oxides are exposed, native oxide etching in the gas phase regime is less attractive. The higher etch rates associated with TEOS oxide, make that approximately 100-125 nm TEOS oxide is etched in the time required for complete native oxide removal. In many practical applications, this exceeds the acceptable limits. For those applications where etch selectivity is critical, the etch process in the enhanced adsorption regime is an attractive alternative as will be discussed in the next section.

<u>enhanced adsorption regime etching</u>

As demonstrated in the previous section, gas phase etching may be used for native oxide removal but is not applicable if low etch selectivities are required. A different etch regime, i.e. enhanced adsorption or condensation regime, can be selected by increasing the pressure to above 0.5-0.6 p_s. In figure 5, the effect of the total pressure on the etch process is shown. For a fixed etch time and three different HF/H_2O flow ratios (indicated as a,b, and c with c one order of magnitude higher as a), the amount of thermal oxide

removal is plotted as a function of the total pressure, expressed as p/p_s. A clear, very sharp transition from negligible etching (< 1 nm/min) to substantial etching (10-100 nm/min) is observed. Since the transition points for the three different flow ratios all fall within the range 0.40-0.55 p_s, it is believed that the increase in etch rate relates to the onset of enhanced adsorption of the vapour mixture. Further prove for this hypothesis is found from other etch experiments at a higher (∂T = 5 °C) temperature: the transition points shift to higher absolute pressures but still correspond to a p/p_s ratio of 0.4-0.5. The fact that the transition point shifts towards lower p/p_s values for increasing HF/H_2O flow ratios, most likely, relates to the way p_s is determined: in figure 5, the value of p_s is taken as the saturation pressure of the binary HF/H_2O mixtures. In reality, however, reaction products such as SiF_4 and H_2SiF_6 are generated. Consequently, the real saturation pressure is that of a ternary $HF/H_2O/SiF_x$ system. If SiF_x addition results in a lowering of the saturation pressure, the observed shift can be explained by an increase of the SiF_x concentration at higher etch rates.

Figure 5 contains additional relevant information. Although the etch rate increases at higher HF/H_2O flow ratios, no such effect is observed when increasing the pressure from 0.5 to 0.9 p_s at a fixed HF/H_2O ratio. This suggests that the absolute partial pressures of HF and H_2O have little effect on the etch rate. This finding is consistent with the multiple layer adsorption hypothesis. If etching takes place while many monolayers are adsorbed, the composition of the adsorbed layer approaches that of a condensed film and thus relates to the composition of the vapour mixture according to the phase diagram. Therefore, although the pressure might affect the thickness of the adsorbed layer, it has little effect on its composition.

The TEOS/thermal oxide etch selectivity, evaluated as a function of p/p_s, is shown in figures 6 and 7. As can be seen in figure 6, the pressures at which enhanced etching starts to occur differ for TEOS and thermal oxides. This difference accounts for the high etch selectivity at the low pressure end in figure 7. For pressures in the range 0.6-0.9 p_s the etch selectivity is approximately 2.5, a value which is similar to that obtained in a diluted HF liquid etch. However, at a pressure equal to the saturation pressure, the etch selectivity is reduced to 1.2. To check whether the differences in etch selectivity are caused by different inhibition times or different etch rates, additional experiments have been carried out at three pressures (0.48 p_s, 0.75 p_s and 1.0 p_s) with the etch time as the varied parameter. From the results, presented in figure 8 and table 2, it can be concluded that the etch selectivity is primarily related to a difference in etch rate for both oxides. The fact that the etch selectivity is close to unity at a pressure equal to the saturation pressure suggests that in the condensation regime the etch rate is no longer adsorption controlled but limited by the diffusion of either HF or SiF_x in the liquid film built up at the oxide surface. That, indeed, a liquid film condenses at a pressure equal to the saturation pressure is experimentally supported by the observed increase in the time required to evacuate the reactor to base pressure after the etch process.

Finally, complete etching of chemical oxide in the enhanced adsorption and condensation regime is, given the high etch rates, almost instantaneously. Immediate and perfect hydrophobicity of the etched silicon wafers is achieved for etch times that correspond with a removal of less than 3 nm thermal oxide, or, alternatively, 8 nm TEOS oxide.

It is concluded that the HF vapour process in the enhanced adsorption regime is perfectly suited for the removal of native oxide even when other than thermal oxides are exposed to the etch ambient. Although the etch rate is relatively high (≥ 10 nm/min), the

oxide removal can be well controlled since the process is highly reproducible ($\leq \pm 5\%$). The adapted hardware allows for etch uniformities better than $\pm$ 10% and given the batch approach, the throughput is no limiting factor.

APPLICATIONS OF INTEGRATED HF VAPOUR ETCHING

Although the feasibility of the HF vapour etch process is demonstrated, its implementation in production environments can only be justified if real improvements, either in terms of device characteristics or production costs (yield) are demonstrated. In the following, some of the successful applications of integrated HF vapour etching are briefly reviewed.

One of the applications tested is that of poly silicon contacts (10). To realize a low contact resistance in sub-micron contact holes consistently, it is vitally important to avoid any interfacial oxide. As depicted in figure 9, the integrated HF vapour etch process is effective for this purpose. As compared to using ex-situ liquid HF, a lower contact resistance with a tighter distribution can be obtained. SIMS analysis shows that for the integrated HF vapour process the amount of interfacial oxide is less than 2E14/cm^2, i.e. less than a monolayer.

Another example of the benefits of integrated HF vapour etching is found in poly emitter applications. In bipolar devices the amount of oxide between the poly-Si and mono-Si emitter area strongly influences the transistor characteristics. By using an in-situ HF vapour etch followed by an intentionally oxide regrowth and LPCVD of polysilicon, the forward gain and emitter resistance can be tuned and, moreover, controlled within tighter limits (11).

Another successful application of the integrated HF vapour process is demonstrated in the fabrication of DRAM devices. Shrinking of the interpoly NO dielectrics is limited by the minimum nitride thickness needed to withstand the subsequent reoxidation. In case of conventional processing, the nitride nucleation is hampered due to the fact that the polysilicon substrate is not entirely free of residual oxide. In the absence of any surface oxide, as is the case with integrated HF vapour processing, the nitride nucleation is instantaneous and very thin, oxidation resistant nitride films can be produced (12). Capacitors prepared using these nitride films, show better electrical characteristics even when thinner nitride films are used (13).

CONCLUSIONS

Silicon oxide etching in an HF-H_2O gas mixture is governed by a subtle balance of sorption mechanisms and surface reactions. Three different etch regimes have been established. In the gasphase regime, the etch process is characterized by limited adsorption, low etch rates and high etch selectivities. In the enhanced adsorption regime, the HF and H_2O are more readily adsorbed onto the oxide which makes the process less sensitive to the exact nature of the oxide. In contrast to the gasphase regime, etch rates are high and etch selectivities low. In the condensation regime etch rates are comparable to those obtained in the enhanced adsorption regime but selectivities are still lower and close

to unity. It is believed that at pressures approaching the condensation pressure the etch rate becomes limited by the transport of either HF or SiF_x in the liquid film built up at the oxide surface.

The benefits of integration of the HF vapour etch process with LPCVD processes in a cluster tool are demonstrated for various critical device applications. Compared to conventional technology, more flexible and better controlled interface engineering is achieved with the integrated HF vapour etch process. The better interface control is reflected in improved electrical characteristics with tighter distributions.

It is concluded that since the process and associated hardware meet the stringent industrial requirements, integrated HF vapour etching can successfully replace liquid HF etching as an oxide removal step in the fabrication of advanced integrated circuits.

ACKNOWLEDGEMENTS

We are grateful to Jack van Putten and Ronald Bast for their assistance in processing and analysis of the wafers. We thank Rudi Wilhelm of ASMJ and Jan Mulder of ASME for their helpful discussions.

REFERENCES

1. J.S. Judge, J. Electrochem. Soc., Vol. 118, 1772-1775 (1971).
2. N. Miki, H. Kikuyama, I. Kawanabe, M. Miyashita and T. Ohmi, IEEE Trans. El. Dev., Vol. 37, No 1, 107-115 (1990).
3. R. McIntosh, T-S. Kuan and E. Defresart, J. Electronic Mat., Vol. 21 No. 1, 57-60 (1992).
4. P.J. Holmes and J.E. Snell, Microelectron. Reliab., Vol. 5, 337-341 (1966).
5. M. Wong, M.M. Moslehi and D.W. reed, J. Electrochem. Soc., Vol. 138, No. 6, 1799-1802 (1991).
6. C.R. Helms and B.E. Deal, J. Vac. Sci. Technol. A, Vol. 10, No. 4, 806-811 (1992).
7. S. Brunauer, L.S. Deming, W.E. Deming and E. Teller, J. Am. Chem. Soc., Vol 62, 1723-1732 (1940)
8. A. Philipossian, private communication.
9. P.A. Munter, O.T. Aepli and R.A. Kossatz, Ind. Eng. Chem., Vol. 41, No. 7, 1504-1508 (1949).
10. F. Walczyk, C. Lage, V. Kanshik and M. Blackwell, in Proceedings of the Bipolar Circuits and Technology Meeting, Minneapolis, 84 (1992).
11. R. Reuss, presented at the Bipolar Circuits and Technology Meeting, Minneapolis, (1993).
12. L.F.Tz. Kwakman, E.J. Lindow, E.H.A. Granneman, F. Martin, J.C. Veler and J.P. Joly, Appl. Surf. Sci., Vol 70/71, 629-633 (1993).
13. M. Yoshimaru, N. Inoue, M. Itoh, H. Kurogi, H. Tamura, N. Hirashita, F. Ichikawa and M. Ino, Proceedings of the International Electron Device Meeting, San Fransisco, 271 (1992).

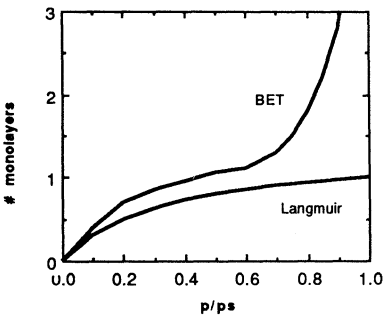


Figure 1. Langmuir and BET adsorption as a function of the relative pressure p/p_s.

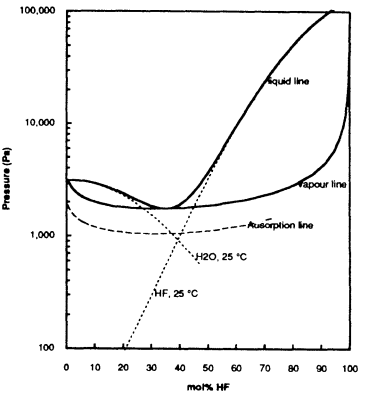


Figure 2. HF/H_2O phase diagram at 25 °C.The curves are calculated based on data of Munter et al.

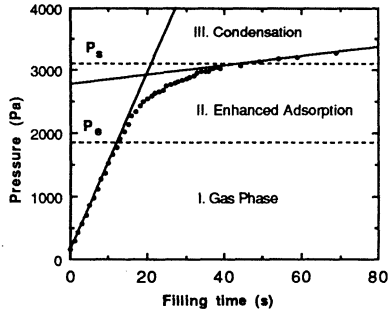


Figure 3. Pressure versus filling time for the isolated reactor. The flow of the 10 % mol $HF-H_2O$ vapour mixture is constant. The different pressure regimes are indicated by dotted lines.

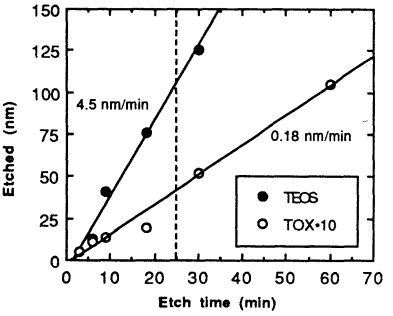


Figure 4. Gas phase etching of different oxides. The amount of etched thermal oxide (TOX) and TEOS oxide as a function of the etch time. The dotted line indicates the minimum etch time required to render a silicon wafer hydrophobic.

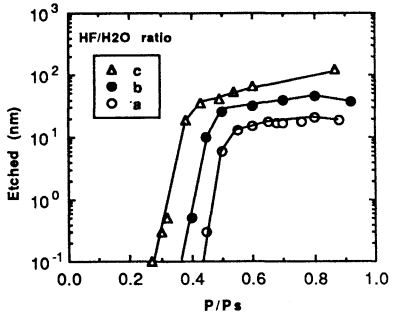


Figure 5. Etched thickness of thermal oxide as a function of the relative pressure (p/p_S) for various HF/H_2O vapour pressures.

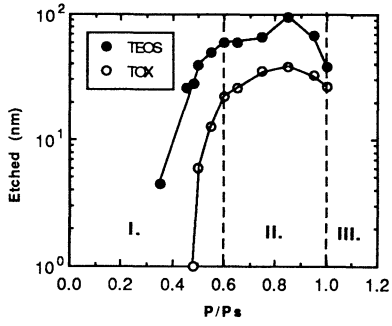


Figure 6. Etched thickness of thermal oxide and TEOS oxide as a function of the relative pressure (p/p_S). The dotted lines indicate the different etch regimes: I. Gas phase, II. Enhanced adsorption and III. Condensation.

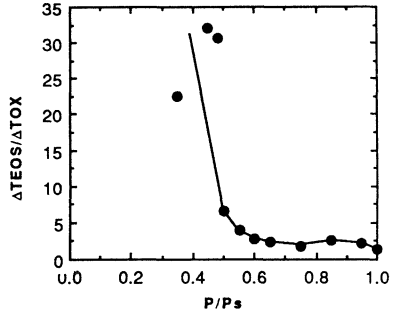


Figure 7. Etch selectivity as a function of the relative pressure. The selectivity is expressed as the ratio of etched thicknesses, Δ TEOS/Δ TOX.

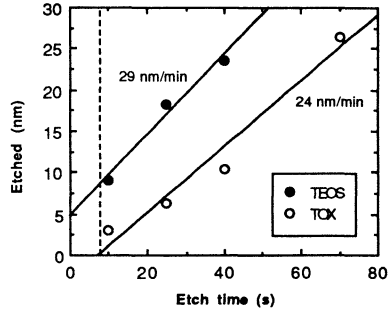


Figure 8. Etched thickness of TEOS and thermal oxide versus etch time at the saturation pressure ($p = p_s$). The dotted line indicates the minimum etch time required to render a silicon wafer hydrophobic.

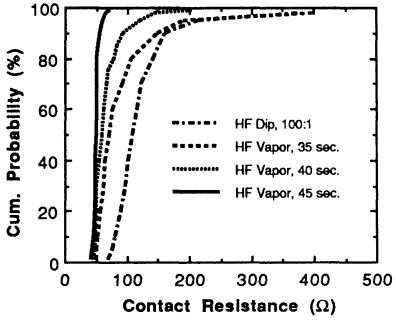


Figure 9. The contact resistance distribution between mono-Si and poly-Si for 1.3 μm^2 contacts. HF dip indicates a conventional process including a liquid oxide removal step. The etch times are varied from 35 to 45 seconds.

HF in H2O (mol%)	Pe (Pa)	Ps (Pa)	Pe/Ps
0	2000	3300	0.61
10	1850	3050	0.61
17	1700	3080	0.55
22	1900	3100	0.61
31	1300	2020	0.64
35	1300	1930	0.67
38	1000	1900	0.53

Table 1. Adsorption and saturation pressures for various HF-H_2O vapour mixtures.

Etch regime	Etch rate (nm/min)		Selectivity TEOS/TOX	Inhibition TOX (s)	Equivalent TOX etched for FSI-b oxide removal (nm)
	TOX	TEOS			
I. Gas Phase (P<0.5*Ps)					
H2O/HF <1	0.2	4.5	25	5-60	<3.0
H2O/HF >1 (P=0.48*Ps)	0.7	30.0	45	<15	>20
II. Enhanced Adsorption (0.60 Ps<P<0.95*Ps)	22-28	51 - 64	2.3 - 2.7	<5	<3.0
III. Condensation (P=Ps)	23.9	29.2	1.2	<5	<3.0

Table 2. Summary of the etch results

CHEMICAL VAPOR CLEANING TECHNOLOGIES FOR DRY PROCESSING IN SEMICONDUCTOR MANUFACTURING

S.E. Beck, D.A. Bohling, B.S. Felker, M.A. George, A.G. Gilicinski, J.C. Ivankovits, J.G. Langan, S.W. Rynders; Air Products and Chemicals, Inc., Allentown, PA.
J.A.T. Norman, D.A. Roberts, G. Voloshin; Schumacher Co., Carlsbad, CA.
D.M. Hess; Lehigh University, Bethlehem, PA,
A. Lane; Texas Instruments, Dallas, TX

ABSTRACT

Chemical Vapor Cleaning is a proposed methodology for removing metallic contamination from semiconductor surfaces. In this process a gas phase coordinating or chelating ligand reacts with a surface metal species to form a volatile coordination compound. This metal coordination compound then desorbs from the surface at relatively low temperatures and is removed from the process chamber under vacuum or gas flow. This paper will review the processing issues surrounding Chemical Vapor Cleaning and describe current results and trends for this technology area.

INTRODUCTION

In the manufacture of state-of-the-art semiconductor device structures, absolutely clean wafers must be utilized in order to obtain high yields and defect free performance[1]. Contamination of wafers can arise from many sources including photoresists, process chemical contaminants, etching residues, and even from systems designed to clean wafers. This contamination is generally removed using various cleaning procedures, historically relying upon a series of acidic, alkaline, and de-ionized (DI) water rinse baths. These processes are historically referred to as the *RCA method* or SC1 and SC2 (for *Standard Clean 1* and *Standard Clean 2*). Wet cleaning of substrates is an important process which removes detritus, etches unwanted substrate material, and otherwise prepares a given surface for further electronics processing. Gas phase processes, or dry cleans, are not necessarily required on purely technical grounds, as wet cleaning technology has been extended each time geometries or design rules have become more challenging. Table 1 shows the design rule trends which will affect shifts towards dry or gas phase cleaning technologies. Table 2 illustrates the analytical detection limits and cleaning efficiencies for state-of-the-art cleaning processes. Of particular interest is the large, increasing disparity between the minimum definition of critical metal impurity contamination and the practical contamination levels achieved with existing cleans. In addition, a similar disparity exists between the practical analytical detection limits and targeted contamination levels for future technology generations. These disparities indicate a need for improvements in both analytical methods and cleaning technologies.

There are a number of compelling reasons why there will be a shift from wet processes to gas phase cleaning processes. These reasons include:

- Difficulties in purifying wet chemical systems to the next generation requirements which are estimated to include soluble molar metal contamination ranging from 10^{-15}M to near 10^{-34}M, or in other notation 10^{-6} to near 10^{-26} ppbv. These metal concentration levels will be extremely difficult to attain except by point of use generation of the wet chemicals from *gas phase* reagents.

- Environmental concerns regarding disposal of large volumes of slightly contaminated aqueous acid and base solutions. This is currently being overcome by expanded use of acid reprocessors and IPA dryers. However, at the trace metal concentrations described previously, reprocessor distillation columns are likely too inefficient to reach extremely low metal contamination levels.

- Incompatibility of the wet clean processes with most cluster tool environments. With semiconductor manufacturing trends towards single wafer processing in a clustered tool environment there is a growing need for cleaning processes compatible with integrated tool processing. A secondary problem associated with wet cleans is that of handling wafers during the cleans in the relatively dirty environment outside the cluster.

- Minimum gate oxide feature sizes are approaching 50Å in thickness. Most wet processes also remove a substantial amount of substrate material which increases the efficiency of the clean but may destroy sensitive or very small features on the wafer. This could lead to problems with clean control and reliability, and ultimately to problems in device yield.

Dry processes developed in the future will not *replace* standard wet cleans, but rather will be used in processes where wet cleans are impractical or inadequate, such as in cluster tool processing or gate oxide pre-cleans. Wet cleans will still dominantly be used for initial preparation of wafers prior to processing. Dry cleans will then be used to augment the wet cleans, removing any residual metal, water, or other material, and will be used for subsequent cleans within the cluster.

Dry cleaning potentially solves the problems outlined above in the following ways:

- Gas phase processing chemicals are much easier to purify relative to metallic impurities than aqueous or wet systems, due mainly to the involatility of most metal salts. Of course, this will require that any developed gas phase processes also address the issues of materials compatibility with the gas phase chemical delivery systems.

- Gas phase processes generally do not require large volumes of chemical reagents and are inherently more environmentally "friendly" than parallel wet processes. Gas phase processing may require chemical abatement systems to avoid environmental releases of products or process gases, but in most cases semiconductor fabs already have sufficient scrubber systems to handle effluent generated during chemical vapor cleaning.

- Gas phase cleaning processes will allow the wafer to go through multiple processing steps, being cleaned between each process, without being exposed to the atmosphere or clean room environment.

- Although perhaps not universally the case for gas phase cleaning, most dry clean processes do not significantly roughen the wafer surface during a metal clean. Therefore, gas phase cleans will potentially allow strict control of film and surface feature thicknesses without the concern of dynamic feature changes during ancillary cleaning processes.

These are the some of the apparent advantages of a dry/gas phase cleaning process today.

Because the standard *RCA* cleans are so effective and remove a large variety of contaminants, shifting to an all dry process for some manufacturing applications is ccomplex. The various contaminants which need to be addressed by any cleaning process or sequence include thick and thin oxides, aluminum and transition metals (Cu, Ni, Cr, Fe, etc.), group I and II mobile ions (Na, Ca, K, etc.), particles, and hydrocarbons or adventitious carbon. Employing an all-dry process will require a change in manufacturing mindset as specific dry cleaning steps will likely be necessary for specific contaminants. Semiconductor manufacturers will also need to better understand the nature and concentrations of contaminants which should be removed prior to employing a cleaning protocol. The reasons for this are simply that some dry processes will be highly effective for a given contamination condition and inappropriate or ineffective for others. A specific example is the removal of thick oxide versus thin native oxide. Whereas an anhydrous HF process might be highly effective for the former[2], a downstream hydrogen plasma clean might be the more appropriate for thin oxide[3]. In addition to cleaning effectiveness considerations, understanding the nature and concentration of specific contaminants will allow the semiconductor manufacturer to choose certain cleaning procedures while omitting others, giving a much higher level of control to the manufacturing process and potentially higher wafer throughput.

Of the various dry or gas phase cleaning methodologies available, research in dry cleaning has mainly focused upon the use of anhydrous HF or UV/downstream plasma enhanced halogen cleaning (vapor phase cleaning). Most of these rely on the surface conversion of metal contaminants to their respective metal halides which generally require moderate to high temperatures for removal. Mediating this reaction with alcohols has led to increased cleaning control for some researchers[2].

This paper will review the processing issues surrounding Chemical Vapor Cleaning (CVC), or the formation and removal of volatile metal complexes from surfaces, and describe current results and trends for this technology area.

DISCUSSION

UV Halogen Processes

Numerous groups have examined metal removal using either downstream plasma excitation or UV excitation to form volatile metal/halogen intermediates[4,5,6] . This chemistry relies upon the formation of the pure metal halides. As has been described by Ruzyllo, these metal halides are at best only moderately volatile[7]. Despite this issue of volatility, the UV/halogen process has been used quite effectively for the removal of metal contaminants although some collateral surface removal is almost always seen during the process.

One novel way to potentially expand the utility of the UV halogen process would be to combine it with some of the concepts utilized for CVC. It is possible to use mixed halogen-ligand systems to form much more volatile metal complexes, as compared to the totally halogenated systems. This concept was first described for cleaning by Gluck who used nitric oxide in combination with halogens to form mixed metal nitrosyl/halide complexes[8]. Although these complexes have limited volatility they do show the utility of adding a mixture of complexing agents to the gas phase cleaning matrix. For example, gold chloride has been used as a Chemical Vapor Deposition (CVD) reagent by volatilizing it in an ambient of carbon monoxide (Reaction 1)[9]. Although the product is only metastable (can not be synthetically isolated) it does have a lifetime long enough to allow transport from the reagent reservoir to the CVD chamber.

$$AuCl_{(s)} + CO \longrightarrow \text{“Cl-Au-CO}_{(vap)}\text{”} \qquad [1]$$

It is conceivable that addition of CO or other d-π backbonding ligands to the cleaning ambient may also greatly increase the effectiveness of the UV/halogen cleans. Volatile copper halogen-ligand compounds are also well known. Copper(I) chloride reacts similarly as the gold compound to form a somewhat volatile product (Reaction 2)[10].

$$Cu + {}^1/_2Cl_2 \longrightarrow CuCl_{(s)} + CO \longrightarrow OC{-}Cu\begin{matrix}\diagup Cl \diagdown \\ \diagdown Cl \diagup\end{matrix}Cu{-}CO \qquad [2]$$

There has also been a great deal of work examining the formation of volatile metal complexes, with particular emphasis on copper, for plasma etching applications. As with the case shown in Reaction 2, copper(I) chloride can be removed from surfaces by using trialkyl phosphines (excellent d-π backbonding ligands) during the plasma exposure[11]. CuCl reacts with two equivalents of triethyl phosphine to form the volatile product according to Reaction 3. Similar reactivity would be expected in UV photoexcitation systems utilized for cleaning. Additionally, this chemistry would not be limited to copper but would be applicable to a number of transition metal systems.

$$CuCl_{(s)} + 2P(CH_2CH_3)_3 \longrightarrow ClCu[P(CH_2CH_3)_3]_{2(vap)} \qquad [3]$$

Recently, alcohols have been used to better control the reaction between HF and silicon oxide surfaces[11]. Alcohols may also be used to play a role in metal removal when used in a UV/halogen process to form the mixed halo-alkoxy metal compounds or simply homoleptic metal alkoxides. Compounds of this type have been used for a number of years for the CVD of metal oxides[12]. Examples of volatile metal alkoxides include titanium and zirconium iso-propoxide or the more recently reported tertiary butoxides of aluminum, molybdenum, copper, and tungsten[13]. Aluminum t-butoxide dimer (shown in Figure 1) has a 200°C vapor pressure of 1 atm.

CVC With Chelating Ligands

Our work has focused upon the use of chelating or coordinating ligands which form volatile metal coordination compounds for the removal of metal contamination from surfaces. As previously described by workers at Air Products, some transition metals can be removed using Chemical Vapor Cleaning, or CVC. This methodology employs the heterogeneous reaction of coordinating ligand systems with specific surface metal contaminants. For example, iron and copper can be removed from oxide surfaces using either 1,1,1,5,5,5-hexafluoro-2,4-pentanedione (HFAC) or trifluoroacetic acid[14-18]. The limitations of this technique have not yet been determined experimentally, although conceptually there should not be a lower concentration reactive limit as long as the contaminants reside on the surface of the substrate. The strict CVC technique does not result in etching or loss of substrate material. It is thought to be almost infinitely selective over the substrate, a theory borne out using AFM to probe wafer surfaces after a CVC clean[19].

The overall reaction between HFAC and surface metal oxides has also been determined, focusing mainly upon the removal of copper from wafer surfaces[20]. A simplified reaction schematic for the removal of copper(I) oxide is shown in Figure 2. HFAC removes Cu(II) and Cu(I) oxides from surface via a direct or disproportionation reaction, respectively. In a non-oxidizing environment the removal of copper(I) oxide leaves copper metal at the surface; this Cu(0) can easily be re-oxidized in an oxidizing ambient (dry O_2, Cl_2, etc.) to form copper(I) or copper(II) which can then can be removed upon further HFAC exposure. These reactions are described more fully in the recent paper by George[20]. This process is not necessarily limited to iron and copper as many other metal HFAC complexes are known to be highly volatile[21].

Additional work by Pearton and coworkers examined the CVC removal of metal halide RIE residue removal[22]. Plasma etching InGaAs and AlGaAs High Electron Mobility Transistor (HEMT) structures using BCl_3/SF_6 plasma leaves AlF_x at the etch-stop layer. The etch-stop residue needs to be removed prior to metallization to assure good ohmic contact. In this case, HFAC was shown to remove greater than 70% of the surface metal halides at the contact interface at 250°C according to the idealized reaction shown as Reaction 4 (the structure of the product is shown in Figure 3). Although thermal budgets for this HEMT device can not tolerate the temperatures required for RIE etch residue removal using HFAC, the process does prove feasibility as a dry clean methodology.

$$AlF_{3(s)} + H^{+}HFAC_{(vap)} \longrightarrow Al(HFAC)_{3(vap)} + HF_{(vap)} \qquad [4]$$

Only one gas phase/dry option is currently known for removing mobile ion contamination: chemical vapor cleaning. For example, native oxide surfaces contaminated with sodium ions can be cleaned by first converting the surface sodium to a more reactive state (Reaction 5) in a downstream plasma or using UV excitation and subsequently reacting this activated species with hexamethyldisilazane (HMDS). This reaction results in the formation of volatile sodium hexamethyldisilamide (Reaction 6)[23,24]. The intermediate sodium amide is represented in quotations as it has not been unequivocally identified as the stoichiometric material. Rather, XPS evidence indicates that, although the sodium is bound to nitrogen on the surface, it is not clear whether this is truly sodium amide. Regardless, the sodium intermediate reacts with HMDS to form a volatile sodium complex which is removed from the surface. As with the CVC technique for transition metals, this process is highly selective towards those metals which can form volatile amide coordination compounds. The process does not remove any of the native oxide or substrate, although investigations of surface roughening on a nanometer scale have not yet been completed.

$$Na_2O + H^{\cdot}/NH_3 \longrightarrow \text{“}NaNH_{2(s)}\text{”} + H_2O_{(vap)} \quad [5]$$

$$\text{“}NaNH_{2(s)}\text{”} + HN[Si(CH_3)_3]_{2(vap)} \longrightarrow NaN[Si(CH_3)_3]_{2(vap)} + NH_{3(vap)} \quad [6]$$

XPS evidence of sodium removal is shown in Figures 4 and 5. Figure 4 represents a full spectrum showing all significant XPS and Augér active peaks between 0-1100eV. The principal sodium peaks are at 1073eV and 267eV for the Na(1s) XPS line and Na($KL_{23}L_{23}$) Augér line, respectively. Chlorine at 193eV can be seen in trace quantities prior to cleaning in Figure 4. Figure 5 shows only the sodium (1s) XPS region before and after cleaning. Sodium levels are reduced to near the XPS detection limit (Fig. 4) after the $H^{\cdot}/NH_3$-HMDS treatment.

SUMMARY

Chemical Vapor Cleaning represents a truly dry, highly selective method for the removal of metal contamination from silicon and SiO_2 surfaces. Since CVC chemistries involve only gas phase reactants and products, they potentially represent an enabling technology for clustered manufacturing processes in semiconductor fabrication. An example of this would be in manufacturing thin gate oxides for state-of-the-art MOS devices where gate thicknesses are approaching 50Å. Current fabrication processes require a wet pre-gate clean due to the sensitivity of the device on final gate integrity. Unfortunately, such a fabrication sequence exposes the devices to numerous sources of contamination and damage. Replacement of the critical wet clean with in-situ dry processes would permit full clustering of these contamination sensitive steps and a reduction in contamination/wafer handling defects. Because of the gaseous phase of the reactants and products, the potential for high contaminant selectivity, and the potential for high cleaning efficiency, CVC processes represent a significant step towards the realization of ultra-clean, clustered processing that will be necessary for the fabrication of future generation ULSI devices.

REFERENCES

1. Kern, W., J. Electrochem. Soc., 137 1887 (1990).

2. Izumi, A., Matsuka, T., Takeuchi, T., Yamano, A., *ECS Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, 92-12 260 (1992), Ruzyllo, J., Torek, K., Daffron, C., Grant, R., Novak, R., J. Electrochem. Soc., 140 L64 (1993).

3. Anthony, B., Beaux, L., Hsu, T., Banerjee, S., Tasch, A., J. Vac. Sci. Technol. **B** 7 621 (1989).

4. Frystak, D.C. and Ruzyllo, J., *ECS Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, 92-12 58 (1992).

5. Sugino, R., Okuno, M., Shigeno, M., Sato, Y., Ohsawa, A., Takashi, I., and Okui, Y., *ECS Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, 92-12 72 (1992).

6. Torek, K., Ruzyllo, J., *ECS Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, 92-12 80 (1992).

7. Ruzyllo, J., Overview of Dry Wafer Cleaning Processes, from the *Handbook of Semiconductor Wafer Cleaning Technology*, Werner Kern, ed., pp. 201-232, Noyes Publications, 1993, and references therein.

8. Gluck, R.M., *ECS Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, 92-12 48 (1992).

9. McCormick, F., 3M Company, personal communication.

10. Håkansson, M., and Jagner, S., Inorg. Chem., 29 5241 (1990).

11. Farkas, J., Chi, K.-M., Hampden-Smith, M.J., Kodas, T.T., Dubois, L.H., J. Appl. Phys., 73 1455 (1993), Hampden-Smith, M.J., Kodas, T.T., MRS Bulletin, June 1993, pp. 39-45.

12. See for example, Bradley, D.C., Chem. Rev., 89 1317 (1989), Bradley, D.C., Factor, M.M., J. Appl. Chem. 9 435 (1959).

13. Baxter, D.V., Chisholm, M.H., DiStasi, V.F., Klang, J.A., Chem. Mater., 3 221 (1991), Jeffries, P.M., Dubois, L.H., Girolami, G.S., Chem. Mater. 4 1169 (1992).

14. Roberts, D.A., Bohling, D.A., Ivankovits, J.C., Norman, J.A.T., United States Patent 5,094,701 10 March, 1992.

15. Roberts, D.A., Bohling, D.A., Ivankovits, J.C., United States Patent 5,213,622 25 May 1993.

16. J.C. Ivankovits, D.A. Bohling, D.A. Roberts, A. Lane, *ECS Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, 92-12 105 (1992).

17. Roberts, D.A., Bohling, D.A., Norman, J.A.T., Ivankovits, J.C., United States Patent 5,221,366 22 June 1993.

18. Roberts, D.A., Bohling, D.A., Ivankovits, J.C., United States Patent 5,213,621 25 May 1993.

19. Beck, S.E., Gilicinski, A.G., Felker, B.S., Langan, J.G., George, M.A., Bohling, D.A., Ivankovits, J.C., Roberts, D.A., *this Proceedings.*

20. George, M.A., Hess, D.W., Beck, S.E., Ivankovits, J.C., Bohling, D.A., Felker, B.S., Lane, A.P., *this Proceedings.*

21. Sievers, R.E., Sadlowski, J.E., Science 201 217 (1978).

22. Pearton, S.J., Ren, F., Katz, A., Chakrabarti, U.K., Lane, E., Hobson, W.S., Kopf, R.F., Abernathy, C.R., Wu, C.S., Bohling, D.A., Ivankovits, J.C., J.Vac. Sci. Technol. **B** 11 546 (1993).

23. Bohling, D.A., George, M.A., Allowed United States Patent Application.

24. Bohling, D.A., Felker, B.S., George, M.A., from *Materials Research Society Symposium Proceedings, Chemical Perspectives of Microelectronic Materials III*, 282 517 (1993).

Table 1: ULTRA CLEAN TECHNOLOGIES ROADMAP†

Device Technology*	1992	1995	1998
Minimum Feature Size	0.35	0.25	0.18
Gate Oxide Thickness	90Å	65Å	40Å
Comparable DRAM (Mbit)	64	256	1024
Single Wafer Processing (%)	70	85	95
Liquid/Gas Phase Processing(%)	25/75	15/85	10/90
Minimum Killing Defect (μm)	0.04-0.1	0.002-0.08	0.001-0.05
Metal Contamination (atoms-cm^{-2})	$\leq 10^{10}$	10^{9}	10^{8}
Metal Ions (atoms-cm^{-2})	10^{9}	10^{8}	TBD
Carbon/Organics (atoms C-cm^{-2})	10^{15}	10^{13}	10^{12}
Mobile Ions (atoms-cm^{-2})	$\leq 10^{10}$	$\leq 10^{10}$	$\leq 10^{10}$
Microroughness (Å)	≤5	≤3	≤2

* First volume semiconductor production and dependent technologies.

† From SIA Roadmap

Table 2: Cleaning Technologies State-Of-The-Art (atoms-cm^{-2})

Impurity	Current Analytical SOA	Current Wet Clean Analytical SOA[1]	Current Dry Clean Analytical SOA[1]
Fe	10^{8} (SPV)	$2X10^{10}$ (VPD)	$\approx 2x10^{13}$(RBS)
Cu	$\geq 10^{10}$ (TXRF)	$\geq 10^{10}$(TXRF)	$\approx 2x10^{13}$(RBS)
Al	$\geq 10^{10}$ (VPD)	$\geq 10^{12}$ (AES)	$5x10^{13}$ (XPS)
Ni	$\geq 10^{10}$ (TXRF)	$\geq 10^{12}$ (TXRF)	$\geq 10^{14}$ (RBS)
Cr	10^{8} (VPD-ICPMS)	$\geq 10^{10}$ (TXRF)	$\geq 10^{14}$ (RBS)
Na	10^{10} - 10^{11} (CV)	10^{10} - 10^{11} (CV)	$\leq 10^{14}$ (XPS)
Metal	10^{8}-10^{10} (ICP-MS)	10^{10} - 10^{11}(VPD)	$\geq 10^{14}$ (RBS)
Mobile Ions	$\leq 10^{11}$ (CV)	$<10^{11}$ (CV)	*not determined*

[1] Best published analytical coupled to cleaning.

Figure 1. Schematic of aluminum *tert*-butoxide.

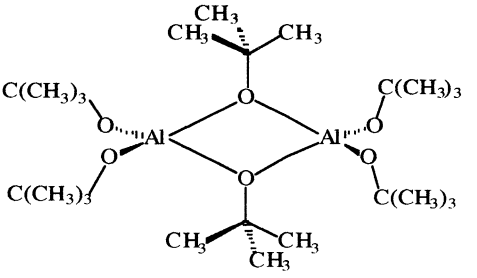


Figure2. Reaction mechanism for CVC of Cu(I) Oxide.

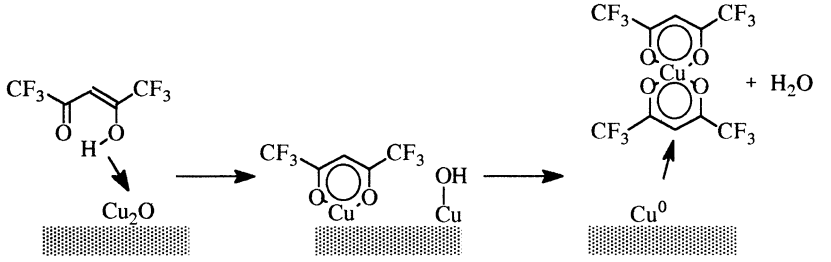


Figure 3. Schematic structure of Al(HFAC)$_3$.

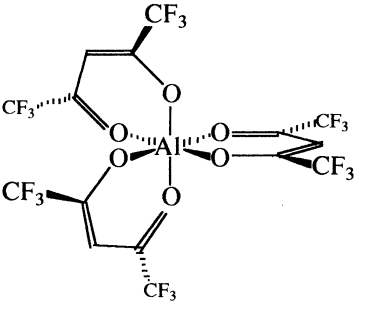


Figure 4. XPS survey spectrum from 0-1100 eV showing a silicon surface contaminated with NaOH before CVC cleaning (above) and after $H^{\cdot}/NH_3$-HMDS CVC cleaning (below).

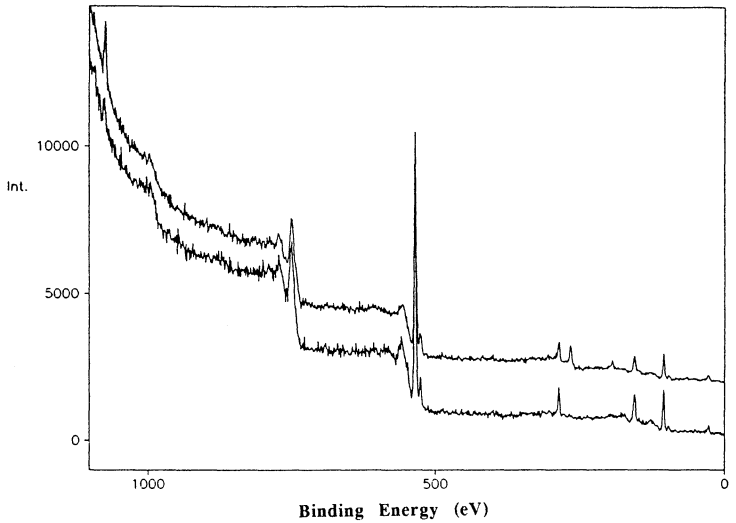
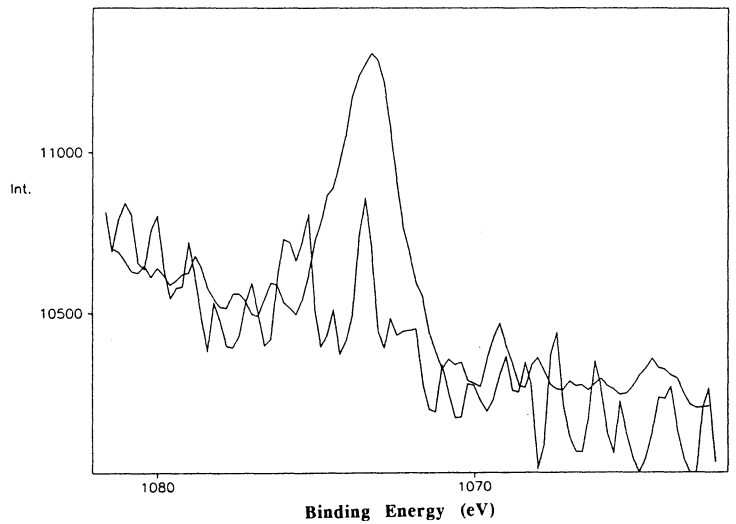


Figure 5. XPS spectrum of the Na(1s) region of NaOH doped substrates before and after $H^{\cdot}/NH_3$-HMDS CVC cleaning.



THE EFFECTS ON SURFACES OF SILICON AND SILICON DIOXIDE EXPOSED TO 1,1,1,5,5,5-HEXAFLUORO-2,4-PENTANEDIONE

S.E. Beck, A.G. Gilicinski, B.S. Felker, J.G. Langan,
M.A. George, D.A. Bohling, J.C. Ivankovits, and D.A. Roberts*
Air Products and Chemicals, Inc., Allentown, PA 18195
*Schumacher Co., Carlsbad, CA 92009

ABSTRACT

This study explores the effects of chemical vapor cleaning (CVC) with 1,1,1,5,5,5-Hexafluoro-2,4-Pentanedione (hfac) on surfaces of Si and SiO_2. These surfaces are not significantly roughened due to short exposures to hfac. Trace amounts of fluorine were found on the exposed surfaces after exposure to the unpurified hfac. These fluorinated species may not be from the hfac ligand but may be from impurities within the reagent used in these experiments. The major volatile contaminant observed in the hfac is ethyl trifluoroacetate. These results underscore the need for high purity reagents when performing any type of clean.

INTRODUCTION

Recently chemical vapor cleaning (CVC) with 1,1,1,5,5,5-hexafluoro-2,4-pentanedione (hfac) was suggested as a method to remove trace levels of transition metals [1]. For any type of vapor phase cleaning to become a viable technology in the production of integrated circuits it must meet certain criteria. These criteria include the ability to remove contaminants to surface concentrations comparable to or better than wet cleans; the process must occur at low temperatures and at high throughput, the semiconductor surface must not be roughened, nor should a residue remain that would be deleterious to device performance and/or reliability. CVC with hfac has been shown to remove copper, iron, chromium, and nickel [1], and with some process optimization may therefore meet the first criteria. Surface metals removal has been accomplished at temperatures between 140°C and 300°C [1,2], thus meeting the second criteria. Fast removal rates of copper films suggest that high throughput can be attained [2]. The purpose of this work is to examine the last two criteria; surface roughening and possible residue from the CVC process. It is now well known that the standard wet cleans (predominantly SC1) can roughen the silicon surface and that this increased surface microroughness can lead to severe degradation of MOS devices [3-5]. Thus for the CVC process to be a successful candidate as a replacement for standard wet cleans it must produce less surface roughening than SC1 or ideally none at all.

EXPERIMENTAL

The wafers used in this experiment were p-type <100> silicon. For the silicon dioxide portion of this study an 800 Å oxide layer was grown in a dry oxygen ambient for 30 minutes at 1100°C followed by a 30 minute anneal in nitrogen at 1100°C. These wafers were then cut into 15mm x 15mm squares. Hfac exposures were performed at surface temperatures of 140°C, 165°C, 200°C. These temperatures were chosen to correspond to those for copper metal deposition from $Cu(hfac)_2$; at 140°C adsorption takes place, 165°C the molecule decomposes on the surface, and 200°C desorption of the hfac ligand occurs [6].

The samples were mounted on a 2.5 cm diameter nickel sample holder that is capable of controllably heating the sample from room temperature to 300°C. Both the sample and sample holder were placed on a magnetically coupled transfer arm in a sample introduction chamber which was then evacuated to a pressure of $< 10^{-5}$ torr. The sample was then transferred into the stainless steel CVC chamber and placed on a heating element. A Pyrex tube then was slid over the sample and holder making contact with a viton gasket below the sample, thus encapsulating it. Isolation of the reaction zone from the chamber stainless steel is necessary since hfac is known to react with stainless steel. The samples were heated to the desired temperature under a nitrogen purge. Exposures were initiated by switching the nitrogen flow through the hfac bubbler that was maintained at 0°C in an ice bath. All exposures were similar to those developed for cleaning in our laboratories. They lasted 2 minutes and were conducted at a total pressure of 10 torr, an hfac partial pressure of approximately 2.5 torr, and a nitrogen flow rate of 38 sccm. (A full description of the CVC reactor and some experimental process conditions are given in reference [2].) All samples were transferred *in vacuo* between the CVC reactor and the XPS system.

X-ray Photoelectron Spectroscopy (XPS) and Contact-mode Atomic Force Microscopy (AFM) were done on the silicon dioxide and as-received silicon samples prior to and following hfac exposure. XPS was performed on a Physical Electronics XPS/Augér system with a double pass cylindrical mirror analyzer. The excitation source was a nonmonochromatized Mg Kα source. The analysis spot size was 3mm in diameter at a 54° take-off angle. The base pressure of the system was 2×10^{-10} torr. Curve fitting was done using software supplied by Perkin-Elmer.

Atomic force microscopy (AFM) was done on a Digital Instruments NanoScope III contact-mode AFM. Samples were attached to steel sample pucks with isopropanol-based colloidal graphite. Images were obtained in air using commercial cantilevers and probes. Several probes were used in this work from Digital Instruments and Park Scientific Instruments. The best data were obtained with "oxide sharpened" silicon nitride tips from Digital Instruments, with a force constant of 0.12 N/m. Scans were made with a data density of 2.1 nm per point in the lateral scan.

A 12 μm ("D") scanner was used to obtain images at scan sizes of 1μm x 1μm and 2μm x 2μm. The lateral axes were calibrated with a 1μm spaced gold ruling. Height was calibrated with a 180 nm height standard and with a step height calibration device [7]. With these calibration samples, 21 Å high squares (2μm x 2μm) were correctly imaged. The procedure for obtaining data was to make surface contact and measure a force curve. The AFM was set to attractive mode imaging by ensuring that the applied force was in the attractive regime. "Scope" mode was used to optimize scan rate and feedback gains. A series of 1μm images was then obtained. This was followed by a 2μm scan to determine whether damage was induced during the 1μm scans. Damage was checked for by visual inspection of the 2μm images, as well as by checking surface roughness in 0.5μm boxes around the 2μm image. From this determination, there was no significant difference in surface roughness in the initially scanned 1μm square versus the surrounding surface. After obtaining images, the 1μm scans were plane-fitted to remove the effect of sample tilt. One pass of a lowpass filter was run to remove high frequency electronic noise from the images before roughness calculations. Roughness measurements were made on the AFM images using version 2.53 of the Digital Instruments NanoScope software. RMS and R_a values were obtained on entire 1μm images, and ± standard deviation values are reported for the number of images that were used in the calculations.

Damage to the silicon or silicon oxide surface was often found when the applied force was over 30 nanoNewtons. Maintaining low forces was critical to obtaining artifact-free images for roughness analysis. As an additional check, field-emission SEM images of the AFM probe were obtained before and after the experiment to check on macroscopic damage to the probe during the analysis.

A continuing effort is aimed at understanding the best methodology for quantitatively characterizing surface roughness in a way that is meaningful for understanding resulting device performance. RMS and R_a are borrowed from stylus profilometry at larger scales, yet the "wavelength" of analysis will determine the scale at which roughness is measured [8]. Fractal analysis methods have been proposed to deal with this, and more recently, power spectral density calculations have been proposed [9]. We are currently evaluating these methods to understand the best manner in which to interpret the AFM results.

RESULTS AND DISCUSSION

Silicon Exposed to Hfac

As-received silicon was examined by AFM and XPS before and after hfac exposure. Carbon concentrations on most samples before treatment generally ranged from 10 to 20 at.%. This is attributed to both the isopropanol-based colloidal graphite used for sample attachment to the steel pucks before AFM measurements and to adventitious carbon from environmental exposure. Of interest is that in cases where there is gross carbon con-

tamination, exposure of the samples to hfac reduces the overall carbon content on the silicon surface by more than twofold. Because these are qualitative results due to the process environment, specific conclusions can not be made regarding whether hfac either adds or removes carbon from native oxide. However, carbon levels after all exposures was less than 13 at. %.

After hfac exposure all samples were found to have silicon, oxygen, carbon, and small amounts of fluorine on the surface. From the ratio of the metallic silicon to silicon oxide peaks in the Si(2p) XPS spectra and minimal changes in the surface oxygen concentrations, it was concluded that little or no etching of the native oxide occurred. Small amounts (≤7 at.%) of fluorine were detected on these surfaces. Therefore, we conclude that there is minimal reaction of the fluorinated species in the hfac with the silicon oxide and that this fluorinated species does not lead to significant etching. The carbon (C(1s)) and fluorine (F(1s)) portions of the spectra were similar for all conditions examined in these experiments. No specific evidence of the intact hfac molecule or molecular fragments such as CF_3 were observed from the C(1s) or F(1s) spectra. However, the fluorine portion of the spectra revealed both metallic fluoride (presumably as SiF_x) and organic fluoride. This indicates that some component of the exposure, either the hfac or impurities in the hfac, interacts with the native oxide surface to form small amounts of SiF_x. This reaction is clearly minimal as evidenced by the low fluorine and carbon levels detected.

AFM measurements reveal little or no change in the surface morphology due to hfac exposure under our process conditions. RMS (standard deviation) and R_a (mean roughness) values were obtained for the silicon samples exposed at 165°C and 200°C. Several sets of data were obtained with different probe tips. Comparisons of the effects of the CVC treatments were made between experiments with the same probes. The resulting roughness values are given in Table I. For the 165°C sample AFM was done with the same Digital Instruments tip but using a force of 130 nN. This force was unusual since sample damage was not found at this level. Careful checking of the 2 μm images for the high force pre-CVC experiment showed no significant differences and the data appear to be true reflections of surface topography. A comparison of the silicon surface roughness before and after treatment of the sample treated at 200°C is shown in Figure 1. For the exposure conditions studied, there appeared to be no change in surface microroughness within the error of the measurements.

Silicon Dioxide Exposed to Hfac

Silicon dioxide films (800Å) exposed to hfac were examined by AFM and XPS before and after hfac exposure. In general, overall carbon levels were unaffected by hfac exposures. Small amounts (≤5 at.%) of fluorine were observed on the surfaces after hfac exposure as compared to as received samples. XPS results for the silicon dioxide samples were very similar to those obtained for the as received silicon samples. There was no

evidence of intact adsorption of the hfac molecule on the oxide surface, although there was some evidence of C-O and C-H type bonding probably due to adventitious carbon. The small amounts of fluorine observed were in the form of both organic (CF_x) and metallic fluoride (SiF_x). AFM was done on the samples before and after hfac exposure using the "oxide sharpened" Digital Instruments tip. The RMS, R_a, and force values before treatment were 1.6 ± 0.1 Å, 1.3 ± 0.1 Å, and 20 nN respectively. These values were again determined after hfac exposure and no significant differences were observed as compared to the pre-treatment values; RMS = 1.7 ± 0.1 Å, R_a = 1.3 ± 0.1 Å, at a force of 22 nN. These values indicate that the hfac treatment under the conditions described in this paper did not significantly affect the surface roughness of silicon dioxide.

Contaminants in Hfac

Contaminants in cleaning agents can be deposited on the wafer surface being cleaned, as has been shown for wet chemical cleans [10]. In order to better ascertain the sources of fluorine surface contamination the hfac was analyzed for impurities using gas chromatography before and after fractional distillation. Atomic contaminants found by inductively coupled plasma-mass spectrometry (ICP-MS) in the sample before purification were aluminum, calcium, chromium, copper, iron, magnesium, manganese, nickel, potassium, sodium, strontium, zinc, and zirconium. All of these were found in concentrations of 1 to 200 ppb. Most of the atomic contaminants were found at levels below 1 ppb after purification. Those above the 1 ppb level include aluminum (5.1 ppb), calcium (3.0 ppb), and iron (1.6 ppb). The major volatile organic contaminant found in the hfac by gas chromatography before and after distillation was ethyl trifluoroacetate which has a vapor pressure very similar to hfac itself. Although surface reactivity differences between hfac and ethyl trifluoroacetate have not yet been determined, the fluorine observed on the surfaces after hfac treatment may be due to the ethyl trifluoroacetate. Further experiments are currently underway to better determine the relevant chemical mechanisms causing the observed surface fluorination.

SUMMARY

We have also demonstrated that hfac treatments typically used for Chemical Vapor Cleaning of trace metal contaminants can be used successfully without significantly roughening the surfaces of silicon and silicon dioxide. However, exposure to unpurified hfac at elevated temperatures has been found to deposit small amounts of fluorine on the treated surfaces. This fluorine may not be from the hfac ligand itself, but may be from impurities within the liquid; ethyl trifluoroacetate was found to be the major contaminant in the hfac. It is our belief that cleaning reagent impurities will negatively affect the performance of current and future dry cleaning processes. Thus, purification of hfac is being pursued to better isolate variables in this cleaning process and show further viability for the CVC cleaning methodology.

ACKNOWLEDGMENTS

The authors would like to thank Gene Karwacki, Steve Rynders, Dave Begany, Jim Stets, and Rebecca Rynders, all of Air Products and Chemicals, Inc., for many insightful discussions related to this work.

REFERENCES

1. J.C. Ivankovits, D.A. Bohling, A. Lane and D.A. Roberts, in *Cleaning Technology in Semiconductor Device Manufacturing*, J. Ruzyllo and R.E. Novak, Editors, PV 92-12, p. 105, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1992).

2. M.A. George, D.W. Hess, S.E. Beck, J.C. Ivankovits, D.A. Bohling, B.S. Felker, and A.P. Lane, *these proceedings.*

3. M. Meuris, M. Heyns, P. Mertens, S. Verhaverbeke, and A. Philipossian, in *Cleaning Technology in Semiconductor Device Manufacturing*, J. Ruzyllo and R.E. Novak, PV 92-12, p. 144, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1992).

4. S. Pirooz, J.C. Coria-Garcia, and L.W. Shive, in *Cleaning Technology in Semiconductor Device Manufacturing*, J. Ruzyllo and R.E. Novak, PV 92-12, p. 162, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1992).

5. T. Ohmi, M. Miyashita, M. Itano, T. Imaoka, and I. Kawanabe, *IEEE Trans. Electron Dev.*, **39**, 537 (1992).

6. S.L. Cohen, M. Liehr, and S. Kasi, *J. Vac. Sci. Technol. A*, **10**, 863 (1992).

7. T. Ohmi and S. Aoyama, *Appl. Phys. Lett.*, **61**, 2479 (1992). Samples were donated by Dr. Futatsuki from Prof. Ohmi's laboratory in Sendai, Japan.

8. I.J. Malik, S. Pirooz, L.W. Shive, A.J. Davenport, and C.M. Vitus, *J. Electrochem. Soc.*, **140**, L75 (1993).

9. L. Peters, *Semiconductor International*, August 1993, p. 62.

10. D.C. Burkman, D. Deal, D.C. Grant, and C.A. Peterson, in *Handbook of Semiconductor Wafer Cleaning Technology*, W. Kern, Editor, p.130. Noyes Publications, East Windsor, NJ 1993.

TABLE I. AFM results for the as-received silicon exposed to hfac.

	Treatment	RMS (Å)	R_a (Å)	Force (nN)	# Points
165°C Sample					
	Before	0.70 ± 0.05	0.55 ± 0.04	130	4
	After	0.69 ± 0.05	0.55 ± 0.04	22	5
200°C Sample					
	Before	0.83 ± 0.04	0.65 ± 0.02	24	2
	After	0.83 ± 0.04	0.65 ± 0.02	22	4

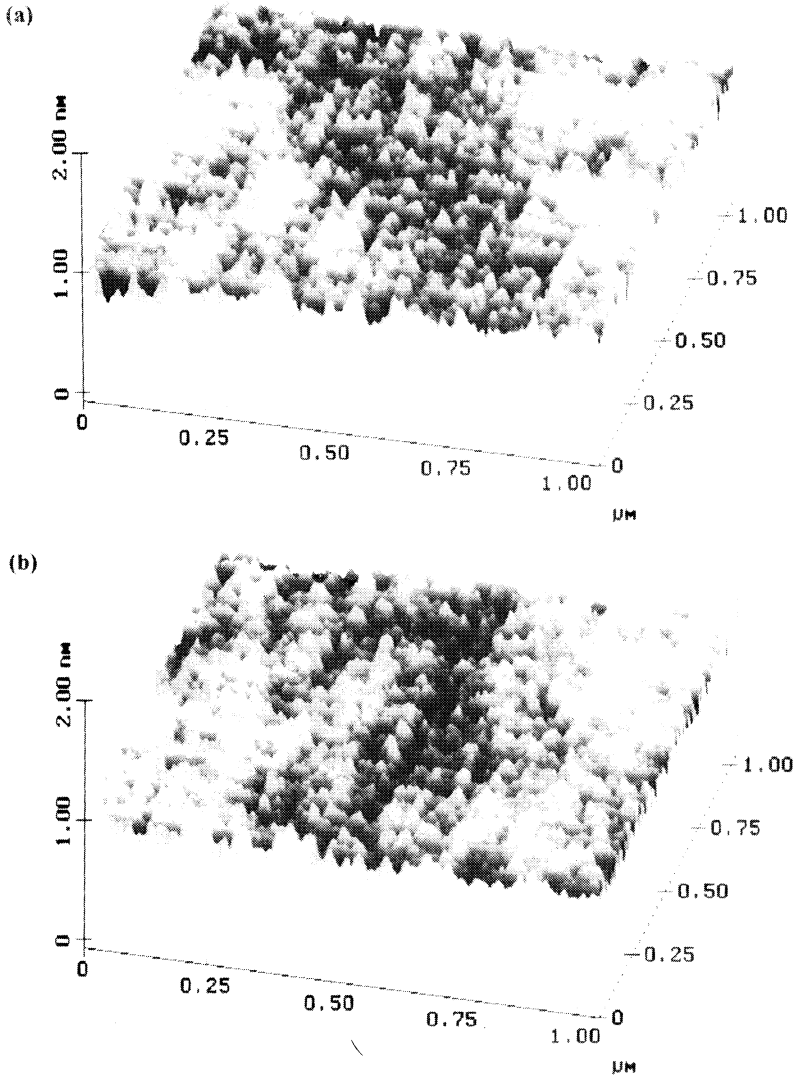


Figure 1 The AFM image of the silicon surface exposed to hfac at 200°C (a) before and (b) after exposure. An "oxide sharpened" Digital Instruments tip was used for these measurements.

REACTION OF 1,1,1,5,5,5-HEXAFLUORO-2,4-PENTANEDIONE (hfac) WITH SURFACES OF CuO,Cu_2O, AND Cu STUDIED BY XPS

M.A. George, D.W. Hess, S.E. Beck*,
J.C. Ivankovits*, D.A. Bohling*,
B.S. Felker*, and A.P. Lane†
Lehigh University, Dept. of Chemical Engineering,
Bethlehem, PA 18015
*Air Products and Chemicals, Inc., Allentown, PA 18195
†Texas Instruments, Dallas, TX 75265

ABSTRACT

The interactions of copper surfaces with 1,1,1,5,5,5-hexafluoro-2,4-pentanedione (hfac) have been investigated. This investigation has provided supporting evidence for proposed reactions with hfac which are thought to be responsible for the vapor phase etching of copper. We have determined that there is a dependence of reaction products on the chemical state of the copper being removed.

INTRODUCTION

Two potential processes under intense investigation for advanced integrated circuit manufacture are copper metallization and vapor phase dry cleaning. While the intent of many researchers working on metallization is to develop selective copper deposition processes this will not necessarily eliminate the need for copper etching (1,2). It has been proposed that 1,1,1,5,5,5-hexafluoro-2,4-pentanedione (hfac) can be utilized to etch copper (3,4,5). For dry vapor phase cleaning hfac has been explored as a possible cleaning agent for copper and other transition metals such as Fe, Ni, and Cr (6). While mechanisms of Cu deposition from Cu-ß-diketonate complexes are well documented, the surface mechanisms for etching using the free ß-diketone ligands have not yet been determined.

In either reactive chemical vapor cleaning (CVC) of copper or reactive chemical vapor etching (CVE) of copper, hfac interacts with the surface bound copper to form a volatile, stable coordination compound as a metal chelate. In order to develop chemical processes which rely on this chelation chemistry, it is necessary to understand the relationship between the chemical state of the species to be removed (copper) and the possible surface reaction mechanisms.

Helms and Park recently developed a generalized thermodynamic model to describe the reactivity of metallic contaminants as a function of their chemical state on the surface of a silicon wafer (7). Contaminant metal bonding on native oxide surfaces of silicon were examined through ternary phase diagrams. The three component system in this approach is comprised of Si,O, and Metal. It is difficult to predict accurately the real chemical environment of a contaminant through this method and thus it is not possible to make predictions of mechanisms of a cleaning process. In this paper the interactions of hfac with the much simpler system of O and Cu were examined. The system of Cu and O is comprised of three oxidation states of copper: cupric oxide (Cu^{+2}), cuprous oxide (Cu^{+1}), and copper metal ($Cu^{(0)}$). This paper provides results of an x-ray photoelectron spectroscopic (XPS) investigation of hfac reactions with bulk films of CuO, Cu_2O, and $Cu^{(0)}$.

EXPERIMENTAL

The substrates utilized were copper foils 1 mm thick and 150 mm Si wafers which had a film of sputtered copper (100 nm) deposited on a sputtered tantalum (100 nm) adhesion layer/etch stop. For investigations of $Cu^{(0)}$ surfaces samples were, cleaned in successive rinses of reagent grade acetone and methanol, and placed in the introduction chamber of the XPS chamber. For investigations of CuO surfaces, 15 mm square samples of the Si wafers were oxidized in a quartz tube furnace in an ambient of dry cylinder air at 350° C for four hours. This oxidation converts the metallic copper to CuO and oxidizes a portion of the underlying Ta to Ta_2O_5. CuO films prepared in this manner were typically 170 nm thick as measured by a Tencor step profilometer. This thickness is within 5% of that predicted from the density change occurring upon conversion of the 100 nm Cu film to CuO.

Cu_2O films were prepared by oxidation of Cu metal in a 70 ppm ambient of O_2 in N_2 at 800° C for 45 minutes. This partial pressure of O_2 has been determined to be in equilibrium with Cu_2O by Roberts and Smith (8). Following oxidation, the samples were cooled in an ambient of N_2. This procedure oxidized the $Cu^{(0)}$ to Cu_2O, but left a thin surface layer of CuO and created a mixed film of Ta_2O_5 and Cu_2O near the original Ta/Cu interface.

The surface analysis system consisted of a Physical Electronics double pass cylindrical mirror analyzer with a 5 keV electron gun. A dual filament, dual source 300 watt x-ray gun was utilized to irradiate the sample with Mg kα radiation (1253.6 eV). The UHV chamber is connected through a sample introduction system to the reactor utilized for hfac reactions and sample manipulators allow direct transfer of the mounted samples between the UHV chamber and the hfac reactor.

The reactor consisted of a pyrex tube which slid over the sample and sealed against a viton gasket encapsulating the mount and puck. Hfac was delivered to the pyrex tube

through a bubbler using a N_2 carrier. This arrangement protects the walls of the reactor chamber from contacting hfac, thus eliminating potential contamination due to reactions of hfac with the stainless steel chamber. All gas connections and isolation valves were constructed of teflon, viton and pyrex. Gas analysis of the hfac delivery system showed a background O_2 contamination level less than 5 ppm in the N_2 measured at the exit port of the reactor at atmospheric pressure.

During hfac exposures and XPS characterization the samples were mounted on a Ni puck. Sample heating was achieved through a graphite disk heating element embedded in the puck and a backside flow of UHP He to aid heat transfer to the sample. Temperature regulation was achieved through closed loop control, using a type R thermocouple placed at the heater surface. The reactor was equipped with a 12 mm diameter quartz McCarrol microwave cavity which was used to dissociate Ar/O_2 mixes for removing adventitious carbon from the sample surface by a downstream plasma process. The cavity was oriented parallel to the substrate surface so that bombardment by ions and UV photons was avoided. Surface temperatures were calibrated versus the thermocouple probe by a 0.125 mm type R thermocouple brought in contact to a sample surface. Calibration temperatures were established at the operating pressures of the hfac reactions and downstream plasma cleans.

All hfac exposures were conducted at a total pressure of 10 torr, a partial pressure of hfac of approximately 2.5 torr, and a N_2 flow rate of 38 sccm. Surface temperatures during these experiments were fixed at temperatures ranging from 140° to 265° C. Experiments were conducted by placing a sample in the reactor and encapsulating the sample in the pyrex tube. The surface was brought to the desired temperature and pressure under a flow of N_2. The reaction was initiated by switching the N_2 flow through the hfac bubbler for the desired amount of time. The reaction was terminated by switching the N_2 to the bypass position and turning off the heater. Depending on the process temperature, approximately 5 to 10 minutes elapsed before the sample cooled to 100° C and could be transferred to the UHV chamber for surface analysis.

RESULTS

Elemental and chemical state information was obtained from the photoelectron spectra by two methods. O(1s), C(1s), and F(1s) chemical state information was deduced by shifts in the relative binding energy of the respective line positions (10). Cu chemical state information was obtained through the use of a combination of the $Cu(2p_{3/2})$ and the $Cu(L_3M_{45}M_{45})$ electron transition. This combination is defined as the Auger parameter which is the sum of the binding energy of the $Cu(2p_{3/2})$ photoelectron and the kinetic energy of the $Cu(L_3M_{45}M_{45})$ Auger electron (9,10). Accepted values of the Auger parameter are: $Cu^{(0)}$ 1850.8eV; CuO 1851.4eV and Cu_2O 1849.1eV (7). $Cu^{(0)}$ and CuO are further differentiated by the location of the $Cu(2p_{3/2})$ at 932.4eV and CuO at 933.2eV and the absence of lower kinetic energy "satellite" peaks of CuO (9,10).

Copper Metal (Cu)

For copper metal studies both Si and Cu foil substrates were utilized. Hfac exposures at 140°,165°,203°,and 265° C revealed no binding energy shifts to $Cu(2p_{3/2})$ or O(1s), however small amounts of F and C were detected. The F(1s) spectra revealed a peak at 688eV which is assigned to a C-F type bonding. There was no peak detected at 686eV which would be indicative of Cu-F bonding. An additional peak was detected at 689.3eV which can be assigned to a Cu-O-F type bond. The C(1s) spectra showed a peak at 284.8 eV and a small peak at 292.7eV, these peaks are indicative of C-H and CF_3, respectively. From other work it has been determined that hfac does not react with $Cu^{(0)}$ to form a volatile compound under the conditions investigated in these experiments, and therefore does not etch $Cu^{(0)}$ (11).

Cuprous Oxide $Cu^{(+1)}$

Cu_2O surfaces were used as obtained from the oxidation furnace without any further cleaning. Surface analysis of these substrates revealed a significant signal at 285eV which we assigned to adventitious carbon. This adventitious carbon could interfere with identification of reaction products remaining on the surface following hfac exposures. To remove this interference the surface was subjected to a downstream microwave plasma. Plasma conditions were 250 millitorr and 100 sccm flow of 95%Ar/5%O_2 at 70 watts of forward power, a surface temperature of 140°C and a duration of 10 minutes. This procedure typically reduced the C(1s) signal by a factor of 10. The surface of these plasma cleaned samples are CuO with the bulk comprised of Cu_2O. Exposures of these surfaces to hfac at 140° and 165 °C left these surfaces unchanged for a 60 second exposure. However, at 203° and 265 ° C the CuO film was removed during the initial 30 seconds of exposure to hfac, leaving Cu_2O as the surface. A subsequent 5 minute exposure to hfac at the same temperature leaves $Cu^{(0)}$ on the surface. XPS spectra corresponding to this sequence of hfac exposure is illustrated in figure 1, which shows the $Cu(2p_{3/2})$ photoelectron spectra for the 265° C sample before hfac exposure, following a 30 second exposure and 300 second exposure.

Cupric Oxide $Cu^{(+2)}$

CuO surfaces prepared for these experiments contained a photoelectron peak at 285eV which corresponding to adventitious carbon. Therefore, theses surfaces were also cleaned with the O_2/Ar microwave plasma. At temperatures of 140° and 165° C an exposure to hfac for 120 seconds leaves the Cu in the form of CuO, similar to results obtained for Cu_2O surfaces. Under the conditions employed it is impossible to tell if only a portion of the CuO layer is being removed or if no reaction is taking place. Nevertheless, it is clear that the chemical state of the Cu remained unchanged for these two temperatures. Strikingly different results occur at 203° and 265° C for similar duration exposures. At these two temperatures the surface is etched to the Ta_2O_5 interface with 3 at.% Cu left

behind as $Cu^{(0)}$. At an exposure of 120 seconds the Cu is still in the CuO chemical state. The change in oxidation state as a function of exposure is illustrated in figure 2 which shows the $Cu(2p_{3/2})$ photoelectron spectra at 120 second and 300 second exposures at 265° C.

DISCUSSION

The results of the hfac interactions discussed above have been utilized to propose plausible mechanisms to corroborate existing information on the reactions of $Cu(hfac)_2$ and the thermochemistry of Cu, Cu_2O and CuO. Our intent is to explain why interactions with Cu_2O leave $Cu^{(0)}$ on the surface and why essentially all of the CuO is removed with only traces of $Cu^{(0)}$ left behind.

Before discussing any of the concerns listed above it is beneficial to consider the thermochemistry of the Cu-O system. It is known that CuO can be reduced to a lower oxidation state by the following reduction reaction (10):

$$2CuO + \Delta \rightleftarrows Cu_2O + \tfrac{1}{2} O_2 \qquad [1]$$

where Δ is heat, photons or energetic neutrals. Rosencwaig and Wertheim demonstrated the reduction of CuO to Cu_2O at 250° C by heating in high vacuum with exposures to x-ray irradiation(12). In this investigation a film of CuO was exposed to the Mg Kα radiation from the 300 watt x-ray gun for 8 hours with periodic sampling of the photoelectron spectra. There was no observable change in the photoelectron spectra; however, our CuO film thickness is 170 nm. In another attempt to reduce the CuO film, a substrate was heated in 10 torr of UHP Ar at 265° C. The photoelectron spectra showed a change to Cu_2O type bonding between 4 and 5 hours. We believe the reduction reaction occurs from the Ta_2O_5/CuO interface outward. As O is generated during the reduction it migrates away from the interface, driven by concentration gradients. As O migrates to the tantalum side it further oxidizes tantalum metal. In the Cu film, O migrates in a direction away from the interface creating a gradient of reduced copper that decreases with distance from the Ta_2O_5/Cu_2O interface and reaches the surface only after the entire film has been reduced. With a sampling depth of only 10 nm, XPS reveals changes in oxidation state only after the entire film has been reduced. Li and Mayer recently published a review of copper oxide reduction reactions and describe in detail this process (13). The <u>overall</u> reaction for CuO with hfac is illustrated in equation **[2]** (3).

$$2\ hfac + CuO \rightleftarrows Cu(hfac)_2 + H_2O \qquad [2]$$

At sufficiently elevated temperatures reduction of CuO according to reaction **[1]** would then compete with the hfac complexation reaction. Further examination of the thermochemistry of the Cu-O system reveals that an equilibrium exists between $Cu^{(0)}$,

Cu_2O and O_2 (8,14). This equilibrium can be written in the form of a further reduction as illustrated by equation **[3]**:

$$Cu_2O + \Delta \rightleftarrows 2Cu^{(0)} + \tfrac{1}{2}O_2 \qquad [3]$$

In this set of experiments it was observed that the reaction of hfac with Cu_2O at 203° and 265° C leaves a $Cu^{(0)}$ surface. This surface may form due to further reduction of Cu_2O to $Cu^{(0)}$ according to reaction **[3]** or by some other mechanism involving the hfac - solid reaction as indicated by the following overall reaction:

$$Cu_2O + 2\ hfac \rightleftarrows Cu^{(0)} + Cu(hfac)_2 + H_2O \qquad [4]$$

Unfortunately it is impossible to determine from data acquired in this study the exact reaction, **[3]** or **[4]**, which is responsible for the creation of the $Cu^{(0)}$. Reactions of hfac with films of CuO at 203° and 265° C for durations of greater than 120 seconds leave very small quantities of $Cu^{(0)}$ at the interface of the Ta_2O_5 surface. This can be explained by invoking a combination of reactions **[1]**,**[3]** and **[4]** to create a small quantity of $Cu^{(0)}$ at the original CuO/Ta_2O_5 interface. For all exposures the O(1s) photoelectron spectra reveal a relative increase in amount of OH^- bonding after exposure to the hfac. This result substantiates arguments for the overall reactions in **[2]** and **[4]**, where one would expect H_2O product to leave a hydrogenated surface.

F(1s) spectra of all samples exposed to hfac show a C-F bond at 688eV. It is possible that this bonding occurs from reactions of an impurity in the hfac, since none of the ratios of the peaks in the C(1s), O(1s) and F(1s) photoelectron spectra correspond to that expected for an hfac molecule. Investigators utilizing XPS to analyze surfaces of $Cu^{(0)}$ deposited from $LCu^{I}hfac$ (L= nuetral ligand) and $Cu^{II}hfac_2$ clearly see ratios of C(1s), O(1s) and F(1s) which correspond to stoichiometry of hfac (15). Furthermore it is not expected that the hfac molecule would dissociate at the surface temperatures utilized in this investigation. Future work will focus on identification of impurities responsible for changes to surfaces during hfac processes.

CONCLUSIONS

The process utilizing hfac to remove Cu from a surface is dependent on the initial chemical state of the Cu. While detailed mechanisms are not known, three overall reactions which are known to occur in the hfac-Cu-O system (**[1]**,**[2]**, and **[3]**) and one proposed reaction (**[4]**), can explain the surface behavior observed in these experiments. This information is useful in identifying process for chemical vapor cleaning (CVC) processes.

ACKNOWLEDGEMENTS

The authors would like to thank Gene Karwacki for numerous discussions on the interpretation of the photoelectron spectra. We also would like to acknowledge the expertise of Jim Stets who preformed SEM analysis on some of the samples.

REFERENCES

1. V.M. Donnelly and M.E. Gross, J. Vac. Sci. Technol. A 11(1), 77 (1993).
2. S.L. Cohen, M. Liehr, and S. Kasi, Appl. Phys. Lett. 60(13), 1585 (1992).
3. F Rousseau, A. Jain, T.T. Kodas, M. Hampden-Smith, J. Doug Farr, and R. Muenchausen, J. Mater. Chem. 2(8), 893-894 (1992).
4. J.A.T. Norman, B.A. Muratore, P.N. Dyer, D.A. Roberts, and A.K. Hochberg, J. Phys. IV, C2-271 (1991).
5. M.J. Hampden-Smith and T.T. Kodas, MRS Bulletin,18 (6), 39 (1993).
6. J.C. Ivankovits, D.A. Bohling, A. Lane, and D.A. Roberts, Proceedings of the 2nd International Symposium on Cleaning Technology in Semiconductor Device Manufacturing, Electrochemical Society, Vol. 92-12, 105 (1992).
7. C.R. Helms and Heungsoo Park, to be published in the Proceedings of the 1993 Spring Cleaning Symposium of the Material Research Society.
8. H.S. Roberts and F. Hastings Smith, J. Am. Chem. Soc.,**43**, 1061(1921).
9. C.D. Wagner, W.M. Riggs, L.E. Davis, J.F. Moulder, and G.E. Muilenberg, Handbook of Photoelectron Spectroscopy, Perkin-Elmer Corporation, Eden Prarie, MN (1979).
10. P.E. Larson, Journal of Electron Spectroscopy and Related Phenomena, 4, 213 (1974).
11. D.A. Roberts, J.C. Ivankovits, J.A.T. Norman, and D.A. Bohling, U.S. Patent 5028724 (1992).
12. A. Rosencwaig and G.K. Wertheim, J. Electron Spectroscopy, 1, 493 (1973).
13. J. Li and J.W. Mayer, Materials Chemistry and Physics, **32**, 1 (1992).
14. F.L. Weichman and J.M. Reyes, Can. J. Phys., **58**, 325 (198).
15. S. L. Cohen, M. Liehr, and S. Kasi, J. Vac. Sci. Technol. **A 10**(4), 863 (1992).

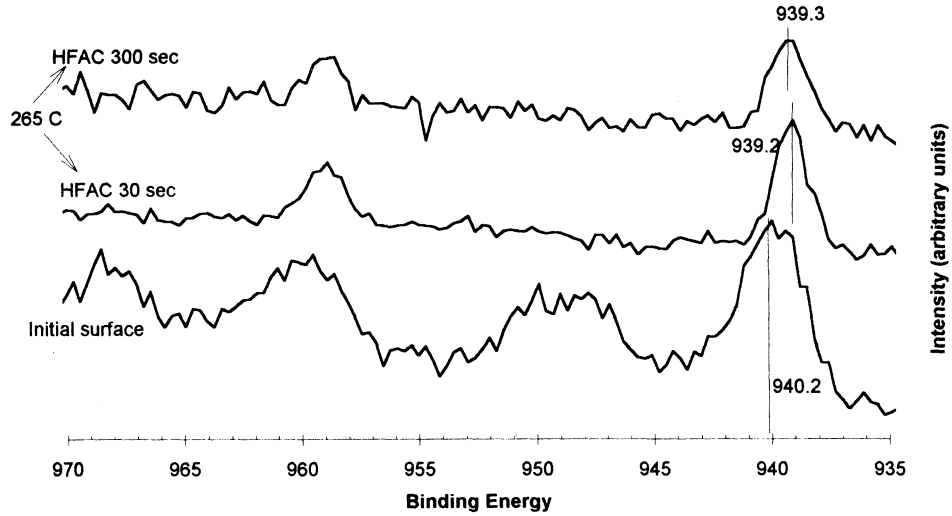


Figure 1. Cu $2p_{3/2}$ Photoelectron spectra of a film of Cu_2O before hfac exposure and after hfac exposures of 30 and 300 seconds. The surface temperature was 265° C and hfac partial pressure 2.5 torr. The initial surface has "shakeup" peaks and an Auger parameter of 1852 which indicates the surface is CuO (cupric oxide). The 30 second exposure has an Auger parameter of 1848.6 which is indicative of Cu_2O (cuprous oxide). The 300 second exposure has an Auger parameter of 1851.1 which is indicative of $Cu^{(0)}$ (metallic). The sample charged approximately 7.0 eV in all three experiments.

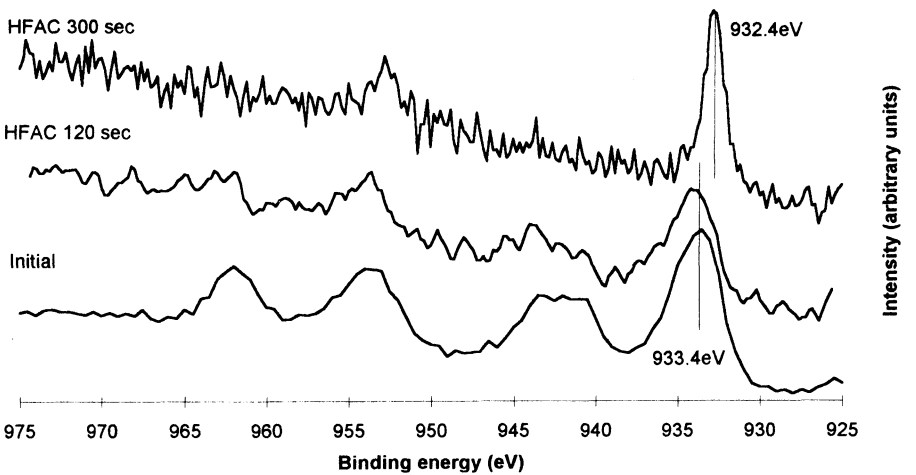


Figure 2. Cu $2p_{3/2}$ Photoelectron spectra of a film of CuO before hfac exposure and after hfac exposures of 120 and 300 seconds. The surface temperature was 203° C and hfac partial pressure 2.5 torr. The initial surface and 120 second exposures have "shakeup" peaks indicative of CuO (cupric oxide). The 300 second exposure has a shift in the binding energy of 1eV and no shakeup peaks, indicative of $Cu^{(0)}$ (metallic). The hfac 300 second exposure represents about 3at.% of the sampled surface, the majority being Ta and O in a ratio of 1:2.5.

REMOVAL OF Al FROM SILICON SURFACES USING UV/Cl_2

C. Daffron, K. Torek, and J. Ruzyllo,
Electronic Materials and Processing Research Laboratory
The Pennsylvania State University
University Park, PA 16802

E. Kamieniecki
QC Solutions, Inc.
Lexington, MA 02173

A gas-phase UV/Cl_2 cleaning process applied using a commercial dry cleaning module has demonstrated the ability to remove aluminum contaminant from a silicon wafer surface. Immersion in an SC-1 solution was used as a method of aluminum contamination. SIMS and Surface Charge Analysis were used to monitor the amount of aluminum remaining on the surface. The reduction of surface aluminum was increasingly effective with increasing wafer temperature and decreasing pressure.

INTRODUCTION

Besides iron, aluminum is recognized as the most difficult to eliminate metallic contaminant in silicon device processing (1). Therefore, methods of aluminum removal must be available in both liquid-phase and gas-phase cleaning modes. In the former case, the SC-2 solution ($HCl:H_2O_2:H_2O$) is effective in aluminum removal. In the latter case, various approaches have been tried with various degree of success.

The purpose of this study was to explore further the use of chlorine interaction with the silicon surface in the presence of UV (ultra-violet) irradiation (UV/Cl_2 process) as a way to remove aluminum from the silicon surfaces. Chlorine is used as a reaction gas because it forms metal chlorides which are more volatile than other metal halides, and because it produces radicals while under UV irradiation. The feasibility of this approach has already been demonstrated (2). In this work the same method is implemented using a prototype commercial dry cleaning module.

EXPERIMENTAL PROCEDURE

Both p-type and n-type, (100), silicon wafers were used in this study. All wafers were subjected to standerd wet clean to establish reproducible starting surface conditions. Subsequently, they were contaminated with aluminum by

immersion in an SC-1 solution (3) consisting of 700 ml of H_2O, 150 ml of H_2O_2, and 100 ml of HCl at 80 °C followed by D.I. water rinse. As demonstrated recently, even the concentration of Al in SC-1 as small as 0.1 ppb will result in the surface concentration of Al on the silicon surface as high as 10^{12} cm^{-2} (4). Dried wafers were then cleaned using a gas-phase UV/Cl_2 procedure implemented using a new type of a cluster tool compatible commercial apparatus (5). The tool is equipped with IR lamps as well as a Xenon UV flashtube which irradiates the inside of the reactor chamber through a sapphire window (Fig. 1). The tool in the version used in this investigation was equipped with an aluminum process chamber. Under certain process conditions erosion of the process chamber did interfere with cleaning processes.

The cleaning procedure consisted of an anhydrous HF/CH_3OH pre-treatment to remove the native oxide from the wafer surface (6), followed by a UV irradiated chlorine radical gas exposure to remove the aluminum contaminant. The pre-treatment step was performed at 300 Torr, 80 °C for 30 seconds. Various process parameters were used during the UV/chlorine exposure step (wafer temperature was varied form 70 °C to 200 °C and gas pressure from 10 Torr to 150 Torr).

The amount of aluminum remaining on the wafer surface was measured directly by Secondary Ion Mass Spectroscopy (SIMS) immediately following the dry cleaning process. An indirect evaluation of the aluminum content was carried out using Surface Charge Analysis (SCA). Prior to SCA, 200 Å thick thermal oxide was grown at 950 °C on a contaminated wafer surface to form negatively charged aluminum oxide complexes (7). By doing this, differentiation between negative charge associated with SC-1 aluminum and iron has become possible as the latter is known to remain during thermal oxidation at the oxide-Si interface where it introduces interface traps.

RESULTS AND DISCUSSION

The results of SCA analysis performed on the wafers immersed prior to thermal oxidation for various times in SC-1 solution are shown in Fig. 2 for both p- and n-type silicon substrates. Initially positive, oxide charge turns negative upon exposure to SC-1 solution. Prolonged exposure to SC-1 changes this charge only slightly. The change of oxide charge vs. immersion time for both dopant types is virtually identical (Fig. 2), and therefore, the mechanism of negative charge formation is idependent of the conductivity type of the substrate.

In order to use SCA to monitor the removal of Al originating from SC-1 solution, a correlation between Al presence on the surface and SC-1 immersion was independently established. Among various surface

characterization methods, SIMS is particularly effective in Al detection, and hence, this method was used in this experiment. Figure 3 shows significant increase of the Al content on the wafer immersed for 10 min. in SC-1 as compared to the reference sample, thus, confirming SCA results showing Al deposition on the surface by SC-1 immersion.

SIMS was also used for initial evaluation of the effectivness of the UV/Cl_2 exposure in removing Al contaminants. Having the option of the *in situ* etching of chemical oxide in anhydrous HF/CH_3OH mixture prior to UV/Cl_2 exposure, we have at first investigated the effect of this oxide on the aluminum removal process. The results shown in Fig. 4 indicate that the aluminum reduction is more efficient if the chemical oxide resulting from SC-1 immersion is etched off *in situ* prior to UV/Cl_2 exposure. Also, SCA analysis has shown that only limited change in the negative oxide charge is accomplished as a result of UV/Cl_2 exposure only (Fig. 5) indicating slow rate of Al volatilization. This result is understood in the light of the recent determination that Al originating from SC-1 solution is distributed on the surface and in the chemical oxide, whereas Fe and Zn are found on the surface on such oxide only (4). On the other hand however, a lack of ultrathin oxide on the silicon surface and/or non-uniform oxide coverage may promote surface roughening during UV/Cl_2 exposure. As revealed in this study by Atomic Force Microscopy (AFM) evaluation, no surface roughning was observed under the process conditions applied. At the same time however, no detectable etching of silicon as a result of UV/Cl_2 exposure was observed. It is generally assumed that the removal of heavy metals from the silicon surface during UV/Cl_2 treatment requires slight etching of silicon so that volatilization of metal chlorides is aided by the lift-off process related to the rapid evaporation of the silicon chlorides (2). As a result, observations made regarding chemical oxide etching in the context of aluminum removal may not necessarily be valid in the case of removal of other metals. This issue will be carefully ddressesd in our future investigations.

All results presented hereafter in this paper are concerned with processes in which UV/Cl_2 exposure was preceded by *in situ* HF/CH_3OH etching of chemical oxide. These results can be summarized as follows.

Figure 6 shows the aluminum to silicon ratios derived from SIMS measurements performed on the wafers exposed to UV/Cl_2 for various times. As seen in this figure, the aluminum level decreases as the exposure time was increased up to 3 minutes. The final determination concerning UV/Cl_2 exposure time needed to accomplish a complete removal of Al from the silicon surface under the process conditions used in this experiment could not be done at this time.This is because for the longer UV/Cl_2 exposure times errosion of the aluminum process chamber in our system intefered with evaluation of aluminum removal efficiency.

The SIMS results were confirmed by surface charge analysis. Figure 7 shows variations of the oxide charge as a function of UV/Cl_2 exposure time. Comparison of curves in Fig. 5 and Fig. 7 stresses the importance of the oxide etching process applied prior to UV/Cl_2 exposure. In Fig. 7, the nagative oxide charge is seen to gradually decrease and turn positive showing that Al is gradually being removed under these conditions. The surface charge analysis have also demonstrated that increased wafer temperature during UV/Cl_2 exposure facilitates the volatilization of aluminum as illustrated in Fig. 8 by changes in the oxide charge.

SUMMARY

The results of this study have confirmed the ability of UV/Cl_2 processing to reduce aluminum on silicon surfaces. The effectiveness of the process was limited unless the silicon chemical oxide was etched off *in situ* prior to UV/Cl_2 exposure. This may be related to the distribution of Al originating from the SC-1 solution in the chemical oxide rather than on the surface of this oxide. In this study the removal of aluminum was accomplished without etching silicon. This last can potentially result in surface roughening. However, the removal of some other metals under the same process conditions, i.e. without slight etching of the silicon substrate, may not be as effective.

ACKNOWLEDGMENTS

This project was supported by the Semiconductor Research Corporation under the contract 92-MJ-274. Thanks are also due to SubMicron Systems, Inc. for providing dry cleaning tool used in this study and to SemiTest, Inc. for making a SCA system available to us.

REFERENCES

1. W. Murray, and W. O'Mara, Solid State Tech., 59, April (1993).
2. R. Sugino, M. Okuno, M. Shigeno, Y. Sato, A. Ohsawa, and T. Ito, Proc. Second Intern. Symp. Cleaning Technol. in Semicon. Dev. Manufacturing, Eds. J. Ruzyllo and R.Novak, The Electrochemical Society, 92-12, 72 (1992).
3. J. Atsumi, S. Ohtsuka, S. Munehira, and K. Kajiyama, Proceedings-The Electrochemical Society, 90-9, 59 (1990).
4. I. Takahashi, J. Ryuta, T. Shingyouji, M.B. Shabani, E. Morita, and Y.Shimanuki, Abst. No. 303, The Electrochem. Soc. Fall Meeting, New Orleans, Oct. 10-15,1993
5. Cluster Clean SP-200, SubMicron Systems, Inc., Allentown, Pennsylvania
6. J. Ruzyllo, K. Torek, C. Daffron, R. Grant, and R. Novak, J. Electrochem. Soc., 140, L64 (1993).
7. J. Kato, and Y. Maruo, J. Electrochem. Soc., 139, 1756 (1992).

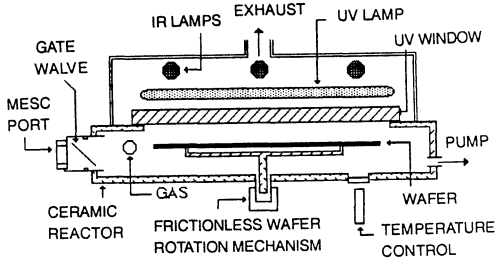


Fig.1 Schematic cross section of the reactor used in this study (5).

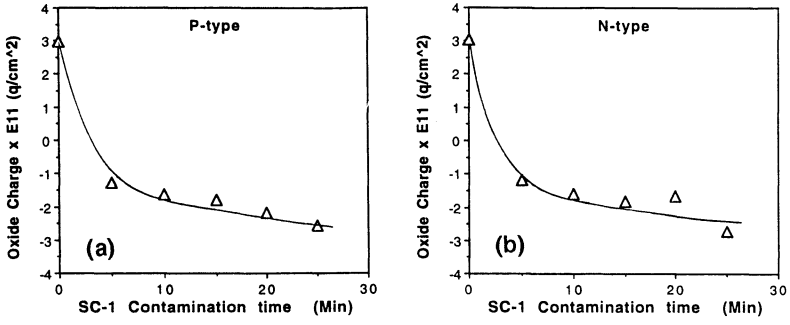


Fig.2 Oxide charge vs. SC-1 immersion time for (a) p-type and (b) n-type Si wafers.

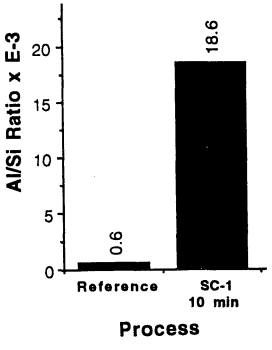


Fig. 3 SIMS results showing increased concentration of Al on the Si surface exposed to SC-1 solution.

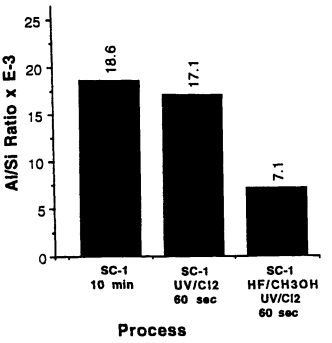


Fig. 4 SIMS results showing more effective removal of Al in the case UV/Cl_2 exposure was preceded by *in situ* etching of chemical oxide

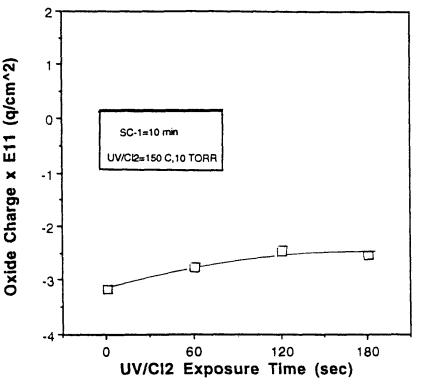


Fig. 5 Oxide charge vs. UV/Cl_2 exposure time without preceding oxide etching step.

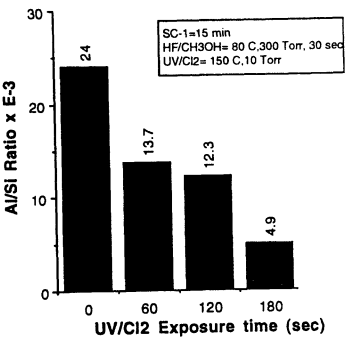


Fig. 6 SIMS results showing changes in Al content as a function of UV/Cl_2 exposure time with preceding oxide etching step.

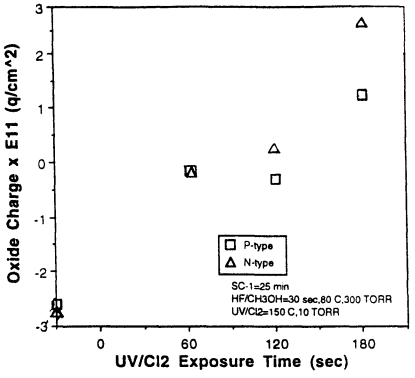


Fig. 7 Oxide charge vs. UV/Cl_2 exposure time with preceding oxide etching step.

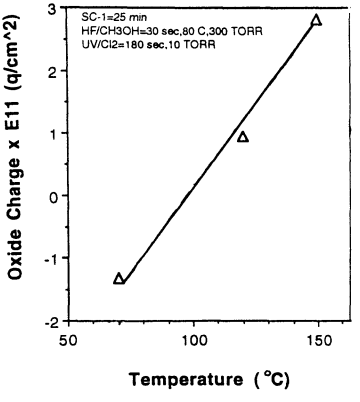


Fig. 8 Oxide charge vs. wafer temperature during UV/Cl_2 exposure.

INTEGRATED PREDEPOSITION CLEANING/PASSIVATION OF Si SURFACES FOR MOS DEVICES WITH SiO_2/Si INTERFACES

S. Hattangady, V. Misra, T. Yasuda, X-L Xu, B. Hornung,
G. Lucovsky and J.J. Wortman

Departments of Materials Science and Engineering, Electrical and Computer Engineering, and Physics, North Carolina State University, Raleigh, NC 27695.

ABSTRACT

A novel approach consisting of i) a low-temperature, 300-400°C, plasma-assisted oxidation to form the SiO_2/Si interface, and ii) 800°C rapid thermal chemical vapor deposition, RTCVD, to deposit the bulk SiO_2 film has been used to fabricate ultrathin gate-oxide heterostructures. This sequence *separates* SiO_2/Si interface formation from the bulk oxide film formation. We have studied the chemistry of the interface formation process by Auger electron spectroscopy (AES) and the electrical properties of the SiO_2/Si interface in device structures including MOS capacitors and FETs. The plasma-assisted oxidation pre-deposition treatment (i) removes residual carbon contamination from the Si surface, (ii) creates a ~ 0.6 nm SiO_2 layer that establishes the crucial SiO_2/Si interface and serves as a foundation for the subsequent rapid thermal CVD oxide, and (iii) forms a low D_{it} SiO_2/Si interface with peak channel mobilities, μ_{eff}, comparable to that of control thermal oxides formed with traditional high-temperature furnace oxidation.

INTRODUCTION

The drive towards ultra-large-scale integration implies a continuous down-scaling of device dimensions and, consequently, ultrathin gate dielectrics with thicknesses of < 10 nm SiO_2 equivalent thickness. This has provided an incentive for the development of low-temperature, low-thermal budget processes for fabricating reliable, ultra-thin gate dielectrics. Rapid thermal processing, RTP[1,2], and low-temperature plasma-assisted deposition[3-5] have emerged as promising candidates for this type of device processing. Both direct-plasma[3] and remote-plasma[4,5] enhanced CVD, RPCVD, processes have been reported for low-temperature gate oxide depositions. The remote-plasma process has been shown[4,5] to produce thin oxide films at low temperatures, ~ 300°C, with very good electrical interface and bulk oxide properties, e.g., D_{it} ~ 2-5 x10^{10} cm^{-2}-eV^{-1}, and breakdown fields, E_b ~ 10 MV-cm^{-1}. Recently, a two-step remote-plasma process consisting of a (i) plasma-assisted oxidation, and (ii) plasma-assisted deposition, was

shown[4] to consistently produce excellent electrical interfaces with even lower mid-gap D_{it} of ~ 1-3 x 10^{10} cm^{-2}-eV^{-1}. However, the low-temperature plasma-deposited oxide films are typically characterized by lower charge-to-breakdown, poorer breakdown integrity, and therefore lower reliability in comparison with thermally grown oxides formed by traditional high-temperature (> 900°C) furnace oxidation.

We describe a two-step process for the formation of gate oxide structures that *separates* interface formation from bulk oxide film formation, that includes high temperature post-processing as well. The key elements of this approach are (i) a low-temperature, 300-400°C, plasma-assisted oxidation to generate a ~ 0.5-0.6 nm oxide which establishes the SiO_2/Si interface, and (ii) an 800°C RTCVD SiO_2 deposition that forms the bulk of the gate dielectric film. The plasma-assisted oxidation treatment (i) removes residual surface carbon contamination from an otherwise H-terminated Si surface by oxidation to CO, CO_2, H_2O, etc., (ii) forms a superficial (~ 0.6 nm) SiO_2 layer that (a) establishes a device-quality SiO_2/Si interface and (b) serves as a *chemical template* for the RTCVD deposited oxide. We have thus combined the advantages of chemically-controlled interface formation by plasma-assisted oxidation, and the robust character of SiO_2 films deposited at a relatively high temperature (800°C) by RTCVD. These two steps have been performed *in situ* and sequentially in a single-chamber UHV-compatible reactor. This process has also been extended to include in-situ deposition of polysilicon gates followed by an ex-situ doping process at 900°C. FET devices formed in this way display peak field-effect mobilities that are comparable to those on control devices that include thermal oxides grown at 900°C. This paper includes effects of short rapid thermal annealing done in situ between the plasma-assisted oxidation and RTCVD oxide depositions.

EXPERIMENTAL

The substrate materials used in this study were 4 inch p-type Si(100) wafers doped to ~ 2x10^{17} cm^{-3}. The wafers were wet-chemically cleaned by the hot-RCA cleaning process described elsewhere[6]. A field oxide was grown thermally, and patterned and etched to reveal the gate-oxide regions. The wafers were hot-RCA cleaned again. Some were rinsed in 1:30 HF:H_2O for 15 s, and then rinsed in running de-ionized water for 5 s and blown dry with filtered, dry N_2. This ensured the complete removal of the wet-chemically grown native oxides and left the Si surface H-atom terminated in the regions of the patterned wafer that were allocated to gate oxide deposition. On other wafers, the final HF rinse was omitted thereby leaving the final wet chemical oxide as a platform for the deposition of the RPCVD oxide film.

A schematic of the dual RTP-RPCVD reactor is shown in Figure 1. The schematic shows a long quartz tube connected to an ultra-high vacuum compatible stainless-steel system. A quartz plasma tube is connected upstream to the main quartz chamber. Megaclass process gases are introduced through a gas feed connected to the top of the plasma tube. The substrate is located in an all-quartz region and, therefore, in an ultra-

high purity environment during processing. The unused process gases and reaction by-products are evacuated through a dry mechanical process pump, Edwards Drystar 40, thus eliminating contamination problems usually associated with oil-based pumps. Substrate heating, in a range between 300°C and 900°C is accomplished with the use of external heater lamps, thus simplifying the internal construction of the reactor. A ~10^{-7} Torr base pressure is achieved with a turbomolecular pump before the initial processing and between subsequent processing steps. In summary, thus, the dual RTP-RPCVD reactor (i) lends itself to ultraclean processing, (ii) offers process flexibility, and (iii) possesses the advantages of multiprocessing capabilities, in that we can perform both rapid-thermal processing and remote-plasma processing or combinations thereof.

For substrates subjected to both plasma and rapid thermal processes, the substrates were ramped up to the oxidation temperature, 300-400°C, in an Ar atmosphere, 200 sccm, 0.30 Torr, over ~2 minutes. Oxygen was then introduced at a flow rate of 10 sccm. The plasma was then initiated and the wafer subjected to a 15 s plasma-assisted oxidation treatment using a 30W rf O_2/Ar discharge. The gas flow and the heaters were immediately cut off following this treatment and the chamber evacuated by the turbo pump to remove any residual O_2. The RTCVD SiO_2 film, ~11 nm, was then deposited with 500 sccm N_2O and 25 sccm SiH_4, 10% in Ar, at a pressure of 3 Torr and a temperature of 800°C over a duration of ~115 s. In a few cases, a vacuum rapid thermal anneal (800-950°C for 90s) was inserted prior to the RTCVD SiO_2 deposition.

MOS capacitors and FETs were then fabricated by standard techniques. For the capacitors, Al was used as the gate electrode material. Post-metallization annealing (PMA) was performed in forming gas, 10% H_2 and 90 %N_2, at a temperature of 400°C for a duration of 30 minutes. Standard photolithography and etching procedures were then performed to complete the device fabrication. In the case of FETs, the processing for the devices included in-situ RTCVD of a ~ 200 nm polysilicon layer following the oxide deposition. This was performed using 300 sccm SiH_4, 10% in Ar, at a pressure of 5 Torr and a temperature of 700°C. This was then followed by (i) an ex-situ dopant drive-in process at 900°C, (ii) (Ti + Al) metallization over the doped poly-Si, (iii) patterning of the device structures, and (iv) a PMA in forming gas at 400°C for 30 min.

Three types of device structures were studied. The important point to note is that the SiO_2/Si interface was formed in three different ways: (a) In the plasma-processed wafers, the interface was primarily formed between the plasma-oxide and the underlying silicon. For the wafers not subjected to the plasma-assisted oxidation, it was formed in one of two ways (b) by the final step of the RCA clean in which case the interfacial oxide is predominantly constituted of the wet-chemical native oxide, and (c) by the RTCVD oxide for those wafers subjected to the rinse in dilute HF following the RCA clean, in which case the interface is formed directly between the RTCVD oxide and the substrate. Note that, separately, a control thermal oxide (dry, 900°C) was also included to serve as a standard for comparison.

RESULTS AND DISCUSSIONS

Chemical Analysis

In a separate RPCVD reactor system integrated with a surface analytical unit, the surface of the Si wafer before and after a plasma pre-oxidation treatment was studied by Auger electron spectroscopy (AES) following transfer of the wafer *in vacuo* from the main chamber to the analytical chamber. The results are summarized in Figure 3. Figure 3(a) shows the AES spectrum of the Si wafer following wet-chemistry and prior to the plasma-oxidation treatment. The spectrum shows distinct C *KLL* and O *KLL* features, in addition to the Si *LVV* features, attesting to the presence of appreciable carbon and trace oxygen remaining on the surface. Figure 3(b) shows the AES spectrum from the same surface immediately following the plasma-oxidation treatment. The carbon signal is virtually unnoticeable thereby attesting to the removal of carbon off the surface to the limit of the AES sensitivity, ~ 0.5 atomic percent. The higher oxygen intensity, on the other hand, is a consequence of superficial oxidation. It is emphasized that the disappearance of a C-atom signature is not a result of a burying of these C-contaminants since the oxide was sufficiently thin, ~0.6 nm or 2-3 atomic layers as estimated from the attenuation of the Si *LVV* features, to permit detection of any interfacial C-species at the SiO_2/Si interface.

Electrical Analysis

MOS Capacitor Characterization

The electrical test data for the MOS capacitor structures obtained from the analysis of capacitance-voltage (C-V) measurements is summarized in Table I. High frequency, 1 MHz, and quasi-static C-V curves were obtained using standard Hewlett-Packard equipment. All C-V data were taken with a voltage sweep rate of 35 $mV\text{-}s^{-1}$. The interfacial density of trapping state densities, D_{it}, was calculated using the high/low frequency method discussed in Ref. 7. The flat band voltages, V_{fb} were also obtained using standard analysis procedures, also outlined in Ref. 7. For a *p*-type substrate material with a hole concentration of ~ $2x10^{17}$ cm^{-3} and using an Al gate electrode, we expect a flat band voltage of -0.85±0.05 V. For this doping density, the minimum detectable value of D_{it} is ~ $2x10^{10}$ $cm^{-2}\text{-}eV^{-1}$. For a thermal oxide grown on the same substrate wafers, we obtained D_{it} = ~ $5x10^{10}$ $cm^{-2}\text{-}eV^{-1}$, and a flat band voltage of -0.88 V. The range of flat band voltages obtained for all wafers in this study was from -0.8 to -1.0 V, and the D_{it} values ranged from $3.5x10^{10}$ $cm^{-2}\text{-}eV^{-1}$ to $12x10^{10}$ $cm^{-2}\text{-}eV^{-1}$, consistent with our expectations for this level of substrate doping, and for the use of Al gate electrodes.

The plasma-processed wafers clearly showed the lowest D_{it} values. Also, the V_{fb} values were consistent with that observed with the control thermal oxide. Furthermore, we did not observe any significant differences between wafers that have been subjected to a vacuum pre-anneal at 800°C for 90 s, prior to the RTCVD oxide deposition, and those

that did not receive this pre-deposition treatment. The higher values of D_{it} for the 400°C oxidation are consistent with the results of previous studies[4]. On the other hand, we observed important differences for the wafers not subjected to the pre-deposition superficial plasma-assisted oxidation step: (a) for the case where the wafers were *not* subjected to the HF rinse, and therefore retained the last chemical oxide of the RCA clean, (i) the D_{it} values are measurably higher than those observed for the plasma processed wafers, and are not changed by the vacuum anneal, and (ii) the flat band voltage is significantly different from that for the control thermal oxide, i.e. less negative, -0.78±0.03 V; however, the V_{fb} approaches the expected value when the in situ vacuum anneal is inserted in the processing sequence. (b) For those wafers for which the last RCA clean sacrificial oxide has been removed by the rinse in dilute HF, the values of D_{it} are significantly higher than for the other pre-deposition processing. In addition, the V_{fb} values are higher than anticipated, indicating a positive fixed charge in the oxide.

MOSFET Characterization

Table II summarizes the peak MOSFET mobility (μ_{eff}) derived from the transconductance characteristics in the linear region (V_{ds} = 0.05V). Also included in the table are the threshold voltage, V_T, values for the respective cases. Figures 3 and 4 show the variation in μ_{eff} as a function of the effective field across the gate oxide, $(V_g-V_T)/t_{ox}$ for the different interface formation and thermal treatments.

The peak effective mobility is the lowest for the case where the wet-chemical oxide is the interfacial oxide. Also, the V_T value (Table II) is higher than that for the thermal oxide. Another important observation (Fig. 3) is that the fall-off in μ_{eff} at higher fields (fall-off characteristic) is shifted to lower field regions and also occurs at a much faster rate than that observed in the case of the control thermal oxide. Note that there is an improvement in the peak value of μ_{eff} when the wet-chemical oxide is removed prior to the RTCVD SiO_2 deposition. More importantly, the device formed with the plasma-assisted interfacial oxide exhibits a μ_{eff} value comparable to that observed for the control thermal oxide. Furthermore, the shift in the μ_{eff} fall-off characteristic is less than that observed for the wet-chemical oxide interface (Fig. 3). Additionally, the V_T value is closer to the expected value. Clearly, the wet-chemical native oxide is detrimental to interfacial quality.

Vacuum annealing of the interfacial plasma-oxide was investigated to examine any effects on V_T and the μ_{eff} fall-off characteristic. Annealing of the interfacial plasma-oxide at 800°C for 90s showed little change in both μ_{eff} and V_T values compared to no separate annealing case wherein any post-deposition thermal annealing occurred in situ during the poly-Si deposition and/or ex-situ dopant drive-in. The fall-off characteristic also remained unaffected (figure not shown). However, annealing at 950°C, while showing a small drop in the peak μ_{eff}, showed two specific improvements: (i) an improvement in the fall-off characteristic (as evidenced from its slope), as seen in Figure 4 , and (ii) V_T values approach those observed with thermal oxides. Based on these exploratory studies, we feel that the annealing process is an important step that needs to be optimized in order to induce any further improvements.

CONCLUSIONS

Our results show that low-temperature, 300-400°C pre-deposition plasma-assisted processing can be combined with intermediate-temperature, 600-800°C, rapid thermal depositions of SiO_2 thin films to yield high performance gate oxide structures. Specifically, device-quality SiO_2/Si interfaces have been formed with a two-step, low-thermal budget process that *separates interface formation from bulk oxide film formation.* The key elements of the process are (i) a low-temperature, plasma-assisted oxidation of the Si, (ii) an 800°C RTCVD SiO_2 deposition, and (iii) a 700C RTCVD poly-Si deposition. The plasma oxidation pre-treatment (a) removes residual carbon contamination from the Si surface (b) forms a ~ 0.6 nm SiO_2 layer that establishes the crucial SiO_2/Si interface and serves as a "template" for the subsequent rapid thermal CVD oxide, and (c) forms a *consistently* low D_{it} and high μ_{eff} SiO_2/Si interface. All processing is performed in-situ and sequentially in a single-chamber ultraclean, flexible reactor system. This aspect of integrated processing is essential in preserving the chemical integrity of the superficially oxidized surface prior to the RTCVD process. Our results emphasize that it is critical to remove the wet-chemical native oxide before commencing any processing. Furthermore, it is essential to passivate this clean surface with a plasma-oxide prior to the RTCVD processing. Annealing of this oxide shows further improvements as evidenced by improvements in V_T and the rate of fall-off in μ_{eff} with gate oxide field. The combination of all of these results suggests that the interface formation process is a critical aspect of device fabrication for structures employing deposited oxides, and that the insertion of the plasma-assisted process holds promise as a complementary processing step in rapid thermal processing sequences for deposited dielectrics on Si substrates.

ACKNOWLEDGMENTS

This research is supported in part by Office of Naval Research, the NSF Engineering Center for Advanced Electronic Materials Processing (NCSU), the North Carolina SEMATECH Center of Excellence, and the Semiconductor Research Corporation.

REFERENCES

1. G.Q. Lo, W.C. Ting, D.K. Shih, and D.L. Kwong, Appl. Phys. Lett. **56**, 979 (1990).
2. X-L Xu, R.T. Kuehn, J.J. Wortman and M.C. Ozturk, Appl. Phys. Lett. **60**, 3063 (1992).
3. J. Batey and E. Tierney, J. Appl. Phys. **60**, 3136 (1986).
4. T. Yasuda, Y. Ma, S. Habermehl, and G. Lucovsky, Appl. Phys. Lett. **60**, 434 (1992).
5. G.G. Fountain, R.A. Rudder, S.V. Hattangady, R.J. Markunas, and P.S Lindorme, J. Appl. Phys. **63**, 4744 (1988).
6. W. Kern, Semiconductor International, 94 (1989).
7. E.H.Nicollian and J.R. Brews, in MOS Physics and Technology (John Wiley and Son, New York, 1982).

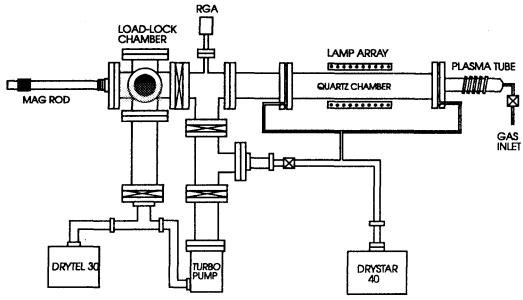


Figure 1: Schematic of the dual RTP-RPECVD reactor

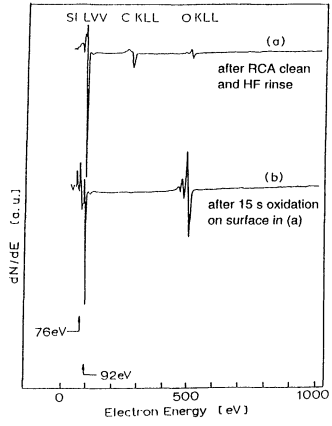


Figure 2:
AES analysis of the Si surface:
(a) after RCA clean and HF rinse, and prior to oxidation
(b) following plasma-assisted oxidation

MIDGAP INTERFACE STATE DENSITIES, D_{it} (x 10^{10} cm^{-2} eV^{-1})

Pre-deposition *plasma* oxidation (with HF rinse)			NO Pre-deposition Oxidation		Control Thermal Ox (900C, dry)
Oxidation Temp (C)	No Vacuum Anneal	Vacuum Anneal (before RTCVD SiO_2)	No HF Rinse	With HF Rinse	
300	3.7 - 3.8	3.8 - 4.1			
400	4.8 - 5.0	4.6 - 4.8	5.1 - 7.0	7.1 - 12.0	5.4 - 6.0

FLAT-BAND VOLTAGE, V_{fb} (± 0.03 V)

Pre-deposition *plasma* oxidation (with HF rinse)			NO Pre-deposition Oxidation		Control Thermal Ox (900C, dry)
Oxidation Temp (C)	No Vacuum Anneal	Vacuum Anneal (before RTCVD SiO_2)	No HF Rinse	With HF Rinse	
300	-0.86	-0.87			
400	-0.88	-0.88	-0.78*	-0.98	-0.88

*-0.87 (vac. annl).

Table I: Electrical Test data on MOS Capacitor Structures

WAFER PROCESS	Peak Effective Mobility, (cm^2/Vs)	Threshold Voltage, V_T (V)
Thermal Oxide (dry, 900°C)	415.8 ± 1.4	0.68 ± 0.003
RTCVD Oxide		
(i) RCA clean oxide interface	379.9 ± 6.9	0.88 ± 0.06
(ii) oxidation during RTCVD	386.7 ± 8.0	0.63 ± 0.05
(iii) Plasma-oxide interface		
- as-deposited (no anneal)	410.2 ± 7.5	0.79 ± 0.05
- vacuum anneal (800°C/90s)	414.8 ± 5.5	0.79 ± 0.06
- vacuum anneal (950°C/90s)	402.3 ± 6.7	0.65 ± 0.04

Table II: Electrical Test data on MOSFET structures

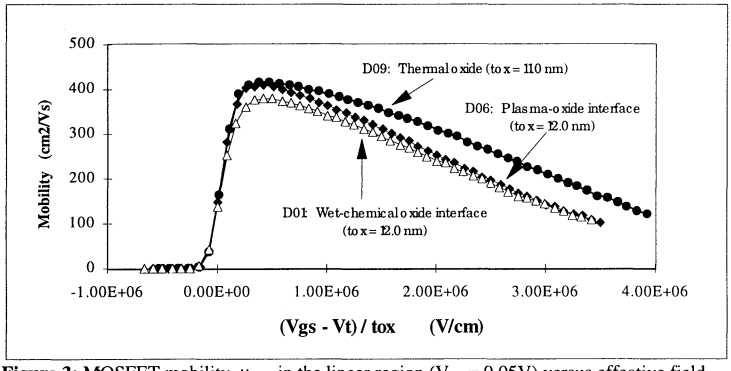


Figure 3: MOSFET mobility, μ_{eff}, in the linear region (V_{ds} = 0.05V) versus effective field, $(V_{gs}-V_T)/t_{ox}$, in the gate oxide showing the detrimental effects of the wet-chemical native oxide interface.

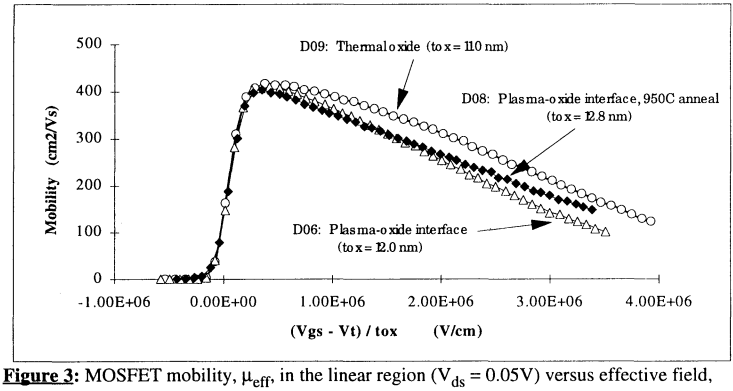


Figure 3: MOSFET mobility, μ_{eff}, in the linear region (V_{ds} = 0.05V) versus effective field, $(V_{gs}-V_T)/t_{ox}$, showing the effects of a 950°C RTA of the plasma-oxide prior to RTCVD SiO_2.

HYDROGEN PLASMA CLEANING PRIOR TO LOW TEMPERATURE GATE OXIDE DEPOSITION IN CLUSTER-FABRICATED MOSFETS

J.S. Montgomery, J.P. Barnak, A. Bayoumi, J.R. Hauser, and R.J. Nemanich
Center for Advanced Electronic Materials Processing
Department of Physics
Department of Materials Science and Engineering
Department of Electrical and Computer Engineering,
North Carolina State University
Raleigh, NC 27695

In this study we evaluate the effectiveness of the hydrogen plasma cleaning of Si(100) prior to the deposition of the gate oxide in the fabrication of the "stacked-gate" field effect transistor. Atomic force microscopy and auger electron spectroscopy are used for surface characterization of the H-plasma clean. The data from AFM shows roughening of the silicon surface in the 150°C to 300°C range. From 400°C to 700°C the surface has a relative rms roughness of ≈2.5 Å, comparable with wafers not treated with the plasma. The AES data indicates less than monolayer coverage of carbon and oxygen. These surface characterization results are then correlated to the MOSFET performance. The performance of the MOSFET is characterized by the threshold voltage and the peak value of the effective mobility. The threshold voltages averaged -0.16 V±0.10 V for samples prepared with H-plasma below 400°C while those processed above 400°C averaged 0.21 V±0.14 V. For plasma durations of 10 minutes, from 400°C to 700°C the peak effective mobility increased from 211 cm^2/Volt-sec to 264 cm^2/Volt-sec. The high field decay of the effective mobility is also measured as an indication of the scattering due to surface roughness.

INTRODUCTION

The hydrogen plasma clean has been investigated as an effective *in-situ* technique for the removal of adsorbates from the silicon surface prior to chemical vapor deposition, atomic layer epitaxy and molecular beam epitaxy (1-4). In these analysis the primary focus has been on the characterization of the surface using standard techniques of auger electron spectroscopy, low energy electron diffraction, reflection high energy electron diffraction, scanning electron microscopy, atomic force microscopy, scanning tunneling microscopy, transmission electron microscopy and others. In separate studies capacitors

and MOSFETs have been fabricated and evaluated on the basis of the processing parameters including *ex-situ* and *in-situ* cleaning configurations prior to gate oxidation (5-7). The preparation of low defect Si-SiO_2 interfaces in the metal-oxide-semiconductor structures is strongly dependent on the silicon surface microstructure and surface contaminants. Therefore, both approaches, surface analysis and device performance, address the same issues but from different perspectives. Cluster-based processing provides the environment to carry out both techniques concurrently. In this study hydrogen plasma cleaning has been considered as a possible *in-situ* cleaning step following *ex-situ* wet chemistry in preparation for the next steps in a cluster arrangement. In previous studies employing AES and LEED, the hydrogen plasma clean has shown that it can remove surface hydrocarbons and leave the surface in a reconstructed state (4). In preliminary work for this study, AFM has also shown that the hydrogen plasma clean can be used without significantly roughening the surface. Surface characterization becomes increasingly important if these analysis can be confirmed in the performance of completed electronic devices. With surface characterization and device performance correlated, surface preparation can be tailored to particular specifications which are known to enhance device performance. In experiments described here, we use the metal-oxide-semiconductor field effect transistor (MOSFET) as the test structure for the effects of the plasma parameters and compare the performance of these devices to the surface analysis of the hydrogen plasma-silicon interaction. The surface analysis produces information on contaminants at the surface; these primarily being carbon and oxide.

EXPERIMENT

The experiments were conducted in a prototype UHV cluster module processing system developed at the Center for Advanced Electronic Materials Processing (8). The equipment is incorporated into the "cluster" configuration in which three process chambers and one analysis chamber are served by a central wafer handler accessible by a wafer entry/exit load lock. The system uses 100 mm diameter wafers and has a load lock which accepts a 25 wafer cassette. The cluster includes a rapid thermal processing (RTP) module, a remote plasma enhanced chemical vapor deposition (RPECVD) module, and a remote plasma cleaning (RPC) module. The analysis chamber is accessible to the other modules through the RPC chamber and has capabilities for auger electron spectroscopy (AES) and reflection high energy electron diffraction (RHEED). A pressure in the 10^{-6} Torr range is established and maintained in the load lock and wafer handler before and during any processing. The RTP module base pressure is maintained in the 10^{-7} Torr range while the RPECVD and RPC chambers have base pressures $\approx 5 \times 10^{-9}$ Torr. The analysis chamber has a base pressure in the mid 10^{-10} Torr range. Therefore, all transfers are made in an high vacuum environment and cross contamination between processes is essentially eliminated.

The plasma cleaning chamber is kept in the UHV range with a turbomolecular pump backed by a multistage roughing pump. The chamber is equipped with a convectron gauge, a cold cathode gauge and a residual gas analyzer. A capacitance manometer provides pressure feedback to a throttling valve for pressure control during processing. The wafer is heated with a PBN ceramic coated resistive element heater controlled by a current source in concert with a thermocouple. Plasma excitation occurs within a quartz tube mounted to the top of the chamber. The RF signal is fed to a coil which has 5 turns along approximately 5 cm of the discharge tube. Hydrogen is delivered to the tube via a mass flow controller in line with the laboratory gas delivery system. The sample was held ≈ 10 cm from the end of the discharge tube during these experiments.

The experiment was divided into three groups of samples. Twenty-five silicon wafers were allocated for the batch to be processed for device fabrication. The samples were (100) orientation p-type silicon, boron doped to a resistivity of 0.05-0.10 Ω-cm and patterned with a 2000 Å field oxide by the ERC-2 mask appropriate for MOSFET fabrication. The batch of 25 wafers was then *ex-situ* cleaned as detailed in Table I.

Table I. Ex-Situ Cleaning Procedure

Base solution: H_20:NH_4OH (30%):H_2O_2 (30%) ⇒ 5:1:1
Acid solution: H_20:HCl (38%):H_2O_2 (30%) ⇒ 5:1:1

1. Dip the wafers in the 80°C base solution for 10 minutes.
2. Rinse the wafers in running DI water for 5 minutes.
3. Dip the wafers in room temperature HF solution for 20 seconds.
4. Dip the wafers momentarily in running DI water.
5. Dip the wafers in the 80°C acid solution for 10 minutes.
6. Rinse the wafers in running DI water for 5 minutes.
7. Dip the wafers in room temperature HF solution for 10 seconds.
8. Place the cassette of wafers in running DI water. Remove each wafer, spin dry, and load wafers into the load lock cassette.
9. Move wafers to the load lock for pump down.

The entire boat was then transferred to the load lock cassette and the load lock. Each wafer in turn was transferred into the plasma cleaning chamber for processing according to its specific process parameters. The parameters varied in this series include cleaning temperature, 200°C to 700°C, duration of plasma exposure, 2 minutes to 60 minutes, and RF power, 20 Watts or 50 Watts. Pressure was held constant for this group at 15 mTorr. Following the hydrogen plasma treatment the wafer was returned to the load lock cassette. Each hydrogen plasma cleaned wafer was then moved to either the RPECVD or the RTP for oxide deposition. Target gate oxide thickness for both

processes was 100 Å. Once again the wafer was returned to the load lock. The final step in the Cluster I processing was the deposition of the poly-silicon to provide the gate contact for the MOSFETs. Target thickness of the polysilicon deposition was 1000 Å. Following all *in-situ* processing the wafers were removed from the load lock and transported to another facility at NCSU for the final processing as detailed in Table II.

Table II. Processing Steps for Device Fabrication.

1. $POCl_3$ doping of polysilicon - 900°C
2. Apply photoresist/ Etch polysilicon/ Strip photoresist
3. RCA clean followed by a buffered oxide etch (BOE)
4. Low temperature oxide deposition - 2000 Å - 410°C
5. Forming gas anneal - 500°C - 10% H_2/ 90% N_2
6. Apply photoresist/ Etch oxide/ Strip photoresist
7. Sputter titanium - 1000 Å
8. Evaporate aluminum - 8000 Å
9. Apply photoresist/ Etch aluminum and titanium/ Strip photoresist
10. Forming gas anneal - 400°C - 10% H_2/ 90% N_2

Sixteen wafers were allocated for AFM analysis. These samples followed the same *ex-situ* procedure as the device wafers and then were loaded for plasma cleaning. The samples were then treated with hydrogen plasma cleans similar to the samples prepared for MOSFET fabrication. In this parallel series the temperature was varied between room temperature and 700°C, the exposure was set at 10 minutes and the power was set at 20 Watts. Again, the pressure for each experiment was maintained at 15 mTorr. Following the hydrogen plasma clean, the samples were then removed from the cluster module processing system and taken for AFM analysis. This analysis was conducted on a Park Scientific Inc. system outfitted with a 10 μ scanner and cantilevers tipped with silicon nitride pyramids with a 3:1 aspect ratio and nominal tip radius of 100 Å.

The transistors used for this series had a gate areas of 100μ, 300μ, and 500μ. Analysis of the devices follows the simple model of transistor operation when obtaining the threshold voltage, V_t, and the effective mobility, μ_{eff}.(9) The threshold voltage is more accurately defined as the extrapolated threshold voltage taken from the I_d-V_d curve with a gate voltage of 3 V. The effective mobility is given by

$$\mu_{eff} = \frac{g_d}{C_{ox}(V_G - V_t)}\left(\frac{W}{L}\right), \qquad [1]$$

where C_{ox} is the capacitance of the gate oxide, V_D is the applied drain voltage, W is the gate width, and L is the gate length. $g_d = (dI_d/dV_d)_{Vg}$ is the transconductance measured at gate voltage Vg.

When the effective mobility is plotted, we can calculate two parameters of the electron mobility at the interface; those being the peak mobility and the high field falloff coefficient. The peak of the effective mobility curve can be compared to the ideal case for boron doped silicon at 300°C of 500 cm^2/Volt-sec.(10) The high field falloff coefficient is a derived constant indicative of the contribution of surface roughness scattering to the mobility of the carriers.(11) This analysis is based on the variational calculations of Ando, et. al.(11) and presents a correlation between this surface scattering parameter, m, and the effective mobility given below

$$\frac{1}{\mu_{eff}} = m\left(N_{dep} + \frac{11}{32}N_{inv}\right)^2, \qquad [2]$$

where N_{dep} is the depletion layer space charge and N_{inv} is the inversion layer space charge.

In-situ analysis using RHEED and AES for selected samples was conducted separately from the device series and the AFM series and was evaluated using standard techniques.

RESULTS

The evaluation of the surface morphology using AFM revealed two effects based on the wafer temperature and the duration of plasma exposure (Fig. 1). The baseline used for the relative rms roughness of the silicon wafer following the *ex-situ* clean but prior to plasma clean was 1.15 Å±0.31 Å where for each value cited the standard deviation is a statistical calculation based on multiple scans. Following the hydrogen plasma clean at the low temperatures (200°C, 300°C) and for the 10 minute durations the surface was roughened to an average value of 18.81 Å±8.70 Å. A representative AFM scan is shown in Fig. 2. For the cleans at higher temperatures, 450°C to 700°C, the surface roughness varied between 0.96 Å and 3.69 Å with no strong correlation to temperature (Fig. 3). The second observed effect was the temporal effects between 2 minute plasma exposures, 5 minute exposures, and 10 minute exposures. The 2 minute and 5 minute plasmas for all temperatures left the surface with rms roughness values between 2.5 Å and 3.7 Å with no major differences between the two durations regarding morphology. In comparing the 2 and 5 minute exposures to the 10 minute plasma there is a marked increase in the surface roughness of the low temperature samples. The temporal behavior of the samples from

450°C to 700°C show no increase in the surface roughness due to exposure length. RHEED analysis shows corresponding variations in changes to the substrate temperature. For the 200°C/10 minute samples we observe a very diffuse 1x1 diffraction pattern. At 450°C/2 minutes the diffraction pattern was a diffuse 2x1 reconstruction. Both the 450°C/10 minute and the 600°C/5 minute show a diffuse 1x1 RHEED pattern. The starting surface following the RCA clean yielded a sharp 1x1 reconstruction. The auger electron analysis of selected wafers produced the following results. The AES spectra of the starting surface prior to plasma cleaning was virtually free of contaminants with only trace quantities of carbon and oxide. Following the hydrogen plasma clean for the 2 and 5 minute plasmas for 300°C and 450°C, increased quantities of carbon and oxygen become evident on the surface with greater than monolayer coverage. The 600°C/5 minute sample produced a spectra with carbon and oxygen as well as nitrogen contamination.

In the results of device performance, we begin with basic operation as seen in the overall yield of working devices and the extrapolated threshold voltage. The yield varied from 83% and 100% with an overall yield of 91%. The threshold voltage showed a significant variation over the range of process parameters. For plasma durations of 10 minutes average per wafer values for V_t varied from -0.24 to 0.31 V with a strong correlation to temperature (Fig. 4). There is also evident a non uniformity in V_t across the wafer based on chip location.

Measurements were taken of the low field transconductance which was mathematically converted to determine a peak mobility value and an effective mobility curve. The average peak mobility per wafer for the 10 minute processes varied from 154±11 cm^2/Volt-sec for the low temperature processes to 258±8 cm^2/Volt-sec for the 700°C case as shown in Fig. 5. The wafers treated for 2 minutes showed better mobility characteristics, ranging from 121±56 cm^2/Volt-sec at 200°C to 299±37 cm^2/Volt-sec at 700°C. The effective mobility values were then plotted against the square of the total space charge as given in Eq. 2. The m coefficient for this series did not show any conclusive trends relative to the process parameters. A similar effect to the threshold voltage was seen in the variance of m based on chip location. Average m values ranged from 7.5 to 9.5.

DISCUSSION

The hydrogen plasma clean has been shown previously(4) and in this report to degrade the silicon surface for low temperatures and extended durations. In the case of this study we see an increase in the surface roughness with a corresponding drop in threshold voltage and peak mobility. In the low temperature regime (<300°C) the

substrate temperature is appropriate for the formation of SiH_4 to produce an etch reaction at the surface(12). This plasma induced roughness produces interface charges as a result of the surface defects. This drives the threshold voltage down and lowers the mobility of the electrons due to an increased number of scattering sites. In the temperatures above 400°C the surface coverage of atomic hydrogen is reduced therefore reducing the etch due to SiH_4 fragmenting. A change in the mechanism of the plasma-surface interaction is seen in the increase of threshold voltage in the 300°C to 500°C range. At these higher temperatures the AFM, threshold voltage, and peak mobility again coincide with a decrease in the number of plasma induced defects. The higher temperatures leave the surface morphology unchanged with surface contamination as the foremost concern. Although there was increased presence of carbon, oxygen and nitrogen for the higher temperatures, the rms roughness, threshold voltage, and peak mobility continued to improve over the same range. More evidence for higher temperature contamination is supported by the RHEED study. In the low temperature cleans the reconstruction is a very diffuse 1x1. We attribute this to surface roughening as opposed to surface contaminants as the AES for the low temperature samples showed only minor increases in the contaminant peaks. In the high temperature cleans the RHEED analysis cannot be related to the surface roughness with sufficient carbon, oxygen, and nitrogen as seen by AES to produce the diffuse 1x1. Therefore the diffuse 2x1 reconstruction represents a combination of two effects: 1) the dominance of the high temperature etch mechanism leaving the surface structure highly ordered and 2) the onset of high temperature contaminants. We propose two possible explanations regarding the presence of carbon, oxygen, and nitrogen in the upper temperature regime. Both explanations involve equipment and not process configurations or hydrogen plasma interactions. First, the pyrolytic boron nitride heater could be the source of nitrogen and small traces of hydrocarbons as the ceramic is heated. Another possible source for these elements is the process gas which is not purified before entering the plasma cleaning chamber.

CONCLUSION

The electrical characterization indicates that the hydrogen plasma within certain parameter regions can be used as an *in-situ* cleaning technique without compromising device performance. Combining the AFM data and the threshold voltage data, process regimes can be established to plasma clean in a low-etch rate environment leaving the surface morphology similar to the starting surface.

ACKNOWLEDGMENTS

This work has been partially supported by the National Science Foundation Engineering Research Centers Program through the Center for Advanced Electronic Materials Processing (Grant CDR 8721505), the Semiconductor Research Corporation (SRC contract #93-MP-132), and the SRC Sematech Center of Excellence program at NCSU (SRC contract #93-MP-509).

The authors would like to expressly thank the following people for the hours of processing, device testing, and helpful discussions: T.P. Schneider, R.J. Carter, C. Silvestre, J.B. Flanigan III, M. Watkins, C. Parker, M. Gleaton, R. Luckett, J. McEwan, E. Vick, and R. Howard.

REFERENCES

1. B. Anthony, L. Breaux, T. Hsu, S. Banerjee, and A. Tasch, Journal of Vacuum Science and Technology B, 1989. **7**: p. 621-626.
2. T. Hsu, B. Anthony, R. Qian, J. Irby, S. Banerjee, A. Tasch, S. Lin, and H. Marcus, Journal of Electronic Materials, 1991. **20**: p. 279-287.
3. A. Tasch, S. Banerjee, B. Anthony, T. Hsu, R. Qian, J. Irby, and D. Kinosky, in Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing. 1992, J. Ruzyllo and R. Novak , Editors, p. 418-427, The Electrochemical Society,
4. T.P. Schneider, J. Cho, D.A. Aldrich, Y.L. Chen, D. Maher, and R.J. Nemanich, in Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing. 1992, J. Ruzyllo and R. Novak , Editors, p. 123-132, The Electrochemical Society,
5. P.O. Hahn and M. Henzler, Journal of Vacuum Science and Technology A, 1984. **2**: p. 574-583.
6. T. Ohmi, K. Kotani, A. Teramoto, and M. Miyashita, IEEE Electron Device Letters, 1992. **12**: p. 652.
7. H.X. Liu, Proc. of the Mat. Res. Soc., (Spring 1993) in press. **315**.
8. J.R. Hauser, N.A. Masnari, and M.A. Littlejohn, Mat. Res. Soc. Symp. Proc., 1989. **146**: p. 15.
9. Y.P. Tsividis, Operation and Modeling of the MOS Transistor. p. 157-158. McGraw-Hill, New York (1987).
10. A.S. Grove, Physics and Technology of Semiconductor Devices. Wiley, New York (1967).
11. T. Ando, A.B. Fowler, and F. Stern, Reviews of Modern Physics, 1982. **54**: p. 437.
12. M. Gates, R. Kunz, and C. Greenlief, Surface Science, 1989. **207**: p. 364-384.

FIGURES

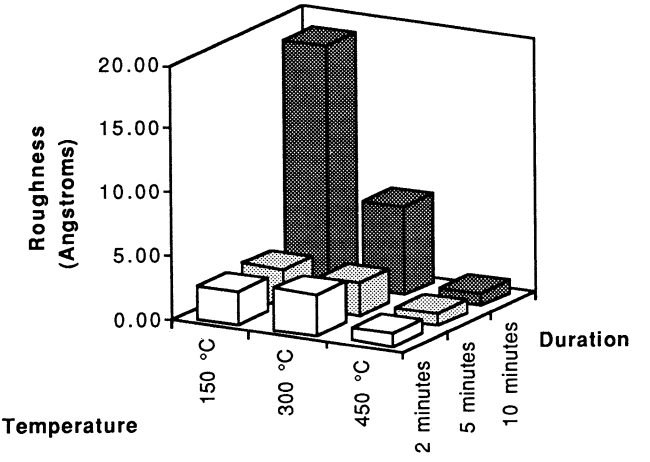


Figure 1. The relative rms roughness vs. H-plasma duration and substrate temperature. The rms roughness were obtained from 10 μm x 10 μm AFM scans of the surface after processing

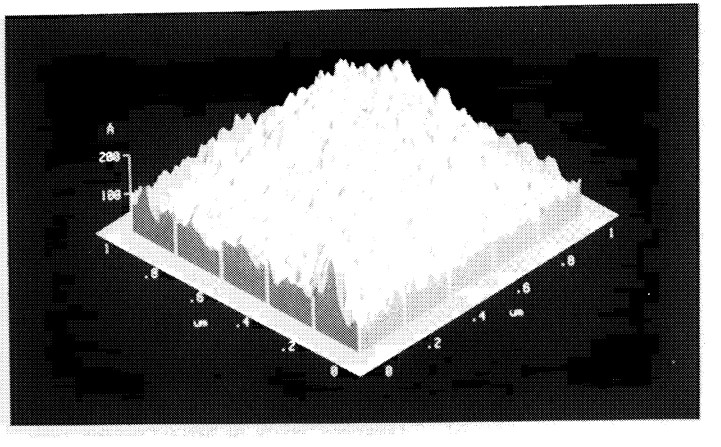


Figure 2. A representative AFM scan of H-plasma cleaned silicon at 150°C for 10 minutes with a process pressure of 15 mTorr

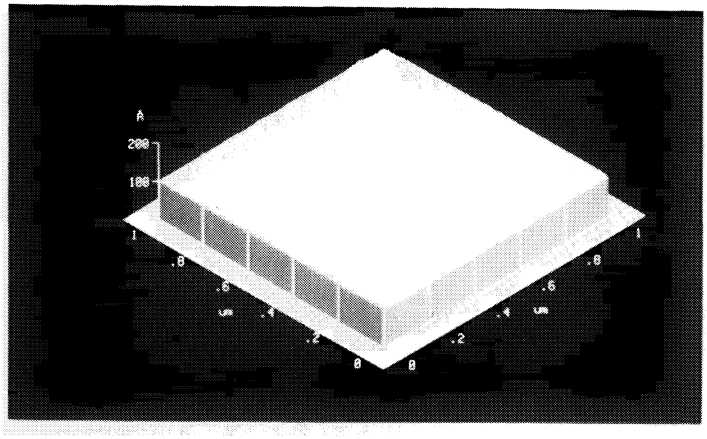


Figure 3. A representative AFM scan of H-plasma cleaned silicon at 450°C for 10 minutes with a process pressure of 15 mTorr

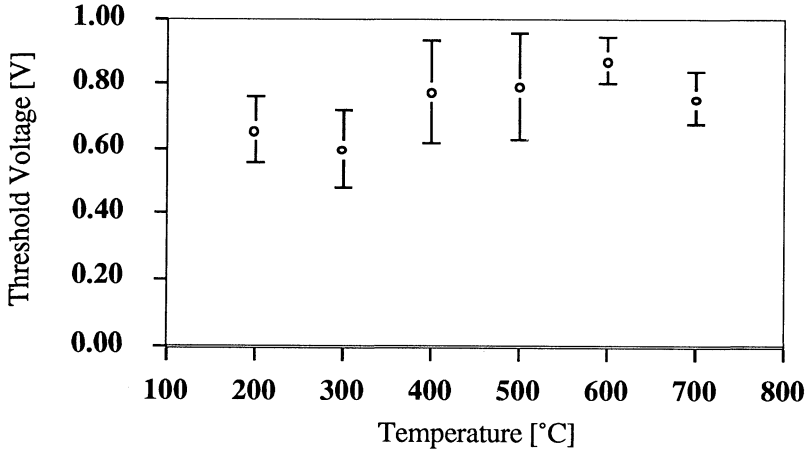


Figure 4. Plot of threshold voltage, V_t, vs. substrate temperature during H-plasma cleaning .

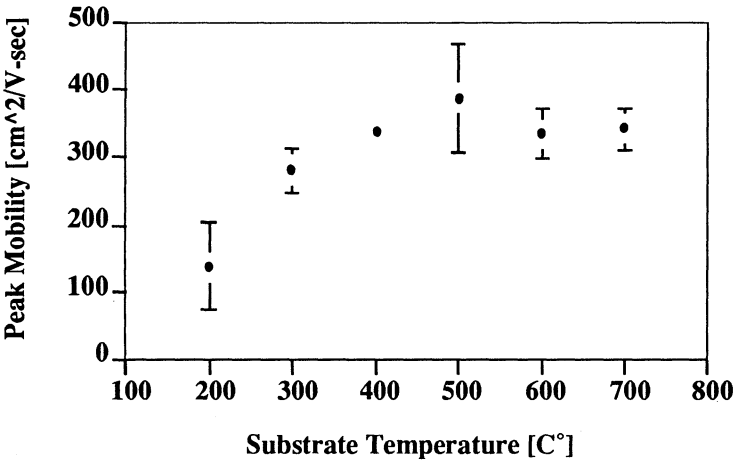


Figure 5. Plot of peak mobility vs. substrate temperature during H-plasma cleaning .

Comparison of In-situ, Isotropic Downstream, and Inductively Coupled Plasma Downstream Post-Contact Etch Cleaning

P. I. Mikulan, T. T. Koo, and S. J. Fonash

Electronic Materials and Processing Research Laboratory
The Pennsylvania State University,
University Park, PA 16802

K. A. Reinhardt [a]

SEMATECH, Austin, TX 78741

Removal of the residue polymer layer on silicon resulting from an oxide etch is examined using several cleaning approaches. Blanket silicon wafers were etched in a split powered diode reactor using a $CHF_3/CF_4/Ar$ chemistry and then were cleaned either in-situ, in an independent isotropic downstream strip module or in an independent inductively coupled plasma downstream strip module. These different cleaning procedures used a variety of flourial based chemistries. These different approaches to post-contact etch cleaning were then evaluated using X-ray photoelectron spectroscopy, single wavelength ellipsometry, thermal wave modulated reflectance, and Schottky barrier current-voltage measurements.

INTRODUCTION

Using carbon and fluorine based chemistries for contact etching often leads to the formation of undesired polymer layers at the silicon surface. Even when these polymer layers are as thin as 20 Å they still can degrade devices by increasing the contact resistance. In the past, attempts have been made to remove these polymers by exposing them to ozone sources,[1] oxygen plasmas,[2] hydrogen plasmas,[3] and fluorinated plasmas.[4] In this study, we subjected wafers that were exposed to an oxide etch process to five different "soft" etch cleanings, (ie., fluorine based chemistries) to assess the effectiveness of these different cleans on the removal of the polymer layer. In addition to removing the polymer, these fluorine based cleans were designed to remove etch-induced damaged silicon as well. Silicon lattice damage is a negative attribute of contact etching.[5,6] Since the surface condition of the silicon maybe roughened from the cleaning, a slow, controllable etch rate of the silicon is important.

EXPERIMENTAL PROCEDURE

In this experiment, we exposed a set of bare p type <100> orientation silicon wafers to the same oxide overetch conditions in an oxide etch reactor using a split powered diode. The etch conditions were 700 W, 550 mT, 22 sccm of CHF_3, 22 sccm of CF_4, and 200 sccm of Ar at a temperature of 40 °C for 26 seconds. The wafers were split into five sub-sets and were subjected to different cleaning environments after etching. The first three sub-sets were cleaned in-situ directly following the overetch

process at 50 W and 800 mT. The first sub-set saw a gas chemistry of 20 sccm of SF_6 and 400 sccm of Ar. The second sub-set saw a chemistry of 60 sccm of SF_6 and 80 sccm of O_2. The third in-situ cleaned sub-set saw a chemistry of 80 sccm of CF_4. The forth and fifth sub-sets of wafers were cleaned in separate reactors installed at the exit load lock of the etch system. One of these was an isotropic downstream strip module (ISO) and the other was an inductively coupled plasma strip module (ICP). The cleaning conditions for the ISO system were 300 W, 1700 mT, 300 sccm of NF_3, and 500 sccm of He at 50 °C. The conditions used in the ICP system were 300 W, 750 mT, and 50 sccm of CF_4 at 80 °C. Table I shows the process conditions for the overetch and five post-etch cleans.

Table I. Process conditions for etching and post-etch cleaning.

	Power (Watts)	Pressure (mTorr)	Gas Flow (sccm)	Time (seconds)	Temp. (Celsius)
Overetch	700 W	550 mT	CHF_3 22 sccm CF_4 22 sccm Ar 200 sccm	26	40 °C
in-situ SF_6/Ar	50 W	800 mT	SF_6 20 sccm Ar 400 sccm	39	40 °C
in-situ SF_6/O2	50 W	800 mT	SF_6 60 sccm O_2 80 sccm	41	40 °C
in-situ CF_4	50 W	800 mT	CF_4 80 sccm	33	40 °C
ISO NF_3/He	300 W	1700 mT	NF_3 300 sccm He 500 sccm	148	50 °C
ICP CF_4	300 W	750 mT	CF_4 50 sccm	117	80 °C

For our evaluation of the five cleaning conditions, we employed X-ray photoelectron spectroscopy (XPS), single wavelength ellipsometry, thermal wave modulated reflectance (TW), and Schottky barrier current-voltage (I-V) measurements to determine the condition of the silicon surface of wafers that were etched and wafers that were etched and cleaned by one of the five cleaning conditions. XPS was used to determine the composition and thickness of any films present after etching or after etching and cleaning. Single wavelength ellipsometry was used to determine polymer thicknesses greater than 50 Å which is the limit of our XPS analysis. TW has been used in the past to monitor reactive ion etching damage[7] and we have used it to monitor damage to the silicon substrate after the etch and after the post-etch cleans. IV measurements were used to determine the resistivity of any remaining polymers or oxides. In addition, correlations between these four independent characterization techniques were examined.

EXPERIMENTAL RESULTS

X-ray photoelectron spectroscopy measurements were taken on one wafer from each of the five sub-sets described above along with an etched wafer that did not see any post-etch cleaning and a control wafer-one that did not see any processing at all. Table II shows the elemental percentages and thicknesses extracted from our XPS

analysis of any polymers and oxides present before and after cleaning. Here, a noticeable difference in polymer thickness is observed between wafers cleaned in-situ and wafers cleaned in a secondary reactor. The wafers cleaned in-situ appear to have minimal polymer thicknesses (<10 Å) whereas wafers cleaned in either of the two separate reactors had polymer thicknesses of >50 Å. We feel that the reason for the thicker remaining polymers for these two separate reactors was due to insufficient processing times rather than a lack of performance by these tools. However, this remains to be verified. We note that, since these tools were installed at the exit load lock of the etch tool, samples cleaned using these cleaning approaches were not exposed to the ambient. Ellipsometry measurements taken on the etched sample showed a polymer thickness of ~112 Å. Similarly, samples cleaned in the ICP reactor after etching had a remaining polymer thickness of ~56 Å and samples cleaned in the ISO reactor after etching had a remaining thickness of ~65 Å.

Table II. Elemental percentages and oxide and polymer thicknesses for etched and etched then cleaned samples.

	Si %	O %	C %	F %	SiO_2 (Å)	CF_x (Å)
Control	70.8	24.8	4.0	0.4	10	0
Etched	1.3	1.6	33.9	62.9	?	> 50
SF_6/Ar	58.9	36.5	3.2	1.4	16	0
SF_6/O_2	59.0	36.9	3.5	0.5	17	0
CF_4	60.3	20.7	9.6	9.4	11	9
ISO	19.6	8.5	28.4	43.5	?	> 50
ICP	19.0	10.4	29.5	41.2	?	> 50

We targeted a total removal of 350 Å of polymer and silicon for each cleaning chemistry. The object was to ensure that all of the polymer would be etched as well as some of the silicon damaged during the oxide etch. The in-situ cleans had times of 39 seconds for the SF_6/Ar, 41 seconds for the, SF_6/O_2 and 33 seconds for the CF_4. A cleaning time of 148 seconds was used for the ISO system and a cleaning time of 117 seconds was used for the ICP system. These times are listed in Table I with the other cleaning parameters.

For the in-situ cleans, there were small variations of elemental percentages on the surfaces of wafers between the SF_6/Ar and SF_6/O_2 cases and a large variation between these two cases and the CF_4 case. The two SF_6 cases showed approximately the same percentages of elemental contents. The CF_4 case shows approximately the same percent of silicon (~60%) as the other two in-situ cases but it differs greatly in oxygen percent (20.7% compared to ~37%), carbon percent (9.6% compared to ~3.5%), and fluorine percent (9.4% compared to ~1.0%) present. These surface layer components were interpreted as being in the remaining ~9 Å polymer layer for the case of CF_4 whereas the remaining surface components for the SF_6 based cases must be on the surface since there is no detectable remaining polymer layer. The remaining polymer from the CF_4 case maybe the result of the cleaning chemistry depositing its own residue instead of an insufficient clean. Oxide thicknesses for these in-situ cases were 16 Å for the SF_6/Ar case, 17 Å for the SF_6/O_2 case, and 11 Å for the CF_4 case. We believe that the oxides found on the in-situ samples were native oxides that formed on the silicon between the time of cleaning and the time of XPS analysis. The XPS

analysis was performed on the wafers after they were removed from the vacuum chamber. The ISO clean left behind a relatively thick polymer layer were the thickness could not be measured by XPS. Using ellipsometry it measured 65 Å in thickness. The elemental percentages in this layer were oxygen 10.4 %, carbon 29.5 %, and fluorine 41.2 %. The ICP clean left a similar polymer layer of ~56 Å as measured by ellipsometry consisting of 8.5 % oxygen, 28.4 % carbon, and 43.5 % fluorine according to XPS.

Thermal wave modulated reflectance (TW) measurements were taken on wafers from each of the five sub-sets. TW measures silicon lattice damage by employing a pulsed argon ion laser and a steady state helium neon laser which monitors the decay of the reflectance changes caused by the argon laser. Thermal wave analysis produces two values from the measurement: an initial value and a decay value. Low thermal wave values indicate minimal damage and large thermal wave values indicate heavier damage.[8] Oxides and polymers present on silicon surfaces are compensated for in the thermal wave analysis. Our control wafer had initial and decay values of 37.3 and 32.6 (37.3/32.6), respectively, and our etched wafer had corresponding values of 886.9/552.7. The control values are typical of those reported for unprocessed bare silicon[9] and the etched values are typical of what we have seen in the past and what others have reported for etched Si surfaces.[7] After cleaning the three in-situ cases had initial and decay values of 264.1/116.5 for the SF_6/Ar case, 97.5/66.7 for the SF_6/O_2 case, and 498.0/309.2 for the CF_4 case. We note that there are significant differences between the TW values for the two SF_6 cleans even though their remaining polymer layers are very similar in composition and thickness. The wafers cleaned in the ISO and ICP systems showed the lowest sets of initial/decay values (56.7/50.1 for the ISO and 98.4/60.5 for the ICP) among the five cleaned sets. These cleans, however, allowed the largest polymer layers to remain. These thermal wave data are shown in Table III.

Table III. Thermal wave values for etched and etched then cleaned samples.

	Initial Value	Decay Value
Control	37.3	32.6
Etched	886.9	552.7
SF_6/Ar	264.1	116.5
SF_6/O_2	97.5	66.7
CF_4	498.0	309.2
ISO	56.7	50.1
ICP	98.4	60.5

Schottky barrier current-voltage measurements were taken on wafers from each set to determine the contact resistivity of the silicon surfaces. Typical forward bias currents from 0 to -4 V are plotted for each sub-set in Fig. I. The forward bias current of a Schottky diode has two regions where different mechanisms control the amount of current flow. Ideally below ~0.5 V forward bias, the current is dominated by the Schottky diode thermionic emission current.[10] Above ~1 V forward bias, the series resistance of the silicon substrate eventually dominates the current. Differences in the amount of current on our etched and cleaned samples above ~1 V forward bias indicate the effects of the resistivity of any polymer layer present. At 4 V forward bias in Fig. 1, the etched sample shows the highest resistivity (lowest current) followed by the ICP

and ISO processed samples. The three in-situ cleaned samples show the least amount of resistance and the SF_6/O_2 and CF_4 samples are the closest to the control value. The SF_6/Ar sample shows different diode current-voltage characteristics than the other processed samples; i.e., the slope of the curve at ~-0.2 V is lower than the others. We attribute this difference to damage introduced during the SF_6/Ar cleaning. We believe that this SF_6/Ar clean contributed damage to the Si substrate as it etched away at least some of the polymer layer caused by the oxide overetch. The presence of argon in plasmas, which is the situation in this SF_6/Ar clean, has been implicated in situations of increased damage in other studies.[11]

CONCLUSIONS

XPS and ellipsometry results showed that both the ISO and ICP cleaning steps failed to remove most of the polymer present after etching whereas the three in-situ cleans were successful. However, thermal wave measurements showed that the ISO and ICP cleans resulted in having lower initial and decay values than did the three in-situ cleans. This result certainly casts doubt on thermal wave's ability to monitor the status of silicon lattice damage after etching. This doubt occurs because the ISO and ICP values should be the same as the etched sample's values since the silicon surface was not exposed to the soft etch. In the TW characterization of the cases of the in-situ cleans using SF_6/O_2 and CF_4 chemistries, the SF_6/O_2 had lower initial and decay thermal wave values than the CF_4 case; hence, the thermal wave correlates with the XPS results in this case. The SF_6/O_2 case also has less carbon and fluorine present than the CF_4 case. The SF6/Ar case compares well to the SF_6/O_2 case in polymer composition and thickness but the SF_6/Ar cleaning procedure damaged the silicon surface. The result of this, in terms of thermal wave values, is that they lie midway between the SF_6/O_2 and CF_4 values for the SF_6/Ar clean yet the reason for their being larger than the SF_6/O_2 values is Si lattice damage caused by Ar. This, of course, is not the reason for the large TW values for the CF_4 clean. The forward bias currents for the Schottky barriers used to characterize the other cleans correlated to the XPS results for remaining polymer thicknesses indicating that the forward I-V's were sensitive to the remaining polymer. For the samples with the thickest amount of polymer present (ISO and ICP), the forward bias currents were the lowest and close to the etched sample. For the samples with the least amount of polymer present (in-situ SF_6/O_2 and in-situ CF_4), the forward bias currents were two decades higher than the forward bias current of the etched sample and were close to the current of the control sample. However, the forward I-V for the Schottky barriers used to characterize the SF_6/Ar clean did not correlate with polymer thickness. The reason for this is the Ar damage to the Si surface.

In summary, the in-situ SF_6/O_2 clean performed the best out of the five cleaning conditions that we examined. The in-situ CF_4 was second with higher concentrations of carbon and fluorine present and higher resistivity as seen in the forward bias current compared to the SF_6/O_2 case. The two secondary reactor cleans (ISO and ICP) were not run long enough to remove all of the polymer present as both left over 50 Å of polymer on the silicon surface. The in-situ SF_6/Ar clean removed all of the polymer present but introduced damage to the silicon surface. In terms of characterization it was seen that Schottky barriers I-V's can be used to detect remaining polymer after cleans if one does not want to use XPS or need the detail it affords. TW results are affected by the presence of polymers and can give a fallacious assessment of cleaning and damage removal.

REFERENCES

(a) On assignment from AMD, Austin, TX.
1. H. Norstrom, et al., J. Electrochem. Soc., Vol. 132, 228, (1985).
2. K. Reinhardt, et al., Mat. Res. Soc. Symp. Proc. (1993).
3. J. P. Simko and G. S. Oehrlein, J. Electrochem. Soc., Vol. 138, No. 1, 277, January (1991).
4. K. Shenai, et al., Proceeding of the 7th Symposium on Plasma Processing, Electrochem. Soc., Vol. 88-22, 179, (1988).
5. S.J. Fonash, Solid State Technology, Vol. 28, no. 4, 201, (1985)
6. G.S. Oehrlien, et al., J. Electrochem. Soc., Vol. 132, no. 6, 1441, (1985).
7. P. Geraghty and W. L. Smith, Mat. Res. Soc. Symp. Proc. Vol. 68. , 387, (1986).
8. W. L. Smith and A. Rosencwaig, Bull. Amer. Phys., Soc. 31, 273, (1986).
9. W. L. Smith, et al., Solid State Tech., 85, January, (1986).
10. J. F. Rembetski, et al., J.J.A.P. Vol. 32, Part 1, 6B, June (1993).
11. K. Reinhardt and F. Duneani, SPIE, Dry Etch Technology, 1593, 32, (1991).

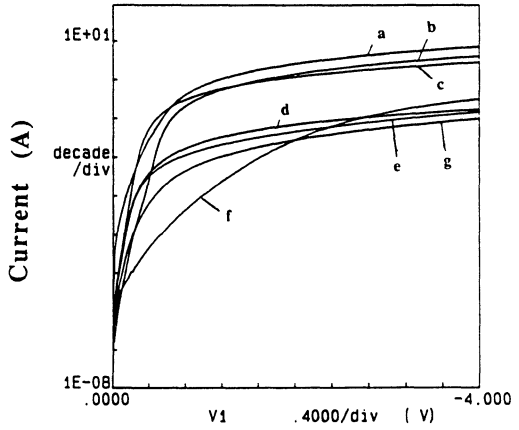


Figure I. Forward bias current for the (a) control, (b) SF_6/O_2, (c) CF_4, (d) ISO, (e) ICP, (f) SF_6/Ar, and (g) etched samples.

REDUCTION OF IN SITU PARTICLE FORMATION DURING CONTACT AND VIA ETCH PROCESSES ON DOWNSTREAM OXIDE ETCHERS

Jeff Martsching, Jackie Amthor, and Karl Mautz
Motorola, Inc., Semiconductor Products Sector
3501 Ed Bluestein Blvd., B-1
Austin, Texas 78762

Downstream oxide etchers are prone to polymer formation and buildup from plasma byproducts. These polymers cause particle failures and lower device yields. Plasma clean and *in situ* descum processes were used to remove polymer deposits and prevent particle problems. The plasma clean process was not as effective in preventing defectivity. The *in situ* descum process was found to reduce particles, increase the number of wafers that could run before wet cleaning, and improve device yield and parametrics.

INTRODUCTION

Downstream oxide etchers used to create contact and via openings, are prone to polymer buildup due to plasma byproducts resulting from the etch process. Over a period of plasma time, the polymer formations grow to the point that separation from the chamber surfaces occurs. This resultant flaking causes catastrophic particle failures and device yield loss due to defects blocking these openings on the wafers. Chamber disassembly and cleaning (wet cleans) were required at intervals of 1250 wafers run, to prevent this phenomena from occurring. These wet cleans were responsible for approximately 60% of the equipment downtime per month. Plasma cleans were investigated to prevent this problem. *In situ* descum steps were tested to remove polymer deposits and other defectivity from the wafer surface before the oxide etch step.

EXPERIMENTATION

The tool was a downstream, isotropic oxide etcher using a NF_3/He chemistry (baseline etch process), with O_2 used as the gas in the descum step (1). The chamber consists of three key components that are inspected and cleaned during the wet clean: *i)* the ceramic ring, *ii)* the upper and lower grounding grids, and *iii)* the upper electrode with the dispersion plate. Microscopic inspection was used to examine and photograph the chamber parts under magnification, and to determine both the degree of polymerization as a function of plasma time and the effectiveness of the plasma clean trials. Polymer was removed from the chamber surfaces, and analyzed using an energy dispersive X-ray spectrometer (EDS). Particle data (0.5-5.0 microns) were taken to test the effectiveness of the processes using a Tencor 4500 Surfscan.

Various aggressive plasma clean steps using ash-type chemistries were tried at designated intervals between product runs. The *in situ* descum step tested consisted of a fairly mild chemistry in regards to photoresist removal (different O_2 gas ratio, low-medium rf power, medium pressure, and 10-15 second step time) in comparison to the clean processes. Characterization of these processes were done using Taguchi experimental designs (2, 3). Following this characterization, a system was dedicated to run only the *in situ* descum process (consisting of the *in situ* descum step prior to the baseline etch process) to determine the effect on particles and device yield, in comparison to the baseline-only process.

RESULTS AND DISCUSSION

The dispersion plate has 12 concentric gas inlets, or slits as shown in Figure 1. Using microscopic inspection of the parts, it was discovered that the slits in the dispersion plate were the area in the chamber most prone to polymer deposits. The polymer buildup occurred as a function of plasma time (4). This led to chamber contamination from polymer flaking that resulted in higher particle levels (greater than 50 add-ons) on wafers and contributed to device yield loss, due to blocked or partially open vias and contacts (5). Analysis of the polymer showed its composition to be mostly fluorine and carbon with some other minor components, such as silicon and aluminum (chamber material). Figure 2 displays the polymer analysis EDS spectra.

Characterization of the clean processes was done using photoresist loss (as a model of polymer) as an output. These tests were run using O_2 as the primary gas, varying the flow, pressure, and rf power to maximize the resist removal, with run times up to 30 minutes. Dedicated clean processes using these aggressive ash-type chemistries (6000Å/minute resist removal rate), done at periodic intervals between product wafer runs (1250 wafers-when wet cleans were required), did not consistently remove the polymer buildup on the dispersion plate. However, particle data showed a slight improvement using the plasma clean, particularly those counts taken directly after the clean was run. Although wafer runs could be extended beyond 1500 and up to 2200 before particle failure, the plasma clean was not implemented at this point, due to poor repeatability. Microscopic examination of the dispersion plate slits, coupled with "pre" and "post" photographs were also used to judge the effectiveness of the plasma cleans. While disturbance of the polymer was observed after the plasma clean processes, undesirable side effects (in the form of chamber arcing) occurred (7). Using the most aggressive plasma clean recipe, complete polymer removal was not obtainable. It was concluded then, that the plasma clean was largely ineffective, at least when done at the standard interval (at 1250 wafers).

Characterization of the *in situ* descum step was done with resist removal as an output. Various descum step processes were tested with differing targeted resist thickness removal (from 300 to 1200Å removed). The descum step used was an 800Å resist removal process, and was used *in situ* before the baseline etch process. Two distinct recipe groups were then run on the etcher, one of which had the *in situ* descum step, and the other with the baseline-only process. As a comparison, tests were run on the baseline process with the descum step done in a separate, dedicated tool. Particle levels on wafers increased with the separate descum tool process, and were lower using

the *in situ* descum step. The difference in polymer buildup on the dispersion plate between the baseline and *in situ* descum process was compared during inspections, with two separate sets of chamber parts being examined. Microscopic examination of the dispersion plate slits displayed a significant difference in polymer formation, clearly favoring the *in situ* descum process. In fact, after 1250 wafer runs with the system running predominantly the *in situ* descum process, the dispersion plate virtually matched the physical appearance of a freshly wet cleaned plate. The absence of large polymer formations precluded the need for separate plasma cleans. In effect, the *in situ* descum is an attenuated plasma-clean, whose superior performance may be explained as a result of the frequency, rather than recipe aggressiveness. The polymer was systematically etched away, before it ever had a chance to accumulate. The *in situ* descum step therefore eliminated the need for the plasma clean processes.

Tests were also run with various ratios of the two oxide etch processes (*in situ* descum and baseline). These tests compared particle data between several etchers, taking into account the type of recipe run, over a specific number of wafers. A particle count was conducted every 250 wafers. At 25 wafers per lot, this represented 10 product lots run. Each product lot ran either the *in situ* descum recipe, or the baseline recipe. Figure 4 displays the particle data from the oxide etch process ratios. Particle counts were then recorded, and correlated to the ratio of one recipe to another (7-3, 9-1, 5-5, etc.). As these tests were done in a production environment, a substantial amount of data was able to be collected to support the validity of the results. The findings showed that when the *in situ* descum recipe was run at a ratio of 10/0, 9/1, and 8/2, particle counts ranged from single digits to a maximum of 20. As the ratio declined, from 7/3 to 5/5, counts were still acceptable, numbering mostly in the teens with none higher than 30. As the ratio declined even further, and the baseline process was more predominantly run, particle counts ranged from 40 to 70, with some approaching 100 when the 0/10 ratio was encountered.

During confirmation testing using the *in situ* descum recipe exclusively, over 5000 wafers could be run before failing for particles and requiring a wet clean, and the average particle count during the cycle (tested after every 50 wafers) was reduced by 3X. Device yield improvement, directly related to the reduced particle levels blocking vias and contact openings, was improved by 10-15%. Parametrics related to contacts and vias were on target and made more stable. The effect of the *in situ* descum processes on the contact and via profiles was measured using SEM micrograph analysis. This data showed that the effect on the profile was minimal, with the *in situ* descum process slightly improving the metal step coverage. The overall equipment uptime of the downstream oxide etcher improved by 10%, due to the decrease in the number of wet cleans that were required.

The defectivity, device yield and equipment uptime data proved the *in situ* descum process was superior to the baseline-only process. The *in situ* descum step has been incorporated into each baseline process as an initial step. The baseline processes vary in length of step time only (long and short), and the incorporation of the *in situ* descum step increased the number of wafers run before particle failure from 1250 to either 2500 or 5000, depending on the baseline process. The yield increase and particle reduction has been consistent as each system was converted to the *in situ* descum process recipes.

Future investigations to decrease the overall downstream oxide etch process defectivity will be done using the main etch step gas flow ratios, temperature and total gas flow factors, along with testing of an rf ramp process on the wafer particle levels. This will be done in conjunction with, and tested against the *in situ* descum process. Initial screening experiments demonstrated some improvement with changes in these process factors.

CONCLUSION

Inspection of the downstream oxide etcher chamber parts identified the dispersion plate slits as the area most affected by polymer build-up due to plasma reaction byproducts. The various clean processes done periodically during the wafer runs were ineffective in removing this polymer formation and preventing particle problems. An *in situ* descum process introduced as an initial step of the baseline etch process was found to prevent this polymer from building up, reduce the particle levels, and increase the device yield. This process extended the amount of plasma time (or wafers run) in the etcher before requiring wet cleaning, improving the equipment uptime.

REFERENCES

1) J. Booth, G. Hancock, and N. Perry, *Appl. Phys. Lett.*, **50**, 318 (1987).
2) G. Taguchi, "System of Experimental Design," Unipub/Kraus International Publications, New York (1987).
3) M. Phadke, "Quality Engineering Using Robust Design," Prentice Hall, New Jersey (1989).
4) J. O'Neill, J. Singh, and G. Gilford, *J. Vac. Sci. Technol.*, **A8**, 1716 (1990).
5) G. Selwyn, J. Singh, and R. Bennett, *J. Vac. Sci. Technol.*, **A7**, 2758 (1989).
6) B. Chapman, "Glow Discharge Processes," Wiley-Interscience, New York (1980).
7) A. Nagy and D. Hess, *J. Electrochem. Soc.*, **129**, 2530 (1982).

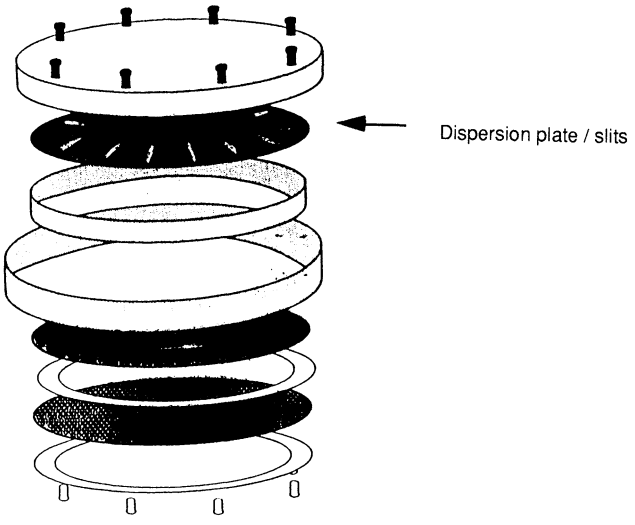


Fig. 1. Downstream oxide etcher chamber construction-exploded view.

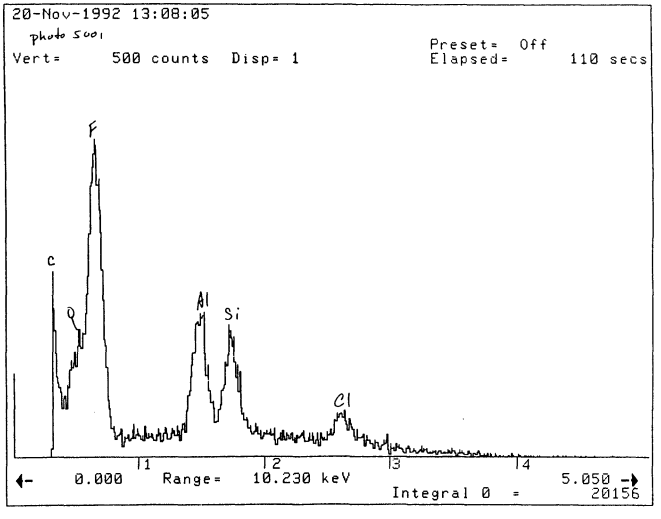


Fig. 2. Polymer analysis spectra using energy dispersive X ray spectroscopy.

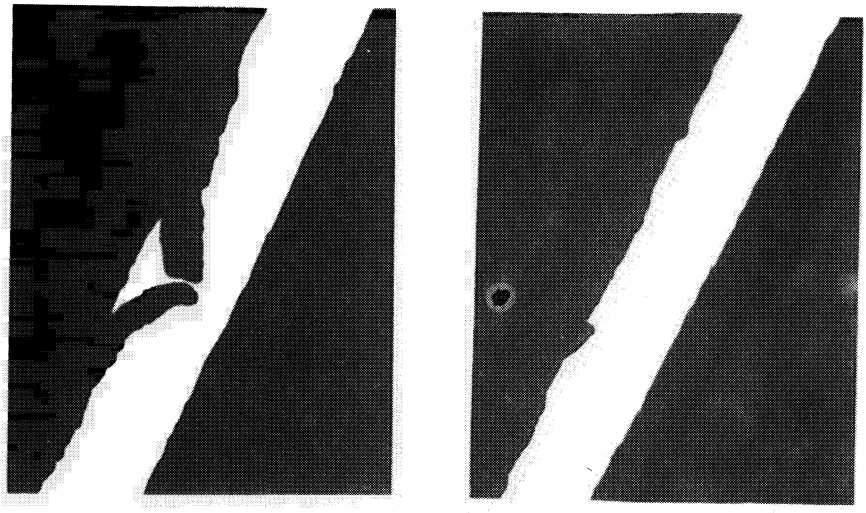


Fig. 3. Optical photographic comparison of polymer deposits from the downstream oxide etch processes. Left is the baseline process and right is the *in situ* descum process. The diagonal feature is the dispersion plate slit. The flaking polymer is visible in the center of the slit and is more prominent on the baseline process. Magnification is 25X.

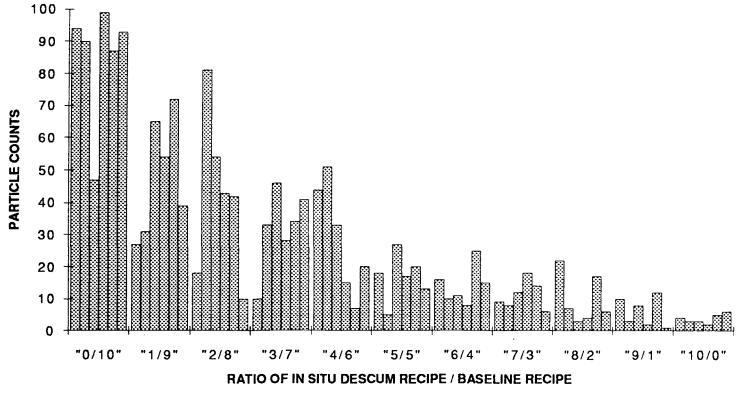


Fig. 4. Particle levels in the downstream oxide etcher due to running the *in situ* descum and baseline process at various ratios after 1250 wafers.

ECR Oxygen Plasma Cleaning of Oxide Etched Surfaces

P. I. Mikulan and S. J. Fonash

Electronic Materials and Processing Research Laboratory
The Pennsylvania State University
University Park, PA 16802

K. A. Reinhardt [a] and T. Ta [b]

SEMATECH, Austin, TX 78741

An electron cyclotron resonance oxygen plasma was employed to remove polymer layers on silicon substrates subjected to oxide etching and some comparison was undertaken with UV-ozone cleaning. Several gas chemistries were used in the oxide etching and each resulted in the formation of different polymer layer thicknesses and compositions. X-ray photoelectron spectroscopy was used to establish this and to determine the thickness and composition of these polymer layers before and after ECR exposure. Schottky barrier current-voltage analysis was also used to monitor the contact resistance of the substrate surfaces before and after the ECR oxygen plasma treatment.

INTRODUCTION

Contact etching using fluorine based chemistries has many advantages such as high etch rates and selectivity between SiO_2 and Si. Chemistries such as CHF_3 and CF_4 have been used extensively[1,2] and there is increasing interest in C_2F_6 based chemistries as well.[3,4] One major drawback to using these chemistries is the formation of fluorocarbon polymers. Although they contribute to the high selectivity by passivating the silicon surface,[5] these polymers, if left on the surface, increase the contact resistance seen in devices.

EXPERIMENTAL PROCEDURE

In this study, we used electron cyclotron resonance plasmas to effectively remove polymer layers formed on silicon after endpoint during oxide etches. We looked at several residue polymer layers that were formed by different etching gas chemistries in several different reactor models. The reactors included a reactive ion etcher (RIE), a magnetically enhanced reactive ion etcher (MERIE), an oxide etch

system (OE), and two high density plasma systems (HD). In the RIE system we used a CHF_3 chemistry. In the MERIE system, we used three different gas chemistries; CHF_3/O_2, CHF_3/Ar, or CHF_3/CF_4/Ar. In the OE system, we used CHF_3/CF_4/Ar. In the first HD system(HD I), we used C_2F_6 or CF_3/CO. In the second HD system (HD II), we employed a CHF_3/CF_4/Ar chemistry. These etching chemistries left behind different polymers on the silicon surface; we then used an oxygen plasma in an ECR chamber to remove these polymers.

Our ECR processing parameters were 400 watts and 0.4 mTorr for 20 minutes. The temperature was not controlled but increased from room temperature to not more than 120 °C in the twenty minute processing time.

In carrying out this experiment, ellipsometry, XPS, and Schottky barrier current-voltage measurements were taken after each of the processing steps of etching, ECR oxygen cleaning, and post-cleaning buffered oxide etching with H_2O:HF in a 4:1 solution. The objective was to monitor the changes in thickness and composition of the films present on the silicon substrate after the different processing steps.

The ellipsometry measurements were performed using a Rudolph Research Auto-EL ellipsometer. XPS analysis was done with a Kratus XSAM 800 pci system at a pressure of $2x10^{-9}$ Torr.. Schottky barrier I-V analysis was performed by fabricating diodes on samples directly after oxide etch, on samples after etch and ECR oxygen clean, and on samples after etch, clean, and subsequent HF etch. The diodes were fabricated by thermally evaporating titanium dots at a pressure below 10^{-7} Torr. Shallow masks were used to define these structures and the diodes' area was 1 $mm.^2$

EXPERIMENTAL RESULTS AND DISCUSSION

Film thicknesses and compositions- For the RIE system and CHF_3 chemistry, the polymer thickness after etching was found to be 78 Å for the etch conditions listed in Table I. The composition of the fluorocarbon layer was 58.5 % C, 23.7 % F, 13.0 % O, and 4.8 % Si and the spectra is shown in Fig. 1a. After the ECR oxygen cleaning, the film thickness decreased from 78 Å to 22 Å and the composition of this film changed from a polymer (high carbon and fluorine content) to an oxide (high oxygen content). The composition of this "oxidized polymer" was 17.1 % C, 0.1 % F, 50.0 % O, and 32.8 % Si. The XPS spectra for the ECR oxygen cleaned sample is shown in Fig. 1b. Samples from this system that received a post-clean HF etch show no detectable film to be present on the silicon surface. The spectrum for the HF etched sample is shown in Fig. 1c. The changes in the thickness and elemental percentages after the three processing steps for the RIE system are summarized in Table IIa, b, and c.

Three different chemistries were used in the MERIE system: CHF_3/CF_4/Ar, CHF_3/Ar, and CHF_3/O_2. The etch conditions are listed in Table I. For the case of the CHF_3/CF_4/Ar chemistry, the polymer thickness (after etching) was found to be 66 Å with a composition of 49.9 % C, 32.6 % F, 10.5 % O, and 7.0 % Si. After the ECR clean, the thickness was reduced to 28 Å with a composition of 22.3 % C, 1.7 % F, 46.1 % O, and 30.0 % Si. As in the RIE case, the film was converted from a polymer to oxide by the ECR oxygen exposure. After an HF etch, there appeared to be no film left (<5 Å) on the silicon surface. These XPS results are summarized in Table IIa, b,

and c. For the CHF_3/Ar chemistry in the MERIE system, the thicknesses were 89 Å after etch, 40 Å after clean, and less than 5 Å after HF etch. For the CHF_3/O_2 chemistry, the film thickness was 59Å after etch, 20 Å after oxygen clean, and less than 5 Å after an HF etch.

For the oxide etch system, the gas chemistry of CHF3/CF4/Ar was used with the process parameters listed in Table I. After etching, the fluorocarbon layer had a thickness of 52 Å. After the ECR clean, the thickness was found to be 27 Å. After the HF etch, there was no detectable film left on the silicon surface.

For the first HD system (HD I), with the gas chemistry of C_2F_6, the polymer layer after etching had a thickness of 43 Å and composition of 36.9 % C, 8.6 % F, 29.8 % O, and 24.7 % Si. After the samples were subjected to the ECR cleaning, the thickness layer was reduced to 35 Å and its composition was 20.5 % C, 0.7 %F, 47.1 % O, and 31.7 % Si. After an HF etch, the film thickness was under 5 Å. These XPS results are summarized in Table IIa, b, and c. For the same system but using a CHF_3/CO chemistry, the polymer layer thickness after etching was 37 Å. After the ECR cleaning, the thickness was reduced to 23 Å. With a subsequent HF etch, the film thickness was reduced to under 5 Å.

For the second HD system (HD II), a gas chemistry of CHF_3/CF_4/Ar was used and the process conditions are listed in Table I. The polymer layer resulting from the etching had a thickness of 75 Å with a composition of 52.3 % C, 29.8 % F, 12.3 % O, and 5.6 % Si. After the ECR cleaning, the thickness was reduced to 26 Å and its composition was 22.5 % C, 0.7 % F, 45.8 % O, and 31.1 % Si. After the HF etching, the film thickness was under 5 Å. The XPS results are summarized in Table IIa, b, and c.

Table I. Process Conditions for the Different Etch Systems and Gas Chemistries.

	Gas Chemistry (sccm)		Power (Watts)	Pressure (mTorr)	B-field (Gauss)
RIE System	CHF3	50	1000	50	
MERIE System	CHF3	100	550	100	80
	O2	3			
	CHF3	26	400	75	0
	Ar	79			
	CHF3	121	1250	200	20
	CF4	24			
	Ar	121			
Oxide Etch	CHF3	22	500	300	
	CF4	22			
	Ar	300			
High Density I	C2F6	30	1500	30	
	CHF3/CO	90	500	20	
High Density II	CHF3	20	1300	325	
	CF4	20			
	Ar	150			

Table IIa. Composition and Thickness of Films after Etching.

	Gas Chemistry	% C	% F	% O	% Si	Thickness
RIE System	CHF_3	58.5	23.7	13.0	4.8	78 A
MERIE System	$CHF_3/CF_4/Ar$	49.9	32.6	10.5	7.0	66A
High Density I	C_2F_6	36.9	8.6	29.8	24.7	43 A
High Density II	$CHF_3/CF_4/Ar$	52.3	29.8	12.3	5.6	75 A

Table IIb. Composition and Thickness of Films after ECR Cleaning.

	Gas Chemistry	% C	% F	% O	% Si	Thickness
RIE System	CHF_3	17.1	0.1	50.0	32.8	22 A
MERIE System	$CHF_3/CF_4/Ar$	22.3	1.7	46.1	30.0	28 A
High Density I	C_2F_6	20.5	0.7	47.1	31.7	35 A
High Density II	$CHF_3/CF_4/Ar$	22.5	0.7	45.8	31.1	26 A

Table IIc. Composition and Thickness of Films after HF Etching.

	Gas Chemistry	% C	% F	% O	% Si	Thickness
RIE System	CHF_3	17.0	0	33.2	49.8	< 5 A
MERIE System	$CHF_3/CF_4/Ar$	13.4	0.7	27.4	58.5	< 5 A
High Density I	C_2F_6	12.7	0	25.1	62.1	< 5 A
High Density II	$CHF_3/CF_4/Ar$	19.9	1.0	29.4	49.7	< 5 A

Schottky Barrier Current-Voltage Characteristics- Schottky barriers were fabricated on samples from each set after etching, after ECR cleaning, and after HF etching to monitor the contact resistance of the wafers' surfaces. In each case, the etched samples had the highest resistivity compared to their respective cleaned samples. In addition, the HF etched samples had even lower resistivities than the ECR cleaned samples and in some cases the resistivity was comparable to the respective control. Here we define a control to be an unprocessed wafer from the same lot.

In Figure 2, the forward currents of diodes fabricated on the etched, ECR cleaned, and HF etched samples are displayed for the RIE CHF_3 case. Here we show that the lowest current (highest resistance) belongs to the etched sample followed by the ECR cleaned sample. The sample which received an HF etch after the ECR cleaning showed the best I-V characteristics compared to the control. To correlate to film thickness, we note that the etched sample had the thickest film (78 Å) and highest resistance followed by the ECR cleaned sample (28 Å) and the HF etched sample (>5 Å).

In Figure 3, we see that the MERIE $CHF_3/CF_4/Ar$ case shows the same trend as the RIE case where the etched sample shows the highest resistance followed by the ECR cleaned sample. This is also true for the MERIE CHF_3/Ar and CHF_3/O_2 cases as well. In general, we saw an improvement in contact resistance after our ECR oxygen clean for each case that we evaluated.

Based on these experimental results and previous models presented by this group,[6,7] we propose the following model of our ECR oxygen cleaned films. During silicon dioxide etching, specifically after end-point, a fluorocarbon residue forms on the silicon substrate as seen in Fig. 4a. This film acts as a protective layer increasing selectivity between SiO_2 and Si and can range in thickness from 30 to 120 Å.[5] When

these films are subjected to an ECR oxygen plasma, the composition changes from a fluorocarbon-rich film to an oxide layer and the thickness is decreased. This is due to the oxygen from the plasma reacting with the carbon in the film creating molecules of volatile CO_x and thereby reducing the total film thickness as seen in this study. In addition, the oxygen also bonds with the silicon within the film and at the surface of the substrate. All of this results in the picture seen in Fig. 4b. As seen in Fig. 4a and Fig. 4b, the SiO_2 etching damaged the silicon substrate leaving a heavily damaged silicon surface having many distorted Si bonds and a more lightly damaged region having only line and point defects. In the ECR oxygen treatment, some of the heavily damaged Si may have been oxidized. Finally, when the ECR plasma treated sample is subjected to an HF etch, the oxide formed during the plasma is removed leaving behind less than 10 Å of an impurity laden film. Based on previous studies, we believe that this remaining film is composed mainly of C-Si bonding.[3] As seen in Fig. 4c, the heavy damaged and light damaged Si layers remain under this film.

Comparison of ECR Oxygen Cleaning to UV-Ozone Cleaning- UV-ozone cleans were performed on wafers that saw the same etch conditions as some of those that were cleaned using the ECR oxygen plasma. The UV-ozone cleaning conditions were 1 slpm of O_2 for twenty minutes in a PR-100 UV-ozone Photoreactor system. In all cases, the ECR clean performed better than the UV-ozone clean. This was determined from thickness measurements and I-V characteristics performed on the cleaned samples. For example, when the total thickness of the etched sample was 75 Å, the UV-ozone cleaned sample had a thickness of 43 Å whereas the ECR cleaned sample had a thickness of 24 Å. Figure 5 shows the I-V curves for both an ECR cleaned sample and a UV-ozone cleaned sample along with the etched sample and control for the oxide etch (OE) $CHF_3/CF_4/Ar$ case. Here the ECR cleaned sample shows a higher current than the UV-ozone cleaned sample. In addition, an HF etch did not affect the I-V curve of the UV-ozone treated sample but did reduce the resistance of the ECR treated sample. This suggests that the UV-ozone treatment was not successful in completely oxidizing the polymer whereas our ECR plasma treatment was successful.

CONCLUSIONS

We have reported that our ECR oxygen plasma has successfully removed fluorocarbon films that form on Si during SiO_2 etching. These polymers that ranged in thickness from 30 to 80 Å and differed in composition depending on the etch tool and chemistry were removed by our oxygen plasma leaving behind a thinner oxide layer created during our ECR process. This oxide can be removed by a wet HF etch. In comparison to an UV-ozone treatment, the ECR oxygen plasma performed substantially better than the UV-ozone treatment in removing the polymer from the Si surface.

ACKNOWLEDGMENTS

The authors thank Dr. Temmel Buyuklimanli of The Pennsylvania State University for the XPS analysis.

REFERENCES

(a) On assignment from AMD, Austin, TX.
(b) On assignment from AT&T, Orlando, FL.
1. J. M. Heddleson, M. W. Horn, and S. J. Fonash, J. Electrochem. Soc., Vol. 137, No. 6, 1960, June (1990).
2. D. Misra and E. L. Heasell, Semicond. Sci. Technol., 5, 229, (1990).
3. K. Reinhardt, et al., Mat. Res. Soc. Symp. (1993).
4. H.-H. Park, et al., Mat. Res. Soc. Symp. Proc. Vol. 259, 219, (1992).
5. G. S. Oehrlein, et al., . Vac. Sci. Technol., A5, 1585, (1987).
6. S. J. Fonash, Solid State Tech., 28, 201, (1985).
7. S. J. Fonash, R. A. Ditizio, T. Gu, P. I. Mikulan, and O. O. Awadelkarim, Mat. Res. Soc. Symp. Proc. Vol. 259, (1992).

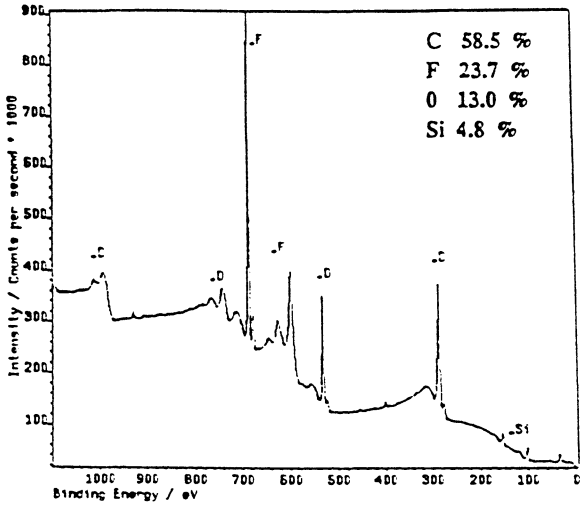


Figure 1(a). XPS results for the etched sample from the RIE reactor using CHF_3 chemistry.

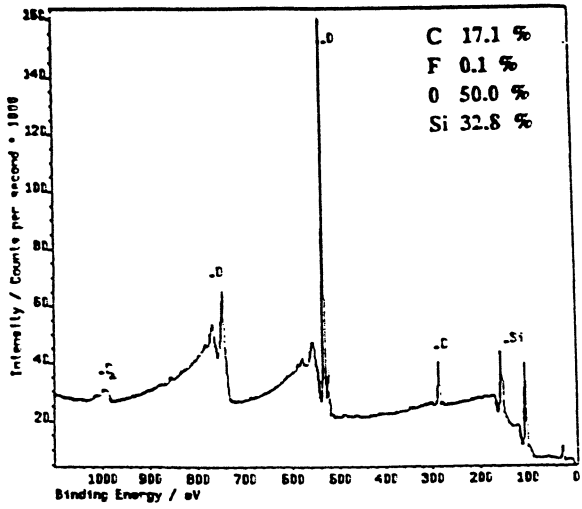


Figure 1(b). XPS results for the ECR oxygen cleaned sample from the RIE reactor using CHF_3 chemistry.

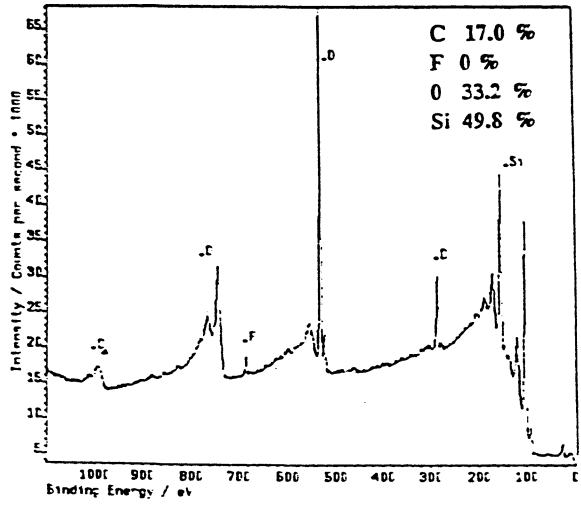


Figure 1(c). XPS results for the HF etched sample from the RIE reactor using CHF_3 chemistry.

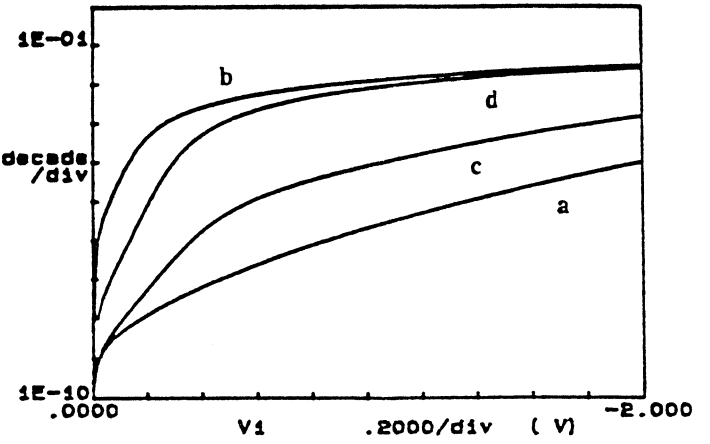


Figure 2. I-V curves for (a) an etched sample, (b) a control sample, (c) an etched and oxygen cleaned sample, (d) an etched, oxygen cleaned and HF etched sample for the RIE CHF_3 case.

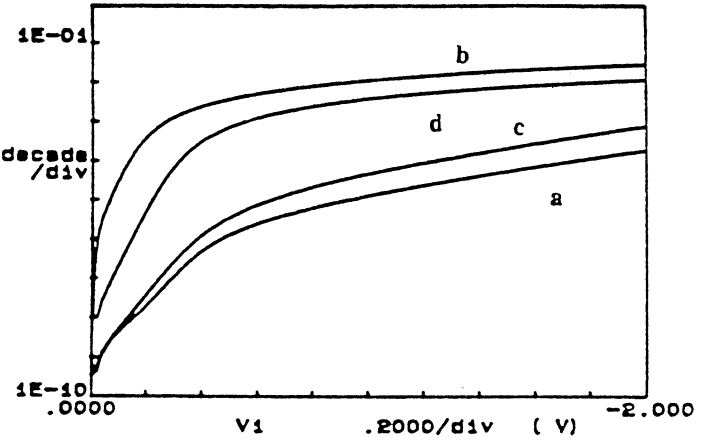


Figure 3. I-V curves for (a) an etched sample, (b) a control sample, (c) an etched and oxygen cleaned sample, (d) an etched, oxygen cleaned and HF etched sample for the MERIE $CHF_3/CF_4/Ar$ case.

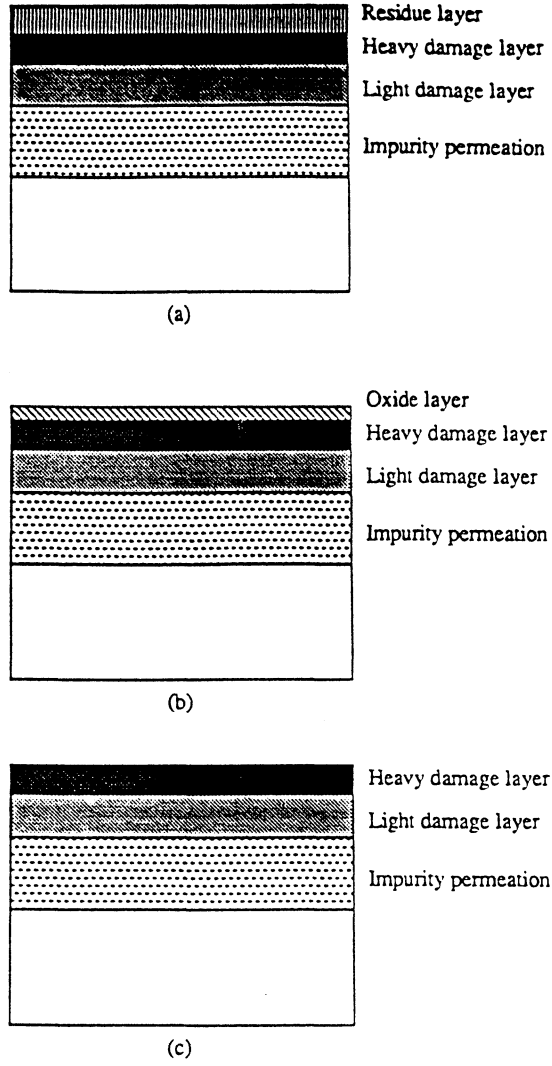


Figure 4. A model of the silicon substrate after (a) etching, (b) etching and ECR oxygen cleaning, and (c) etching, ECR cleaning and subsequent HF etching.

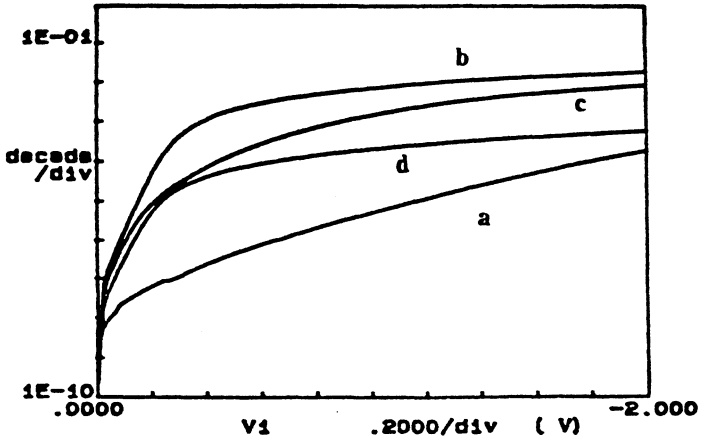


Figure 5. I-V curves for (a) an etched sample, (b) a control sample, (c) an etched and oxygen cleaned sample, and (d) an etched and UV-ozone cleaned sample for the OE CHF_3/CF_4/Ar case.

REDUCTION OF SURFACE ROUGHENING AND SUBSURFACE DEFECTS IN H-PLASMA CLEANING OF Si(100)

T.P. Schneider*, J.S. Montgomery*, H. Ying*, J.P. Barnak†, Y.L. Chen†, D.M. Maher†, and R.J. Nemanich*
*Department of Physics, Box 8202, North Carolina State University, Raleigh, NC 27695-8202
†Department of Materials Science and Engineering, Box 7907, North Carolina State University, Raleigh, NC 27695-7907

ABSTRACT

The development of surface roughness and subsurface defects during H-plasma exposure of Si (100) surfaces was investigated. The H-plasma was characterized with residual gas analysis (RGA) and a double Langmuir probe (DLP). RGA data was used to detect the etch products of the H-plasma and Si (100) surface interaction. The data indicates that the silane fragment SiH_2 decreases in signal intensity with increased sample temperature. The DLP data indicates that in the region above the Si surface the plasma density is ~ $2.5x10^8$ cm^{-3}. The Si surface is characterized with atomic force microscopy (AFM) and cross-sectional transmission electron microscopy (TEM). AFM data indicates that surface roughness is greater for samples processed at lower process temperatures. TEM micrographs indicate that the surface is (i) rough for 60 min and (ii) smooth for 1 min H-plasma exposures. The subsurface region is characterized with TEM and Raman spectroscopy. TEM micrographs indicate subsurface defects for 150°C, 60 min H-plasma exposures. The 450°C, 60 min H-plasma exposures lead to TEM micrographs with no observable subsurface defects. The Raman data indicates Si-H bonding at ~ 2100 cm^{-1} for 150°C, 60 min H-plasma processing. In contrast, 450°C, 1 min H-plasma exposures result in no detectable Si-H signal in the Raman spectra.

INTRODUCTION

H-plasma cleaning of Si (100) surfaces has been shown to be an effective *in situ* process for removal of carbon and oxygen after an *ex situ* wet cleaning step (1). Some of the aspects of H-plasma cleaning are (i) control of surface structure (1x1, 3x1, or 2x1) due to H induced reconstructions (2), and (ii) chemical passivation of the surface (3). For a short duration H-plasma exposure (< 2.0 min), the above two aspects depend on the process pressure and substrate temperature (T_S). In this study we extend the substrate temperature range, and the results presented here indicate that surface roughness and subsurface defect formation also depend on the exposure time and substrate temperature.

Previously Johnson *et. al.* (4) have shown that hydrogenation of n-type Si (100) for 60 min at 150°C results in the formation of {111} microcracks or H-stabilized platelets within 0.1 μm of the exposed surface. Furthermore, the hydrogenation of n-type Si (100) proceeds due to H-diffusion, and the defects are not related to plasma or radiation damage

(4). By applying the H-plasma in a remote mode, the concentration of ions reaching the surface is minimized. Thus, it is the stable neutral atomic species (*i.e.* atomic H) that react at the surface.

In this study plasma, surface, and subsurface characterizations are used to determine process conditions which reduce surface roughness and subsurface defects A discussion of the etching process and the relationship between subsurface H and subsurface defects is included.

EXPERIMENTAL

The samples used in this study were 25 mm diameter phosphorous doped Si (100) wafers with a resistivity of 0.8-1.2 Ω-cm and thickness of 20 mils. The *ex situ* surface preparation consisted of a 5.0 min uv-ozone exposure followed by a spin etch in 1:1:10::HF:H_2O:ethanol (5). Low energy electron diffraction (LEED) measurements indicate that the surface symmetry is 1x1 after the *ex situ* clean (2). The wafers were then exposed to a rf (13.56 MHz) excited hydrogen discharge. The excitation source was formed by a 12 turn coil around a 25.4 mm quartz tube. The samples were placed 40 cm downstream from the center of the excitation volume. In this setup the samples were remote from the plasma glow with the exception of some diffuse light around the sample at low pressures (< 20 mTorr). The process pressure was established by turbomolecular pumping and a throttle valve interconnected with a pressure transducer. Sample heating was accomplished by a tungsten coil ~ 4 mm from the backside of the wafer. The temperature was measured by a thermocouple placed directly behind the center of the sample. The H-plasma system is shown schematically in ref. 2.

Real-time *in situ* identification of the gas phase species was achieved by residual gas analysis (RGA). The RGA operated in the Faraday Cup mode and was positioned between the throttle valve and the turbo pump. The charged species in the plasma were monitored with a double Langmuir probe (DLP). The probe is comprised of cylindrically symmetric double sleeved Al_2O_3 around 0.5 mm diameter tungsten wire. The I-V characteristics collected with the DLP were obtained from the sample surface region. This information is used to calculate the electron temperature and plasma density.

Surface characterization included atomic force microscopy (AFM) and cross-sectional transmission electron microscopy (TEM). The AFM was used to study surface topography following the processing.

The subsurface region was characterized with cross-sectional TEM and Raman spectroscopy. TEM specimens were prepared using conventional techniques including mechanical thinning and Ar-ion milling. TEM micrographs were recorded at 200 or 300 keV. The Raman scattering was excited with 200 mWatts of 514.5 nm Ar^+ laser radiation focused to a 100 μm x 3 mm spot. The spectra were obtained with an instrument resolution of ~ 4 cm^{-1} and a step size of 2 cm^{-1}.

RESULTS

Silane fragmentation patterns were identified with the RGA (6). The largest peak in the silane fragmentation pattern is the 30 amu peak (SiH_2). The SiH_2 signal intensity was tracked as a function of substrate temperature, bias, and process pressure. Fig.1 represents the substrate temperature influence on the concentration of gas phase SiH_2. The data

indicates that the SiH_2 is a maximum at ~100°C and decreases with an increase in substrate temperature. In contrast to the pronounced thermal dependence, the SiH_2 peak does not vary significantly with substrate bias (±25 V) or process pressure (10 - 200 mTorr).

The determination of the electron temperature (τ_e) and plasma density (n_0) from the DLP data followed the method outlined in ref. 7. For H-plasma conditions of 20 Watts and 15 mTorr, $\tau_e \sim 4$ eV and n_0 is estimated from the expression

$$I_{sat}^{+} = \frac{1}{2} n_0 e \sqrt{\frac{\tau_e}{m_i}} A \qquad [1]$$

where I_{sat}^{+} is the ion saturation current, e is the electronic charge, A is the exposed area of the probe, and m_i is the ion mass. Using Eqn. [1], the plasma density near the surface is ~ 2.5×10^8 cm^{-3}. The flux to the surface can be calculated from the form

$$\left[H^{+}\right] = \frac{n_0 \langle v_i \rangle}{4} \qquad [2]$$

where $\langle v_i \rangle = \sqrt{\frac{8\tau}{\pi m_i}}$ is the thermal average ion speed. From Eqn. [2] and assuming τ = 0.043 eV (500 K), the H^+ flux to the Si surface is ~ 2.4×10^{13} cm^{-2} sec^{-1}. The DLP data can also be used to estimate the dissociation coefficient (χ) for molecular hydrogen. The details of the calculation are in ref. (8). Using the value of χ, the atomic H flux can be estimated. The resulting expression is

$$[H] = 2.1 \times 10^{18} cm^{-2} sec^{-1} \bullet \chi \bullet P(mTorr) \qquad [3]$$

where P(mTorr) is the process pressure in units of mTorr. For H-plasma conditions of 20 Watts and 15 mTorr, $\chi = 0.45$ and the H flux to the Si surface is ~ 1.4×10^{19} cm^{-2} sec^{-1}.

AFM images can be divided into two temperature regions for H-plasma processing at 15 mTorr: (i) low temperatures (< 200°C) resulting in a root mean square (rms) roughness of > 15 Å and (ii) higher temperatures (> 450°C) resulting in an rms roughness of < 5 Å. A summary of the thermal and temporal trends of the rms roughness, determined from the AFM images, is displayed in Fig. 2. The temporal dependence does not exhibit an obvious trend. In contrast, the temperature dependence indicates that lower temperatures result in greater rms roughness values.

Extended defects with an associated strain field are evident in two-beam and n-beam systematic images which are recorded under bright-field, dark-field or dark-field weak-beam diffracting conditions. In the cross-sectional bright-field image (Fig. 3a), these defects are observed below the Si (100) surface after 150°C, 60 min H-plasma exposure. Defects denoted as a - type images in Fig. 3a are essentially closer to the surface (i.e. within 10 nm), whereas defects denoted as b - and c - type images lie as deep as 200nm and 300 nm, respectively, from the silicon (100) surface. These defects have an image size which

increases typically from ~ 1nm (i.e. a - type images) to ~ 70nm (i.e. c - type images). The number density, N_d, of extended defect images per unit area was $\geq 10^9$ cm^{-2} from plan view micrographs not included here (12). Based on the trace analysis method, the habit plane of b - type images is one of inclined {111}'s and the habit plane of c - type images is one of edge-on {111}'s. In Fig. 3b for the 450°C, 60 min H-plasma exposure, these image features are not observed.

Fig. 4a and 4b are the dark-field weak-beam electron micrographs of the Si (100) substrate after the 450°C, 1 min H-plasma exposure in cross-sectional mode and plan-view mode, respectively. No obvious contrast feature from a strain center due to the defect is observed. According to ref. 12, when the defect structure in Fig. 3a is imaged in plan-view such that the H-exposed Si (100) is at the electron entrance surface of the specimen, b - and c - type images give rise to loop-like contrast features whereas a - type images typically appear as spots. If the same specimen area is imaged in two-beam, dark-field diffracting conditions at or near the Bragg condition (i.e. $s_g \sim 0$), then the loop-like features corresponding to b - type images and the spot-like features corresponding to a - type images typically exhibit black/white lobe contrast. The black/white contrast is enhanced at regions of the image where $s_g < 0$, as is expected for extended defects which are located near the electron entrance surface of the specimen. Even in the two-beam, dark-field image where $s_g < 0$, defect contrast was not observed in the specimen after the 450°C, 1 min H-exposure.

Raman spectroscopy data indicating subsurface H in Si (100) has been previously published (2,4). The Raman spectroscopy data in Fig. 5a is representative of the Si (100) samples exposed to 150°C, 60 min H-plasma conditions. The spectra indicates a dominant signal at ~ 1470 cm^{-1} due to the three phonon overtone of the optical phonon branch (4). Fig. 5b is representative of samples receiving the 450°C, 60 min H-plasma exposure. Comparing the spectra in Figs. 5 a and b, the spectra for 150°C, 60 min H-plasma exposure indicates an additional feature at ~ 2100 cm^{-1}. This additional feature is associated with Si-H bonding in the Si crystal (4). For samples processed for 450°C, 60 min H-plasma conditions, the Raman spectra is similar to unprocessed samples, *i.e.* no Si-H features (2,4). Following the calculation of the N.M. Johnson, *et. al.* (4), the H concentration contained in the near surface region can be estimated. Equating the ratios of intensities at 520 cm^{-1} (not displayed here) and 2100 cm^{-1} to the respective ratios of concentrations, and using the Si atomic density, 5.0×10^{22} cm^{-3}, the near surface H concentration is ~ 5×10^{19} cm^{-3}.

DISCUSSION

The dose of ions and atomic H that the H-plasma processed samples received can be determined from the calculated fluxes. For the 60 min H-plasma exposures, the ion dose is ~ 8.75×10^{16} cm^{-2} and the atomic H dose is ~ 5.02×10^{22} cm^{-2}. In other words, the ion dose is ~ 10^6 times lower than the atomic H dose. The dose ratio is the same for the 2 min exposures. Given the large dose differential in the same plasma environment, it is reasonable to assume that the surface roughness and subsurface defects are largely due to atomic H reacting with the Si and not due to the ions.

The atomic H interacts with the Si surface at low temperatures (< 350°C) to form SiH_x species on the surface which can result in etch products (9). Etch products are indicated by the observed fragmentation of silane in the RGA spectra. The temperature

dependence of the RGA data displayed in Fig. 1 indicates that etching of the Si (100) by the H-plasma is enhanced at low temperature. The summary of the AFM data displayed in Fig. 2 indicates that the rms roughness is increased at low temperature. Combining these results, the surface etching by the H-plasma results in rough surface topography.

This prompts the question as to why the etching is increased at lower temperature. Previous calculations of the temperature dependence of the surface H coverage indicates that the atomic H surface concentration decreases with increasing surface temperature (8,11). Hence, the fact that the etching and roughness are increased at low temperature is related to the higher surface H concentration. At higher temperature, atomic H recombines on the Si (100) surface to form stable H_2 desorption products thus decreasing the surface H concentration (9). The increased H concentration at low temperature produces bond strain between surface Si-H_2 units (10). This bond strain weakens the Si-Si backbonds and makes them susceptible to etching by the atomic H (10). Therefore, surface etching is increased at low temperature due to the increase in atomic H coverage leading to weakening of the Si-Si backbond.

During the 150°C, 60 min H-plasma exposure, the atomic H diffuses into the subsurface region of the Si sample (4). Following exposure to 150°C, 60 min H-plasma conditions, the Raman spectra indicates subsurface Si-H bonding (Fig. 5a) and the cross-sectional TEM indicates subsurface defects (Fig. 3a). Increasing the processing temperature to 450°C results in Raman spectra with no indication of Si-H bonding (Fig. 5b) and no observable subsurface defects in the TEM (Fig. 3b). The Raman and TEM data collectively suggest that (i) the subsurface H concentration is related to the subsurface defects and (ii) the concentrations of subsurface H and subsurface defects are temperature dependent. Since atomic H is not implanted into the Si (100), it is reasonable to associate the depth of subsurface defects with the diffusion of subsurface H. The depth of diffusion of atomic H can be estimated based on an effective diffusion coefficient for 150°C of $D_{eff} \approx 1.8 \times 10^{-13}$ cm^2 sec^{-1} (13). Hence, the calculated depth for 60 min is ~ 254 nm. The depth of the defects observed in the TEM micrographs is $\leq$ 300 nm. The close agreement between the diffusion depth of atomic H and the depth of defects suggests that the defects are related to the subsurface atomic H. The temperature dependence of the subsurface H and subsurface defects can also be explained in terms of atomic H diffusion. At higher temperatures, two changes influencing atomic H diffusion occur. First, the surface concentration of atomic H is reduced (11) so the concentration available for diffusion into the sample is decreased. Second, the effective diffusivity of atomic H is increased so H can migrate rapidly and not build up in the subsurface region. Therefore, higher temperature (450°C) H-plasma processing results in a reduced subsurface H concentration and, hence, no subsurface defects.

CONCLUSIONS

To summarize, the RGA spectra indicates that surface etching of Si (100) by plasma excited H decreases with increased substrate temperature. AFM images indicate that surface roughening is decreased for samples exposed to the H-plasma at increased temperature. The TEM data indicates that surface roughness is decreased for H-plasma conditions of 450°C. The TEM data also indicates that the subsurface defect density is reduced for 450°C, as opposed to 150°C, 60 min H-plasma processing. The TEM and Raman data suggest that the subsurface defects are related to the subsurface hydrogen

concentration. Furthermore, the reduction of subsurface defects is achieved by H-plasma processing at higher temperature (450°C).

ACKNOWLEDGEMENTS

We acknowledge helpful discussions with R. Thomas, R. Markunas and R. Rudder of the Research Triangle Institute. We also thank A. Sowers for his help in collection of the Raman spectra and R. Carter for his efforts in processing the Si wafers. This work was supported in part by the NSF, through grant CDR 8721505, and the Engineering Research Center for Advanced Electronic Materials Processing at NCSU.

REFERENCES

1. R.A. Rudder, S.V. Hattengady, J.B. Posthill, and R.J. Markunas, Mat. Res. Soc. Symp. Proc., 116, 529 (1988).
2. T.P. Schneider, J. Cho, D.A. Aldrich, Y.L. Chen, D. Maher, and R.J. Nemanich, Proc. 180th. Ann. Mting. ECS, 92-12, 122 (1991).
3. J. Cho, T.P. Schneider, J. Vander Weide, H. Jeon, and R.J. Nemanich, Appl. Phys. Lett., 59, 1995 (1991).
4. N.M. Johnson, F.A. Ponce, R.A. Street, and R.J. Nemanich, Phys. Rev. B, 35, 4166 (1987).
5. D.B. Fenner, D.K. Biegelsen, and R.D. Brigans, J. Appl. Phys., 66, 419 (1990).
6. T.P. Schneider, J. Cho, J. Vander Weide, S.E. Wells, G. Lucovsky, and R.J. Nemanich, M.J. Mantini, R.A. Rudder, R.J. Markunas, Mat. Res. Soc. Symp. Proc., 204, 333 (1991).
7. R.M. Clements, J. Vac. Sci. Technol., 15, 193 (1978).
8. T.P. Schneider, J. Cho, and R.J. Nemanich to be published.
9. S.M. Gates, R.R. Kunz, and C.M. Greenlief, Surf. Sci., 207, 364 (1989).
10. J.J. Boland, Surf. Sci., 261, 17 (1992).
11. T.P. Schneider, J. Cho, and R.J. Nemanich, Mat. Res. Soc. Symp. Proc., 315 (Spring 1993) in press.
12. Y.L. Chen and D.M. Maher, Mat. Res. Soc. Symp. Proc., 280, in press (1992).
13. N.M. Johnson, in Hydrogen in Semiconductors, J.I. Pankove and N.M. Johnson, Editors, p. 328. Academic Press, San Diego, CA (1991).

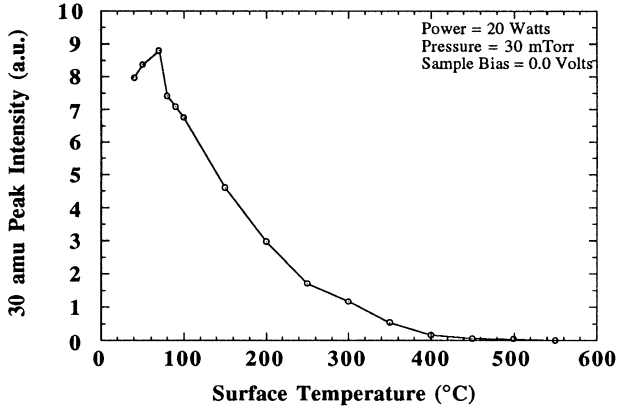


Fig. 1 Temperature dependence of the 30 amu signal from residual gas analysis spectra collected during H-plasma processing.

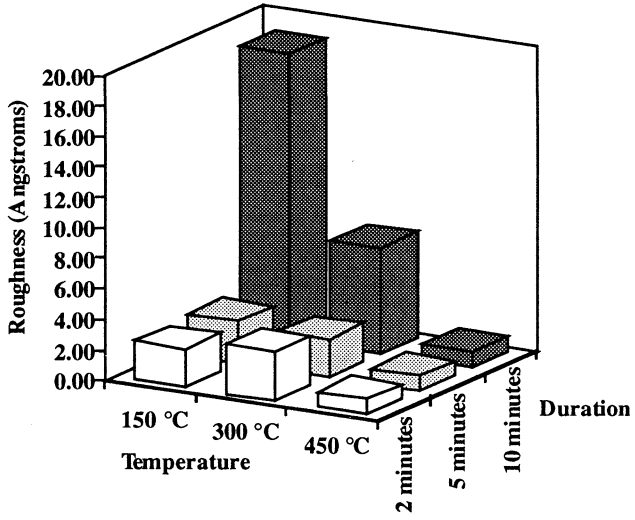


Fig. 2 Summary of the temperature and exposure time dependence of the rms surface roughness, calculated from AFM images, following H-plasma exposure.

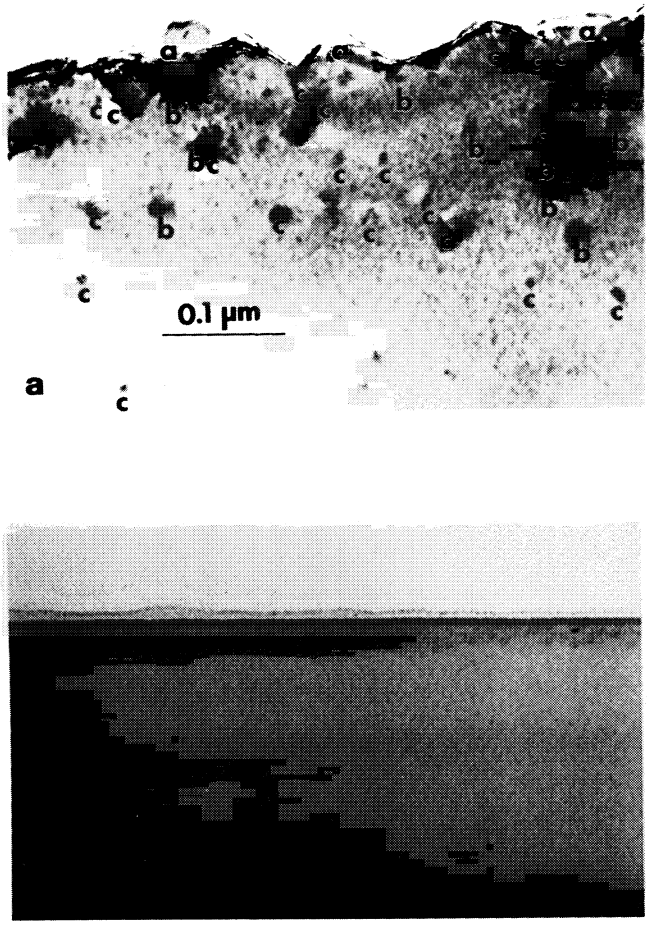


Fig. 3 TEM cross-sectional mode: bright-field images of Si (001) after 60 min H-plasma exposures at (a) 150°C, where three image features are identified: a - type, b - type, and c - type images, and (b) 450°C, where the a -, b - or c - type image features are not observed. Both micrographs, (a) and (b), have the same scale as indicated in (a).

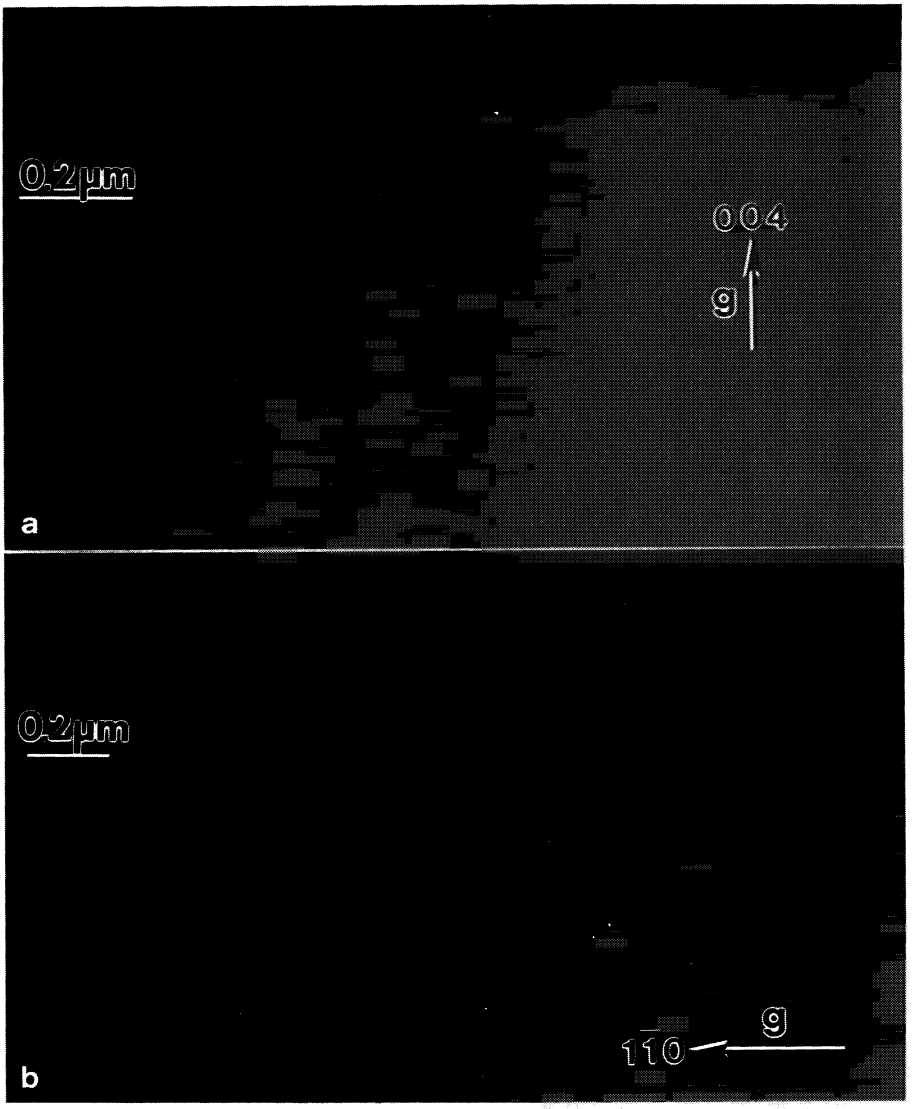


Fig 4 Si (001) after a 1 min H-plasma exposure at 450°C. In (a), cross-sectional mode: dark-field weak-beam image at **g**, 3**g**, $s_{3g} \sim 0$ with **g** = [004]. In (b), plan-view mode: weak-beam dark-field image at **g**, 3**g**, $s_{3g} \sim 0$ with **g** = [2 2 0]. No obvious contrast feature from a strain center due to the defect was observed.

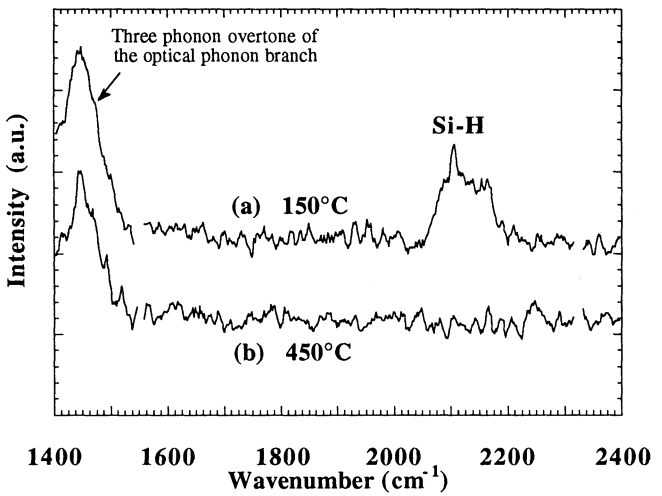


Fig. 5 Raman spectra collected from Si (100) following H-plasma exposure for 60 min at (a) 150°C and (b) 450°C. The feature at ~ 2100 cm^{-1} is related to Si-H bonding in a Si crystal.

IN SITU CHAMBER CLEANING USING HALOGENATED-GAS PLASMAS EVALUATED BY EXTRACTED-PLASMA-PARAMETER ANALYSIS

Kazuhide Ino[1)], Iwao Natori[1,2)], Akihiro Ichikawa[1,2)] and Tadahiro Ohmi[1)]
[1)]Department of Electronic Engineering, Tohoku University, Aza-Aoba, Aramaki, Aobaku, Sendai 980, Japan
[2)]Laboratory for Microelectronics, Research Institute of Electrical Communication, Tohoku University, 2-1-1, Katahira, Aoba-ku, Sendai 980, Japan

ABSTRACT

We have demonstrated that high-efficiency *in situ* chamber cleaning with the short gas residence time is available for SiO_2 RIE chambers by using NF_3 plasma. The plasma of NF_3 gas, which has a low bond energy, can generate high density ions and radicals with low kinetic energy. The cleaning efficiency of several halogenated-gas plasmas have been evaluated based on extracted-plasma-parameter analysis. In this analysis important plasma parameters, such as ion energy and ion flux density, could be extracted through a simple rf waveform measurement at the excitation electrode. The accuracy of this technique has been confirmed with a newly developed rf-plasma direct probing method and the ion current measurements.

INTRODUCTION

In order to establish fluctuation-free processing for future ULSI fabrication, it is a necessity to make the processing chamber conditions always identical at the start of each processing[1]. To this end, the condition of the chamber inner surface must be absolutely clean, or must be stabilized with a deposition layer. The technique of intentionally forming a film on the chamber walls, a pre-deposition layer, guarantees near-identical conditions for subsequent processing. However, such a technique has many problems. The biggest problem is that of particle generation, which is the leading cause of decreasing device yield at present. Therefore in order to keep the chamber inner surface free from sub-products, the establishment of high-efficiency *in situ* chamber cleaning technology is desired.

In order to establish high accuracy pattern etching with high etch rate and selectivity, a new etching technique is proposed[2], which is characterized by a high gas flow rate and a high pumping rate. In this technique, a high etch rate for crystalline silicon has been obtained. The reason for increased etch rate is that the high gas flow rate supplies a sufficient reactant gas and the high pumping rate enables the effective evacuation of reaction products[2-4]. Then it is expected that the effective evacuation can suppress sub-products deposition onto chamber walls and internal fixtures, and that the high-gas-flow-rate technique can enhance the removal of the deposited materials.

The purpose of this paper is to present high-efficiency *in situ* chamber inner surface cleaning technology, which enables us to ideally initialize the chamber conditions after each process run. Firstly we describe a convenient plasma-evaluation

technique, which is called extracted-plasma-parameter analysis[5-7], for estimating the cleaning efficiency of several halogenated specialty gases. In this analysis the two important plasma parameters, ion energy and ion flux density, could be extracted through very simple rf waveform measurements at the excitation electrode. This technique also enables us to *in situ* monitor the plasma parameters without inducing any contaminations and external disturbances to the plasma. And based on the results of this analysis, the high-ion-density and low-ion-bombardment-energy plasma has been created. The accuracy of the technique has been confirmed with a newly developed rf-plasma direct probing method[8,9] and the ion current measurements. We also demonstrated that *in situ* chamber cleaning under a high gas flow rate and a high pumping rate enhances the removal of sub-products adhering on the inner surface of reactive ion etching (RIE) chambers used for SiO_2 etching.

EXPERIMENTAL

Experiments were performed using a parallel-plate capacitively-coupled RIE equipment having 13.56MHz rf excitation. The electrodes and the chamber were made of stainless steel with mirror-polished surfaces to minimize outgassing. A high-voltage probe (Tektronix P6015) was attached directly to the backside of the plasma excitation electrode in order to minimize the stray impedance effects, which allows for the input voltage waveform Vrf(t) to be read on an oscilloscope. And plasma parameters were extracted as in the following[5,6]. The instantaneous voltage of the plasma excitation electrode is expressed by

$$V_{rf}(t) = V_{rfo}\sin(\omega t)+V_{dc}\ , \quad (\ V_{dc}< 0\ ). \tag{1}$$

Here, Vrfo is the amplitude of the rf waveform, ω is the angular rf driving frequency, and Vdc is the self-bias voltage of the powered electrode. And the time-averaged plasma potential Vp was estimated by using the well known equation[10,11] in this experiment,

$$V_p = \frac{V_{rfo}+V_{dc}}{2}\ , \quad (\ V_{dc}< 0\ ). \tag{2}$$

The ion energy (Eion) bombarding the substrate surface was defined as a difference between the time-averaged plasma potential and the self-bias voltage of the substrate electrode:

$$E_{ion} = V_p - V_{dc}\ , \quad (\ V_{dc}< 0\ ). \tag{3}$$

In addition a new parameter called *Flux Parameter* is introduced as a measure of ion density,

$$\textit{Flux Parameter} = \frac{P}{V_{pp}} \tag{4}$$

where P is the rf input power and Vpp = 2Vrfo. Since P/Vpp has a dimension of current

and relates to the plasma density, the parameter can be taken as a measure of ion flux density incident on the substrate surface[7,12]. By use of these plasma-parameters, we have estimated the cleaning efficiency of several halogenated specialty gases. And the accuracy of the analysis has been confirmed with a newly developed rf-plasma direct probing method[8,9] and the ion current measurements. Moreover the rf-excited plasma potential Vp(t) has been measured directly by the probe.

RESULTS AND DISCUSSION

Firstly we will describe how dramatic changes can occur when sub-products are deposited on an inner surface. Figure 1 shows the relationship between the reactor surface condition and the SiH_4 decomposition rate[13,14]. Only this experiment was carried out in an 1" electropolished SUS316L tubes, whose internal surface has a composition of about 65% Cr_2O_3 by O_2 passivation of the original stainless surface[15]. This figure shows the effect of poly-silicon deposition degree on the unreacted silane fraction as a function of gas residence time, i.e. the mean time a gas remains in the tube, at 0.01% SiH_4/Ar at 400°C. Initially, the decomposition rate was slow on the bare reactor surface without any silicon deposition. After the first poly-silicon deposition by flowing a pure SiH_4 gas at 450°C for 30 minutes, the decomposition rate doubled. And we have found that the thermal decomposition rate stabilized after four cycles (a total deposition rate was 2.5 hours), where the inner surface of the tube was totally covered by a poly-silicon layer. In other words, with a change in the surface condition a fluctuation in processing occurs. In order to avoid this type of fluctuation, the condition of the inner surface must be absolutely clean, or must be stabilized with a deposition layer. However, the technique of intentionally forming a film on the inner surface is by no means acceptable for high quality processing, because particle generation is quite crucial. Therefore the establishment of high-efficiency *in situ* chamber cleaning technology is quite essential in order to maintain the process reproducibility.

Figure 2 shows the relationship between plasma parameters and the bond energy for five specialty gases. These plasma parameters have been extracted, as we have indicated before. It can be clearly seen from this figure that the lower the bond energy of a gas is, the lower its ion bombardment energy and the higher its ion flux density. However, the time-averaged plasma potential does not appear to depend on the bond energy. These results lead to the conclusion that the optimal gas for *in situ* chamber cleaning is halogenated gas with low bond energy, which can generate high density ions and radicals with low kinetic energy.

We have evaluated the etch rate of a mixture of the photoresist TSMR-8900 and an OCD silica solution coated onto a silicon wafer in order to simulate the sub-products adhering on the inner surface of RIE chambers used for SiO_2 etching. The SiO_2 RIE process is believed to be the major cause of yield loss due to process induced particles. Figure 3 shows the etch rate of chamber deposited materials by using NF_3(a), CCl_4(b) and HBr(c) plasmas as a function of bombarding ion energy and ion flux density, where the gas flow rate was 50sccm. We have seen that the etch rate of deposited material is in general the greatest when fluorinated gases with low bond energy are used, while

chlorinated gases and bromium gases etch it only slowly. It is also seen from Figure 3(a) that a large etch rate is obtained even for smaller ion bombardment energies when the ion flux parameter is high.

Figure 4 shows the etch rate of deposited materials and the gas residence time as a function of NF_3 gas flow rate at a constant pressure of 10mTorr. The rf input power was maintained at 150W, then the ion bombardment energy was also a constant value of 320eV. The increase in the flow rate resulted in a dramatic increase in the etch rate. The reason for increased etch rate is that the reduction of gas residence time would provide a dramatic increase in the etching spices and the effective evacuation of reaction products. Then it is confirmed that *in situ* chamber cleaning with a high flow rate and a high pumping rate can enhance the removal of the sub-products adhering on chamber walls and internal fixtures.

Figure 5(a) shows the photograph of a grounded electrode after SiO_2 etching by CF_4/H_2 plasma for 10 hours, where the total pressure was 45mTorr and the flow rate of CF_4 and H_2 were 15 and 10sccm, respectively. The grounded electrode has been discolored into brown by adhered sub-products. Figure 5(b) shows the electrode after *in situ* chamber cleaning by NF_3 plasma for 30 minutes. It is clearly seen that the sub-products have been completely cleared away from the electrode. The cleaning conditions were the rf input power of 300W, NF_3 gas flow rate of 50sccm, and the pressure of 100mTorr. It is confirmed that high-efficiency *in situ* chamber cleaning is available for SiO_2 RIE chambers by using NF_3 plasma.

Figure 6 shows the waveforms of the plasma potential Vp(t) and the excitation electrode voltage Vrf(t) at 60mTorr in argon, where the rf input-power is 90W. By use of a newly-developed rf-plasma direct probing method, the relationship between the plasma potential and the rf electrode voltage has been clarified. The important point to note is the distortion of the plasma potential. In general, it has been considered that the waveform of the plasma potential is sinusoidal for the simplified capacitive model of the sheath[10]. Therefore the distortion of the measured waveform seems to be induced by the increased direct current (i.e. the positive ion current and the electron current) flowing through the sheath, which is not small compared to the displacement current for the resistive model of the sheath.

Figure 7 compares the rf input-power dependence of the time-averaged plasma potentials obtained by two different methods. One is measured by a newly developed rf Langmuir probe with the high impedance between the probe and ground, and the other is estimated from the voltage waveform of the plasma excitation electrode by use of Eq.(2). As can be seen in the figure, estimated values from voltage waveforms are in good agreement with those which are accurately measured by the new rf Langmuir probe. Then it is confirmed that the time-averaged plasma potential could be estimated through a simple rf waveform measurement.

Figure 8 shows the relationship between the flux parameter calculated by using Eq.(4) and the ion current fed into the rf electrode for NF_3, CCl_4 and Ar. The ion current was determined by measuring the saturated current while the dc voltage of the electrode was continuously changed to the side of negative bias. The ion current is almost proportional to the flux parameter. Therefore, by use of this new parameter we can

estimate the ion flux density. However, the straight line drawn in the graph does not pass through the origin. If the flux parameter indicates the ion flux density, the line would indeed pass through the origin. The precision with which Vpp are measured in this work is adequate to eliminate measurement uncertainty as the reason for the nonzero intercept in Fig. 8. The most likely explanation for the failure of the line to pass through the origin is that the rf input power measured at the rf generator includes not only the power-loss in the plasma but also that of a matching network and parasitic resistance. The flux parameter, however, could be used as a measure of ion flux density. Then the accuracy of extracted-plasma-parameter analysis has been confirmed.

CONCLUSION

We have demonstrated that high-efficiency *in situ* chamber cleaning with the short gas residence time is available for SiO_2 RIE chambers by using the plasma of NF_3 gas which has a low bond energy. And the accuracy of extracted-plasma-parameter analysis has been verified by the accurate characterization of rf-generated plasma by a new probe measurement technique, and by the ion current measurements. Moreover the rf-excited plasma potential has been measured directly by the probing method, which has clarified the relationship between the plasma potential and the rf electrode voltage.

ACKNOWLEDGMENT

This study was carried out at the Super Clean Room of Laboratory for Microelectronics, Research Institute of Electrical Communication, Tohoku University.

REFERENCES

1. T. Ohmi, *Breakthrough for Scientific Semiconductor Manufacturing in 2001 - A Proposal from Tohoku University, a special issue of Break Through,* No. 71, p. 36, Realize Inc., Tokyo (1992)
2. K. Tsujimoto, T. Kumihashi, N. Kofuji and S. Tachi, *Digest of Technical Papers of 1992 VLSI Symposium, Seattle,* p. 46 (1992)
3. B. N. Chapman and V. J. Minkiewicz, J. Vac. Sci. Technol., **15**, 329 (1978)
4. B. N. Chapman, T. A. Hansen and V. J. Minkiewicz, J. Appl. Phys., **51**, 3608 (1980)
5. T. Yamashita, S. Hasaka, I. Natori, H. Fukui and T. Ohmi, IEEE Trans. Semi. Manu., **5**, 223 (1992)
6. T. Yamashita, S. Hasaka, I. Natori and T. Ohmi, IEICE TRANS. ELECTRON., E75-C, **7**, 839 (1992)
7. S. Hasaka, I. Natori, T. Yamashita and T. Ohmi, *Extended Abstracts of 181th ECS Meeting, St.Louis,* No. 66, p. 107 (1992)
8. M. Hirayama, W. Shindo and T. Ohmi, *Extended Abstracts of SSDM, Makuhari,* p. 210 (1993)
9. M. Hirayama and T. Ohmi, in preparation for publication
10. K. Köhler, J. W. Coburn, D. E. Horne, and E. Kay, J. Appl. Phys., **57**, 59 (1985)

11. J. W. Coburn and E. Kay, J. Appl. Phys., **43**, 4965 (1972)
12. R. Petri, D. Henry and N. Sadeghi, J. Appl. Phys., **72**, 2644 (1992)
13. S. Takahashi, T. Watanabe, S. Miyoshi, A. Ohki, K. Kawada, M. Nakamura, Michael S. K. Chen and T. Ohmi, *Extended Abstracts of 182nd ECS Meeting, Toronto,* No. 414, p. 612 (1992)
14. T. Ohmi, T. Watanabe, Michael S. K. Chen, K. Kawada, A. Ohki, M. Nakamura and K. Hirao, to be published in J. Electrochem. Soc.
15. M. Nakamura, K. Kawada, A. Ohki, A. Hioki, K. Hirao and T. Ohmi, *Extended Abstracts of 180th ECS Meeting, Phoenix,* No. 534, p. 798 (1991)

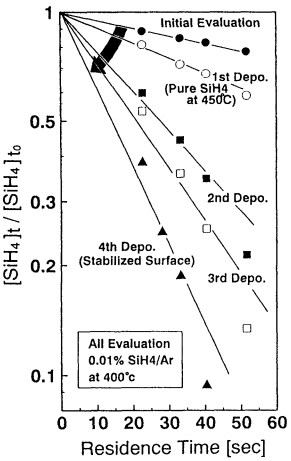


Figure 1 The thermal decomposition characteristics of SiH_4 with the surface condition transition.

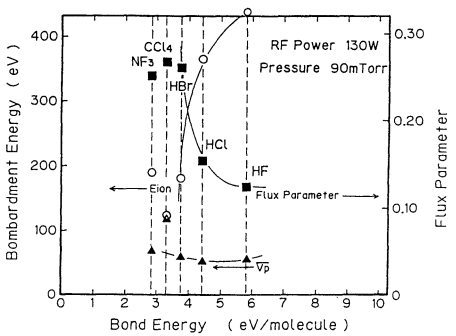
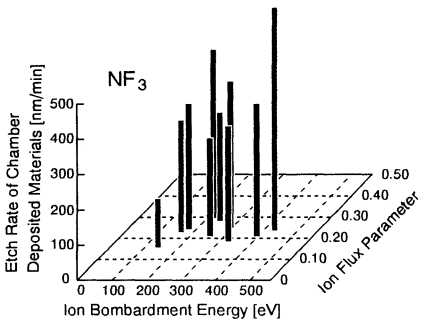
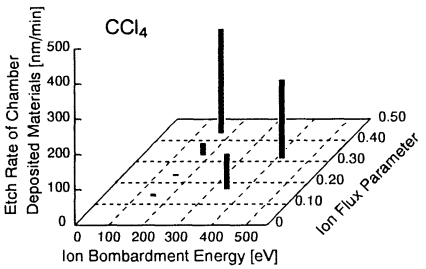


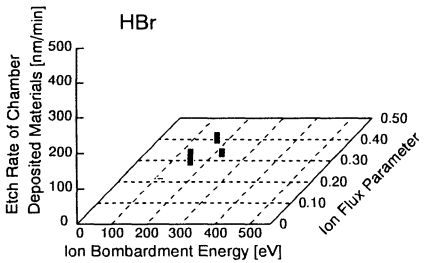
Figure 2 The relationship between bond energy and estimated plasma parameters, such as ion bombardment energy(Eion), the flux parameter and the time-averaged plasma potential(Vp).



(a)



(b)



(c)

Figure 3 The etch rate of a mixture of photoresist and an OCD silica solution modeled sub-products of etching chamber for NF_3(a), CCl_4(b) and HBr(c).

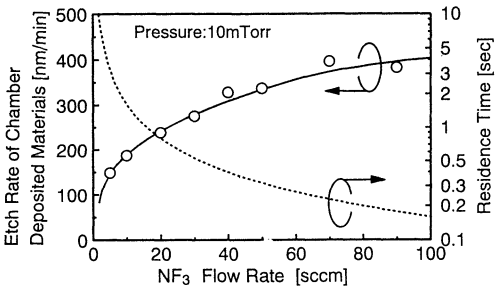
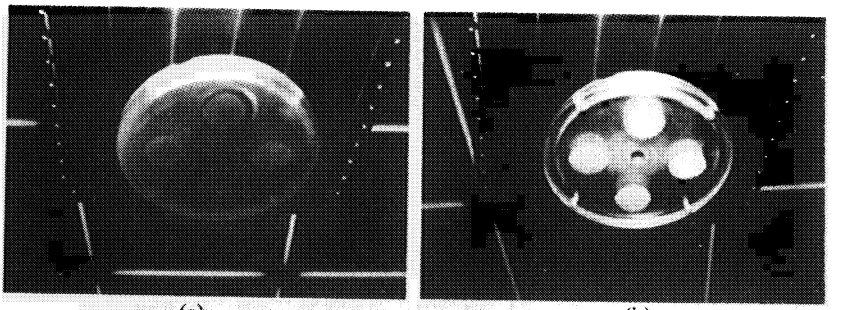


Figure 4 The etch rate of a mixture of photoresist and an OCD silica solution modeled sub-products of etching chamber and the gas residence time as a function of NF_3 gas flow rate at a constant pressure of 10mTorr.



(a) (b)

Figure 5 The photographs of the grounded electrode after SiO_2 etching for 10 hours(a), and after *in situ* chamber cleaning by NF_3 plasma for 30 minutes(b).

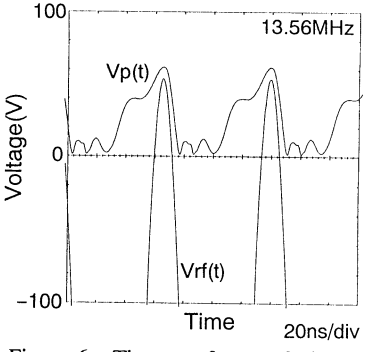


Figure 6 The waveforms of plasma potential Vp(t) and excitation electrode voltage Vrf(t) at 60mTorr in argon. The rf input-power is 90W.

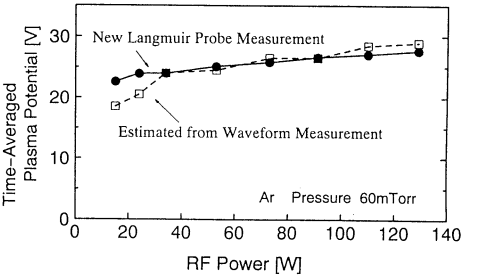


Figure 7 The rf input-power dependence of the time-averaged plasma potential which is measured by a newly developed rf Langmuir probe and estimated from the voltage waveform of the plasma excitation electrode.

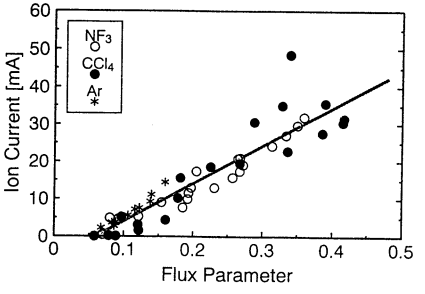


Figure 8 The relationship between the flux parameter and the ion current.

SELECTIVE ETCHING OF NATIVE OXIDE USING VAPOR HF PROCESSING

John M. de Larios and John O. Borland
Genus, Inc. Thin Film Division
1139 Karlstad Dr.
Sunnyvale, CA 94086

ABSTRACT

Selective etching of native oxide in the presence of thermal and deposited oxides is studied in a low pressure-single wafer reactor using azeotropic HF/H_2O, H_2O, azeotropic HCl/H_2O, and anhydrous HF + IPA. The oxide etch rate and the time required to initiate the etch is sensitive to the type of reactants introduced into the etch chamber. This initiation time, or "delay time," has a significant influence on etch selectivity. SIMS encapsulation studies were performed to determine surface contamination levels associated with the gas and vapor phase cleans.

INTRODUCTION

The selective removal of a native or chemical oxide from a Si surface is required for many applications involving the manufacture of VLSI devices. A successful selective etch process must have the capability of removing native oxides in the presence of thermal, deposited, or doped oxides. Selectivity issues are important for the following applications illustrated in Fig. 1: 1) Pre-Gate Oxidation, 2) Pre-Tungsten silicide, 3) Pre-Poly, and 4) Pre-Nitride Cleans (1). Another important application not shown here is the removal of native oxide in a contact opening prior to metal deposition. In all of the above applications, the native oxide must be selectively removed from a Si surface in the presence of thermal or CVD oxides. Currently alternatives for native oxide removal include aqueous chemical cleaning, rapid thermal cleaning, plasma cleaning, and gas and vapor phase cleaning. A comparison of methods is presented in Table I (2). Using aqueous chemistries, the minimum native oxide thickness is obtained using an "HF Last" clean followed by a DI rinse. This type of processing has been associated with a particle deposition problem due to the reactivity of the Si surface. Wet cleaning can also result in poor selectivity since all types of oxides begin to etch upon immersion in a wet bath. Rapid thermal cleaning at high temperatures in hydrogen is capable of removing native oxide through the desorption of SiO. However, non-uniform removal of the oxide film can cause surface pitting and sidewall undercutting. Carbon contamination on the wafer surface is likely to form carbides that can affect the integrity of a subsequent process. Plasma cleaning can cause surface damage due to ion bombardment and charging affects. It is also associated with contamination of the wafer surface. Vapor HF methods can alleviate many of the contamination and damage issues listed above, but may be limited by the presence of surface residues and poor selectivity. This is especially true when removing native oxide in the presence of doped oxides.

In this report, we examine the dependence oxide etch selectivity on the chemistry of the reactants during HF vapor processing. The reactants include combinations of azeotropic HF/H_2O, azeotropic HCl/H_2O, H_2O, IPA, and anhydrous HF. Previous workers have studied the affects of wafer temperature (3, 4, 5), processing pressure (6), and reactant moisture content (7). Using an azeotropic HF/H_2O source to produce the reactant vapor, Wong et al. (3) determined that the etch selectivity of PSG to thermal oxide could be increased from 18:1 to at least 2,900:1 by raising the wafer temperature from 25°C to 50°C. Watanabe et al. (6) developed a low pressure selective etching technique resulting in a etch ratio of 2,000:1 between BPSG and thermal oxide. This allowed them to use the BPSG as a mold for 256 Mb DRAM capacitors. Miki et al. (7) showed that the etch selectivity was strongly dependent on the moisture levels in the reactor when using anhydrous HF. Lowering the moisture levels allowed the etching of native oxides in the presence of doped CVD oxides. In general, however, etching with anhydrous HF without adding a solvent such as water or alcohol can result in uneven etching with poor uniformity and reproducibility. This lack of control is likely a result of localized etching in areas of increased surface water contamination levels.

Table I. Limitations of Cleaning Methods.

CLEANING METHOD	PROBLEMS
Aqueous HF	Particle Deposition, Selectivity Control
Rapid Thermal Cleaning	Surface Pitting, Sidewall Undercutting
Plasma Cleaning	Surface Damage, Contamination
Vapor HF	Residues, Selectivity Control

EXPERIMENTAL

Native oxide, thermal oxide, and deposited oxide films were processed on a single wafer-low pressure HF vapor system (8). The wafer was held in a SiC chamber at ambient temperature and pressures below 350 Torr. Etch selectivity data has been collected using gas and vapor phase mixtures of HF, H_2O, HCl, and IPA. Under normal operations, a N_2 carrier gas is used to transport azeotropic HF/H_2O (38.4% HF), azeotropic HCl/H_2O (22.8% HCl), H_2O, and high purity IPA vapor to the wafer surface. In addition, this reactor has the capability for delivering anhydrous HF without a carrier gas. The combinations used in this study are listed in Table II. Typically the HF source, either the azeotropic solution or anhydrous HF, is delivered to the chamber while the second source delivers either H_2O or azeotropic HCl/H_2O as dilutants or IPA as a solvent when etching with anhydrous HF. Oxide thicknesses were measured using film thickness reflectometry and ellipsometry. Oxide etch rates and "delay times" (the time required to initiate the etch reaction) were then determined. SIMS encapsulation experiments were performed to determine the surface contamination levels and compare the vapor cleans to a conventional HF strip followed by a DI water rinse.

Table II. Reactant Source Combinations Used on Vapor Phase System.

SOURCE #1	SOURCE #2
Azeotropic HF/H_2O	—
Azeotropic HF/H_2O	H_2O
Azeotropic HF/H_2O	Azeotropic HCl/H_2O
Anhydrous HF	IPA

RESULTS AND DISCUSSION

Etch selectivity of different thick oxides using aqueous processing is simply defined by the ratio of etch rates for the various materials. This definition must be modified when determining the vapor phase HF etch selectivity of native oxides for two reasons: 1) vapor phase processing leads to a significant "delay" time during which no etching takes place, and 2) a comparison of the selectivity of native or chemical oxides to thicker oxides films is difficult since native oxide etch rates are not particularly meaningful compared to the time required to remove the native oxide. Therefore, etch selectivity between native oxide and other oxides is defined simply by the amount of thermal or deposited oxide removed during the time required to over etch the native oxide by 50%. While this definition of native oxide etch selectivity is necessarily arbitrary, it allows a meaningful comparison of selectivity using different reactants and films. It is assumed that this etch time gives complete removal of the native oxide.

Azeotropic HF/H_2O

An example of the dependence of the delay time and the etch rate on the type of oxides is shown in Fig. 2 for etching using N_2 carrier gas supplying a single azeotropic HF/H_2O source. Under this set of processing conditions, the condensation process leads to a unique delay time for different types of oxides. During this delay time, the reactants are introduced into the chamber, but partial pressures are sufficiently low that etching does not take place. The delay times for native oxide, thermal oxide, TEOS, PSG (4%), and BPSG (4%B, 7%P), are 4 sec, 7.1 sec, 5.7 sec, 8.1 sec, and 2.0 sec, respectively. The etch rates were not measured for native oxide. The etch rates for thermal, TEOS, PSG, and BPSG are 48 Å/sec, 78 Å/sec, 189 Å/sec, and 129 Å/sec, respectively. The vapor phase etch characteristics of these oxides illustrate the difficulty in assigning values of etch selectivity relative to native oxide. Using the above mentioned 50% native oxide over etch definition of selectivity rather than a ratio or etch rates as used for wet chemical processing, the over etch time for native oxide is 12 sec. This over etch time is simple determined by first locating the time where the "knee" occurs in the native oxide etch curve and then increasing this time by 50%. Following this definition, the native oxide etch selectivity for thermal oxide, TEOS, PSG, and BPSG is, 217 Å, 523 Å, 725 Å, and 1250 Å, respectively. These values are also listed in Table III for thermal oxide and TEOS. HF vapor processing has the potential for improved selectivity since there is the potential for controlling the delay time as well as the etch rate.

Azeotropic $HF/H_2O + H_2O$

Dilution of the azeotropic HF/H_2O mixture with H_2O reduced thermal oxide etch rates but also shortened the delay time. This is illustrated in Fig. 3 for different ratios of N_2 carrier gas flows supplied to the azeotropic HF/H_2O and H_2O sources. The delay times are less than 3 sec for all cases compared to the delay time of 7.1 sec shown in Fig. 2 for the etching of thermal oxide using azeotropic HF/H_2O. The dilute etching of native oxide is compared to thermal oxide and TEOS in Fig. 4. In this case, the 50% over etch time for native oxide is approximately 9 sec compared to 12 sec for the azeotropic HF/H_2O sources. A comparison of Figs. 2 and 4 and Table III shows that

the dilution of the azeotropic HF with H_2O significantly reduces both the etch rate and the delay time of the thermal oxide and TEOS. The reduction in etch rate dominates, giving native oxide etch selectivities for the of the thermal oxide and TEOS 21 Å and 38 Å, respectively. The native oxide etch selectivity is improved by adding additional H_2O compared to the single azeotropic HF/H_2O source due to the much reduced etch rate of the thermal oxide and TEOS.

Table III. Thermal and TEOS Etch Selectivity: Amount of Oxide Removed During a 50% Native Oxide Over Etch.

	Native Oxide	Thermal Oxide			TEOS		
REACTANTS	50% Over Etch sec	Rate Å/sec	Delay sec	Sel. Å	Rate Å/sec	Delay sec	Sel. Å
Az.HF	12	48	7.1	217	78	5.7	523
Az.HF+H2O	9	3.2	2.0	21	5.4	1.0	38
Az.HF+Az.HCl	8	3.3	12	0	—	—	—
Anhyd. HF+IPA	18	1.5	15	< 10	6	15	<20

Note: Az. is azeotropic Anhyd. is anhydrous.

Azeotropic HF/H_2O + Azeotropic HCl/H_2O

In contrast to the case of diluting the azeotropic HF/H_2O with additional H_2O, mixing the azeotropic HF/H_2O with azeotropic HCl/H_2O increases the delay time for thermal oxide to over 12 sec while lowering the native oxide delay time. Since the 50% over etch time of native oxide of 9 sec is less than the 12 sec thermal oxide delay time, the selectivity is 0 Å. The etch rates for azeotropic HF/H_2O and azeotropic HF/H_2O diluted with HCl are nearly the same. Diluting azeotropic HF/H_2O with HCl therefore has a marked improvement in selectivity as illustrated in Fig. 5.

Anhydrous HF + IPA

Repeatable and uniform etching with anhydrous HF requires the addition of a solvent. If a solvent is not present, trace amounts of water on the wafer or in the reactor can cause local initiation of etching. Water resulting as a byproduct of this reaction can cause further local etching leading to non-uniform etch conditions. Gas phase processing using mixtures of alcohols and HF has been studied by previous workers (1, 5, 9). IPA has an advantage over water as a solvent since it will wet the bare Si surface after the native oxide is removed. Indeed, stripping native oxide with a HF/IPA mixture has the potential of a more complete removal of native oxide since there is no hydrophilic/hydrophobic transition. A comparison of native oxide, thermal oxide and TEOS etch as shown in Fig. 6 indicates that during the 50% over etch time of 18 sec, less than < 10 Å of thermal and < 20 Å of TEOS are removed. This improvement in selectivity compared to the azeotropic HF/H_2O case is due to a combination of the long delay times and low etch rates as indicated in Table III. It should be noted that the etch rates for thermal oxide and TEOS shown in Fig. 6 are not linear during the early stages of etching. The etch rate calculations are made for short etch times as this rate if of more importance when measuring etch selectivity.

Si Surface Contamination

Considerations other than etch selectivity are important when determining the appropriate vapor etch chemistry for a given application. For example, while vapor phase $HF/H_2O/HCl$ has been found to give equivalent electrical results compared to aqueous cleaning for pre-gate oxide cleans (10), this vapor mixture is not suitable for a pre-epi clean due to the formation of defects in the epi. However, a dilution of the vapor HF with IPA has produced high quality epi. SIMS encapsulation studies comparing vapor HF cleaned wafers and vapor HF + IPA cleaned wafers show less carbon and oxygen when the added IPA is used. Improved wetting of the reactants on the Si surface during the transition from hydrophilic to a hydrophobic conditions likely leads to a more complete removal of the native oxide when IPA is present.

Two series of wafers were given the cleans listed in Tables IV and V prior to CVD of epi and tungsten silicide, respectively. SIMS studies were then performed sputtering back through these encapsulating layers to the interface between the deposited films and the Si substrate. The data in Table IV compares surfaces where the native oxide is stripped with azeotropic HF, azeotropic HF followed by an IPA Dry, and a mixture of azeotropic HF + IPA. For these vapor cleans, the mixture of HF and IPA produces the lowest level of interfacial oxygen. The low fluorine levels are due to the desorption of fluorine below the temperature of the epi deposition.

The wafers listed in Table V were given either a standard 10:1 HF dip plus spin rinse dry, an azeotropic HF/H_2O vapor clean, or an anhydrous HF + IPA vapor clean prior to a dichlorosilane based CVD tungsten silicide deposition. The interfacial contamination as determined by SIMS are also plotted in Fig. 7. These data indicate that a standard wet HF followed by a DI Rinse process lowers the oxygen level at the interface by two orders of magnitude compared to the sample that was not cleaned. The azeotropic HF/H_2O clean leaves slightly more oxygen while the mixture of anhydrous HF + IPA has a significantly reduced oxygen signal. This capability of reducing the oxygen level using the anhydrous HF + IPA may be related to the lack of a hydrophilic to hydrophobic transition. There are not significant differences in the carbon signals for the cleaned samples. It is however interesting to note that the alcohol clean does not cause a increase in carbon levels. The fluorine signal is also reduced for the vapor cleans, although fluorine in the WF_6 gas source makes it difficult to determine the source of this contaminant. A direct comparison between the contamination levels shown in Tables V and VI cannot be made because of the differences related to the CVD encapsulation techniques used.

CONCLUSIONS

The vapor phase etch selectivity of native oxide relative to thermal and deposited oxides can be improved by diluting an azeotropic HF/H_2O source with H_2O or azeotropic HCl/H_2O. Anhydrous HF mixed with IPA as a solvent also has shown improved selectivity. The observed differences in selectivity are related to changes in both the etch rate and the delay time during which no etching takes place. SIMS encapsulation studies of contamination at the interface between a CVD film and a Si substrate are dependent on the pre-clean. The lowest contamination levels are found when vapor IPA is introduced into the vapor cleaning system.

Table IV. SIMS Epi-Encapsulation (at/cm^2).

CLEANING METHOD	OXYGEN	CARBON	FLUORINE
Wet HF with DI Rinse	2 e 13	1 e 13	< 1.7 e 9
Azeotropic HF/H_2O	1 e 15	4 e 13	< 1.7 e 9
Azeotropic HF/H_2O + IPA	1 e 12	2 e 12	< 1.7 e 9

Table V. SIMS Tungsten Silicide-Encapsulation (at/cm^2).

CLEANING METHOD	OXYGEN	CARBON	FLUORINE
No Clean	4 e 15	1 e 14	4 e 13
Wet HF with DI Rinse	4 e 13	6 e 13	1 e 13
Azeotropic HF/H_2O	5 e 13	5 e 13	1 e 13
Anhydrous HF + IPA	8 e 12	4 e 13	4 e 12

REFERENCES

1. J.M. de Larios, J.O. Borland, S. Hatada, I. Tamatani, International Conference on Solid State Devices and Materials (SSDM), p. 140, August 29 - September 1 (1993).

2. J.O. Borland, IEEE Bipolar/BiCMOS Circuits & Tech. Mtg., p. 67, (1992).

3. M. Wong, M. Moslehi, and R. Bowling, J. Electrochem. Soc., 140, 205 (1993).

4. C. Galewski, J. Lou, and W. Oldham, IEEE Trans. on Semi. Manuf., 3, 93 (1990).

5. J. Ruzyllo, K. Torek, C. Daffron, R. Grant, and R. Novak, J. Electrochem. Soc. 140, L64 (1993).

6. H. Watanabe, T. Tatsumi, S. Ohnishi, T. Hamada, I Honma, and T. Kikkawa, IEDM, Dec, 259 (1992).

7. M. Miki, H. Kikuyama, M. Maeno, J. Murota, and T. Ohmi, IEDM Tech. Dig, Dec. 730 (1988).

8. B.E. Deal, M.A. McNeilly, D.B. Kao, and J.M. de Larios, 36th Annual Technical Meeting of the Institute of Environmental Sciences, New Orleans, LA, April 23-27 (1990).

9. A. Izumi, T. Matsuka, K. Miya, T. Takeuchi, A. Yamano, J. Tsuchimoto, H. Itoh, and H. Abe, International Conference on Solid State Devices and Materials (SSDM), p. 534, August 29 - September 1 (1993).

10. B. Van Eck, S. Bhat, V. Menon, J. de Larios, and P. Haake, Microcontamination 92 Proceedings, p. 694, October 27-30 (1992).

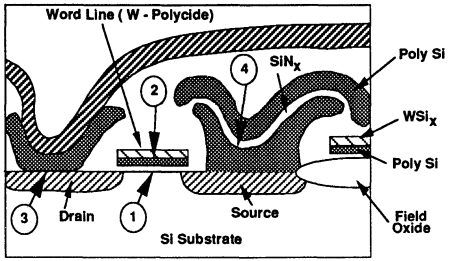


Fig. 1. Applications for HF vapor processing include: 1) Pre-gate Oxidation, 2) Pre-Silicide CVD, 3) Pre-Poly CVD, and 4)Pre-Nitride CVD [1].

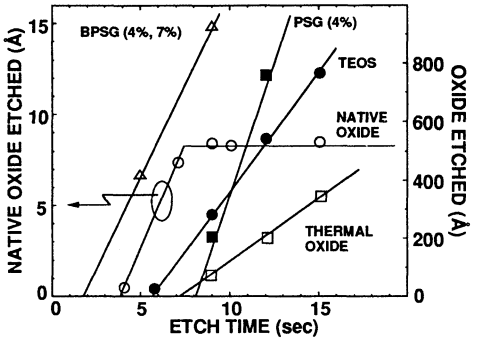


Fig. 2. Etch rate and delay times using azeotropic HF/H2O are strongly dependent on the oxide type.

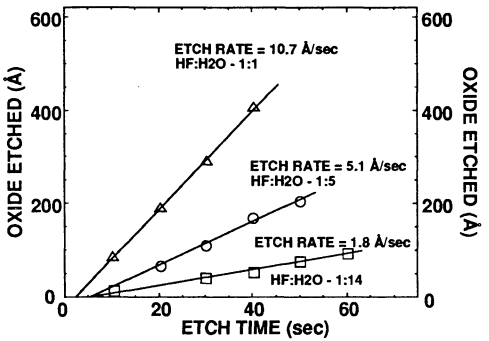


Fig. 3. The ratio of N2 carrier gas flows to the azeotropic HF/H2O and H2O sources has a large affect on the thermal oxide etch rate.

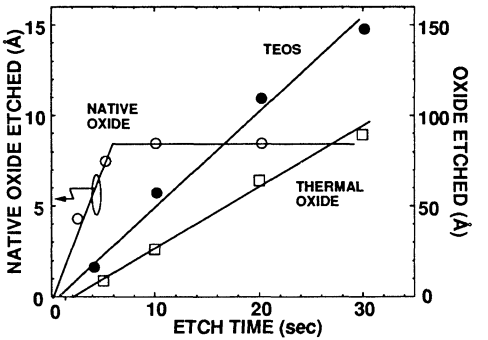


Fig. 4. Diluting the azeotropic HF/H2O source with a second H2O source improves the native oxide etch selectivity relative to TEOS and thermal oxide.

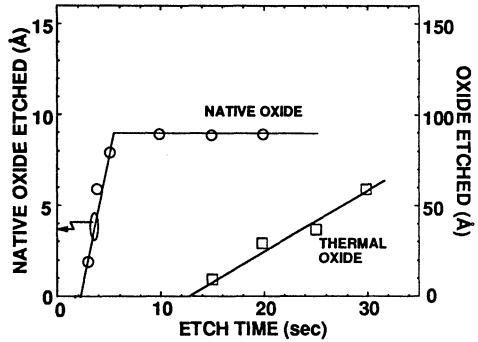


Fig. 5. Diluting the azeotropic HF/H2O with azeotropic HF/HCl increases the delay time of thermal oxide and allows selective removal of native oxide.

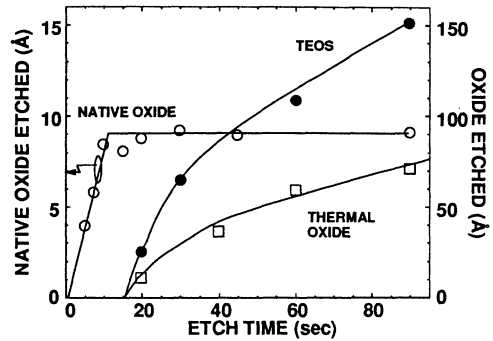


Fig. 6. Etch curves for thermal oxide, TEOS, and native oxide using anhydrous HF and IPA.

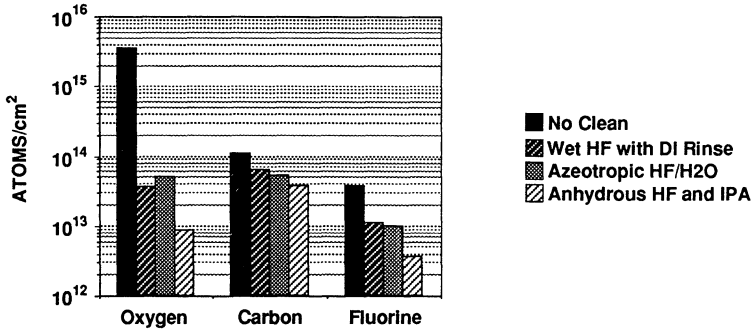


Fig. 7. SIMS data showing the effect of surface treatment on contamination levels at the tungsten silicide/Si interface.

IN-SITU SURFACE ANALYSIS IN HF VAPOR-PHASE CLEANING OF Si

D.J. Oostra and F.J.G. Hakkens
Philips Research Laboratories
P.O. Box 80.000
5600 JA Eindhoven
The Netherlands

HF/H_2O vapor phase cleaning of thermally oxidized Si is investigated in a high-vacuum compatible etch facility. The transition curve separating the pressure region of controlled etching from the region of very fast etching is determined as a function of HF and H_2O gas pressure. *In-situ* Auger electron spectroscopy (AES) and x-ray photo-electron spectroscopy (XPS) demonstrate that up to 10^{15} carbon atoms/cm^2 and to lesser extent O and F are present at the surface after gas-phase etching. The results indicate that C builds up after the etch process. Epitaxial Si and SiGe layers have been grown after etching by chemical vapor deposition (CVD) at temperatures as low as 600 °C. Channeling RBS measurements indicate a minimum yield as low as 2.7%, comparable with the minimum yield of bulk Si.

INTRODUCTION

HF/H_2O vapor phase cleaning has attracted much attention as a reliable way for reproducibly removing oxide layers from Si surfaces and creating a terminated, passive surface (1). Such a dry cleaning technique opens the way to integrated cluster-tools in which cleaning and subsequent processing of Si wafers takes place without intermediate exposure of the wafers to an uncontrolled atmosphere (2). Subsequent processing may involve poly-silicon deposition or re-oxidation for bipolar or MOSFET transistor fabrication, respectively. Another application is in the combination of this low-temperature cleaning with molecular beam epitaxy (MBE) or chemical vapor deposition (CVD) of Si and SiGe. In all these examples the state of the Si surface before the processing will influence the final interface. For example, residual organic or metal contaminants after the cleaning step will be incorporated at the interface. Knowledge of the state of the surface after the cleaning step and at the onset of the next processing step is thus extremely important. In this study we present preliminary results obtained on an experimental set-up dedicated for *in-situ* study of the state of the surface after cleaning. After the cleaning

process and/or analysis of the surface, samples can be processed further, without breaking the vacuum. In the case described below, Si and SiGe have been deposited by CVD.

EXPERIMENT

HF/H_2O vapor phase cleaning of Si has been investigated in a high-vacuum compatible etch facility, indicated in Fig. 1. Si samples (p-type, 25 Ωcm) with a thermal oxide of 100 nm are cleaned by introducing H_2O and HF vapor in a chamber made of HF resistant steel (Monel). Details on the etch chamber have recently been published (3). Samples can be transported via a gold-coated gate-valve into a high-vacuum cold-wall process chamber for low-pressure CVD (LPCVD) of Si or SiGe, or can be transported further to a chamber for Rutherford backscattering spectrometry (RBS) and Auger electron spectroscopy (AES) analysis, or to an analysis chamber for x-ray photo-electron spectroscopy (XPS). Etch rates have been obtained from the O and Si peak in RBS spectra obtained in the channeling geometry. In these experiments 2 MeV He^+ ions coming in normal to the surface in a 170° scattering geometry (10° between incoming and outgoing beam) have been used. The final state of the surface after etching has been investigated by AES and XPS. In AES 3 keV electrons have been used. Auger electrons have been analyzed in a single-pass cylindrical mirror analyzer (CMA). In the XPS experiments, Mg-Kα (1253.6 eV) radiation has been used. Photo-electrons have been collected in a double-pass CMA positioned at an angle of 30° with the surface normal of the sample. Survey scans have been made using a 100 eV pass energy, peak scans were obtained with either a 50 eV or a 25 eV pass energy. LPCVD has been performed immediately after etching the sample, without pre-baking. The LPCVD process employs SiH_4 and GeH_4 as source gases at pressures of about 100 mTorr.

RESULTS AND DISCUSSION

Etch Rates

HF/H_2O etch rates at room temperature of thermally grown SiO_2 have been determined at pressures varying between 1 and 10 Torr. From the obtained etch rates, the transition curve separating the region of controlled etching, with etch rates of a few nm/min, from the region of very fast etching, with etch rates of more than 100 nm/min, is determined. This transition curve is indicated in Fig. 2. In the region above the curve, 100 nm thermally grown SiO_2 is etched within 1 minute of exposure to H_2O and HF. For comparison,

the condensation curve as calculated by Helms and Deal (4) is included. Noticeably, the measured curve is less dependent on HF pressure than expected from the calculated condensation curve. An off-set between the curves is at least expected to be caused by our arbitrary definition of the transition curve. Furthermore, a substrate temperature somewhat different from that used in the calculation leads to differences in etch velocities because of changes in the ad- and desorption and reaction rates. However, parameters like dilution of the HF concentration during etching, the concentration of reaction products, and the state of the surface upon introduction may also play a role in the HF dependence.

Our experiments showed that contamination of HF gas, e.g. by a minute leak in the gas inlet system, causes the measured transition curve to move upward, i.e. to higher H_2O pressures. A point at the transition, like 7 torr H_2O and 1 torr HF, can therefore be used to check the cleanliness of the gas system.

AES Analyses

An example of AES analyses of the surface before, half-way, and after etching is indicated in Fig. 3. At the top a spectrum of a sample on which a 100 nm thick oxide layer has been grown is shown. Some carbon may be observed at the surface, probably caused by adsorbed hydrocarbons. After part of the oxide layer is etched in the controlled etch region with a gas mixture of 7 Torr HF and 3 Torr H_2O, the middle spectrum is obtained. This spectrum does not show any indication of contaminants. After etching the total oxide layer, the bottom spectrum is obtained. This spectrum demonstrates that after etching oxygen is still present at the surface and furthermore, that carbon is present. This final result is in agreement with the results of van der Heide *et al.* (1) and Ermolieff *et al.* (5) who observed with ex-situ XPS that after HF vapor phase cleaning of Si wafers C, O and F are present at the surface. However, contrary to the observations of van der Heide *et al.* (1), our results suggest that C builds up at the surface after the etching process. This C contamination is not present at the original SiO_2-Si interface, as checked by a depth profile AES analysis. Therefore we think that this C contamination is caused by adsorption of hydrocarbons from residual gases. This implies that a passivation of the Si surface against C build-up is not obtained. A similar conclusion was reached by Kasi *et al.* (6,7) after experiments in which they cleaned Si surfaces by a combined RCA clean and HF etch and subsequently exposed the surfaces deliberately to hydrocarbon contaminants. This C contamination indicates the need for clean processing or more elaborate passivation procedures. For example, wet HF/H_2O cleaning followed by UV-ozone cleaning is known to yield oxidized C-free surfaces (6-8).

The amount of F present at the surface cannot be measured with AES.

Therefore, an XPS analysis has also been performed on etched surfaces. The results obtained with this technique are discussed below.

XPS Analyses

An XPS survey scan obtained on a sample etched in 7 Torr HF and 3 Torr H_2O is shown in Fig. 4. The spectrum confirms that C, O and F are present at the surface. Detailed peak scans with a pass energy of 50 eV (not shown) have also been obtained. The results are in good agreement with the results of Ermolieff *et al.* (5). The F peak is relatively broad, which indicates two F bonding states, generally ascribed to Si-F and O-Si-F. Using the same procedure as Ermolieff *et al.*, *i.e.* with the sub-monolayer theory of Madey and Yates (9), modified by Carley and Roberts (10), the surface concentration of O, F and C has been obtained using:

$$\frac{I_m/S_m}{I_s/S_s} = \frac{M_s n}{A\rho\lambda\cos\theta} \qquad [1]$$

I_m, I_s, S_m, and S_s are the XPS peak intensities and Scofield's photo-ionization sensitivities (11) of the substrate material (s) and adsorbates (m), respectively. M_s is the molecular weight of the silicon substrate and ρ its mass density. λ is the electron mean free path of the Si(2p) electrons ($\sim$ 2.5 nm). θ is the angle between the normal of the surface sample and the detection line and A is the Avogadro number. This leads to a surface coverage of $9x10^{14}$ C/cm^2, $4x10^{14}$ O/cm^2, and $2x10^{14}$ F/cm^2. Noticeably, the carbon contamination is larger than that reported by van der Heide *et al.* (1). An analysis obtained several hours after etching indicated that the amount of C increases slowly at the cost of the amount of fluorine present. This suggests that Si-F bonds are exchanged by Si-C like bonds.

In our experiments, a similar amount of contaminants has been observed after etching samples in 3 Torr HF and 3 Torr H_2O, which suggests that the coverage by contaminants is not very dependent on the etch conditions.

Epitaxial Growth

The contaminants present at the surface do not impede epitaxial growth of Si and SiGe by LPCVD. After etching, Si samples were transferred to the reaction chamber, heated resistively to a temperature of 600 °C or higher and subsequently exposed to a pressure of 100 to 200 mTorr SiH_4 or SiH_4/GeH_4.

Figure 5 shows channeling-RBS measurements of LPCVD Si grown at 750 °C and as low as 600 °C. In both experiments the minimum yield at the surface is 2.7%, which is comparable to the minimum yield obtained on crystalline Si wafers, indicating epitaxial growth. It should be mentioned, however, that such a minimum yield is not a sufficient condition to obtain device-quality epi-layers.

CONCLUSIONS

In conclusion, HF/H_2O vapor phase cleaning of Si is investigated *in-situ* in a high-vacuum facility. First results obtained on etching of SiO_2 demonstrate that the transition of controlled to very high etch rates is less dependent on HF vapor pressure than expected. Furthermore, the transition appears to be sensitive to contamination of HF gas. After etching, C, and to a lesser extent, O and F are observed at the Si surface. The results indicate that the C contamination builds up after the etch process by adsorption of residual gases. This indicates the need for more elaborate cleaning and passivation steps, e.g. by additional UV-ozone cleaning. Still, the measured amounts of these contaminants are low enough to allow for epitaxial growth of Si or SiGe by LPCVD.

REFERENCES

1. P.A.M. van der Heide, M.J. Baan Hofman, and H.J. Ronde, J. Vac. Sci. Technol. A7, 1719 (1989).
2. C. Werkhoven, E. Granneman, L. Kwakman, M. Hendriks, S. Verhaverbeke, M. Heyns, and H. Bender, Mat. Res. Soc. Spring Meeting 1993.
3. A.E.T. Kuiper and E.G.C. Lathouwers, J. Electrochem. Soc. 139, 2594 (1992).
4. C.R. Helms and B.E. Deal, Journal IES, May/June, 21 (1992).
5. A. Ermolieff, F. Martin, A. Amouroux, S. Marthon, and J.F.M. Westendorp, Semicond. Sci. Technol. 6, 98 (1991).
6. S.R. Kasi, M. Liehr, P.A. Thiry, H. Dallaporta, and M. Offenberg, Appl. Phys. Lett. 59, 108 (1991).
7. S.R. Kasi and M. Liehr, J. Vac. Sci. Technol. A10, 795 (1992).
8. T. Kaneko, M. Suemitsu, and N. Miyamoto, Jap. J. Appl. Phys. 28, 2425 (1989).
9. T.E. Madey, J.T. Yates Jr. and N. E. Erickson, Chem. Phys. Lett. 19, 487 (1973).
10. A.F. Carley and M.W. Roberts, Proc. R. Soc. A363, 403 (1978).
11. J.H. Scofield, J. Electron Spectrosc. 8, 129 (1976).

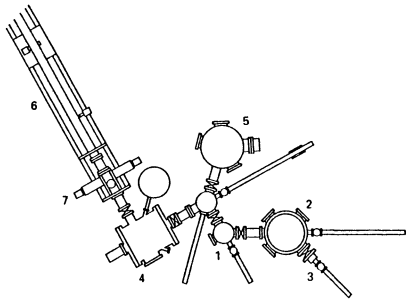


Fig. 1: Experimental set-up with load-lock (1), CVD chamber (2), HF/H_2O etch chamber (3), RBS and AES analysis chamber (4), and XPS analysis chamber (5). The last stage of the RBS ion beam line (6) is indicated, including the spot-defining slit section (7).

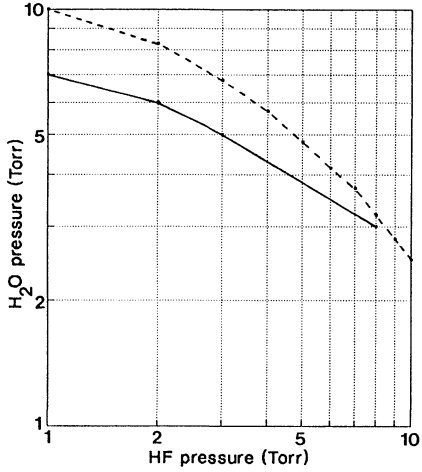


Fig. 2: Transition curve (solid line) separating controlled etch rates (nm/min) from very fast etch rates (>100 nm/min). The condensation curve as calculated by Helms and Deal (4) is also indicated (dashed line).

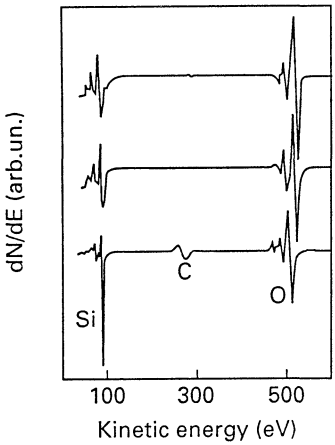


Fig. 3: Auger electron spectra before (top), during (middle) and after (bottom) etching of 100 nm SiO_2 on Si.

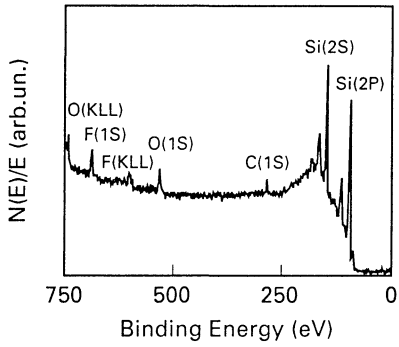


Fig. 4: XPS survey spectrum obtained after etching.

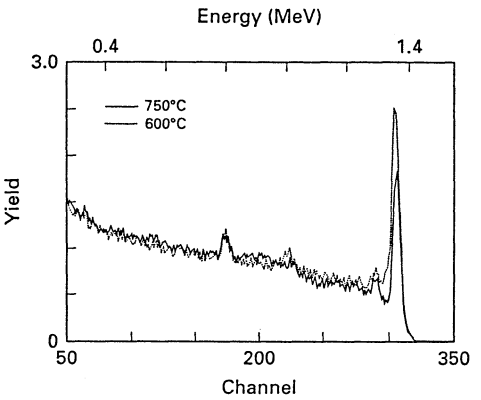


Fig. 5: Channeling-RBS spectra of LPCVD Si, deposited at 600 °C and 750 °C on Si(001).

VAPOR PHASE CLEANING OF POLYSILICON EMITTER AND TITANIUM SALICIDE STRUCTURES FOR 0.35 MICRON TECHNOLOGIES

Brynne Bohannon, Texas Instruments, Dallas, Texas 75265
Bob Witowski, SEMATECH, Austin, Texas 78741
Joel Barnett, FSI International, Austin, Texas 78746
Dan Syverson, FSI International, Chaska, Minnesota 55318

In an effort to advance device technologies, gas phase cleans are being developed by several researchers[1-4]. This study, supported by SEMATECH, Texas Instruments, and FSI International, evaluated vapor phase cleaning utilizing an FSI EXCALIBUR® MVP for application in a Phase III, 0.35 micron technology node, in attempt to identify cleaning advantages over conventional wet cleans. Two applications are reported, 0.6μm emitter diode pre polysilicon deposition clean for BiCMOS devices and pre-titanium deposition clean prior to salicide formation on 0.6μm polysilicon interconnects for BiCMOS and CMOS devices. The goal in this study was to accomplish technical parity or improvement in electrical performance of short loop test vehicles. The results of these tests are reported here.

INTRODUCTION

The applications selected for this study were chosen based on process sensitivity and/or desired improvements in electrical performance. In shallow emitter junctions, surface characteristics are critical in controlling electrical properties of the final transistor. Trace levels of metallic contamination can result in excessive leakage currents. Surface roughness as well as residual native oxides, can also influence emitter formation. In salicide processing the concerns are similar to emitter processing, although an increased sensitivity to particulate and/or oxide surface defects can result in poor selective silicide formation. A vapor phase approach to cleaning was selected by SEMATECH member companies for these critical applications based on demonstrated and perceived process advantages. FSI International was selected as supplier of the vapor cleaning system, an EXCALIBUR MVP (Multi Vapor Processing) system.

EXPERIMENTAL

Mixtures of hydrogen fluoride, hydrogen chloride and water vapor diluted in nitrogen are injected in the EXCALIBUR MVP system to reduce oxides and surface metallics on wafer surfaces. In addition to those gases, ozone generated from oxygen is injected to remove hydrocarbon or organic contamination. The clean is completed by brief dispenses of

de-ionized water, removing water soluble residual metal chlorides and fluorides. The system controller allows logical sequences and/or combinations of the above mentioned chemistries. Processes are carried out one wafer at a time at approximate atmospheric pressure and ambient temperatures. Figure 1 depicts the system used in the study and the cross section of the process chamber where reactive gases are injected and water rinsing takes place.

Wafers used in this study for metric characterization, as well as substrates for building short loop test structures, were 150 mm P type <100> silicon with a nominal resistivity of 15 ohms/square. Metallic contamination removal was determined by intentionally contaminating substrates by resist ashing technique[5] and analyzing using a Rigaku Total Reflectance X-ray Fluorescence (TXRF) analyzer. Surface roughness measurements of the cleans were determined using a Digital Instruments Nanoscope III Atomic Force Microscope (AFM). Design of experiment (DOE) methodologies were used to model the vapor process effects on etch rates, uniformities and selectivities of various oxides, as well as metallic ion contamination removal. Where appropriate, processing parameters were borrowed from a parallel program at AT&T to reduce characterization time. The initial focus was to not exceed oxide loss targets for each application. Once completed, this "etch" process became the foundation for construction of recipe sequences to be used in the application splits. Variations in the exposure time to HCl and ozone were the primary considerations in the split designs. Each application would compare vapor processes to the in-house standard aqueous clean over the course of 3 to 4 short flow split lots. The intentions at outset were to progressively reduce the number of splits to one or two final vapor processes. However, due to schedule priority, lots were required to be processed in parallel, therefore not allowing progressive refinement.

A cross sectional diagram of the short flow diode structure is indicated in Figure 2. The various cleans were performed prior to low pressure chemical vapor deposition of polysilicon. The test structure and criteria used to characterize diodes were as follows: (1) Junction leakage information was collected from N+/P moat block diodes (Figure 3) with a LOCOS edge. Diode area was $1.45 \times 10^{-3}/cm^2$ with a perimeter of 0.17 cm. Each die contained 1250 diodes. Leakage is reported as the reverse current at 0.5 volt bias. (2) Van der Pauw structures (Figure 4) were used to determine single point 0.6μm diameter polysilicon to silicon contact resistance. Contact chain structures with 4960 chained contacts (Figure 5) were used to determine cleaning effects on high density structures. The resistance for both resistance structures was determined by the voltage drop produced with an injection current of 1.0×10^{-3} amps.

Figure 6 depicts the cross section of the titanium salicide structure. Cleaning required the removal of approximately 100Å thermal oxide from an implant anneal on 3750Å polysilicon prior to deposition of 600Å titanium. Initial silicide was produced in forming gas at 585°C followed by a low pressure anneal at 750°C after titanium strip. Resistivity of interconnect polysilicon was measured using a constant length (760μm x 0.6μm) resistor bridge (Figure 7). A serpent and comb structure (Figure 8) provided continuity and bridging yield informa-

tion on serpentines 19460μm long, 0.6μm wide, with 1.2μm spacing. In all testing each wafer contained 24 die which were probed by an automated probe station. All collected data was then analyzed using Statistical Analysis Software (SAS).

RESULTS AND DISCUSSIONS

Analytical Data

Experimental design studies indicated that metallic contamination removal did not model well with experimental results, therefore, decisions on processes were based on best oxide selectivities and uniformities that produced wafers with residual metallics below detection limits for TXRF. Figure 9 reveals average surface metals detected by TXRF of various wafers, including control wafers (as received), contaminated wafers (after resist ash), and two vapor cleans with and without HCl added. Intentional contamination of wafers produced metal levels in excess of 1 x 10^{13} atoms/cm^2. Vapor HF processes followed by short rinse and dry reduce metals. However, the more noble metals are not completely removed. The addition of HCl gas to the vapor process clearly produces a cleaner wafer surface when compared to using vapor HF alone. All detectable metals are reduced below detection limits of approximately 1 x 10^{10} atoms/cm^2.

A short study was performed to determine the surface roughness characteristics of the various cleans that would be used in the comparisons. Sample wafers were exposed to aqueous HF dips and vapor cleans with and without HCl. As can be seen in Table 1, no significant differences are found between cleans evaluated.

Table 1: Surface roughness characteristics of various cleans compared to control wafers.

PROCESS	RMS (Å)	$R_{average}$ (Å)
Control	1.73	1.34
10% HF 60" dip - rinse/dry	1.67	1.32
1% BHF 45" dip - rinse/dry	3.96	1.50
1% BHF 90" dip - rinse/dry	1.68	1.33
Vapor HF - rinse/dry	1.55	1.21
Vapor HF + HCl - rinse dry	1.35	1.03

Emitter Diode Results

Vapor processes were selected from the general characterization work. The desire was to produce a native oxide free "clean" surface, therefore, variations on the HF-HCl-R/D scheme were used. Ozone, although desirable, was left out of the study due to contamination problems produced by the ozone generator. The first lot, #1151, was split into four

different vapor cleans which were compared to the process of record, a 45" 1% BHF dip followed by a 10 minute rinse-dry (Table 2). All of the splits, except vapor split #4, were preceded by a reversed RCA clean [(HCl + H_2O_2 + H_2O) - (NH_4O_4 + H_2O_2 + H_2O)].

Table 2: Pre-polysilicon emitter diode clean matrix.

Process of record	90" 1% $BHF_{(Aq)}$ - 10' Rinse - Dry
EMIT 1	5" 0.2% HF + 3.3% HCl - Rinse/Dry
EMIT 2	5" 0.2% HF + 3.3% HCl - 7" HCl purge - 10" HCl + Rinse - Rinse/Dry
EMIT 3	5" 0.2% HF + 3.3% HCl - 7" HCl purge - 10" HCl + Rinse - Rinse/Dry
EMIT 4*	5" 0.2% HF + 3.3% HCl - 7" HCl purge - 10" HCl + Rinse - Rinse/Dry
* No pre-furnace RCA clean used	

The results of the first lot, #1151, are graphed in Figures 10 and 11 plotting junction leakage and single point contact resistance. The data indicates that no significant differences were found in junction leakage, although a minor reduction in distribution is realized. From the Van der Pauw structures, all four vapor splits produced lower contact resistance and smaller variations than the wet HF dip process, with the best vapor process producing approximately 1300 ohms resistance. The net conclusion was to reduce the vapor splits from four to two, selecting EMIT 1 and EMIT 3 to be applied to the remaining lots.

Based on good results from lot #1151, EMIT 1 and EMIT 3 were chosen for the next two lots, 9947 and 1070, to further compare with the standard wet HF process. Similar effects were observed, that is, no significant difference in junction leakage with slight reductions in leakage distribution (Figure 12), and lower single point contact resistance and distribution (Figure 13) for both vapor cleans. Contact chain resistance data collected on these two lots are plotted in Figure 14. In this case, vapor clean EMIT 1 provided the lowest resistance and smallest error, followed by EMIT 3 and then the standard wet clean, possibly an indication that the etch process in EMIT 3 was not as robust as EMIT 1 in removing oxides and residues generated in high density contact chains. Yield data (Figure 15) extracted from the contact chain structures reveal significant differences between the vapor cleans and the wet processes with EMIT 1 yielding 100% on both lots.

Emitter Cleaning Discussion

In this comparison, it was found that none of the cleans had a significant effect on average junction leakage, although slight improvements in distribution were realized when processed using vapor. Data from contact resistance measurements of polysilicon to single cystal silicon indicated that the vapor process was consistent in reducing interface resistance

with slight improvements in distribution. Contact chain resistance was lower and yield was higher for one of the vapor cleans evaluated, EMIT 1. This improvement is possibly due to the addition of HCl to the etchant chemistry allowing the removal of a small amount of sub-oxide or silicon layer which could impede intimate contact. Reasons that may explain the poor distribution of the wet clean and higher contact resistance may relate to the high probability of non-uniform wetting of thousands of contacts followed by subsequent extensive water rinsing allowing re-oxidation of the silicon.

Titanium Salicide/Polysilicon Results

The objectives in this application are to remove the oxide formed on polysilicon during an anneal and produce sheet resistivity of less than 5 ohms/□ or better than the standard wet clean. The standard wet process is a 90 second 1% buffered HF immersion followed by a 10 minute DI water rinse and then spin dry. Four lots were processed with each splitting the standard clean to various vapor cleans (Table 3).

Table 3: Pre-titanium silicide clean matrix.

Standard wet clean	90 sec. 1% buffered HF - 10' rinse/dry
SIL 1	5" 0.7% HF - 10" R/D (rinse dry)
SIL 2	30" 12% $_{(w)}O_3$ - 20" 1.7% HF etch - 10" R/D
SIL 3	5" 0.7% HF + 3.3% HCl etch - 10" R/D
SIL 4	30" 12% $_{(w)}O_3$ - 5" 1.7% HF + 3.3% HCl etch - 10" R/D

The target sheet resistivity of 5 ohms/□ was met for all cleans including the standard clean (Figure 16). The most significant difference between the standard and the vapor cleans was improved standard deviations, primarily in SIL 1 and SIL 3. SIL 2 and SIL 4 both utilized the ozone process. It was discovered later that these processes were not purging the ozone sufficiently, therefore allowing re-oxidation of the polysilicon after etching the oxide. This may account for the higher distributions on these vapor splits. Average yield from the serpent and comb structures (Figure 17) indicates that all vapor cleans performed slightly better than the wet clean with SIL 2 producing the highest yield at 100% across two lots.

Titanium Salicide Clean Discussion

In this study, all cleans exceeded the objective of 5 ohms/□ polysilicon sheet resistivity. Two cleans SIL 1 and SIL 3 produced tighter resistivity distributions, possibly due to the elimination of water marks that can be found with most wet processes and reductions in rinse times from 10 minutes to 10 seconds. More study is required, to fully understand the distribution differences of various cleans.

CONCLUSION

From this study it can be concluded that vapor phase cleaning, when compared to wet cleaning, exceeded our expectations of technical parity on 0.35μm devices. We have demonstrated surface metallic impurity removal without increasing surface roughness of silicon. Emitter clean work based on short loop diodes identified two vapor processes that improved junction leakage distribution and significantly lowered contact resistance. Chain structures also indicated lower contact resistance and higher yield when using the vapor process. In the salicide study, the two vapor cleaning processes tightened resistivity distributions over the standard wet clean and produced slightly higher yield. The improvements in polysilicon contact resistance and polysilicon sheet resistivity will lend itself well to the objectives of emitter and salicide processing where minimization of these attributes is important.

ACKNOWLEDGMENTS

The authors would like to acknowledge the efforts of the late Mike Gordon who performed all surface analytical work. We would also like to acknowledge Annette Martin for system operation and data collection, Caryn Morris and Gracie Jenkins for lot inspection, as well as equipment support by Tim Vaughn and Dan Gay.

REFERENCES

1. R. Sugino, M. Okuno, M. Shigeno, Y. Sato, A. Ohsawa, T. Ito, and Y. Okui, The Electrochemical Soc., Pennington, N.J., Proc. Vol. 92-12, 1992, pp. 72-79
2. J. C. Ivankovits, D. A. Bohling, A. Lane, and D. A. Roberts, The Electrochemical Soc., Pennington, N.J., Proc. Vol. 92-12, 1992, pp. 105-111
3. S. Bedge, G. A. Ruggles, and H.H. Lamb, The Electrochemical Soc., Pennington, N.J., Proc. Vol. 92-12, 1992, pp. 112-121
4. D.B. Kao, B.R. Cairns, B. E. Deal, The Electrochemical Soc., Pennington, N.J., Proc. Vol. 92-12, 1992, pp. 251-259
5. B. Witowski, Proceedings of the Institute of Environmental Sciences, May, 1991

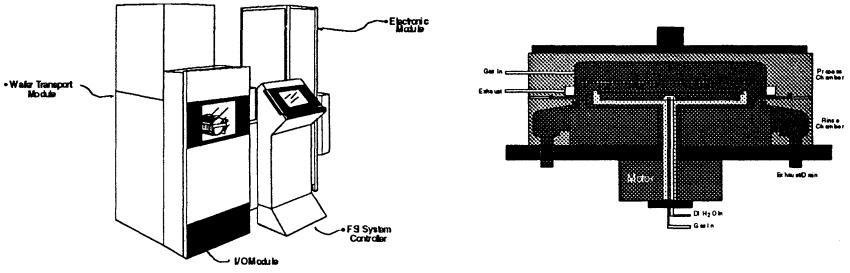


Figure 1: Vapor cleaning system and cross sectional diagram of process chamber.

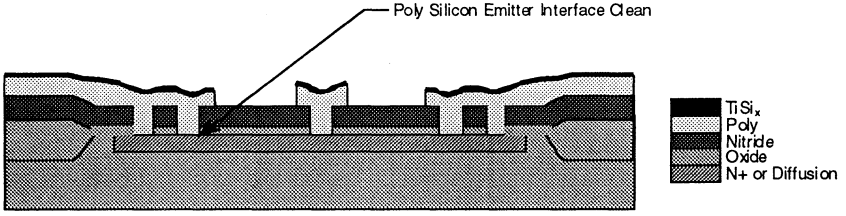


Figure 2: Cross section of diode test structure used in for study of pre polysilicon deposition cleans.

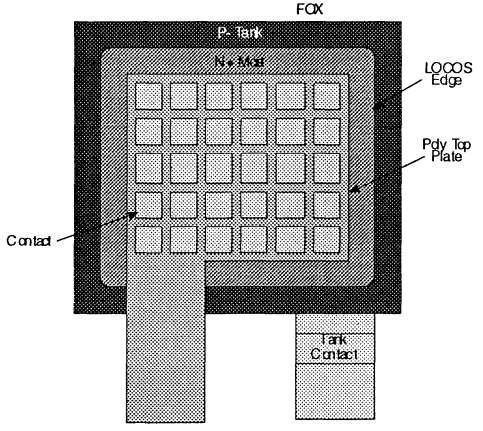


Figure 3: Moat block diode array for junction leakage data collection.

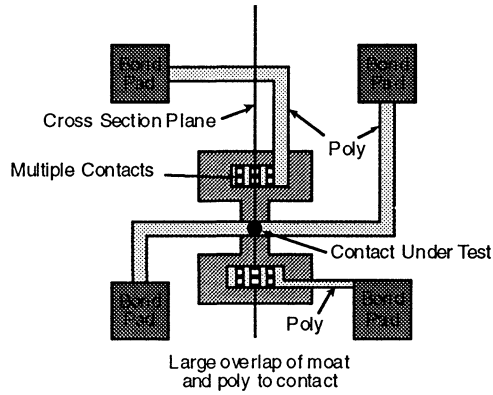


Figure 4: Van der Pauw structure for measuring single point contact resistance.

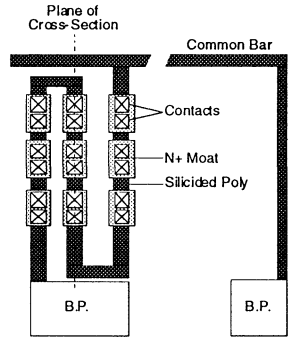


Figure 5: Contact chain structure for collecting chain resistance and yield data.

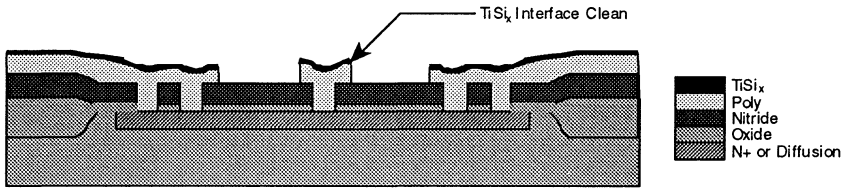


Figure 6: Cross section of polysilicon structure used for the study of pre titanium salicide cleans.

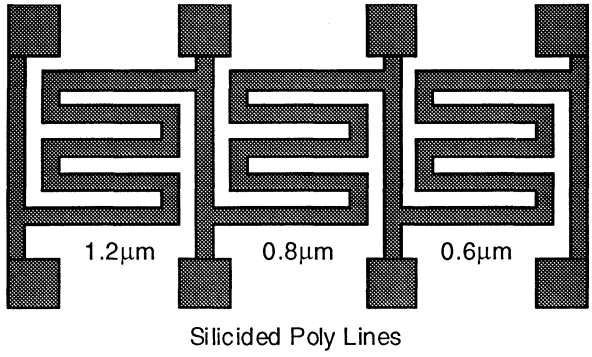


Figure 7: Constant length resistor bridge for measuring sheet resistivity.

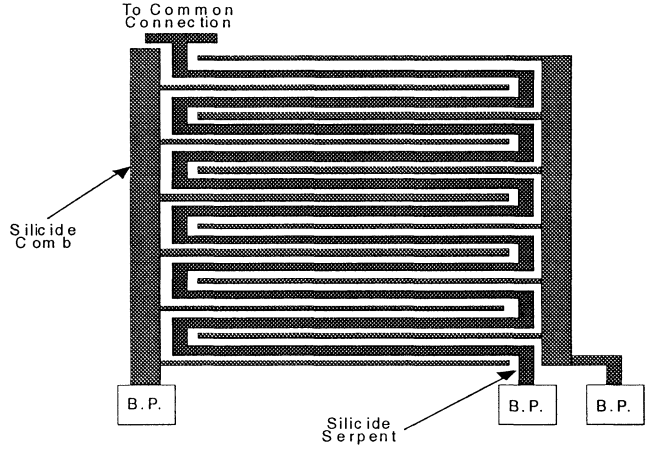


Figure 8: Serpentine and comb structure for measuring bridging and continuity.

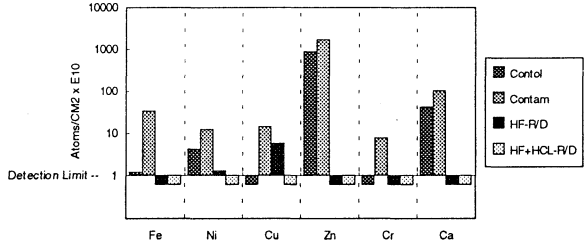


Figure 9: The effect of various vapor cleans on surface metallic contamination.

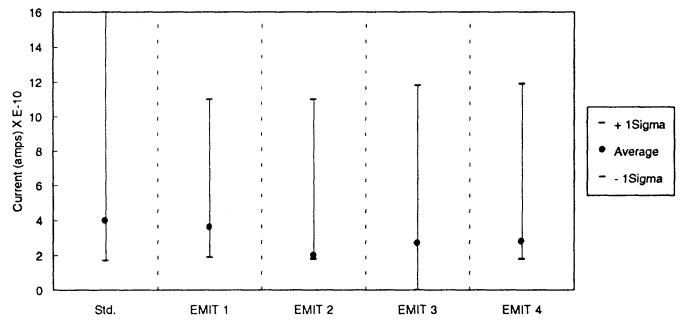


Figure 10: Junction leakage data from lot 1151.

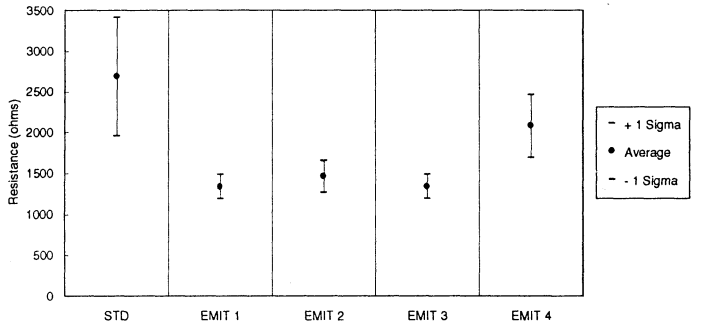


Figure 11: Single point contact resistance data from lot 1151.

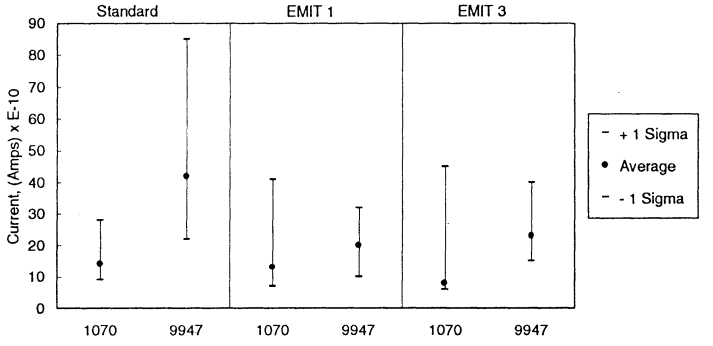


Figure 12: Junction leakage from lots 9947 and 1070.

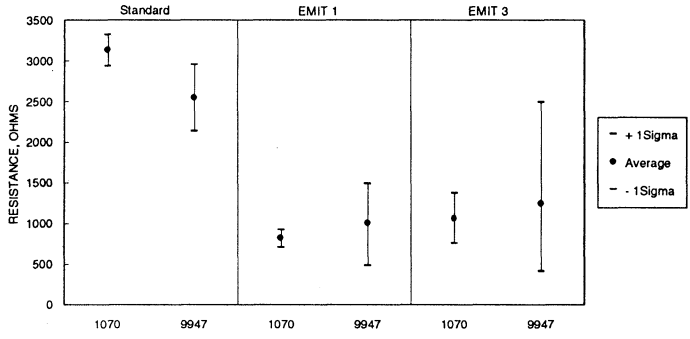


Figure 13: Single point contact resistance from lots 9947 and 1070.

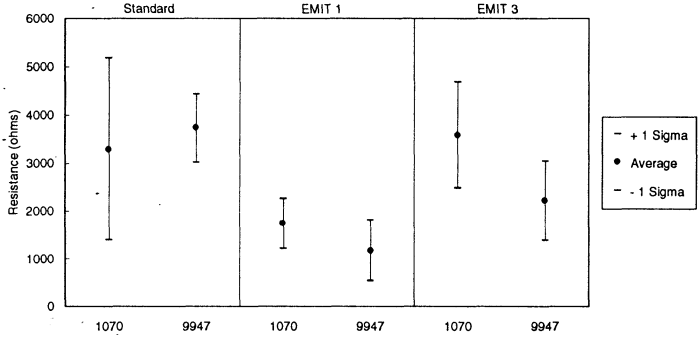


Figure 14: Contact chain resistance data on lots 9947 and 1070.

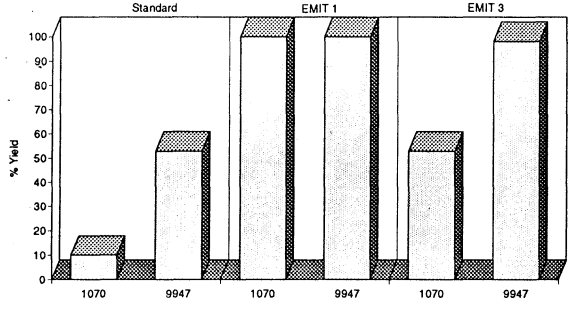


Figure 15: Contact chain yield data on lots 9947 and 1070.

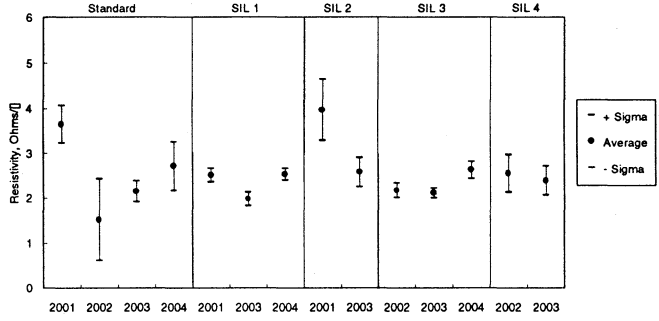


Figure 16: Sheet resistivity data titanium salicide polysilicon for lots 2001 - 2004.

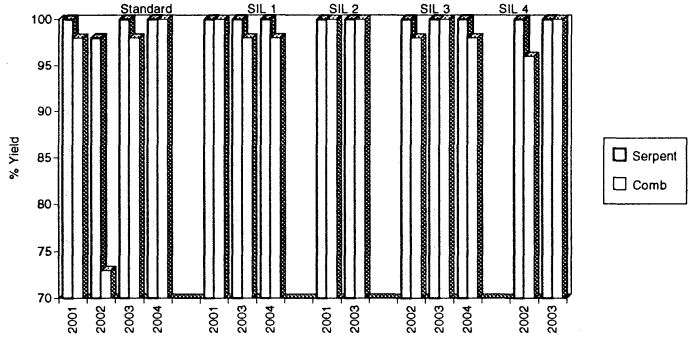


Figure 17: Serpent and comb structure yield after salicide formation for lots 2001 - 2004.

GAS-PHASE ETCHING OF SILICON OXIDE WITH ANHYDROUS HF AND ISOPROPANOL

Jeffery W. Butterbaugh, C. Fred Hiatt and David C. Gray
FSI International, Chaska, MN 55318

The ability to clean the surface of a silicon wafer in a vacuum environment with gas-phase reagents has been identified as a key technology for the production of sub-half-micron integrated circuits. One step of the cleaning process is the removal of native oxide before gate oxidation, epitaxial growth, or metal deposition. In this study the etching of silicon oxide with a gas-phase mixture of anhydrous HF, isopropanol and nitrogen was investigated in a single-wafer reactor. Reactor pressures up to 150 torr and wafer temperatures up to 50 °C were investigated. Over a relatively small parameter space, oxide etching rates greater than 800 Å/minute were obtained. The etching characteristics were examined as a function of pressure, flow rate, wafer temperature and feed gas composition. The importance of water to the etching reaction was also investigated. It is unclear whether isopropanol itself takes part in the etching reaction, or if it simply enhances the etching reaction between silicon oxide, HF, and water.

INTRODUCTION

Wafer cleaning during integrated circuit (IC) manufacturing is a critical part of the production cycle and accounts for approximately 60% of the time required to manufacture the IC. Shrinking critical dimensions, thinner dielectric film thicknesses and larger chip sizes cause even greater challenges for cleaning processes. As feature sizes approach 0.25 microns and smaller, even trace amounts of contamination from organics, metal ions, and native oxides will drastically reduce process yields and raise production costs. The most common way to prepare wafers for oxide growth, epitaxial layer growth and other film deposition is to perform a final critical cleaning step just prior to introducing the wafers into the growth reactor. However, most wafer cleaning processes involve wet chemicals and wafer surfaces can become contaminated during the transfer from the cleaning process to the reactor.

Atmospheric, vapor-phase, HF/H_2O processes are currently being implemented for silicon wafer cleaning and the removal of native oxide from the silicon surface (1,2). This type of process significantly reduces chemical usage and disposal problems over traditional wet bench and spray processes. However, due to the nature of the process (non-vacuum, water vapor) it is difficult to integrate into a vacuum cluster. A method

must be developed which will clean the wafer in a dry environment so that it can be transferred directly into a vacuum system for subsequent film growth and deposition processes.

The current process being investigated is the removal of silicon oxide with a gas-phase mixture of anhydrous HF and isopropyl alcohol (IPA) in nitrogen. Removal of native oxide is just one cleaning step that is needed for pre-gate or pre-deposition wafer conditioning. Cleaning processes for the removal of organic, metallic and particulate contaminants as well as final conditioning of the wafer surface also must be developed.

Aqueous mixtures of HF and alcohol have been under investigation for pre-oxidation cleans in the past (3). Researchers found an improvement in the electrical properties of thin oxide films grown on silicon after aqueous HF/ethanol cleaning (4). Work has been reported on silicon oxide etching with HF/methanol mixtures in an atmospheric, vapor-phase reactor, as well (5). Atmospheric, vapor-phase HF/methanol was reported to provide much better native oxide:BPSG selectivity than vapor phase HF/H_2O.

More recently, Ruzyllo *et al.* reported on the use of methanol with HF in a vacuum chamber for etching silicon oxide (6). That work was analogous to the work reported here, except that methanol was used instead of IPA. Ruzyllo *et al.* found a significant enhancement to the oxide etching rate with the addition of methanol to the feed gas (via a bubbler). The oxide etching rate with the HF/methanol system was found to be strongly dependent on the wafer temperature and reactor pressure. Many of the dependencies reported by Ruzyllo *et al.* for the HF/methanol system were found in the current study of the HF/IPA system.

Currently, the details of the mechanism by which alcohol takes part in, or enhances, the reaction of HF with silicon oxide are not understood. It is possible that water is still an important reactant in the etching processes and that the addition of alcohol enhances either water adsorption or the reaction of water with HF and silicon oxide. In order to determine the importance of water as a reactant it is necessary to remove water completely from the HF/alcohol system. However, this is difficult due to the nature of the mid- to high-vacuum reactors used for this process and also because water is a product of the reaction of HF with silicon oxide. Nevertheless, an attempt was made in this work to determine the importance of water in the HF/alcohol silicon oxide etching process.

EXPERIMENTAL

The experimental reactor is a vacuum chamber which can accommodate wafers up to 200 mm in diameter. Reactive gases are fed through stainless steel tubing and are evenly distributed in the reactor. The volume of the reactor is variable. The wafer is heated and the wafer temperature is measured by thermocouples which contact the back side. A dry pump is used to evacuate the chamber to a base pressure of a few tens of millitorr.

A quadrupole residual gas analyzer (RGA) is used to sample gases from the reactor exhaust or from the reactor feed gases. A long sampling line is required (about 1 m) due to physical limitations of the apparatus, but a sampling assist pump is used near the RGA sampling orifice to minimize the residence time of sample gases in the sampling tube. A needle valve at the RGA end of the sampling tube controls the pressure in the RGA. The RGA is controlled by a PC and has the capability of automated library searches and scan analysis which was used to get a rough idea of the alcohol and water concentration in the bubbler feed gas stream. This analysis is only roughly quantitative since it does not take into account relative cracking probability and sensitivity of various species.

Anhydrous HF is fed to the reactor through heated lines and a heated mass flow controller. IPA is fed to the reactor by passing dry N_2 through a reservoir of liquid IPA at room temperature. The N_2/IPA stream can also be run through a cartridge of type 3A molecular sieves to remove any moisture from the stream. RGA analysis indicates an IPA concentration of approximately 4% in the nitrogen carrier gas emerging from the bubbler containing 100% IPA. With a mixture of 50% water and 50% IPA in the bubbler, the nitrogen carrier contains about 2% IPA and 1.5% water as it exits the bubbler. With 100% water in the bubbler, they nitrogen carrier contains about 2 % water. With only dry nitrogen flowing through the reactor at 100 torr, about 0.2% background water is measured at the exhaust.

The etching rate was measured with thick oxide films grown on 150 mm p-type (100) silicon wafers. 4000 angstrom thermal oxide films were grown at 1000 °C. The oxide thickness was measured before and after etching at 49 points on the wafer with a Prometrix Spectramap SM200/e. Uniformity of etching was calculated as one standard deviation of the 49 points divided by the mean, also known as the coefficient of variance (COV).

The dependence of the oxide etching rate was measured as a function of total flow rate, pressure, wafer temperature, feed gas composition, and reactor volume. Oxide etching rate was also measured as a function of added water by flowing the bubbler stream with and without the molecular sieve and also by adding water to the IPA bubbler (figure 1).

RESULTS AND DISCUSSION

Figure 2 illustrates the relative stability of the process over both a 2-day period and a 20-day period during which the system was down for maintenance. For the first two pairs of runs on the first day there appeared to be a second wafer effect, but on the second and twenty-third day this effect was not seen. Wafers were placed in the chamber by a load lock robot so the chamber was under vacuum between process runs. A possible explanation for variations in etching rate is variable water partial pressure in the reactor due to the production of water by the reaction process.

Figure 3 shows the dependence of etching rate on wafer temperature. As the wafer temperature is increased above room temperature, the etching rate decreases significantly. This is similar to the temperature dependence of HF/H_2O vapor etching reported by Wong and coworkers (2). In the case of vapor-phase etching, the temperature dependence was explained by the need for a water condensate layer on the wafer surface in order for the etching reaction to proceed (2). A similar mechanism may also dominate in the HF/IPA process as suggested by Ruzyllo *et al.* (6). Under vacuum conditions it is possible that the etching reaction and product desorption are relatively fast causing reactant adsorption to be a rate-limiting step. Higher wafer temperature would decrease the rate of adsorption leading to a lower surface concentration of reactants and a decrease in the reaction rate.

Etching rate increases dramatically with an increase in total reactor pressure from 50 to 150 torr as shown in Figure 4. This pressure dependence is another characteristic of an adsorption-limited surface reaction. The pressure and temperature dependencies of the etching rate with the HF/IPA system are similar to those with the HF/methanol system as reported by Ruzyllo *et al.* (6). In fact, the etching rates for the two systems at similar conditions (40 C, 100 torr) are almost identical.

In another set of experiments the HF fraction in the feed gas was varied while holding the total flow and IPA concentration relatively constant. Figure 5 shows the effect of HF fraction while the IPA concentration was held at about 2%. The oxide etching rate is roughly proportional to the HF concentration under these conditions. Increasing etching rate with increasing total pressure and increasing HF fraction (both of which increase the HF partial pressure) is consistent with a rate-limiting step of HF adsorption.

Also indicated in Figure 5 is the very low etching rate (less than 5 Å/minute) when IPA is not included in the feed gas. At this time, more detailed data on the dependence of etching rate on IPA fraction is not available. It appears that above about 2% IPA in the feed gas mixture the etching rate is independent of the IPA fraction.

Considerable effort was made to eliminate water from the process chamber in order to determine the importance of IPA, itself. RGA analysis indicates a baseline level of water in the chamber which is difficult to remove due to the relatively high base pressure of the reactor. With 100% IPA in the bubbler, there was no detectable difference in water concentration of the feed gas with and without the molecular sieve. The etching rate of thermal oxide films also showed no significant difference with the molecular sieve being used as opposed to not being used (see Figure 6). However, this only indicates that the affect of water which is introduced by the alcohol bubbler is below the threshold of the background water already in the process chamber. In the future a turbomolecular pump will be used to reduce the base pressure of the reactor.

Water was also added to the reactor by mixing the IPA with water in the bubbler and also by totally replacing the IPA with water. With a 50% IPA, 50% water mixture in the bubbler added water was measurable by RGA. RGA analysis was also able to show that the molecular sieve was trapping added water out of the bubbler stream (Figure 7a). Figure 7a also shows that the sieve must first become saturated with IPA before a steady IPA concentration is reached at the output.

Figure 7b shows RGA analysis of the gases leaving the reactor during an etching process. As the HF flow is started, the evolution of SiF_4 is clearly seen as the intensity at m/e=84 increases (this peak corresponds to SiF_3^+ and should actually be at m/e=85). At these conditions the residence time in the reactor is about 1 minute, which correlates well with the rise time seen in the HF concentration. It is apparent from Figure 7b that water is an important reaction product in the HF/IPA oxide etching process.

A summary of experiments performed with and without added water is shown in Figure 6. It is clear that alcohol significantly enhances the oxide etching rate above that obtained by just adding water to the process. Once alcohol is added to the process it is unclear whether added or background water is still important since water cannot be totally eliminated from the process.

SUMMARY

The dependence of HF/IPA oxide etching on process parameters was measured and shown to agree well with data reported for the HF/methanol process (6). The HF/alcohol oxide etching process appears to HF-absorption limited. An attempt was made to establish the relative importance of water and alcohol in this study. While the enhancement of thermal oxide etching rate with alcohol addition is again confirmed, it is unclear whether water is still an important contributor to the etching reaction. Further investigations of the importance of water are being made in a high vacuum apparatus so that initial water concentrations can be carefully controlled and monitored.

ACKNOWLEDGMENTS

This work was funded in part by a grant from the National Institute of Standards and Technology, Advanced Technology Program. The authors would also like to acknowledge the work of Larry Zimmerman and Roger Gifford on the collection and analysis of experimental data.

REFERENCES

1. M. Wong, M.M. Moslehi, and D.W Reed, *J. Electrochem. Soc.*, **138**(6), 1799 (1991).

2. M. Wong, M.M. Moslehi, and R.A. Bowling, *J. Electrochem. Soc.*, **140**(1), 205 (1993).

3. J.L. Prom, J. Castagne, G. Sarrabayrouse, and A. Munoz-Yague, *IEE Proc. I*, **135**(1), 20 (1988).

4. J.L. Prom, P. Morfuli, K. Kassmi, G. Pananakakis, and G. Sarrabayrouse, *IEE Proc. G*, **138**(3), 321 (1991).

5. A. Izumi, T. Matsuka, T. Takeuchi, and A. Yamano, *Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, eds. J. Ruzyllo and R. Novak, **ECS Proceedings 92-12**, 260 (1992).

6. J. Ruzyllo, K. Torek, C. Daffron, R. Grant, and R. Novak, *J. Electrochem. Soc.*, **140**(4), L64 (1993).

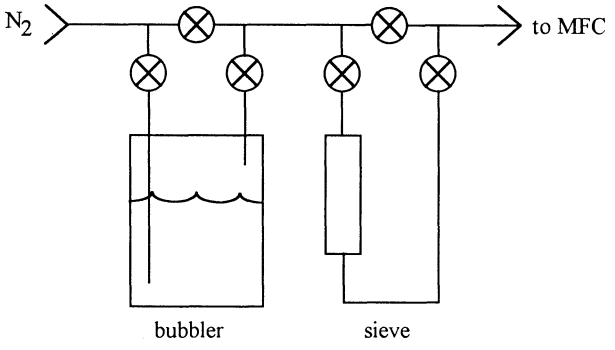


Figure 1. Schematic of bubbler/sieve manifold. Valves allow for the independent bypassing of the bubbler and/or the sieve.

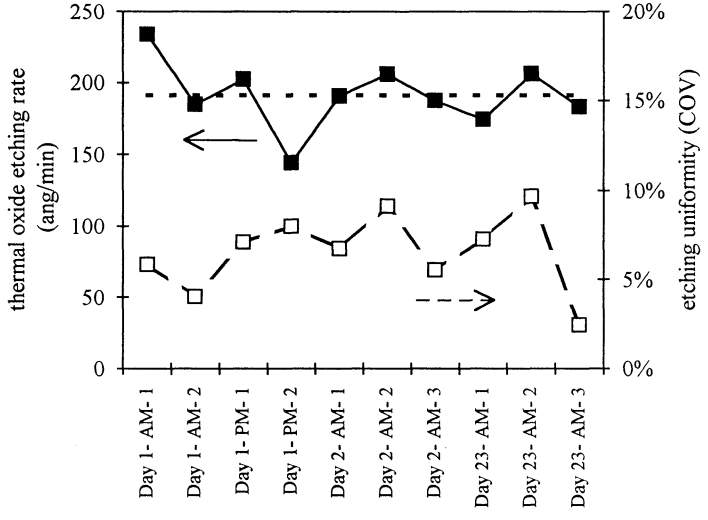


Figure 2. Etching rate repeatability and uniformity at 40 C and 100 torr. (average rate = 191.3 Å/minute, std. dev. rate = 23.5 Å/minute)

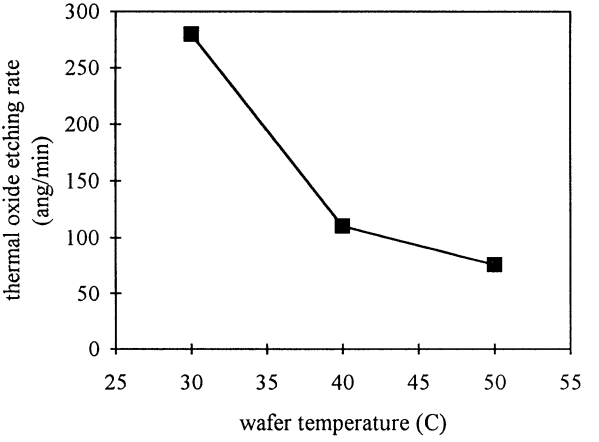


Figure 3. Dependence on wafer temperature (1000 sccm N_2/IPA; 500 sccm HF; 1000 sccm N_2; 100 torr).

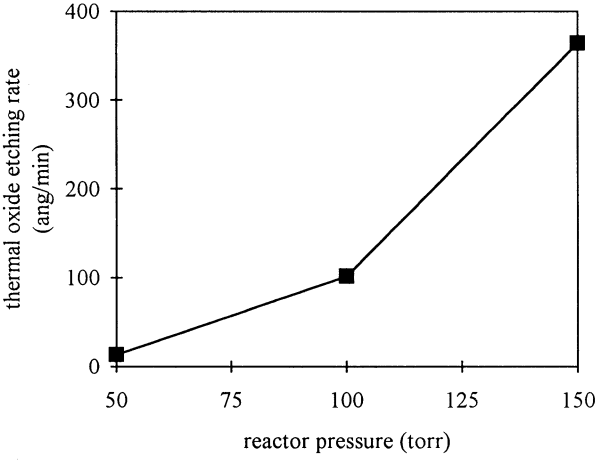


Figure 4. Dependence on pressure (500 sccm N_2/IPA; 250 sccm HF, 500 sccm N_2; 40 C).

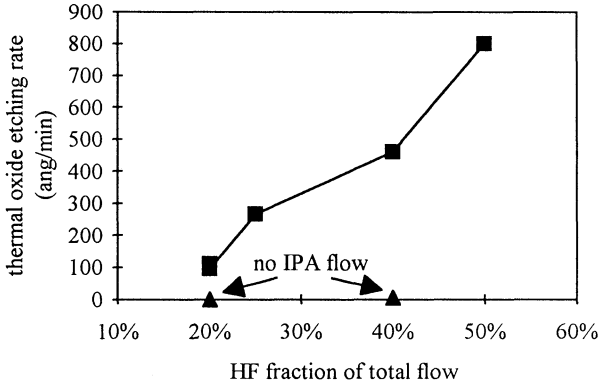


Figure 5. Dependence on HF fraction (1000 sccm N_2/IPA; 2000-2500 sccm total flow; 40 C; 100 torr).

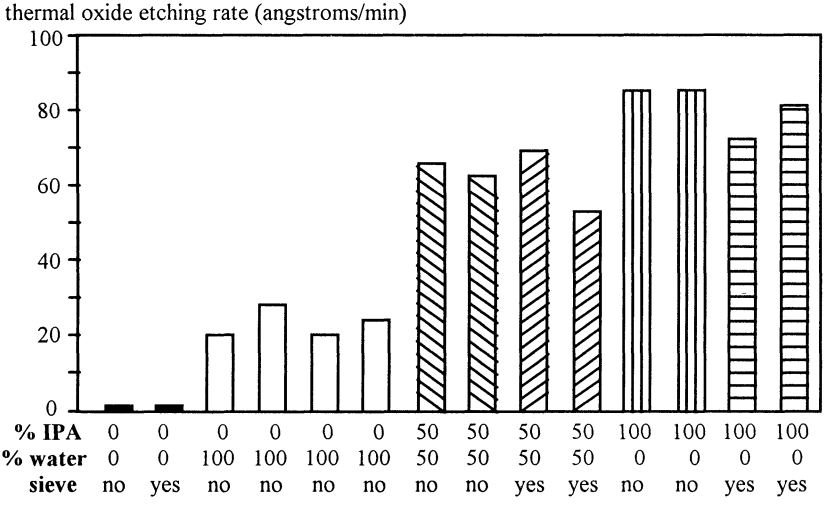
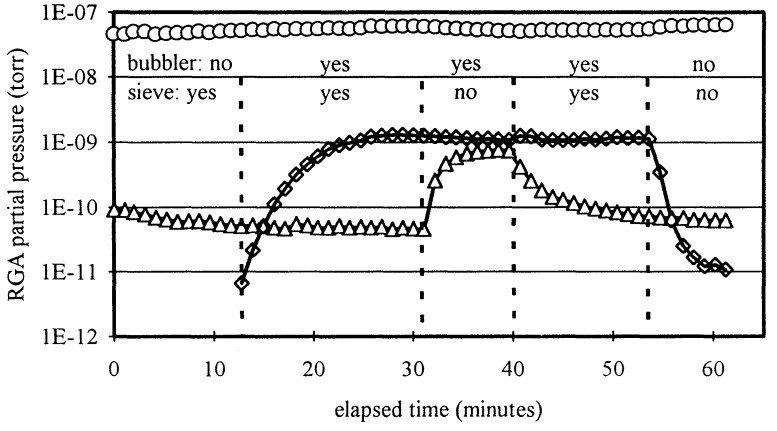


Figure 6. Dependence on added water (125 sccm through bubbler manifold; 175 sccm HF, 200 sccm N_2; 40 C; 100 torr). Bar labels indicate the liquid composition in the bubbler and whether or not the gas stream through the bubbler was routed through the molecular sieve (see figure 1).

(a)



(b)

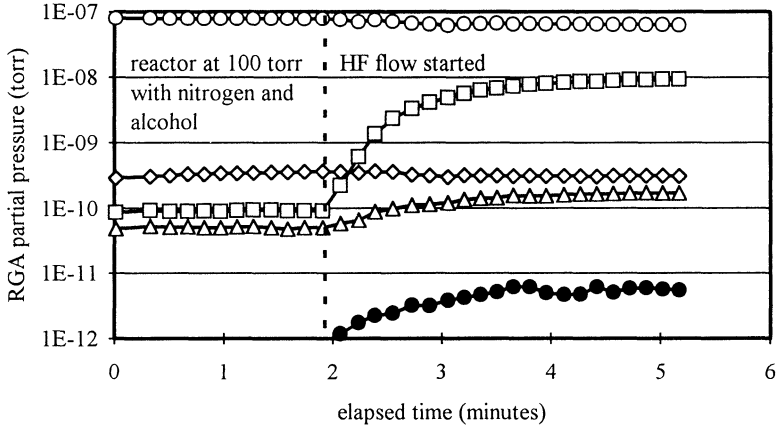


Figure 7. (a) RGA analysis of nitrogen gas stream from bubbler containing 50% IPA and 50% water. Different combinations of flow through the bubbler and sieve are shown (see figure 1). (b) RGA analysis of exhaust gases during an etching run. Plotted peaks include m/e=28, N_2^+ (O), m/e=18, H_2O^+ (Δ), m/e=45, IPA fragment (◊), m/e=20, HF^+ (□), and m/e=84, SiF_3^+ (●). (the peak for SiF_3^+ should actually occur at m/e=85)

SILICON SURFACES EXPOSED TO ANHYDROUS HF/CH_3OH ETCHING

Kevin Torek and Jerzy Ruzyllo
Electronic Materials and Processing Research Laboratory
The Pennsylvania State University
University Park, PA 16802

Emil Kamieniecki
QC Solutions, Inc.
Lexington, MA 01821

Anhydrous HF/CH_3OH has been demonstrated to be a viable method for native/chemical oxide etching. After the oxide etch, the silicon surface activity was studied using XPS, surface charge analysis, and contact angle. SCA and contact angle results for anhydrous HF/CH_3OH etching are compared with those obtained using liquid HF/H_2O solution. The surface activity after anhydrous HF/CH_3OH oxide etching was found to be sensitive to process parameters. Intermediate formation of water during oxide etching is believed to play an important role in determining the silicon surface activity following anydrous HFCH_3OH oxide etching.

INTRODUCTION

HF-last RCA cleaning is being intensely studied for ULSI applications. One feature of such cleaning is the chemical passivation of bare silicon by aqueous HF etching under proper conditions. Failure to chemically passivate the bare silicon surface against oxidative attack results in the silicon becoming partially covered with a native/chemical oxide film of uncontrolled thickness when the unprotected material comes into contact with oxygen and moisture. Such contaminant films degrade the quality of material systems which depend on a clean interface, such as epilayers, silicide, contacts, polysilicon emitters, and MOS gate insulators.

In this study, oxide etching by anhydrous HF/CH_3OH, originally proposed by Izumi et. al. (1), is being investigated as part of a future cluster tool compatible cleaning technology in which the oxide etch takes place at reduced pressure and elevated temperature. The feasibility of this approach was confirmed in our initial investigation (2). One aspect of this experiment is the characterization of the silicon surface following anhydrous HF/CH_3OH oxide etching. Specifically, the Si surface activity following anhydrous HF/CH_3OH oxide etching is evaluated as a function of process parameters. Surface Charge Analysis (SCA) and contact angle measurements are the tools chosen for tracking surface activity. The activity of the silicon surface from which native/chemical oxide was etched using anhydrous HF/CH_3OH is compared to that resulting from a dilute HF:H_2O native/chemical

oxide etch. SCA and contact angle measurements are well suited for surface monitoring since no further processing other than native/chemical oxide etch is required.

EXPERIMENTAL

In this work, a prototype commercial reactor (3) is used to implement the anhydrous HF/CH_3OH process (Fig. 1). Briefly, HF, purified N_2, and CH_3OH-laden N_2 are fed through mass flow controllers into the reactor. Methanol is contained in a temperature-controlled bubbler. Wafer temperature and reactor pressure are controlled by IR lamps and a dry mechanical pump.

P-type (100) Si wafers were used as shipped. The condition of the silicon surface following native/chemical oxide etching was monitored at regular intervals using SCA and contact angle measurements. For SCA measurements, samples were biased into accumulation first. Two SCA parameters were used to monitor re-oxidation: $\Delta Q_{ox\text{-}acc}$ and IQF_{acc} .$\Delta Q_{ox\text{-}acc}$ is the hysterisis in the depletion width vs. induced charge plot in the accumulation region. This hysterysis has been attributed to slow states at the silicon surface. IQF, interface quality factor, is defined as (4):

$$IQF = \frac{dQ_{ind}}{dQ_{sc}} \qquad [1]$$

and is directly proportional to interface trap density D_{it}:

$$D_{it} = \left[\frac{\varepsilon_s}{q^2 W_d}\right] \bullet [IQF - 1] \qquad [2]$$

where Q_{ind} is the induced charge, Q_{sc} is the depletion charge, ε_s is the silicon permittivity, and W_d is the depletion width. IQF_{acc} is the value of IQF evaluated during the sweep from accumulation towards depletion when the Fermi level is at midgap. Low IQF_{acc} values are obtained on electrically passivated silicon surfaces. For passivated surfaces, lower $\Delta Q_{ox\text{-}acc}$ values indicate thicker oxide, while the opposite is true for IQF_{acc} (4). High initial surface activity, on the other hand, results in increasing $\Delta Q_{ox\text{-}acc}$ with ambient air exposure time. The behavior of IQF_{acc} is the same for either initially passive or initially active surfaces. For contact angle measurements, 20 µl water droplets were dispensed onto the samples and photographed after 1 minute. Contact angle was measured from the pictures to about ± 2° (5). A 2 minute HF(1):H_2O(10) immersion followed by a 1 minute rinse was used as a control for SCA measurements. For contact angle measurements, the HF was diluted to HF(1):H_2O(100) and wet etch without any rinse was used as the

least active surface. While the use of different HF:H_2O ratios in the SCA and contact angle experiments may result in differing surface activities for the two wet etch standards, the surface activity trends with varying anhydrous etch paramaters may still be compared using the different wet etches as the "standard" surface activity for the different analytical techniques.

RESULTS AND DISCUSSION

XPS spectra of anhydrous HF/CH_3OH etched surfaces show indirect evidence of silicon surface passivation by hydrogen in that F_{1s}, O_{1s}, and C_{1s} peaks are very weak (2). For HF:H_2O etching, post-etch surface activity depends on HF concentration. It follows that, by varying anhydrous HF/CH_3OH etch parameters, it should be possible to control surface activity, similar to liquid HF and vapor HF etching (6). SCA and contact angle measurements were used to rapidly evaluate the effects of various anhydrous HF/CH_3OH etch parameters on surface activity.

The shape of the SCA plot of W_d versus Q_{ind} and its evolution with ambient air exposure time is illustrated in Fig. 2. A single SCA measurement consists of three bias sweeps. The first sweep, towards accumulation, traces out the lines in the lower right-hand side of the figures. The second sweep, into depletion, traces out the lines in the upper half of the figures, and the final sweep traces out the lines in the lower left of the figures. Figure 2a shows W_d vs. Q_{ind} curves for a dilute HF dip with water rinse (HF(1):H_2O(200) for 2 minutes + H_2O rinse for 1 minute) taken 3, 23, 36, 49, and 59 minutes after etching. $\Delta Q_{ox\text{-}acc}$ decreases as the native/chemical oxide becomes thicker, consistent with previous observations (7). The slow states resulting in $\Delta Q_{ox\text{-}acc}$ are believed to be associated with defects identified with ionized silicon atoms (8). IQF_{acc} increases as the silicon-native/chemical oxide interface becomes more electrically active. This IQF_{acc} increase may be due to a decrease in the hydrogen passivation of the bare silicon wafer. Figure 2b shows the same curves for an anhydrous HF/CH_3OH etch process taken 80, 179, 230, 327, and 445 minutes after etching. The evolution of these curves is generally different from those in Fig. 2a. Decreasing positive surface charge results in the curves shifting to the left with time. Also, IQF_{acc} for the anhydrous HF/CH_3OH etch decreases with time. Increasing $\Delta Q_{ox\text{-}acc}$ and decreasing IQF_{acc} indicate an initially weakly passivated silicon surface becoming passivated with native/chemical oxide.

While the curves in Fig. 2b indicate an incompletely passivated surface after that particular HF/CH_3OH etch recipe, the evolution of $\Delta Q_{ox\text{-}acc}$ and IQF_{acc} is in general sensitive to the anhydrous HF/CH_3OH etch parameters. A more detailed evaluation of surface activity trends following anhydrous HF/CH_3OH etching utilizes the unique capabilities of the reactor used in this study. Process variables included N_2 flow rate through the bubbler (methanol flow rate), etch time, and HF flow rate. Pressure, temperaure, and total flow were held constant at 300 Torr, 60°C, and 1550 SCCM.

The effect of methanol flow rate on surface activity is shown in Figs. 3 and 4 via IQF_{acc} and contact angle measurements. As noted earlier, different HF:H_2O dilutions were used in the different experiments but the anhydrous etch trends are directly comparable. The trend is toward less activity with more methanol flow, with activity reaching a minimum at 1300 SCCM. Figure 4 shows that the least active surface was achieved for an HF(1):H_2O(100) dip and N_2 blow dry without any rinse. However, when followed by a 1 minute rinse the aqueous etch results gives rise to a more active surface. The rinsed surface, which is more realistic based on safety, is at least as active as an anhydrous HF/CH_3OH etched surface where 1500 SCCM methanol flow rate was used.

The effect of etch time on surface activity is depicted in Figs. 5 and 6. The activity of anhydrous HF/CH_3OH etched surfaces appear to reach a minimum for a 3 minute etch under the conditions indicated in Fig. 5. The 3 minute, 500 SCCM methanol flow rate etch, figures 5 and 6, resulted in IQF_{acc} and contact angle evolution similar to the 1 minute 1500 SCCM methanol flow rate etch, figures 3 and 4.

Finally, the effect of HF flow rate on surface activity following the oxide etch was evaluated. Methanol flow rate and etch time were held at 500 SCCM and 1 minute while HF flow rates of 58, 40, 20, and 10 SCCM were used. The trend is towards less active, more hydrophobic surfaces as the HF flow rate is reduced from 58 to 10 SCCM. This is a confirmation of results discussed earlier, showing less active surfaces for higher CH_3OH/HF flow ratio, except instead of increasing CH_3OH flow, HF flow was decreased with the same general effect on surface activity.

Interpreting the variation of surface activity with etch parameters necessitates a consideration of the etch mechanism. In general, anhydrous HF + vapor oxide etching, with various condensible gases including methanol, occurs through a thin condensed layer on the oxide surface. The elevated temperature and reduced pressure capabilities of the system used in this study allow great control over this condensed layer. A direct study of the thickness, composition, and uniformity of this layer has not yet been undertaken. In addition, no effort was made so far to directly detect native/chemical oxide etch endpoint.

While we do not have direct chemical or endpoint information, we conjecture that intermediate H_2O generated by the etch reaction plays an important role in determining the stability of the bare silicon surface, especially in light of the effect rinsing had on the surface activity of the wet etched sample. Higher methanol flow rate may result in less H_2O being present during the final stage of etching, which may result in lower surface activity for the higher CH_3OH flow rates. Similarly, for the 500 SCCM methanol process, longer times can be expected to result in less H_2O being present during the final stage of etching. For the 500 SCCM, 1 minute etch, the lower surface activity with lower HF concentration in the incoming gases may be analagous to the case of aqueous oxide etching where lower surface activity is obtained for oxides removed by highly diluted aqueous HF etching than for those removed by concentrated solutions.

CONCLUSIONS

Overall, the anhydrous HF/CH_3OH etching yields a range of silicon surface activity depending on etch parameters. Less active surfaces were obtained for recipes using a higher methanol/HF flow rate ratio and longer overetch. Changes in the state of the Si surface can be readily monitored using SCA and contact angle measurements. The activity of silicon surfaces following anhydrous HF/CH_3OH etching was compared with that of silicon surfaces after aqueous HF etching. The anhydrous HF/CH_3OH etch was found capable of producing a bare silicon surface less active than that produced by a dilute aqueous HF etch with H_2O rinse. We propose that the formation of water during anhydrous HF/CH_3OH etching plays an important role in determining the activity of bare silicon surfaces following various anhydrous HF/CH_3OH etch recipes.

Surface charge analysis reveals that initially passivated bare silicon surfaces evolve in a manner differing both qualitatively and quantitatively from those on surfaces not initially passivated. The differences in surface charge evolution reflect the different chemical and electrical changes taking place on the silicon surface.

ACKNOWLEDGEMENTS

This project was supported by the Semiconductor Research Corporation under contract number 92-MJ-274. Thanks are also due to SubMicron Systems, Inc. for providing the tool used in this study.

REFERENCES

1. A. Izumi, T. Matsuka, T. Takeuchi and A Yamano, in Cleaning Technology in Semiconductor Device Manufacturing/1992, J. Ruzyllo and R. E. Novak, Editors, PV 92-12, p. 260, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1992).
2. J. Ruzyllo, K. Torek, C. Daffron, R. Grant, and R. Novak, J. Electrochem. Soc., 140, L64 (1993).
3. Cluster Clean SP-200, SubMicron Systems, Inc.
4. E. Kamieniecki, Semicon/Europa 91 Technical Proceedings, (1991).
5. Procedure adopted after S. Verhaverbeke.
6. A. Philipossian, J. Electrochem. Soc., 139, p. 2956 (1992).
7. E. Kamieniecki and J. Faggiato, Handbook of Silicon Wafer Cleaning Technology, ch. IV.-3, Ed. W. Kern, Noyes Publications (1993).
8. B. E. Deal, J. Electrochem. Soc. 121, 198C (1974).

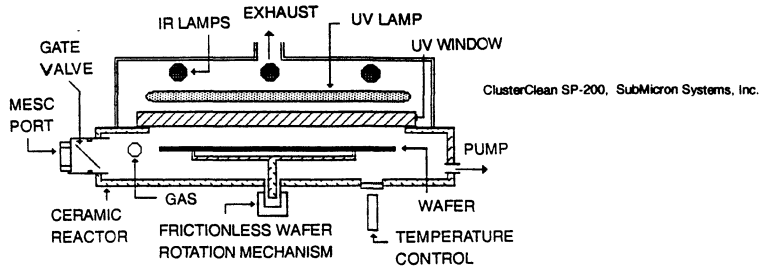
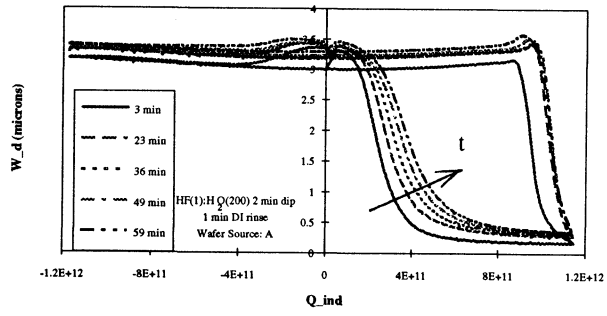
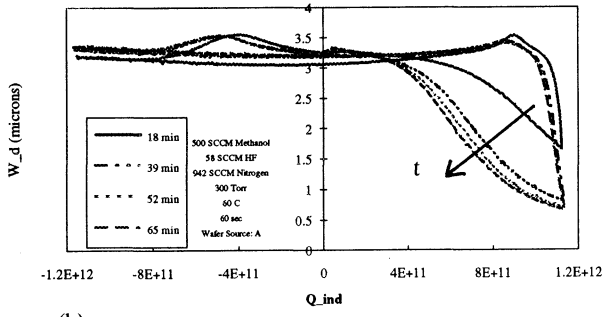


Fig. 1. Prototype commercial clusterable cleaning reactor used in this study.



(a)



(b)

Fig. 2. SCA vs ambient air exposure time (t) for:
(a) dilute HF(1):H_2O(100) 2 min. dip and 1 min. rinse, and
(b) an anhydrous HF/CH_3OH etch process.

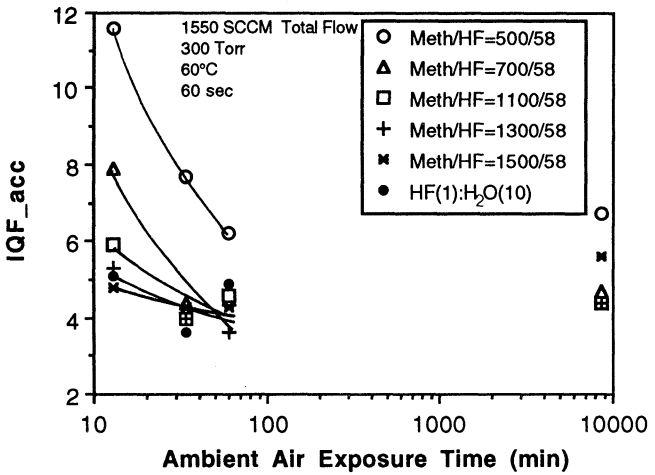


Fig. 3. IQF_{acc} vs. time for different CH_3OH flow rates.

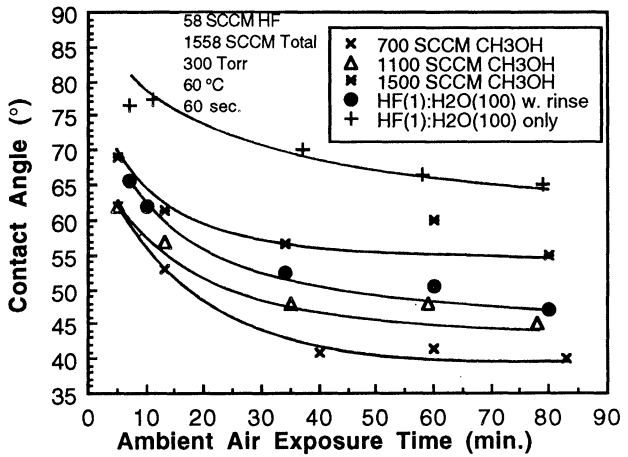


Fig. 4. Contact angle vs. time for different CH_3OH flow rates.

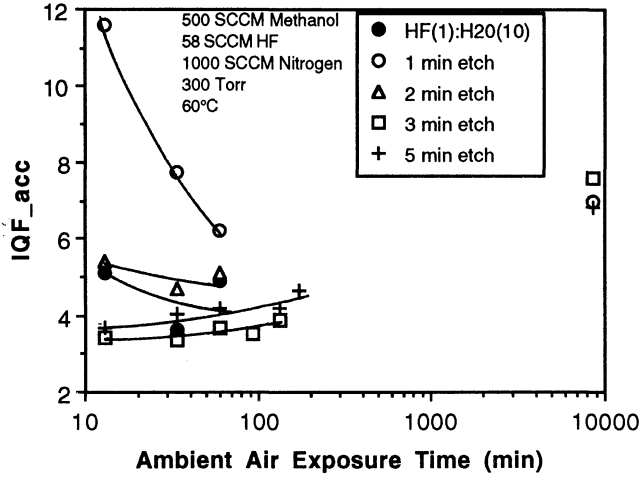


Fig. 5. IQF_{acc} vs. time for different etch times.

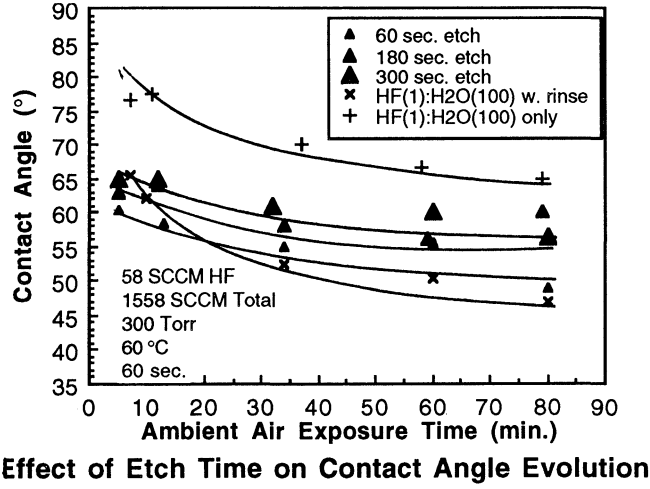


Fig. 6. Contact angle vs. time for different etch times.

COMPARISON OF VAPOR-PHASE AND WET CHEMICAL PRE-GATE OXIDE & PRE-CONTACT CLEANS

C. W. Draper and V. E. Anyanwu
AT&T Engineering Research Center
Princeton, NJ 08542-0900

J. H. Eisenberg, G. J. Felton, P. K. Roy, S. Chittipeddi & P. F. Bechtold
AT&T Bell Laboratories
555 Union Boulevard
Allentown, PA 18103

G. Hagner, D. Cooper & D. Syverson
FSI International
Chaska, MN 55318-1096

B. Witowski, B. Van Eck & M. Gordon
SEMATECH
Austin, TX 78741

We report the results of an evaluation comparing wet chemical and vapor-phase cleaning of the pre-gate oxide and pre-contact levels. The gate oxide is a 9 nm CMOS application, while the pre-contact clean is at the titanium silicide level prior to the titanium and aluminum alloy thin film depositions. The vias are 1μm in diameter with BPTEOS and TEOS dielectrics. Results for modular (zone) tester lots indicate that improved or equivalent performance can be achieved with the vapor-phase clean.

INTRODUCTION

During the later part of 1992 SEMATECH established Project E42, a Vapor-Phase Cleaning Applications Development Program, which utilized the resources of AT&T Bell Laboratories, Texas Instruments, FSI, International and SEMATECH to evaluate the readiness of vapor-phase cleaning for specific cleaning requirements. The TI portion of this project will be reviewed in a separate paper in the proceedings. Following the completion of the SEMATECH defined project in December, 1992, AT&T and FSI, International continued the evaluation of vapor-phase cleaning through August, 1993. This report will primarily review our findings for the two specific applications defined by the SEMATECH project, however, we have enhanced the data base upon which these evaluations are made by including the additional data collected during the extension into 1993.

The two targeted CMOS process technology applications were pre-gate oxide cleaning technology and pre-contact cleaning. We have opted to treat each application as a complete subject within the subheadings that follow the experimental section of this report. Brief descriptions of the application, the standard clean, desired attributes, zone tester and electrical data will be included. The extent of the discussion is constrained by the page count limits placed in proceedings papers. We conclude with a summary of our findings.

EXPERIMENTAL

The vapor-phase equipment used in the work described here was an Excalibur II beta-site vintage prototype. The Excalibur II tool is a single wafer vapor-phase processing unit offering anhydrous HF and HCl, 0_3, and H_20 vapor. HF is also available for backside wafer processing. Chemical etching, cleaning, insitu rinsing and drying can all be achieved with great recipe flexibility through the *Windows* environment of the computer interface. A typical recipe sequence includes the following steps: chamber load, purge, one or more chemical dispenses, purge, rinse/dry, purge and chamber unload.

The work described here was accomplished inside the AT&T Bell Laboratories Device Development Line (DDL) in Allentown, PA. During the course of the vapor-phase evaluation the primary function of this cleanroom was completion of the development of 0.5 m technology. The timing of the SEMATECH project was such that the pre-gate application was evaluated with a nominally 9 nm gate oxide, 0.5 μm technology short loop zone tester, and the pre-contact application was evaluated with a 0.9 μm technology window/via short loop zone tester. All the experiments were conducted with 125 mm wafers.

Monitor wafers for light scattering events (*particle counts*) were either SEH or MEMC wafers fresh from the shipping containers. These were not reused, but instead used as substrates for the oxide etch uniformity studies after oxidation. The etch studies were all based on a 20 nm etch target from a 100 nm dry thermal oxide wafer. The work horse metrology instruments used were the Tencor 6200 Surfscan for light scattering events and Prometrix 200 for oxide film thicknesses. All TXRF was accomplished at SEMATECH utilizing commercial Rigaku instrumentation. SIMS and ESCA were done in Bell Labs with a Perkin Elmer PHI-6300 and PHI-5400 respectively.

PROCESS DEMONSTRATION

A subset of the process demonstrations apply directly when attempting to interpret the electrical results described later in this paper, and so we very briefly review them here.

Particle adders (all LSC counts >0.2 μm) were determined for 125 mm Si monitor wafers (with typical initial counts <5) exposed to a standard 5 sec, 0.2 LPM HF chemical dispense followed by insitu spin rinse and dry. Within days following installation the particle adders were <25. During three extended reproducibility studies <5 adders per wafer were found over an extensive data base. A chamber cleaning recipe was developed that quickly returned the particle counts to acceptable levels following routine and unscheduled maintenance or following episodic particle bursts.

Etch uniformity (% 1 sigma/mean) for all categories (lot-to-lot, wafer-to-wafer and within wafer) was determined for a nominally 20 nm etch from a 100 nm thermal oxide. The etch uniformity was studied in three extended reproducibility studies and sampled with monitor wafers during the course of the complete 18 months. With the exception of lot to lot, the etch uniformities were all < 2%. The lot-to-lot was <5%, and the larger variability most likely may be attributed to differing furnace oxides and wafer storage conditions.

TVS data confirmed mobile ion levels below 1 x 10^{10} cm^{-2}. Transition metal contamination removal was measured using monitor wafers coated and ashed with photoresist. The test methodology is described in reference 1. Figure 1 is a bar graph summary of the TXRF data for six elements and four wafer conditions. The relatively high Zn and Ca levels are characteristic of this vendor's monitor wafers. Following the ashing of the photoresist Fe, Ni, Cu and Cr levels between 10^{11} and 10^{12} are typical. The particular asher used was a conventional oxygen plasma barrel asher, however we have found this data to be representative of downstream and ozone photoresist ashers as well. The HF with spin rinse and dry is effective at reducing all metal contaminants to below detection limits except for the Cu, confirming earlier findings at SEMATECH (2). The addition of HCl to the rinse sequence produces a wafer surface with all metals below detection limits. We emphasize that space limitations prohibit us from including the extensive data that we have supporting the graphical summary in Figure 1, however we have sufficient data to justify the calculation of means and standard deviations for the contaminant residuals, and we have repeated these experiments more than a half dozen times over the duration of this project.

Extensive evaluation of both monitor wafers and wafers that were stripped of a 15 nm sacrificial oxide indicated no significant difference in surface microroughness (as measured with AFM) between unprocessed controls, the standard wet bench cleans or any vapor-phase chemical dispense sequence. After very extensive SIMS and ESCA studies for light element contamination, complimenting the TXRF, we can conclude that: all the surfaces are exceptionally clean, the atomic surface fluorine concentration is reduced by a factor of 2-3X by the use of the in-situ rinse following the AHF. All the vapor-phase recipes have a 1-3 atomic % flourine level which is 2-5X that of the wet bench HF last standard.

PRE-CONTACT CLEAN APPLICATION

The modular zone tester used as the vehicle for the pre-contact application is one of a family of Metal 1 testers used for our 0.9 μm and 1.25 μm production environments as well as our 0.5 μm development technology. These testers monitor the window, window-to-gate, and dielectric yields as well as associated parameters. AT&T's view of the desired outputs and attributes for the pre-contact clean are:

- *Clearing* of the oxidized/nitrided uppermost layer of the titanium silicide. The oxygen and nitrogen are incorporated during RTA forming of the silicide.
- Not to increase the window diameter by >20 %. The windows are nominally 1 μm in diameter.
- Does not undercut the BPTEOS. The selectivity ratios for the wet chemical process are such that this can happen.
- No pitting attack of the titanium silicide.
- Acceptable contact resistance.
- Approach 0.1 defects per million windows.

The pre-Ti deposition wet clean following RTA window reflow is an 8:1 EG/BHF dip. The wet bench used for the standard clean is automated with a robot to insure that the 30 second etch is precise.

The contact window tester chip is divided into three major sections: contact (window) yield, dielectric yield, and parametrics and reliability. The contact yield portion of the chip is composed of four nominal yield sections, one doublet yield section and one smaller than nominal window yield section. Each yield section contains 11 subsections with about 10,000 contact windows each. With 112 chips on each zone tester wafer there are roughly 74 million contact windows per wafer. The characterization of the contact yield sections is as follows: 4 Volts is forced through all 11 subsections and the current is measured. IF R = V/I is > 1 Mohm, THEN each of the 11 subsections is measured alone, AND IF R > 1 Mohm the subsection is a fail.

A family of CONMAT, "contact material", vapor-phase recipes were investigated using a 16 cell DOE matrix. The details of the experimental design phase of this work are described in the program final report (3). Basically the CONMAT recipe is a short time, low flow vapor-phase HF light etch, optimized for a 5 nm thermal oxide equivalent target (meant to mimic the oxy-nitride present atop the titanium silicide after forming). The BPTEOS to TEOS etch selectively is between 1.1 and 1.2.

The test data for a representative lot is presented in Table I. The first three columns: cell name, window contact resistance and standard deviation are self-explanatory. The window step ratio is a measure of the metal coverage. It is the ratio of the resistance of a metal runner that follows the via step to a similar planar runner that

does not follow the steps. The data for the contact resistance and window step coverage are identical in view of the standard deviations. The dielectric thickness derived from the electrical tests provides data for a direct comparison with the etch deltas derived from thermal oxide monitor wafers processed with the tester lots, and with a predicted BPTEOS etch delta based on modelling work. The last five columns present the defects per million vias (N_o) for the window, doublet and sub-nominal via chains, and the 0.95 confidence levels for the nominal via defect density.

Table I. Pre-Contact Clean Application - Tester Data Summary

Cell	Window Contact Resistance	Std Dev	Window Step Ratio	Stnd Dev	Dielectric Thickness	Stnd Dev	No Window	No Doublet	No Subnominal	0.95 Poisson CL Low	0.95 Poisson CL High
Stnd wet	0.40	0.10	1.09	0.02	5,423	69	0.31	0.22	0.42	0.26	0.36
CONMAT	0.41	0.11	1.09	0.01	5,087	100	0.25	0.20	0.39	0.20	0.31
CONMAT	0.44	0.12	1.09	0.01	5,135	132	0.31	0.17	0.58	0.26	0.38
CONMAT	0.43	0.11	1.09	0.02	5,038	87	0.29	0.21	0.48	0.24	0.35
CONMAT	0.45	0.12	1.08	0.02	4,870	54	0.27	0.14	0.37	0.22	0.33

The data we considered in determining the *relative effectiveness* of the vapor-phase cleans to the standard wet bench clean is based on comparison of the mean value for the nominal window defects (per million) to the low and high 95 % confidence level limits of the wet clean cell within the lot. With this criteria applied we conclude the vapor-phase CONMAT recipe demonstrates *improved or equal to wet* performance in each of the three lots processed.

PRE-GATE OXIDE APPLICATION

The modular gate oxide tester used as the test vehicle has a 9 nm gate oxide. AT&T's view of the pre-gate cleaning requirements and desired attributes are:

- Must remove 15 nm gate zero sacrificial oxide
- Leave the Si surface free of metallic, organic and particle contamination.
- Atomically smooth Si surface.
- No over etching beyond 20 nm thermal oxide equivalent
- Gate oxide defect density < 1 cm^{-2} and Fowler-Nordheim Voltages > 15 volts.
- Superior gate oxide thickness reproducibility and uniformity.

We point out that the atomically smooth Si surface attribute comes from reports in the literature rather than from AT&T's experience with wet benches and our current products. Significant particle reductions throughout front end processing and a focus on pregate oxidation cleaning improvements have measurably reduced D_o values obtainable with a conventional thermal oxidation. Earlier work by one of the authors (PKR, 4)

focused on the advantages of the stacked oxide dielectric, which has been advanced considerably by Motorola (5). That work suggested achievable limits in conventional thermal oxide D_o values somewhat higher than those obtained in this study for either the standard wet or vapor-phase cleans.

Figure 2 is a schematic of the test structure used to characterize the pre-gate oxide device lots. The large area capacitor (~ 0.1 cm^2) is tested under accumulation using a voltage ramp. The failure criteria is >1 $\mu A/cm^2$ leakage. The defect density data (LGOX-Do where $D_o = -\ln(Y)/A$) represent failure due to oxide shorts that are potential reliability failures. J-Ramp accelerated aging test of small area grid capacitors (2.5×10^{-4} cm^2) generates charge-to-breakdown, N_{bd} and oxide tunneling characteristics. The failure criteria is $V_{measured} < 0.85\ V_{previous}$. N_{bd} and V_{bd} represent intrisic wear-out characteristics of the gate oxide. We point out that we have not characterized these nine lots for TDDB wear out or CV characteristics. The data we have compiled includes D_o data for both large area and patterned small area capacitors. The patterned, or PGOX D_o will emphasize perimeter related effects. The breakdown field of the gate oxide V_{bd} represents a measure of the intrinsic dielectric strength. The J-ramp aging test yields N_{bd}, charge to breakdown and V_{FN}, Fowler-Nordheim tunneling characteristics which speak to wear-out of the gate oxide. FNVs of 15 volts and log N_{bd} values approaching 0.7 to 0.9 are generally accepted targets for successful 0.35 μm technology regardless of the nature of the gate oxide dielectric: conventional or stacked.

The standard pre-gate cleaning sequence is a megasonic ammonia hydroxide-hydrogen peroxide, followed by sulfuric and hydrogen peroxide, an HF last, overflow rinse and dry. In all vapor-phase cells the HF last was replaced with the AHF dispense targeted for a 25 nm thermal oxide etch equivalent. The in situ spin was run either without or with vapor HCl. Again Figure 1 shows the added benefit of HCl in the rinse for copper removal.

Over the course of the 16 month program nine lots of gate oxide testers, each lot containing approximately 40 wafers were completed through electrical testing. We emphasize that all this data has been considered in formulating the discussion below. The formal SEMATECH end of contract member company review (6) and report (3) only considered the electrical data from the first four lots, and unfortunately operator errors in areas outside the pre-gate cleaning split severely degraded the value of over half of that data.

To include even a representative sampling of the raw data from the quantity of test data associated with nine lots is well beyond the space limitations allowed. In Figure 3 we do present box plots from one lot. The box plots in Figure 3 present the mean D_o and the 95 and 5 percent confidence level points for each of the cells. If the mean of one cell fell outside 2 sigma of the standard clean then the cell was judged as either improved or poorer relative to the standard clean.

Applying this criteria to the LGOX D_o data in Figure 3 we judge the relative effectiveness of two vapor-phase cells as improved and two others as equal, relative to the wet standard. The details of the processing chemistries corresponding to the vapor-phase cleans have been detailed in reference 3. As the size of the electrical results data base grew, it became evident that the LGOX D_os were more or less equivalent, while at the same time it became clearer that the PGOX D_os were indicative of a substantial improvement. In Figure 4 screened PGOX D_os plotted relative to the standard are presented as a function of test voltages, for the failure criteria described above. This data comes from lots processed at very different times and in fact, in multiple oxidation furnaces. At the 4.5V level we have also plotted the 95% confidence level (2 sigma) point of the standard cleans in order to emphasize the statistical significance of the difference in three of the four examples.

Another important intrinsic oxide quality parameter is T_{ox} FNV. It is the oxide "thickness" derived from the Fowler-Nordheim analysis of the J-ramp test. We have found that the vapor-phase pre-gate oxidation cleans yield conventionally grown thermal oxide gates with very low non-uniformities across the wafers. T_{ox} FNVs < 0.5% standard deviation have been repeatably obtained. We also note that although the Log Nbd and Vbd values for the vapor-phase cleans are not as dramatically improved as the PGOX D_os, that the standard deviations for these parameters are almost without exception half the size of the relative wet clean standard deviations.

In summary, the electrical test data suggest the following vapor-phase pre-gate clean advantages: a statistically lower patterned GOX D_o, some improvements in Nbd and Vbd, within wafer standard deviations on many parameters that are half the size of the wet clean standard deviations, and equivalence of large area GOX D_o. From our process demonstration work we know we have exceptionally low particle counts, no detectable microsurface roughening and a silicon surface containing no detectable metals. We have on the order of 3 atomic % fluorine on the vapor-phased processed surfaces. In view of these findings can we offer even a tentative correlation that would support the electrical data? Given that both the standard wet cleaning sequence and vapor-phase clean are very low particle count processes one would expect the LGOX to be less sensitive to differences then the more device realistic PGOX. Since we have no copper issue with our devices or fabrication line it is not surprising that we found the *with HCl* vapor-phase cells to be about the same as the *without HCl* cells. The improved Tox FNV can be thought of in terms of a "microporosity" measure within the initial stages of the thermal oxide growth on the vapor-phase cleaned bare silicon surface. Certainly, numerous references in Tseng and Tobin (5) cite the advantages of small quantities of fluorine at the silicon-silicon dioxide interface. Whatever the *conditioning* of the silicon atomic surface in preparation for the thermal oxidation it would appear that the vapor-phase processing clearly provides a more uniform condition across the wafer and wafer-to-wafer within a cell than the wet clean.

REFERENCES

1. N. StreckfuB, et. al., Fresenius J. Anal. Chem. 343, 765, (1992).

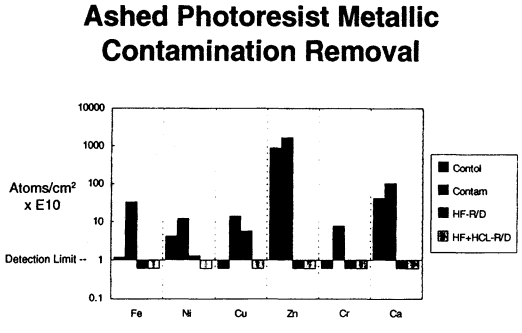
2. SEM-91060586A-ENG, FSI Excalibur ISR 200 Anhydrous HF Processor, SEMATECH Project S28, Date: July 18, 1991.

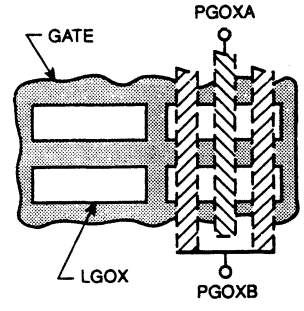
3. SEM-93011469A-ENG, Vapor-Phase Cleaning Applications Development, SEMATECH Project E42, Date: August 19, 1993.

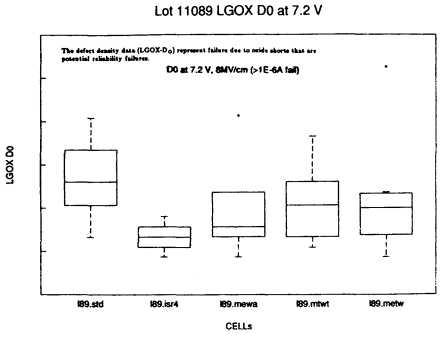
4. P. K. Roy and A. K. Sinha, AT&T Technical Journal, 67(6), 155, (Nov/Dec 1988).

5. H-H Tseng and P. J. Tobin, Semi. Intern. 15(8), 68, (July 1992), and numerous references therein.

6. Vapor-Phase Cleaning Applications Development Program, Project E42 Final Program Review, December 15, 1992, Dallas, TX.







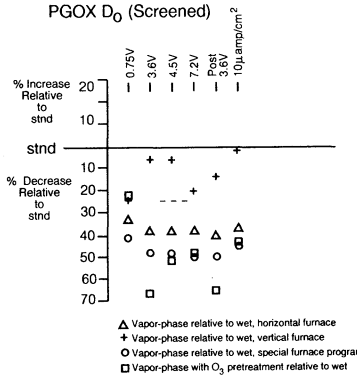


Figure 1. Upper Left. Bar graph summary of TXRF data evaluation of the relative effectiveness of vapor-phase HF with and without HCl in removing ashed photoresist transition metal residues from blanket-coated, bare silicon wafer surfaces.

Figure 2. Upper Right. Schematic diagram of the gate oxide (GOX) module tester.

Figure 3. Lower Left. Relative Large Area GOX Do's for one lot of module tester wafers. The box indicates the mean and 95 % CL limits for each cell within the lot.

Figure 4. Lower Right. Relative Patterned Small Area GOX Do's for four different lots . The standard clean's 95 % CL at 4.5 V is indicated by the dashed line. Three of the four lots show statistically significant marked improvements.

CLEANING OF SILICON SURFACE AFTER RIE USING UV/OZONE AND HF/CH_3OH

David K. Hwang and Jerzy Ruzyllo
Electronic Material Processing and Research Laboratory
The Pennsylvania State University
University Park, PA 16802

Emil Kamieniecki
QC Solutions
Lexington, MA 02173

The removal of a polymer-like film deposited by a fluorocarbon -based reactive ion etching (RIE) chemistry using UV/Ozone followed in-situ by an HF/CH_3OH oxide etch was investigated. The two step cleaning is accomplished in a prototype of a cluster-tool compatible dry cleaning module. RIE on bare silicon wafers using a CHF_3 chemistry was performed to simulate an overetch process. The change in the polymer thickness during the UV/Ozone removal process was monitored using an ellipsometer. XPS results indicate a significant reduction in the carbon, fluorine and oxygen content on the silicon surface after the cleaning process. Surface charge analysis (SCA) was also used to compare the surface condition of the etched and cleaned sample with an unetched sample.

INTRODUCTION

Selective etching of SiO_2 on Si is an important part of processing highly integrated circuits. Reactive Ion Etching (RIE) is a method of pattern transfer that combines physical sputtering with chemical etching and provides a high degree of anisotropy. The sputtering and the exposure to the plasma can lead to bombardment damage. More over, etching results in the deposition of an involatile polymer in the case of fluorocarbon -based RIE chemistries. This polymer prevents excessive etching of the Si substrate. Prior to subsequent processing the polymer film must be removed. This concerns also very thin oxide layer

that remains on the surface following polymer volatization. Typically, these two applications are performed separately, e.g. O_2-plasma ashing of polymer followed by an HF:H_2O etching. In this experiment we are investigating integration of these two steps using a prototype of a dry cleaning reactor.

The UV/Ozone process (1) has been found to be effective for removing a variety of organic contaminants from the surface including polymer-like films deposited by RIE (2). On the other hand, an anhydrous HF/CH_3OH process was found effective in thin oxide etching applications (3). The goal of this study was to combine these operations into an integrated post-RIE cleaning process.

EXPERIMENTAL

RIE of bare silicon wafers was carried out to simulate an overetch process. A CHF_3/N_2 chemistry was used with a gas flow of 40 sccm of CHF_3 and 60 sccm of N_2 at 100 mT. The applied power was 550 watts. The overetch process deposited a polymer approx. 65Å thick the presence of which was confirmed using x-ray photoelectron spectroscopy (XPS) and the thickness measured with an ellipsometer using a fixed index of refraction of 1.465.

A prototype of a cluster tool compatible commercial apparatus (4) was used in this study, Fig. 1. The process chamber in the apparatus is compatible with eight inch wafers. It is equipped with IR heating lamps, a 500 watt high pressure broad spectrum xenon lamp which irradiates the inside of the chamber through a sapphire window. The system is also equipped with an ozone generator. The system uses an all stainless steel gas delivery system.

The Si wafers with the polymer film were cleaned using various combinations of UV and ozone exposure. The addition of methanol to the UV/Ozone process was also investigated. Oxygen was flowed through the ozone generator and into the chamber while methanol contained in a bubbler was carry into the process chamber using a N_2 carrier gas, when needed. Irradiation by the IR and/or UV lamp was done through the sapphire window. A pressure of 500 Torr and temperature of 120°C was maintained in the process chamber. An ellipsometer was used to monitor the change in the polymer thickness

following the UV/Ozone exposures. XPS was performed at various stages during the cleaning process to determine the effectiveness of the polymer removal.

Following the UV/Ozone cleaning process a anhydrous HF/CH_3OH etch was performed in the same process chamber to remove the residue layer left after the UV/Ozone cleaning process. The process was carried out at 80°C and 300 Torr for 1 minute.

Additional information concerning condition of the surface was obtained from surface charge analysis (SCA) (5). SCA measurements were taken after the various processing steps and comparisons were made with control samples that were not exposed to RIE.

RESULTS AND DISCUSSION

The results of the ellipsometer measurements on the RIE Si wafers indicate the presence of a polymer film 60-70Å in thickness. The effectiveness of the polymer removal for the various combinations of UV with ozone are shown in Fig. 2, which shows the remaining polymer thickness after various processes. UV exposure and ozone alone resulted in a very slow removal rate. The combination of UV with ozone significantly increased the removal rate of the polymer. The addition of methanol to the UV/Ozone process was found to further increase the removal rate of the polymer film . This is likely due to the formation of OH which, as a very strong oxidant, accelerates the process of polymer oxidation. With the addition of methanol most of the polymer is removed within the first 5 minutes. Since the recipe using the combination of UV, ozone, and methanol was found to be the most effective at removing the polymer the rest of the study will emphasize this process.

The removal rate decreases as the film thickness approaches 20Å. Further UV/Ozone cleaning did not decrease the thickness of this remaining film. Figures 3 and 4 show the change in the composition of the film due to the UV/Ozone/methanol process. Initially, Fig. 3, the polymer film is composed mainly of carbon, fluorine, and oxygen. After the UV/Ozone/methanol process, Fig. 4, the level of carbon and fluorine have been decreased but the amount of oxygen has drastically increased. The Si peaks have also become more evident. The high oxygen content of the film and the presence of the Si peaks indicate

that the film has a SiO_x composition. Applications of a anhydrous HF/CH_3OH etch was found to be effective in removing most of the remaining film. The film thickness after the anhydrous HF/CH_3OH etch could not be measured by the ellipsometer. Figure 5 is the XPS spectrum of the surface after the anhydrous HF etch. The oxygen peak has been greatly reduced and the presence of carbon and fluorine have also been greatly reduced. The remaining small oxygen peak could be due to reoxidation of the surface during transport from the dry cleaning chamber to the XPS apparatus. Further application of the UV/Ozone and HF/CH_3OH procedures in sequence was found to further reduce the carbon concentration at the surface but do not affect the concentration of the surface fluorine, Fig. 6. As the fluorine peak remains relatively unchanged throughout the cleaning process, it is likely that the fluorine was slightly implanted during the RIE process. Another possibility is that fluorine results from the HF/CH_3OH process. However, it would be difficult to explain the presence of fluorine on the surface which was not exposed to the HF/CH_3OH process (Fig. 3).

The XPS characterization provides information on the chemical condition of the surface, but not on its physical state. Surface Charge Analysis (SCA) provides results that can be linked with both chemical and physical state of the Si surface. The SCA was used in this study to compare the RIE treated surfaces with the control surfaces. Figure 7 shows the SCA results of the control sample that had gone through a anhydrous HF/CH_3OH etch only and RIE processed samples that had been cleaned with the UV/Ozone/methanol followed by a anhydrous HF etch and the repeat UV/Ozone and HF cycle. The SCA shows that the Si surfaces are very different. Since XPS results indicate that most of the polymer is being removed the differences in the SCA results is be due to the surface damage caused by RIE.

SUMMARY

The polymer deposited by a CHF_3 RIE process can be removed by a UV/Ozone process. The additional of methanol to the process was found to increase the removal rate of the polymer. After the UV/Ozone process an oxygen rich film is remaining on the surface. A anhydrous HF/CH_3OH etch was found to be successful in removing this film. The

XPS results indicate that the presence of carbon and fluorine have been significantly reduced by the UV/Ozone clean followed by the anhydrous HF/CH_3OH etch. The surface damage resulting from the RIE remains unaffected by the surface treatments applied in this study.

ACKNOWLEDGEMENTS

This project was sponsored by the Semiconductor Research Corporation under the contract 92-MJ-274. Also, thanks are due to SubMicron Systems, Inc. for providing the tool used in this study.

REFERENCES

[1] J.R. Vig, J. Vac. Sci. Technol. A3(3), 1027, 1985.
[2] J. Ruzyllo, G.T. Duranko, J.T. Kennedy, C.G. Pantano, First International Sym. ULSI, Phila., May, 1987.
[3] J. Ruzyllo, K. Torek, C. Daffron, R. Grant, R. Novak, J. Electrochem. Soc. 140, L64, 1993.
[4] SubMicron Systems, Inc., Allentown, Pennsylvania, Model SP-200.
[5] E. Kamieniecki, J. Vac. Sci. Technol., 20(3), 811, 1982.

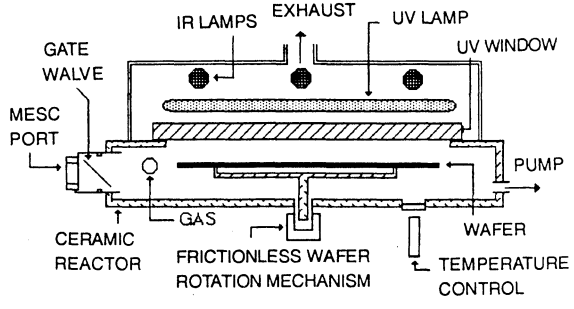


Figure 1 Schematic of the prototype cluster tool used in this study. The system also has an ozone generator not shown in this figure.

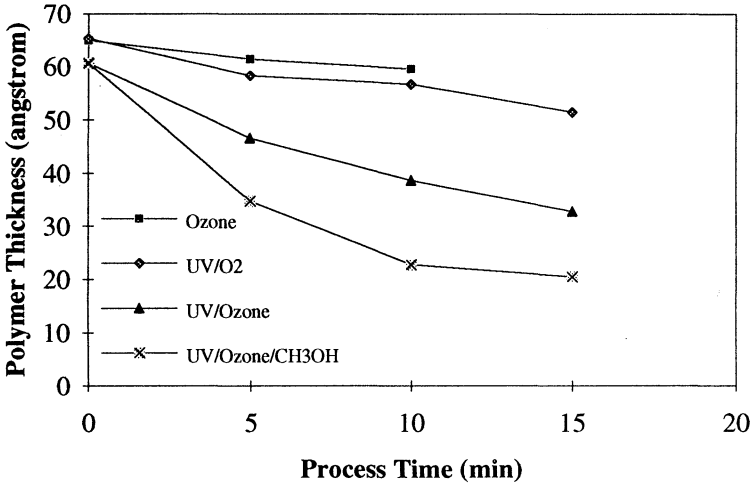


Figure 2 Removal of the RIE polymer as shown by the decreasing thickness of the polymer film as measured by ellipsometry using a constant index of refraction of 1.465.

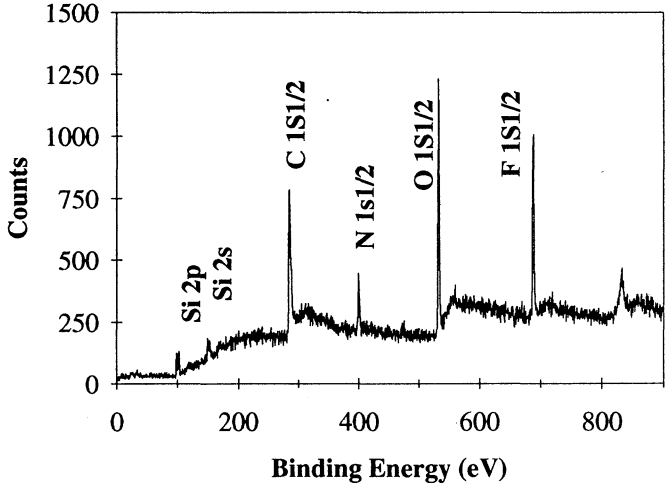


Figure 3 XPS spectrum of a sample after a CHF_3/N_2 RIE.

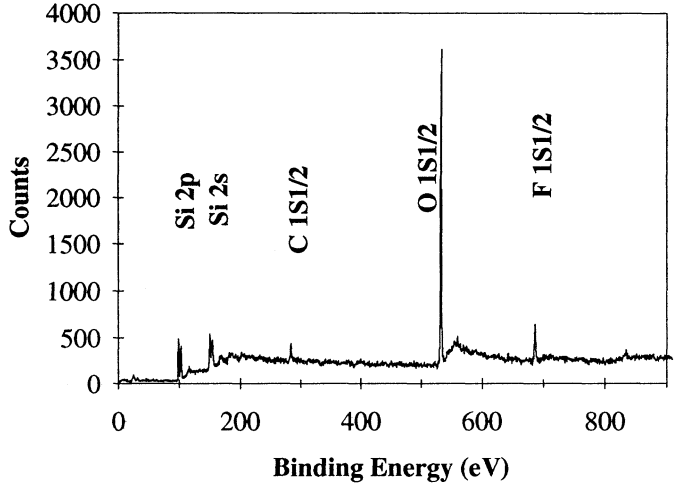


Figure 4 XPS spectrum of a sample after the UV/Ozone with the addition of methanol (CH_3OH). (Note the change in the vertical scale)

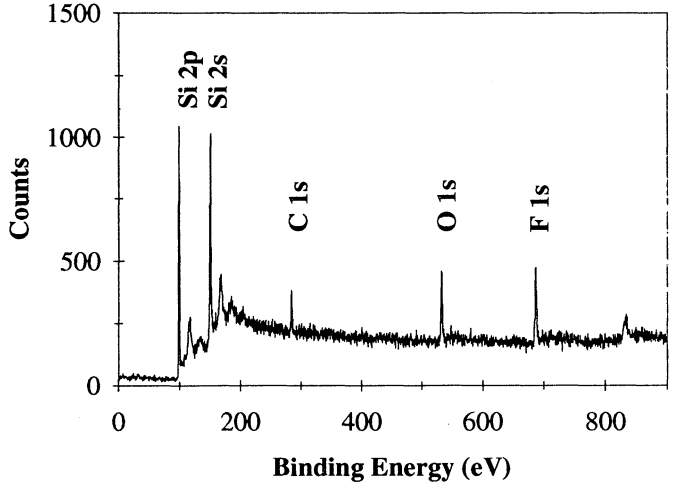


Figure 5 XPS spectrum of a sample that was UV/Ozone cleaned followed by a anhydrous HF etch.

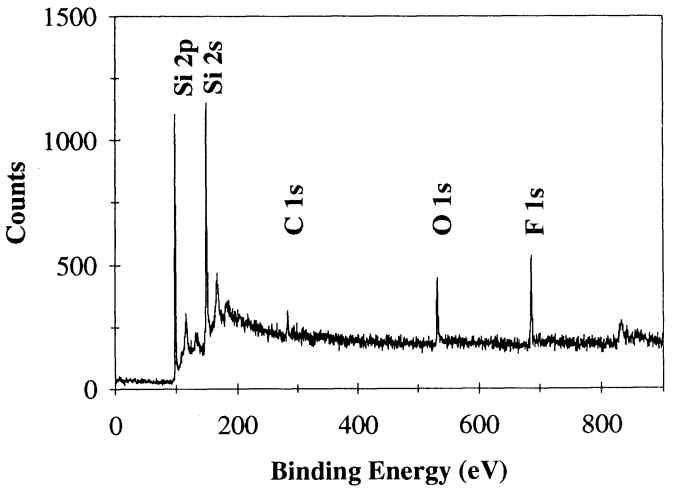


Figure 6 XPS spectrum of a sample that received the UV/Ozone clean followed by a anhydrous HF etch then a repeated 1 min UV/Ozone and HF etch clean.

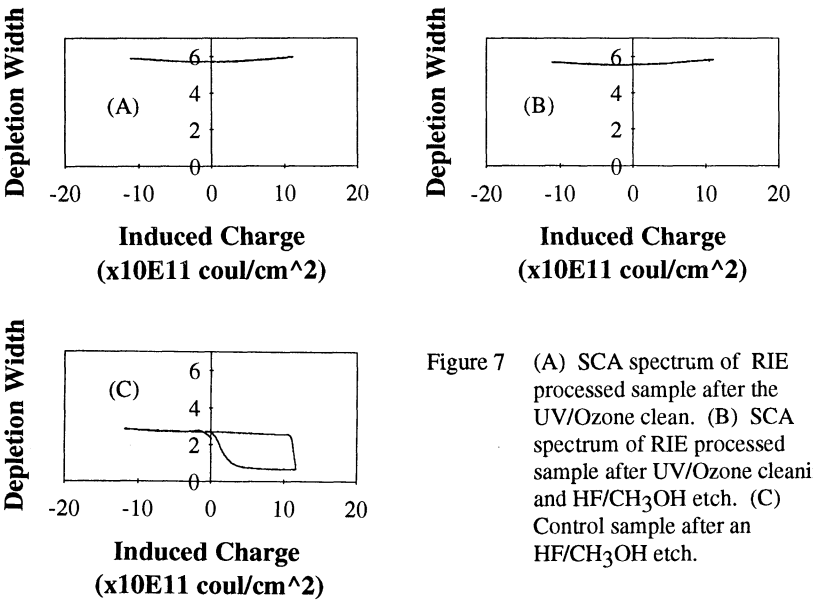


Figure 7 (A) SCA spectrum of RIE processed sample after the UV/Ozone clean. (B) SCA spectrum of RIE processed sample after UV/Ozone cleaning and HF/CH_3OH etch. (C) Control sample after an HF/CH_3OH etch.

Removal of Fe and Al by Pyrochemical Cleaning

Young Limb, Bich-Yen Nguyen and Philip Tobin

Motorola, Advanced Products Research and Development Laboratory
Austin, Texas 78721

A new HCl-based thermal cleaning process which we call Pyrochemical cleaning was developed. The cleaning efficiency of this new cleaning process was examined by intentionally introducing contaminants on the wafer surface and measuring with a TXRF spectrometer the residual contaminant concentration after the cleaning. The results showed that the new cleaning process is effective in removing metallic contaminants including Fe and Al. The reliability of Al-contaminated gate oxide was observed to dramatically improve when Pyrochemical cleaning was utilized.

Introduction

As device feature size scales down, chip size rapidly increases and the number of process steps for fabrication also increases. Therefore, the effect of process-induced contamination becomes increasingly important for successful production of the scaled-down devices. Furthermore, new processes such as CMP, trench isolation and salicide processing may also aggravate the problem. It is believed that the process-induced contamination must be controlled below the 1E10 atoms/cm2 level for successfully manufacturing ULSI devices (1). It is a challenging task and can not be achieved without an effective cleaning process. In order to enhance cleaning capability, we developed a new HCl-based thermal cleaning process which we refer to as Pyrochemical cleaning.

Pyrochemical Cleaning

The removal of metallic contaminants on a wafer surface by a typical Pyrochemical cleaning is achieved by heating the wafer at 650C in 3% HCl, 2% O2 and N2 ambient for 30 minutes as illustrated in Figure 1. During the heating, the metallic contaminants react with HCl and O2, form volatile reaction products, metal chlorides and/or metal oxychlorides and are eliminated by evaporation. During the heating, hydrocarbons can also react with the O2, to produce volatile reaction products such as H2O, CO and CO2. The major advantage of Pyrochemical cleaning is to allow the early elimination of contaminants prior to hot processes which may remain on the wafer surface after wet cleaning and other processes which cause irreversible damage to the device. Pyrochemical cleaning may be substituted for SC2 cleaning or used as a last clean prior to a gate oxidation when cost-effective chemicals are utilized in wet cleanings.

In this paper, we will show that Pyrochemical cleaning is very effective in removing two primary metallic contaminants found on wafer surface in the fabs, Fe (2, 4) and Al (3) and the secondary metallic contaminants such as Ni, Cr and Cu as well. We will also demonstrate that the catastrophic reliability degradation of gate oxide induced by Al and Fe contamination is avoided by Pyrochemical cleaning.

Experimental Procedure

P type, (100) oriented, polished Si wafers, on which the surface heavy metal concentration is below 5E10 atoms/cm2, were used. The wafers were intentionally contaminated at a localized area or on the whole surface of the wafers using a spin-on technique with aqueous NH4OH and H2O2 solutions containing a known concentration of dissolved contaminants. The removal of metallic contaminants by a cleaning process was assessed by measuring the change of the contaminant concentration on the monitors before and after the cleaning. The contaminant concentration was primarily measured using Rigaku models 3725 and 3726 TXRF spectrometers having the minimum detection limit of 1E11 and 5E9 atoms/cm2 for Fe, respectively, and also by VPD-ICP-MS. The Pyrochemical cleaning was carried out in standard horizontal diffusion furnaces with fused silica tubes.

The gate oxide was grown on N type, (100) wafers at 900C in O2 ambient with 3% HCl unless specified otherwise. The effect of Al and Fe contamination on gate oxide integrity was assessed by intentionally contaminating the Si substrate with different concentrations of Fe and Al using a spin-on technique after RCA clean prior to the oxidation.

Results and Discussion

Removal of Fe, Ni, Cr and Cu

The removal of Fe, Ni, Cr and Cu by Pyrochemical cleaning was investigated by intentionally contaminating a monitor wafer with a high concentration of Fe, Ni, Cr and Cu, approximately, 7-9E13 atoms/cm2, and measuring by TXRF the change of the concentration after the cleaning. Figures 2 (a) and (b) exhibit the TXRF spectra of Fe, Ni Cr and Cu as contaminated and after Pyrochemical cleaning, respectively. The TXRF spectra of Fe, Ni, Cr and Cu disappear after Pyrochemical cleaning, verifying that the contaminants are totally removed.

The HCl concentration dependence of Pyrochemical cleaning efficiency on Fe, Ni, Cu and Cr was examined. Five wafers were intentionally contaminated with approximately equal amounts of Fe, Ni, Cr and Cu followed by Pyrochemical cleaning with varying concentrations of HCl from 0 to 3%. After the cleaning, the concentration of the contaminants on the wafers were analyzed by TXRF. The result, plotted in Figure 3 reveals that the removal efficiency of Pyrochemical cleaning is strongly HCl concentration-dependent. It shows that the efficiency increases with increasing concentration of HCL, reaching 100 % for all the contaminants including Cr at 3% HCl.

Effect of Fe Contamination On QBD

The effect of Fe contamination on QBD of 105A oxide was investigated by intentionally contaminating the Si substrate with varying concentrations of Fe from 5E11 to 4.5E12 atoms/cm2 prior to the oxidation. The oxide was grown at 900C with 3% HCl. In order to see the effect of HCl during the oxidation on QBD, 105A oxide was also grown without HCl. Figure 4 exhibits the QBD characteristics of the oxides grown with and without 3% HCL. It is seen that the QBD is not affected by the Fe contamination regardless of the concentration range studied when 3% HCl is used. However, the QBD with no HCl is seriously degraded even for the lowest concentration of Fe contamination studied, 5E11

atoms/cm2. This result clearly suggests that Fe can be a benign contaminant if HCl is used properly.

Removal of Al

Figure 5 (a) and (b) reveal the removal of Al by Pyrochemical cleaning. A monitor wafer was intentionally contaminated with a high concentration of Al, approximately 4.3E15 atoms/cm2 and followed by Pyrochemical cleaning and measurement by a TXRF. Figure 5 (a) and (b) reveals TXRF spectrum of the Al as contaminated and after Pyrochemical cleaning, respectively. It is clearly seen that the Al spectrum completely disappears after Pyrochemical cleaning, showing that the Al was removed.

Effect of Al Contamination on QBD

The effect of Al contamination on 105A gate oxide was examined by intentionally contaminating the silicon surface with a high concentration of Al, about 4.7E13 atoms/cm2 prior to the oxidation and subsequently growing the gate oxide with 3% HCl without and with Pyrochemical cleaning. The result is seen in Figure 6 (a) which reveals that the QBD characteristics of the former without Pyrochemical cleaning is extremely poor whereas that of the latter with Pyrochemical cleaning, Figure 6 (b) is normal. These results clearly shows that the Al contamination can cause a catastrophic reliability problem for the gate oxide which is avoided by removing Al by Pyrochemical cleaning. It is also interesting to find from Figure 6 (a) that the QBD is severely degraded even though 3% HCl is used during the oxidation. It indicates that the use of HCl during the oxidation does not alleviate the detrimental effect of the Al contamination as it does for the Fe contamination and thus Al must be removed before the oxidation.

Removal of SC1-induced contamination

The SC1-induced metal contamination and the resulting degradation of QBD characteristics of 105A oxide when SC1 is used as a pregate clean, were examined. In addition, the removal of the SC1-induced contaminants by Pyrochemical cleaning and the consequent recovery of the QBD were also demonstrated. The SC1 solution was mixed with a standard electronic grade H2O2 and NH4OH. The purity of the SC1 was analyzed by ICP-MS and a TXRF spectrometer as shown in Figure 7. The SC1 contains Al, Fe and Zn as major impurities, approximately 19, 9.5 and 5.4 ppb, respectively, and 2-4 ppb of Ni, Cr and Cu as minor impurities. Figure 7 also depicts the concentration of the contaminants induced on the wafer surface when a wafer was cleaned by the SC1. It shows that the wafer is contaminated with a high concentration of Al and Fe, approximately 9.4E12 and 7.0E11 atoms/cm2, respectively and also with a small concentration of Zn, 1.6E11 atoms/cm2. No other elements were found on the wafer surface in a measurable amount by VPD-ICP-MS. In order to compare the propensity of Al, Fe and Zn sticking on Si substrate, a relative adhesion coefficient for Al, Fe and Zn was calculated from Figure 7. We assume a linear relationship between the impurity concentration in the SC1 and the contaminant concentration induced on the wafer after the SC1 clean to calculate the relative adhesion coefficients shown in Figure 8. Clearly Al has the strongest tendency of sticking to the Si surface and is followed by Fe. It displays that the relative adhesion coefficient of Al is about a factor of 6 higher than that of Fe. It means that even a very low Al impurity in SC1 can result in a high Al contamination on the wafer and can pose a disastrous reliability problem of gate oxide. Figure 9 reveals the removal of the SC1-induced contaminants by Pyrochemical cleaning. The concentration of Al is drastically reduced and that of Fe and Zn is diminished to a non detectable level after Pyrochemical cleaning.

Effect of SC1 Clean on QBD

Figure 10 shows the QBD characteristics of 105A oxides which were grown with three different pregate cleans: SC1 clean, Pyrochemical clean after the SC1 and RCA clean. The QBD characteristics of the Pyrochemical pre-cleaned oxide is the best and followed by that of the RCA oxide and that of the SC1 oxide. It is obvious from Figure 7 that the poor QBD of the SC1 oxide results from the excessive Al contamination induced by SC1. Even though the oxide was also contaminated with Fe, it is unlikely that it contributed to the degradation of the QBD because the oxide was grown with 3% HCl. It is evident from Figure 9 that the excellent QBD characteristics of the Pyrochemical oxide results from the removal of Al by Pyrochemical cleaning.

Conclusions

1. Pyrochemical clean effectively removes Fe, Al, Cr, Ni, Cu and Zn from wafer surface.

2. Fe contamination severely degrades the QBD characteristics of thin oxide. However, the QBD is not affected by Fe contamination when 3% HCl is used during oxidation.

3. Al has a greater tendency of sticking to Si surface in SC1.

4. Al contamination severely degrades the QBD characteristics of thin oxide. The use of HCl during oxidation does not alleviate the degradation of QBD induced by Al contamination.

5. The degradation of the QBD induced by Al contamination is recovered when Al is removed by Pyrochemical cleaning.

6. Use of Pyrochemical cleaning dramatically improves the QBD characteristics of the thin oxide grown with SC1 as a pregate clean.

References

1. Tadahiro Ohmi, Takashi Imaoka, Takehiko Kezuka, Jun Takano and Masahi Kogure, J. Electrochem. Soc., vol. 140, no. 3 (1993).

2. T. Anzai, et al.: Proc. 1st Workshop Ultra Clean Technology, paper no. II.4, p. 73-94 (Nov., 1989).

3. Shimono, et al.: ibid, paper no. II.3, p. 49-72 (Nov. 1989).

4. Worth B. Henely, Lubek Jastrezebski and Nadim F. Haddad, the proceedings of the 1993 IEEE International Reliability Physics Symposium, March 22-25, 1993.

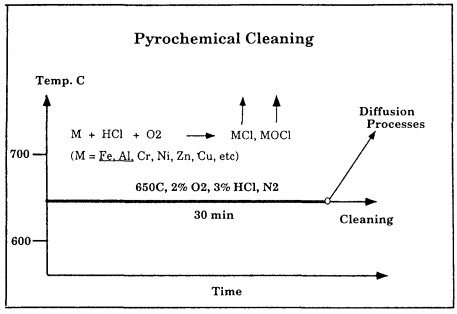


Figure 1, Schematic diagram of Pyrochemical cleaning process.

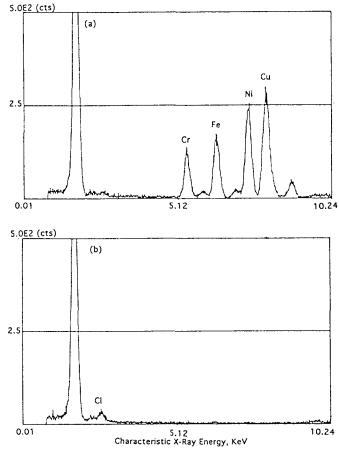


Figure 2, TXRF spectra of Fe, Ni, Cr and Cu intentionally introduced on a wafer (a) before and (b) after Pyrochemical Cleaning.

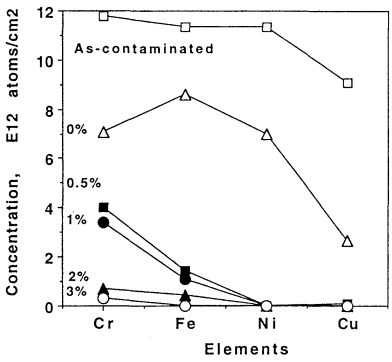


Figure 3, HCl concentration dependency of Pyrochemical cleaning for removal of Fe, Ni, Cr and Cu.

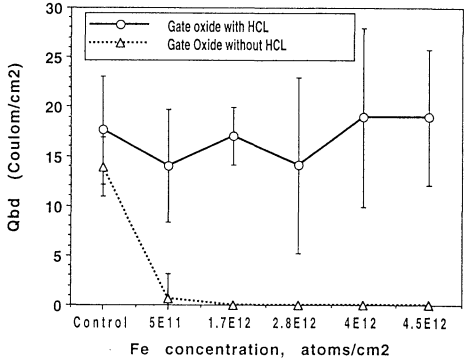


Figure 4, Effect of HCl during oxidation on gate oxide integrity.

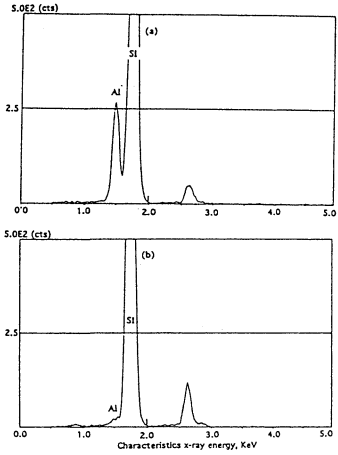


Figure 5, TXRF spectra of 4.3E15 atoms/cm2 of Al intentionally introduced on a wafer (a) before and (b) after Pyrochemical cleaning.

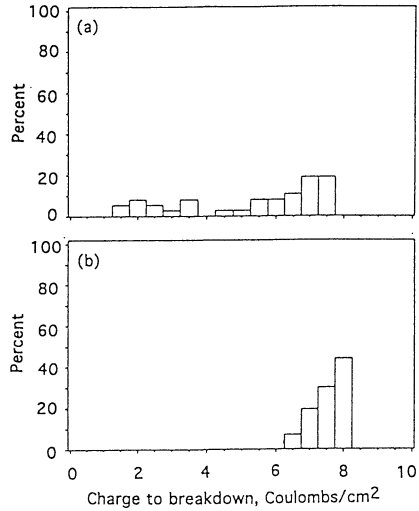


Figure 6, Charge to breakdown characteristics of 105A gate oxide intentionally contaminated with Al prior to the oxidation (a) without and (b) with Pyrochemical cleaning.

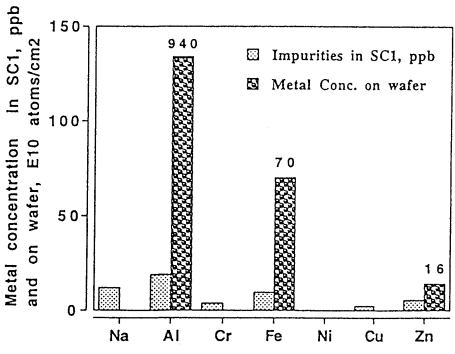


Figure 7, Metal concentration in SC1 solution and metal concentration induced on a wafer after cleaning by the SC1.

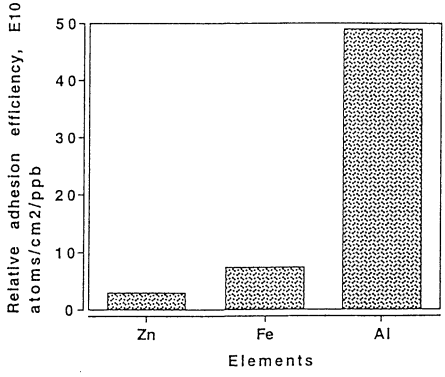


Figure 8, Relative adhesion efficiency of Zn, Fe and Al in SC1 solution.

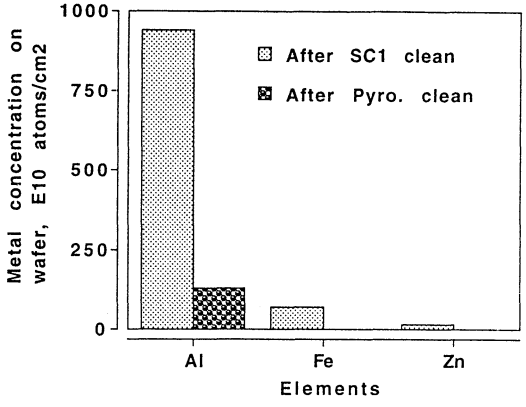


Figure 9, Removal of SC1-induced metallic contaminants by Pyrochemical cleaning.

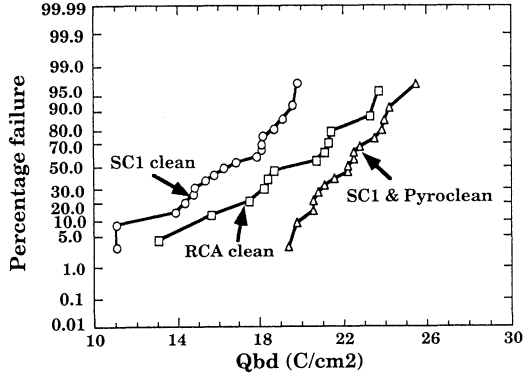


Figure 10, Charge to breakdown characteristics of 105A gate oxide with various pregate cleans.

THE INTERACTION OF HYDROGEN PLASMAS WITH Ga-BASED III-V SEMICONDUCTOR SURFACES

Z. Lu, S. Habermehl, G. Lucovsky, N. Dietz and K.J. Bachmann, Departments of Physics, and Material Science and Engineering, North Carolina State University, Raleigh, NC 27695

R. M. Osgood, Jr., Department. of Electrical Engineering and Applied Physics, Columbia University, New York, NY 10027

The interaction of hydrogen with Ga-based semiconductor (GaAs, GaP, GaSb) surfaces using both remote RF plasma and electron cyclotron resonance (ECR) plasma reactors was studied. Surface sensitive techniques such as Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS), and low energy electron diffraction (LEED) are used to characterize the surfaces in integrated ultrahigh vacuum processing systems. It is concluded that hydrogen does demonstrate a significant cleaning effects on all Ga-based III-V semiconductor surfaces. However, a both chemically clean and structurally ordered surface is difficult to obtain due to the differences in reactivity of different oxides.

I. INTRODUCTION

Hydrogen plasmas have been previously used to remove surface contamination such as carbon and oxygen from GaAs (100) surfaces.[1] However, many aspects of hydrogen processing of GaAs surfaces, such as surface passivation and damage (both physical and chemical), as well as surface cleaning, i.e., removal of surface contaminants, have not been explored in a comprehensive way. In addition, little is known about how hydrogen interacts with other III-V compound semiconductor surfaces such as GaP and GaSb. Previous experimental results indicated that mid-band gap interface states could be increased when Si surfaces were exposed to hydrogen plasma treatments.[2] In the case of compound III-V semiconductor surfaces, such surface processing is more complex since the rate of reaction of hydrogen with the oxides of the two atom constitute could be different due to the different bond energies of these oxides. This paper exams the interaction of hydrogen with three Ga-based semiconductor surfaces (GaSb, GaP, GaAs), not only in achieving surface cleaning and/or ordering, but also in understanding how and why surface passivation and damage occur.

II. EXPERIMENTAL

Our experiments were carried out in two different UHV integrated processing systems. Hydrogen plasmas were generated by either a remote RF or microwave electron cyclotron resonance (ECR) source. Both types of plasma sources are highly efficient in producing atomic hydrogen and have common characteristics of being downstream and remote, and generally producing low damage to substrates. Typical operating conditions for the RF plasma source are 10-30 mTorr at RF power 15-50 W. The ECR hydrogen plasma

typically operates at 0.5-1 mTorr and a microwave power of 50-70 W. However these ndividual processing parameters such as operating time and drive power, should not be directly compared, since more fundamental plasma parameters, such as plasma density, ion and electron temperature, etc. determine the rate of reactions. In both systems, power was coupled into the process gases using a quartz tube. The base pressures in both systems were $5\text{-}10 \times 10^{-9}$ Torr. Sample surfaces were exposed to downstream RF and ECR plasmas at remote locations of approximately 8 and 12 inches, respectively. For the studies described in this paper, the samples were grounded. However, no significant differences in surface cleaning were found when bias voltages were applied to the substrates. In the remote RF plasma system, hydrogen was either fed through the plasma tube, or injected downstream via a dispersal showerhead ring and activated from a He plasma. Hydrogen was also pre-mixed with He at different ratios, but this did not produce significant differences in the cleaning results. The details of both remote RF plasma[3] and ECR plasma operating conditions for hydrogen cleaning of semiconductor surfaces, as well for the XPS measurements have been discussed previously.[3] The system that has the remote RF plasma source was equipped with Auger Electron Spectroscopy (AES) and Low energy electron diffraction (LEED), both on-line in a separate analysis chamber. The other system with the ECR plasma source was equipped with an Al monochromatic X-ray Photoelectron Spectroscopy (MXPS), also in a separate analysis chamber. Samples were transferred under UHV conditions to the respective analysis chambers after exposure to hydrogen in the respective processing chambers. AES has a higher surface sensitivity for chemical analysis than MXPS, and LEED provides information relative to surface crystallinity. In addition, the high resolution MXPS provides a unique capability in studying surface passivation through changes in the band bending as well the bonding chemistry (see Fig. 3). Combining the results of all three complementary surface sensitive techniques, we can exam this fundamentally interesting and technologically important process from several different vantage points.

III. RESULTS AND DISCUSSIONS

As we can anticipate, highly reactive atomic hydrogen, generated by a plasma process, can be effective in removing surface contaminants. Consider first H interactions with GaSb surfaces. A significant reduction of native oxides and of surface carbon has been achieved by exposure of chemically treated surfaces to atomic H as shown in Fig. 1. The spectra labeled *a* show an n-type (111) GaSb surface after one minute of off-line processing in a 50% NH_4OH solution. The resulting oxide is composed primarily of Sb_2O_3 and Ga_2O_3, with some Sb_2O_5, as determined respectively from core-level chemical shifts of 2.4 eV, 1 eV, 3.8 eV toward higher binding energies (BE). The rather large shifts for the Sb atoms allow the oxidized component to be well separated from the substrate peak; however, for Ga, the oxidized component appears as a shoulder on the Ga substrate peak. After 30 minutes of ECR-hydrogen plasma processing (1 mTorr at a microwave poser of 60 W) at room temperature, the Sb-oxide signal is completely gone, while the Ga_2O_3 shoulder is only slightly reduced (see spectra labeled *b*). The results displayed in Fig. 1(*b*) also show that the C 1s signal has disappeared, indicating that the hydrogen plasma eliminates surface hydrocarbons. At the same time, the substrate intensity for both the Sb and Ga peaks

increased significantly, also consistent with overlayer removal. However, a careful curve fitting of Ga $2p_{3/2}$ core level features shows that sub-monolayer residual Ga-oxide is still left on the surface. These data then demonstrate that the Sb-oxides react more readily with the hydrogen plasma than Ga_2O_3; this is a predictable result since the Sb-oxides are less thermodynamically stable than Ga_2O_3, as indicated by free energy of formation data.[4] In summary, Sb-oxides and surface carbon can be removed easily by an ECR-H plasma at room temperature, while Ga-oxide is found more difficult to remove.

Hydrogen cleaning of GaP surfaces was motivated by the need for a low-temperature cleaning before growth of Si epitaxial layers by a remote plasma process. Both GaP (100) and GaP (111) samples were examined. Figure 2 summarizes the results for remote RF H-plasma interactions with GaP (111) surfaces. The experimental conditions for this surface treatment are as follows: a flow rate of 25 sccm H_2 through that plasma tube; a chamber pressure of 10 mTorr; a maximum exposure of 6 minutes; a sample temperature at 530°C and an RF power 50 W. The AES spectra show that sample heating alone, e.g., 530°C for 20 minutes, will heat desorb some hydrocarbon adsorbates, but will not significantly reduce the oxygen signal. H-exposure times from 30 s to 2 minutes significantly reduce the oxygen O KLL intensity as shown Fig. 2(A). Longer treatments to 6 minutes eventually minimize, but never completely eliminate the oxygen signal. A LEED pattern after the 6 minutes exposure gives sharp (1x1) diffraction spots on a diffuse background. Similar AES results have also been obtained on GaP (100); however, the LEED pattern is no better than that of GaP (111).

Special attention was paid to GaAs surfaces in this paper. Figure 3(A) shows XPS spectra for GaAs (110) surfaces for different ECR-H exposure times at 1 mTorr and at a microwave power level of 50 W. The XPS spectrum of a chemically cleaned surface typically has mixture of As_2O_3 and Ga_2O_3. As_2O_3 is identified using XPS by a 3 eV chemical shift toward higher binding energy of the As $2p_{3/2}$ peak with reference to the As peak of the GaAs substrate, whilst the Ga $2p_{3/2}$ peak of Ga_2O_3 has a 1 eV chemical shift toward higher binding energy with reference to the Ga $2p_{3/2}$ peak in GaAs. A comparison of *a* and **b** in Fig. 3(A) show that a 20-minutes hydrogen plasma exposure removes nearly two-thirds of the As_2O_3; however it does not cause any detectable removal of the Ga_2O_3. After the 20 minutes exposure, that all of the As $2p_{3/2}$ and Ga $2p_{3/2}$ peaks shift 0.25 eV toward higher BEs. The fact that both core levels shift in the same direction and by the same amount indicates a change in energy of the electronic states and surface bands. This shift toward higher BE of both As and Ga substrate and oxide peaks was observed repeatedly for n-GaAs (110), and demonstrates a flattening of the surface bands relative to the initial oxidized surface. As shown in the traces labeled *c*, additional processing to remove nearly all of the As-oxide, but leaving a Ga-oxide rich surface, caused an eventual shift of the peak positions by ~0.40 eV to higher BEs from the initial surface. Paralleling the studies on GaSb shown in Fig. 1, for GaAs we find that hydrogen reduces the less strongly bonded As-oxide much more readily than Ga-oxide.[4] When the surface As-oxide and elemental As are removed from GaAs at room temperature (as in *c*), band flattening at the GaAs surface, associated with fewer mid-gap states and therefore less surface Fermi level pinning can be attributed to a reduction of As, and As-oxide related surface states, as well as hydrogen termination.[5] This passivation effect has been previously observed by *in situ* photoluminescence experiments.[6]

Heating during plasma processing expedites the removal of Ga-oxides and also affects the positions of the Ga and As, GaAs substrate peak positions. For example, spectra labeled *e* show the results of heating the sample to 350°C during a 20 minutes exposure to plasma-generated H. The As peak moves ~0.48 eV to lower BE, and the Ga peak shifts ~0.39 eV, also toward lower BE. In addition, the peaks become narrower and more symmetric. An additional 20-minutes of plasma processing at a sample temperature of 350°C (see the spectra labeled *f*) produces the maximum shift observed toward the position of a bare pinned surface. During this processing step the Ga-oxide is significantly reduced demonstrating that heating accelerates the reduction of Ga-oxide, but also increases band bending. This band bending change can be explained as follows: initial band flattening after room temperature processing can be attributed to the removal of unstable surface carbon, As-oxides and free As, all of which were previously thought as the origins of high interface mid-gap states.[6] Following this, when a sub-monolayer Ga-oxide covered GaAs surface is exposed to highly reactive hydrogen plasma at higher temperature (350°C), the plasma-generated hydrogen not only further reduces the Ga-oxide, but also attacks substrate GaAs by etching the GaAs, and generating volatile Ga-H and As-H species. This last step creates surface defects, therefore inducing electronic states in the middle of the band gap, which in turn cause surface band bending with the Fermi-level heavily pinned in the middle of the band gap.

Figure 3(B) contains AES spectra of GaAs (110) before and after a remote RF hydrogen plasma exposure of 5 minutes. 100 sccm He flows through plasma tube and 20 sccm of H_2 goes through down stream gas ring; the process pressure is 30 mTorr and RF power is 50 W. After this exposure trace amounts of C and O can still be detected. The purity of the H_2 was checked with a differentially pumped mass spectrometer. No gas phase contaminants were detected up to pressures of 100 mTorr., indicating that the gas delivery system was leak tight. With down stream injected H_2, there is little chance of quartz tube wall corrosion. This has been detected in other experiments with H_2 delivered through the plasma tube. We therefore believe the trace amount of oxygen, which was routinely seen, after the downstream H_2 injection comes from strongly-bonded Ga-oxide, which is not chemically reduced.

The observation of (1x1) LEED patterns (see Fig. 3(C)) shows that these surfaces have long range order, while the diffuse background suggests that this order may be limited in a small surface domains. This is consistent with the XPS results which show that final chemically-cleaned surfaces are electronically damaged. Both AES and XPS show that there is an initial rapid reduction of the carbon and oxygen signals, followed by a slow removal of surface oxygen by additional processing. This can be clearly shown in the XPS data where less strongly bonded species like As-oxide and Sb-oxide are removed even at room temperature; however, the more strongly bonded Ga-oxide is reduced slowly at higher temperatures (typically 350°C to 430°C). We believe the final cleaning quality is determined by the purity of the process gases, as well as the base pressure of the vacuum systems. At the final stage of surface cleaning, taking GaAs as an example, there can be competitive reactions of reduction and reoxidation due to residual oxygen and water vapor in the vacuum ambient. Reoxidation becomes significant at final stages of the cleaning process. The

oxidation and reduction rates for both As-oxide and Ga-oxide are different and they *compete* to determine what remains on the processed surface. For a surface like GaP, which has much slower oxidation rate than GaAs, the final cleaned surface (see Fig. 2(A), trace *d*) is often significantly less oxidized than GaAs (see Fig. 3 (B)) as revealed in the respective AES spectra.[7]

In conclusion, the use of plasma-generated hydrogen demonstrates a significant cleaning effects on all of Ga-based III-V semiconductor surfaces studied as revealed by AES and XPS spectra, and LEED. Reoxidation during the hydrogen plasma process plays a significant role in determining the final cleanliness of these surfaces. However, a chemically clean and structurally ordered III-V surface is difficult to obtain due to the differences in the reactivity and stability of the different native oxide constituents, e.g., As_2O_3 and Ga_2O_3.

ACKNOWLEDGMENTS

This research is in part supported by ONR, NSF and the North Carolina SCOE. RMO would like to acknowledge support from AFOSR/DARPA.

REFERENCES:

1. A. Takmori, Sugata, K. Asakawa, E. Miyauchi and H. Hashimoto, Jpn. J. Appl. Phys. **26**, L142 (1987); S. V. Hattangady, R. A. Rudder, M. J. Mantini, G. G. Fountain, J. B. Posthill and R. J. Markunas, J. Appl. Phys. **68**, 1233 (1990).

2. T. Yasuda, Y. Ma, S. Habermehl, and G. Lucovsky, Appl. Phys. Lett. **60**, 434 (1992).

3. Z. Lu, M. T. Schmidt, D. Chen, R. M. Osgood, Jr., W. Holber, D. V Podlesnik, J. Forster, Appl. Phys. Lett. **58**, 1143 (1991).

4. The heat of formation is F=-238 kcal/mol for Ga_2O_3, -136 kcal/mol for As_2O_3, and -166.5kcal/mol for Sb_2O_3 from CRC Handbook of Chemistry and Physics, 60 th ed. (Chemical Rubber, Boca Raton, FL, 1979), p-D-45.

5. See for example, S. D. Offsey, J. M. Woodall, A. C. Warren, P. D. Kircher, T. I. Chappell and G. D. Pettit, Appl. Phys. Lett. **48**, 475 (1986).

6. R. A. Gottscho, B. L. Prepernau, S. J. Pearton, A. B. Emerson, and K. P. Giapis, J. Appl. Phys. **68**, 440 (1990).

7. K. Navratil, Czech J. Phys. **B18**, 266 (1968); Y. Kato, K. M. Geib, R. G. Gann, P. R. Brusenback, and C. W. Wilmsen, J. Vac. Sci. Technol. **A2**, 588 (1984).

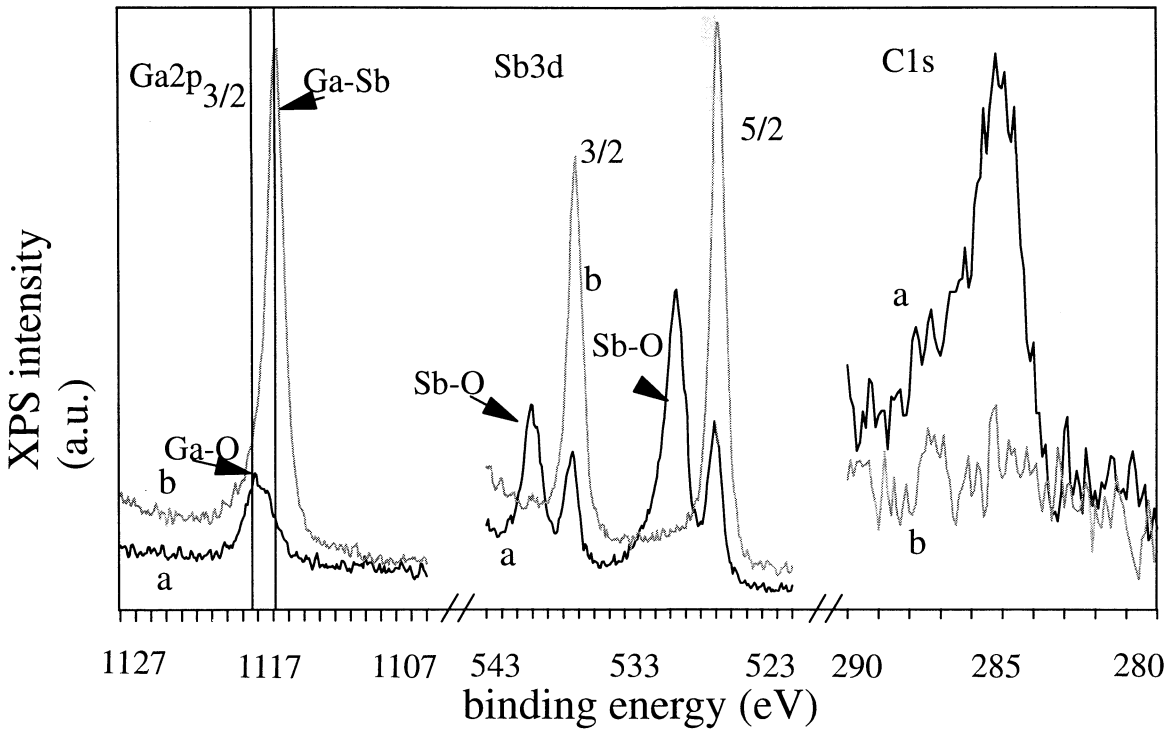
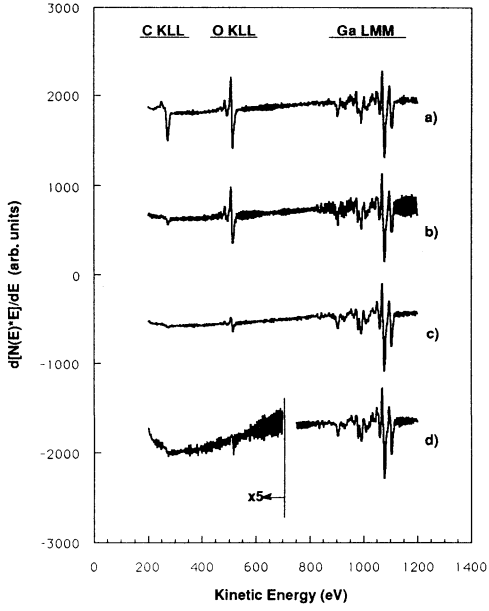


Figure 1: Processing of GaSb surfaces. a: treated 50% NH4OH b: exposed to an ECR-H at room temperature for 30 min.

(A)



(B)

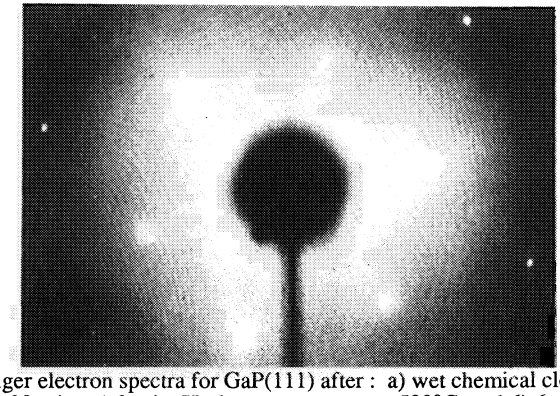


Figure 2: (A); Auger electron spectra for GaP(111) after : a) wet chemical cleaning, b) 530°C anneal, for 20 min., c) 2 min. H-plasma exposure, at 530°C, and d) 6 min. H-plasma exposure, at 530°C; (B) LEED image of GaP(111) after 6 min. H-plasma.

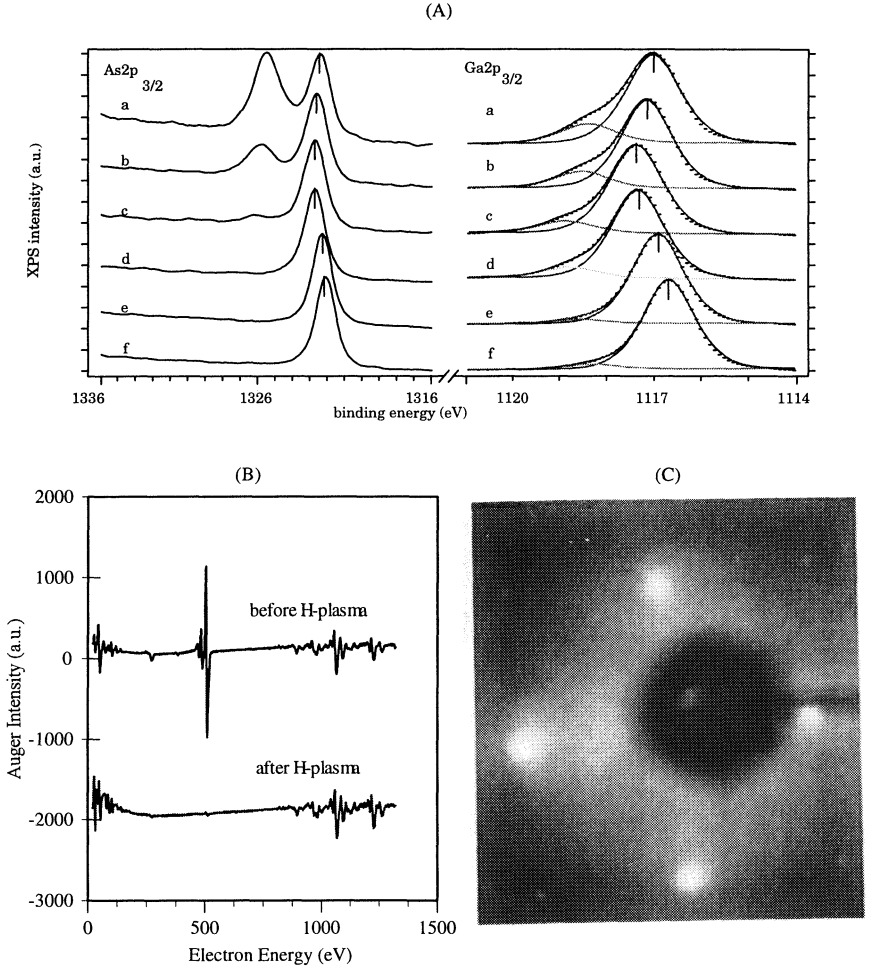


Figure 3: (A) XPS spectra of the As2p$_{3/2}$ and Ga2p$_{3/2}$ core levels:a)for the initial surface prepared by 50% NH_4OH (1 min.) after solvent cleaning; b) after ECR-H plasma processing for 20 min. at room temperature(RT); c)with an additional 20 min. exposure at RT; d) another 15 min, at RT; e) after an additional 20 min. processing at 350^{o}C; f) final 20 min. processing at 350^{o}C; B)Auger spectra of GaAs(110), a) before and b) after remote H-plasma cleaning; C) LEED image of GaAs(110) after 30 sec. remote rf H plasma.

PARTICLE CONTROL

PREVENTION OF PARTICLE DEPOSITION IN HF SOLUTION

A.Saito, K.Ohta, H.Itoh and H.Oka

Production Engineering Research Laboratory
Hitachi, Ltd.
292 Yoshida-cho, Totsuka-ku,Yokohama 244, JAPAN

A serious problem for LSI fabrication is that particles very easily adhere to the Si wafer in hydrofluoric acid(HF) solution. It was clarified that this is due to the zeta potential of the Si wafer and a particle becoming high. To prevent particle deposition, a new method for HF solution using an anionic surfactant, called "zeta potential control", was developed. When the surfactant is added to the HF solution, the number of deposited particles was reduced to less than one fifth.

INTRODUCTION

As semiconductor devices are finely fabricated, the deposition of small particles deteriorates the production yield. A serious problem now is that particles very easily adhere to the Si wafer in hydrofluoric acid (HF) solution. It is thought to be because the zeta potential of the Si wafer and a particle become high.

The mechanism of particle deposition in wet processes has been clarified[1]. The particle deposition depends on the balance of van der Waals force and the electrical repulsive force between the substrate and a particle. The ionic strength of the solution, zeta potential of the substrate and a particle, and particle size influence the particle deposition. Most particles are charged negatively, so when the zeta potential of the substrate and a particle become high (the value of zeta potential is nearly zero), the particle easily adheres to the substrate. The zeta potential of a Si particle depends on its surface situation. The zeta potential is thought to become high when the native oxide of the particle surface is removed in HF solution. So particles very easily adhere in HF solution.

Therefore it is very important to control the zeta potential of the substrate and the particle. A novel method for prevention of particle deposition was proposed at the 179th meeting which was held in spring 1991[2]. That method was called "zeta potential control". Particles are prevented from adhering to the Si wafer by controlling their zeta potential.

The zeta potential can be changed by adding organic solvent to the water. But, this is not effective in the case of etching solutions such as HF solution.

In this paper the effect of adding anionic surfactant (surface active agent) to the HF solution was investigated. The relationship between the zeta potential and the particle deposition is also discussed.

EXPERIMENTAL

1 μm-size Si particles (Ko-jundo Kagaku) were used as dispersing particles, and n-type Si wafers (Shin-etsu Kagaku) as substrate. Several anionic surfactants were used as shown in Table 1.

The zeta potential of the particle was measured by electrophoresis[3] using LASER ZEE TM MODEL 501 (Pen kem). The surface energy of pure water containing surfactant was measured by Du Noüy tensiometer. The contact angle of pure water containing surfactant on Si wafer was measured after the wafer was dipped in HF solution to remove the native oxide.

The particle deposition experiment was performed as follows. A Si wafer was dipped into the various concentrations of HF solution with dispersed Si particles. The number of particles deposited on the wafer was measured using laser inspection system LS-6000(Hitachi). The same treatment was made after adding the surfactant.

RESULTS AND DISCUSSION

Surfactants in pure water

Fig.1 shows the zeta potential of a Si particle versus the concentration of surfactants in pure water. The zeta potential was changed to the lower value as the anionic surfactant was added. This is because the surfactant adsorbed on the Si surface. Surfactants containing fluorine atoms were more effective in changing the zeta potential.

Surfactants can change the surface energy of liquid. Fig.2 shows this effect in pure water for the surfactants used in Fig.1. There was good coincidence between the zeta potential and the surface energy except for surfactant No.2. Although it has the ability to change the surface energy, the zeta potential was not changed as shown in Fig.1.

The adsorption of the surfactant on the Si surface must be considered. Next the contact angle of the water containing the surfactant on the Si

wafer was measured. As shown in Fig.3, the contact angle of surfactant No.2 did not decrease, which means it does not adsorb well on the Si surface. This is the reason why the zeta potential was not changed using surfactant No.2. The zeta potential change of a Si particle can be explained by both the surface energy change and the adsorption of the surfactant on the Si surface.

Surfactants in HF solution

The zeta potential of a Si particle in HF solution was measured. Ammonium perfluoroalkyl carboxylate was used for the HF solution because it was the most effective for changing the zeta potential in pure water.

Fig.4 shows the zeta potential of a Si particle versus the concentration of HF solution. The zeta potential became high as the concentration increased. In low concentration, the surface of the Si particle was covered by native oxide, so its zeta potential was almost the same as a non-treated Si particle. As the concentration of HF increased, the thickness of native oxide decreased and the zeta potential became high. In 0.5% HF, the surface is almost free of native oxide and the zeta potential was nearly zero.

When the ammonium perfluoroalkyl carboxylate was added to the solution, the zeta potential of a Si particle became low because of adsorption of the anionic surfactant on the Si surface. It was shown that the surfactant was also effective in HF solution as well as in pure water.

Fig.5 shows the relationship between the number of deposited particles and the concentration of HF solution. The number of deposited particles was smaller below 0.1% HF than above 0.1%. This is because the zeta potential of the Si wafer and a particle was not so high that particles did not adhere to the Si wafer. Particle deposition below 0.1% HF is attributed to the wettability of the Si wafer. When the wettability is good, the water containing particles attaches to the wafer. These particles remain on the wafer after the drying process[4].

When the surfactant was added to the HF solution, the number of deposited particles decreased, which corresponded to the zeta potential change shown in Fig.4. The number of deposited particles was reduced to less than one fifth.

CONCLUSION

The particle deposition in HF solution was clarified. Particles easily adhered to the wafer because of the high zeta potential. When the anionic

surfactant was added to the solution, particles did not adhere because the zeta potential became low.

REFERENCES

[1]A.Saito et al. :Proceedings of Microcontamination Conference and Exposition 91 (1991) p.562-569
[2]A.Saito et al. :Proceedings of the Third International Symposium on VLSI Science and Technology (179th Meeting of ECS, 1991) p.749-754
[3]A.Delgado et al. : Acta Polymerica, 37, p.361-364 (1986)
[4]L.D.Michaels et al. :Proceedings of Microcontamination Conference and Exposition 88 (1988) p.184

Table 1 Surfactants used for experiment

No.1	Tri-(2-hydroxy ethyl) ammonium dodesylbenzene sulfonate
No.2	Tri-(2-hydroxy ethyl) ammonium dodesyl sulfate
No.3	2-hydroxy ethyl ammonium octyl sulfate
No.4	Ammonium perfluoroalkyl sulfonate
No.5	Ammonium perfluoroalkyl carboxylate

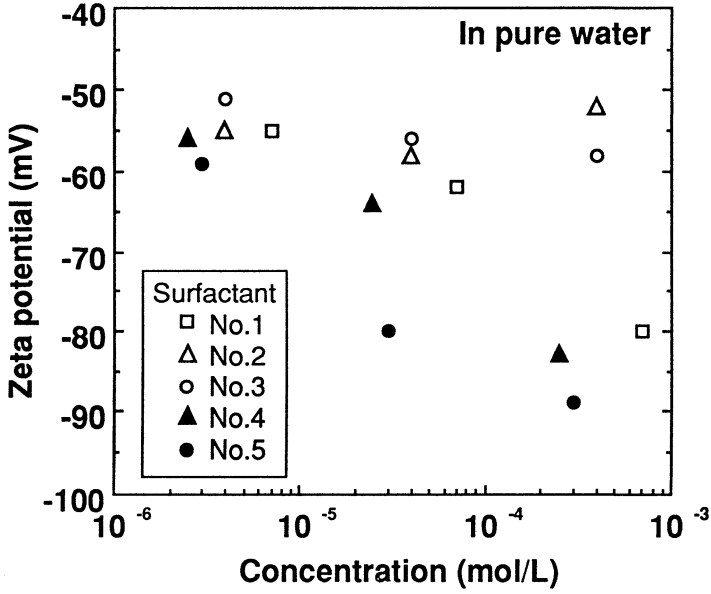


Fig.1 Relationship between zeta potential of Si particle and concentration of various surfactants

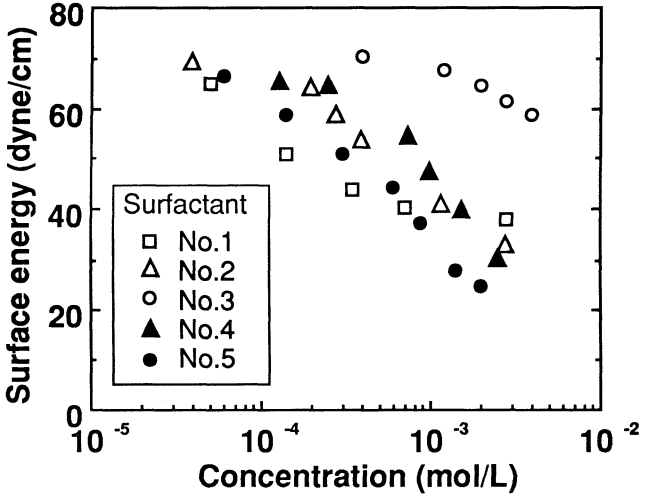


Fig.2 Relationship between surface energy and concentration of surfactant

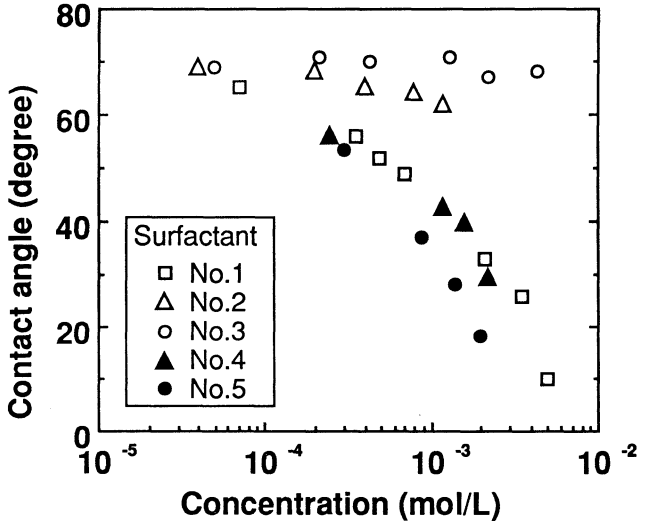


Fig.3 Relationship between contact angle and concentration of surfactant

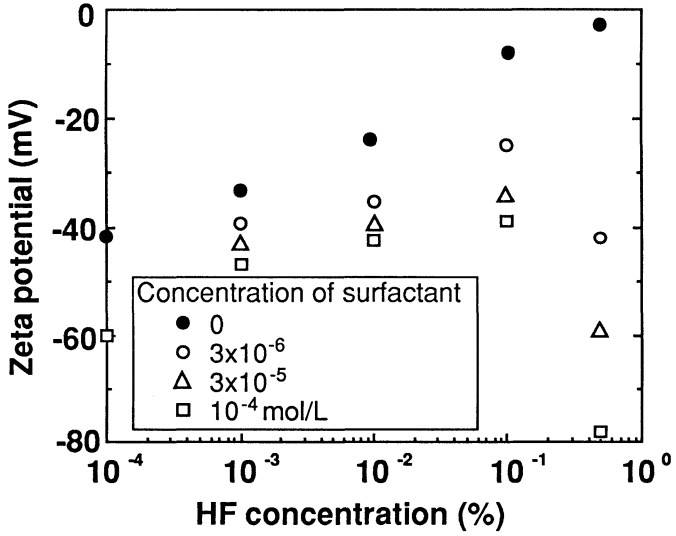


Fig. 4 Zeta potential of Si particle in HF solution

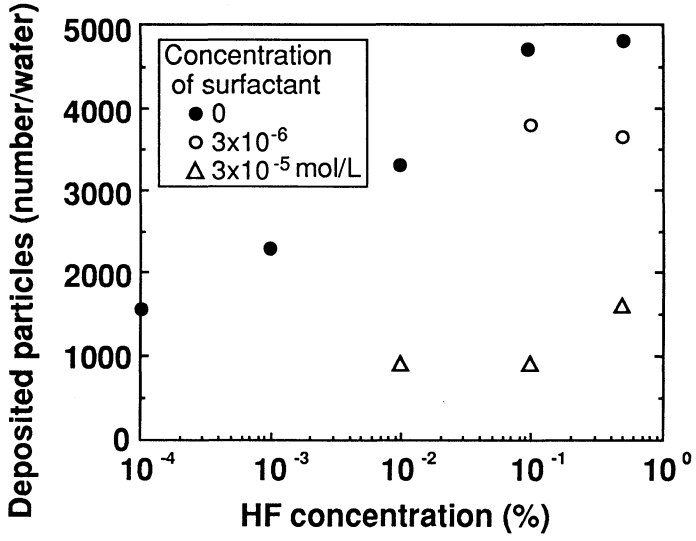


Fig.5 Particle deposition in HF solution

A NEW METHOD FOR SIMULTANEOUS CHARACTERISATION OF PROCESS CLEANLINESS AND TRUE PARTICLE REMOVAL EFFICIENCY

N.E. Henelius, H. Ronkainen**, O.J. Anttila* and J.M. Molarius***
**Okmetic Ltd. Sinimäentie 12, 02630 Espoo, Finland*
***VTT Semiconductor Laboratory Olarinluoma 9, 02200 Espoo, Finland*

Many experiments in wafer cleaning technology rely on comparing wafer particle counts before and after processing steps. The number of particles often changes dramatically, but there are more difficult cases where the variations appear slight. They need to be analysed in greater detail by separating the effects of true particle removal efficiency and process cleanliness. A new method for rapidly accomplishing this, utilising powerful PC-based software and a modern light point defect counter, is here presented for the first time. Other possible applications, related to crystal material quality, include improved analysis of oxidation induced stacking faults, crystal originated particles, minority carrier recombination lifetime and oxygen precipitation behaviour.

INTRODUCTION

Experiments and process development in wafer cleaning technology often rely on comparing wafer particle counts before and after processing steps. In many cases a huge reduction in the number of particles occurs, and the process is characterised by *particle removal efficiency* (case A, fig. 1.). In other cases an equally obvious increase in the number of particles is seen (case B, fig. 1.), especially if the step is repeated several times. The process is characterised by the number of *particles added per wafer per pass* (PWP) [1]. In reality, however, there are often processes where the particle levels change only slightly (case C, fig. 1). Significant particle deposition and removal processes, only marginally affecting the total number of particles, may still occur. We aimed at finding an efficient and thorough method for comparing wafers before and after processing steps, particle-by-particle. Particles would have to be identified as:

1. *Removed particles*, existing before the process and eliminated by it.
2. *Fixed particles*, present before the process and not moved by it.
3. *Added particles*. These are added during or after the process.

This classification would make it possible to calculate *true particle removal efficiency*. Applying this method to real processes would have to result in a clear picture

of particle deposition and removal taking place, which is useful information when developing and trouble-shooting equipment and processes. Decisions could then be made whether to enhance cleanliness or particle removal efficiency.

IMPLEMENTATION

The light point defect (LPD) counter used is a Censor ANS-100 [2]. Mechanically it works by placing the wafer to be scanned on a movable vacuum chuck by a robotic arm. Laser light is focused onto the wafer into a spot size of 30×200 μm^2. The chuck is simultaneously rotated and translated with the result that the laser spot describes a spiral path on the wafer. The scattered light is detected and expressed as ppm of the incident light. The whole wafer scan is stored in an array of 256×256 pixels. The width of a pixel is thus about 800 μm on a 200 mm wafer but only 400 μm on a 100 mm wafer.

The instrument is sensitive, capable of detecting particles smaller than 0.1 μm, and has a high counting accuracy. The spatial resolution is good and the size and position information of each detected LPD is stored. It is a highly advanced instrument compared with the instruments of the previous generations. We felt, however, that it should be possible to develop more sophisticated ways of analysing the tremendous amounts of data generated by the measurements, than provided by the original Censor software.

An MS Windows™ software package written in C++, VTTWAFER, was adapted for reading and analysing Censor ANS-100 data files. Special emphasis was placed on speed, flexibility and graphics. Many different types of analysis can be performed, each in its own specially designed window. The Haze Window is the normal starting point, single wafer files can be opened and haze or LPD maps displayed using a number of different colour palettes. Features include zooming, filtering, file comparison, haze and LPD bin definiton and freely definable edge and flat exclusions. Multiple files can be opened for exporting the haze and LPD bin distribution data to spreadsheets for further analysis.

The Particle Window is designed for comparing LPD maps. Two wafers, or two sets of wafers, can be compared for common (matched) particles. Particle patterns are compared and optionally moved and rotated to find the maximum number of particles having the same, or nearly the same position, in both sets. This is done because of the inescapable differences in wafer positioning even between subsequent measurements; the same particles will not necessarily end up in the same pixels when a measurement is repeated. Particle reduction may be applied, by which particles in adjacent pixels are reduced to one (the biggest). This will in many cases give truer results as "shadowing" is eliminated. The user may also decide how large size differences will be allowed during matching.

The Batch Window allows 2D or 3D representation of batch data. Data can be averaged over multiple wafers. Particle matching between two different batches can be done in this window which means that it is possible to show e.g. the average 2D distribution of particles removed from a cassette of wafers during a process step.

The analysis capability of VTTWAFER is enhanced by an option to import data from other types of measurement equipment.

APPLICATIONS

We have been developing and using VTTWAFER for analysing particle-related experiments for over one year now. The effort has been worthwile, VTTWAFER has provided us with important in-sights, fast process evaluation, and above all it has been possible to convincingly convey experimental results.

The reliability of the particle matching concept can be questioned. However, repeated measurements of the same wafer show that, unless it has been subject to bad storage or treatment, the number of unmatched particles is generally below 2 to 5 % on consecutive measurements. In these cases the unmatched particles usually are distributed close to the lower limit of the dynamic range. They can then easily be explained by small variations in particle sizing.

Some problems have also occured, e.g. once the particle matching failed completely when remeasuring a set of wafers after an interval of two months. We found that the zero position of the vacuum chuck of the ANS-100 had changed over time.

Comparing Megasonic Units Using True Particle Removal Efficiency

Two cassettes of similarly contaminated wafers were measured with the ANS-100 (particles > 0.2 μm). They were processed in two different Megasonic units, of which unit B was newly installed, and then re-measured. The total particle count decreased for unit A and increased for unit B (fig. 2). VTTWAFER, however, showed that most particles present after processing in unit A were present before the cleaning (i.e. fixed), while most particles present after processing in unit B were added during the cleaning (fig. 3). The average true particle removal efficiency for Megasonic unit B (52 %) was thus significantly greater than for Megasonic unit A (42 %). Fig. 4 shows a small area of a processed wafer featuring removed, fixed and added particles.

Comparing total particle counts before and after processing would in this case have been totally misleading because of the difference in cleanliness between the two Megasonic units. However, using VTTWAFER it was still possible to conduct relevant experiments while waiting for unit B to clean up. This was of great value working in a

production environment where time allocated to experimental work necessarily is a scarce resource. The difference in removal efficiency between the two Megasonic units remained after the cleanliness of sytem B was improved.

Characterising Particles by Annealing

Knowledge of particle composition can be valuable when eliminating particle sources. VTTWAFER's particle matching features can be utilised for this purpose. We tested the concept by annealing wafers (10 min, 1050 °C, Ar ambient) contaminated with particles assumed to be either silica polish residue or plastics from liquid tubing. The particle patterns remained almost unchanged proving that the particles were not easily evaporated (e.g. plastic). The same wafers were annealed once more, this time in an ambient containing 10 % oxygen. Again almost no changes in the particle patterns were observed, thus indicating that the particles were not organic.

Studying Particle Patterns

Sometimes particles appear in more or less distinct patterns on wafer surfaces. These patterns will often appear much more clearly when averaged over multiple wafers, suitably filtered and displayed in 2D or 3D. Fig. 5 displays the distribution of particles, averaged over one cassette of wafers, after cleaning in a spray post system. The concentration of particles is much larger in the central regions of the wafer. This may be due to uneven distribution of chemicals on the wafer surface. The picture thus gives a clue on how to improve the process.

VTTWAFER also offers the possibility of combining particle-to-particle comparisons and averaged 2D or 3D distribution maps. That may be helpful in characterising both cleaning processes (removed particles) and processes such as wafer storage and transport that may cause contamination (added particles). Fig. 6 shows the distribution of removed particles from one cassette of wafers held stationary above a megasonic transducer. A slightly higher number of removed particles can be observed in the beam area (perpendicular to the flat), but the differences between different wafer areas are surprisingy small. Fig. 7 displays the averaged distribution of added particles after a hermetically sealed cassette of wafers was dropped from a height of one meter. VTTWAFER revealed that the original particles were not affected but that the impact generated some large particles, probably originating from the cassette. Their distribution is centered close to the area of impact.

Characterising Semiconductor Material Properties

The data analysis capability of the software can also be used for visualising crystal material properties measured using an LPD counter or other suitable tools. These

properties include oxygen and carbon concentrations, resistivity, oxidation induced stacking fault (OSF) density, minority carrier recombination lifetime (τ) and crystal originated particle (COP) density. Fig. 8 shows an LPD map featuring a fairly high density of OSF's in a circular formation close to the wafer periphery. The radial OSF density distribution from the same wafer is shown in fig. 9. The stacking faults were made visible through wet oxidation followed by a 4-minute defect etch (Wright). Very low OSF densities, well below $1/cm^2$, can easily be measured if the defect contrast is enhanced by a short chemo-mechanical polish after the etch. The COP density can be visualised in a similar way, but in this case the possibility of comparing LPD maps before and after the slightly etching clean [3] is of great help. Fig. 10 shows a minority carrier recombination lifetime map, measured using a SEMILAB WT-85 system [4] and imported to the VTTWAFER software. Far more advanced data analysis can be performed, e.g. data from several wafers, of the same crystal, can be combined to yield a lifetime map for any crystal cross-section. Lifetime measurements can also be used to evaluate the oxygen precipitation behaviour and its uniformity. In fig. 11 the distribution of nuclei for precipitation is made visible by first submitting the wafer to a dry oxidation (4h@850 °C plus 12h@1000 °C) and then measuring the lifetime, which has been reduced by precipitation. The radial structure is a result of the crystal growing process.

The possibility of presenting data from several different instruments in a clear and standardized fashion makes it easier to find correlations between different properties and thus to optimise crystal material quality.

CONCLUSIONS

It is obvious that advanced software can significantly increase the value of the information provided by modern LPD counters. Particles can be classified as removed, fixed or added by comparing wafer LPD maps before and after processing. This allows the calculation of true particle removal efficiency, even under circumstances where process cleanliness is not established. This concept has a number of applications in research and process development related to wafer cleaning, storage and transport. A wide range of other applications exist in the area of semiconductor material characterisation.

REFERENCES

1. B.J. Tullis, Microcontamination, p. 67, Nov 1985
2. E.F. Steigmeier and H. Auderset, Appl.Physics A, p. 531, 1990
3. Y. Shimanuki, "Crystal-Originated Particles (COP)", Ultra Clean Processing of Silicon Surfaces UCPSS '92
4. WT-85, Manuals, Semilab RT, H-1047 Budapest, Foti ut 56, Hungary

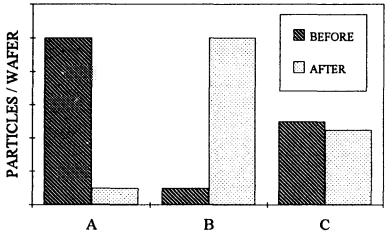


Figure 1. Three different cases (A, B, C) showing how processing can affect the number of particles on wafers.

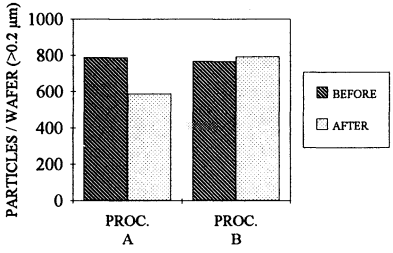


Figure 2. The average number of particles / wafer / cassette, before and after two different processes. Proc. A appears better at particle reduction, but this is not the truth, as revealed by fig. 3.

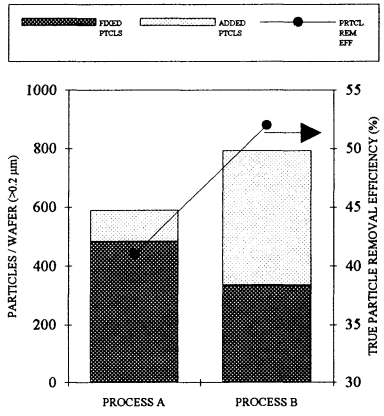


Figure 3. The particles of the processed wafers of fig. 2, classified as either fixed or added by PC software analysis of particle maps measured with the Censor ANS-100. The cleanliness of process A is superior, as shown by the smaller number of added particles. *Process B is revealed to be better at removing particles.*

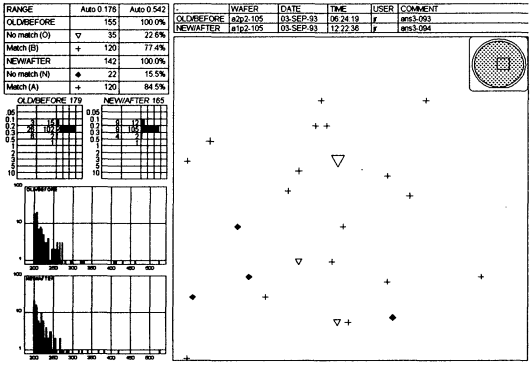


Figure 4. A small area of an LPD map based on two measurements, the wafer processed in between. The particles removed are shown as unfilled triangles. The fixed particles, i.e. not affected by the process step, appear as crosses. The particles added are shown as filled diamonds. The size of the symbol indicate the size of the particle.

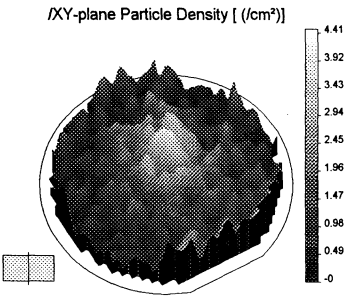


Figure 5. The distribution of particles, averaged over one cassette of wafers, after cleaning in a spray post system.

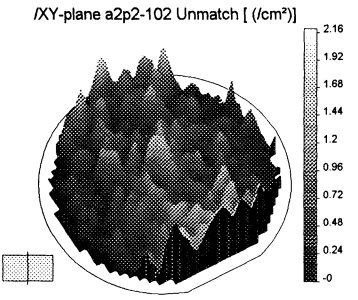


Figure 6. The distribution of removed particles from one cassette of wafers held stationary above a megasonic transducer.

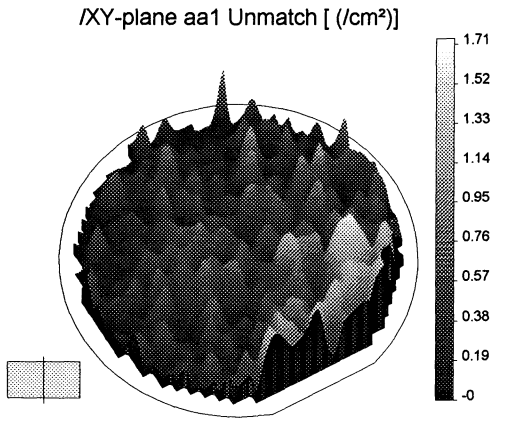


Figure 7. The averaged distribution of particles added to one sealed cassette of wafers by dropping the cassette from a height of one meter. The particles are fairly large and probably originate from the cassette. Their distribution is centered close to the area of impact.

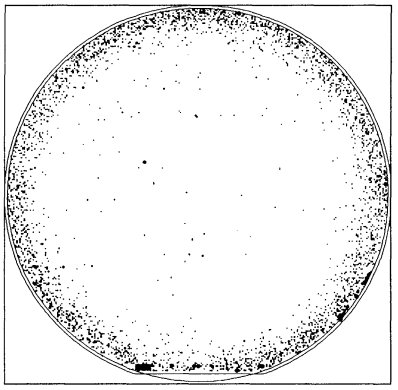


Figure 8. Oxidation induced stacking fault distribution (experimental crystal), made visible by a 4 min Wright etch and subsequent LPD scan.

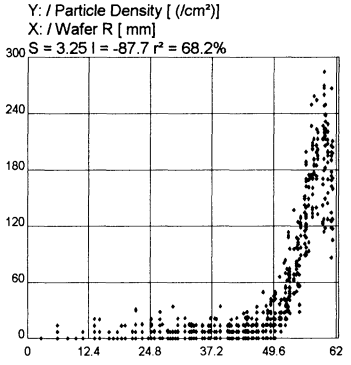


Figure 9. The radial distribution of the stacking faults on the wafer in fig. 8.

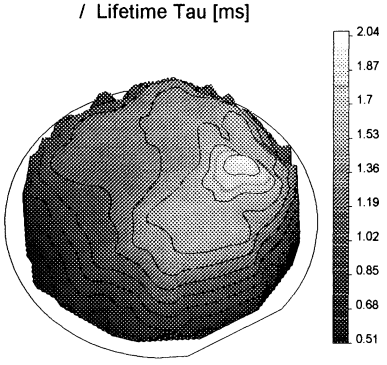


Figure 10. Minority carrier recombination lifetime map of a 30 Ωcm P100 wafer after dry oxidation (30 min, 900 °C). The high lifetimes recorded, almost 2 ms, indicate a very clean wafer with regard to metals.

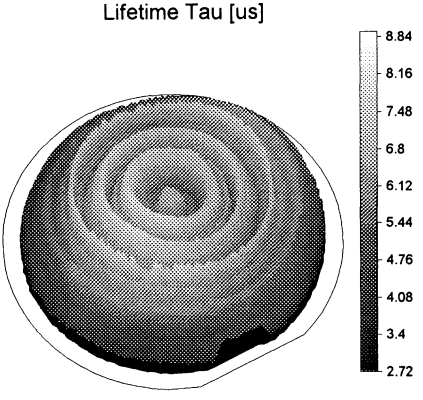


Figure 11. Oxygen precipitation behaviour can easily be monitored by oxidation (e.g. 4h@850 °C plus 12h@1000 °C, dry) followed by lifetime mapping. The ring structure originates from nuclei born during crystal growth.

ELECTROKINETIC CHARACTERISTICS OF NITRIDE WAFERS IN AQUEOUS SOLUTIONS AND THEIR IMPACT ON PARTICULATE DEPOSITION

Der'E Jan and Srini Raghavan
Department of Materials Science and Engineering
University of Arizona, Tucson, AZ 85721

ABSTRACT

A streaming potential cell for handling 5" wafers was fabricated and the interfacial electrical characteristics of LPCVD and PECVD silicon nitride wafers subjected to different cleaning procedures were measured using this cell. The isoelectric point (IEP) of silicon nitride was dependent on the cleaning method as well deposition technique. X-ray photoelectron spectroscopic measurement of Si/O and Si/N ratio of films were made to explain the difference in IEP values. Polystyrene latex (PSL) particle deposition from aqueous solutions onto silicon nitride wafers was investigated and correlated with the electrokinetic potential data.

INTRODUCTION

Silicon nitride films are widely used in integrated circuit processing as passivation and gate dielectric material, and as local oxidation masks. Low pressure chemical vapor deposition (LPCVD) and plasma-enhanced chemical vapor deposition (PECVD) are the most common techniques employed to deposit silicon nitride during device fabrication. LPCVD nitride films are typically deposited from a mixture of dichlorosilane and ammonia and are stoichiometric Si_3N_4 films with a Si/N ratio close to 0.75. On the other hand, PECVD nitrides deposited from a mixture of silane, ammonia and/or nitrogen have a composition of $Si_xN_yH_z$, where z is typically 0.2 to 0.3.

Nitride films are exposed to a variety of liquid chemicals during integrated circuit manufacturing. An important characteristic of a wafer surface that plays a key role in particulate contamination during wet chemical processing is its electrokinetic (zeta) potential. Particulate contaminant deposition onto the wafer surface depends on the nature of charge developed by the wafer and the contaminants in a given liquid medium. Specifically, electrical double layers develop at the wafer/liquid and contaminant/liquid interfaces, and the interaction of these double layers determine whether the contaminant may be attracted to the surface of the wafer or not. If the contaminant and the wafer surface are charged alike, the double layers will interact

in a repulsive manner making the deposition of the contaminant unfavorable. Colloidal contaminants will be attracted to the surface of the wafer, if the wafer and the contaminant are oppositely charged.

The measurement of electrokinetic data for "real" wafers has not been reported in literature. Electrophoretic data collected on particles have been used as representative values of wafers. The electrophoretic method is not suitable to characterize the properties of thin surface layers deposited under defined conditions.

The objectives of the research work reported in this paper were to develop a technique to characterize the electrokinetic potential of silicon nitride wafers processed in various aqueous cleaning solutions and to carry out particulate contamination studies on these wafers in an effort to correlate the electrical characteristics to particulate contamination. X-ray photoelectron spectroscopic measurement of Si/O and Si/N ratio of films has been made to explain the difference in IEP values of nitride wafers subjected to different cleaning treatments.

EXPERIMENTAL MATERIALS

Five inch LPCVD and PECVD silicon nitride wafers were donated by IBM corporation. The substrate for the nitride films was boron doped (100) silicon with a resistivity in the range of 10-20 Ω-cm. LPCVD nitride films (IBM trademark : ZI PAD) were deposited at 785 ± 10 °C and at a pressure 0.2 ± 0.02 Torr, using NH_3 (160 cc/min.), SiH_2Cl_2 (40 cc/min.) and N_2 (400 cc/min.) in a hot-wall tube reactor. The thickness of the films was measured to be 3000 ± 100 Å. The deposition of PECVD (IBM trademark : WC ASM) films was carried out in a parallel plate reactor operating at a temperature of 400 ± 7 °C , with NH_3, SiH_4 and N_2 flowing at a rate of 2000, 290 and 1200 cc/min. respectively. The thickness of PECVD nitride layers was 3600 ± 100 Å.

All chemicals used to clean the wafers were of electronic grade. H_2O_2 (30%), H_2SO_4 (95-97%), buffered oxide etch (BOE 100:1) and NH_4OH (27-31%) were purchased from Olin Hunt Specialty Products Inc.. Phosphoric acid (85-87%) was obtained from Jones-Hamilton and polystyrene spheres (0.5 μm) were bought from Duke Scientific Corporation. Electronic grade water from a Millipore RO-DI system (Milli-Q 4-bowl) was used to make the required electrolyte solutions. All electrolytes used for the regulation of ionic strength and pH were of electronic grade.

EXPERIMENTAL METHODS

Silicon nitride wafers were subjected to the following chemical treatments: (i)

piranha (H_2SO_4:H_2O_2 = 5:1) at a temperature of 90 ± 5 °C for ten minutes, (ii) RCA1 (NH_4OH:H_2O_2:H_2O = 1:1:5) at a temperature of 80 ± 5 °C for 10 minutes, (iii) piranha followed by BOE (100:1) for 1 minute and (iv) treatment (iii) followed by a ten minute phosphoric acid (180°C for LPCVD nitride film and 150°C for PECVD nitride film) clean. All cleaning treatments were carried out in a class 100 clean room at the University of Arizona.

A streaming potential cell capable of handling 5" wafers was specially designed and constructed for the zeta potential measurements. It was constructed from two ultra high molecular weight polyethylene (UHMWPE) blocks each with an accurately cut depression to take 5" wafers. A PTFE gasket of 14.7 cm in diameter and 0.076 cm in thickness was used to separate the silicon nitride wafers. An area of 0.8 cm x 14.2 cm was cut in the center of the gasket to create a liquid flow channel. The top block had suitable cutouts for liquid inlet and outlet ports and for electrode placement as shown in Fig.1. Two platinized platinum electrodes were located on the top block of the cell to measure the streaming potential. The platinum electrodes were regularly platinized using a 3.5 % (w/v) solution of chloroplatinic acid doped with 0.005 % w/v lead acetate to reduce the asymmetry potential generated between the electrodes due to polarization (1,2). A Paar EKA (Electrokinetic Analyzer) instrument was used to measure streaming potential values at pressure drop values ranging from 20-90 mbar. The slope of the streaming potential (E_s) versus pressure drop plot was automatically recorded and used to calculate the zeta potential according to the following equation:

$$\zeta = 4\pi\eta \frac{\kappa}{\epsilon} \times \frac{\Delta E_s}{\Delta p} \qquad (1)$$

In the above equation, η, ϵ,κ are viscosity, dielectric constant and conductivity of the solution, respectively.

Wagenen et al (3,4) and Bowen (5) studied the hydrodynamic requirements for accurate measurement of streaming potential using a flat plate configuration. According to their work, two main requirements must be met: (i) laminar flow in the channel and (ii) the length (L_e) of channel needed to generate the steady laminar flow must be less than 10 % of the total channel length (L). For the designed streaming potential cell, at the highest flow rate of 550 cc/min., the Reynold's number was calculated to be around 2000 indicating the existence of laminar flow conditions in the channel between the wafers.

A VG ESCALAB MKII photoelectron spectrometer with an aluminum anode ($K_{\alpha 1,2}$= 1486.6 eV) as the X-ray source was employed in the XPS analysis. The FT-IR spectra of nitride wafers were obtained with a Perkin Elmer 1800 Fourier-transform infrared spectrometer, in the region from 800 to 4000 cm^{-1}. During the

measurement, the sample chamber was purged with nitrogen gas to reduce moisture content. Twenty scans at a resolution of 4 cm^{-1} were signal averaged.

Particle deposition experiments were carried out in the cleanroom. The DI water contained in a 2-liter PTFE tank was spiked with a small predetermined volume of 0.5 μm polystyrene particle dispersion (3 x 10^7 particles/cc) to yield a particle level of 5,000 or 15,000 particles/cc. The pH of the DI water to which PSL particles were added was first adjusted to 9.7 and the precleaned nitride wafers were dipped in the contaminated water for 5 minutes and then dried by spinning. The number of polystyrene particles on the wafer was then counted using a Tencor 5000 surface scanner. The pH of the contaminated water was then sequentially adjusted to lower pH values and the deposition experiments were repeated.

RESULTS AND DISCUSSION

The hydrogen content of PECVD nitride wafers was first determined using the FTIR transmission technique. Fig. 2 shows the FT-IR spectrum of PECVD nitride wafer. Evidence for substantial amounts of bonded hydrogen may be seen from the strong absorption peaks characteristic of N-H and Si-H stretching at 3350 and 2160 cm^{-1}, respectively. Based on the method proposed by Lanford and Rand (6), the atomic density of hydrogen per unit area was calculated using the formula:

$$\text{Total H/cm}^2 = 1.36 \times 10^{17} \times (1.4 \times \text{area of N-H} + \text{area of Si-H}) \quad (2)$$

Using equation (2) and the thickness of nitride film, the hydrogen content of PECVD nitride films was calculated to be approximately 2.0 x 10^{22} atoms/cm^3 (or roughly 25 atomic %). The fraction of hydrogen present as Si-H was calculated to about 0.37. It may be mentioned that the fraction of hydrogen bonded to Si is a strong function of Si/N ratio in the feed gas stream (7,8). The hydrogen content of LPCVD wafers was also measured and was found to be approximately 4 atomic %.

Zeta potential values of LPCVD nitride wafers measured in 0.001 M KCl solution are shown in Fig. 3 as a function of solution pH. It is can be seen that the IEP (isoelectric point) values of LPCVD nitride wafers vary from 3.5 to 5.3 depending on the cleaning process. The wafers cleaned by piranha and RCA1 exhibit IEP values of 3.8 and 4.5,respectively. Since the hydrogen peroxide in both solutions is a strong oxidizer, the oxidation of nitride wafers during cleaning in these solutions may be expected. It has been shown that the IEP of SiO_2 film is in the pH range of 2.8 to 3.5 (2,9). The IEP of nitride wafer cleaned by piranha, and then etched by BOE to remove the thin oxide film grown on the nitride wafer during the piranha cleaning shifts the IEP to a pH of 5.3. This value most likely represents the real IEP value of the LPCVD nitride wafer. The wafer cleaned by piranha, BOE

and followed by a phosphoric acid etch to remove 2000 Å of silicon nitride layer exhibits an IEP value of 3.5. The reason for this low IEP value may be due to the adsorption of phosphate ions on the nitride wafer.

Zeta potential of PECVD silicon nitride wafers cleaned by different methods is shown in Fig. 4. The IEP values of PECVD wafers cleaned by piranha and RCA1 occur at pH values of 4.2 and 4.8 respectively, which are slightly higher than those of LPCVD nitride wafers. The wafers cleaned by piranha followed by BOE show an IEP of about 4.9 which is lower than that of the LPCVD nitride wafer subjected to a similar treatment. The zeta potential values of PECVD nitride wafers cleaned by piranha, BOE and then etched by phosphoric acid are negative in the pH range of 3.5 to 9.3.

In order to explain the difference in IEP values of LPCVD nitride films cleaned by different procedures, Si/O and Si/N ratios of the surface of the cleaned wafers was carried out using X-ray photoelectron spectroscopy (XPS). The XPS results are summarized in table I. The atomic densities were calculated by determining the areas under the peaks for each element divided the atomic sensitivity factors which are 0.42, 0.66 and 0.27 for N (1s), O (1s) and Si (2p) respectively (10). The results show that the nitride film cleaned by piranha followed by BOE has the largest Si/O and N/O values (lowest O content). The nitride film cleaned by piranha, BOE and then phosphoric acid has the lowest Si/O and N/O values. This indicates that the IEP value of nitride film decreases with increasing level of oxidation during the cleaning.

Table I Si/N, Si/O and N/O ratios of cleaned LPCVD wafers as determined by XPS.

Sample Treatment	Ratio			IEP
	Si/N	Si/O	N/O	
Piranha	0.77	2.99	3.88	3.7
Piranha, and then BOE	0.81	3.78	4.66	5.3
Piranha, BOE and then Phosphoric acid	0.80	2.53	3.16	3.5

In an effort to correlate the zeta potential values of wafers to the extent of particulate contamination, LPCVD nitride wafers cleaned by piranha and by piranha followed by BOE were dipped in DI water adjusted to different pH values containing

0.5 μm PSL particles at a concentration of 5000/ml and 15000/ml. The zeta potential values of PSL particles were previously measured to be -50 mV to -100 mV in the pH range of 3.0 to 10.0. Electrostatic adsorption of PSL particles onto the surface of nitride wafer would be favorable at pH values lower than the IEP of nitride wafer.

The results of the contamination experiments for LPCVD nitride wafers cleaned by piranha and piranha followed by BOE are shown in Fig. 5 and 6, respectively. From Fig. 5 it can be seen that the number of PSL particles on the nitride wafer cleaned in piranha increases with decreasing pH and changes sharply in the vicinity of the IEP value (3.5) of the wafer. Deposition appears to be favorable at pH values where the wafer has a positive zeta potential. The results for the wafers cleaned with piranha followed by BOE, shown in Fig. 6, also follow the general trend exhibited by the data in figure 5. Contamination increases sharply at pH values below IEP (5.3) for both concentrations of PSL particles. These results indicate that electrostatic interaction between PSL particles and wafers is a contributing factor for contamination. At pH values above IEP, electrostatic repulsion between negatively charged wafer and particles result in a substantial reduction in particulate contamination.

CONCLUSIONS

The zeta potential of 5" LPCVD and PECVD silicon nitride films was characterized using the streaming potential method. The results shows that the IEP of the silicon nitride films depends on the cleaning treatment. The IEP of the LPCVD and PECVD wafers cleaned by piranha followed by BOE are 5.3 and 4.9 respectively, and most likely represent the real IEP of the nitride wafers. Si/O and Si/N ratios determined using XPS reveal that the IEP value is affected by the level of oxidation that occurs during cleaning. Polystyrene latex particle deposition from aqueous solutions onto nitride wafers correlated with the zeta potential data. Electrostatic interaction between PSL particles and wafers appears to a contributing factor for contamination.

ACKNOWLEDGEMENTS

The authors wish to acknowledge the Sematech Center of Excellence at the University of Arizona for the financial support to carry out this work. Sincere thanks are extended to Dr. Kevin Albaugh for providing samples of wafers, Dr. Roger Sperline for consultation in FTIR analysis, Dr. Guy Hudson for the XPS analysis and Mr. Darrell Dunn for designing the 5" streaming potential cell.

REFERENCES

1. A. M. Feltham and M. Spiro, Chem. Rev., 71, 177 (1971).
2. P. J. Scales, F. Grieser and T. W. Healy, Langmuir, 8, 965 (1992).
3. R. A. Van Wagenen and J. D. Andrade, J. Colloid Interface Sci., 76, 305 (1980).
4. R. A. Van Wagenen and J. D. Andrade, J. Electrochem. Soc., 123, 1438 (1976).
5. B. D. Bowen, J. Colloid Interface Sci., 106, 367 (1985).
6. W. A. Lanford and M. J. Rand, J. Appl. Phys. 49, 2473 (1978).
7. H. J. Stein and H. A. R. Wegener, J. Electrochem. Soc., 124, 908 (1977).
8. E. A. Taft, J. Electrochem. Soc., 118, 1341 (1971).
9. Unpublished result.
10. M. P. Seah and G. C. Smith, in Empirically Derived Atomic Sensitivity Factors for XPS, D. Briggs and M. P. Seah, Editors, p. 635. John Wiley & Sons, New York (1990).

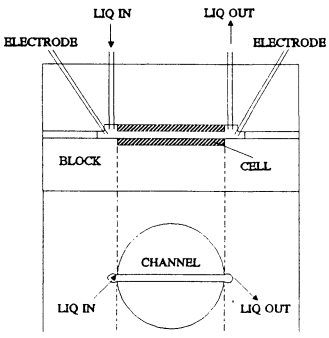


Fig. 1 A schematic sketch of the streaming potential cell for 5" wafers.

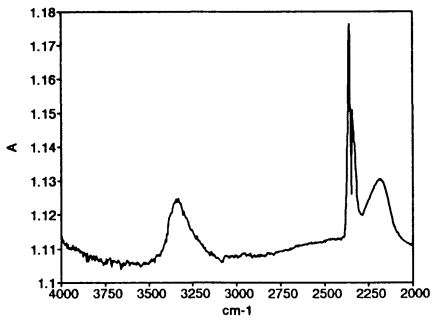


Fig. 2 FTIR spectrum of PECVD silicon nitride film.

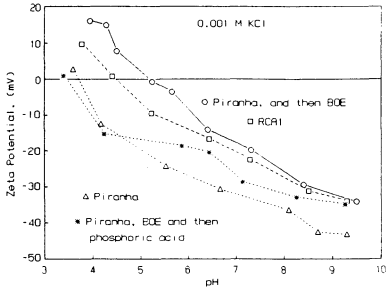


Fig. 3 Zeta potential of LPCVD nitride wafers cleaned by different methods as a function of solution pH.

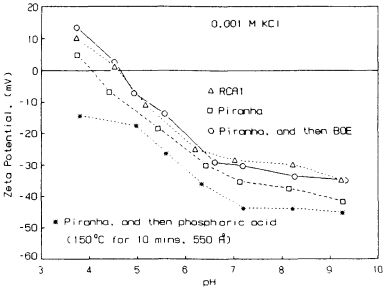


Fig. 4 Zeta potential of PECVD nitride wafers processed in various cleaning solutions as a function of pH.

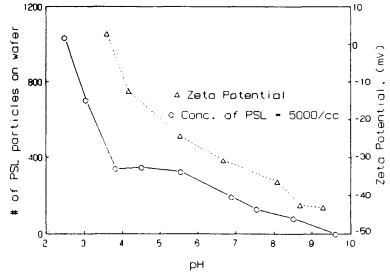


Fig. 5 Correlation between zeta potential values and PSL particle deposition on LPCVD nitride wafers cleaned by piranha.

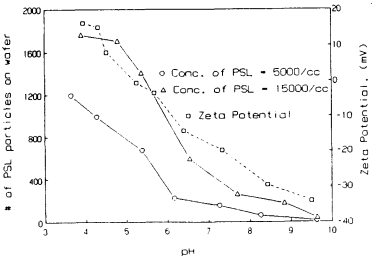


Fig. 6 Correlation between zeta potential values and extent of PSL contamination on LPCVD nitride wafers cleaned by piranha, followed by BOE.

A DESIGN OF EXPERIMENTS APPROACH TO AN OPTIMIZED SC-1/MEGASONIC CLEAN FOR SUB-0.15 MICRON PARTICLE REMOVAL*

P. J. Resnick, C. L. J. Adkins, P. J. Clews, E. V. Thomas, and S. T. Cannaday
Sandia National Laboratories
Albuquerque, NM 87185-5800

A statistical design of experiments approach has been employed to evaluate the particle removal efficacy of the SC-1/megasonic clean for sub-0.15 μm inorganic particles. The effects of megasonic input power, solution chemistry, bath temperature, and immersion time have been investigated. Immersion time was not observed to be a statistically significant factor. The NH_4OH/H_2O_2 ratio was significant, but varying the molar H_2O_2 concentration had no effect on inorganic particle removal. Substantially diluted chemistries, performed with high megasonic input power and moderate-to-elevated temperatures, was shown to be very effective for small particle removal.

INTRODUCTION

RCA cleans (SC-1 and SC-2) have been in existence for over 20 years and it is well known that the SC-1 clean, coupled with high frequency acoustic power (megasonics), effectively removes particles above 0.30 μm from silicon surfaces (1). However, it is not clear whether the SC-1 clean will adequately remove smaller particles on future generation devices with reduced design rules. As part of the work for the SEMATECH/Sandia Contamination Free Manufacturing Research Center, a statistical design of experiments approach has been employed to evaluate sub-0.15 μm particle removal efficacy of the SC-1/megasonic clean. Until recently, routine detection of smaller particles was not possible due to the limitations of surface particle metrology equipment. However, with the introduction of equipment capable of detecting particles well below 0.15 μm in size, it is now possible to experimentally assess the performance of the SC-1/megasonic clean for small particle removal. An extension of the SC-1/megasonic clean to the next generation technology for small particle removal would represent a significant cost of ownership savings for the industry.

The objective of the designed experiments was to understand any limitations to particle removal that may exist in the SC-1-type chemistry with the use of megasonics, and

* This work was performed at Sandia National Laboratories, which is operated for the U.S. Department of Energy under contract no. DE-AC04-76DP000789. This work was funded through a cooperative research and development agreement with SEMATECH.

to obtain an empirical response surface for process optimization. The effects of megasonic input power, solution chemistry, bath temperature, and immersion time on particle removal were investigated and are reported below.

EXPERIMENTAL

Prior to performing the designed experiments on the megasonic cleaning system, it was necessary to determine the number of particles that are contributed by the spin rinse dryer (SRD). A large number of added particles from the dryer would greatly reduce the signal-to-noise ratio, making data analysis difficult. A small experimental matrix was performed to assess the effects of spin speed, spin time, nitrogen flow (on/off), and heater (on/off) on particle addition from the Verteq 1600 SRD. This tool was operated in "dry only" mode in these experiments, as well as all subsequent experiments. Virgin 150 mm silicon wafers were immersed in a DI water cascade overflow bath and spun dry under various process conditions. A Tencor Surfscan 6200 was used to measure particles on the wafers. The dryer was found to contribute negligible numbers of particles (often less than 10) ≥ 0.13 micron in size, provided the nitrogen flow remained on.

Following the spin dryer evaluation, a screening experiment using a Verteq focused beam megasonic process tank was designed and performed to determine the main effects in the SC-1/megasonic clean. The wafers used in this, and all subsequent tests, were 150 mm Unisil, n-type $\langle 100 \rangle$ silicon wafers. A stable and reproducible "contaminant" particle source was required. Silicon nitride was chosen as a contaminant particle because it is difficult to remove, it is detectable on bare silicon, and it is representative of a semiconductor fab environment. Approximately 1000 silicon nitride particles in the 0.10 to 0.30 μm range were deposited on each wafer using an aerosol technique. The RCA process chemistry was varied from the standard concentration to one that was very dilute by changing both the weight fraction of hydrogen peroxide and the ratio of ammonium hydroxide to hydrogen peroxide. Megasonic input power ranged from 0 to 300 watts and bath temperature ranged from 25°C to 65°C. The wafer immersion time was evaluated in terms of its constituent components, which were chain speed and number of passes over the transducer. The chain speed refers to the speed at which the wafer cassette is physically transported over the transducer, and ranged from 25 to 70 mm/minute. The number of passes over the transducer ranged from 2 to 6. The resulting total immersion time ranged from 6 to 52 minutes. Seven wafers were processed in each run -- three wafers were contaminated with silicon nitride particles, two wafers were contaminated with ashed photoresist, and two wafers were uncontaminated (blanks). The ashed photoresist was intended to provide a response for a different (organic) particle, and the uncontaminated wafers were used to provide a blank correction to the particle removal data.

The cleaning efficiency is defined in terms of the removal of the added silicon nitride particles. A more rigorous expression for the cleaning efficiency is given in terms of the

number of light point defects (LPDs) added and removed. This terminology is used because it is often difficult to distinguish particles from other light scattering events (caused by surface roughness, for example) with conventional laser based scanning instruments. The cleaning efficiency, η, may be expressed as

$$\eta = \frac{\text{Light Point Defects Removed - B}}{\text{Light Point Defects Added}}, \qquad [1]$$

where B is the number of light point defects removed from the uncontaminated wafers (blank correction).

The screening experiment indicated that neither chain speed nor number of passes over the transducer (within the experimental range stated above) had a significant effect on particle removal. A confirmatory experiment, in which the only variables were chain speed and number of passes, validated this finding. All subsequent experiments were performed with a constant chain speed (44 mm/min) and two passes over the transducer, for a total immersion time of 10 minutes.

A full-factorial experiment was performed to determine the linear response and assess factor interactions. The bare (uncontaminated) wafers included in these runs were used to provide blank corrections to the data. The data from these runs indicate that megasonic power is a significant factor, as well as bath temperature and chemical ratio. The data also indicate interactions involving power. The full-factorial matrix was augmented with additional experimental points which allowed the fit of the data to a quadratic regression equation (third order terms and higher were not supported by the experimental design). These experimental matrices, along with the reduced results, are given in Table I. The results obtained from the ashed photoresist wafers were too irreproducible to obtain a regression fit; however, the data indicate that particle chemistry is significant.

The regression fit of the data indicated that input power was indeed the dominant factor, appearing in linear, quadratic, and interaction terms with bath temperature and chemical ratio. The effect of megasonic input power diminishes above ~150 W, at which point there appears to be little benefit from increasing power. Increased temperature substantially increased the particle removal efficiency, provided that the input power was below 150 W. The regression equation for particle removal efficiency, based on transformed parameters, is given as

$$f = \beta_0 + \beta_1 \mathrm{T} + \beta_2 \mathrm{P} + \beta_3 \mathrm{R} + \beta_4 \mathrm{P}^2 + \beta_5 \mathrm{T} \cdot \mathrm{P} + \beta_6 \mathrm{P} \cdot \mathrm{R}, \qquad [2]$$

where T is dimensionless bath temperature, P is dimensionless megasonic input power, and R is a logarithmic transform of the volume ratio of ammonium hydroxide to hydrogen peroxide. These parameters have been transformed into dimensionless quantities for orthogonal centering about zero through the following:

$$T = \frac{\text{temperature (deg C) - 45}}{20}, \qquad [3]$$

$$P = \frac{\text{power (watts) - 150}}{150}, \qquad [4]$$

$$R = \log_{10}\left(\frac{[NH_4OH]}{[H_2O_2]}\right) + 1.0. \qquad [5]$$

The function f is the predicted particle removal efficiency transformed through a modified logit function, which is used to constrain the response to values between 0 and 1. The inverse of the modified logit function is given in equation [6].

$$\text{Predicted Efficiency} = \frac{e^f}{(1+e^f)} + 0.01. \qquad [6]$$

The regression coefficients are given in Table II, along with the associated standard errors. Contour plots (generated from the regression) showing the dependence of cleaning efficiency on input power, bath temperature, and chemical ratio are presented in Figures 1 through 3 for a particle size range from 0.1 to 0.3 μm. The contour lines represent constant cleaning efficiency. Particle removal efficiency depends strongly on power when the input power is below about 150 Watts, as seen by the close spacing of the contour lines (below 150 W) in Figures 1 through 3. Cleaning efficiency also depends strongly on bath temperature, particularly at lower megasonic power levels. This phenomenon is shown graphically in Figure 4, where cleaning efficiency is seen to change rapidly with increasing temperature at low power, but at high power the cleaning efficiency is independent of temperature. Chemical ratio had only a moderate effect on particle removal, within the defined experimental space.

DISCUSSION

Power was found to be the dominant factor with respect to the cleaning efficiency of the megasonic/SC-1 cleaning system. The data have been presented thus far in terms of megasonic input power. In order to increase the applicability of these results to other cleaning tools, a more generic expression of power, such as power density, is desirable.

To a first approximation, power density can be estimated as input power divided by the area of the transducer (for focused beam megasonics). This is only an approximation since transducer efficiency and coupling losses, which might be significant, are ignored. For the equipment used in these studies, the transducer area was about 77.4 cm^2. Therefore the maximum input power of 300 Watts would correspond to a power density of about 3.88 W/cm^2. The power density at which increased power had little benefit is about 1.9 W/cm^2 (corresponding to an input power of about 150 Watts).

Although chemical ratio is a statistically significant factor for particle removal, the response surface is not very sensitive to relatively small (one decade) changes in the chemical ratio. Excellent cleaning efficiencies were attained with highly dilute chemistries. Indirect evidence of surface roughening was observed for cleans performed in concentrated chemistries, particularly at high power and high temperature. Under these process conditions, LPD counts were often higher after performing a clean than prior to the clean. High LPD counts were also observed on the blank correction wafers. No such observations were noted for dilute chemistries. The conclusion that increased LPD count is a manifestation of surface roughening, under conditions of concentrated chemistry and high temperature, is consistent with the findings of Ohmi (2) and Meuris *et al.* (3). Preliminary work on bath lifetime indicated that a dilute SC-1 chemistry (1:10:130) operated at 45°C has a bath half-life of over 250 minutes. This half-life calculation is based on loss of NH_4OH. The H_2O_2 concentration was observed to be stable at 45°C over the duration of the seven hour test period. Bath cleaning effectiveness remained unchanged during the seven hours. By comparison, the traditional SC-1 chemistry operated at 70°C has a half-life of 16 minutes (4), based on the decomposition of hydrogen peroxide.

Silicon nitride particles were used for the purposes of this study. As noted above, high removal efficiencies were attained for various bath chemistry, temperature, and megasonic powers. The experimental results obtained from the ashed photoresist wafers indicate that particle chemistry is a factor. The importance of particle "type" has been observed in previous studies (5). How this factor affects regions within the experimental space where high removal efficiency has been observed will be examined more closely in future experiments.

CONCLUSIONS

Based on statistically designed experiments, megasonic power has been observed in these experiments to be the dominant factor for silicon nitride particle removal using SC-1 type chemistries. Bath temperature and the ratio of ammonium hydroxide to hydrogen peroxide modify the effect of power on particle removal. Immersion time in the bath was not a significant factor over the experimental range of 6 to 52 minutes. Using dilute chemistries, cleaning efficiencies of greater than 95% were consistently attainable with input megasonic power above 150 W (1.9 W/cm^2, based on perfect transducer efficiency).

The use of substantially diluted chemistries has significant cost saving ramifications for semiconductor manufacturers. The reduced chemical usage also reduces waste water treatment requirements, resulting in an environmentally conscious mode of manufacturing. Additionally, bath lifetimes may be extended by using dilute chemistries at moderate temperature (*e.g.*, 45°C) rather than the traditional high temperature processes.

ACKNOWLEDGMENTS

This research was sponsored by the Contamination Free Manufacturing Research Center at Sandia National Laboratories supported by SEMATECH and the United States Department of Energy.

REFERENCES

1. Menon, V. B. and R. P. Donovan, in Semiconductor Cleaning Technology/1989, J. Ruzyllo and R. E. Novak, Editors, p. 167, PV 90-9, The Electrochemical Society, Inc., Pennington, NJ (1989).

2. Ohmi, T., in IES 1992 Proceedings, p. 287, V 1, Mount Prospect, IL (1992).

3. Meuris, M., M. M. Heyns, P. W. Mertens, S. Verhaverbeke, and A. Philipossian, Microcontamination, May, 31 (1992).

4. van den Meerakker, J. E. A. M., M. H. M. van der Straaten, J. Electrochem. Soc., 137, 1239 (1990)

5. Menon, V. B., L. D. Michaels, R. P. Donovan and D. S. Ensor, Solid State Technology/Contamination Control Supplement, March, S7 (1989).

TABLE I

Tabulated particle removal efficiencies from full-factorial and response surface matrices (some replicates omitted). Chemical Ratio is defined as $NH_4OH:H_2O_2:H_2O$

Run #	Temp (Deg C)	Power (Watts)	Chemical Ratio	%Si_3N_4 Removed 0.10 - 0.30 μm	%Si_3N_4 Removed 0.15 - 0.30 μm
1	65	0	1:1:5	92	90
2	65	300	1:1:5	84	84
3	25	300	1:1:5	97	124
4	25	0	1:1:5	59	55
5	45	150	1:1:12	94	85
6	65	300	1:1:68	92	82
7	65	0	1:1:68	97	104
8	25	0	1:1:68	45	38
9	25	300	1:1:68	96	92
10	45	150	1:10:59	93	89
11	45	0	1:10:130	69	60
12	25	150	1:10:130	101	99
13	45	150	1:10:130	94	90
14	45	150	1:10:130	88	76
15	45	150	1:10:130	98	97
16	65	150	1:10:130	98	94
17	45	300	1:10:130	98	96
18	45	150	1:10:690	88	81
19	65	0	1:100:600	72	55
20	65	300	1:100:600	100	104
21	25	300	1:100:600	97	90
22	25	0	1:100:600	25	21
23	45	150	1:100:1300	105	114
24	65	300	1:100:6900	100	97
25	65	0	1:100:6900	73	71
26	25	300	1:100:6900	93	83
27	25	0	1:100:6900	18	14

TABLE II

Regression coefficients and standard errors

	β_0	β_1	β_2	β_3	β_4	β_5	β_6
Coefficient:	3.06	0.542	1.325	-0.004	-1.143	-0.562	-0.675
Std. Error:	0.29	0.22	0.22	0.22	0.36	0.23	0.23

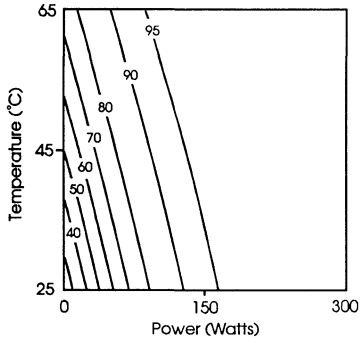


Figure 1. Contour plot of cleaning efficiency as a function of megasonic power and bath temperature with [NH4OH]/[H2O2] = 0.01

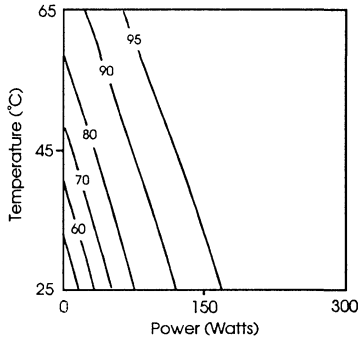


Figure 2. Contour plot of cleaning efficiency as a function of megasonic power and bath temperature with [NH4OH]/[H2O2] = 0.10

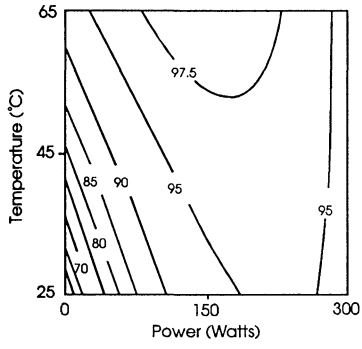


Figure 3. Contour plot of cleaning efficiency as a function of megasonic power and bath temperature with [NH4OH]/[H2O2] = 1.0

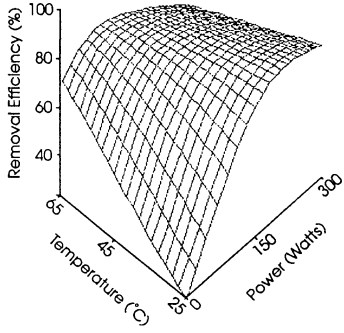


Figure 4. Three-dimensional response surface plot. [NH4OH]/[H2O2] = 0.01

BEHAVIOR OF ULTRA FINE METALLIC PARTICLES (~10nm) ON SILICON WAFER SURFACE

Hitoshi MORINAGA, Takashi FUTATSUKI and Tadahiro OHMI
Department of Electronics, Faculty of Engineering
TOHOKU UNIVERSITY
Aza-Aoba, Aramaki, Aoba-ku, Sendai 980, Japan

Eiji FUCHITA, Masaaki ODA and Chikara HAYASHI
VACUUM METALLURGICAL CO.,LTD.
516 Yokota, Sambu-machi, Sambu-gun
Chiba 289-12, Japan

Ultra fine particles with diameter of several to several hundreds of nanometers were adhered onto the Si surface and the removal efficiency of the ultra fine particles using various cleaning solutions was investigated. It has been found that the conventional cleaning methods are unacceptable for removing Au ultra fine particles with diameter of less than several tens of nanometers. In addition, it has also been found that particle removal by chemical etching, such as DHF-H_2O_2, causes increased surface roughness due to local chemical reactions.

INTRODUCTION

With continued advances in ULSI fabrication technology, the preparation of Ultra Clean Wafer Surfaces is essential. An Ultra Clean Wafer Surface is characterized as a surface which is 1) Particle free, 2) Organic-contamination free, 3) Metallic-contamination free, 4) Native-oxide free, 5) Completely hydrogen-terminated, and 6) Surface microroughness free (1).

In particular, realization of a particle free wafer surface is one of the most important items, because particles will definitely contribute to the pattern defects, which automatically deteriorate the ULSI yield. Therefore, particles are the biggest obstacle to realize the high performance process which achieves the 100% yield. In general, it is considered that the diameter of particles which adversely affect the yield is larger than one tenth of the ULSI pattern size. Therefore, as the pattern size has already been smaller than 1μm in fabrication, ultra fine particles with diameter of 0.1μm or less have recently become important. At the beginning of the 21st century, we wish to make ULSI with 0.1μm pattern size. And then, the particles in the range of 10nm will become critically important. And ultra fine particles of this type are expected to be difficult to remove. Despite this serious concern, however, the study of ultra fine particles on Si wafer surface has not been carried out very much due to the difficulty of detecting and handling technique of the ultra fine particles.

In this study, we have adhered ultra fine metallic particles onto the Si wafer surface, and the removal efficiency of the ultra fine particles using various cleaning solutions was investigated. And then, we also studied surface microroughness caused by the particles.

EXPERIMENTAL

Required Technologies for Studying Ultra Fine Particles on Si Wafer Surface

Two technologies are required to study ultra fine particle removal:
1) the technology to detect ultra fine particles on the Si wafer surface and
2) the technology to get ultra fine particles to adhere onto the Si surface in large numbers without having them cluster together.

Ultra fine particles with diameter of 0.1μm or less can not be detected on the Si surface with a laser light-scattering particle counter which has a detection limit larger than 0.1μm. At present, Scanning Electron Microscopy (SEM) is the only effective method for detecting such particles. In order to detect ultra fine particles of 0.1μm or less with SEM, however, it is necessary to magnify the Si surface by 10,000 to 100,000 times. In this case, the observation area is only 1 to 100μm^2 in size. Due to the very small observation area, it is extremely difficult to locate an ultra fine particle. This problem has constituted one of the major obstacles studying ultra fine particle removal. The challenges for this study, then, were to establish a technology which can generate particles of a uniform size and then to get these particles to adhere homogeneously to the Si surface in sufficient numbers so that there are several per 1-100μm^2 yet without clustering. The authors employed a gas deposition method to get the ultra fine particles to meet these challenges.

Sample Preparation by Gas Deposition Method

In the gas deposition method, particles generated by gas phase condensation are adhered onto the substrates (2). Figure 1 shows the schematic diagram of the apparatus for the gas deposition method. Generally, in the gas phase condensation method, metal atoms evaporated from an evaporation source collide with gas atoms and during cooling down they condense to form a fine particle. Further growth of the particle takes place with the coalescence of the particles. This method is generally used to make ultra fine particles. But we still have some problems here. In the regions further from the evaporation source, particles will cluster together. If particles are clustered together, they will work as large size particles even though the individual particles are very small. Therefore, we provide two chambers, one is for vaporizing, and the other one is to deposit the particles to the substrates. And we provide a different pressure by using He gas and vacuum pumps. Because of the pressure difference, the appropriate size of particles without clustering, will be brought to surface through the transfer pipe.

The ultra fine particles generated by this method feature the following unique

characteristics: 1) Almost all kind of metal elements can be used to make ultra fine particles. 2) Ceramic particles can be generated by using reactive gases. 3) Particle size can be easily controlled (about 1nm ~ 1μm) by varying the parameters of metal temperature and gas pressure. Particle size distribution is sharp. 4) Individual particles do not cluster together (In other words, isolated particles can be generated.). 5) Ultra fine particles are of high purity level because they are generated through condensation in a high-purity inert gas.

Figure 2 shows the SEM images of prepared sample wafers. For the comparison, these images have the same magnification. But, in actual observation, appropriate magnifications are used. As can be seen, the particles with diameter of 150nm to 4nm are obtained. In conventional studies, 150nm is small enough, but for us it's still large. And, Atomic size of Gold is about 0.3nm. Therefore, 4nm is almost close to the size of the atoms.

The authors selected Au particles to adhere on the Si surface for the following three reasons. Firstly, the metallic particles are not very well studied. Secondary, it is one of the metals which have higher electronegativity than Si. It is well-known that this type of metals are adsorbed onto the Si surface and severely deteriorate device performance. It is interesting, therefore, to examine its behavior. Thirdly, Au is stable in the chemicals. Therefore, it is favorable for the study of the particle removal in the various chemical solutions.

The sample Si wafers were Cz (100) oriented N-type.

Cleaning Methods Examined

The cleaning sequence in this study was carried out as follows.

(1) Ultrapure water rinsing (10min at room temperature)
↓
(2) Diluted HF (DHF) cleaning (1min at room temperature)
(HF: 0.5%)
↓
(3) APM cleaning (10min at 80-90°C)
(NH_4OH : H_2O_2 : H_2O = 1:1:5)

APM (NH_4OH - H_2O_2 - H_2O) cleaning (SC-1 cleaning) is the conventional cleaning method for particle removal proposed by W.Kern and D.A.Puotinen (3).

(1) Ultrapure water rinsing (10min at room temperature)
↓
(2) DHF-H_2O_2 cleaning (1 or 5min at room temperature)
(HF: 0.5%, H_2O_2: 3%)

DHF-H_2O_2 cleaning is the cleaning method for metal removal proposed by

T.Shimono et al (4). All cleanings were followed by rinsing with ultrapure water (UPW) for 10min and drying by nitrogen gas blowing. The results of each cleaning were observed by SEM.

RESULTS AND DISCUSSION

Removal Efficiency of Ultra Fine Metallic Particles

Figure 3 shows the SEM images of the sample wafer with 150nm Au fine particles after various cleanings. Particles can not be removed by UPW rinsing and DHF cleaning. However, APM cleaning can remove the particles. This tendency coincides with the result of the conventional study. And, as can be seen from Figure 4, if the radius of the particles becomes smaller, in the range of 10nm, it's very difficult to remove them. With UPW cleaning and DHF cleaning, no obvious difference was observed from the initial state. In the case of APM cleaning, the number of the particles decrease, but particles are becoming larger in size. Further, Figure 5 shows the result for 4nm particles which is close to the size of the atoms. Also, in this case, the number of the particles decreases after APM cleaning, but particles are becoming larger in size. Figure 6 indicates the result of previous studies. For any size of the particles, after UPW cleaning and DHF cleaning, almost no particles are removed. But, after APM cleaning, the number decreases for any size. When we consider the numbers of particles, it looks like decreasing. But, particles have become larger. To consider this effect, therefore, we used the total volume of particles on the vertical axis. In the case of APM cleaning, the total volume of 150nm particles decreases. But the total volume of 13nm and 4nm particles shows no major change, so they are not removed.

This is believed to be because Au ultra fine particles move on the Si surface and cluster together, growing in size while combining atoms. Horizontal movement can be described by Brownian movement caused by the collision with liquid molecules. From the Einstein equation, displacement $\bar{x}$ after t seconds is given by:

$$\bar{x} = \sqrt{\frac{k\,T\,t}{3\,\pi\,\mu\,a}} \qquad [1]$$

where k = Boltzmann constant, T = absolute temperature, μ = coefficient of viscosity, and r = radius of particle (5). In the case of 10 nm particles, the displacement after 1 second is calculated as 6μm (in 20°C water). They move in a horizontal manner, but particles also wish to move vertically. However, the Van der Waals force restricts the vertical movement. Therefore, Brownian movement results only in a horizontal motion, so they can not move in a vertical manner. For reasons mentioned above, we believe that small particles were not removed in this study.

Surface Microroughness Caused by Particles

In wet cleaning processes, cleaning solutions which have dissolving effect are

generally used. Contaminants and Si surface are generally dissolved by the cleaning solutions. Contaminants like organic materials decompose in the strong oxidizing agent such as SPM (H_2SO_4 – H_2O_2) and ozonized ultrapure water. In this case, Si surface is also oxidized but Si is not dissolved. However, Si surface is etched by the solutions such as DHF–H_2O_2, APM and DHF. We must be careful using this type of chemicals. When the surface is masked with particles, the surface will be etched irregularly due to the different etching rate between the area masked with particles and the clean surface. It will cause surface microroughness.

This time, we have investigated such particle induced microroughness by using the DHF–H_2O_2 cleaning. Figure 7 shows the SEM images of a Si wafer with Au ultra fine particles after DHF–H_2O_2 cleaning. Many small holes were observed on the Si surface. On the other hand, in the case of a Si wafer without particles, no obvious differences was observed between the initial state and after DHF–H_2O_2 cleaning (Figure 8).

A possible mechanism for the roughening is shown in Figure 9. In DHF–H_2O_2 solution, the etching rate of SiO_2 by HF is always larger than the Si oxidation rate by H_2O_2. Therefore, the Si surface is always exposed to the solution. And then, when there are metallic particles like Au which features higher electronegativity than Si, Au will attract electrons from Si to facilitate Si oxidation. Therefore local excess oxidation occurs. Since the oxidation area is etched by HF rapidly, irregular etching will occur. Therefore, the surface is damaged.

CONCLUSION

This study has established a method to evaluate ultra fine particle removal efficiency using the gas deposition method. It has been found that the conventional cleaning methods are unacceptable for removing Au ultra fine particles with diameter of less than several tens of nanometers. In addition, it has also been found that the Si surface gets rougher when the DHF–H_2O_2 cleaning is performed to remove Au ultra fine particles. This is believed to be because Au, which features higher electronegativity than Si, attracts electrons from Si facilitating Si oxidation.

In conclusion, we would like to propose that, for ultra fine particle removal, a new cleaning method is urgently required. Moreover, we should notice that when there are particles on the Si surface, cleaning by chemical etching causes surface roughness increase due to local chemical reactions.

ACKNOWLEDGEMENT

This research has been carried out in the laboratory of Vacuum Metallurgical Co.,Ltd., in Mini Super Clean Room at the Faculty of Engineering and in Laboratory for Microelectronics attached to The Electric Communication Laboratory in Tohoku University.

REFERENCES

1. T.Ohmi, BREAK THROUGH FOR SCIENTIFIC SEMICONDUCTOR MANUFACTURING IN 2001, p.36, Realize INC, Japan (1992).
2. M.Oda and N.Saegusa, "Formation of Mono-Dispersed Fe_3O_4 Fine Particles", Jpn. J. Appl. Phys., Vol.24, No.9, 702 (1985).
3. W.Kern and D.A.Puotinen, "Cleaning Solution Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology", RCA Rev., Vol.31, 187, (1970).
4. T.Shimono and M.Tsuji, "A New Cleaning Solution for Metallic Impurities on the Silicon Wafer Surface", IEICE Trans. on Electron., Vol.E75-C, No.7, 812 (1992).
5. F.Yonezawa, Brownian Movement, p.59, Kyoritu Press, Japan (1986)

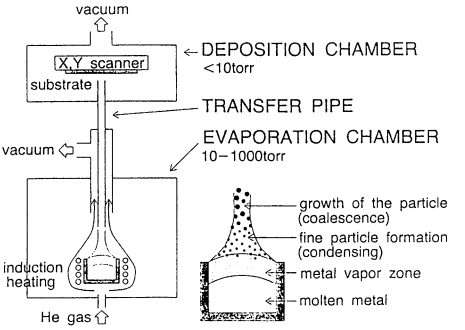


Figure 1. Schematic diagram of the sample preparation apparatus (Gas Deposition Method).

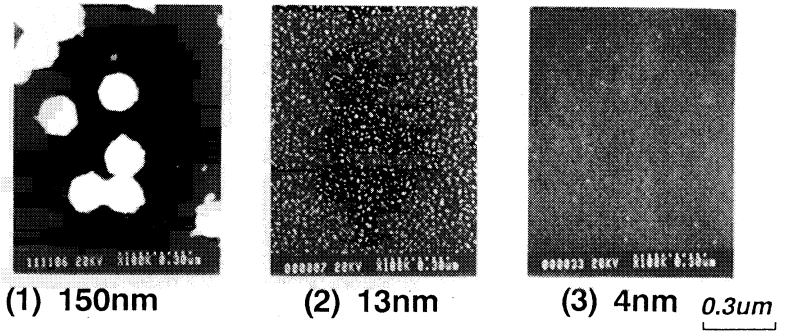


Figure 2. SEM images of prepared sample wafers. Au ultra fine particles with diameter of 150nm to 4nm on the Si wafer are obtained by Gas Deposition Method.

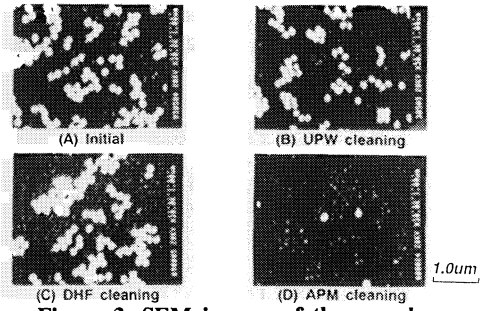


Figure 3. SEM images of the sample wafer with Au fine particles (150nm) after various cleanings.

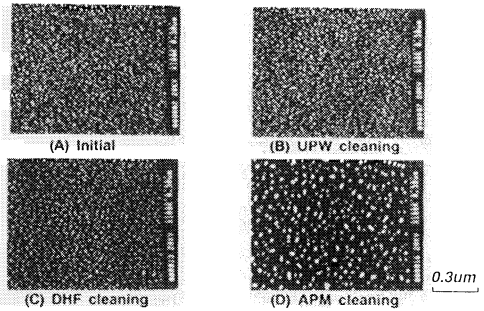


Figure 4. SEM images of the sample wafer with Au ultra fine particles (13nm) after various cleanings. (note increase in particle size)

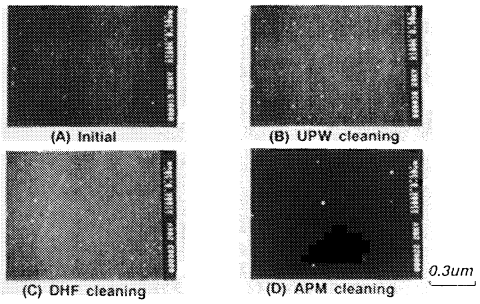


Figure 5. SEM images of the sample wafer with Au ultra fine particles (4nm) after various cleanings.

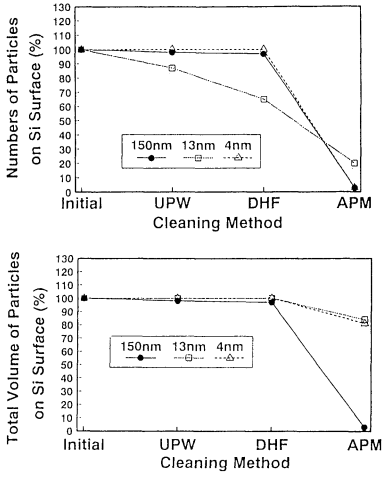


Figure 6. The removal efficiency of the Au ultra fine particles using various cleaning solutions.

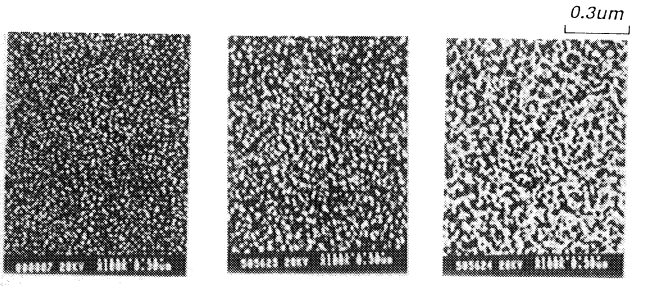


Figure 7. SEM images of the sample wafer with Au ultra fine particles after DHF-H_2O_2 cleaning. The Si surface got rougher.

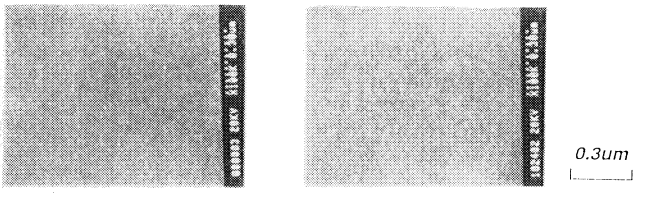


Figure 8. SEM images of the sample wafer with Au ultra fine particles after DHF-H_2O_2 cleaning. No obvious differences was observed.

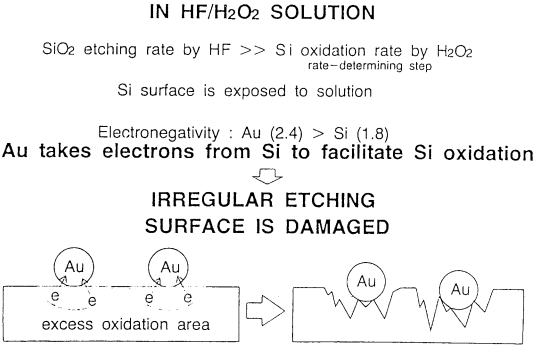


Figure 9. Mechanism of surface microroughness caused by Au particles with DHF-H_2O_2 cleaning.

Separate detection of particles and bubbles in liquid

Kazuo Takeda, Yoshitoshi Itoh, and Atsushi Hiraiwa
Central Research Laboratory, Hitachi, Ltd.
Kokubunji, Tokyo 185, JAPAN

Kenji Yasuda
Advanced Research Laboratory, Hitachi, Ltd.
Hatoyama, Saitama 350-03, JAPAN

Kyo Suda
Hitachi Electric Engineering, Co. Ltd.
Kanda, Tokyo 100, JAPAN

A new liquid-phase particle counting technology is developed for monitoring deionized water used in the deep submicron LSI process. This technology can separately detects particles from bubbles in the liquid, and has a sensitivity of detecting 38 nm particles. It is based on electrophoresis and light scattering, and is proven effective through experiments using ultrasonically generated bubbles.

INTRODUCTION

As devices have become smaller, cleaning technologies have become a key issue in LSI (large scale integrated circuit) fabrication. Effective cleaning is essential for maintaining high yield and reliability. Dust particles in deionized water and cleaning solution must be monitored to keep and improve clean fabrication processes. Various liquid-phase particle counters have been developed for this purpose and are widely used. However, they are not necessarily effective in practical use because they detect bubbles generated in the particle filtration system as dust particles.

Two approaches[1,2] have been reported for detecting particles and distinguish them from bubbles through optical measurement of their refractive indices. One[2] is based on the Mie theory[3,4], and is not applicable to the Rayleigh scattering region (particle diameter, $D_p < 0.2$ μm). The other[1] is based on the phase shifts of scattered light. The measurement difficulties in the Mie scattering region occur because the phase of the light scattered from a particle is a cyclic function of the particle size and refractive index. Furthermore, the signs of phase shifts change at a specific particle size, which depends on the particle material.

The purpose of this work was to develop a technology for measuring a wide range particles (D_p: from < 0.05 μm to > 10 μm) and distinguishing them from bubbles. For this purpose, the electrochemical separation of particles and bubbles were measured with a laser ultramicroscopic particle counting system.

PRINCIPLE OF SEPARATE DETECTION OF PARTICLES AND BUBBLES

Particles are accompanied by an adhesive layer that surrounds them in liquid. Their motion is governed by the electrostatic potential at the interface between the adhesive layer and the liquid. The potential is called the ζ-potential, and depends on the particle material and the liquid. In contrast, bubbles are not accompanied such a layer and are electrically neutral. Therefore, we can separate particles from bubbles by using the electrophoresis phenomenon. The velocity U_e of the electrophoresis is described as a function of the ζ-potential in the following way.

$$U_e = \varepsilon \zeta E / (4\pi \eta) \equiv \alpha E, \qquad (1)$$

where ζ is the ζ-potential, ε is the dielectric constant of liquid, η is the viscosity of liquid, and E is the electric field intensity. The electric field directs the migration of particles in the flowing liquid. Thus, we can distinguish particles from bubbles by detecting change in the flow direction. It is noted that Eq. (1) is almost independent of particle size and shape[5]. This result is of practical importance, because it allows particles to be separated from bubbles independent of their size and shape.

MEASUREMENT SYSTEM

Figures 1 (a) and (b) show the measurement system. A flow cell made of quartz is irradiated by a laser light (He-Ne laser, power: 10 mW, wavelength: 633 nm) focused by a cardioid condenser (Olympus, DCW). The irradiated region in the cell extends almost parallel to the flow direction. Particles in the liquid are counted by detecting the light that is scattered when the particles pass through the irradiated region (Fig. 1(a)). The smallest polystyrene particles detected were 38 nm. The flow cell has a pair of electrodes (Pt) 1 mm apart at its side walls. An electric field E (0～3 kV/mm) is formed between the electrodes to direct the motion of the flowing particles (Fig. 1(b)).

Directional change increases the particle counting rate (counts /s). On the other hand, the motion of bubbles is not influenced by the electric field and their counting rate remains constant. Figure 2 shows the detection cross-section for particles under the electric field.

The particle concentration N_p and the bubble concentration N_b can be calculated from the increase in the counting rates as follows.

$$N_p = \kappa\,(C(E) - C(0))\,, \tag{2}$$

$$N_b = C(0)/(UWd) - N_p\,, \tag{3}$$

where $\kappa = 1/(\alpha\, EWL)$,

$C(E)$: the average counting rate under the electric field E,

$C(0)$: the average counting rate under no field,

U : the flow velocity,

W :the width of the detection volume,

d : the thickness of the detection volume, and

L : the length of detection volume.

RESULTS & DISCUSSIONS

Figures 3 shows the counting rate of polystyrene particles added to sample water where the electric field is repeatedly applied. As expected, the counting rate was increased by application of the electric field. The detection cross-section of particles was $Wd + \alpha\, EWL/U$ ($\propto C(E)$) and that of bubbles was Wd ($\propto C(0)$) as shown in Fig. 1 (a) and Fig. 2. Accordingly, $C(E)/C(0)$ is a linear function of the electric field intensity. This is experimentally confirmed by Fig. 4.

The bubbles were generated for a limited period and in a controlled manner, by an ultrasonic cell that was placed at the upper stream and driven by a voltage of 50 V (frequency: 1.08 MHz). To check the generation of bubbles, we measured the particle size distribution of sample water with and without ultrasonication (Fig. 5). It is clearly seen that the bubbles larger than 2 μm (D_p) were generated by ultrasonication. The life time of a bubble is proportional to D_p^3, and of the order of 1 second[6]. It is longer than the time interval (~ 0.1 sec) between generation and detection in this experiment.

Figures 6 (a) and (b) show an example of the separate detection of particles and bubbles using this technology. The sample water contains not only polystyrene particles (D_p: 0.8 μm, concentration: 3.5×10^4 ml^{-1}), but also bubbles. The increase of counting rates induced by ultrasonication reflects the generation of bubbles (Fig. 6 (a)). The concentrations of polystyrene particles and bubbles were calculated using Eqs. (2) and (3). Figure 6 (b) clearly shows that this system measured the concentration of only the polystyrene particles, independent of whether or not bubbles were present. The value of the concentration is also consistent with the sample preparation condition.

CONCLUSION

A liquid-phase particle counting technology was developed for detecting and distinguishing them from bubbles based on electrophoresis and light scattering. The validity of this method was proven through experiments with ultrasonically generated bubbles.

ACKNOWLEDGMENTS

The authors thank Mr. Ishi, Dr. Koizumi, and Mr. Yatsugake of Hitachi Electric Engineering, Co. Ltd., and Dr. Umemura of Hitachi Advanced Research Laboratory for helpful discussions.

REFERENCES

1. M.A. Taubenblatt and J.S. Batchelder, Appl. Opt. **30** 4972 (1991)
2. K. Takeda, I. Yoshitoshi, and C. Munakata, Meas. Sci. Tech. **3** 27 (1992)
3. G. Mie, Ann. Phys., **25** 377 (1908)
4. C.F. Bohren and D.R. Huffman: *Absorption and Scattering of Light by Small Particles,* Wiley, New York (1983)
5. S. Ikeda: *Colloid Chemistry,* p. 120, Shokabo, Tokyo (1986)
6. J. Saneyoshi, Bull. of T.I.T., Series B, No. 6 27 (1953)

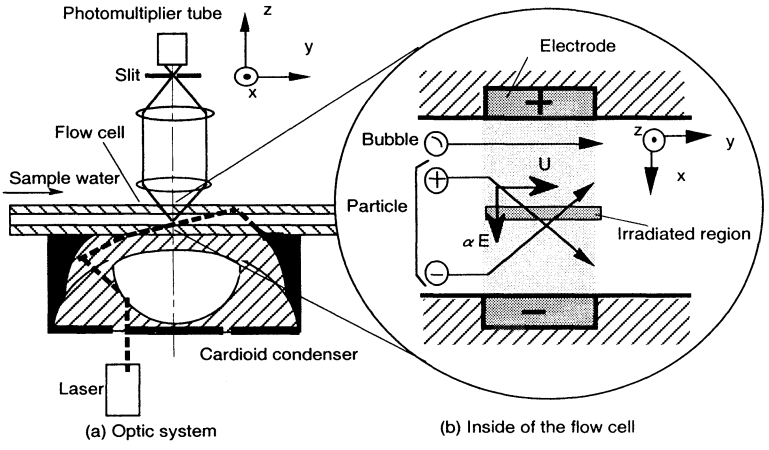


Fig. 1 Measurement system

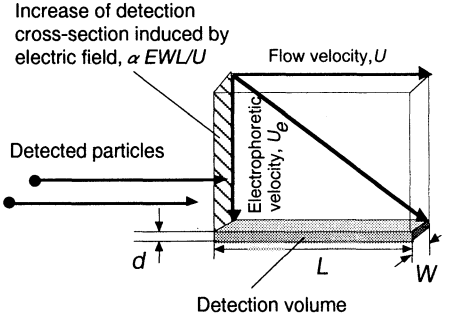


Fig. 2 Detection cross-section under the electric field

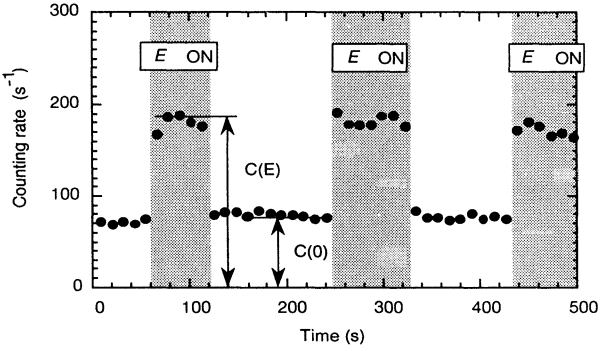


Fig. 3 Counting rate enhanced by the electric field
Sample: polystyrene particles (D_p=0.3 μm),
E:3000V/mm,
U:0.13 m/s,
C(E): the average of counting rate under the electric field *E*,
C(0): the average of counting rate under no field.

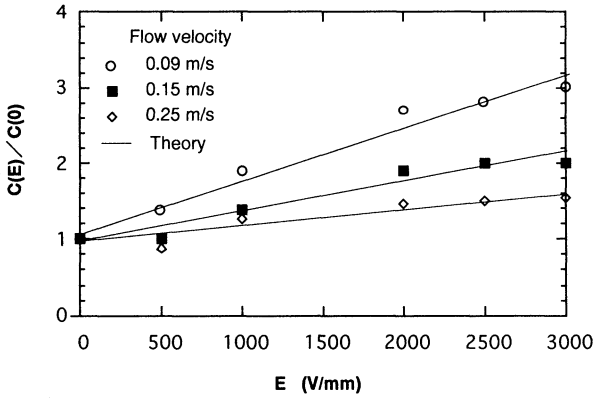


Fig. 4 Counting rates as a function of the electric field
Sample: polystyrene particles (D_p=0.3 μm).
Theoretical curve : $C(E)/C(0) = 1+(L/d)\,\alpha\, E/U$,
where, L/d = 3.2, α =1.8x10^{-8} m^2/(Vs).

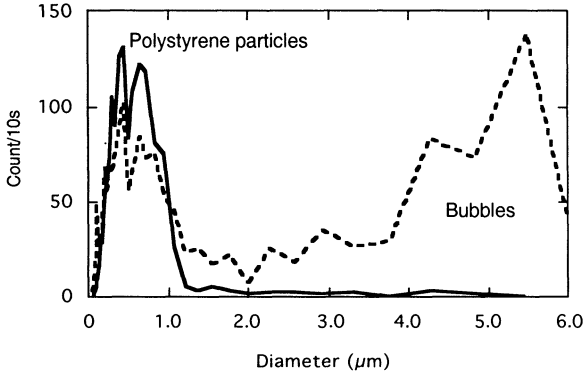


Fig. 5 Distribution of polystyrene particles and bubbles generated by ultrasonication.

Sample: polystyrene particles (D_p=0.8 μm)

—— : under no ultrasonication,

■ ■ ■ : under ultrasonication.

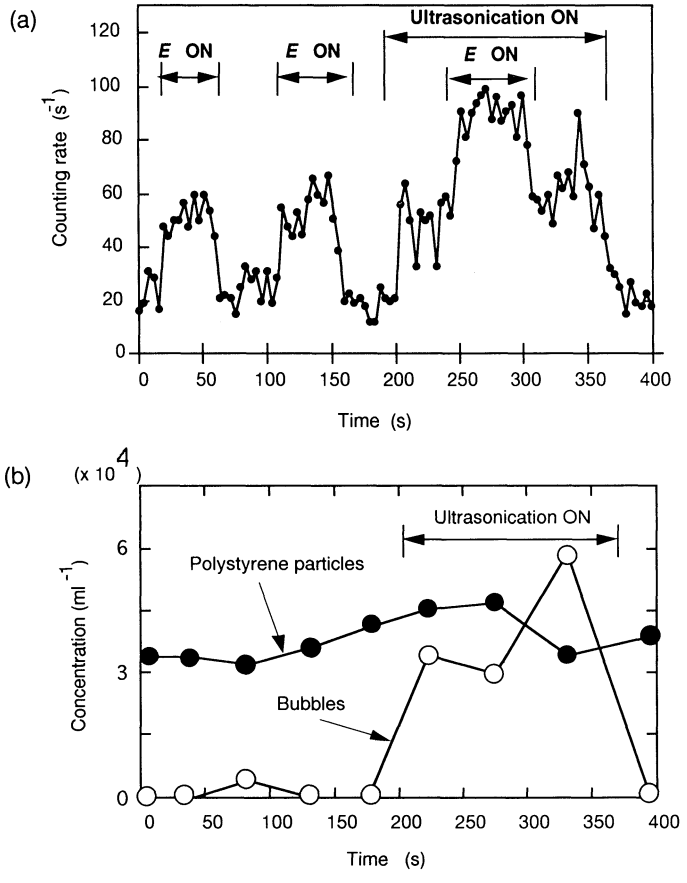


Fig. 6 Separate measurement of polystyrene particles and bubbles

Sample: polystyrene particles (D_p=0.8 μm)

(a) Counting rates

(b) Concentration change calculated from data of (a) using Eqs. (2) and (3).

THE EFFECTS OF INCREASED CHEMICAL TEMPERATURES IN A CENTRIFUGAL SPRAY PROCESSOR

Kurt Christenson

FSI International
322 Lake Hazeltine Drive
Chaska, MN 55318 USA

ABSTRACT

Considerable effort has been expended to optimize the bath temperature and blend of the APM chemistry (Ammonia Peroxide Mix - $NH_4OH:H_2O_2:H_2O$) to maximize particle removal and minimize surface roughness in an immersion process (1,2,3). But little work has been done to optimize these parameters in a spray processor which employs shorter chemical exposure times and lower process temperatures. This study reports the results of raising the APM chemistry temperature and changing the APM blend ratio on the particle addition and removal performance of an acid processor. Higher chemistry temperatures increased the particle removal efficiency and, with reduced NH_4OH and H_2O_2 concentrations, did not lead to an increase in particle addition. Also described is an in-line chemical heater that was used in the experiment.

INTRODUCTION

In 1970 Kern first published the now standard "RCA clean" which consists of basic and acidic peroxide solutions (4). Recently, considerable effort has been expended to optimize the bath temperature and blend ratio of the APM chemistry (Ammonia Peroxide Mix - $NH_4OH:H_2O_2:H_2O$) to maximize particle removal and minimize surface roughening (1,2,3). All of this work has concentrated on immersion processing with bath temperatures generally ranging between 70 and 90°C and immersion times of approximately 10 minutes. With the exception of Pirooz et al. and Sugihara et al., this work only investigated variations in the solution temperature and NH_4OH concentration (5,6) This paper reports an initial study of the particle performance of RCA cleans in an acid processor as a function of on-wafer temperature, the NH_4OH concentration and the H_2O_2 concentration.

The experiment was conducted in an FSI MERCURY® OC spray processor. In the MERCURY OC, a carrier of wafers is mounted on the axis a turn table that can rotate from 0 to 750 rpm. Chemicals and rinse water are dispensed in a nitrogen atomized stream from separate spray posts mounted in the side of the chamber. At low rotational speeds, the fluids are evenly distributed and form "puddles" on the wafers. The centrifugal force present at high speeds is used to throw off spent chemicals or rinse water and to aid in drying. The chemical delivery system begins with pneumatic valves which feed DI water and chemicals into a mixing manifold and are proportionally driven by the system controller utilizing feedback from flow pickups in each chemical line. After blending in the manifold, the chemistry travels to the chemical spray post and is atomized onto the wafers with nitrogen.

It is difficult to achieve on-wafer temperatures in the 70 to 90°C range with this system. First, there are many components which cause transient cooling effects, wetted components which absorb heat when changing from cold to hot solutions. These include the valves, tubing, chamber, turntable, cassette and the wafers themselves. Second, after the temperature of these components has equilibrated, there are still continuous heat losses that limit the steady state temperature. The DI water base of an APM solution begins at 95°C in the water heater but then cools through convection as it flows to the MERCURY chemical mixing manifold and from the manifold to the spray post. In the manifold, the hot DI is mixed with cold NH_4OH and H_2O_2 causing a further drop in fluid temperature. In the chamber there is further cooling due to evaporation and convection. Maximum on-wafer temperatures for the RCA chemistries is near 50°C with a 95°C water heater set point.

In order to increase the on-wafer temperature, an in-line chemical heater was added between the mixing manifold and the spray post. The heater consisted of a spiral of 3/8" PFA tubing surrounding three, 2 kW infra-red lamps. Aqueous based fluids efficiently absorb the IR radiation whereas the PFA is largely transparent at the wavelengths of interest. When operating at full theoretical power, the heater can produce a 45°C temperature rise with a flow rate of 2,000 cc/min. Reheating the chemistry near the spray post can overcome many of the mechanisms which cause temperature loss in the standard system. Increasing the flow rate of the cleaning chemistry can also reduce the effects of the cooling mechanisms but would increase chemical consumption. Therefor, increased flows with more dilute blends were also investigated.

EXPERIMENT

On-wafer temperature measurements were made with a RTD attached to the back of a test wafer with an epoxy adhesive. The RTD signal was recorded by a HOBO-TEMP miniature data logger which was fixtured within the wafer cassette. Temperature curves for flows of DI water were taken under three conditions:

1. 1650 cc/min flow, in-line chemical heater inactive
2. 2400 cc/min flow, in-line heater inactive
3. 2400 cc/min flow, in-line heater operating with a set point of 95°C

For particle experiments, prime, 150 mm, P (100) wafers were first precleaned in an FSI MERCURY® MP to remove any contamination from shipping. Particle addition experiments consisted of two runs of 25 of these wafers in the MERCURY OC for each of three treatment conditions listed below. Challenge wafers for particle removal were prepared by dipping precleaned wafers in a bath of 10:1 HF for one minute followed by rinsing and drying in a PHOENIX® Spin Rinse Drier. Particle removal experiments consisted of two runs of 25 challenge wafers each for each of three treatment conditions listed below. All particle measurements were made with an ESTEK™ 8500 Wafer Inspection System calibrated with NIST traceable latex spheres.

Particle test wafers were processed in the MERCURY OC using the B clean cleaning sequence:

4:1 H_2SO_4:H_2O_2, 60 seconds
Hot rinse, cold rinse
100:1 HF, 90 seconds
Cold rinse
NH_4OH:H_2O_2:H_2O, 180 seconds, blend ratio varied by treatment
HCl:H_2O_2:H_2O, 90 seconds, blend ratio varied by treatment
Hot final rinse and spin dry

The APM and HPM blend ratios for the three particle performance treatments were as follows:

1. Standard dispense, 1650 cc/min, 0.6:1:5 APM blend and 1400 cc/min, 1:1:5 HPM blend
2. High flow dispense, 2400 cc/min, 0.6:1:5 APM blend, 2400 cc/min, 1:1:5 HPM blend, both with 95° C in-line chemical heater set point
3. 2400 cc/min dispenses with heater active and blend ratios reduced to 0.25:0.25:5 for both APM and HPM

RESULTS AND DISCUSSION

Figures 1a, 1b and 1c show the on-wafer temperature data for DI water flowing at the total flow rate of the standard APM dispense conditions (1650 cc/min), the high-flow dispense conditions (2400 cc/min) and the high-flow dispense conditions utilizing the in-line heater respectively. Increasing the total flow rate from 1650 cc/min to 2400 cc/min increased the peak APM temperature from 50° to 56°C. Equally important, it shortened the time constant of the transient effects. The time to reach 1/2 of the maximum temperature rise dropped from 42 to 30 seconds and the average temperature during the cycle rose by approximately 8°C. Further increasing the flows to 3 to 4 l / min would further reduce the time constants of the transient effects and increase the steady state temperatures.

Combining the in-line chemical heater with the high flows further raised the peak temperature by 10° to 66°C and raised the average temperature by 6°C. The transient response during the initial temperature rise was not improved with the activation of the heater. The temperature curves of the high flow with heater matched those of the high flow without heater for the first 30 seconds.

The hot rinse preceding the HPM cycle preheated the wafers and complicated the HPM temperature data. Instead of asymptotically heating toward the steady state temperature from ambient, the wafers are cooling toward steady state. Further, the flow rates of the hot rinse exceeded the capacity of the DI water heater and reduced its output temperature. This resulted in reduced temperatures for the HPM chemistry being dispensed during most of the HPM cycle. The rise in the on-wafer temperature at the end of the high flow HPM cycle probably reflects the recovery of the DI water temperature toward 95°C. Activation of the in-line chemical heater reduced the effect of the dip in DI heater temperatures and provided an 11°C increase in the average on-wafer temperatures in the HPM cycle.

The wafer temperature never equilibrated during any of the four minute dispenses. Therefor, it is impossible to determine quantitatively the increase in steady state temperatures from either the increase in flow rate or the chemical heater. Likewise, because the system has multiple time constants whose dominance varies through the dispense, a quantitative improvement in transient response is difficult to define. Tests to allow the construction of an analytic model which predicts the temperature response of the system are planned for the future.

However, the pragmatic goal of increasing the on-wafer chemistry temperature was clearly reached. Increasing the flow rate during the APM dispense shortened the duration of some transient effects which allowed the system temperature to rise more quickly.

Higher flows also yielded higher maximum temperatures through dominance over steady state cooling effects. Combining the in-line chemical heater with high flows did not further reduce the duration of transient effects during APM but did significantly increase the peak and average temperatures of both the APM and HPM chemistries.

Figures 2a, 2b and 2c respectively show data on particle addition to initially clean wafers for three treatments:

1. Standard dispense, 1650 cc/min, 0.6:1:5 APM blend and 1400 cc/min, 1:1:5 HPM blend
2. High flow dispense, 2400 cc/min, 0.6:1:5 APM blend, 2400 cc/min, 1:1:5 HPM blend, both with 95°C in-line chemical heater set point
3. 2400 cc/min dispenses with heater but with blend ratios reduced to 0.25:0.25:5 for both APM and HPM

There was no statistical difference at the 95% confidence level between treatments 1 and 3; both were approximately particle neutral, they neither added nor removed particles from initially clean wafers, for particles larger than 0.15μm. Treatment 2, however, showed a significant degradation, adding over 20 particles per wafer on average. The source of these particles has not been determined at this time. One possibility is that the increased temperatures allowed some contaminated liquids to dry in place rather than flow down the drain. A second possibility is that the increased aggressiveness of the APM chemistry with temperature lead to roughening or pitting of the surface. Further work is necessary in this area.

Figures 3a, 3b and 3c show the particle removal performance of the above three treatments for "HF Last" particles. The improvement from 92% to 95% removal between treatments 1 and 2 is to be expected based on the increase in the on-wafer temperature. The improvement from 95% to 98% between treatments 2 and 3 is more difficult to explain. While the total flow rates and in-line heater set points for the treatments were identical, it is possible that treatment 3 was on average hotter than treatment 2. Treatment 2 had larger volumes of cold H_2O_2 and NH_4OH mixed in with the stream of hot DI water yielding a lower temperature mixture. While the mixture did reach 95°C during the dispense, there may have been a difference in the transient heating characteristics which were not monitored during the cleaning runs.

Assuming that the particle removal activity is dominated by the APM chemistry, a more likely explanation lies in a change in the chemical activity of the APM associated with the reduced H_2O_2 and NH_4OH concentrations. Possible differences in the two treatments include a change in the silicon etch rate, a change in the solution pH, a change in the thickness of the electrostatic double layer and a change in the Zeta potential of the silicon and contaminant particle surfaces.

Sugihara et al. have investigated the variation of silicon etch rate with APM blend ratio (5). Their figure 1 shows an area of "excessive etching rate" for low H_2O_2 concentrations and an area of "low etching rate" for low NH_4OH concentrations. While no etch rate was measured for a 0.25:0.25:5 ratio which lies between the regions of "low" and "excessive" etching rate, 0.25:0.25:5 does lie midway between two ratios which were measured as being 7.5 and 17 A/min. Therefor, it is likely that the etch rate for 0.25:0.25:5 is near the rate for 0.5:1:5 which Sugihara et al. reported as 11 A/min.

Itano et al. have investigated the pH of APM solutions for blend ratios of x:1:5 and x:0:5, but not for intermediate H_2O_2 concentrations (7) The decrease in NH_4OH concentration from 1:1:5 to 0.25:1:5 is reported to give a decrease in solution pH from approximately 9.9 to 9.5 at 80°C. However, a decrease in H_2O_2 concentration from 0.25:1:5 to 0.25:0:5 is reported to increase the pH from approximately 9.5 to 10.5. It would appear from Itano's data that the net effect of changing from 1:1:5 to 0.25:0.25:5 will be a slight rise in pH from its initial value of 9.9.

Reducing the NH_4OH concentration does lead to an increase in the range of the electrostatic double layer repulsion forces which inhibit the particle from approaching the surface and re depositing (8). The range of this interaction is proportional to the inverse square root of the ionic strength of the solution (9) In the absence of a change in H_2O_2 concentration, a 2x decrease in NH_4OH concentration would yield a 1.4x increase in the thickness of the double layers. This increase in thickness would reduce the rate of re deposition from the fluid and hence improve the net particle removal efficiency. The effect of the simultaneous change in the H_2O_2 concentration has yet to be determined.

Both the particle deposition from dilute city water and the Zeta potential of Fe_2O_3 particles show a broad minimum in solutions with a pH between 8 and 11 (7,10). Therefor, the small shift in pH expected in this experiment should not account for the variations in net particle removal that were observed. Because none of the mechanisms discussed above clearly accounts for the observed improvement in net particle removal, further experimentation will be necessary to understand the substantial improvement in net particle removal that was observed in this experiment.

CONCLUSION

The on-wafer temperatures of RCA chemistries in spray processors can be increased significantly by utilizing higher chemistry flow rates and can be further increased by the use of an in-line chemical heater. Where possible, a hot rinse to preheat the wafers before dispensing the cleaning chemistry greatly increases the average on-wafer temperature for

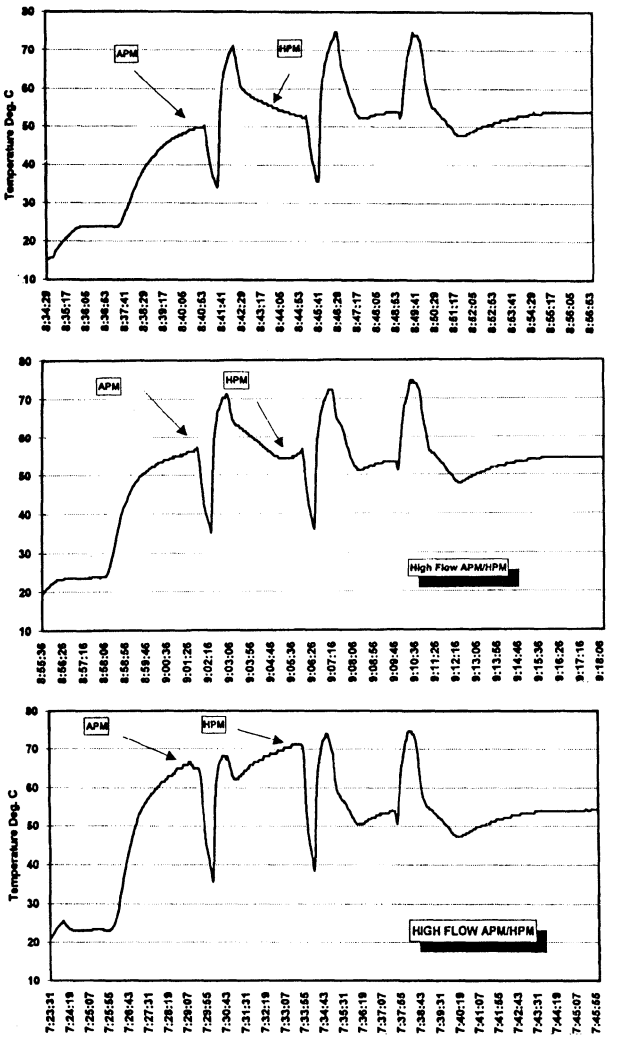
short dispenses. While increased on-wafer temperatures can result in greater particle removal efficiency, it is necessary to modify the blend ratios that are optimal at lower temperatures to prevent particle deposition.

ACKNOWLEDGMENTS

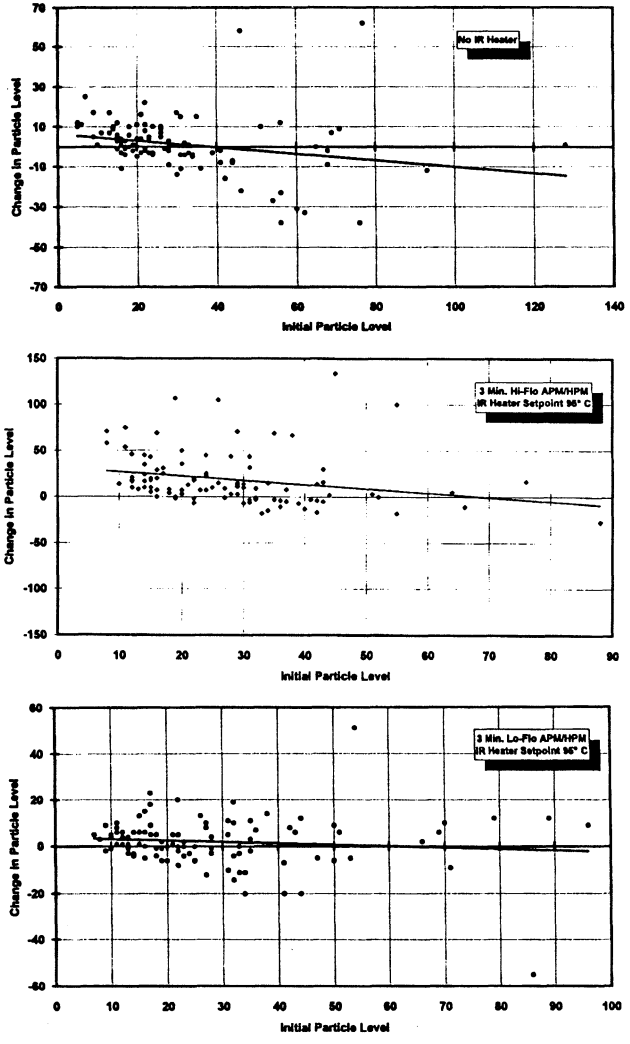
The author would like to thank Brent Carlson, Ed Hanzlik and Jim Oikari for their help in the implementation of and data acquisition with the in-line heater.

REFERENCES

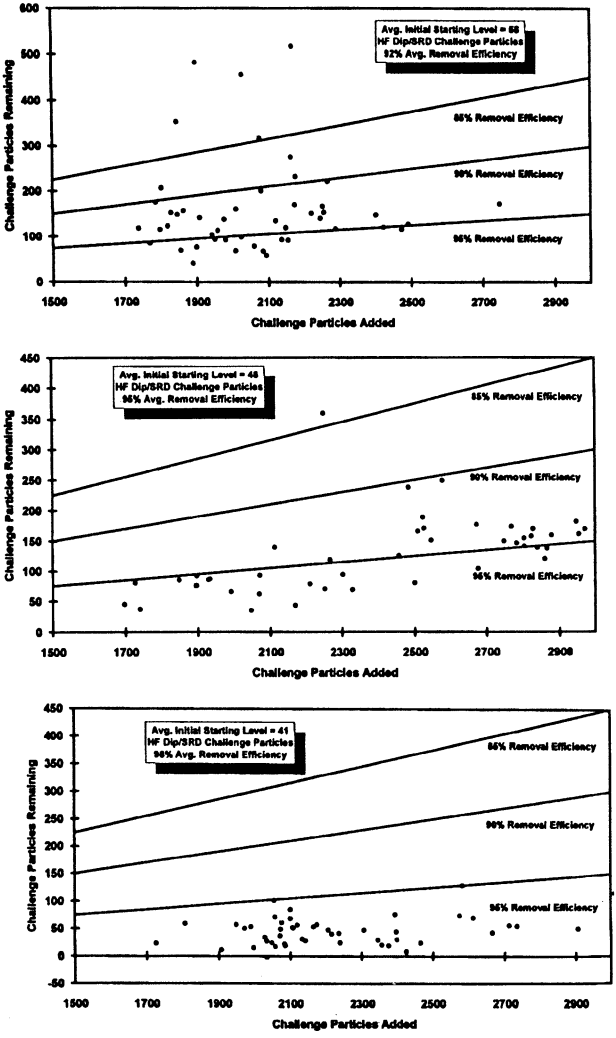
1. M. Meuris, M. Heyns, P. Mertens, S. Verhaverbeke and A. Philipossian, "Investigating Techniques to Improve Gate-Oxide Integrity", Microcontamination, May 1992, p. 31.
2. T. Ohmi, Foresightedness in RCA Cleaning Concept and Their Present Problem", Proc. 8th Workshop on Ultra Clean Technology, Tokyo, Dec. 1990, pp. 5-15.
3. W. A. Syverson, M. J. Fleming and P. J. Schubring, "The Benefits of SC-1 / SC-2 Megasonic Wafer Cleaning", Proceedings of the Second Int'l Symp. on Cleaning Tech. in Semiconductor Device Manufacturing, ECS, 92(12):10-17, 1991.
4. W. Kern and D. Poutinen, "Cleaning Solution Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology", RCA Review, 31, June 1970, pp. 187-205.
5. Y. Sugihara, S. Shimokawa and Y. Oshida, "Influence of Metallic Impurities on SC-1 Cleaning", Proc. 1993 Semiconductor Pure Water and Chemicals Conf., March 1993, Santa Clara, Marjorie Balazs Ed., p. 66.
6. S. Pirooz, J. Coria-Garcia and L. Shive, "The Effect of SC-1 Cleaning of the Surface Microroughness of P+ and P- Wafers", Proceedings of the Second Int'l Symp. on Cleaning Tech. in Semiconductor Device Manufacturing, ECS, 92(12):162-169, 1991
7. M. Itano, F. W. Kern, M. Miyashita and T. Ohmi, "Particle Removal from Silicon Wafer Surface in Wet Cleaning Process", IEEE Tran. on Semiconductor Device Manufacturing, 6 (3), August 1993, p. 258.
8. M. Itano et al., "Particles in ULSI Grade Chemicals and Their Adhesion to Silicon Surfaces", Third Symp. on Particles on Surfaces: Detection, Adhesion and Removal, Fine Particle Soc. Meeting, San Diego, CA, August 1990.
9. B. Donavan, "Particle Deposition", Intensive Short Course in Semiconductor Wafer Cleaning Technology, W. Kern Ed., Austin, TX, 1993.
10. T. Niida et al., "Controlling for Particle Adhesion in Liquids: a Basic Way of Thinking", Chem. Eng. Inst. of Japan, Kansai Branch, Osaka, Japan, pp. 14-25, Sept. 1989.



Figures 1a - 1c. On-wafer temperatures traces for two, 4 minute dispenses of DI water with each followed by brief cold and hot rinses. Dispense flow rates were set to simulate the chemical dispenses: a) 1650 cc/min with in-line heater inactive. b) 2400 cc/min with in-line heater inactive. c) 2400 cc/min with in-line heater active at 95°C set point.



Figures 2a - 2c. Particle addition performance for treatments 1, 2 and 3 for particles larger than 0.15µm. The x axis indicates the initial wafer particle count before the test clean. The y axis indicates the net change in the particle count due to the test clean (post count minus pre count).



Figures 3a - 3c. Particle removal performance for treatments 1, 2 and 3. The x axis indicates the number of "HF Last" challenge particles added to the wafer over and above the count on the precleaned wafer. The y axis indicates the number of these added challenge particles remaining after the clean. Diagonal lines mark the boundaries of 85, 90 and 95% challenge particle removal efficiencies.

CHARACTERIZATION AND MONITORING

EFFECTS OF RESIDUAL IRON CONTAMINATION INTRODUCED DURING WET CHEMICAL PROCESSING ON THIN OXIDE BREAKDOWN AND RELIABILITY CHARACTERISTICS

Worth B. Henley, Lubek Jastrzebski, and Nadim F. Haddad*
University of South Florida, 4202 Fowler Ave, Tampa, FL 33620
*IBM Corporation, 9500 Godwin Dr., Manassas,VA 22110

The effects of residual iron contamination introduced during wet chemical processing on subsequent thermal oxide characteristics are investigated. Iron concentration is measured using a diffusion length technique applicable to real-time line monitoring. The density of gate oxide weak spots is given as a function of iron contamination level for oxide thicknesses ranging from 75 to 200A. Reduction of oxide thickness from 20nm to 10nm requires a reduction in iron contamination by 100 times. Iron contamination limits concerning gate oxide integrity are established.

INTRODUCTION

The relationship between circuit yield and base silicon material properties is often difficult to determine given the complexity of modern ULSI fabrication procedures. The detrimental effects of foreign material particulate defects on circuit yield are relatively easy to understand and visualize, and for this reason have received a great deal of attention in the struggle for better yields. Indeed significant progress in this area now allows routine production of 4, 16, and soon 64 and 256 Mbit complexity circuits. Less obvious are the adverse effects of low level chemical contaminates in the silicon materials. Over time, this class of defect has often been lumped into the somewhat ambiguous category of Non-Visible-Defect (NVD). Formost among these defect generators are transition metal impurities introduced into the silicon through contaminated chemicals or "dirty" processing equipment. Realizing that some background contamination level is unavoidable, understanding how, and at what concentration, contamination begins to adversely effect device operation is critical for process control specifications.

REVIEW OF LITERATURE

Heavy metal contaminates originate in the starting silicon wafers or can be introduced at any of the various stages of IC processing by contaminated chemicals, corroded supply lines, wafer handling, process tooling, etc. A recent survey of over 2000 state-of-the-art Czochralski silicon substrates showed a iron concentration in the range of $5x10^9$ to $1x10^{12}$ cm^{-3} [1,2]. Projected requirements for 200mm ULSI wafers call for iron contamination levels lower that $1.4x10^{11}$ cm^{-3} (approximately 3 parts per trillion) though most suppliers feel even lower contamination levels will be required[3].

Metallic contamination can be introduced into the silicon wafer during almost any process operation in the integrated circuit fabrication sequence. Metallics are generally introduced on the wafer surface from contaminated chemicals, corroded supply lines, improper cleaning, contact with stainless steels, and photoresist processing. If this contamination is not cleaned from the wafer surface , the metal will be diffused into the wafer during subsequent thermal processing. Due to the high diffusivity, metallic surface

contamination becomes distributed throughout the wafer after even minimal thermal processing[2]. Among process related sources, ion implantation, plasma processing, and chemical cleans are most often cited as contamination sources[4,5].

The effect of heavy metal impurities on silicon electrical properties depends on the form the impurity takes in the silicon crystal matrix[6]. Metallic impurities which remain dissolved within the silicon matrix create efficient mid-bandgap recombination centers and thereby reduce minority carrier lifetime. The corresponding increase in generation rate leads to increased diffused junction leakage. Heavy metal impurities may also agglomerate and form distinct, separate phase, high conductivity, metal-silicide precipitates. These precipitates occur within the bulk or at the surface of the wafer. Heavy metal precipitates which occur within the device fabrication region are extremely detrimental to IC yield. Such precipitates degrade thin dielectric and diffused junction properties. The ratio between the amount of precipitated heavy metals and the amount of dissolved, interstitial heavy metals is characteristic for each type of heavy metal and the process conditions.[7,8]

For advanced VLSI process technologies, the most critical yield limiting aspect of heavy metal contamination is the detrimental effect of heavy metal silicide precipitates on thin gate oxide dielectric breakdown[9]. The problem is exacerbated as technology scaling reduces feature size and film thickness such that the precipitate defects are more pronounced in effect. Previous studies which have investigated the effects of iron impurity contamination on silicon devices have shown that iron precipitates primarily as a rod-like $FeSi_2$ phase[8]. These precipitates were shown to occur at or near the silicon surface or Si-SiO_2 interface[10] and can reduce the breakdown voltage of thin SiO_2 layers. Most of these experiments were performed at very high levels of iron contamination, e.g. [Fe]=10^{14} to 10^{15} cm^{-3}, which is much above the range required for state-of-the-art micron and sub-micron fabrication technologies.

EXPERIMENTAL PROCEDURE

The experimental effort consisted of MOSDOT fabrication on clean wafers and on wafers intentionally contaminated with iron. Throughout all the processing steps, extreme care was taken to avoid the uncontrolled introduction of metal contaminates. High quality 2 ohm-cm, <100>, 3" p-type float zone wafers were used for the experimentation. Float zone wafers were chosen to eliminate any unwanted internal gettering uncertainties. During several of the experimental runs, equivalent Czochralski process wafers were included for comparison to the float zone wafer results.

Following a SC1/HF/SC2 clean sequence, wafers were intentionally contaminated with iron by spin applying a 1 to 40 ppm aqueous $FeCl_3$ solution onto the wafer before the oxidation following the procedure described by Hourai [11]. A controlled amount of contaminated solution is applied to the hydrophilic wafer surface while the wafer is stationary on a teflon spinner chuck. The solution is left in contact with the wafer surface for 60 seconds. After the adsorption period, the wafer is spun dry at ~3500 rpm. Following the contamination procedure, the wafers were taken immediately for oxidation. Control samples were withheld from the contamination procedures to provide reference oxide quality data.

The surface iron contamination was driven into the wafer bulk by an in-situ anneal in N_2 at the oxidation temperature for 25 minutes before the oxygen flow began. For all the furnace process runs, quartzware boats were kept separate as to which had contained

the iron contaminated samples and which had the clean samples. Thermal oxides of 7.5, 10, 13, 16, and 20 nm were grown at 850°C and 900°C in dry O_2. Aluminum electrodes were formed by thermal evaporation to define the MOSDOT capacitors. The wafers were subsequently annealed for 20 minutes at 450°C in a 5% H_2/95% N_2 forming gas ambient.

Iron concentration was measured on all samples after oxidation via diffusion length analysis. Diffusion length was measured using a surface photovoltage (SPV) procedure[12]. The iron concentration analysis procedure using diffusion length measurements is outlined in detail by Zoth[2]. The SPV iron determination method provides an iron detection limit of ~$1x10^{10}$ cm^{-3}. Iron concentration on the samples tested covered a range of 10^{10} cm^{-3} to 10^{14} cm^{-3}.

Oxide breakdown was determined in accumulation mode by applying a ramp voltage stress of 1MV/cm/sec until a current of 0.02 to 0.2 A/cm^2 was exceeded (dependant upon the oxide thickness). At this current level, significant deviation from Fowler-Nordheim tunneling had occurred. TDDB stress testing was performed by applying constant electric field (typically 10MV/cm) and monitoring the leakage current through the capacitor. Approximately 250 MOSDOTs were used for the ramp voltage I-V testing and 100 MOSDOTs on each wafer were used for the TDDB testing. All testing was performed at 22°C.

EXPERIMENTAL RESULTS

The spin on technique proved very effective at introducing iron contamination into the silicon wafers. There was some lack of reproducibility in the low concentration samples, but nevertheless a spectrum of samples in the desired concentration range was obtained. The oxidation temperature also had an effect on resulting silicon contamination level for a given solution contamination concentration. The 900°C oxidation repeatably resulted in about 2 to 3 times more iron contamination than the 850°C oxidation for the same contamination solution. This is most likely a result of solid solubility considerations. The solubility of iron at 900°C is approximately $1x10^{14}$ $atoms/cm^3$, while the solubility at 850°C is approximately $5x10^{13}$ $atoms/cm^3$. Figure 1 shows the measured wafer iron contamination level as a function of the solution concentration for the two different processing temperatures. The oxidation time had very little effect on the contamination level achieved.

During the contaminated oxidations, clean wafers were interspersed with the intentionally contaminated wafers to monitor any cross contamination that occurred between the wafers. Results from these measurements are shown in figure 2. Wafers upstream from the contamination are not effected were not affected by the iron doped wafers. Wafer 8, a clean wafer sandwiched between two highly contaminated wafers, experienced a 2X increase in iron contamination level compared to clean wafers not in direct proximity to the contamination. While this increase is certainly significant, it was less than expected considering the proximity to the iron doped wafers. This result suggests that iron contaminates are not efficiently transported in the vapor phase from wafer to wafer during the oxidation process. Subsequent oxidation runs in the furnace showed the furnace baseline background iron contamination level of approximately $5x10^{10}$ $atoms/cm^3$ was not effected (within the measurement error) by the iron contaminated wafer oxidation.

Oxide Breakdown and Reliability Testing

The detrimental effects of low level iron contamination on gate oxide quality is clearly shown by the ramp voltage oxide breakdown testing. The critical iron concentration

at which oxide breakdown voltage degrades is a function of the oxide thickness, with thinner oxide layers being more susceptible to contamination. This trend is illustrated in figure 3, which shows oxide breakdown field histograms for the 20, 16, 13, 10, and 7.5 nm oxides, each with approximately $5x10^{12}$ cm^{-3} iron concentration. At this iron contamination level, the oxides thicker than 13 nm are only slightly effected, defect density is low and the breakdown field is near 12 MV/cm, typical of high quality oxides. Once the oxide thickness approaches 10nm or less, a distinct degradation in oxide quality at this iron concentration is noticed. For [Fe] = $5x10^{12}$ cm^{-3}, the 10nm oxide mean breakdown field is reduced to only 7.5 MV/cm and a wide dispersion in breakdown field exists across the wafer. At this contamination level, The 7.5 nm oxide is very poor quality with average breakdown field of 1.3 MV/cm and defect dominated breakdown behavior.

Oxide defect density analysis is shown in figure 4, where defect density is plotted as a function of iron concentration for the oxide thicknesses evaluated. The evidence of a critical iron contamination threshold for each oxide thickness is clearly shown in this figure. As would be expected, the iron contamination threshold which degrades oxide quality decreases as the oxide thickness is reduced.

Time Dependent Dielectric Breakdown (TDDB) oxide reliability testing evaluates the wearout lifetime of gate oxides. TDDB test results for the various oxide thicknesses are shown in figures 5a through 5d. The detrimental effects of low level iron contamination on oxide lifetime are clearly shown by this test data. For each of the iron contaminated samples, the distinct change in slope of the TDDB failure curves indicates activation of a second breakdown mechanism occurs between 10^3 and 10^4 seconds as a result of the high field stress. Referring to figure 5b, the oxide failure rate is seen to increase dramatically, then return to the initial slope value. The increased failure rate is due to the rapid wearout of MOSDOTs that contain iron silicide precipitates. Once these MOSDOTs have failed, the remaining MOSDOTs which do not contain precipitates fail at the expected log-normal rate, and the slope returns to the initial expected value. Such a mechanism is consistent with our model which relates oxide failure to iron-silicide precipitates at the $Si-SiO_2$ interface. The enhancement in local electric field around the precipitate causes increased charge injection.

Gate oxide thickness has distinct effect on the iron contamination relation to reliability failure. For the 20nm oxides, for even the highly contaminated [Fe] = $4x10^{13}$ cm^{-3} sample, approximately 10^4 seconds elapse before significant oxide wearout begins to occur. Equivalent concentration levels for thinner oxides cause rapid oxide failure. Contamination levels above the threshold level for the particular oxide thickness significantly reduce the oxide quality. The TDDB data is summarized in figure 6, which plots time to 50% failure (t_{50}) versus iron concentration for the various oxide thicknesses. For these stress conditions and a given desired lifetime, the maximum acceptable iron contamination limits can be determined.

Iron Contamination Control Limits for Advanced ULSI Processing

At this point, it is relevant to compare iron contamination thresholds indicated critical by the TDDB test to those identified by our previous iron-induced defect density analysis. By comparing the iron concentration which results in TDDB $t_{50} = 10^5$ seconds to the iron concentration which causes a defect density = 2 defects/cm^2, a decision can be made as to which is the limiting gate oxide degradation factor, TDDB reliability or defect density. These comparison criteria (10^5 sec and 2 defects/cm^2) were determined by a review of relevant literature concerning ULSI yield and reliability projections. The results of this comparison analysis (figure 4 to figure 6) are shown in Table 1. The critical iron contamination thresholds for the two types of testing are very close. This test method

cross-correlation increases the confidence of the contamination control limits which must be set for each oxide thickness.

Table 1: Comparison of threshold iron contamination control limits determined by TDDB stress results and ramp voltage oxide breakdown defect density testing. Threshold criteria are time to 50% failure for the TDDB stress results and contamination level at 2 defects/cm^2 for the ramp voltage testing.

T_{ox} (nm)	Iron Concentration(cm^{-3}) @ $t_{50} = 10^5$ sec	Iron Concentration(cm^{-3}) @ Defect Density = 2 defects / cm^2
8	$1x10^{11}$	$8x10^{10}$
10	$4x10^{11}$	$3x10^{11}$
13	$1x10^{12}$	$1x10^{12}$
20	$1x10^{13}$	$2x10^{13}$

Oxide Failure Mechanism Related to Iron Contamination

The review of literature presents several studies that demonstrate the following: 1) during oxidation, iron contaminates pile-up at the Si-SiO_2 interface, 2) iron precipitation is enhanced by silicon self-interstitials released during thermal oxidation, 3) iron precipitates as a rod-like conductive $FeSi_2$ phase, 4) precipitates form at the Si-SiO_2 interface and can penetrate the oxide region, and 5) oxide breakdown can occur as a result of interface metallic precipitates.

Data collected during this study is consistent with the above findings. The proposed physical failure model is shown in figure 7. The failure mechanism combines the reported properties of iron in silicon with electrical test data on oxide breakdown characteristics. Iron contamination introduced from the wafer surface is quickly incorporated by rapid in-diffusion during the beginning of the hot process cycle. The interstitial iron precipitates as iron-silicide ($FeSi_2$) due to the impurity supersaturation that occurs during wafer cooling from high temperature (>800°C) operations. These precipitates tend to form at the Si-SiO_2 interface because of impurity pile-up and enhanced nucleation during the oxidation process. At the very low contamination levels used in this study, direct observation of iron precipitates in silicon is near impossible using imaging techniques. Key to the analysis is the finding that the precipitate weak spots are especially detrimental because of the 'lighting-rod' effect which occurs due to the conductive singularity protruding into the dielectric medium. Thus, the electrical effects of very small precipitate defects are magnified far beyond what is explainable by oxide thinning considerations alone. This, combined with the fact that the gate oxide is so very thin (i.e., 6 to 10 nm = 10 to 25 atoms thick), explains why such minute trace contamination levels of iron in silicon are very detrimental to gate oxide quality.

CONCLUSIONS

The susceptibility of thin silicon oxides to low-level iron contamination has been evaluated by comparing the oxide breakdown and reliability characteristics of oxides grown on clean wafers to oxides grown on wafers intentionally contaminated with iron. Extreme care was taken throughout the experimentation to eliminate and control second order oxide

breakdown mechanisms not related to iron contamination. Experimental results show the dramatic lowering of gate oxide integrity (GOI) and Time Dependent Dielectric Breakdown (TDDB) reliability quality in the presence of iron contamination. Using the experimental data, iron concentration control limits have been set which must be met to maintain a given oxide quality level. The control limits were determined by analyzing the GOI/oxide defect density results together with the TDDB wearout results. Both test methods correlate well to indicate the threshold iron contamination limits which must be maintained to produce high quality gate oxide layers. As expected, thinner oxide films require more stringent contamination control specifications. The data indicates that a reduction of oxide thickness from 20nm to 10nm, corresponding to a transition from 1.0μm to 0.5μm technology, requires a reduction in iron contamination level by two orders of magnitude (from 10^{13} cm^{-3} to 10^{11} cm^{-3}).

ACKNOWLEDGEMENTS

This work was supported by the Florida SRC/Sematech Center of Excellence (SCOE) program and the IBM Corporation.

REFERENCES

1. L. Jastrzebski, W. Henley, C. Neuse, *Solid State Technology* , (Dec. 1992), p. 27.
2. G. Zoth, W. Bergholz, *Journal of Applied Physics*, **67**, 6764 (1990).
3. M. Watanabe,*Solid State Technology*, (April 1991), p. 133.
4. T. Ohmi, et al., *Journal of the Electrochemical Society*, **139**, 3317-3335 (1992).
5. *Nikkei Microdevices* , (1990), p. 54.
6. A. Ohsawa, et al., *Semiconductor Silicon 1990*, **90-7**, 601-613 (1990).
7. K. Hiramoto, et al., *Journal of Applied Physics*, **28**,12,L2109-2112 (1989).
8. K. Honda, et al., *Applied Physics Letters*, **46**, 582-584 (1985).
9. L. Jastrzebski, *Semiconductor Silicon 1990*, **PV90-7**, 614-627 (1990).
10. R. Takizawa, et al., *Journal of Applied Physics*, **62**, 4933-4935 (1987).
11. M. Hourai, et al., *Japanese Journal of Applied Physics*, **27**,12, L2361 (1988).
12. J. Lagowski, et al., *Semiconductor Science Technology*, **7**, A185-A192 (1992).

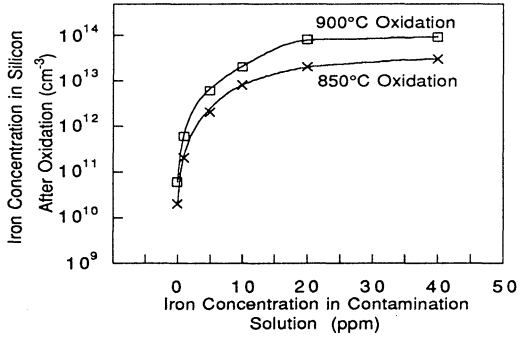


Figure 1: Iron contamination in silicon wafer resulting from spin-application of iron contaminated solution. At high solution contamination levels the wafer concentration saturates at the iron solubility level for the given oxidation temperature.

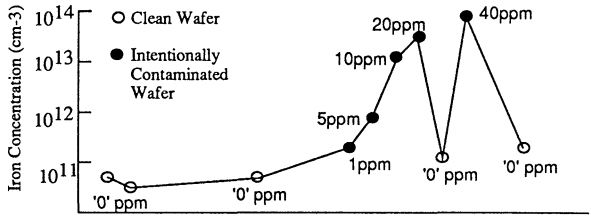


Figure 2: Effect of wafer position in furnace on resulting iron contamination. "Clean" wafers were interspersed among the intentionally contaminated wafers to monitor cross contamination within the oxidation process. Very little cross contamination of the clean wafers occurred.

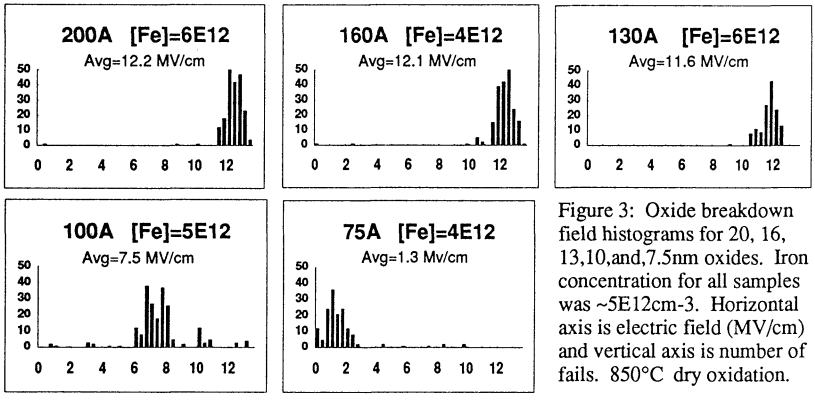


Figure 3: Oxide breakdown field histograms for 20, 16, 13,10,and,7.5nm oxides. Iron concentration for all samples was ~5E12cm-3. Horizontal axis is electric field (MV/cm) and vertical axis is number of fails. 850°C dry oxidation.

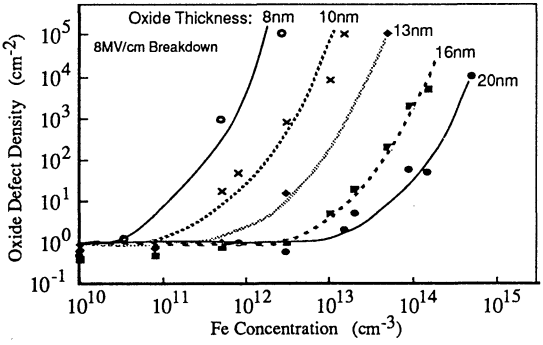


Figure 4: MOSDOT capacitor data. Oxide defect density versus iron contamination level. A defect is defined as breakdown occurring at less than 8MV/cm during ramp voltage I/V test.

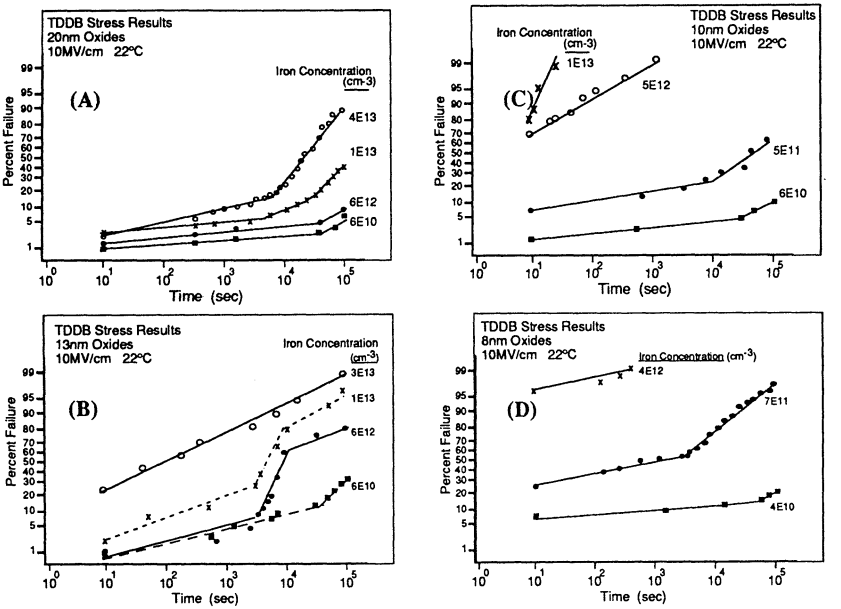


Figure 5: TDDB data for various iron concentrations and oxide thicknesses. 100 MOSDOTs were tested for each oxide thickness and iron concentration. Oxide thicknesses: (a) 20nm, (b) 13nm, (c) 10nm, (d) 8nm.

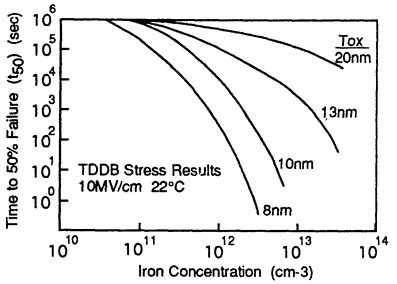


Figure 6: Time to 50% population failure (t_{50}) versus iron concentration for varous oxide thicknesses. Increased iron concentration significantly reduces the oxide wearout lifetime.

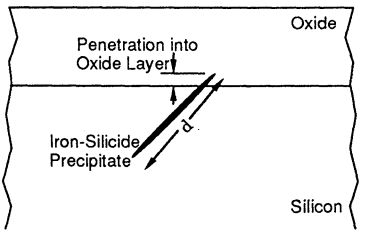


Figure 7: Oxide failure model related to iron contamination. Iron-silicide precipitates at the Si-SiO_2 interface cause oxide weak spots and enhanced charge injection resulting in oxide breakdown.

SURFACE RECOMBINATION VELOCITY AND RECOMBINATION LIFETIME IN IRON CONTAMINATED SILICON

A. Buczkowski, F. Shimura, and G. A. Rozgonyi
Department of Materials Science and Engineering
North Carolina State University
Raleigh, NC 27695-7916

A theoretical simulation of available experimental data on recombination lifetime and surface recombination velocity in silicon samples contaminated with iron has been performed. Both, n-type and p-type samples have been studied based on experimental data, determined primarily by deep level transient spectroscopy and photoconductance decay, for samples intentionally doped with iron. Differences observed for n- and p-type silicon, as well in the absolute value of bulk lifetime and the surface recombination velocity, along with their temperature dependencies are explained. The effect of iron contaminants present in concentrations typical of modern silicon device material has been evaluated by comparing the theoretical lifetime results to the experimental data. Finally, the problem of "true" bulk lifetime determination by transient photoconductance is discussed in terms the total recombination process which proceeds via both bulk and surface recombination centers.

INTRODUCTION

Iron in p-type silicon is present in two forms, namely interstitial iron Fe_i and the iron-boron complex FeB. The ratio of Fe_i to FeB is dependent on the total iron and boron concentrations, and temperature [1-3]. At room temperature and below iron is typically paired with boron, while at temperature above 180 °C this complex dissociates and interstitial Fe_i prevails. In n-type silicon the only form is the Fe_i. Both Fe_i and FeB recombination centers are donor in nature; however, they are characterized with different electrical properties and recombination activity. In addition to iron, additional unknown background contamination can independently coexist. This unknown defect can be modeled as a type III recombination center. It is assumed that bulk states are localized in the energy domain and each defect creates one single state with fixed energy. Electrical properties of defects used for theoretical simulations of bulk lifetime are listed in Table I. For surface states we assume for recombination velocity calculations that two independent types of surface states are continuously distributed within the silicon forbidden bandgap. The first type originates from the silicon/silicon dioxide interface and is characterized with a parabolic energy distribution. These states are donor in nature when located below the middle the bandgap, and acceptor when located above [4]. The second type surface states are described with a gaussian distribution and originates from surface contamination by iron. These two types of surface states are responsible for the presence of surface charge Q_{it}, which is neutralized by a charge contained in the near-surface space charge region, Q_{scr}. Additionally, a constant fixed positive charge within the oxide, Q_f, is assumed for calculations. A full list of data used for surface recombination velocity calculations is presented in Table II.

Table I. Electrical properties of defects used for theoretical simulations of bulk lifetime

name	p-type	n-type	comments	
n_d	$1*10^{15}$	$1*10^{15}$	doping concentration	[cm^{-3}]
n_e	0.	0.	excess electron concentr.	[cm^{-3}]
n_{tot}	$5*10^{10}$	$5*10^{10}$	total Fe concentr.(Fe_i + FeB)	[cm^{-3}]
U_o	$1.0*10^{-23}$	0.0	pre-exp factor	[cm^3]
U	0.68	--(a)	binding energy	[eV]
E_{t1}	-0.46	--(a)	energy FeB	[eV]
σ_{p1}	$1.5*10^{-14}$	--(a)	hole capt. cross sec. FeB	[cm^2]
σ_{n1}	$5.*10^{-13}$	--(a)	electr. capt. cross sec. FeB	[cm^2]
E_{t2}	-0.19	-.19	energy Fe_i	[eV]
σ_{p2}	$4.4*10^{-16}$	$4.4*10^{-16}$	hole capt. cross sec. of Fe_i	[cm^2]
σ_{n2}	$6.3*10^{-15}$	$6.3*10^{-15}$	electr. capt. cross sec. Fe_i	[cm^2]
n_{t3}	$2*10^{10}$	$2*10^{10}$	background trap III concentr.	[cm^{-3}]
E_{t3}	0.3	0.3	energy trap III	[eV]
σ_{p3}	$1*10^{-15}$	$1*10^{-15}$	hole cap. cross sec. trap III	[cm^2]
σ_{n3}	$1*10^{-14}$	$1*10^{-14}$	electr. cap. cross sec. trap III	[cm^2]

(a) not applicable in n-type silicon

Table II . Electrical properties of defects used for theoretical simulations of surface recombination velocity

name	value	comments	
n_f	$1*10^9$	density of states in oxide	[cm^{-2}]
n_{it1}	$1*10^{10}$	surf. states with parabolic distr.	[cm^{-2}]
σ_{p1}(a)	$1*10^{-17}$	hole cap. cross section	[cm^2]
σ_{n1}(a)	$1*10^{-16}$	electron cap. cross section	[cm^2]
σ_{p1}(b)	$1*10^{-16}$	hole cap. cross section	[cm^2]
σ_{n1}(b)	$1*10^{-17}$	electron cap. cross section	[cm^2]
n_{it2}	$1*10^9$	surf. states with gauss. distr., Fe_i	[cm^{-2}]
E_{t2}	-0.19	energy of Fe_i	[eV]
σ_{p2}	$4.4*10^{-16}$	hole capture cross section of Fe_i	[cm^2]
σ_{n2}	$6.3*10^{-15}$	electr. capt. cross section of Fe_i	[cm^2]

(a) for states located below, and (b) above the middle of the forbidden bandgap

RESULTS

Bulk Lifetime

It is assumed that the recombination process is controlled by three kinds of recombination centers: thus, the total bulk recombination lifetime is given by formulae:

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{FeB}} + \frac{1}{\tau_{Fe}} + \frac{1}{\tau_{III}} \qquad [1]$$

where τ_{FeB}, τ_{Fe}, and τ_{III} are related to iron-boron complex, interstitial iron and unknown background contamination, respectively. Each bulk lifetime component can be described by the Shockley-Read-Hall theory, as illustrated below:

$$\frac{1}{\tau_k} = \frac{1}{\sigma_{n,k} v_{th} n_{t,k}} \left(\frac{p_0 + p_{1,k} + \Delta n}{p_0 + n_0 + \Delta n} \right) + \frac{1}{\sigma_{p,k} v_{th} n_{t,k}} \left(\frac{n_0 + n_{1,k} + \Delta n}{p_0 + n_0 + \Delta n} \right), \; k = 1, 2, 3 \qquad [2]$$

The meaning of used symbols is listed in Table I; for more detailed explanation see, for example, Ref. 5. The temperature dependent concentration of iron-boron and substitutional iron is and given by Eqn. 3:

$$n_{FeB} = n_{tot} n_d U_0 \exp\left(\frac{U}{kT}\right) / \left[1 + n_d U_0 \exp\left(\frac{U}{kT}\right) \right]$$
$$n_{Fe} = n_{tot} - n_{FeB} \qquad [3]$$

The results of theoretical simulations for bulk lifetime are presented in Figs. 1a and b, where the temperature dependence of lifetime for p- and n-type silicon is shown, respectively. The influence of background recombination centers is also illustrated. Note that the bulk lifetime at room temperature is lower in a p-type sample than in an n-type sample, (290 µs vs. 1500 µs), even though iron in p-type silicon forms the shallow FeB complex, which is less active than the deeper Fe_i present in n-type material. This difference results from both, the donor nature of iron and the larger capture cross section of FeB pair with respect to Fe_i. Recall that the recombination activity of a defect is not solely dependent on energy level, but on the combined action of energy, capture cross section and donor/acceptor nature of defect. Not only the room temperature lifetime, but also the temperature dependence of lifetime for p- and n-type silicon are significantly different from each other, as illustrated in Fig. 2. This difference derives from the dissociation of FeB pairs observed only in p-type material. As a result, the lifetime vs. temperature curve is characterized with a local minimum at temperatures about 180°C. In n-type silicon, where the only form is interstitial Fe_i, a monotonic lifetime increase with temperature obtains. The theoretical simulations are summarized in Table III.

Table III. Bulk recombination lifetime components for data of Table I.

type	total [µs]	FeB [µs]	Fe_i [µs]	background contaminant [µs]
p-type	290	340	$1*10^6$	2160
n-type	1560	---	2380	4520

Surface Recombination Velocity

The total concentration of surface states n_{it} is given by:

$$n_{it} = \sum_{k=1}^{2} n_{it,k} \qquad [4]$$

where the n_{it1} and n_{it2} components originate from the silicon/silicon dioxide interface and surface iron contamination, respectively:

$$n_{it,k} = \int_{E_v}^{E_c} D_{it,k}\, dE \qquad [5]$$

It is assumed based on some experimental evidences [4,6], that the n_{it1} energy distribution can be described by parabolic function, while due to insufficient information the n_{it2} was arbitrarily selected to be gaussian, with the maximum located at the energy observed by deep level transient spectroscopy for bulk defects associated with interstitial iron. Thus,

$$D_{it1}(E) = A(1 + B E^2) \qquad [6]$$

$$D_{it2}(E) = C \exp\left[-\left(\frac{E - E_{t2}}{2D}\right)^2\right], \quad \text{for } E_v < E < E_c \qquad [7]$$

where A, B and C, D are defect distribution parameters associated with parabolic and gaussian curves, respectively. Furthermore, it was assumed that capture cross sections of surface states, as listed in Table II, were energy independent, although the proposed solution is not restricted in this term. Calculations for n- and p-type material were performed for the same set of data, with the Fermi level location as the only difference. Total integrated concentrations of surface states $n_{it1}=10^{10}$ cm^{-2}, and $n_{it2}=10^{9}$ cm^{-2} were assumed, respectively, as illustrated in Fig. 3. These states yield a value for surface charge which is controlled by the Fermi level position (e.g. doping concentration) with respect to the surface state level and donor or acceptor nature of the state. In addition to fast state charge, there was a fixed positive charge $n_f = 10^9$ cm^{-2} present within the oxide layer. In order to satisfy the charge neutrality requirement the fast state and fixed oxide charges are compensated by the Q_{scr}. As a result, the semiconductor bands bend at the surface, and surface potential is generated [7,8]. The surface potential V_s can be found as a root of the charge balance equation:

$$Q_f + Q_{it}(V_s) + Q_{scr}(V_s) = 0 \qquad [8]$$

where

$$Q_{it}(V_s) = \int_{E_v}^{E_c} \left[q_{it1}(V_s) + q_{it2}(V_s)\right] dE \qquad [8a]$$

and

$$q_{it,k}(V_s) = q\left[F^* - f_{s,k}(V_s)\right] D_{it,k}\ ; \qquad F^* = \begin{cases} 1 & \text{for donor states} \\ 0 & \text{for acceptor states} \end{cases} \qquad [8b]$$

$$f_{s,k}(V_s) = \left(1 + \exp\frac{E_{t,k} - E_F - q V_s}{kT}\right)^{-1} \qquad [8c]$$

The q and E_F is the electronic charge and the Fermi level, respectively. Detailed description of the Q_{scr} charge component can be found in Ref. [6,7]. The energy distribution of surface charge without oxide charge included, at the total charge equilibrium condition is presented in Fig. 4 (a) and (b), respectively, for n- and p-type silicon. This distribution is obviously

different from the distribution of surface states since some surface states are neutral while others are charged (positively for donor and negatively for acceptor states). In case of n-type material, for data listed in Table II, the total surface charge including oxide is negative, while for p-type it is positive. The corresponding surface potential is also negative and positive, respectively. These energy distributed surface states give rise to a surface recombination process [8] whose activity depends on the surface state concentration and their location affected by surface potential with respect to Fermi level. Surface recombination velocity is also consisted of two components:

$$S = \sum_{k=1}^{2} S_k(V_s) \qquad [9]$$

where

$$S_k(V_s) = \upsilon_{th} \sqrt{\sigma_{n,k}\sigma_{p,k}}\, \frac{(n_0 + p_0)}{2 n_i}\, J_k(V_s)$$

$$J_k(V_s) = \int_{E_v}^{E_c} \frac{D_{it,k}}{\cosh\left[\frac{E - E_i}{kT} - u_{0,k}\right] + \cosh\left(\frac{q V_s}{kT} + \frac{E_F - E_i}{kT} - u_{0,k}\right)} dE \qquad [9a]$$

and

$$u_{0,k} = \ln\left(\sqrt{\frac{\sigma_{p,k}}{\sigma_{n,k}}}\right)$$

with n_i and E_i being the intrinsic carrier concentration and the energy of the middle of forbidden bandgap (set to be zero, reference level), respectively. Finally, the surface lifetime and the effective lifetime as measured, for example, with a transient photoconductance technique, can be expressed as follow:

$$\tau_{surf} = \frac{1}{\frac{2}{\alpha D}} \qquad [10]$$

with α being the first root of

$$\tan(\alpha d / 2) = \frac{S}{\alpha D} \qquad [11]$$

and

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surf}} \qquad [12]$$

Results of numerical calculations for surface potential, charge, recombination velocity and lifetime at room temperature are summarized in Table IV.

Table IV. Surface potential, charge, recombination velocity and lifetime for p- and n-type silicon for data listed in Tables I and II.

type	V_s [mV]	Q_f+Q_{it} [cm^{-2}]	S_1[a] [cm/s]	S_2[b] [cm/s]	S [cm/s]	τ_{surf}[c] [µs]	τ_{eff} [µs]
n	-2	-1.6E9	5.6	8.4	14	2350	940
p	+10	+4.5E9	5.6	119	125	269	139

surf. rec. vel. resulting from (a) SiO2/Si interface, and (b) iron contamination
(c) wafer thickness d = 650 µm assumed

CONCLUSIONS

Theoretical simulations of bulk lifetime and surface recombination velocity illustrate that:

- bulk lifetime for silicon contaminated with iron is lower in p-type than in n-type material by about one order of magnitude. This difference is attributed to the donor nature of iron recombination centers. This lifetime is of the order of several hundred microseconds in p- and several milliseconds in n-type material.
- experimental lifetime data observed for commercial n- and p-type silicon show that this material is contaminated with iron at concentrations of about 10^9 cm^{-2}.
- temperature dependence of lifetime in p-type samples contaminated with iron is characterized with a specific local minimum around 180°C. This minimum results from Fe-B complex dissociation. In n-type samples iron is located interstitially and a monotonic increase of lifetime with temperature is observed.
- surface recombination velocity is higher in p-type material then in n-type by about one order of magnitude. This recombination velocity results from both the SiO_2/Si interface, and surface iron contamination; however, at low and moderate iron contamination levels ($<10^9$ cm^{-2}), it is governed mainly by SiO_2/Si states. Typical values of srv are of the order of several hundred cm/s while for n-type several tens of cm/s.
- surface lifetime simulated for oxidized samples is of the same order of magnitude as the bulk lifetime and is longer for n-type material than for p-type. Therefore, an effective lifetime is determined by photoconductance decay measurements and its value is limited by the lower recombination component, bulk or surface. Even for samples not contaminated with iron, the effective lifetime would not exceed values which result from the recombination activity of SiO_2/Si surface states, i.e. several hundred microseconds for p- and several milliseconds for n-type silicon. Since n-type surface lifetimes are higher than those in p-type, the effective lifetime for n-type silicon is longer.

ACKNOWLEDGMENTS

Authors would like to acknowledge W. Huber from MEMC Electronic Materials and H. Daio from Showa Denko for stimulating discusions.

REFERENCES

1. G. Watkins, Semicond. Sci. Technol., **6**, B111 (1991)
2. L. Kimmerling and J. Benton, Physica, **116B**, 297 (1983)

3. Y. Hayamizu, T. Hamaguchi, S. Ushio, T. Abe and F. Shimura, J. Appl. Phys., **69**, 3077 (1991)
4. *Ionizing Radiation Effects in MOS Devices and Circuits*, eds. T. Ma and P. Dressendorfer, John Wiley, New York (1989)
5. A. Buczkowski, Z. Radzimski, Y. Kirino, F. Shimura and G. Rozgonyi, in *Defects in Materials*/1991, P. Bristowe et al., Editors, **209**, p. 567, Materials Research Society, Pittsburgh, Pennsylvania
6. A. Many, Y. Goldstein and N. Grover, *Semiconductor Surfaces*, North Holland Publishing Comp., Amsterdam (1965)
7. A. Buczkowski, G. Rozgonyi and F. Shimura, Jap. J. Appl. Phys., **32**, L218 (1993)
8. D. Fitzgerald and A. Grove, Surface Science, **9**, 347 (1968)

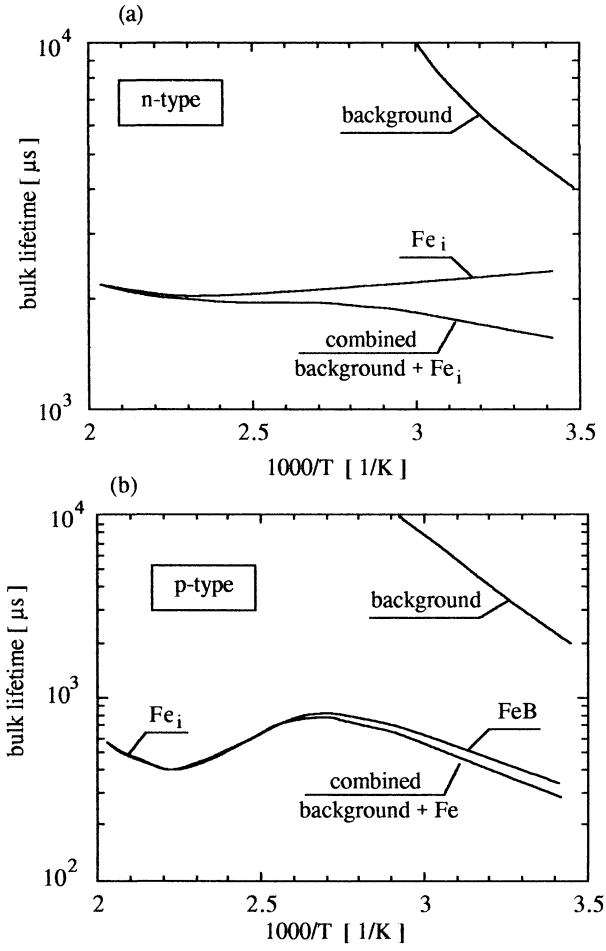


Fig. 1. Theoretical temperature dependence of bulk recombination lifetime for (a) n-type and (b) p-type silicon contaminated with iron. An additional lifetime reduction due to an unknown background contamination is also shown.

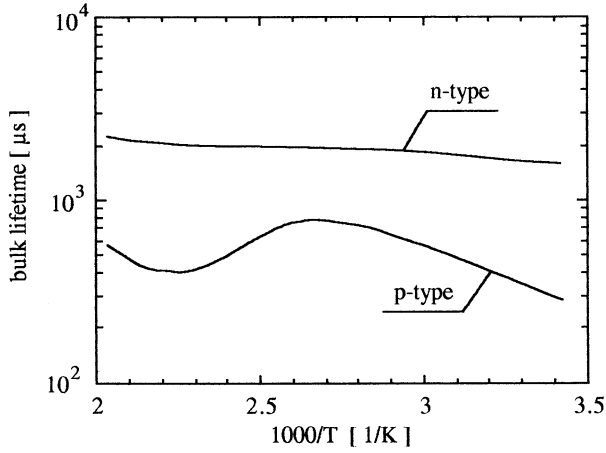


Fig. 2. Comparison of bulk recombination lifetime for n- and p-type silicon contaminated with the same amount of iron, $N_{Fe}=5*10^{10}cm^{-3}$.

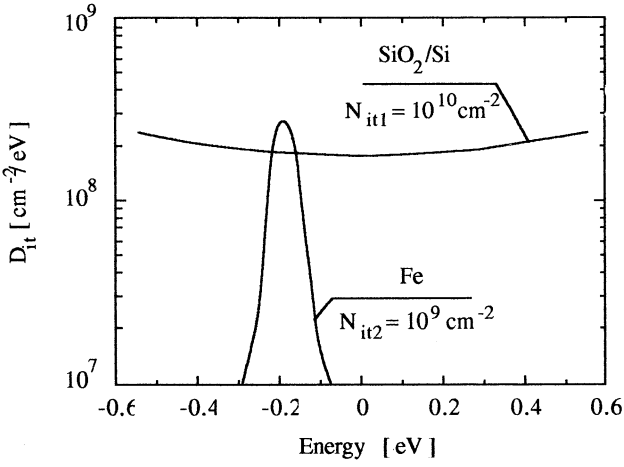


Fig. 3. Energy distribution of surface states resulting from SiO_2/Si interface (parabolic curve, donor type for negative and acceptor for positive energies, respectively) and from surface contamination by iron (gaussian curve, donor type).

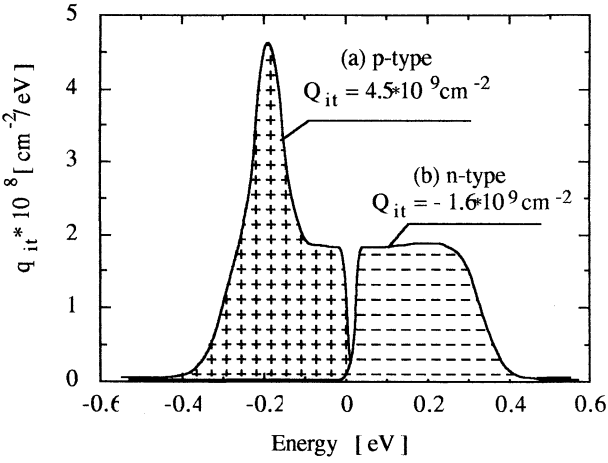


Fig. 4. Energy distribution of combined surface state charge resulting from SiO_2/Si interface and iron contamination for (a) p-type and (b) n-type silicon.

MONITORING AND OPTIMIZATION OF SILICON SURFACE QUALITY

Hichem M'saad, Jurgen Michel, A. Reddy, and L. C. Kimerling

Department of Materials Science and Engineering
Massachusetts Institute of Technology
Cambridge, MA 02139

We have used contactless photoconductance decay measurements to monitor cleaning processes, surface contamination and surface roughness. Changes in surface chemistry are evidenced by a degradation (increase) in the surface recombination velocity (decrease in measured decay time). We have applied the tool to monitor cleaning effectiveness, surface cleanliness and roughness during cell processing.
We show that 5×10^{-4} M of I_2 in methanol is sufficient to electrically passivate the silicon surface with iodine. The measured minority carrier lifetime in this solution is 90% of that in 48% HF. We illustrate that I-terminated silicon surfaces are more stable than H-terminated surfaces. We confirm that deionized water is responsible for the roughening of silicon surfaces. We show that NH_4F is a superior alternate clean to dilute HF.

INTRODUCTION

The preparation of the silicon surface prior to various processing steps has become one of the most critical issues in semiconductor fabrication. Control of the silicon surface chemistry and topography is crucial. HF etching has been the key step in producing contamination-free and chemically stable silicon surfaces. We demonstrate that iodine termination of silicon dangling bonds leads to a more electrically stable Si surface than hydrogen termination. We also show that NH_4F solutions provide an electrically superior surface termination than HF-treated surfaces. We attribute these results to the fact that basic solutions produce atomically flat surfaces as compared to the atomically rough HF-treated surfaces.

Because of its simplicity, non destructive nature, and *in situ* measurement capability, radio-frequency photoconductance decay spectroscopy (RF-PCD) is a major tool for the study and characterization of semiconductor surfaces in our laboratory. Minority carriers injected by a xenon flash lamp produce eddy currents which are detected as transient absorption of the rf signal. The signal decays are digitized

and analyzed by computer. A block diagram of the inductively coupled apparatus, operating at 50 MHz, is shown in Figure 1. The wafer is placed over a 3 cm-diameter coil. The circuit coil acts as the primary of a transformer while the wafer acts as its secondary counterpart. In this study, we use RF-PCD to achieve improvements in semiconductor cleaning technology as a process monitor of surface recombination velocity.

STANDARD CLEAN PROCEDURE

Before minority carrier lifetime measurement, the wafer is first cleaned to remove any surface contamination. Our initial cleaning procedure was a three-step process whereby the wafer is first piranha-etched for one minute, rinsed with DI water with a resistivity of 18 MΩ-cm, and dilute HF (DHF) etched for one minute. After HF etching, the surface is predominantly terminated by hydrogen (1). The H-terminated surface is hydrophobic and is passivated against reoxidation (2). Throughout cleaning, Fluoroware^{TM} teflon vessels and CMOS-grade chemicals were used. We have consistently achieved reproducible results based on this cleaning.

Poorly prepared wafer lots can require additional treatment. When experimenting with a new batch of FZ(111) wafers, we obtained values in the range between 60 and 80 μs, which are very small for float-zone Si. We then re-cleaned the wafers and re-measured. The lifetime increased appreciably. A third cleaning yielded even a greater increase in lifetime. The cleaning process was repeated until the change in measured lifetime was minimal which usually occurred after the fourth cleaning. A schematic representation of our observations is shown in Figure 2. For every wafer batch, we optimize the cleaning process as discussed above.

Our standard clean was developed by variation of etching times. Changing the duration of the piranha etch and keeping the DHF etch time constant results in a six to eightfold increase in lifetime after four minutes of etching. We have noticed an increase in measured lifetime after three minutes of DHF etching, a modest increase after four minutes, and a decrease with five minutes of etching. The decrease in lifetime at long etching times is attributed to surface roughening with DHF exposure as demonstrated by Higashi *et al.* (3). The standard cleaning is a five-minute piranha etch and a four-minute DHF etch (Table 1).

HALOGEN PASSIVATION

We have reported in a previous publication that iodine and bromine can electrically passivate Si surfaces (4). In this paper, we report a comprehensive study of the stability of the iodine passivation. We have determined the iodine concen-

tration that produces the optimum passivation in methanol by dissolution of I_2 crystals of known mass in 50 ml of methanol. The silicon wafer was first cleaned and immersed in 48% HF for measurement. It was cleaned again and immersed in methanol. A watchglass was used to cover the beaker to prevent evaporation of the methanol solution. The iodine solution was added drop-wise and lifetime was measured *in situ* until the surface was saturated as indicated by an asymptotic lifetime value. Figure 3 shows the variation in measured lifetime with iodine molarity for both n- and p-type FZ-Si. We see from both graphs that lifetime increases linearly once iodine concentration reaches 4×10^{-5} M and remains constant beyond 5×10^{-4} M of I_2. This highest measured lifetime is 90% of the value in 48% HF solution.

We conducted a series of experiments on two different wafers to compare the passivation stability between iodine and hydrogen. This subject is of practical interest because of storage times during wafer processing. To measure the stability of H passivation, the sample was cleaned as described above and placed in concentrated HF for measurement. It was then removed from HF with teflon tweezers and placed on a Fabwipe directly over the measurement coil. The lifetime was then measured at specific time intervals. The first measurement was taken within one minute of transferring the wafer to the clean room air and the rest were taken at 5 minute intervals. The sample was cleaned again and placed in methanol (with a watchglass cover) for measurement. Iodine solution was then added drop-wise until the measurement saturated. The sample was then removed from solution using clean teflon tweezers, placed on a Fabwipe, and measured every 5 minutes. Results are shown in Figures 4 and 5. The n-FZ(111) of Figure 4 had a higher lifetime immediately after removal from the iodine solution. It took twice as long for the measured lifetime of the I-treated wafer to return to the expected value in air. In Figure 5, the p-FZ(100) wafer lifetime after iodine treatment decayed to an asymptotic value 50% higher than HF:air level. In surface recombination velocity (srv) terms, this difference corresponds to srv=394 cm/s and 998 cm/s in air for the I- and H-passivated surfaces, respectively. The iodine passivation yielded consistently higher lifetime values than hydrogen passivation at all times. The tendency for the surface to contaminate in air is relatively less for iodine-treated surfaces. It is well known that the hydrophobic H-terminated silicon surface is subject to fast carbon-hydride recontamination during subsequent handling in air (5,6).

SURFACE ROUGHNESS MONITORING

As the next generation of chips approaches minimum line-width dimensions of 0.3 μm, the gate oxide thickness of CMOS capacitors drops below 50 $\mathring{A}$. Silicon surfaces treated with aqueous HF solutions prior to the growth of gate oxides are rough on this nanometer scale. Flatter Si surfaces are required for uniformly thin oxides.

Higashi (3) and Pietsch (7) have reported that, unlike HF acid, ammonium fluoride, a highly buffered HF solution, produces atomically flat surfaces on Si(111) that are monohydride-terminated. Using both vacuum scanning tunneling microscopy and low-energy electron diffraction, they were able to obtain flat surfaces that are extremely well ordered exhibiting terraces which extend thousands of angstroms with an rms roughness substantially "smaller than 0.07 $\AA$". The formation of the terraces is a consequence of the anisotropic etching of highly basic solutions such as NH_4F.

Since DI water roughens Si surfaces (8), we have conducted an experiment to see whether surface roughness can be correlated to measured lifetime. A CZ-Si wafer was cleaned, and placed in 48% HF for minority carrier lifetime measurement. The wafer was then DI water rinsed for 5 min and placed in a fresh 48% HF solution for another RF-PCD measurement. The process was repeated many times and the data is summarized in Fig. 6. The lifetime decays with water rinsing. This result is attributed to the added active sites produced by the surface roughening by DI water.

Based on this experimental capability, we studied the application of RF-PCD as a surface roughness monitor for different cleans. N-type FZ Si(111) were cleaned with a five-minute piranha etch followed by four-minute immersion in the solution of interest: i.e. 500 ml of 50:1 HF; or 500 ml of 40% NH_4F; or 250 ml of 40% NH_4F with 250 ml of 50:1 HF. The wafer was then placed in 48% HF as a standard ambient for lifetime measurement. It should be noted here that 48% HF does not alter the surface morphology or the H termination implying that the HF itself does not etch the surface (9).

The lifetime results are shown in a histogram (Fig. 7). A significant increase in lifetime relative to DHF cleaning (from 435 μs to 560 μs) was observed with NH_4F etching. These values are quantitatively reproducible suggesting that the clean chemistry can yield an atomically identical interface! These results support the claim by Higashi that the smoothening of the surface is reversible (3). The state of the surface in blends of NH_4F and HF follows the rule of mixtures.

CONCLUSION

We have employed radio-frequency photoconductance decay spectroscopy as an *in situ* monitor of the silicon surface and cleaning effectiveness. The method is, in addition, an effective monitor of surface roughness on a nanometer scale.

We have shown that I-terminated Si(111) surface is more electronically stable than its hydrogen-terminated counterpart upon exposure to air in a clean room environment. The NH_4F treatment is a more effective solution than DHF based on

the use of surface recombination velocity as a measurement of clean effectiveness and surface roughness.

ACKNOWLEDGMENTS

This work was supported by the National Renewable Energy Laboratory, Golden, Colorado, under contract No. XD-2-11004-4 and the MIT Leaders For Manufacturing (LFM) program.

REFERENCES

1. H. Ubara, T. Imura, and A. Hiraki, Solid State Commun. **50**, 673 (1984).
2. D. Gräf, M. Grundner, R. Schulz, and L. Mühlhoff, J. Appl. Phys. **68**, 5155 (1990).
3. G. S. Higashi, R. S. Becker, Y. J. Chabal, and A. J. Becker, Appl. Phys. Lett. **58**, 1656 (1991).
4. H. M'saad, J. Michel, J. J. Lappe and L. C. Kimerling, submitted to the Journal of Electronic Materials.
5. T. Takahagi, I. Nagai, A. Ishitani, H. Kuroda, and Y. Nagasawa, J. Appl. Phys. **64**, 3516 (1988).
6. M. Tabe, Appl. Phys. Lett. **45**, 1073 (1984).
7. G. J. Pietsch, U. Köhler, and M. Henzler, J. Appl. Phys. **73** (10), 4797 (1993).
8. C. R. Barrett, MRS Bulletin, 3 (July 1993).
9. G. S. Higashi, Y. J. Chabal, G. W. Trucks, and Krishnan Raghavachari, Appl. Phys. Lett. **56**, 656 (1990).

Table 1: Wafer cleaning procedure before minority carrier lifetime measurement

1) 5 min piranha etch 3:1 H_2SO_4/H_2O_2
2) 15 sec DI water rinse.
3) 4 min 50:1 DI:HF etch.

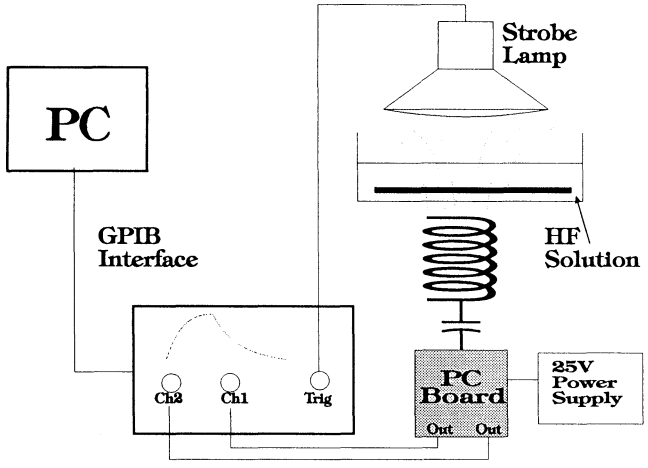


Fig. 1: Schematic of the radio-frequency photoconductance decay apparatus. The system is computer-controlled.

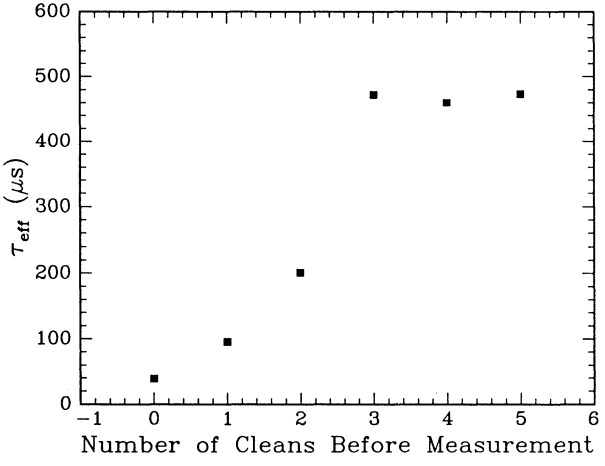


Fig. 2: Variation of measured lifetime with number of cleans for a contaminated phosphorous-doped float zone Si(111) to a resistivity of 2.66 Ω-cm. The wafer is 5 cm in diameter and 520 μm thick.

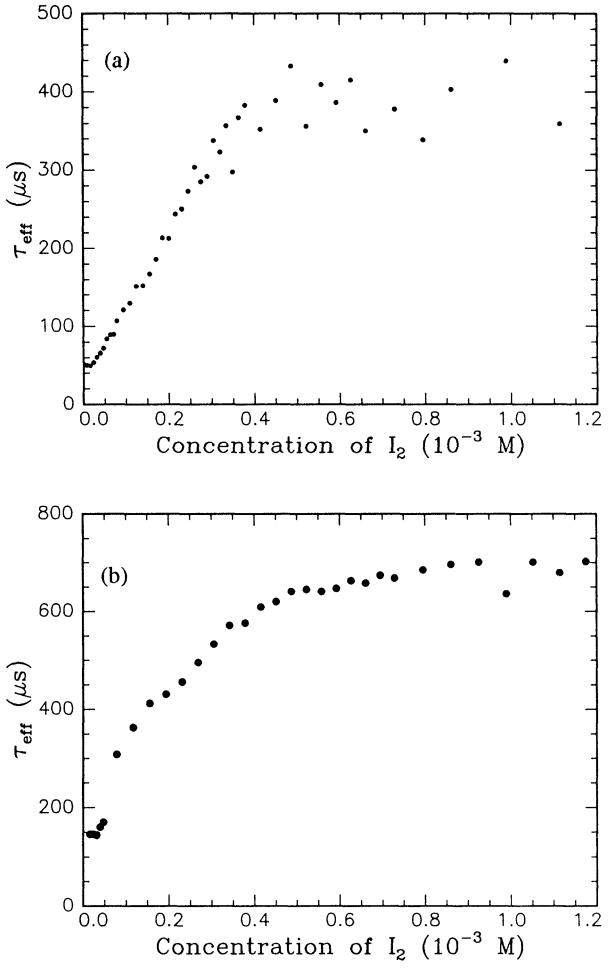


Fig. 3: The variation of lifetime with iodine concentration in methanol. The increase in lifetime is attributed to the passivation of the silicon surface with iodine. The surface recombination velocity is lowered as iodine bonds to the surface atoms. (a) n-type FZ Si(111) in non N_2-bubbled methanol and (b) p-type FZ-Si in N_2-bubbled methanol.

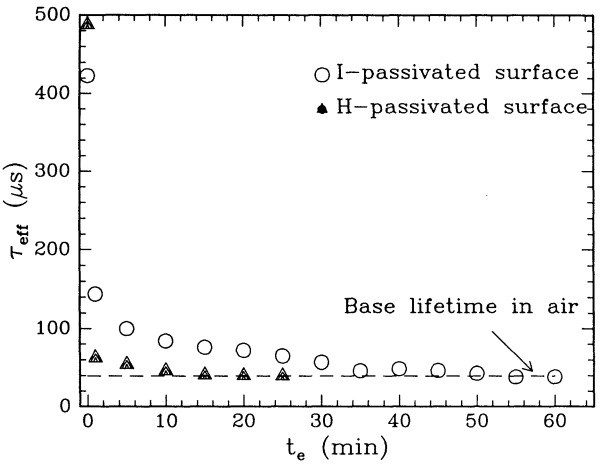


Fig. 4: Superior passivation stability of I vs. H. The wafer is float-zone n-Si(111). t_e is the time that the wafer was exposed to air.

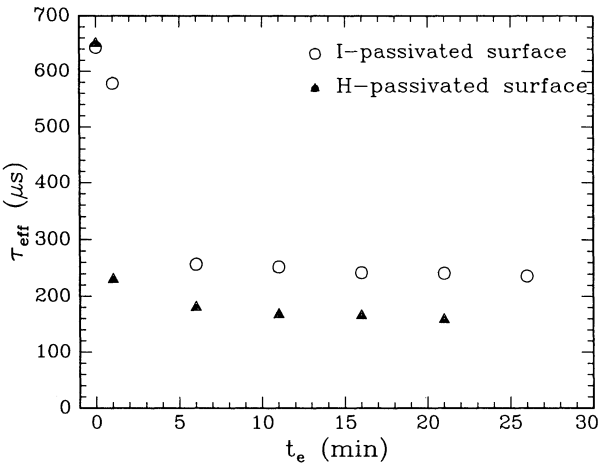


Fig. 5: Superior passivation stability of I vs. H. The wafer is float-zone p-Si(100). t_e is the time that the wafer was exposed to air.

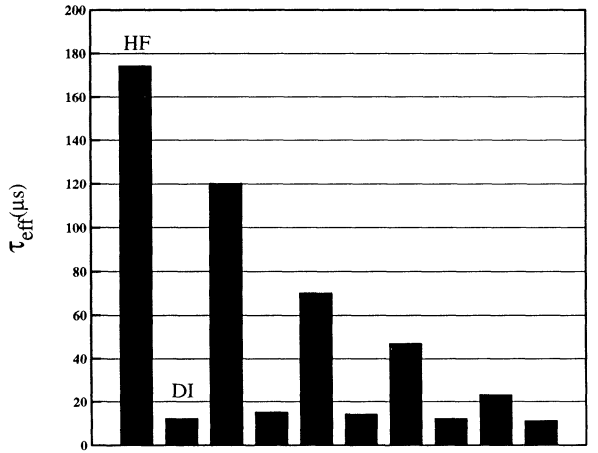


Fig. 6: Influence of sequential exposure between 48% HF and DI water on decay time for a Czochralski Si(100). The decrease in lifetime is attributed to the roughening action of DI water on Si surface. The wafer is rinsed in DI water for 5 minutes each time.

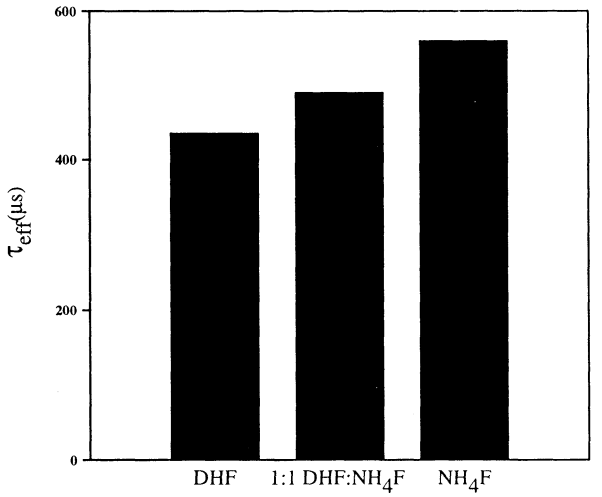


Fig. 7: Variation of lifetime with etch solution showing the correlation between surface roughness and measured lifetime.

METAL CONTAMINATION MONITORING

IN A SEMICONDUCTOR MANUFACTURING ENVIRONMENT

E. E. Fisch, R. H. Gaylord, S. A. Estes
IBM Microelectronics
Essex Junction, Vermont 05452

A new method for monitoring metal contamination introduced by silicon wafer cleaning equipment is presented. Developed and tested in a manufacturing environment, the method is based on diffusion-length mapping using the commercially available Electrolytic Metal Tracer (ELYMAT). Controlled comparisons between minority carrier diffusion length measurement results and surface metal concentrations measured by Total Reflection X-Ray Fluorescence Spectroscopy (TXRF) were carried-out to define optimal wafer processing. Experiments run on wafer cleaning tools in the manufacturing line verified sensitivity of the monitoring method to tool condition. The advantages of this monitoring method include reproducibility to better than 5%, minimal monitor processing, measurement simplicity, monitor reuse, and high-resolution wafer maps which often provide diagnostic clues to the origin of the metal contamination. The importance of identifying metal levels is illustrated with manufacturing examples.

INTRODUCTION

A method for monitoring metal contamination introduced by commercial silicon-wafer cleaning equipment has been developed and tested at IBM's semiconductor manufacturing facility in Essex Junction, Vermont. The widespread use of RCA-type[1] cleaning cycles throughout integrated circuit processing makes them a prudent target for improved monitoring and, ultimately, reduced metal levels. Many aspects of performance, such as particle levels and etch rates, are already well measured; metal levels have received much less attention. Certain metals (especially 3-D transition metals) have low room-temperature solubility and a high diffusion coefficient in silicon. These properties, in combination, can reduce carrier lifetimes, cause crystal damage, and degrade oxide integrity. Both the increasing number of steps required for ULSI device manufacturing, and the shrinking device dimensions have driven acceptable metal levels below 10^{10} atoms/cm^3 per process step. The vulnerability of new technologies to metal contamination has motivated commercial development of semi-automatic equipment to

detect trace metal levels. The monitoring method outlined in this paper is based on one of these -- the "Electrolytic Metal Tracer" (ELYMAT)[2].

The foundation of our metal monitoring plan is minority-carrier diffusion-length (L_d) wafer mapping. It is sensitive to metals like Fe, Mo, and Cr, which form bulk recombination centers in silicon. The average L_d provides a quantitative target which can be used for control limits, while the map provides a visual footprint of the contamination source. Figure 1 shows an "Elymap" of a wafer after cleaning in a spray-type chemical tool and illustrates the meaning of "footprint". In theory, the technique is well suited to tool monitoring. The purpose of this work was to develop a reproducible method for monitoring wet cleaning processes, including the anneal to drive the surface-metal contaminants into the silicon, which is required for the L_d measurement technique. This was accomplished in two steps: 1) to establish the effectiveness of the L_d measurement and drive-in on controlled wafers; and 2) to test the method for effectiveness, reproducibility, and ease of integration into a wafer-fabrication line.

A Brief Description of the ELYMAT Metal Test

The ELYMAT measurement has been described previously[2]. The measurement cell is shown schematically in Figure 2. The voltage bias shown, positive back side relative to the front, is appropriate for p-type silicon wafers in the back-side photocurrent (BPC) mode. The HF-filled cell has two purposes: it suppresses surface recombination by hydrogen passivation of the silicon surface, and creates a wide-area space charge region for free-carrier collection. The front side of the wafer is illuminated with a scanning 670 nm laser. Minority carriers are generated near that surface. Because surface recombination is eliminated, the carriers either recombine in the silicon bulk or are measured as BPC current (I_{BPC}) at the back space charge region. The diffusion length (L_d) is easily calculated from I_{BPC}[2]. The current is measured as a function of the scanning laser position, so a high-resolution L_d map is generated. The ELYMAT also has a front-side photocurrent mode (FPC). (Other monitoring work[3] has shown that the FPC photo-induced and dark currents are meaningful parameters, driven by the presence of Cu and Ni. In our monitoring, the FPC current was much less sensitive to the wafer cleaning processes than the BPC current, and will not be discussed here.)

In addition to the laser-induced photocurrents, there is a finite "dark" current (I_{dk}) that is measured with the bias on and without photogeneration. This dark current gives an average "generation rate" for the entire wafer and is sensitive to fast-diffusing metals like Ni and Cu that form near-surface precipitates. The ELYMAT detection limit for these metals has been estimated[3] to be less than 10^{10} atoms/cm^3. This average quality factor is measured each time a BPC ELYMAT scan is taken, but it cannot be mapped. Our measurements on processed monitor wafers showed that I_{dk} was either stable from tool to tool, or corroborated the diffusion-length data.

EQUIVALENT FE CONCENTRATION

Although the diffusion length is a physically meaningful quantity, it is not recognized as a tool's quality parameter. A busy manufacturing-tool owner is unlikely to respond to "a reduction in L_d". To make the importance of monitoring data more immediate, a calculation was developed to report the data in terms of a metal concentration. Diffusion-length reduction is attributed to a concentration of metal. Because L_d does not provide elemental identification, one metal (Fe) was chosen for the calculation. Other factors may well contribute to the final diffusion length. This possibility led to the use of the word "equivalent" in the final quality parameter's designation: equivalent Fe concentration (equ. Fe/cm^3). The details of the calculation are simple. First, it is assumed that any degradation in diffusion length is entirely due to the presence of Fe recombination centers. (This was found to be quantitatively valid for most wet cleans.) Next, the Elymat diffusion length is corrected slightly to correlate to surface photovoltage L_d's. It was found that

$$L_{d[SPV]} = L_{d[ELYMAT]} / 1.1 \qquad [1]$$

in the regime where both techniques are valid. Now, Zoth's Deep-Level Transient Spectroscopy (DLTS) Fe concentration/surface photovoltage L_d calibration curves[4] can be used to convert ELYMAT L_d's to an "equivalent Fe concentration":

$$\text{equ. Fe/cm}^3 = 10^{17} / (L_{d[ELYMAT]})^2 \qquad [2]$$

This equation provides the basis of the scheme of metal monitoring which we describe below.

OPTIMIZATION OF MONITOR PROCESSING

We intentionally contaminated standard eight-inch virgin silicon monitor wafers (<100>, 10 ohm-cm) with Fe for this study. The choice of Fe was partly motivated by the widespread use of stainless steel in silicon processing equipment. The elements Fe, Cu and Ni are all common metal contaminants, but Fe dominates for many processes. After an initial RCA-type clean, wafers were dipped half-way into an iron-spiked solution, rinsed thoroughly in deionized water and air-dried in a class 100 hood. The surface concentration was determined with Total Reflection X-Ray Fluorescence Spectroscopy (TXRF). The wafers were subsequently processed in one of three N_2-ambient, drive-in anneals:

(i) 650°C furnace anneal for 30 minutes

(ii) 1050°C furnace anneal for 30 minutes

(iii) 1100°C rapid thermal anneal (RTA) for 1 minute

L_d maps were measured on the ELYMAT. The bulk silicon Fe levels resulting from each anneal can be calculated from the diffusion length data using Equation [2] since, by design, Fe is the dominant contaminant. The anticipated bulk Fe contamination is calculated from the pre-anneal TXRF surface concentration data by assuming that both sides of the wafer are contaminated equally and that all of the surface metal is driven into in the bulk:

$$[\text{Fe atoms/cm}^3] = 2\,[\text{Fe atoms/cm}^2] \,/\, \text{wafer thickness} \qquad [3]$$

Large deviations of the equivalent Fe result from that indicated by this calculation are evidence that the given anneal did was not suitable. The data are summarized in Table 1.

High metal levels were detected on the control side of the wafer that received anneal (ii), suggesting that the high-temperature cycle in our monitor furnace evaporated residual metals from some other source (furnace walls, filler wafers)[5]. There was no evidence of cross-contamination when the other two anneals were used. The close correlation between ELYMAT and TXRF data for anneals (i) and (ii) indicates that either of these anneals could be used with good success. The 30-minute drive-in anneal at 650°C was chosen as the process of record for metal drive-in since the RTA anneal was logistically inconvenient for manufacturing. The 650°C temperature is high enough to allow metal to diffuse into the silicon, yet low enough to prevent contamination from other sources. This anneal also produced the clearest Elymap, as defined by the delineation between the control and Fe-dipped halves of the wafer.

The reproducibility of the monitor anneal scheme was tested by repeating anneal/measurement cycles on monitor wafers with different initial metal levels. When wafers were measured, annealed, and re-measured there was no statistically significant change in diffusion length. This repeatability implies that, using Equation [2], it is possible to determine the amount of equ. Fe/cm^3 added by a *single* clean cycle, even if the wafer has seen previous processing steps. To test the feasibility of subtractive data interpretation, two wafers were processed simultaneously through three clean/anneal cycles (wafer clean, 650°C anneal). The L_d's were measured before and after each cycle, converted to equ. Fe/cm^3, and subtracted to determine the amount of equ. Fe/cm3 added by the individual clean. The resulting data is shown in Figure 3; the two wafers registered comparable metal levels for each cleaning cycle.

ROUTINE METAL MONITORING

The measurements and assumptions described above form the basis for the manufacturing metal monitoring scheme which is presented in this section. Virgin P-silicon <100> wafers are used for monitors and the ELYMAT is used in BPC mode only. The process flow for the RCA-type clean is:

1. L_d pre-measurement
2. clean to be monitored
3. drive-in anneal
4. L_d measurement
5. repeat steps 2-4 repeated until L_d<200 μm

Raw L_d data is entered into a process-control program that calculates the equ. Fe/cm^3 added, plots it on a tool control chart, and flags the operator if the point exceeds an upper control limit. The limit is calculated for each tool according to standard statistical process control guidelines.

The wafer must be replaced when the metal levels are high enough to compromise the sensitivity of the technique. Repeatable L_d measurements for our configuration of the ELYMAT is about 130 μm, so the 200 μm limit is conservative. Handling damage can also impact the wafers after repeated measurements, although this is not generally a limitation. The number of permissible runs for a given wafer varies according to the level of metals added by the cleaning tool. We have cycled a single wafer as many as ten times. Of course, the wafer map becomes the composite of metal distributions from all previous processing steps when a monitor is reused. The financial advantages of reducing the number of raw wafers usually outweighs the overlay of information on the Elymap. When a tool problem is suspected, a virgin monitor can be run to obtain the unobstructed Elymap of the metal distribution.

The monitoring method outlined above clearly determines physical differences in cleaning tools. The sensitivity was illustrated when twelve monitors were processed, one through each of twelve chemical cleaning tools, and annealed in a single furnace. The data indicated extreme tool-to-tool variations (Figure 4). A subsequent inspection of each tool revealed that the differences correlated perfectly to delaminated spots on cover lids and/or to an older version of chemical distribution. Tool maintenance was then initiated to resolve the previously undetected problems.

In addition to illustrating that trace metal monitoring is *possible*, we must verify that it is *necessary* in order to justify the cost. This was accomplished by identifying low-metal cleans with this monitoring scheme and linking specific pre-cleans to 4 Mb DRAM device performance. Pre-clean tools were ranked according to the equ. Fe/cm^3 metal

level data. Our cleaning tools perform within reasonable limits, but variations in the typical amount of metal added by a particular tool were used to identify "good" and "bad" tools. This ranking was applied to evaluate the effect of metals in the two experiments below:

1. Five 4 Mb DRAM lots were dedicated to "good" pre-clean tools, and five lots were dedicated to "bad" pre-clean tools. The lots dedicated to "good" tools had consistently higher yield at electrical test.

2. A critical furnace pre-clean was identified and production lots were run randomly on any of eight cleaning tools. Electrical data recorded during eighty days was sorted according to pre-clean tool. High levels of gate-to-substrate shorts were found on the lots which ran through "bad" pre-clean tools.

CONCLUSIONS

One option for monitoring metal contamination on wet chemical wafer cleaning tools has been described. The monitoring technique is not only financially attractive and simple, but also effective. Although the ELYMAT measurement neither detects all metals, nor speciates the elements, it is a valuable monitoring tool. The ELYMAT data demonstrated a sensitivity to manufacturing cleaning-tool metal differences. The importance of identifying (and reducing) these metal levels in 4 Mb DRAM manufacturing was proven by correlating improved device performance to low-metal cleaning tools.

ACKNOWLEDGMENTS

John Coady, Frank Gelsdorf, Brian Lloyd, and Guenther Zoth and other members of the IBM metal contamination community have provided valuable advice and support. The work of many individuals from IBM Burlington's engineering, manufacturing, and testing areas was essential to this paper and is greatly appreciated.

REFERENCES

1. W. Kern and D. A. Puotinen, *RCA Review*, **31**, 187 (1970).

2. H. Föll, V. Lehmann, G. Zoth, F. Gelsdorf, and B. Gottinger, "Analytical Techniques for Semiconductor Materials and Process Characterization", B. O. Kolbeson, D. V. McCaughan, and W. Vandervorst, Editors, p. 44, **Vol. 90-11**, The Electrochemical Society, Pennington, NJ (1990).

3. W. Bergholz, D. Landsmann, P. Schauberger, and B. Schoepperl,"ECS Symposium on Crystalline Defects and Contamination: Their Impact and Control in Device Manufacturing", Grenoble, Sept. 17, 1993.

4. G. Zoth and W. Bergholz, *J. Appl. Phys.*, **67,** 6764 (1990).

5. P. Eichinger, J. Hage, D. Huber, and R. Falster, proceedings from SEMICON Southwest, Austin, Nov. 1992.

Table 1. Raw data and calculated iron concentrations in the silicon bulk of wafers intentionally contaminated with iron.

Anneal Temperature (°C)	Wafer Half	Raw Data		Calculated from Equ. (2) or (3)	
		TXRF Fe/cm^2	ELYMAT Ld (μm)	TXRF Fe/cm^3	ELYMAT eq Fe/cm^3
650	Control	DL	702	--	2.5×10^{11}
	Fe-dipped	5.3×10^{10}	330	1.4×10^{12}	1.2×10^{12}
1050	Control	DL	230	--	2.5×10^{12}
	Fe-dipped	5.1×10^{10}	180	1.4×10^{12}	4.0×10^{12}
1100	Control	DL	470	--	5.9×10^{11}
	Fe-dipped	4.5×10^{10}	260	1.2×10^{12}	1.9×10^{12}

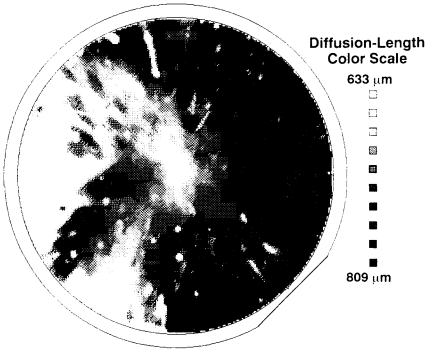


Figure 1. An ELYMAT diffusion-length map of a silicon wafer cleaned in a chemical spray tool and annealed at 650°C for 30 minutes. The effect of the spin-dry is clearly visible.

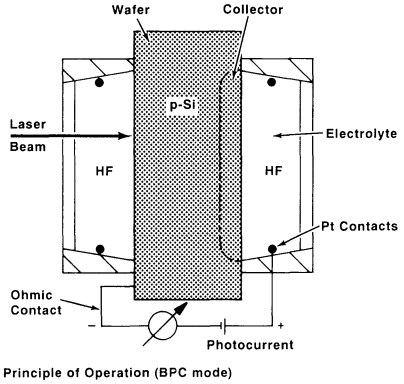


Figure 2. The ELYMAT measurement cell with voltage bias set to measure photo-induced current in BPC mode on a p-type silicon wafer.

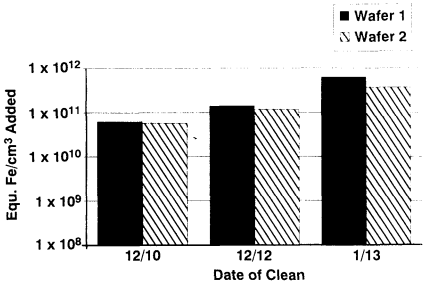


Figure 3. Monitor reuse investigated with two monitor wafers run through identical clean/anneal/measurement cycles.

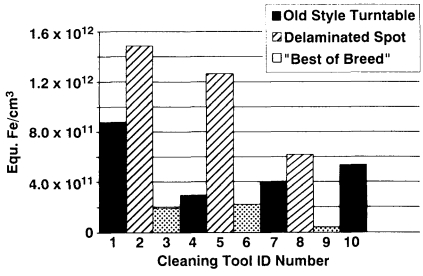


Figure 4. Baseline measurements of cleaning tools link average equivalent from concentrations with real tool differences.

CONTROL OF MANUFACTURING CLEANING OPERATIONS USING SURFACE PHOTOVOLTAGE TECHNIQUES

A.M. Hoff
Center for Microelectronics Research
University of South Florida
4202 E. Fowler Avenue, CMR-ENB252
Tampa, FL 33620-5350

E.J. Persson, J. Chacon, and B. DeSelms
AT&T Microelectronics
9333 South John Young Parkway
Orlando, FL 32819

The use of surface photovoltage (SPV) techniques to monitor and control spray processor cleaning in a manufacturing environment is described. The principle advantages of the SPV technique are that it provides short-loop feedback on process quality and that the fabrication of electronic test structures is not required. Results from the implementation of SPV monitoring techniques show that iron contamination may be tracked and controlled at a sensitivity level well below that required by ULSI technologies.

INTRODUCTION

Spray processor cleaning operations have become a standard in the IC industry. Spray tools are relatively automatic, wafers being cleaned are exposed only to fresh chemicals, and the tools add few particles. However, significant risk is associated with the use of these tools due to the potential for the introduction of molecular contamination or non-visible defects. Factors such as mis-programming, contaminated chemicals provided by bulk dispense or point of use storage systems, or failure of wetted surface passivation in the spray tool may all result in metallic contamination being introduced in one or many succeeding loads of wafers. In-line process monitoring reduces this risk and at the same time provides useful feedback needed for process optimization.

In most studies of issues related to metals and cleaning, surface analysis techniques or the fabrication of electrical structures have been used to obtain experimental responses. The SPV technique used in this work employs the carrier transport properties of the silicon wafer itself as a sensitive sensor to monitor process cleanliness. A capacitive probe is used to measure the spectral response of the wafer surface potential from which the diffusion length of minority carriers is determined. Iron and other metals may be detected through a modulation of their electrical activity produced by successive pairing and dissociation of the metal with dopant atoms in the crystal (1,2). In the case of iron, its association with boron may be broken with either thermal or optical energy (3). Measurement of minority carrier diffusion length, with the iron atoms paired with boron in the crystal, followed by a diffusion length measurement with the iron boron pairs separated provides a measure of iron concentration with a sensitivity approaching the $10^{8}cm^{-3}$ range.

Metals, iron in particular, have been shown to degrade thin oxide quality (4) and to contaminate surfaces to varying degrees as a function of cleaning chemistry (5). Robust processes must guard against inadvertent metal contamination of wafers especially prior to thermal processing. This work investigates issues related to the implementation of metal

monitoring in spray processors using SPV techniques. Monitor wafer quality, surface contamination, thermal drive-in treatments, timing to measurement, and sensitivity issues are addressed. A short loop process for sample preparation is described. Examples of the utility of the method toward identifying problems are given.

EXPERIMENTAL

SPV measurement of diffusion length, L, is performed under conditions which produce very low excitation. In this situation L may be related to the concentration of recombination centers in the silicon (3). In p-type silicon, and in this work, diffusion length measurements were used in conjunction with low temperature defect reactions between iron and boron to determine the quantity of iron in the material (1,3). To accomplish this, iron was first paired with boron by a one day storage at room temperature or by a short 80°C anneal (6). An initial diffusion length, L_i, was measured and then the wafer was heated to 200°C for ten minutes followed by a quench on a cold metal plate or in water. Rapid cooling is required to prevent formation of Fe-B pairs which are ten times less efficient as recombination centers compared to free interstitial iron, Fe_i (1). A final diffusion length, L_f, was measured and the concentration of iron, [Fe], was calculated from (1):

$$[Fe] = 1.1 \times 10^{16} [L_f^{-2} - L_i^{-2}] (cm^{-3}) \quad [1]$$

For low concentration measurements diffusion length values must be obtained with a reasonable degree of precision. The SPV instrument used in this work (CMS-IIIA) was an earlier model compared with current instruments (7) yet it should exhibit a measurement precision of five to ten percent. A gauge study was performed on silicon materials with varying diffusion length. Diffusion length measurements were performed on two p-type and one n-type wafers on a regular basis. This data will be used to establish the repeatability of the measurements in relation to nominal diffusion lengths.

Another possible source of variation is the starting silicon material. CZ material from five sources were measured at a minimum of nine points per wafer and [Fe] was calculated. Four inch samples from four vendors were measured as received with no additional processing. Two groups of 5" wafers were measured. The first, including 50 wafers, were cleaned and given a rapid thermal oxidation, RTO, at 1150°C for two minutes and then SPV measurements were performed. The second group was also measured, as in the case of the 4" material, without any processing.

To compare the effects of cleaning and thermal processes a few samples were given RTO or gate oxidation including Cl with and without a pre-thermal-treatment "RCA" clean (8). The wafers were then measured for Fe using thermal activation.

Studies were performed on spray processors in the manufacturing line. Wafers to be processed were first screened by cleaning followed by RTO as above. This oxidation process is adequate to uniformly contaminate silicon wafers with surface deposited Fe (1). These wafers were measured at 61 places before and after thermal Fe activation and cold plate quench for [Fe] determination. Nearly 250Å of oxide was formed by this process which was removed prior to processor screening. The wafers were then divided among spray processors for a standard pre-furnace clean, "RCA1": $HF:H_20$: "RCA2". After the clean process wafers were given RTO and then measured by SPV. Other wafers were identified and processed through selected spray processors without the pre-screening described above. Following the clean all wafers were given RTO and [Fe] was measured by SPV using thermal activation and water quench.

Finally a corroded thermocouple was discovered in an older model of spray processor by visual inspection. This was used to assess the surface/bulk contamination which would result from cleaning in that environment. Wafers were cleaned in another spray processor and in the contaminated tool. Then the wafers were given RTO and [Fe] was measured by SPV using thermal activation.

RESULTS AND DISCUSSION

The results of the instrument gauge study are shown in Fig. 1, Fig. 2, and Fig. 3. This data was collected over a few months time. Eleven hundred diffusion length measurements were taken on a nominal L=204μm p-type wafer and on an L=146μm n-type wafer. Nine hundred measurements were taken on an L=374μm p-type wafer. The standard deviations of these measurements were 2.35μm, 1.23μm, and 3.35μm respectively. Six sigma divided by twice the mean for each wafer resulted in values of 3.4%, 2.5%, and 2.7%. These results indicate an overall variation of 3% in the range of measured values at a given L. For L_i=350μm, this value implies a minimum [Fe] determined with this instrument would be roughly $5.4x10^{9}cm^{-3}$ (9). This value assumes Fe to be the dominant recombination center.

Fig. 4 depicts the results of the material comparisons. In the case of the A: 5"CZ data recall that this group was cleaned and given RTO before [Fe] determination. For the purposes of monitoring spray processors for contamination the four materials in the center of the figure are acceptable based on an estimation that $1x10^{11}cm^{-3}$ is a threshold value to maintain acceptable oxide defect levels in 0.5μm technologies (4). Optimization studies would require low [Fe] levels and the scatter in the data would imply that prescreening of all samples would be necessary.

Wafers which received no clean followed by RTO exhibited an iron level of $2x10^{13}cm^{-3}$. Those which were oxidized in a gate process averaged $4x10^{12}cm^{-3}$, a five times improvement. Wafers which were cleaned and given RTO or gate oxidation indicated [Fe] from 2 to $3x10^{11}cm^{-3}$. The latter is nearly a 100x improvement over the no clean RTO case. RTO was chosen as the contamination drive-in method over the furnace for speed reasons and since a cold wall system should minimize contamination provided by the thermal process. An estimate of the amount of Fe on the non-cleaned surface yields $1x10^{12}cm^{-2}$ which with RCA clean and oxidation is reduced to nearly $1x10^{10}cm^{-2}$. These results are consistent with TXRF comparisons between RCA1, RCA2, and no clean treatments. Surface iron resulting from RCA1 was determined to be 1 to $2x10^{12}cm^{-2}$, RCA2 resulted in no detectable surface Fe, and no clean resulted in Fe as high as $1.4x10^{12}cm^{-2}$. The TXRF data also predicted the result of mis-programming of a spray tool. An error had been made in the down loaded program to an older model of processor which called for two consecutive RCA1 steps rather than an RCA1 followed by RCA2. Wafers processed in this process exhibited [Fe] close to $1x10^{13}cm^{-3}$. The corroded thermocouple comparison resulted in an average value of [Fe] of $2x10^{10}cm^{-3}$ for the controls and 2 to $3x10^{12}cm^{-3}$ from the contaminated system indicating significant Fe contamination of wafer surfaces. Iron levels this high would produce post activation diffusion lengths shorter than 100μm.

Screening of the spray processor systems for [Fe], depicted in Fig. 5, showed that all systems were within tolerable levels for technologies in the range from 0.5μm to 1μm (4). Iron data shown are from wafers processed at the top and bottom of a cassette. The

average of the two is also shown. The results of maintenance on processor C are seen in the last case for that system.

Time series for six different spray processors are shown in Fig. 6 and Fig. 7. Data for older model systems are shown in Fig. 6. The system indicated by a diamond shows an out of control point above $10^{13}cm^{-3}$, somewhat higher than the corrosion case described above. Inspection of the system indicated a small scratch in the turntable passivation. Fig. 7 indicates that following initial excursions all three systems settled to a nominal range lower than $3x10^{11}cm^{-3}$. Some of the noise in Fig. 7 was determined to be related to monitor material L fluctuations. In this case [Fe] was estimated from final L measurement only. Isolated groups of wafers exhibited unusually low L values or regions with low L values. The majority of wafers exhibited L_i values greater than 350μm, but for occasional samples L_i could measure near 100μm. An iron reading of $1x10^{12}cm^{-3}$ is equivalent to 0.02PPB, which is well within most monitor wafer specifications. If the final goal is optimization or control of [Fe] to very low levels then pre-measurement is a necessity. However, depending on the technology level which must be controlled to, it should be possible to avoid pre-screening. In addition the contamination specification need not be reduced for most applications. Fig. 8 represents a tool which may be used to address the sensitivity level, [Fe] range, expected given a post activation L measurement over a range of L_i values. Equation [1] was used to generate this figure and Fe is assumed to be the principle contaminant (1). To use the figure enter at a value of L_f on the x axis. Proceed at this value of x toward increasing [Fe]. This line will intersect the L_i lines over a range of [Fe]. For example if L_f is 200μm, then [Fe] will range from $4.7x10^{10}cm^{-3}$ to $2x10^{11}cm^{-3}$ for $220\mu m<L_i<400\mu m$. Similarly, control to a maximum of $1x10^{11}cm^{-3}$ would require $L_f \geq 250\mu m$. A flag for a catastrophic event might be an L_f value below 100μm, independent of the initial L_i value. Such an event would necessitate further investigation just as an out of range electrical in-line monitor would. Further, although the pair dynamics following RTO are not well understood, this approach might also allow measurement immediately following RTO without a thermal activation to provide a quick indication of the maximum [Fe] present.

CONCLUSIONS

The results of this work show that SPV measurements of diffusion length may be used to monitor metal contamination in spray process cleaning systems. Cases representing catastrophic risk were detected quickly allowing corrective measures to be taken. In addition, surface concentrations of contaminant estimated from SPV measurements appear to correlate with TXRF surface analysis techniques. Sampling and control efforts may be tailored to the desired [Fe] threshold for a given technology and the range of [Fe] expected may be estimated from L values following thermal activation. Hence, an estimation of [Fe] contamination which may exist in a cleaning system may be obtained in roughly one hour including the clean process.

ACKNOWLEDGEMENTS

The authors wish to thank Tim Campbell of AT&T Orlando for TXRF contributions.

REFERENCES

1. G. Zoth and W. Bergholz, J. Appl. Phys., **67**, p. 6764 (1990).

2. K. Mishra, in Extended Abstracts/1992, **PV 92-2**, n426, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1992).

3. J. Lagowski, P. Edelman, A.M. Kontkiewicz, O. Milic, W. Henley, M. Dexter, L. Jastrzebski, and A.M. Hoff, accepted for publication in Applied Physics Letters.

4. W.B. Henley, L. Jastrzebski, and N.F. Haddad, MRS Symp., **262**, p. 993 (1992).

5. P. Gupta, Proceedings Microcontamination, p. 580 (1992).

6. J. Lagowski, P. Edelman, M. Dexter, and W. Henley, Semicond. Sci. Tech., **7**, p. A185 (1992).

7. Semiconductor Diagnostics, Inc., Tampa, FL.

8. W. Kern and D.A. Puotinen, RCA Rev., **31**,p. 187 (1970).

9. L. Jastrzebski, O. Milic, M. Dexter, J. Lagowski, D. DeBusk, K. Nauka, R. Witowski, M. Gordon, and E. Persson, in Cleaning Technology in Semiconductor Device Manufacturing, J. Ruzyllo and R.E. Novak Editors, **PV 92-12**, p. 294, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1992).

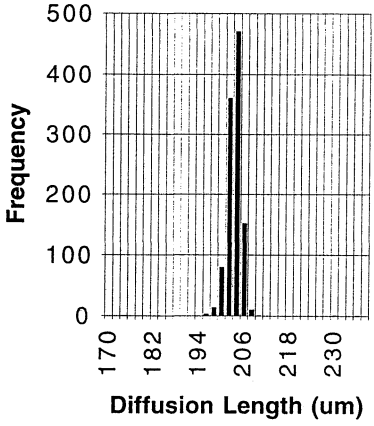


Fig. 1. L measurements of p-type wafer. L=204μm, N=1100, σ=2.35μm.

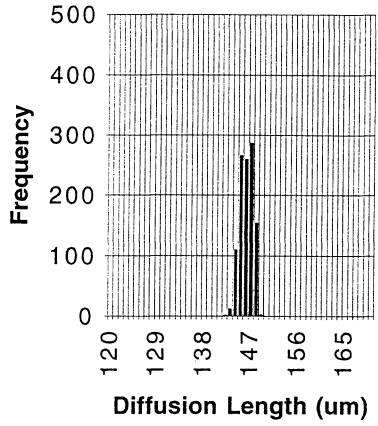


Fig. 2. L measurements of n-type wafer. L=146μm, N=1100, σ=1.23μm.

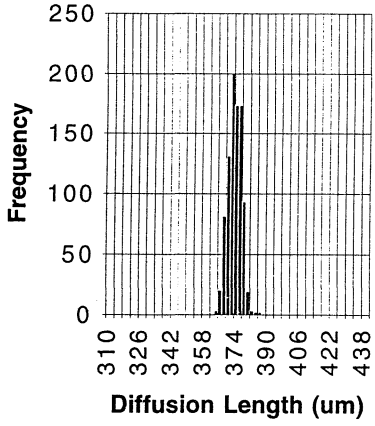


Fig. 3. L measurements of p-type wafer. L=374μm, N=900, σ=3.35μm.

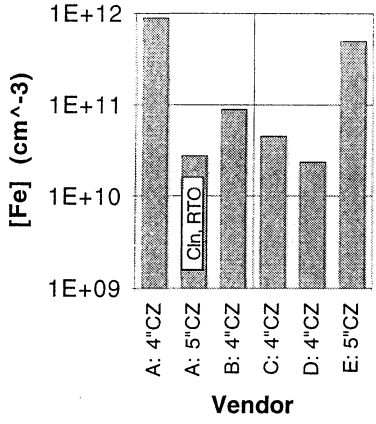


Fig. 4. [Fe] (cm^{-3}) obtained on wafers from different sources.

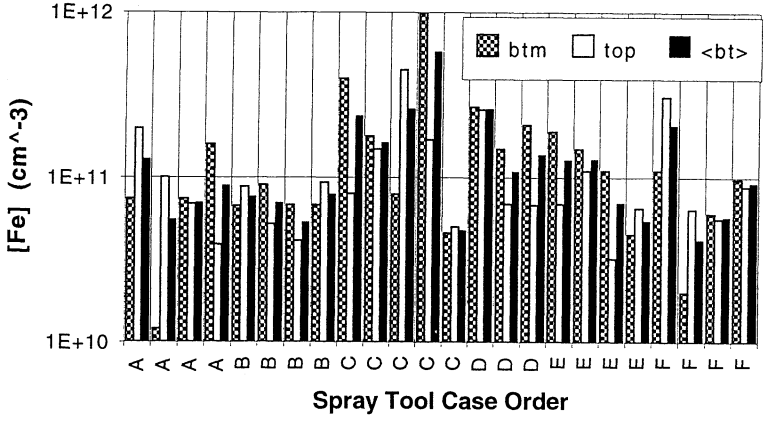


Fig. 5. Iron contamination levels obtained from various spray processors. Measurement order is indicated from left to right for each tool.

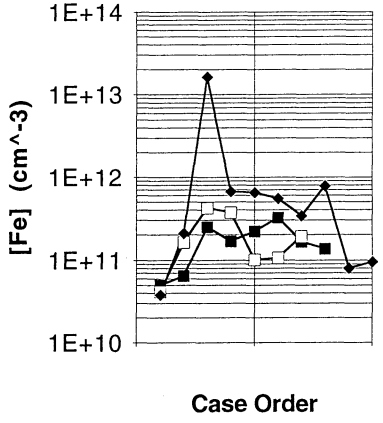


Fig. 6. [Fe] data from three older model processors. The 1E13 level shown was the result of a scratched rotor.

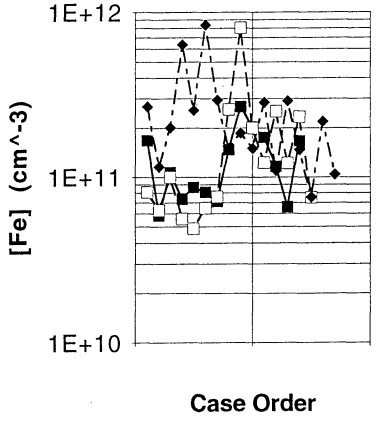


Fig. 7. [Fe] data from three spray processors. Levels settled to below 3E11 for all systems.

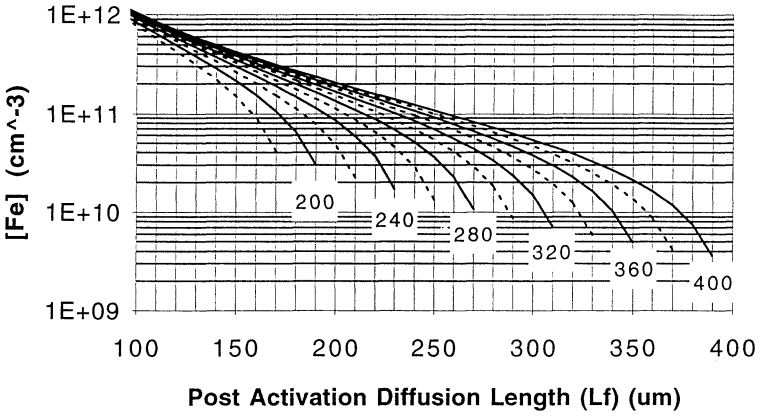


Fig. 8. Calculations of [Fe] versus post activation diffusion length value, L_f using Equ. [1]. Values of initial diffusion length are shown inset below their respective lines. Dashed lines are midpoint values, i.e. 400>380>360. Length values are in micrometers.

HEAVY METAL AND ORGANIC CLEANING EFFICIENCY OPTIMIZATION AND MONITORING FOR REAL-TIME, IN-LINE PROCESS CONTROL BY SURFACE PHOTOVOLTAGE

L. Jastrzebski and W. Henley
Center for Microelectronics Research
University of South Florida, 4202 Fowler Avenue, ENG 118
Tampa, FL 33620
D. DeBusk
National Semiconductor Corporation, South Portland, Maine
N. Haddad
IBM Corporation, Manassas, Virginia
J. Lowell and V. Wenner
Advanced Micro Devices, Austin, Texas
K. Nauka
Hewlett-Packard Company, Palo Alto, California
E. Persson
AT&T Microelectronics, Orlando, Florida

The surface photovoltage (SPV) method was used to optimize cleaning efficiency and to monitor, in-line, heavy metal contamination and charge during critical processing steps for Statistical Process Control (SPC). Examples of the optimization of various cleaning steps, effects of the purity of virgin and reused chemicals, and the surface topology on cleaning efficiency will be given together with examples of SPC monitoring of real problems in processing lines.

INTRODUCTION

The reduction of the gate oxide thickness with technology evolution requires the continuous reduction of heavy metal contamination levels.[1] The heavy metals precipitates formed during oxidations at silicon/SiO_2 interface[2-5] will cause localized high electric field regions which will result in formation of weak spots in the gate oxides leading to GOI[4-6] (gate oxide integrity) and reliability problems.[2] Fe is the most prevalent heavy metal contaminant during IC processing[1], and it has been shown that, to maintain the density of weak spots in the gate oxide caused by Fe precipitates below 1 per cm^2, the Fe contamination introduced during pre-gate cleaning and oxidation has to be reduced from 1 x 10^{13} cm^{-3} level for 200Å thick oxide (1 μm technology) to 8 x 10^{10} cm^{-3} level for 100Å thick oxide (0.35 μm technology). Capability to measure heavy metal contamination with sufficient sensitivity is required in order to optimize cleaning steps and for development of measurement procedures necessary for Statistical Process Control (SPC) of IC lines.

We used the SPV method[7] to measure heavy metal contamination after cleaning[8] and to monitor, in-line, heavy metal contamination and charge during critical processing steps for SPC. Examples of the optimization of various cleaning steps, the effect of purity of virgin and reused chemicals, and surface topology on cleaning efficiency will be given together with examples of SPC monitoring of real problems in processing lines.

EXPERIMENTAL APPROACH

SPV provides a means for non-contact, non-destructive, real-time monitoring of minority carrier lifetime, metallic contamination and surface charge in silicon wafers at various stages of processing.[8] The SPV measurements were performed with commercially available equipment[9] with sensitivity for Fe detection in the 10^8 cm^{-3} range[12] and were done on product as well as monitor wafers. This allowed evaluation of the effects from surface topology, characteristic for a given technology, on cleaning efficiency. The measurement of charge takes 0.6 sec/point and diffusion length 2 to 4 sec/point. For this work, we used p-type CZ medium oxygen content 10 Ωcm wafers.

During SPV measurement the potential barrier present at the silicon surface or silicon/dielectric interface is used as a detector for the photovoltaic effect which is sensed by a non-contact capacitive transducer. The diffusion length of minority carriers and surface recombination is determined independently from the spectral dependance of SPV signal.[6] Surface charge is obtained from the dependance of the SPV signal on light intensity.[7] Identification and determination of Fe and Cr concentrations (even in the presence of other recombination centers, e.g., oxygen precipitates) was measured via changes of lifetime during dissociation of Fe-B[11,12] and Cr-B[13] pairs. Due to the difference in pairing energies, characteristic for each heavy metal, pair dissociation can be selectively performed in-situ for each of the metals by a combination of light and temperature.[12]

Fe and Cr contamination, introduced during cleaning, were measured after a high-temperature treatment (a typical oxidation/annealing sequence used during IC processing or RTA at 1100°C for 5 minutes[8]) which was used to drive these metals left on the surface by cleaning into the bulk of the wafer. In the case of SPC of critical steps, e.g., gate or field oxidation, well drives, or oxidations involved in LDD formation and S/D implant anneals, the wafers were measured after oxidations/anneals. Surface recombination measurements after cleaning and prior to a high-temperature treatment provided information about Cu and Ni contamination.[8] Only surfaces with similar chemistry and similar surface charge values were compared. This measurement was especially useful to monitor contamination introduced during HF based cleaning operations, e.g., HF last cleans.

Al and Ca were determined from surface charge measurements after cleaning and prior to high-temperature operation. In addition to Ca or Al contamination, the measured charge depends on surface chemistry[15], e.g., change in degree of surface oxidation or hydrogenation which can change in time. Figures 1a and 1b show surface charge as a function of time after completion of SC-1 cleaning steps for various levels of Al and Ca contamination present in chemicals. The time is measured from the completion of wafer rinse. The step-like reduction of the surface charge at certain times corresponds to growth of monolayer of room temperature oxide[15] on the surface.

All charge measurements performed for SPC of Al and Ca contamination during SC-1 cleans were done between 5 to 30 minutes after completion of the rinse which eliminated the variable related to various degree of surface oxidation. The Al and Ca changes in the range of $1x10^{10}cm^{-2}$ result in surface charge as shown in Figures 2a and 2b which compares surface charge with surface Al and Ca concentration as measured by AAS.

In contrast to Fe and Cr measurements, the surface recombination and surface charge measurements provide information about the increase or reduction of the contamination level, but not quantitative data about the Al or Ca concentrations. These measurements were used successfully for SPC monitoring of contamination during SC-1 cleaning steps.

EXPERIMENTAL RESULTS

EFFECT OF SURFACE TOPOLOGY ON CLEANING EFFICIENCY

In order to evaluate the effect of pattern (surface topology) on cleaning efficiency, we compared the contamination after cleaning of blank monitor wafers and device wafers which went through typical steps involved in LDD formation (Figure 3). The pattern was formed using 0.75 μm technology. This data clearly shows Fe contamination level in the patterned wafers to be about one order of magnitude higher than in the blank monitor wafer. The comparison of the contamination introduced during various steps involved in LDD formation indicates that the difference occurs during ion implantation step followed by activation. This step involved photoresist operation, implantation, ashing and stripping of photoresist cleaning and annealing for implant activation. It has been identified that the surface topology of the product wafer has a detrimental effect of the cleaning of photoresist residue from the pattern corners which is the heavy metal contamination source during the high-temperature treatment used for implant activation. Although, due to proprietary nature, the details of circuit layout and details of the processing steps involved in LDD formation can not be discussed, this data clearly identifies the capability of the SPV technique to evaluate the effect from device pattern or cleaning efficiency.

COMPARISON OF CLEANS

The results of various experiments, designed to compare contamination levels for various cleans, are shown in Figures 4, 5, and 6. In all cases, the Fe was measured after drive-in performed during 900°C/20 min oxidation. Unless stated otherwise, all cleans were done on the silicon wafers as received from the silicon supplier. Surface Fe contamination in these wafers was around few x 10^{10} cm^{-2} level as measured by SPV after RTA drive-in[7] and TXRF.

Figure 4 compares various cleaning methods (MEGA grade chemicals were used). The best results were obtained for the modified SC-1, SC-2 cleaning (0.2:1.5 ratio of ammonia:H_2O_2:H_2O) which also gives the best surface roughness. Figure 7 compares the results of Fe contamination for SC-1, SC-2 cleaning for various shipments of SEMI grade and MEGA grade chemicals received over a period of four and a half months. Fe concentration level measured in some of these chemicals by ICPMS are also marked in Figure 5. Fe concentration in chemicals measured by ICPMS tracks very well with Fe introduced to wafers during these cleans. The results for MEGA grade chemicals are very consistent and do not vary substantially with successive shipments while the results obtained for SEMI grade chemicals depend very strongly on the shipment since the contamination level in SEMI grade chemicals could exhibit large fluctuations.

Figure 6 shows the effect of cleaning temperature on heavy metal contamination introduced during SC-1/SC-2 cleaning process. A decrease of temperature resulted in a reduction of Fe concentration (plating of heavy metals decreases with temperature), but also leads to an increase of positive charge in the oxide which is probably related to an increase of organic contaminant level. There is an optimum temperature for SC-1/SC-2 cleaning steps which is a trade-off between heavy metals and organic contamination.

In order to optimize usage of chemicals, the effect of heavy metal contamination build-up in wet chemical sinks during repetitive cleaning cycles without chemical replacement was investigated as a function of cleaning load (number of wafers cleaned). The silicon wafers (lots of 50 wafers) were initially coated with photoresist, the photoresist was ashed, piranha strip and wafers were cleaning using SC-1/SC-2 sequence and oxidized. The same wet chemicals were used for cleaning of subsequent lots. The

resulting Fe contamination as a function of cleaning cycles is shown in Figure 7. It is apparent that, for this cleaning configuration, the gradual build-up of heavy metals in SC-1/SC-2 bath which resulted in increasing wafer contamination started to take place after about three cleaning cycles (150 wafers). In this case, the replacement of chemicals after each cleaning cycle was not necessary.

APPLICATION OF SPV TO SPC OF CLEANS

Examples of application of SPV for SPC of pre-oxidation cleaning are shown in Figures 8 and 9. In both cases, the wafers were measured after oxidations. Split lot experiments showed that the heavy metal contamination from cleaning operations exceeded one order of magnitude heavy metals levels introduced from the furnace ambients, therefore, resulting variations in the heavy metal contamination level could be attributed to control and reproducibility of cleaning operations. Figure 8 shows the SPC chart for a wet chemical sink in which chemicals were not replaced after each cleaning cycle. Each point is an average of the 5-point Fe measurements on two wafers from a 50-wafer batch cleaned and oxidized at 900°C for 30 minutes. The allowable Fe contamination threshold for this particular technology is marked by the dashed line. Above this level, Fe has a detrimental effect on gate oxide integrity.[2] This SPC chart shows that about eight cleaning runs could be performed before the contamination in the liquid will build up to unacceptably high level and chemicals have to be replaced.

Figure 9 shows the SPC chart of contamination introduced by self-contained spray acid processor. Each point corresponds to one cleaning run (average value for two wafers, 9-point measurements on each wafer). The cracking of the protective coating of the turntable resulted in an unacceptable increase of the Fe contamination level. The replacement of the turntable rectified this problem. These results are similar to data reported by Hoff and co-workers from AT&T Microelectronics of Orlando.[10]

SPC OF Ca, Al AND Cu CONTAMINATION

Al, Ca and Cu contamination are monitored on the wafers after cleaning but prior to oxidation. The SPC chart of surface recombination used to monitor Cu contamination after HF dip ("HF last" cleaning sequence) is shown in Figure 10. Each point corresponds to average value of surface recombination measured on one wafer from a 25-wafer lot after rinse. In the case of the non-contaminated HF (stable line), Cu concentration was below detection level of TXRF (less than few x 10^{10} cm^{-2}). Values of Cu surface concentration measured by TXRF on wafers with high surface recombination are marked in Figure 12. It is clear that SPV measurements detect Cu contamination problems.

The SPC chart of charge used to monitor Al/Ca contamination left by SC-1 cleaning is shown in Figure 11. Each point corresponds to average value of charge measured on two wafers from a 25-wafer lot (9 points per wafer) after the rinse. The reduction of the charge indicates an increase of Al contamination resulting from contaminated chemicals at the point of use. The ICPMS analysis of the contaminated chemicals revealed Al concentration of 76ppb in the solution which introduced negative charge of the surface.

SUMMARY

The SPV method was used to optimize cleaning efficiency, study the effects of pattern and chemical purity on heavy metal contamination left during cleans. Fe contamination level introduced during cleaning was measured quantitatively following high temperature operation, oxidation or RTA used to drive in Fe into the bulk of the wafer.

Variations of Fe contamination levels in the wafers, on the level of 10^{10} cm^{-3} (which corresponds to 10^{9} cm^{-2} surface contamination), after cleaning were monitored as a function of changes of processing conditions. The Al, Ca and Cu contaminations were monitored through their effect on surface charge and surface recombination after completion of the rinse and prior to oxidation. These measurements were extremely useful in monitoring of "HF last" cleans. Since SPV measurements are fast, they do not require any wafer preparation and the performance of various cleaning stations can be easily evaluated and they can be used as a real-time monitor for SPC.

ACKNOWLEDGEMENTS

This work was supported by the Florida SRC/Sematech Center of Excellence (SCOE) program.

REFERENCES

1. L. Jastrzebski, W. Henley, C. Nuese, *Solid State Tech.*, **35(12)**, 27 (1992).
2. W. Henley, L. Jastrzebski, N. Haddad, *Proc. 1993 IEEE Rel. Phys. Symp.*, Atlanta,GA, p.22.
3. A. Ohsawa, K. Honda, R. Takizawa, T. Nakanishi, M. Aoki, *Semicon. Silicon 1990*, H.R. Huff editor, PV 90-7 p. 601 Electrochem. Society Softbound Proceedings Series, Pennington, NJ (1990).
4. K. Honda, A. Ohsawa, N. Toyokura, *Appl. Phys. Lett.*, **46**, 582 (1985).
5. R. Takizawa, T. Nakanishi, A. Ohsawa, *J. Appl. Phys.*, **62 (12)**, 4933 (1987).
6. W. Henley,L. Jastrzebski, *Proc. of the Mat. Res. Society*, San Fran., CA, Apr. 1992,Vol.262,p993..
7. J. Lagowski, P. Edelman, M. Dexter, W. Henley, *Semicon. Sci. Tech.*, **7**, A185 (1992).
8. L. Jastrzebski, O. Milic, M. Dexter, J. Lagowski, D. DeBusk, K. Nauka, R. Witowski, M. Gordon, E. Persson, *J. Electrochem. Society*, **140(4)**, 1152 (1993).
9. Model CMS III-A manufactured by Semiconductor Diagnostics, Inc. of Tampa, FL.
10. A. Hoff, et. al., this vol., *Proc. of the Electrochem. Soc. Meeting*, New Orleans,LA, Oct. 1993.
11. G. Zoth and W. Bergholz, *J. Appl. Phys.*, **67(11)**, 6764 (1990).
12. J. Lagowski, P. Edelman, A.M. Kontkiewicz, O. Milic, W. Henley, M. Dexter, L. Jastrzebski, A.M. Hoff, *Appl. Phys. Lett.*, in press.
13. K. Mishra and R. Falster, *Proc.of the Electrochem. Soc. Meeting*, Toronto, Canada, October 1992.
14. K. Mishra, in *Proceedings of the National Renewable Energy Laboratory 1992 Workshop*, Breckenridge, CO, August 1992.
15. H. Shimizu, C. Munakata, *Semicond. Sci. Tech.*, **6**, 756 (1991).

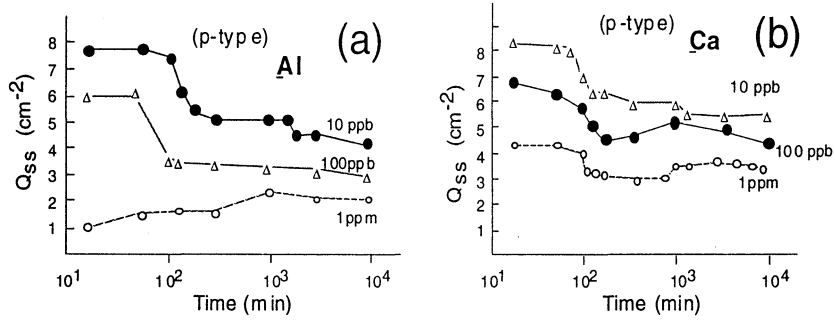


Figure 1: Surface charge as a function of exposure time to SC-1 solution contaminated with various levels of: (a) Al, (b) Ca

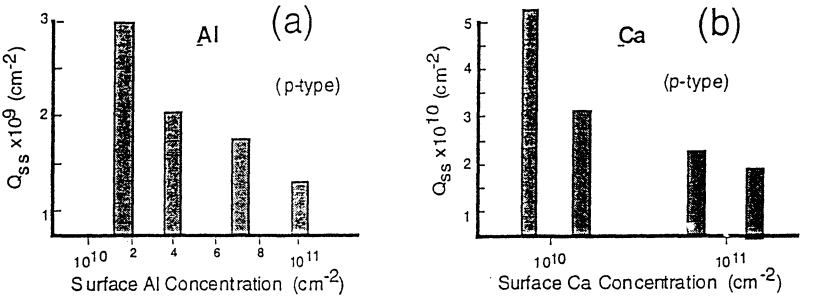


Figure 2: Surface charge measured measured on p-type wafers correlated to AAS measurements of: (a) surface Al concentration, and (b) surface Ca concentration

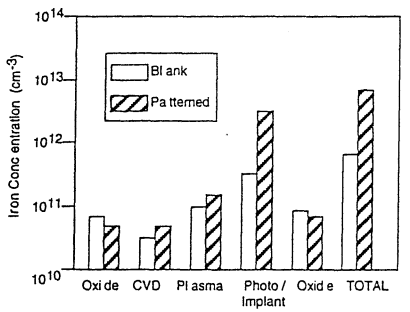


Figure 3: Fe contamination introduced by various process steps involved in LDD formation.

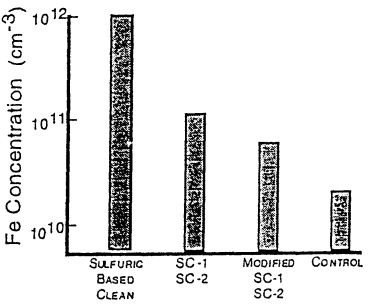


Figure 4: Fe contamination introduced by various cleaning chemistries. Note the control wafer had a starting iron concentration of $2x10^{10}$ cm^{-3}.

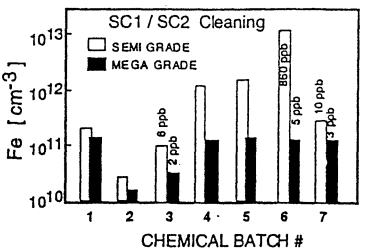


Figure 5: Fe contamination introduced during SC1/SC2 cleaning for different batches of SEMI and MEGA grade chemicals. Values of Fe in chemicals measured by ICPMS.

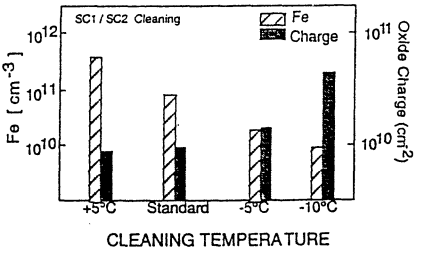


Figure 6: The effect of temperature on the SC1/SC2 cleaning. Decreasing the temperature reduces the Fe contamination, but also increases oxide charge (organic contaminates).

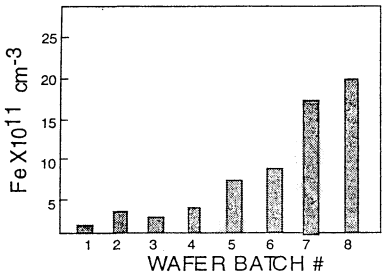


Figure 7: Build-up of heavy metals in cleaning sinks (SC1-SC2) as a function of cleaning cycles. (Chemicals not replaced)

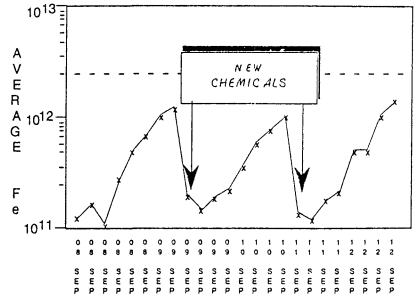


Figure 8: SPC chart of build up of heavy metals in wet sinks used for pre-oxidation cleaning, SC1-SC2. Horizontal line is upper allowable GOI contamination limit for this technology

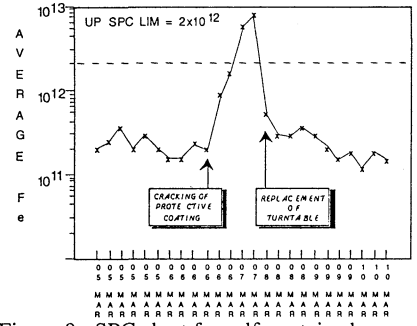


Figure 9: SPC chart for self-contained spray processor. Horizontal line is upper allowable GOI contamination limit for this technology.

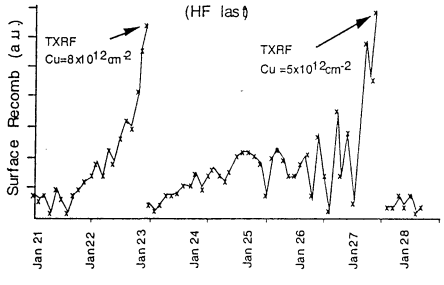


Figure 10: SPC chart of surface recombination values measured after HF last SC1-SC2. Copper surface contamination was measured by TXRF.

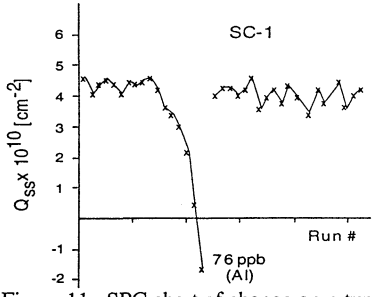


Figure 11: SPC chart of change on p-type silicon wafers measured after SC-1. Value of Al in SC-1 was measured during yield bust by ICPMS.

The Use of Chemical Sensors and Process Control Methods to Improve HF Chemical Etching of Silica

J. L. Dolcin, AT&T Microelectronics, 555 Union Blvd, Allentown, PA 18103

B. C. Chung, C. W. Draper, R. Ellis, Jr. and *A. Karp,* AT&T Engineering Research Center Princeton, NJ 08542-0900

We report on the use of HF chemical sensors to improve the control of both 100:1 and 15:1 HF etch baths used in a bipolar technology manufacturing line. The commercial HF sensor selected for this application is based on the induction of a current from a primary coil to a secondary coil when the coils are immersed in hydrofluoric acid-water solutions. The design of the sensor is such that only polymer surfaces are exposed to the acid. The output of the sensors are used in a Wet Chemical Advisor we have developed to improve the operator control of the etch baths. We present data demonstrating how the Advisor was used to understand the sources of both episodic and drift variations to the specified bath chemistries.

INTRODUCTION

The etching of silicon dioxide films by HF acid solutions is one of the most widely used wet chemical operations in semiconductor manufacturing. If the wet chemical benches are well designed, the baths properly made-up, the incoming oxide films of consistent quality and the operation of the etching process well controlled, then repeatable and uniform etching of the dielectric can be obtained from lot-to-lot, within the carrier from wafer position 1 through 25, and within the wafer across the surface area. Recent SEMATECH projects have set maximum nonuniformity targets of 2 % in a number of wet chemical and vapor-phase cleaning projects. From the vantage point of the manufacturing engineer two of the more significant variation sources are errors made by the shop people in making up baths and ineffective use of manually intensive process control procedures. Unfortunately, the consequences of these variances can show up as episodic losses of entire product lots as the result of significant over or under etching.

Recent advances in chemical sensor technologies suggested that there was a more effective way to control these wet chemical etch processes. We have used HF sensors to provide signals to a PC platform we call a Wet Chem Advisor. The software code we have developed for this advisor provides significant engineering, process analyst and shop operation advice. Bath make-up errors and manual process checks have nearly been eliminated. We will review some of the sources of variations in the device line

discovered as a result of our work and discuss how the Wet Chem Advisor has changed the methods used to control the etch processes and eliminated these sources of variation.

EXPERIMENTAL

The device fabrication line that this work was accomplished in is a rather mature 100 mm silicon wafer bipolar device cleanroom in AT&T's Allentown, PA manufacturing location. The line produces a mix of older bipolar devices and newer BEST (Bipolar Enhanced Self-Aligned Technology) BICMOS products (1,2). The same cleanroom manufactures wafers based on submicron and 10 micrometer lithographies. The conventional bipolar devices have no gate oxide, whereas the BEST device codes have nominally 15 nm gates. The cleanroom is very small by industry standards and space limitations play a critical roll in many decisions about wet chemical processing facilities. Our shop operators are expected to both move the product wafers and provide process control to the six front end HF facilities we utilize. Although more senior shop people are used to make-up baths on first shift Monday morning, our fab does not have full-time process analysts available to monitor and control the etch facilities. In normal operations our HF baths are made-up early on Monday mornings and dumped last shift on Friday.

The manual control of etch baths is based on the use of monitor wafer standards and etch rates derived from the etch deltas measured after a standard etch time in a given bath. The bath is spiked or diluted, and the iteration repeated until the etch rate specification is met. This had been the existing operator practice within this fab for some time, and was to be used when baths were first made-up as well for a process check throughout the five day work week during each of the three shifts. The shop recipe for first making up a bath is derived from knowledge of the bottled chemical concentrations and the total volume of the etch facility. The target concentration expressed in the standard volume ratio is either 15:1 or 100:1.

The HF wet decks are each fitted with continuous circulation and filtration of the HF. The recirculation flow is approximately 4 lpm and a typical total volume is 20 liters. The facilities have temperature controllers. Most of the HF wells do not have covers, and in those sinks that do have covers they are used intermittently. The sinks are all manually operated with digital timers that the operators set after checking the lot traveler with shop flow. Shop flow dictates the etch facility and etch time for the process step. During the course of this work two of the facilities were upgraded with robotic arms, and we will describe later how the Advisor is to be utilized to download the etch time to the robot arm.

The silicon dioxide used in the work described below is a dry thermal oxide grown at 900 degrees C in oxygen with 1% HCl or equivalent TCA. Oxide thicknesses

were measured with either a manual single point Rudolf or Nanospec ellipsometer or with an automated multipoint Prometrix Spectramap.

THE WET CHEM ADVISOR

The HF Wet Chem Advisor is a PC platform receiving input signals from two sensors located in each etch facility. For this particular bipolar application there are six facilities that have had the sensors installed. The sensors themselves are commercially available units: an HF sensor(3) and a temperature sensor(4). The HF sensor operates on the induction principle. An AC reference signal in a primary coil induces a signal in a secondary coil that is connected to the first coil by the conductivity of the HF solution. All the sensor components are completely enclosed in HF compatible polymer compounds. The output signal is 4-20 mA DC and serves as one input to the Wet Chem Advisor. The temperature sensor is a negative thermal coefficient thermistor. This type of sensor was selected for its excellent sensitivity over the normal room temperature operating range. It is easily implemented into the PC platform, as it requires only a 1 mA current loop from the PC's 5 volt bus. The various HF and temperature signals are input via a 16 channel multiplexed A/D converter. The source code for the Advisor is written in C and provides easy software access to the multiplexor hardware.

The software code has been designed to provide the manufacturing engineer and shop operation with simple to interpret and easy to implement advice. Table I summarizes these features.

Table I. HF Wet Chem Advisor Feature Summary

Optional Control Limits	The engineer has the option to set upper and lower HF concentration control limits around the target.
Operator Warning	An out of control situation is signalled to both the engineering station(the PC Advisor) and light post at the etch station.
Corrective Action	The Advisor calculates the quantity of water or HF required to bring the facility back to target and displays this for the operator and engineer.
Summary Status	The default screen on the PC summarizes the current status of all six facilities: HF concentration, etch rate, water to HF ratio, bath temperature and status relative to target specification.

The replacement of the labor intensive process control procedures with the Wet Chem Advisor is dependent on being able to demonstrate that the advisor is both accurate and reliable. We have developed algorithms to calculate, within the PC based Advisor, the etch rates of silica based upon sensor input for bath temperature and HF

concentration. The incorporation of temperature coefficients has improved the accuracy of the sensor beyond the commercial vendor's specifications. Figure 1 is a family of etch rate curves for a dry thermal oxide for HF concentrations between 0.5 and 4.5 weight percent, and between 16 and 34 degrees Celsius. It is readily evident that an error of 10 % in the HF concentration together with an error in the bath temperature control of 2 degrees Celsius can produce an etch rate that is >20 % from a target value. It may not be obvious, but the data also suggests that if the temperature is left uncontrolled, and it is not monitored as a process variable, then the set of concentrations and temperatures producing an electrical output at the sensor is not unique. Maintenance issues, feedback and control deficiencies and poor equipment performance all contribute to make it difficult to reliably control the etch bath temperature fluctuations to better than several degrees, and thus in our view accurate real time temperature input is required in order to insure the calculation of accurate current etch rates.

In order to evaluate the use of the Advisor within the manufacturing environment before committing to final design, and as a means to investigate the order of magnitude of relative sources of variation, a prototype Advisor system was installed in one 100:1 HF bath for a period of two weeks. The Advisor's output was not available to the shop operators and thus the archived data represents a reasonable description of the "before" standard sources of variation. Figure 2 presents a subset of the data collected in that evaluation. The bath target in terms of weight percent HF is 0.58. The trace in the figure is the bath concentration as determined by the Advisor and stored in the PC. Nine data points taken every 3 minute period are averaged to create the trace in the figure. The curve in this figure starts on the last day of the first week, bridges the weekend when the bath is dumped, comes up again when the bath is mixed on Monday morning by the operator, and covers the entire second week. The bath is at the target HF concentration and target etch rate as determined by oxide thickness delta measurements at the start of the trace on the left hand side of the figure. As water evaporates from the bath the HF concentration drifts up. The slope of this evaporation effect is fairly constant, as one would expect for an environment with a somewhat controlled temperature and relative humidity. The downward spikes in the trace indicate the effort of the shop operators to drive the bath back into specification through semi-regular additions of 200:1 HF. As mentioned above the Advisor display functions were not available to the operators and so this trace provides a history of the "normal" operator procedures and a measure of this procedure's relative effectiveness. It is clear from the concentration prepared in the bath make-up on Monday that operator error in mixing the chemicals can be a major source of episodic variation. On the second day of week two the Advisor was used by engineering to bring the bath back into specification and the oxide thickness etch delta was determined to be on target. Over the balance of the second week the impact of both evaporation and operator spiking can be seen.

VARIATION SOURCES

There are many sources of variation in the wet chemical etching of dielectric silicon dioxide thin films. These variations manifest themselves as nonuniformities in lot-to-lot, wafer-to-wafer and within wafer etch deltas. The source of the variance generally falls into one of three categories: [1] inherent oxide quality, [2] changes in the state of the wet chemical environment providing the etch medium, or [3] plain operator error. We consider operator errors that impact the bath itself as type two, and these the Advisor can detect, remedy and eliminate. Other than installing robotic arms over the critical etch tanks, there is little that can be done to insure that the operator is at the sink when the timer sounds in a manually intensive production environment.

It is generally thought that the thermal oxides produced in furnaces equipped with computer controlled mass flow controllers and sophisticated thermal ramping programs are of very high quality, possessing uniform properties across the wafer, from wafer-to-wafer and from lot-to-lot. For this reason we expect the variation associated with the oxide thin films to be small compared with some of the variances associated with the wet chemical etching. Figure 3 presents some data (5) which helps to quantify the within wafer and wafer-to-wafer uniformity of etched thermal oxides. Thermal oxide wafers obtained from seven different AT&T semiconductor device fabrication lines were etched in the same bath at the same time. Before and after oxide thickness measurements on the same Prometrix instrument assured minimal variations other than the inherent differences of the oxides themselves. This data suggests that although the thermal oxidation furnace programs are essentially the same from location to location, the thermal oxides produced are not identical in their response to HF etching. All locations have within wafer % standard deviations below 5 %. Some locations have exceptionally uniform values. The bipolar fab is the data at 2 %. We can conclude from this type of data, and independent electrical test data that qualifies the gate oxide in our BEST devices, that the silicon dioxide films themselves do not represent one of the more important sources of variation relative to others.

The trial described above in Figure 2 helped to provide some relative magnitude on the sources of variation that we certainly appreciated prior to the two week study. As we started to install the sensors and use them as individual facilities prior to wiring them into the Advisor network, we learned about other more subtle sources of variation. A complete listing and discussion would be beyond the scope and page limits associated with this proceedings type manuscript, and so we have opted instead to touch upon some of the more important sources of variation. These are summarized in Table II. They are by no means unique to this bipolar device line.

Table II. Sources of Variation in Etching Silicon Dioxide Thin Films in HF Baths	
Wrong initial bath concentration	Operators take liberties with the precision of the volumetric measurements. Residual acid (if the bath was not thoroughly rinsed when drained) or residual water (if it was rinsed out) trapped in plumbing that does not drain impacts the accuracy of the make-up recipe. No etch rate check or insufficient statistics in qualifying a fresh bath.
Normal drift of concentration from target	Selective evaporation of water from the binary mixture. The use of hand gun sprays.
Changes in total volume	Evaporation and drag out reduce level in the overflow reservoir. An effective process control based on spiking needs a consistent total volume.
Ineffective process check	No etch rate check because of demands for operator's time. Errors in performing the process check. Insufficient statistics.
Wafer storage issues	No sulfuric acid-hydrogen peroxide preclean for organics removal.

To place some of these variations in perspective with the 2 % associated with the inherent quality of the oxide described above, we can state that the 12 % error in bath make-up in Figure 2 has been found on occasion to approach 20 %, although these are clearly episodic instances and were remedied with operator retraining. The daily drift rate in Figure 2 can be used to estimate an evaporation effect on the order of 5 % per day, even with the "before" manual spiking practice.

ADVISOR METHODOLOGY

The Wet Chem Advisor approach is very simple and straightforward. Provide an in-line, simple to use and interpret, exception-based alarming, process monitoring system. In our approach we have permanently placed sensors in each of the bath's HF recirculation loops assuring continuous in-line sampling. An alternative portable dip-stick sampling approach is possible, but in our manufacturing environment this would have simply added to the manually intensive operator/engineer work load instead

of reducing it. "Two levels" of status information are calculated and displayed. For the engineer, process analyst or layout operator the multifacility summary display at the Advisor's PC provides a single source for all the real time data being acquired and for all the derived parameters of interest. For the shop operators the light post at the etch facility provides a visual "go, no go" indicator. They can readily ascertain the bench status even from other nearby facilities where they frequently have to split their work load. We have considered the use of a smaller alphanumeric display at each etch facility to duplicate the "advice" line of the Advisor so that operators do not have to physically walk to the Advisor to obtain the spiking guidance. The fab is so small though that we are going to revisit this feature at a future date after the operators have had sufficient experience with the system. In this way they can provide their collective input for practical improvements. The light post is illuminated red when the concentration and temperature conditions causes the etch rate to move beyond the control limits set by engineering for that facility. Since the entire Advisor system is presently undergoing prove-in these control limits have yet to be established. Several months worth of sensor data and derived bath parameters are continuously stored in the Advisor. This data can be used as input into commercial process control statistical packages, and part of our initial evaluation will be to work with the production and quality assurance engineers to select a single statistics package that best meets the collective present and future requirements. Statistical packages are also available within high level shop flow and product tracking systems. Within AT&T, Processing Information Exchange (PIX) information management systems (6) allow engineers a single point of access to data from the cleanroom operations, electrical testing and final chip probe. As a result of interconnecting the shop flow system with the Advisor to server the needs of the robotic etch facilities the gateway to the PIX system is also established. How the data can best be used to provide historical moving averages, ranges or cumulative sum deviations from the mean is yet to be determined.

With the incorporation of robotic arms at two etch facilities the Advisor's functional responsibility also includes the element of control. Although not yet implemented the planned approach for using the Advisor's information to control the etch process is as follows: The shop flow system queried by the operator will both direct the operator to a robotic sink and simultaneously download, through the Advisor, the information needed to prepare the robot for the manual start. The operator activates the robot after loading of the cassette(s). The etch time downloaded into the robot will be calculated by the Advisor based on current conditions instead of being a fixed etch time as presently used with the sink timers. We estimate that for a bath which is roughly 10 % off the target this would add or reduce a standard 5 minute etch cycle by at most 30 seconds. Such a control strategy is easily implemented into a robotic system, but in our view would prove counterproductive for manually operated sinks, even if the varying etch times were downloaded to the sink timers from shop flow.

SUMMARY

We have presented data demonstrating how the Advisor was used to understand the sources of both episodic and drift variations to the specified bath chemistries. We have designed an exception-based advise and control strategy built into a PC platform that uses a relatively simple software code to provide real time information in a factory compatible, simple to use format.

REFERENCES

1. Moerschel, K. G., et. al., Semi. Internat., 13 (11), 73 (1990).
2. Moerschel, K.G., et. al., Proceed. IEEE 1990 Custom Intergrated Circuits Conf., May 13-16, 1990, Boston, MA, paper 18.3.1.
3. Hydrofluoric Acid Monitor, Model CM-110, Horiba, Ltd. Kyoto, Japan.
4. Series 400 Type Thermistor, Model ON-401-DP, Omega Products, Stamford, CT.
5. Anyanwu, V.E., Draper, C.W., Eisenberg, J.H. and Evans, J., Multi-location Silicon Dioxide Thin Film Etch Uniformity Study, unpublished data.
6. Muething, K. A. and Parry R., Integrated Access to Semiconductor Manufacturing Data, presented at AUTOFACT '92, Detroit, MI, Nov. 10-12, 1992.

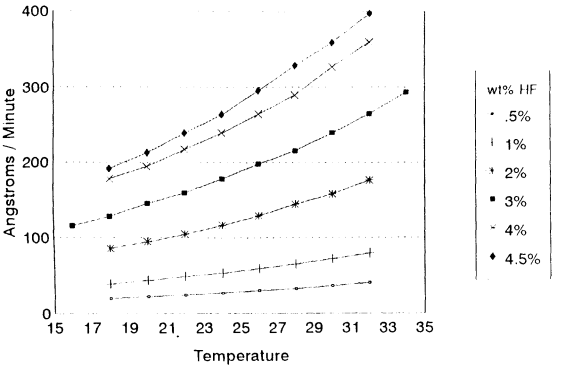


Figure 1. Etch rates of thermal oxide as a function of both HF concentration and bath temperature.

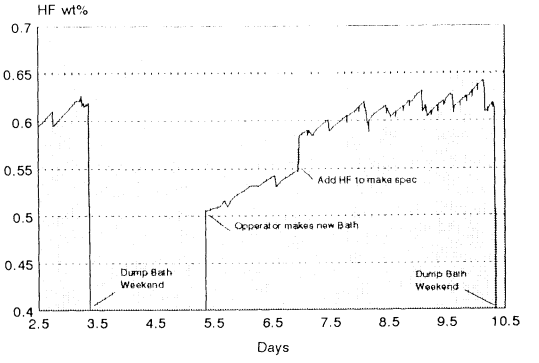


Figure 2. Beta-site trial for Wet Chem Advisor in a 100:1 HF facility in a bipolar manufacturing line.

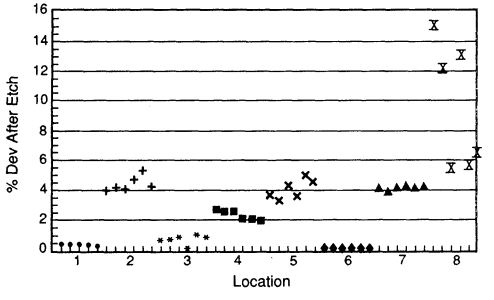


Figure 3. Etch rate data comparison of within wafer nonuniformities for 100:1 HF sink for thermal oxides from 8 different fabs.

AFM OBSERVATION OF Si(100) SURFACE AFTER HYDROGEN ANNEALING AND WET CHEMICAL PROCESSING

Y.Yanase, H.Horie, Y.Oka, M.Sano, S.Sumita and T.Shigematsu

Sumitomo Sitix Corp., Silicon Technology Center
Kohoku, Kishima-gun, Saga 849-05, Japan

Hydrogen gas plays an important role in the epitaxial growth process, acting as both a high temperature pre-cleaning ambient and the carrier gas during epitaxial growth. Effect of hydrogen (H_2) on the morphology and micro-roughness of Si(100) surface was investigated using AFM (atomic force microscopy). The surface after H_2 annealing showed a periodic terrace and step structure reflecting the double-domain (2x1+1x2) reconstructed structure. This structure was maintained even after subsequent HCl vapor etching and epitaxial layer deposition in the Si epitaxial process. H_2 annealed Si wafers were used as a reference in the evaluation of the change in the morphology and the micro-roughness of the Si surface caused by the wet chemical process SC-1 cleaning ($NH_4OH/H_2O_2/H_2O$). It was found that although the micro-roughness on the terrace increase with SC-1 cleaning, the periodic step and the terrace structure are preserved after the SC-1 cleaning. This result shows that the wet chemicals react in layer by layer manner, and that the etching sites exist not only at the step edge, but also at the terrace.

INTRODUCTION

Along with the device size miniaturization in VLSI/ULSI's toward sub-half-micron level, the effect of surface micro-structure or of so-called micro-roughness is expected to become critical to device reliability as well as to manufacturing yield.

There have been various basic studies on the structure of silicon surface, mainly on clean Si(111) surface, using reflection high energy electron diffraction (RHEED) (1), low energy electron diffraction (LEED), transmission electron microscopy and diffraction (TEM-TED) (2) and reflection electron microscopy (REM) (3).

By using scanning tunneling microscopy (STM) (4), atomic images of a cleaned Si(111)-7x7 (5) and (100)-2x1 (6) reconstructed structure were observed under ultra high vacuum (UHV-STM).

As compared to these techniques, atomic force microscopy (AFM) (7), which utilizes a fine needle closely placed to the surface to be observed in controlling the atomic force between the needle and the surface, can observe surface micro-roughness more directly, and can be applied to non-electro-conductive materials. Observation of atomic step structure was reported by several researchers (8).

However, most of these surface observation was done under UHV, and the surface

was pre-cleaned with wet chemical treatment (9,10) and subsequent high temperature thermal etching in vacuum environment (11,12). In other words, the surface is far different from actual condition to be applied to ULSI manufacturing.

Izunome et al. (13) reported periodic step and terrace formation on Si(100) surfaces after silicon epitaxial growth observed by AFM in air without pre treatment. They found that this periodic structure, with a double atomic layer step and terrace, was formed during the epitaxial layer growth depending on the mis-orientation angle from the [100] direction.

In this work, we have investigated Si wafer surface that has been subjected to vapor phase epitaxial growth process, which consists of hydrogen annealing, HCl vapor etcing at temperature ranging 700-1160℃, and subsequent epitaxial layer deposition, by using an AFM. We have also investigated the effect of mis-orientation, effect of the annealing temperature, and effect of subsequent wet chemical treatment, i.e., cleaning with $NH_4OH/H_2O_2/H_2O$ mixture (14,15), on the surface morphology or surface structure of silicon wafers.

EXPERIMENTAL RESULTS AND DISCUSSION

Periodic step and terrace formation during epitaxial growth process

Firstly, we investigated the periodic step and terrace formation on Si(100) vicinal surfaces during Si epitaxial growth process. The following three types of samples were prepared using CZ-grown 150 mm diameter (100) oriented P^+ wafers (B-doped, 20 m $\Omega \cdot$cm) as the starting material. The mis-orientation angle was about 0.1° towards the $[01\bar{1}]$ direction as measured by an X-ray diffractometer.

(a) A P-type epitaxial layar (10 μ m thick, 10 $\Omega \cdot$cm) was grown on top of the P^+ wafer with a conventional vertical reactor using $SiHCl_3$ and H_2 under atmospheric pressure at about 1100℃, while B_2H_6 was used as the dopant gas. The heat treatment process is shown in the solid line in Fig. 1.

(b) The P^+ wafer was subjected to HCl vapor etching and cooled down as shown by the dotted line in Fig. 1, without depositing the epitaxial layer.

(c) The P^+ wafer was subjected to the same heat treatment as (b) but the gas ambient was only H_2 and no HCl gas was used.

the surface structure of these three samples was investigated under atmospheric air ambient using an AFM with a NanoScope II (Digital Instruments). Conventional pyramidal shaped Si_3N_4 cantilever tips were used and their spring constant was 0.58N/m. The atomic force was less than 1nN and the observation area was 2x2 μ m^2 at the center of the wafer.

The AFM images observed in these samples are shown in Fig.2. The periodic step and terrace configuration were observed in (a), (b) and (c). These results indicate that the periodic step and terrace configuration is formed during the H_2 annealing process as well as during epitaxial growth. We believe that the formation is attributable to H_2 thermal etching and reconstruction.

Effect of mis-orientation on the surface morphology of H_2 annealed wafer surface

The relation between the mis-orientation angle and the surface morphology of H_2 annealed wafer surface was investigated for various mis-orientation angles. In this measurement, Si(100) wafers with a resistivity of 40 Ω·cm and mis-orientation angles of less than 0.05° to 2.0° towards the [01$\bar{1}$] direction, and Si(111) wafers with a resistivity of 10 Ω·cm with mis-orientation angles of less than 0.1° towards the [11$\bar{2}$] direction were used. These wafers were annealed at 1100℃ in H_2 for 10min before AFM observation.

The AFM image observed in the H_2 annealed Si(100) surface with a mis-orientation angle less than 0.05° is shown in Fig.3. The periodic step formation and two directional step edges alternating with each other, were seen. Island and defects were observed with the same direction as the step edges. The step height was measured to be about 0.14nm, which is in good agreement with that of a mono-atomic step height. This structure reflects that of the atomic images of the clean Si(100) surfaces with the double-domain (2x1+1x2) reconstruction observed using UHV-STM (6).

Fig.4(a)-(f) show AFM images of the H_2 annealed samples with various mis-orientation angles. In the AFM image of samples with mis-orientation angles of 0.1° and greater towards the [01$\bar{1}$] direction, vertical stripes with an S_A composition were observed towards the [011] direction. Chadi (16) labeled these downward steps running parallel to the dimer rows as S_A and running perpendicular to the dimer rows as S_B. However, S_B steps were observed between the S_A steps as saw teeth like steps. This result indicates that the surface of Si(100) after H_2 annealing is composed of mono-atomic steps and flat terraces on a atomic level.

We also investigated the Si(111) surface after H_2 annealing and found a step height of 0.31nm indicating the surface composition to be that of a mono layer, as shown in Fig.5. In the Si(111) case, however, the terrace is flatter than the Si(100) terrace.

Effect of H_2 annealing temperature

The relation between the H_2 annealing temperature and the surface structure was investigated using the samples with mis-orientation angles of less than 0.05° . The H_2 annealing temperature was from 700 to 1160℃ for 10min. These samples were dipped in a 5%HF solution for 1min to remove the native oxide before H_2 annealing.

Fig.6 shows the AFM images for the samples H_2 annealed at various annealing temperatures. For samples annealed at temperatures of 800℃ or lower, the AFM image, shown in Fig.6(a),was similar to that of a mirror-polished wafer prior to H_2 annealing. In the case of 900℃ annealed sample, shown in Fig.6(b), many pits with depths of about 10nm were observed.

During H_2 annealing at 900℃ the native oxide layer that are present on the surface will be removed by H_2. However it is believed that the removal of this native oxide is imperfect at temperatures of about 900℃. Therefore, some areas of bare silicon will appear before others. Due to small amount of moisture and oxygen that are present in the reactor, these areas of bare silicon will be etched according to the following

reactions (17,18).

$$Si(s) + H_2O(g) \rightarrow SiO(g) + H_2(g) \quad [1]$$

$$Si(s) + O_2(g) \rightarrow 2SiO(g) \quad [2]$$

The etching rate by the moisture is faster on bare silicon than on SiO_2, therefore a difference in etch rates will be established. The result of these differing etch rates is thought to be the cause of the formation of pits on the surface of the samples annealed in H_2 at 900℃.

In the case of the sample annealed at 1000℃ for 10min, shown in Fig.6(c), the atomic step is observed but there was a high level of roughness on the terrace. For the sample annealed at 1000℃ for 60min, the level of roughness on the terrace and the observed pits were the same as in the case of the 10min annealed sample. From these results we believe that the annealing time is not related to the terrace roughness and pit formation but is due to the moisture and oxygen present in the reactor.

For annealing temperatures of 1100℃ and higher, shown in Fig.6(d), the terrace was observed to be flat and clear step morphology was observed.

Effect of wet chemical processing after H_2 annealing

In order to study the effect of wet chemical wafer cleaning process on the surface micro-roughness, H_2 annealed Si(100) wafers were cleaned in $NH_4OH/H_2O_2/H_2O$ solutions with various mixing ratios. The mixing ratios of the $NH_4OH/H_2O_2/H_2O$ solutions were 1/1/5 and 1/10/100 at 80℃. Following three types of samples were prepared:

(sample A) : Etched amount from the surface was 10nm; mixed ratio of the etchant was 1/1/5.

(sample B) : Etched amount from the surface was 40nm; mixed ratio of the etchant was 1/1/5.

(sample C) : Etched amount from the surface was 10nm; mixed ratio of the etchant was 1/10/100.

The samples were then subjected to the AFM observation with an area of 4x4 μm^2.

Figs.7(a)-(e) show, AFM images of a mirror polished sample, a H_2 annealed sample and the samples that were subjected to the different SC-1 cleaning processes. The surface of the mirror polished sample, Fig.7(a), was found to have no periodic structure nor morphology, and a roughness average, Ra, of 0.07nm. The roughness average, Ra, was measured over a 3 μ m length. The H_2 annealed sample, Fig.7(b), showed a periodic atomic step structure as previously observed. The Ra was measured as 0.04nm on the terrace. In the case of sample A, Fig.7(c), which was the image observed in the H_2 annealed sample cleaned in a $NH_4OH/H_2O_2/H_2O$ (1/1/5) SC-1 cleaning solution, 10nm was etched from its surface after cleaning. The AFM image of sample A after SC-1 cleaning showed that it has a step morphology slightly less clear than the H_2 annealed

sample. The Ra on the terrace was measured as 0.07nm, the same as that of the mirror-polished surface. Sample C, Fig.7(e), which was cleaned in a $NH_4OH/H_2O_2/H_2O$ (1/10/100) SC-1 cleaning solution also had 10nm etched from its surface after the cleaning. The AFM image of sample C showed little difference from that of sample A, and also had an Ra of 0.07nm on its terrace. For sample B, Fig.7(d), a H_2 annealed wafer cleaned in a $NH_4OH/H_2O_2/H_2O$ (1/1/5) SC-1 cleaning solution, 40nm was etched from its surface. In this case the step morphology became unclear and the Ra was measured to be 0.12nm, the worst of all cases. The mono-atomic step height is about 0.135nm and in the case of samples A and C, the step morphology were still observed even though 10nm had been etched from their surfaces.

This result suggests that the etching of the SC-1 cleaning process proceeds with a layer by layer mechanism. On the other hand, the roughness on the terrace increases with the amount of SC-1 etching (sample B). Therefore it is concluded that the etching sites of SC-1 cleaning not only exist on the step edge but also on the terrace.

CONCLUSION

Surface structure of Si(100) wafers that were subjected to epitaxial growth process and associated gas etching or hydrogen annealing process, was investigated with AFM observation. After H_2 annealing the surface had a periodic terrace and mono-atomic step formation reflecting the double-domain (2x1+1x2) reconstructed structure. The vicinal Si(111) surface has a double atomic step and terrace formation, and the flatness on the terrace was better than that of the Si(100) surface. The change of the morphology and micro-roughness due to subsequent SC-1 wet chemical cleaning process after the H_2 annealing was also investigated. The surface morphology after SC-1 cleaning was found to remain unchanged to that of the H_2 annealed sample, It is concluded that the etching with the SC-1 cleaning solution proceeds with a layer by layer mechanism. However, we found that etching sites exist not only on the step edges but also on the terrace.

REFERENCES

1. K.Sakamoto, T.Sakamoto, K.Miki and S.Nagao, J. Electrochem. Soc., 136, 2705 (1989)
2. T.Nakayama, Y.Tanishiro and K.Takayanagi, Jpn. J. Appl. Phys., 26, L280 (1987)
3. N.Inoue, Y.Tanishiro and K.Yagi, Jpn. J. Appl. Phys., 26, L293 (1987)
4. G.Binning, H.Rohrer. Ch.Gerber and E.Weibel, Phys. Rev. Lett., 49, 57 (1982)
5. G.Binning, H.Rohrer. Ch.Gerber and E.Weibel, Phys. Rev. Lett., 50, 120 (1983)
6. K.Miki, H.Tokumoto, T.Sakamoto and K.Kajimura, Jpn. J. Appl. Phys., 28, L1483 (1989)
7. M.Suzuki, Y.Kudou and H.Kubota, Jpn. J. Appl. Phys., 58, 2225 (1991)
8. G.Binning, C.F.Quate and Ch.Gerber, Phys. Rev. Lett., 56, 930 (1986)

9. Y.Morita, K.Miki and H.Tokumoto, Jpn. J. Appl. Phys., 30, 3570 (1991)
10. Y.Nakagawa, A.Ishitani, T.Takahagi, H.Kuroda, H.Tokumoto, M.Ono and
11. G.E.Becker and J.C.Bean, J. Appl. Phys., 48, 3395 (1977)
12. A.Ishizaka and Y.Shiraki, J. Electrochem. Soc., 133, 666 (1986)
K.Kajimura, J. Vac. Sci. & Technol., A8, 262 (1990)
13. K.Izunome, Y.Saito and H.Kubota, Jpn. J. Appl. Phys., 31, 1277 (1992)
14. W.Kern and D.A.Puotinen, RCA REV.,31, 187 (1970)
15. T.Ohmi, M.Miyashita, M.Itano, T.Imaoka and I.Kawanabe, IEEE Trans. Electron Devices, 39, 537 (1992)
16. D.J.Chadi, Phys. Rev. Lett., 59, 1691 (1987)
17. G.Ghidini and F.W.Smith, J. Electrochem. Soc., 131, 2924 (1984)
18. J.A.Friedrich, G.W.Neudeck and S.T.Liu, Appl. Phys. Lett., 53, 2543 (1988)

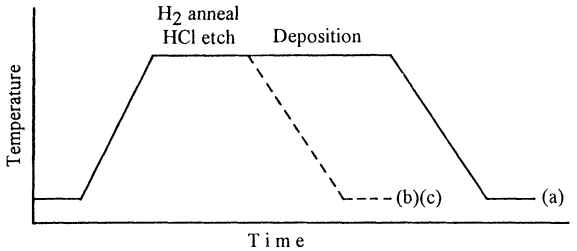


Fig.1. The epitaxial heat process.

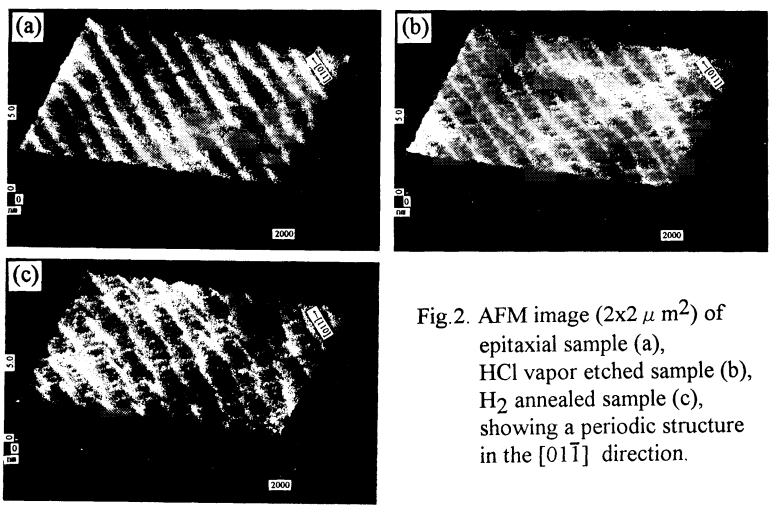


Fig.2. AFM image (2x2 μ m^2) of epitaxial sample (a), HCl vapor etched sample (b), H_2 annealed sample (c), showing a periodic structure in the $[01\bar{1}]$ direction.

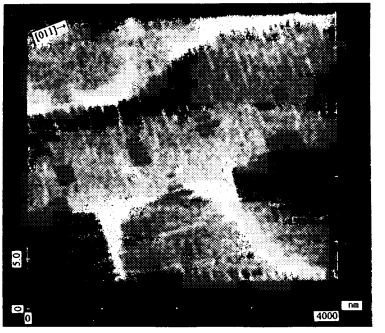


Fig.3. AFM image (4x4 μ m^2) of H_2 annealed Si(100) surface with mis-orientaion angle less than 0.05°

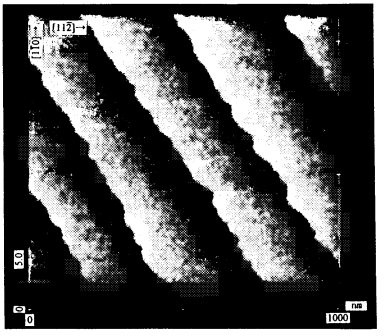


Fig.5. AFM image (1x1 μ m^2) of Si(111) surface after H_2 annealing.

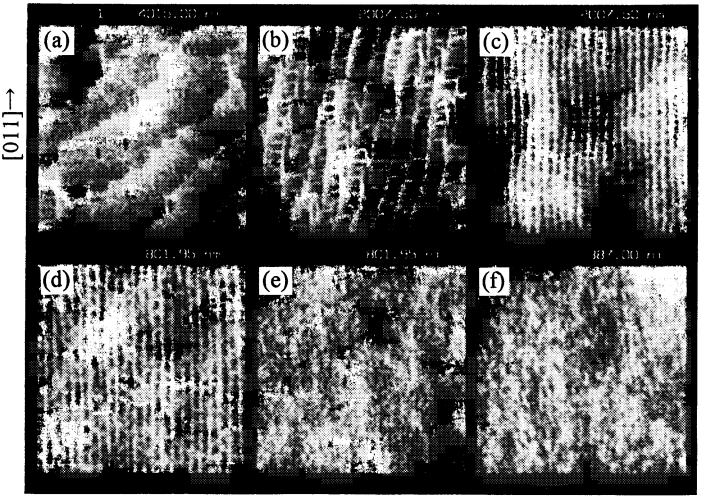


Fig.4. AFM image of Si(100) surface after H_2 annealing with various mis-orientation angles, a<0.05° , b=0.1° , c=0.2° , d=0.5° , e=1.0° and f=2.0° .

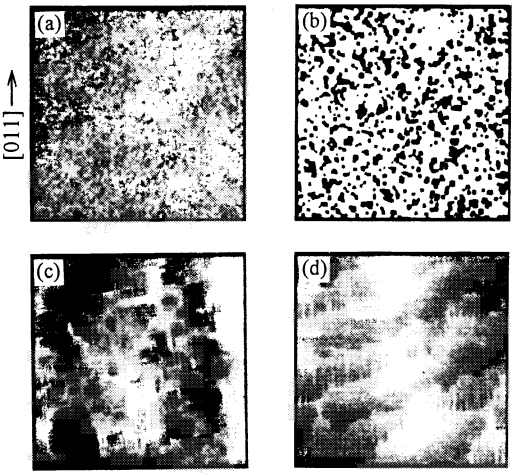


Fig.6. AFM image (4x4 μ m^2) of H_2 annealed Si(100) surface after H_2 annealing with various annealing temperatures, (a) 800 ℃, (b) 900℃, (c) 1000℃, (d) 1100℃.

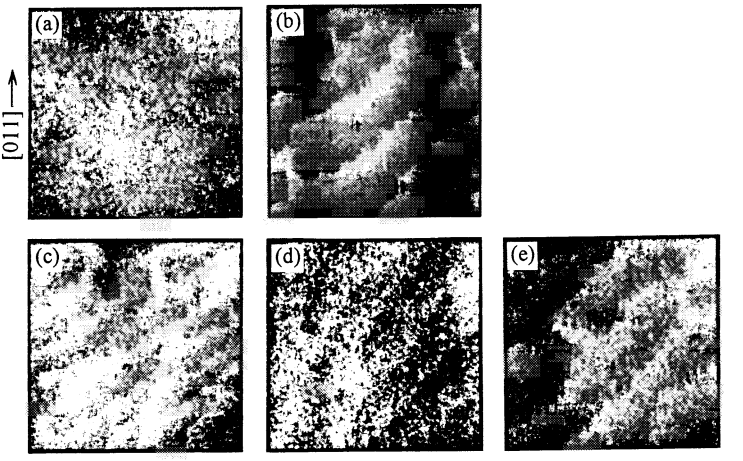


Fig.7. AFM image (4x4 μ m^2) of (a) mirror polished sample, (b) H_2 annealed sample and H_2 annealed samples after SC-1 cleaning with $NH_4OH/H_2O_2/H_2O$ mixing ratio of (c) 1/1/5(10nm) : sample A, (d) 1/1/5(40nm) : sample B and (e) 1/10/100(10nm) : sample C.

HIGH SENSITIVITY SURFACE ANALYSIS OF SILICON WAFERS BY TIME-OF FLIGHT SECONDARY ION MASS SPECTROMETRY (TOF-SIMS)

B. Schueler and R. S. Hockett

Charles Evans & Associates
301 Chesapeake Drive
Redwood City, CA 94063

This paper addresses the analytical requirements for future clean silicon wafers, the limitations of present analytical technology for surface contamination analysis, and where some new TOF-SIMS capability may fit within these requirements. The focus is on metal contamination. Some comments are made on detection of organic contamination; particulate contamination is not addressed in this paper.

INTRODUCTION

As integrated device linewidths continue to decrease, the need increases to further reduce surface metal contamination on silicon wafers. The estimated analytical requirements for future clean silicon wafers are listed in Table I.

Table I. Estimated Analytical Requirements for Metals on Future Silicon Wafers

Elements	Detection Requirement
Na, K, Li	$<10^9$ atoms/cm^2
Al, Ca	$<10^{10}$ atoms/cm^2
Ti, Cr, Fe, Co, Ni, Cu, Zn	$<10^8$ atoms/cm^2

Present analytical techniques which are used for measuring surface metal contaminants include: TXRF, VPD/AAS, VPD/TXRF, VPD/ICP-MS, SIMS and TOF-SIMS [1]. TXRF provides detection limits of the order 10^9cm^{-2} to 10^{10}cm^{-2} for transition metal contamination, with an analytical depth of approx. 80 Angstroms [2]. VPD technologies provide detection limits on the order of 10^8cm^{-2} to 10^9cm^{-2} for all the metals listed in Table 1 [3], however, the collection efficiency is a function of the chemical bond [3,4], so that accuracy of the measurement is unknown. SIMS provides detection limits for the alkali and light metals on the order of 10^9cm^{-2}, however, SIMS is not as sensitive enough for transition metals because of the matrix mass interferences. There is an opportunity for a single analytical technique which could reach the detection limits in Table I without the chemical bond issue of VPD/..technologies.

Present-day TOF-SIMS can provide high sensitivity analyses of sample surfaces at primary ion doses $<10^{12}$cm^{-2}, i.e. below the "static SIMS" limit. This high surface

sensitivity is due the high secondary ion transmission and simultaneous mass detection capability inherent of the technique. An analysis can be carried out in such a way that almost all secondary ion of a given polarity are collected in a mass spectrum, unlike conventional SIMS. These analytical conditions, where approx. 1% of the surface layer is affected by the primary ion beam are very well suited for the characterization of organic contaminants. TOF-SIMS has become a rather established analytical technique for organic surface analysis of e.g. polymer materials, providing characteristic ion mass spectra of the molecular compounds. If the primary ion dose exceeds the static SIMS limit, characteristic organic molecular information is irreversibly lost. Information on atomic contaminants for this surface layer is automatically provided.

The application of TOF-SIMS in atomic metal contamination analysis of silicon wafers requires different considerations. Detection limits of 10^9-10^{10}cm^{-2} per monolayer of material can be obtained by TOF-SIMS and are presently unrivaled by other techniques. If only the outermost surface layer of the sample is analyzed, the result is interesting in itself but quantification of the result is rather ambiguous since no direct comparison to any other technique is available. Impurity concentrations from the outer monolayer can be skewed by surface coverage with organic contaminants and by non-uniform diffusion of the contaminants through the native oxide. All the above factors indicate that the TOF-SIMS analysis should be integrated throughout the native oxide layer to take best advantage of the intrinsically high sensitivity of the technique and to provide quantitative results. This goal can in fact be achieved by utilizing a pulsed high current primary ion gun with the TOF spectrometer in order to consume and analyze the complete native oxide layer over an extended area within a reasonable time period. This approach promises metal detection limits of the order 10^8-10^9cm2 for many contaminants.

EXPERIMENTAL

The experiments were conducted using a Charles Evans & Associates model TFS-4000MMI time-of-flight secondary ion mass spectrometer. A detailed description of the mass spectrometer is given in reference [5]. The instrument is configured for ion microscope ion imaging analysis with lateral resolutions up to approx. 1mm, as well as microprobe imaging with lateral resolutions of approx. 0.2mm. The system is equipped a microfocused Ga Liquid Metal Ion Gun (LMIG) for high resolution microprobe imaging applications. The LMIG is operated at beam energies between 15 and 25keV. A high current pulsed Cs primary ion gun is provided for high speed data acquisition and microscope imaging applications at high mass resolution. The Cs column is operated at primary ion energies of 11keV and is capable of providing well is excess of 10^4 Cs primary ions into a sub-nanosecond pulse. Mass resolutions of m/Dm=7500 at $^{28}Si^+$ and m/Dm=13000 at $C_2F_5^+$ are routinely obtained. The instrument is also equipped with low energy (15eV) electron charge compensation to provide analysis of electrically insulating surfaces.

The data system allows the storage of every position (x,y) and time (mass) coordinate during the analysis. This storage procedure results in a "raw data" file, containing all information collected during the analysis and is the available for a retrospective data replay on any suitable computer system. It is thus possible to reconstruct ion images from any arbitrary secondary ion signal detected within the analysis mass range (typically 0-1000u). Conversely, mass spectra can be reconstructed from any

sub-region of the secondary ion images which appear to be of interest. Additionally, it is possible to integrate selected peak intensities for a given time period (e.g.1min.) and monitor the evolution of the ion signals with analysis time. For analyses utilizing high primary ion beam doses, the result can be displayed in form of a depth profile while the analysis is still in progress.

RESULTS

1. Trace metal analysis

Trace metal analysis of silicon wafers by TOF-SIMS has to date been primarily applied to the topmost monolayers of the sample surface. This approach can provide the "true" surface concentration of impurities but is relatively dependent on the condition of the surface layer. Any wafer surface analyzed so far in this laboratory exhibited relatively large amounts of organic surface contaminants which usually cover only a fraction of the surface monolayer but can, in extreme cases suppress metal detection from the surface. No obvious correlation between high levels of metal contaminants and organic surface contamination is observed. It is clear that the wafer surface analysis has to extend at least beyond the organic surface contamination layer.

Probably the most pressing reason to extend TOF-surface analysis throughout the native oxide layer of the wafer surface is the issue of impurity quantitation. Standard surface analysis techniques such as TXRF analyze the top 80 Angstrom of the surface and VPD/AAS dissolves and analyzes the native oxide layer. In order to provide cross calibration of the TOF surface analysis with these techniques, quantitative analysis can only be provided if the analyzed sample depth is comparable. This approach has been implemented in the TOF analysis by utilizing a high current pulsed Cs source. The ion gun is operated at repetition rates of 33kHz and rastered over an area of up to 180mmx180mm. Under these conditions it is possible to provide material removal rates of approx. 1.5 Angstrom/minute during the analysis with an analysis duty cycle of 100%. A 30 minute analysis therefore provides an analysis depth of roughly 50 Angstrom which is compatible and allows comparison of the data with TXRF and VPD/AAS analyses. First experiments utilizing this mode of TOF-SIMS operation are reported in this section.

The need and virtues for such in-depth trace element analysis by TOF-SIMS obtained with the high current Cs gun is illustrated in Figure 1. The analytical area was 100mmx100mm with an analysis depth of 50 Angstrom. The total analysis time was 30 minutes. The silicon wafer had been intentionally contaminated with transition metals by spin coating and was previously analyzed by VPD/AAS, as well as TXRF. The Fe surface concentration was given as $1x10^{13}cm^{-2}$. The TOF-SIMS depth profile in Figure 1 was generated by integrating the secondary ion counts of ^{56}Fe, $^{28}Si_2$, SiO_2, C_4H_8, and Cu for 45 seconds in each cycle during the analysis. At the same time, the counts for all detected secondary ions are integrated in the resulting mass spectrum over the duration of the analysis. It is clearly seen in Figure 1 that Fe and Cu penetrate well into the native oxide layer of the wafer surface. The C_4H_8 secondary ion intensity, which is indicative for hydrocarbon surface contamination, falls very quickly from the beginning of the analysis (surface) and disappears after a few minutes due to primary ion beam damage. The maximum of the Fe ion intensity is <u>not</u> observed at the very surface but some monolayers deeper, indicating that Fe is depleted at the surface or partially masked by other

contaminants. This qualitative behavior is not observed for Cu, which immediately starts out at high levels and drops to low levels as the analysis proceeds through the native oxide layer. This seems to indicate that the initial depletion of Fe at the top surface is not due to coverage by organic contaminants but a result of Fe diffusion into the native oxide.

In summary, the depth profile in Figure 1 shows that extended analysis depth are crucial if semi quantitative TOF-SIMS analysis is to be attempted since surface diffusion can very strongly influence the observed surface concentrations. The layer-by-layer analysis provided by TOF-SIMS does, however also provide at least qualitative insight into the depth distribution of the contaminants as a rather interesting byproduct. This information appears rather important as an additional indicator for the origin of some contaminants, particularly alkali metals. Extended analysis depth (and area) does, of course, also increase the detection sensitivity.

To demonstrate that TOF-SIMS can provide quantitative metal contamination analysis on silicon wafers under the above experimental conditions, a set of wafers having different Fe surface concentrations was analyzed. The wafer were first analyzed by TXRF to determine the Fe impurity levels and then analyzed with the TOF-SIMS system. The wafers had Fe surface concentrations between $4x10^{10}$ and $1x10^{13}cm^{-2}$ as determined by the TXRF measurements. The TOF-SIMS analyses were obtained for analytical areas of 65mmx65mm on at least two spots of the wafer surface with an analytical depth of approx. 50 Angstrom. Selected samples were again analyzed using ion collection areas of 100mmx100mm, and 150mmx150mm and utilizing the same analytical depth. The maximum data acquisition time was 30 minutes.

Figure 2 shows a correlation of the surface concentration obtained by TOF-SIMS and those determined by TXRF. For TOF-SIMS the integrated Fe counts obtained during the analysis were normalized to the integrated counts of Si_2. This normalization is assumed to provide a representation of the relative Fe concentration with respect to Si and is relatively insensitive to potential fluctuations of the primary ion current. For a given analytical area the integrated Si_2 intensity will provide a course measure of the amount of material consumed. It can be seen from Figure 2 that the normalized Fe surface concentration determined by TOF-SIMS correlates rather well with the TXRF measurements within the experimental errors. The solid line shown in the graph represents a slope of one and thus a linear relationship between the TOF-SIMS and TXRF experimental data. Semiquantitative analysis of metal impurity concentrations on silicon wafers thus appears to be feasible under conditions where the complete native oxide layer is analyzed.

It should be noted at this point that good correlation of impurity concentrations determined by TOF-SIMS and TXRF is also obtained under conditions where only the top surface is analyzed. The main difference is, however, that the scaling of the Fe intensity determined by TOF-SIMS was not linear with respect to TXRF and the fitting lines indicated a much shallower dependence of the normalized TOF-SIMS results, more compatible with a square root dependence. This effect, observed in this and other laboratories [6], may have been a result of surface diffusion.

The detection limits achievable by TOF-SIMS are dependent on the ability of the instrument to separate the element of interest from interfering signals (e.g. ^{56}Fe from $^{28}Si_2$), secondary ion transmission, and the analyzed area. An additional restriction does result from the fact that the analysis has to be completed within a reasonable time period,

which should probably not exceed 30 minutes. The analysis time is strictly related with the analyzed area. Figure 3 shows the number of secondary ion counts for ^{56}Fe obtained for three different analysis areas. The analysis depth in all three cases was approx. 50 Angstrom with a maximum analysis time of 30 minutes. The Fe counts for each analytical area were normalized to the highest Si_2 intensity within the set. The three sets of data are compatible with a linear dependence of the integrated Fe intensity versus Fe concentration determined by TXRF. The smallest analysis area of 65mmx65mm would provide the minimum detectable Fe peak with 30 counts at a surface concentration of approx. 10^9cm^{-2} and provide a rather intense signal at $10^{10}cm^{-2}$ levels. This extrapolated detection limit can be improved by utilizing an ion collection area of 150mmx150mm with detectable Fe signals in the mid to high 10^8cm^{-2} contamination levels. The detection of Fe in Si is a relatively demanding task on the spectrometer due to the proximity of the interfering Si_2 species. Further, more detailed studies are required to unambiguously determine whether Fe can indeed be detected at these low levels. With present performance levels for TOF-SIMS instruments [7,8] it would seem to be a good estimate to place Fe detection limits into the region of 10^9-$10^{10}cm^{-2}$.

TOF-SIMS detection limits for other elements than Fe can at least be estimated using reasonable assumptions for ionization efficiency and proximity of interfering ion species. It shall be assumed that the analytical area is 150mmx150mm, 50 Angstrom deep (Figure 3). The detection of Al is rather straightforward since the only interfering mass species is C_2H_3. Additionally, Al has better ionization efficiency than Fe (by a factor of >2). The achievable detection limits can therefore rather safely be placed at surface concentrations of 10^8cm^{-2}. A similar situation applies for Mg. Na on the other hand has no interfering mass species and is known to have ionization efficiencies approx. 10 times higher than typical transition metals, resulting in estimated detection limits around 10^7cm^{-2}. Similar detection limits are expected for most alkali metals. On the other extreme, Zn provides rather poor detection limits under SIMS conditions due to its low ionization efficiency and detection limits in the mid 10^9cm^{-2} are expected, i.e. in the vicinity of TXRF detection limits today.

Using the above assumptions, it is interesting to estimate the contamination levels of F Na, Mg, and Al for wafers having different Fe surface concentrations. Table II below gives the result of such an estimate. The surface concentration was estimated from the signal intensity normalized to Si_2, using Figure 2 as reference, and conservatively assuming that the actual metal concentration is a factor 2 lower for Al and Mg, and 10 times lower for Na. The ionization efficiency of Fluorine is excellent for negative secondary ions but F^+ is also formed rather inefficiently and a correction factor of 50 was applied with respect to Fe.

Table II. Surface Areal Densities for Elements
on the Surface of the Spin Coat Contaminated Silicon Wafers

Sample	Fe(TXRF) cm^{-2}	F(TOF) $est.cm^{-2}$	Na(TOF) $est.cm^{-2}$	Mg(TOF) $est.cm^{-2}$	Al(TOF) $est.cm^{-2}$
2	$4x10^{10}$	$1x10^{12}$	$3x10^{10}$	$4x10^{10}$	$8x10^{12}$
1	$7x10^{10}$	$3x10^{12}$	$6x10^{10}$	$5x10^{11}$	$2x10^{13}$
4	$1x10^{11}$	$1x10^{12}$	$9x10^{11}$	$5x10^{10}$	$3x10^{12}$
3	$9x10^{11}$	$2x10^{12}$	$3x10^{10}$	$5x10^{10}$	$5x10^{13}$

The estimated Fluorine surface concentrations for the four wafers were found to be rather uniform in the region of $10^{12}cm^{-2}$. Additionally, it was observed that the maximum intensity of F was always observed at the beginning of the analysis and can thus be identified as a "true" surface contaminant. This result is not very surprising since the cleaning procedure most likely involved a wafer immersion in hydrofluoric acid. Contrary to Fluorine, Na, Mg, and Al yielded the highest intensity below the top monolayer and remained at high levels throughout the native oxide layer. Sample#4 appeared to have the highest Na contamination level but showed the lowest Mg and Al levels of the group. Sample#1 showed the highest overall low mass contamination levels despite of the rather low Fe contamination. It should be noted that this particular sample had a Zn contamination level of $10^{12}cm^{-2}$. Although this set of data gives only a rather course estimate of the low mass contaminants, it seems rather clear that wafers that exhibit low levels of transition element contaminants are not necessarily the one having low alkali metal or, e.g. low levels of Al. This particular element region is, of course not within the analysis range of TXRF.

2. Organic surface analysis

Organic surface analysis of wafer surfaces is automatically obtained in the early phases of the analysis when the primary ion dose is below $10^{12}cm^{-2}$. Under these primary ion dose conditions it is possible to obtain secondary ion mass spectra which contain signals characteristic to the structure of the organic compound(s) in question [9]. In order to obtain an organic secondary ion mass spectrum of the sample surface, the primary ion current is typically reduced since the mass spectrum can only obtained from a fraction of the topmost monolayer. Typical analysis times for such measurements are 5-10 minutes.

Figure 4a shows the positive secondary ion mass spectrum obtained from the surface of a silicon wafer in the mass range of 0-250u. Without going to great detail it is rather obvious that the majority of ion signals observed in this mass spectrum is due to organic molecular species. The most prominent molecular signals in the low mass range are due to hydrocarbon contaminants and are of the type $C_nH_m^+$ (m=15, 27, 29, 41, 43, etc.). These signals are observed on virtually any sample surface and are thus relatively unspecific. This type of "fingerprint" mass spectrum is, however, also observed from clean surfaces of polyethylene and may well partially be due to packaging materials. Figure 4b shows an expanded region from the same mass spectrum around mass 42. The four secondary ion signals can be unambiguously identified as $SiCH_2$, C_2OH_2, C_2NH_4, and C_3H_6 with an error of less than 0.001 mass units. The signal at C_2NH_4 strongly indicates the presence of amines on the surface. A further examination of the mass spectrum shows that a variety of higher mass signals of this type are observed (particularly at even masses), indicating the presence of a relatively high molecular weight amine on the surface and not simply a residue of an Ammonium Hydroxide cleaning step. A more detailed analysis of the organic contaminants is rather difficult since the history of the sample is not known.

A typical organic contamination signal caused by packaging materials is observed at mass 149u (Figure 4a). Exact mass assignment identifies this ion signal as $C_8O_3H_5$ within 0.0004 mass units. This signal is typical for any dialkylphtalates which are commonly used as plasticizer for polymeric materials.

The example in Figure 4 gives only relatively unspecific organic contamination signals. It should, however be noted that a rather strong variation in the amount of organic contaminants was observed in the wafers analyzed for metal impurities in the previous section. The most pronounced difference was found in the presence of amines on the surface which are usually not due to the packaging container (most commonly polyethylene or polypropylene). Before the TOF-SIMS analysis, the samples were inside a polystyrene box, which apparently did not cause any major organic contamination of the wafer surface.

TOF-SIMS can also be applied for the investigation of small area contaminations such as particle contaminants on wafers or residues on integrated circuits. Sub-micrometer analysis is typically performed using the microfocused beam of a Liquid Metal Ion Gun (LMIG). Analyses utilizing the pulsed LMIG as primary ion gun can provide lateral image resolutions better than 0.2mm. Organic as well as inorganic information can be extracted from analytical areas smaller than 1mmx1mm. The identification of organic particles with sizes much smaller than 1mm will depend on its composition, particular the secondary ion yield of the compound in question. This restriction does not apply for the analysis of elemental impurities since the destructive effect of the primary ion beam is not critical for this type of application.

CONCLUSION

TOF-SIMS can provide high sensitivity surface analysis of silicon wafers with metal detection limits well below $10^9 cm^{-2}$ for many elements. The detection limits for alkali metals and halogens are expected to be well below this limit. Any element can in be analyzed and particularly good detection limits are expected for those elements which are not accessible by TXRF analysis. Additionally, TOF-SIMS analysis also provides information on organic contaminants at the surface layer of the sample and specific molecular information can be extracted in either small or large area analysis.

ACKNOWLEDGMENT

The authors would like to thank J.M.Metz for providing the TXRF analysis for the silicon wafers investigated in this study, and E.P.Marsh for contributions in preparing the experiments.

REFERENCES

[1] R. S. Hockett, "Ultratrace Impurity Analysis by SIMS and TXRF," Handbook of Semiconductor Wafer Cleaning Technology, edited by Werner Kern, Noyes Publications (Park Ridge, New Jersey) pp. 537-592 (1993).

[2] R. S. Hockett, "High Sensitivity Characterization of Contamination on Silicon Surfaces Using TXRF," 1993 Proceedings Vol 1 of the Institute of Environmental Sciences, The Institute of Environmental Sciences (Mount Prospect, Illinois) pp. 432-459 (1993).

[3] A. Shimazaki, "Chemical Analysis of Silicon Wafer Surface Contamination," Defects in Silicon II, edited by W. M. Bullis, U. Gosele, and F. Shimura, ECS Proceedings Vol. 91-9, The Electrochemical Society (Pennington, NJ) pp. 47-56 (1991)

[4] C. R. Helms and H-S Park, "Generalized Model of Metal Bonding and Cleaning from Wafer Surfaces," presented at the Materials Research Society, April 1993, San Francisco, 1993.

[5] B.Schueler, Microsc. Microanal. Microstruct., 3, p.119ff. (1992).

[6] U.Juergens, et.al., Proc. SIMS VII Conf., Wiley & Sons, p.447f. (1989)

[7] B.Schueler, et.al., Proc. SIMS VIII Conf., Wiley & Sons, p.281ff. (1991)

[8] U.Juergens, et.al., Proc. SIMS VIII Conf., Wiley & Sons, p.277ff. (1991)

[9] see for example: Proc. SIMS VIII Conf., Wiley & Sons, (1991)

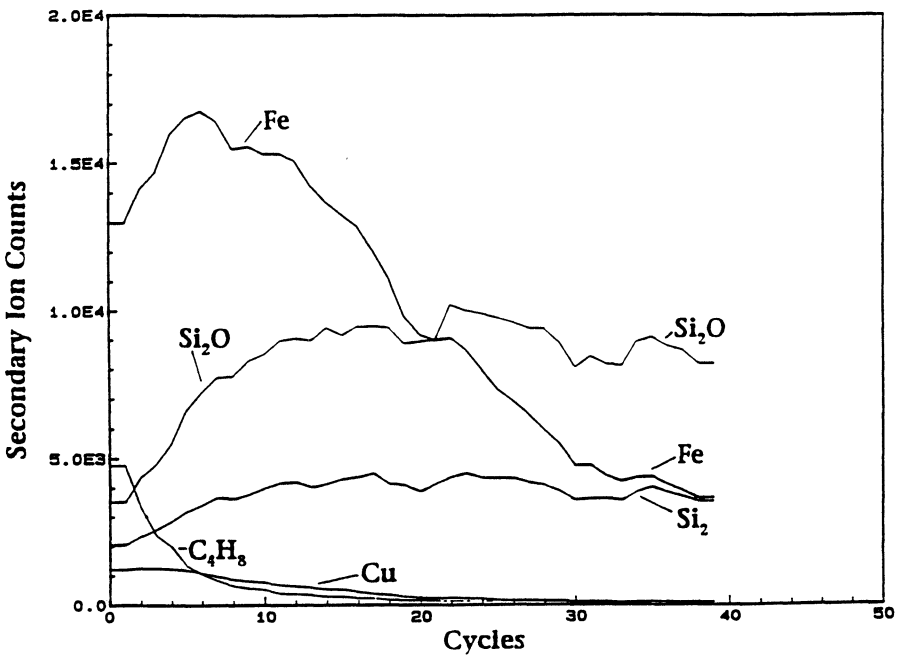


Figure 1. TOF-SIMS analysis of a silicon wafer with $10^{13}cm^{-2}$ surface concentration of Fe using the pulsed Cs primary ion gun. The data for selected secondary ions are presented in form of a multielement depth profile. Each cycle represents the integrated counts for the respective secondary ions in a 45 second period. All data are collected within the same analysis. The total analysis time was 30 minutes and the estimated analysis depth is approximately 50 Angstroms. The analyzed area is 100mmx100mm.

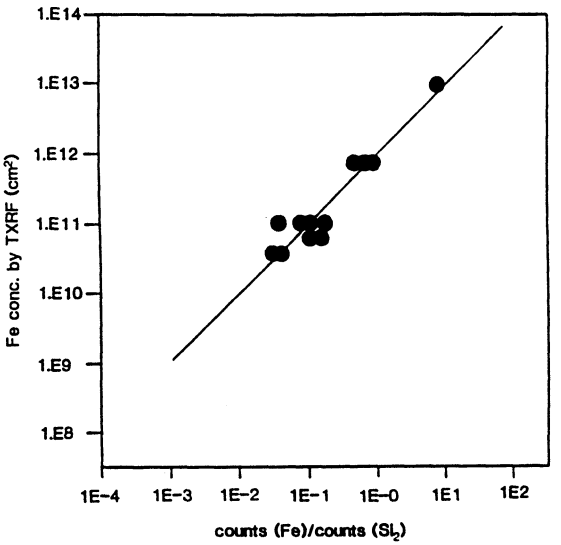


Figure 2. Fe surface concentration determined by TXRF versus the normalized intensity of Fe (Fe/Si_2) determined by TOF-SIMS. The approximate analysis depth for TOF-SIMS is approx. 50 Angstroms.

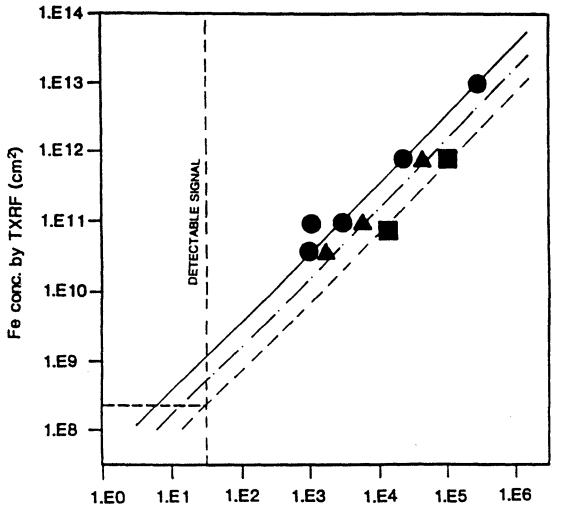


Figure 3. Fe counts obtained during TOF-SIMS analysis of silicon wafers using analysis areas of 65 μmx65μm(●), 100μmx100μm(▲), and 150μmx150μm(■) versus Fe concentration determined by TXRF. The detection limits are indicated by linear extrapolation through the data points.

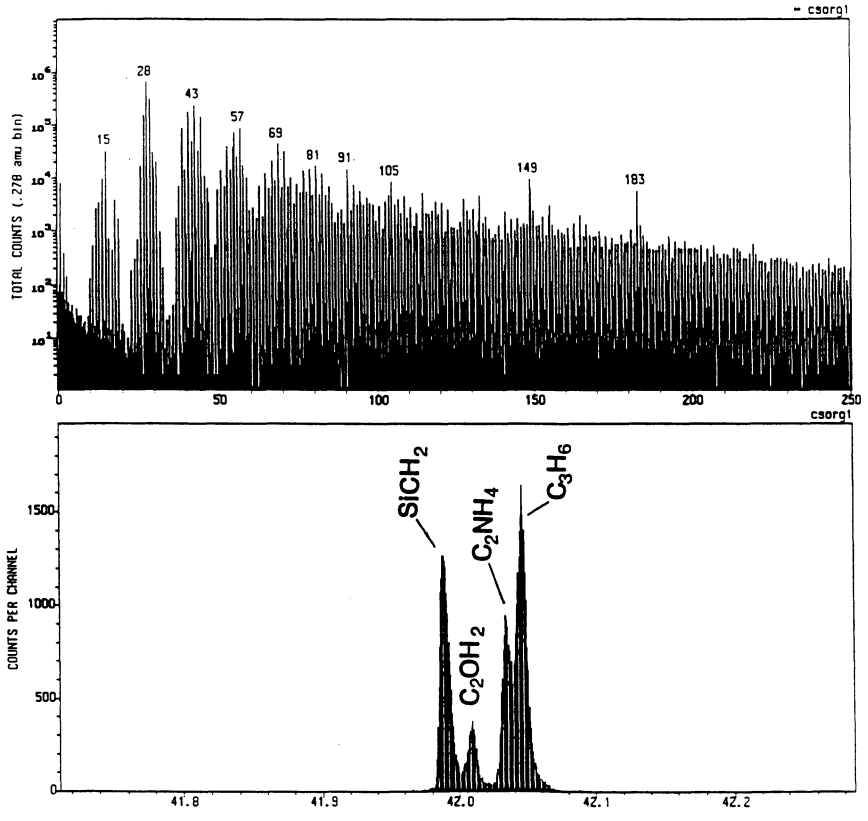


Figure 4. Positive secondary ion mass spectrum obtained from the surface of a silicon wafer. The Cs primary ion dose was approx. 10^{11} cm^{-2}. Figure 4a shows a logarithmic display of the mass spectrum in the mass range from 0 to 250μ. Figure 4b is an expanded section of the same mass spectrum showing the signals around mass 42μ with their respective identification.

SILICON WAFER SURFACE ANALYSIS BY ELECTROTHERMAL VAPORIZATION INDUCTIVELY-COUPLED PLASMA MASS SPECTROMETRY (ETV-ICP-MS)

Kenneth Ruth, Philip Schmidt, Jose Coria, and Erik Mori
MEMC Electronic Materials, Inc.
501 Pearl Dr. St. Peters, MO 63376

ABSTRACT

Advances in the electronics industry towards large-scale integration of semiconductor devices have placed strict demands on the ability to measure and monitor ultratrace levels of impurities. Metallic contaminants above 10^{10} atoms/cm^2 can cause electrical component failures and ultimately result in lower yields. This work describes the use of ETV-ICP-MS as a complimentary alternative analytical technique to assessing metallic impurity levels on silicon wafer surfaces. Instrument capabilities and limitations toward this application will be discussed.

INTRODUCTION

Significant reduction of contaminants on silicon wafers surfaces is needed in order to meet future requirements of the microelectronic industry. Contaminants, namely alkaline and alkaline earth, and transition metals are known to lower device yields. Some of the common defects include leakage and anomalous drift currents, oxide breakdown, and minority carrier lifetime degradation as a result of high diffusivities and solubilities of these contaminants in silicon and silicon oxide. Several analytical techniques are presently capable of detecting trace level impurites on the surface of silicon. In terms of chemical analysis, secondary ion mass spectrometry, SIMS [1,2]; total reflectance X-ray fluorescence, TXRF [3]; ion chromatography [4], and graphite furnace atomic absorption, GFAAS [2] are typically employed for silicon surface analysis. Recently, ICP-MS with flow injection has been applied for wafer surface analysis [5,6]. However, ICP-MS **using electrothermal vaporization (ETV)** is introduced here as an alternative method sample introduction method. Prior initial work on ETV-ICP-MS for silicon wafer surface analysis have shown excellent detection limits of 10^7 atoms/cm^2 [7]. ICP-MS possesses many of the

advantages of other techniques, namely low volume work, multielement capability, analysis speed, low detection limits, and sample versatility. The goal of this paper is to discuss the instrument capabilities and limitations toward this application.

EXPERIMENTAL

A VG Plasmaquad II+ Turbo series quadrupole-based ICP-MS and a Mark III electrothermal vaporization accessory were employed. The ICP-MS instrumental parameters, and calibration standard preparations have been described elsewhere [8]. The ETV-ICP-MS conditions described in this text were optimized to obtain routine performance for the elements studied.

A method similar to droplet surface etching (DSE) known as acid drop (AD) was used for collecting silicon wafer surface impurities [9]. A water droplet (typically 250-500 μL) consisting of a 10% HF (v/v) and 20% H_2O_2 (v/v) solution is added on to and scanned over the entire front wafer surface within one minute. The use of hydrogen peroxide enables this technique to extract essentially all of Cu that has been found to electroplate on the silicon surface after an HF-treatment [3,5,9]. Recovery studies consisted of intentional contamination on wafers using atomic absorption standards of known concentration and volume.

The instrument can rapidly analyze one (using single ion monitoring, SIM) or more elements (multielement scan or peak jump) simultaneously. SIM is used to obtain maximum sensitivity, thus lower detection limits. Multielement analysis is applied when only limited volumes (<200 μL) are available. In the multielement scan, a selected atomic mass range is swept over the data acquisition time while in peak jump only certain isotopes are selected. However, with peak jumping, the quadrupole requires extensive settling (stabilization) times before signal is acquired. Due to ETV's transient nature, multielement scanning mode was used since it provided more reproducible results over the peak jumping mode. This effect is explained further in the text.

RESULTS AND DISCUSSION

Recovery studies were performed by spiking and evenly dispersing a known amount of trace metals standard solution and drying the liquid on silicon wafers. The contaminants are subsequently extracted using $HF-H_2O_2$ mixture as described in the Experimental Section above. Table I shows that the average recoveries of intentionally-contaminated 200-mm wafers at $5x10^{10}$, $1x10^{11}$, and $5x10^{11}$ atoms/cm^2 are within $\pm$16% of the expected value except for Ti. These values were based on at least four wafers with single extraction per wafer and duplicate runs per wafer. The decreased recovery for Ti at $5x10^{10}$ atoms/cm^2 is ascribed to the formation of a refractory carbide with the graphite tube prior to the vaporization stage. Note however, excellent recoveries are obtained above this level and extracting with hydrogen peroxide mixed with HF leads to essentially 100% Cu recovery.

Correlation between similar sample introduction techniques such as ETV-ICP-MS and GFAAS using the graphite furnace were also performed. The graph in Figure 1 indicates that ETV-ICP-MS for iron correlates well with GFAAS. The data represents over 75 wafers tested in the range between low 10^{10} atoms/cm^2 to high 10^{11} atoms/cm^2. The analysis of ^{56}Fe by ETV-ICP-MS is facilitated by removal of $^{40}Ar^{16}O$ isobaric interference originating from water as the oxygen source. This is accomplished by venting moisture through the sample injection orifice during the drying stage [8]. ETV possesses the advantages over flow injection with ultrasonic nebulization (FIA-USN-ICP-MS) and GFAA since all critical elements including Fe can be analyzed simultaneously by one technique [5]. Similar correlation was obtained for other elements such as Na, Zn, Cu, Ni, and Cr.

The detection limits for a 200-mm wafer using SIM and multielement scanning shown in Table II demonstrate that ETV-ICP-MS is capable of measuring at 10^8-10^9 atoms/cm^2. The detection limits will vary with wafer size, extraction collection volume, and injection volume for methods such as IC, ICP-MS, and GFAAS where total liquid impurity collection from a single wafer is critical. The absolute detection limit for ICP-MS is in the tens of picograms to sub-picogram range. However, the sensitivity will decrease as the number of elements for analysis is increased. Despite a data collection time of 1.2-3 seconds, the technique's transient nature with a residence (i.e., integration/data collection) time of 0.5 seconds allows only a limited number of sweeps through the entire mass range of interest. The scanning mode in multielement ETV analysis requires fewer adjustments to the quadrupole stabilization time. This is

in contrast to the peak jumping mode where it is necessary to perform a stabilization for every isotope of interest. This results in less signal variation and hence preference with the scanning mode.

High sample throughput is achieved since analysis time is only 60-70 seconds per measurement for 12 elements (typically Na, Mg, Al, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, and Zn). This is in contrast to GFAAS where only one element is analyzed for the same allotted time, and TXRF where typically 1000 seconds are required for sufficient signal detection.

In quadrupole-based ICP-MS, where resolution is around 0.5 amu, elements such as Ca and K are presently not amenable to ETV-ICP-MS due to a large ^{40}Ar mass spectral interference in the vicinity of the isotopes of interest. The detection limits for P, Si, O, N, Cl, and S are also poor compared to the other techniques due to air entrainment and low ionization factors.

We believe ICP-MS continues to provide a valuable research tool in defining cleaning process for silicon wafers. However, it is presently not amenable for ***routine*** work due to the operation, calibration, and maintenance complexity when analyzing sub-ppb levels of impurities on wafer surfaces. However, with ongoing automation, data processing, and sample handling issues, we expect ICP-MS with possibly high resolution-based systems and advances in wafer surface preparation to drive to lower analytical detection limits.

CONCLUSION

This work describes how the ICP-MS is employed as an alternative and complimentary technique in monitoring impurity levels on silicon wafers. ETV-ICP-MS is able to measure metallic impurities at the levels well below 10^{10} atoms/cm^2. ETV-ICP-MS is also capable of analyzing iron, and is invaluable for high-throughput and multielement ultratrace level work.

REFERENCES

(1) C.E. Young, M.J. Pellin, W.F. Calaway, B. Jorgensen, E.L. Schweitzer, and D.M. Gruen, *Nucl. Instrum. Methods Phys. Res. B* **27**, 119 (1987).

(2) T. Shiraiwa, N. Fujino, S. Sumita, and Y. Tanizoe, *Semiconductor Fabrication: Technology and Metrology*, ASTM 990, Ed. D.C. Gupta, p. 314-23, American Society for Testing and Materials, Philadelphia (1989).

(3) C. Neumann and P. Eichinger, *Spectrochim. Acta*, **46B**, 10, 1369-77 (1991).

(4) K. Ruth and R. Shaw, *J. Chromatogr.*, **546**, 243-9 (1991).

(5) J. Fucsko, S.S. Tan and M.K. Balazs, *J. Electrochem. Soc.*, **140(4)**, 1105-9, 1993.

(6) M. Tsuji, U. Hase, and T. Shimono, *52nd Autumn Meeting of Jap. Soc. Appl. Phys.*, Abstr. 10p-C-5, Oct. 12, 1991.

(7) Y. Okui and M. Yoshida, *Ultraclean Technology*, **4**, 1520, 1992.

(8) K. Ruth, P. Schmidt, and E. Mori, *Spectrosc.*, **7(9)**, 36-39, Nov.-Dec.(1992)

(9) W. Hub and V. Penka, *Microcontam. Conf. Proc.*, 266-279, 1991.

Table I. Average Percent Recoveries of Trace Metals on Bare 200-mm Wafers

Isotope/ Element	5E10 Recovery (%)	1E11 Recovery (%)	5E11 Recovery (%)
^{23}Na	113	101	114
^{24}Mg	104	104	103
^{27}Al	108	104	92
^{46}Ti	76	94	99
^{53}Cr	93	101	98
^{55}Mn	97	95	103
^{56}Fe	100	100	111
^{58}Ni	98	99	98
^{59}Co	98	99	101
^{63}Cu	100	98	105
^{64}Zn	97	84	101

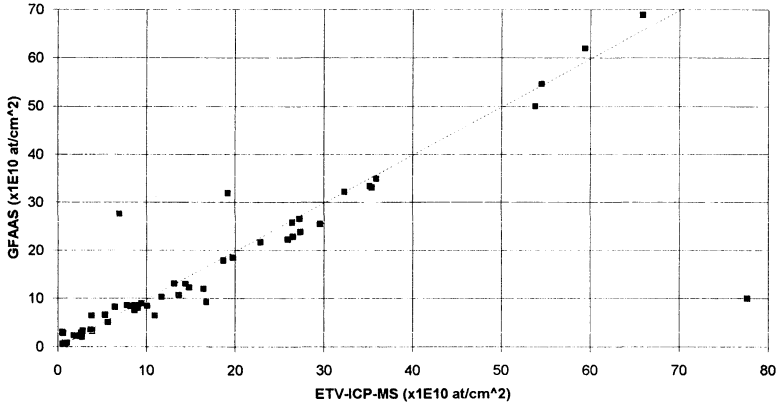


Figure 1. Correlation for Fe Between ETV-ICP-MS and GFAAS on Silicon Wafers.

TABLE II. Typical Detection Limits on 200-mm Si Wafer Surfaces

Element/ Isotope	Detection Limit* ppbw	Detection Limit Atoms/cm^2	Sample Introduction Method	Sample Volume mL
^{23}Na	0.1	2.1E+09	ETV-multielem scan	0.25
^{24}Mg	0.1	2.0E+09	ETV-multielem scan	0.25
^{27}Al	0.05	8.9E+08	ETV-SIM	0.25
"	0.1	1.8E+09	ETV-multielem scan	0.25
^{46}Ti	0.3	3.1E+09	ETV-multielem scan	0.25
^{56}Fe	0.03	2.6E+08	ETV-SIM	0.25
"	0.1	8.5E+08	ETV-multielem scan	0.25
^{59}Co	0.1	2.4E+08	ETV-multielem scan	0.25
^{66}Zn	0.05	3.6E+08	ETV-SIM	0.25
"	0.1	7.5E+08	ETV-multielem scan	0.25
^{53}Cr	0.3	2.7E+09	ETV-multielem scan	0.25
^{55}Mn	0.1	8.7E+08	ETV-multielem scan	0.25
^{60}Ni	0.3	2.4E+09	ETV-multielem scan	0.25
^{63}Cu	0.1	7.6E+08	ETV-multielem scan	0.25

* based on at least 3σ of a blank baseline noise peak height. Typical injection volume is 60 μL.

Observation of Hydrocarbons on Silicon Wafers using APIMS-TDS

N. Yabumoto, N. Kawamura *, and Y. Komine*

NTT Interdisciplinary Research Labs., *NTT LSI Labs.
3-1 Morinosato Wakamiya, Atsugi-shi, Kanagawa, 243-01, JAPAN

ABSTRACT

An APIMS-TDS (atmospheric pressure ionization mass spectroscopy-thermal desorption spectroscopy) system has been developed for analyzing hydrocarbons on silicon wafers. The measurement is carried out with flowing highly purified gas. Desorption of hydrocarbons is observed sensitively without a fear of oil back from vacuum system. Combustion reaction is also found out in the case of oxygen gas flowing. They are completely burned during thermal oxidation, but they may react with silicon to make silicon carbide in heating in argon gas.

INTRODUCTION

Silicon wafer surfaces are attacked by many materials such as particles, metals, native oxide, water and hydrocarbons during LSI fabrication process. Among these materials, particles, metals, and native oxide are analyzed by several methods, for instance laser counting, total reflection X-ray fluorescence, secondary ion mass spectroscopy, atomic absorption spectroscopy and X-ray photoelectron spectroscopy. Thermal desorption spectroscopy (TDS) has an ability for detecting small amounts of water[1]. It can also analyze hydrocarbons. However, we have a fear that we may not distinguish the hydrocarbons which exist on the silicon surface before setting TDS apparatus from ones which are adsorbed by oil back during pumping down. This problem always happens when we analyze a trace amount of carbon related contamination in the vacuum system.

Atmospheric pressure ionization mass spectroscopy (APIMS) has been used to investigate ppb-ppt level impurities in highly purified gas[2]. We made a TDS system using an APIMS as a detector (APIMS-TDS). The aim of this system is to detect hydrocarbons with high sensitivity without a fear of oil back from vacuum system and to perform in-situ observation of reactions on the silicon surface under flowing gases.

This paper reports the detection of hydrocarbons on silicon wafers by APIMS-TDS after HF-cleaning, and the combustion of hydrocarbons during thermal oxidation. The effects of hydrocarbons on heating process are also mentioned.

EXPERIMENTAL

Samples were cut to 2 cm x 5 cm from 4-inch n-type silicon (100) wafers both side of which were mirror polished. After RCA cleaning, the samples were dipped in 1% HF solution and rinsed in de-ionized water. After this treatment, the samples which were intentionally contaminated by acetone and ethanol were also prepared.

Ionization potentials of hydrocarbons are lower than that of argon gas. If hydrocarbons desorb from the silicon surfaces in argon gas, they are detected by APIMS. The sample was heated programmably at 20℃/min from room temperature to 1000℃ in a quartz tube as shown in Fig. 1. The quartz tube was piped to the APIMS apparatus by a 1/4-inch diameter, 40-inch long SUS316 electro-polished (EP) tube using the ultra-clean-gas-piping method[3]. The temperature of this EP tube was controlled at 120℃. 1 l/min of highly purified argon gas supplied through a zircon getter type purifier flowed during measurement. The concentrations of all impurities in the argon gas were less than 5 ppb. In order to distinguish it from the background spectrum, the APIMS-TDS spectrum was measured by means of the magnet sample transport system[1].

APIMS-TDS analysis of the oxygen gas was also carried out in order to investigate the reaction of the hydrocarbons during thermal oxidation. When heated in oxygen, the hydrocarbons are burned in addition to desorption[4]. It was expected that the hydrocarbons on the silicon surface would disappear after oxidation but might remain when heated in the argon gas. After APIMS-TDS in argon gas and in oxygen gas, the surfaces were observed by RHEED to identify hydrocarbon related defects.

RESULTS AND DISCUSSION

Argon gas was purified for about one day after setting the sample in the quartz tube. 5-10 l/min of highly purified argon gas was initially passed in order to drive out the air components. The flow rate was then reduced to 1 l/min. Figure 2 shows the purification progress of argon gas in the APIMS-TDS system under 1 l/min gas flow. Moisture (H_2O^+, H_3O^+), carbon dioxide, carbon monoxide and ethylene which are derived from the air decrease gradually with time. The dew point also becomes low. H_3O^+ is a cluster ion which is formed by the reaction of $H_2O^+ + H_2O \rightarrow H_3O^+ + OH$. Consequently, H_3O^+ is observed when there is enough moisture for this reaction, i. e. 100 ppb in the gas[3]. After the argon gas becomes pure, the quartz tube is heated to 1050℃ twice at 20 hours and 22 hours to remove the adsorbants on the inner surface of the tube. The moisture comes out at this time.

Figure 3 shows the APIMS spectra after gas purification. This is the condition just before TDS analysis. Relative ion intensity (RI_x) is defined as the ratio I_x/I_t, where I_x is the ion intensity to note and I_t is the sum of the total ion intensities. The impurities observed in the purified argon gas are methane, moisture, oxygen, carbon dioxide and hydrogen which is observed by the forms of ArH^+ and Ar_2H^+. The concentrations of all impurities except hydrogen are below 5 ppb.

Spectra from the sample and background of the APIMS-TDS system were

measured from M/e=2 to M/e=100 to investigate the desorbed components. Figure 4 (a) and (b) shows APIMS-TDS spectra of the silicon surface cleaned by HF solution and the background. In the background, only the signals for argon, water, and hydrogen appear. H_2O^+, ArH^+ and Ar_2H^+ increase gradually with temperature. Ar^+ and Ar_2^+ hardly change. In the HF-cleaned surface, H_2O^+, H_3O^+, ArH^+ and Ar_2H^+ desorb with peaks, and spectra of other mass numbers appear corresponding to hydrocarbons. Ar^+ and Ar_2^+ decrease slightly in response to the increase of other spectra, because the sum of the totalion intensities of APIMS is almost constant.

The main spectra considered to correspond to hydrocarbons are shown in Fig. 5. Although the desorbed species have not yet been determined from these spectra, they begin to desorb at about 300℃ and some of them continue to desorb at 1000℃. This indicates that several kinds of trace amount hydrocarbons are adsorbing on the silicon surface before setting in the APIMS-TDS system.

Figure 6 (a) and (b) shows APIMS-TDS spectra of the HF-cleaned silicon surface in argon gas and TDS spectra in vacuum, respectively. Since the background of ethylene in the APIMS-TDS spectra is extremely small, spectra from the sample show clearly. On the other hand, the background of TDS spectra is pretty high because of the existence of trace nitrogen.

It is well known that HF cleaning causes a hydrogen-terminated silicon surface. The hydrogen is desorbed from the silicon (100) surface as hydrogen molecules by the reaction of $SiH_2 \rightarrow SiH + 1/2H_2$ at about 400℃, and $SiH \rightarrow Si + 1/2H_2$ at about 500℃. In APIMS-TDS spectra in argon gas, hydrogen appears with the forms of ArH^+, Ar_2H^+ and H_3O^+, as shown in figure 7. ArH^+ is formed by the two reactions of $Ar^+ + H_2 \rightarrow ArH^+ + H$, and $Ar_2^+ + H_2 \rightarrow ArH^+ + H + Ar$. Ar_2H^+ is formed by $Ar_2^+ + H_2 \rightarrow Ar_2H^+ + H$. The spectra of Ar^+ and Ar_2^+ have two small minimum values corresponded with two peaks of ArH^+ and Ar_2H^+. H_3O^+ occurs from $H_2O^+ + H_2 \rightarrow H_3O^+ + H$, which is different from H_3O^+ formation by the collision of H_2O^+ and H_2O. As ArH^+, Ar_2H^+ and H_3O^+ ions are generated from hydrogen, their spectrum figures are similar. The total volume of desorbed hydrogen is given by the sum of these spectra, as shown in Fig. 6(a). The relative volume of ethylene to hydrogen is about 1/100 in both APIMS-TDS and TDS. The increase in the background of hydrogen with temperature is small and the coincidence between signal and background at high temperatures is good in APIMS-TDS.

In inert gas and in vacuum, hydrocarbons might react with silicon to form silicon carbide in addition to desorption in the heating process. On the other hand, hydrocarbons might burn in oxygen to form carbon dioxide and water. There is about 100 times more hydrogen than hydrocarbons, and this also reacts with oxygen to form water. Therefore, if water is detected, it does not prove that hydrocarbons on the silicon surface burn in the oxygen. If carbon dioxide is detected, the proof that hydrocarbons burn in the oxygen can be found out. Carbon dioxide is detected by APIMS as CO_3^- ion in oxygen gas. Figure 8 shows the APIMS-TDS spectra of CO_3^- when oxygen is flowing. Samples of ethanol dip and acetone dip in addition to HF dip are also shown in the same figure. Hydrocarbons burn at 400-

600℃. These temperatures coincide with the ignition temperatures of various hydrocarbons.

Hydrocarbons on the silicon surface finish burning at 650℃. We compared a sample that was heated to 1000℃ in argon after heating to 650℃ in oxygen (Fig. 9 (a)) with one that was heated only in argon to 1000℃ (Fig. 9 (b)) by means of RHEED. RHEED observations were carried out after HF cleaning followed by heating to 1000℃ in the APIMS-TDS system. Only silicon (100) RHEED pattern is observed in (a). The other RHEED pattern which is thought to be based on the formation of silicon carbide and surface roughness is observed in (b). The same pattern was also observed on the sample that was heated in vacuum. Consequently, hydrocarbons on the silicon wafer may cause secondary contamination by the heating process except thermal oxidation.

SUMMARY

An APIMS-TDS (atmospheric pressure ionization mass spectroscopy-thermal desorption spectroscopy) system has been developed for analyzing hydrocarbons on silicon wafers. This system achieves high sensitivity observation of desorption of hydrocarbons without a fear of oil back contamination from a vacuum system. It is also able to investigate reactions of contamination with various flowing gases. Several kinds of trace hydrocarbons were adsorbed on the silicon surface after HF cleaning, and they were completely burned in thermal oxidation.

ACKNOWLEDGEMENTS

We would like to thank Prof. Kazuyuki Saito of the university of Aizu for his useful discussion and Dr. Satoru Kurosawa of NTT Interdisciplinary Research Laboratories for his continuous encouragement.

REFERENCES

(1) N. Yabumoto, K. Minegishi, K. Saito, M. Morita, and T. Ohmi., Semiconductor cleaning technol./1989, 90-9, Electrochem. Soc., 265 (1990).
(2) Y. Mitsui, T. Irie, and K. Mizokami., Ultra Clean Technol. Vol. 1, 12 (1990)
(3) N. Yabumoto, T. Amemiya, K. Kawai, T. Kimura, T. Shimono, T. Nakayasu, A. Nishina, Y. Mitsui, H. Mihira, and Y. Sakakibara, Automated Integrated Circuits Manufacturing, 92-8, Electrochem. Soc., 99 (1992).
(4) N. Kawamura and N. Yabumoto., to be submitted.

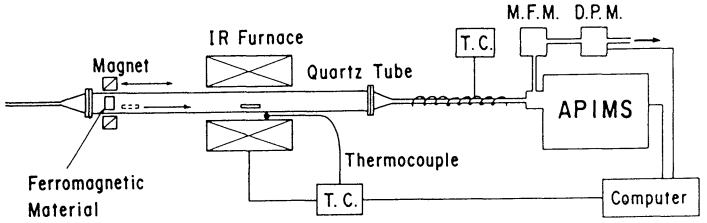


Fig. 1 APIMS-TDS system.

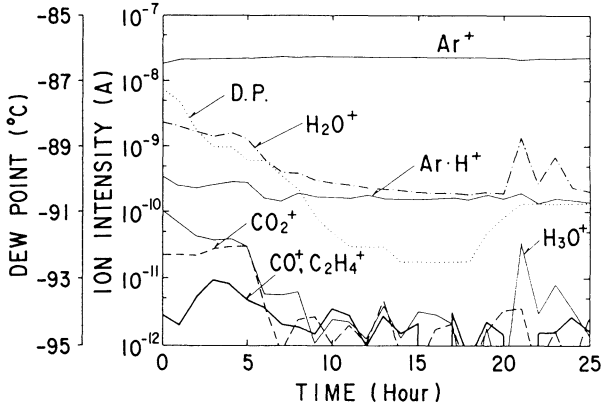


Fig. 2 Purification of argon gas in the APIMS-TDS system.

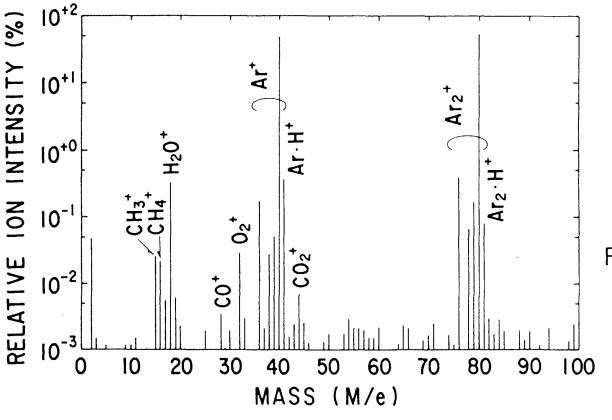


Fig. 3 APIMS spectra after gas purification. This condition corresponds to just before TDS analysis.

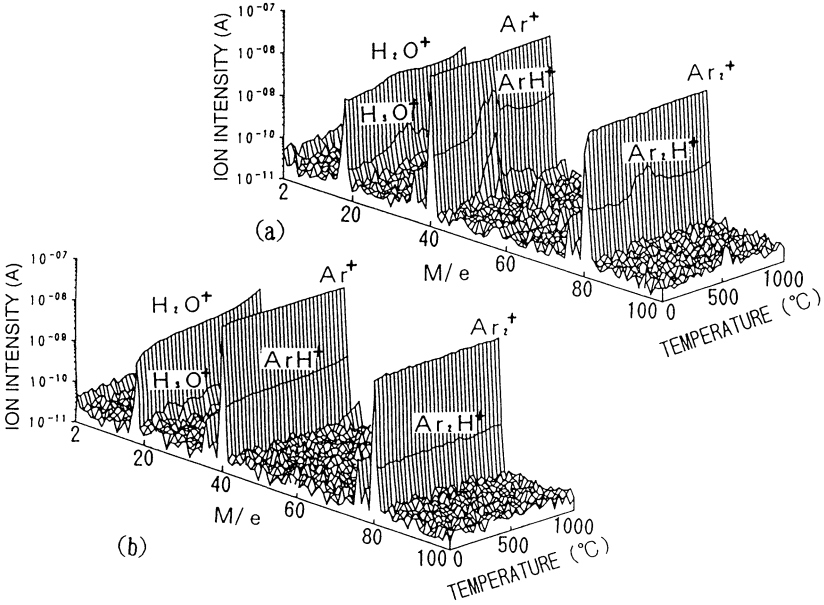


Fig. 4 APIMS-TDS spectra of (a) HF-cleaned silicon surface and (b) background. M/e=2-100, Temperature=RT-1000°C.

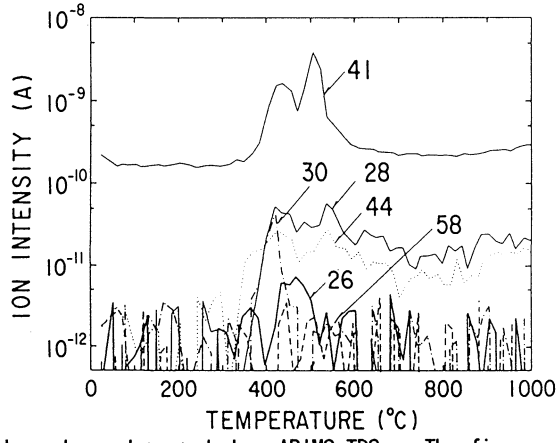


Fig. 5 Hydrocarbons detected by APIMS-TDS. The figures are mass numbers.

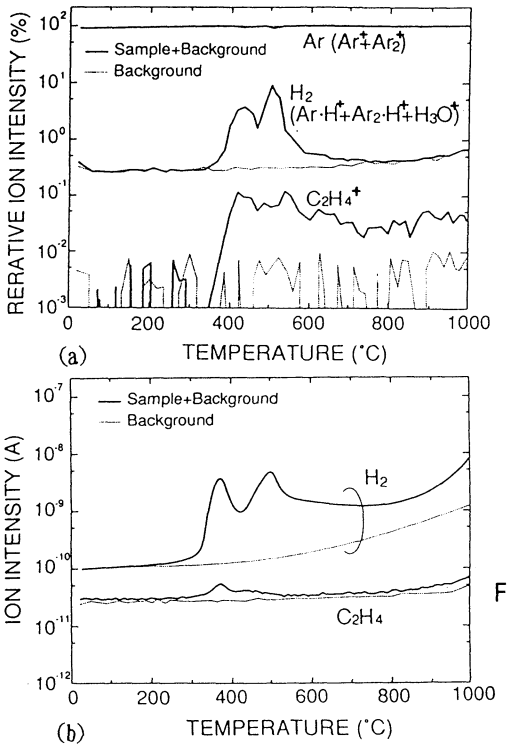


Fig. 6 Hydrogen and ethylene detected by (a) APIMS-TDS and (b) TDS.

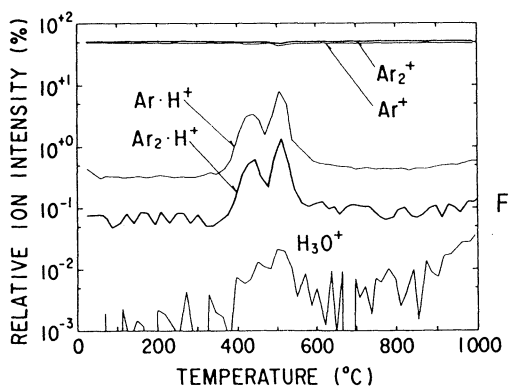


Fig. 7 APIMS-TDS spectra in argon gas related to hydrogen appeared with the forms of ArH^+, Ar_2H^+ and H_3O^+,

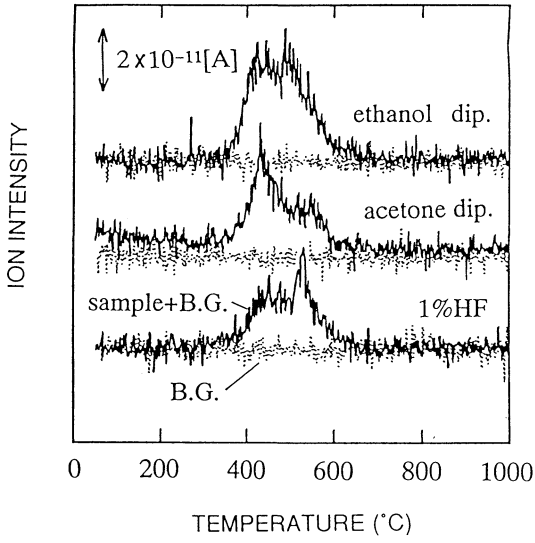


Fig. 8 APIMS-TDS spectra of CO_3^- measured under flowing oxygen.

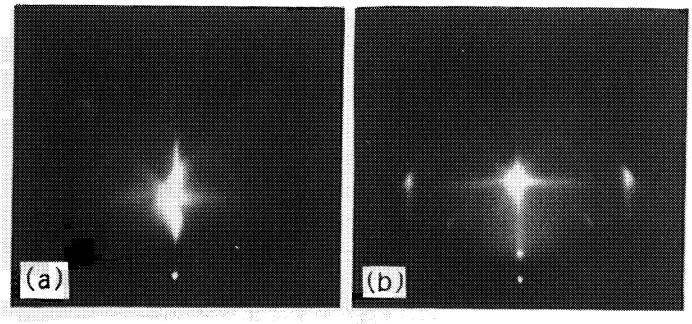


Fig. 9 RHEED pattern of (a) the silicon surface heated to 1000℃ in argon after heating to 650℃ in oxygen and (b) the silicon surface heated only in argon to 1000℃.

A SEMI-QUANTITATIVE METHOD FOR STUDYING PHOTORESIST STRIPPING

A. L. P. Rotondaro, M. Meuris, H. F. Schmidt, M. M. Heyns, W. Vandervorst,
C. Claeys, L. Hellemans* and I. Snauwaert*.
IMEC
Kapeldreef 75, B-3001 Leuven, Belgium.
*Lab. Chem. Biolog. Dynamica, KUL
Celestijnenlaan 200D, B-3001 Leuven, Belgium.

ABSTRACT

Sensitive light scattering measurements are used to quantify the amount of residues after photoresist stripping on different substrates. The high sensitivity of this technique provides unique information regarding the efficiency of several stripping procedures by identifying photoresist traces that could not be detected by other methods. The proposed procedure permits the optimisation of photoresist contamination removal steps like dry and wet stripping on a quantitative basis.

INTRODUCTION

The complete stripping of photoresist layers is a crucial step in achieving low contamination levels during wafer processing (1). Till now, the effectiveness of the photoresist removal has been only evaluated in a qualitative way due to the lack of a more quantitative technique which can measure the photoresist residues on the wafer surface. In this paper, the use of sensitive light scattering measurements is proposed as a tool to quantify photoresist residues.

EXPERIMENTAL

Standard I-line positive photoresist (UCB-JSR IX500) was spun on silicon, thermal oxide and LPCVD nitride substrates. The photoresist was exposed by a stepper using a dedicated test structure maskset. After the photoresist development, a high dose ion implantation (4 10^{15} ions/cm^2 80 KeV As) was used to cross-link the photoresist layer on some samples. This type of treatment makes the photoresist hard to be removed (2) as a "graphitization" of the top layer occurs (3).

Different stripping procedures were applied to the I/I and blank photoresist samples: dry O_2 plasma ash in a PRS800 reactor followed by a wet strip in a 4:1 H_2SO_4:H_2O_2 (SPM) solution, and dry or wet stripping only. Since the photoresist pattern is not transferred to the wafer surface, it is possible to detect the photoresist residues with sensitive light scattering measurements. To this purpose a Censor ANS-

100 machine is used. It detects the photoresist residues as light point defects (LPD's) in the ranges of 0.15 to 0.30 or 0.30 to 2.0 μm latex sphere equivalent (LSE). The photoresist residues can be identified by comparing the LPD distribution over the wafers with the pattern of the test structure maskset.

RESULTS AND DISCUSSION

The sensitive light scattering measurements performed after stripping the I/I photoresist layer clearly show the residues that are not removed by the different treatments (Fig. 1), as the pattern of the test structure maskset can be easily identified on the LPD plots. After O_2 plasma ashing for 45 min a residual layer is left on the wafers (Fig. 2a) and a subsequent treatment for 50 min in SPM at 95 °C is unable to remove the residues (Fig. 2b) (4). Furthermore, a cleaning for 10 min in a 0.25:1:4 $NH_4OH:H_2O_2:H_2O$ (SC1) bath at 70 °C after the stripping can not erase the photoresist pattern from the wafers surface either (Fig. 2c). The analysis of blank photoresist stripping presented better results when compared to the removal of the I/I layers. A 30 min O_2 plasma dry strip of these samples leaves a considerable amount of residues on the wafers (Fig. 2d) but the original photoresist pattern can hardly be recognised. A subsequent wet strip for 10 min in SPM at 80 °C can remove the remaining layer (Fig. 2e) and the particle contamination measured after the stripping treatments of the blank photoresist layer is reduced by a 20 min SC1 cleaning at 70 °C (Fig. 2f) (5) or by a 2 min immersion in a 0.5%HF:0.1%IPA solution (Fig. 3). Moreover, the samples with blank photoresist can be efficiently stripped by a 10 min immersion treatment in a SPM solution at 80 °C in agreement with earlier reported results for AZ-type resists (4).

In order to verify if the detected pattern on the stripped I/I samples results from the roughening of the silicon surface exposed to the ion beam a detailed haze mapping is performed on a region of 3.5 x 3.5 mm^2 of these samples. The obtained images (Fig. 4) show that the haze values at the areas that have received the ion implantation are comparable to the ones from the masked regions. This indicates that the detected patterns do not result from differences in roughness between photoresist protected and silicon exposed regions. Furthermore, it is possible to notice on the detailed haze maps that most of the light scattering occurs at the borders of the photoresist pattern (Fig. 4). The analysis of the samples with Atomic Force Microscope (AFM) has shown that very tiny residual walls are present on those borders (Fig. 5). These walls have 150 nm in width and only 20 nm in height which demonstrates the high sensitivity of the used technique for detecting residual features on the wafer surface. The samples were also investigated with Image Secondary Ion Mass Spectroscopy (Image-SIMS) and the results do not have shown any difference in the amount of carbon contamination between the photoresist stripped and the silicon open areas, as the residual walls are too small to be resolved by the technique.

The residues that were measured with the Censor after the stripping of the high dose I/I photoresist layer can not be detected by fluorescence microscope inspection or by low sensitivity light scattering particle measurements. This indicates that the high sensitivity provided by the Censor is fundamental for an in depth study of photoresist removal. The measuring technique has shown to be independent of the substrate on

which the photoresist layers are applied as it can precisely detect residues on silicon, thermal oxide and LPCVD nitride substrates.

It is also observed that the temperature of the SPM solution plays an important role in the particle cross contamination of the stripping bath. In this study, wafers that have received a half coating with a photoresist layer but no I/I were stripped for 10 min in SPM solutions at 80 or 95 °C. In the case of the treatment at 80 °C almost no particle cross contamination can be observed on the wafers (Fig. 6) whereas, when the SPM solution is heated at 95 °C a high particle contamination can be detected (Fig. 6). In both cases the particle contamination is reduced to values comparable to before the photoresist application by either a 20 min treatment in an SC1 solution at 70 °C (Fig. 6) or a 2 min immersion in a 0.5%HF:0.1%IPA bath (Fig. 6).

A similar experiment was conducted by covering half wafer with photoresist and performing a high dose I/I on the samples before they were stripped for 45 min in O_2 plasma and 20 min in SPM at 80 °C. The amount of residues left after stripping are strongly reduced in this case (Fig. 7) when compared to the mask exposed samples (Fig. 2b). This result agrees with what has been observed before as only one residual wall remains at the border of the previous photoresist layer (Fig. 7) for the half covered wafers. This indicates that to reproduce the amount of residues that can be generated during CMOS processing a maskset exposure should be applied instead of the half wafer or the total wafer covering procedure when studying I/I photoresist stripping processes.

CONCLUSIONS

The thorough analysis of different stripping processes can be conducted by quantifying the photoresist residues from the LPD plots. Sensitive light scattering permits to reveal residues that are not detected by other methods and thereby provides fundamental information. The results for high dose I/I and blank photoresist layers clearly indicate the residues that are not removed by the stripping procedures. This permits the optimisation of the treatments on a quantitative basis. It was observed that a residual layer remains on the wafers for the high dose I/I resist, whereas a clean surface can be obtained for the blank samples when standard dry and/or wet stripping procedures are used. The residues of the I/I layer have been identified to be tiny walls at the borders of the photoresist pattern. From the LPD plots it is possible to identify the critical steps regarding photoresist contamination so that further actions can be taken to completely remove the residues.

ACKNOWLEDGMENTS

A. L. P. Rotondaro would like to thank CNPq (Conselho Nacional de Desenvolvimento Científico e Tecnológico) Brazil, for financial support. The authors would like to acknowledge Prof. G. Declerck for continuous supporting this work.

REFERENCES

1. D. A. Peters and C. A. Deckert, J. Electrochem. Soc., 126, 883 (1979).
2. L. Peters, Semicond. Intern., 15, 58 (1992).
3. Y. Okuyama et al., J. Electrochem. Soc., 125, 1293 (1978).
4. L. H. Kaplan and B. K. Bergin, J. Electrochem. Soc., 127, 386 (1980).
5. S. D. Hossain, Extend. Abstr. 93-1 Spring Meet. Electrochem. Soc., 1143 (1993).

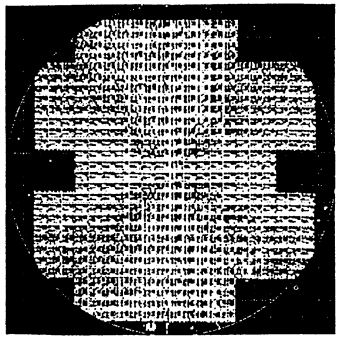


Figure 1: High dose I/I photoresist residues detected as LPD's by the Censor ANS-100 after dry stripping for 45 min in O_2 plasma, wet stripping for 50 min in SPM solution at 95 °C and cleaning for 10 min in SC1 at 70 °C.

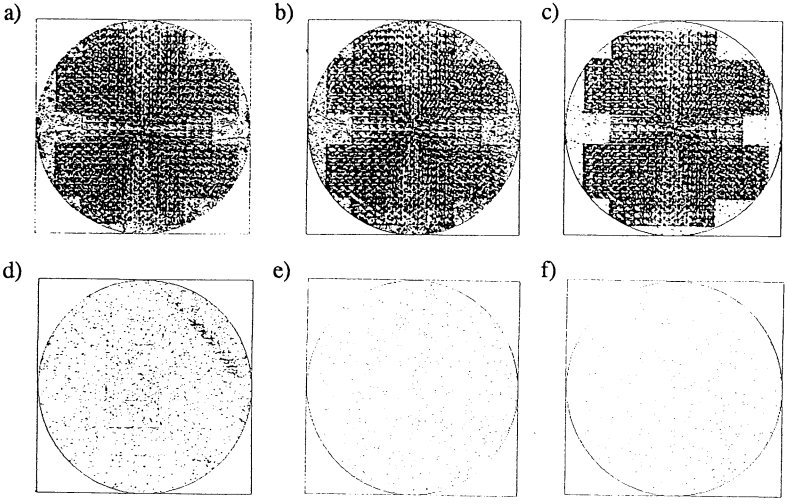


Figure 2: LPD plots from the Censor ANS-100: a, b and c are the results for high dose I/I photoresist; d, e and f are the results for blank photoresist. A and d show the residues after plasma dry ashing treatment; b and e indicate the effect of a further SPM wet stripping and c and f present the residues left after a final cleaning in SC1.

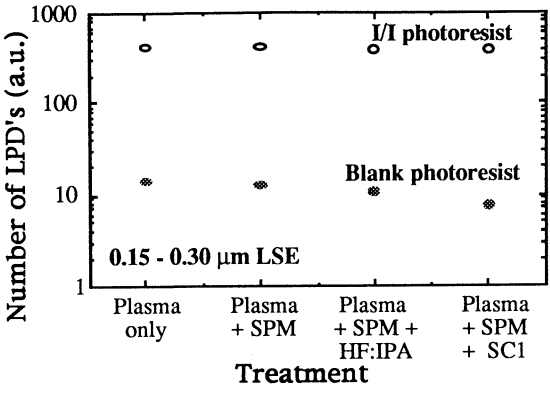


Figure 3: LPD's in the range of 0.15 to 0.30 µm LSE measured on silicon wafers after a dry stripping in O_2 plasma followed by a wet stripping in SPM and a final cleaning in SC1 at 70 ºC or in 0.5%HF:0.1%IPA. (o) high dose I/I photoresist and (•) blank photoresist.

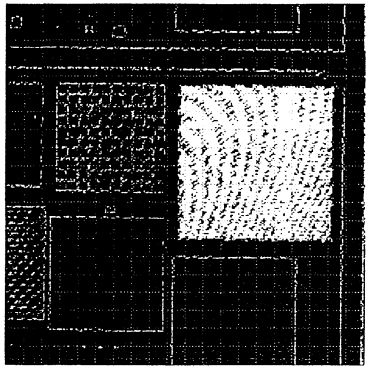


Figure 4: Typical haze detailed mapping of a region of 3.5 x 3.5 mm^2 measured by the Censor ANS-100 after 45 min dry followed by a 50 min SPM wet strip of an I/I photoresist layer.

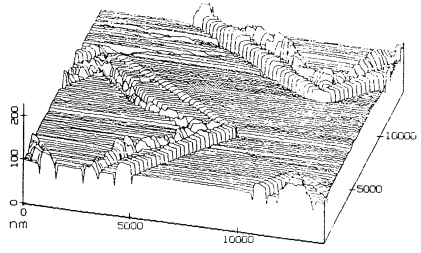


Figure 5: Atomic Force Microscope results from a region of 14 x 14 μm^2 of an I/I photoresist coated wafer that have been stripped for 45 min in O_2 plasma and 50 min SPM solution.

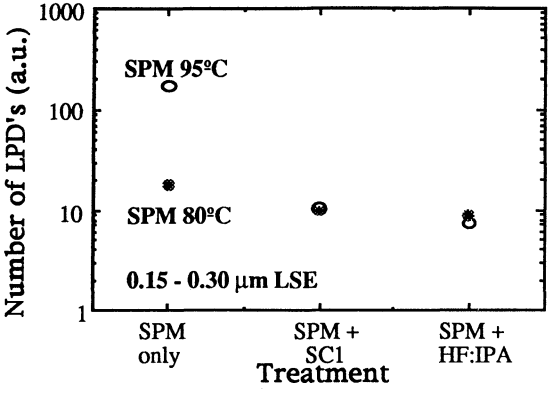


Figure 6: LPD's measured in the range of 0.15 to 0.30 µm LSE on silicon wafers coated with blank photoresist after stripping for 10 min in SPM at 95 ºC (o) or 80 ºC (•) and further cleaned for 20 min in SC1 at 70 ºC. or for 2 min in 0.5%:0.1% HF:IPA.

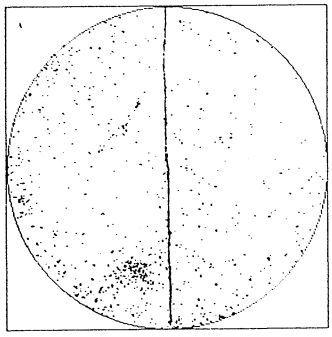


Figure 7: Typical LPD plot of a photoresist left half coated wafer that have received a high dose I/I, 45 min O_2 plasma dry strip and 20 min SPM at 80 ºC wet strip.

SURFACE PHOTOVOLTAGE MEASUREMENT OF CONTAMINATION INTRODUCED BY RESIST ASHING PROCESSES

A.M. Hoff
Center for Microelectronics Research
University of South Florida
4202 E. Fowler Avenue, CMR-ENB252
Tampa, FL 33620-5350

E.J. Persson
AT&T Microelectronics
9333 South John Young Parkway
Orlando, FL 32819

Surface photovoltage (SPV) measurements of minority carrier diffusion length in silicon have been used to study the incorporation of metallic impurities from resist as the result of plasma ashing and chemical clean-up processes. The SPV method provides quick feedback of the amount of metallic contamination introduced when ashing is performed and avoids the lengthy production of electronic test structures. Iron contamination levels above $10^{13}cm^{-3}$ have been observed and their effect on MOS electrical structures is shown.

INTRODUCTION

Productive resist removal processes must not only remove organic material, but in addition, metallic species present in the resist must be removed. Although resist ashing typically removes the organic species effectively, post-ash cleans are employed to remove the non-volatile species including metals. The traditional approach to study contamination in relation to process techniques has employed electronic test structures and surface chemical analysis techniques. For example the role of the plasma ash process in imparting a heavy metal dose to the wafer surface during resist stripping has been previously studied using such methods (1). SPV measurement of contamination provides a productive alternative which yields comparable information. In the case of resist removal and clean-up processes the interaction between materials and process techniques may be addressed in a rapid manner while avoiding the fabrication of electronic test structures and surface chemical analysis.

Among the metal species present in the positive photoresist used in this work, Fe, Cr, and Ni exhibit the highest concentration levels, with typical analyses indicating levels in the tens of PPB range. The upper specification limits for all metals have been dropping in recent years but these limits still extend roughly from 10 PPB to 100 PPB. Further, ultra-clean resist may not lead to contamination free substrates, as even "clean" resists have been shown to contaminate (1). As process complexities increase and device tolerance to metals decrease, robust process design will be required to manufacture next generation devices. Such designs will depend heavily on an understanding of the relationships between process techniques and contamination.

This study addresses conventional process techniques to demonstrate the utility of the SPV measurement toward quantifying the in-process contamination level of wafers at

various stages of a masking level loop. SPV measurements allow quick determination of contamination levels with limited additional processing. The SPV technique uses the silicon wafer properties to assess the presence of contamination (2). Before and after measurements of wafers can quantify the level of defects acting as recombination centers introduced by a given process. The measurement is performed by a non-contact probing apparatus which senses the response of the wafer surface potential to optical excitation. The spectral dependence of this response is used to determine the minority carrier diffusion length in the wafer. Iron is the principal contaminant present. Its concentration in the bulk of the silicon wafer, following the resist removal process and a thermal incorporation step, may be determined from diffusion length measurements. In this method, low temperature defect reactions are used which cycle Fe in boron doped silicon between a paired association with boron, Fe-B, and the isolated interstitial Fe_i (3). The Fe_i concentration is minimized by pair formation with boron over time periods of 1 day at room temperature or by a short 20 minute to 1 hour 80°C anneal. At this point, with pair concentration maximized, a maximum possible diffusion length (L) is measured. Interstitial iron is produced by pair dissociation achieved with a 200°C anneal followed by rapid wafer cooling to minimize Fe-B pair formation. The Fe_i species created by this process act as efficient recombination centers and result in the measurement of a minimum diffusion length value. Therefore, a typical iron concentration measurement involves a pairing process and L_i measurement followed by the thermal anneal to form Fe_i and a subsequent L_f measurement. For the purposes of this study [Fe], the iron concentration in the wafer, is calculated from (3):

$$[Fe] = 1.1 \times 10^{16} [L_f^{-2} - L_i^{-2}] \ (cm^{-3}) \qquad [1]$$

The defect behavior of the other metals present in resist is not well understood at present. For example, evidence exists that Cr may form pairs with boron and that this pair concentration may be modulated with temperature (4). Such processes are expected to effect low (PPT) iron concentration measurements but are not expected to significantly influence the results of the present work.

The purpose of this investigation, therefore, was to demonstrate the use of SPV measurements in the study of metallic contamination transferred to silicon by resist ashing and to assess the efficiency of subsequent cleaning methods in the removal of metallic species.

EXPERIMENTAL

In this study, p-type (100) silicon wafers with resistivity in the range of 5 to 50 Ω-cm were used. All wafers were cleaned by a modified "RCA1;(NH_4OH:H_2O_2:H_2O)": HF:$H_2$0: "RCA2;(HCl:H_2O_2:H_2O)" process in an automated spray tool (5). Two sets of experiments were performed. In the first, control samples were given a rapid thermal oxidation, RTO, for 2 minutes at 1150°C following cleaning. Other experimental samples were processed as follows: No chemical coating; HMDS coat only; HMDS+positive resist coat +soft bake. These wafers were processed through a batch photoresist ash and then split between no additional clean and a sulfuric-peroxide (SP) post-ash clean. The wafers were then combined and processed through RTO as above. SPV measurements for contamination determination were taken following RTO. The wafers were then stripped of oxide, cleaned by the "RCA" process above, and oxidized in a furnace gate oxidation process to a thickness of 150Å. Aluminum capacitors were then fabricated on all samples.

SPV mapping measurements were performed with the capacitors in place and electrical characterization consisting of breakdown distribution measurements were performed. The second experiment addressed the effects of post-ash cleans, the effect of thin oxide presence prior to resist coat and ash, and the effect of RTA ambient. Similar starting material was cleaned and oxidized to 150Å. The wafers were split into two groups and the oxide was removed from one group. This group received an additional spray "RCA" clean. The two groups were then recombined, coated with resist and plasma ashed as in experiment 1. The wafers were then split three ways and given: no additional cleaning; a spray "RCA(A)" clean, in which the HF step between the organic removal and metals removal sections of the process is excluded; or a spray sulfuric peroxide clean. The wafers were then processed in one of two rapid thermal environments, O_2 or N_2, at 1150°C for two minutes. At this point SPV measurements were performed to assess the contamination levels present in the processed wafers.

RESULTS AND DISCUSSION

In the first experiment of this study background process [Fe] levels, contamination induced by the batch ashing reactor, and the possibility that adhesion promotion chemistry may act as a contamination source were investigated. The experiment also compared the maximum levels of contamination obtained when samples were not cleaned following resist ashing with contamination present following a post-ash SP clean. The background [Fe] contamination levels for samples cleaned in "RCA" and then given an RTO averaged 7 x $10^{10}cm^{-3}$. Wafers not coated with resist but ashed with other coated wafers exhibited levels from $10^{12}cm^{-3}$ to $10^{13}cm^{-3}$ indicating a potential for vapor transport of contamination in the batch vacuum system. The majority of wafers in the group receiving no resist coat, or HMDS coat only followed by the ash process exhibited [Fe] in midrange $10^{11}cm^{-3}$. Further, SP clean appears to be ineffective in removing this contamination. This result is consistent with previous direct plasma work in which the authors found that the role of that energetic environment was to drive the contamination into the silicon beyond the reach of subsequent chemical cleans (1). These findings are summarized in Fig. 1.

The right half of Fig. 1 depicts the comparison between coated and ashed wafers which received no subsequent cleaning prior to RTO and similar wafers which were processed through an SP clean between ash and RTO. The average [Fe] contamination level of the wafers which were not cleaned following the O_2 ash is 1.9 x $10^{13}cm^{-3}$ whereas the SP clean removed surface contamination which led to a bulk value after RTO which was roughly 10%, 1.8 x $10^{12}cm^{-3}$, of the non-cleaned value. Assuming a uniform distribution of iron throughout the wafer (3) a surface concentration dose of 1 x $10^{12}cm^{-2}$ resulted from the O_2 ash process. Contamination levels as high as $10^{13}cm^{-3}$ may be above the threshold between good and poor device quality, lead to the formation of $FeSi_2$ precipitates (3), and reduce gate oxide quality (6). Breakdown characteristics of representative samples of C-V dots formed on these substrates following RTO oxide removal are shown in Fig. 2. Low field failures exist in all cases for contamination levels from $10^{11}cm^{-3}$ to $10^{13}cm^{-3}$ and the cumulative 50% failure value of the field varies from 10.3 $MVcm^{-1}$ down to 10 $MVcm^{-1}$ for the most contaminated wafers. Typical oxide defect densities for failure at or below 8 $MVcm^{-1}$ for [Fe] of $10^{11}cm^{-3}$, determined from the breakdown field data, were less than $20cm^{-2}$ whereas for $10^{12}cm^{-3}$ to $10^{13}cm^{-3}$ contamination levels, defect densities ranged from $25cm^{-2}$ to $80cm^{-2}$. In Fig. 2 the percent failing for the 1 x$10^{11}cm^{-3}$ versus oxide field is lowest overall. Below 5 $MVcm^{-1}$ the 1 x

$10^{13}cm^{-3}$ percent failure is highest and for fields greater than 5 $MVcm^{-1}$ this concentrations percent failure data is nearly the same as the 1 x $10^{12}cm^{-3}$ data. These results, although somewhat high, are consistent with a previously reported range of oxide defect densities wherein the contamination threshold observed was roughly $10^{13}cm^{-3}$ (6). In addition the present results support the earlier supposition of Zoth and Bergholz that an iron concentration of $10^{13}cm^{-3}$ was near a critical threshold dividing good from poor quality devices (3).

These results were obtained with bare silicon wafers as starting material and only one post-ash clean was performed. Fig. 3 presents a summary of the effects addressed by the second group of experiments in this study. Considering the first four cases of Fig. 3, oxide presence does appear to block some of the contamination from entering the silicon wafers. Pairwise comparisons between these averages over groups of wafers given no post-ash clean indicate a reduction in bulk [Fe] by a factor of two to three if thermal oxide were present under the resist during the ash process independent of the RTA ambient used. Further, over all of the cases investigated the oxidative anneal process appears to lead to lower levels of bulk contamination compared to the nitrogen anneal ambient. This latter point may be significant to technologists engaged in process improvement investigations in which sensitivity to low levels of surface contamination is an issue. Further study is required to assess the effects that RTA ambients including, for example, argon, nitrogen, or nitrogen/oxygen mixtures may have on the efficiency of surface contamination transfer into the bulk silicon.

On average, the spray processor "RCA(A)" cleans yielded slightly better results than the SP cleans in the same tool type. These results could be expected given the variation of chemical activity in the "RCA(A)", i.e. organic then metal removal, versus the SP clean. When "RCA(A)" and SP clean results are ratioed pairwise to the matching no clean cases with no oxide present, i.e. (RCA(A)/no clean), the post-ash process clean ((A) or SP) may be estimated to reduce the contamination transferred to the bulk silicon by approximately 90%. These results are consistent with the results of experiment 1 of this work. Similar treatment of the cases in which oxide was present indicate that roughly 80% of the contamination was removed by the two cleaning methods regardless of the RTA ambient. This result suggests that thin oxide is able to collect contamination but in this study the cleans could not remove it and the RTA process drove the contamination into the silicon. To minimize contamination reaching the wafer from resist ashing the amount of oxide needed to trap the contamination as a sacrificial layer to be removed before a subsequent thermal process should be studied.

CONCLUSIONS

In this study, direct plasma ash of photoresist was shown to contaminate both bare silicon and thermal oxides to levels higher than may be tolerated by future generations of devices. Further, conventional cleaning methods are not able to remove 100% of this contamination. The RTA ambient used to incorporate the contamination must be addressed in relation to the sensitivity desired in the experiment. These results were obtained using SPV techniques with limited post processing after the resist removal process. Hence, the time required to obtain meaningful results in process contamination and cleaning experiments may be shortened to hours and only one additional thermal process is required. The results obtained are quantitative and correlate to previous studies which employed the fabrication of electrical test structures and surface analysis techniques.

In summary, it should be noted that the resist processes studied in this work were rather benign when compared to more challenging processes such as high dose implant and plasma etch. Still significant potential for the introduction of contamination has been observed and should be the subject of additional study.

REFERENCES

1. S. Fujimura and H. Yano, in Plasma Processing/1987, G.S. Mathad, G.C. Schwartz, and R.A. Gottscho Editors, **PV 87-6**, p. 352, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1987).

2. J. Lagowski, P. Edelman, M. Dexter, and W. Henley, Semicond. Sci. Tech., **7**, p. A185 (1992).

3. G. Zoth and W. Bergholz, J. Appl. Phys., **67**, p. 6764 (1990).

4. K. Mishra, in Extended Abstracts/1992, **PV 92-2**, n426, The Electrochemical Society Softbound Proceedings Series, Pennington, NJ (1992).

5. W. Kern and D.A. Puotinen, RCA Rev., **31**,p. 187 (1970).

6. W.B. Henley, L. Jastrzebski, and N.F. Haddad, MRS Symp., **262**, p. 993 (1992).

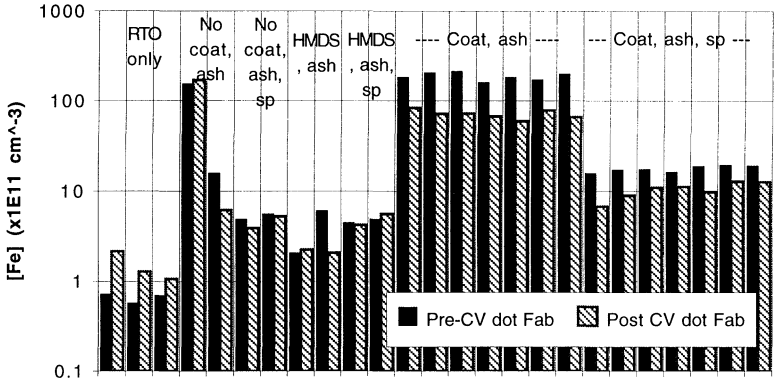


Fig. 1. Iron concentration (x 10^{11}cm^{-3}) versus process condition both before and after C-V dot fabrication

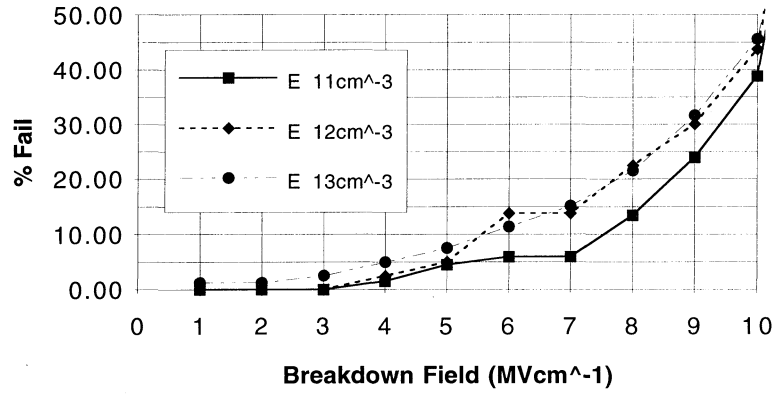


Fig. 2. Oxide breakdown percent failure, by average iron contamination level, versus oxide field. Field axis indicates bins for comparison between [Fe].

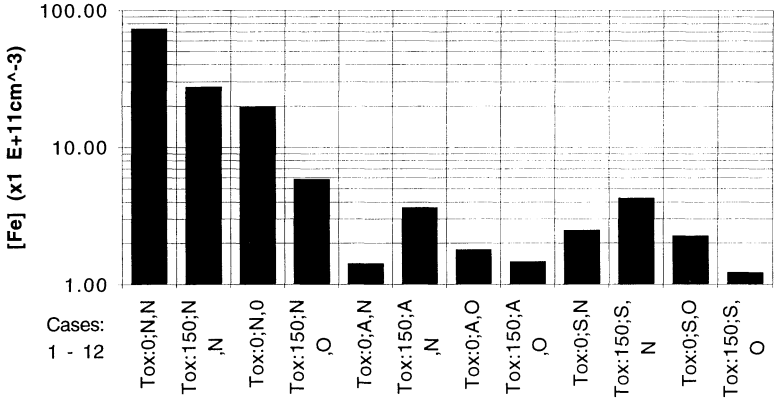


Fig. 3. Iron concentration (x $10^{11}cm^{-3}$) versus process case. Fields are: T_{ox}: 0Å or 150Å ; Clean: N=no, A=RCA(A), S=SP ; RTA Ambient: $O=O_2$, $N=N_2$.

AUTHOR INDEX

SUBJECT INDEX