CLEANING TECHNOLOGY IN SEMICONDUCTOR DEVICE MANUFACTURING

Proceedings of the Sixth International Symposium

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PREFACE

The Sixth International Symposium of Cleaning Technology in Semiconductor Device Manufacturing was held during the Fall Meeting of The Electrochemical Society in Honolulu, Hawaii, in October 1999. This Series of symposia was initiated in 1989 during the Society Fall Meeting in Hollywood, Florida. Since then, the "ECS Cleaning Symposium" has been established as a prime forum for the exchange of technical information regarding advanced wafer cleaning technology. The meeting in Honolulu was no exception in this regard. The number of participants, as well as the quality of papers presented, was a reflection of the continued need for improvement of surface preparation methods to meet the yield challenges of the semiconductor industry.

With very few exceptions, papers presented during the symposium are included in this volume. The papers are divided into several sections with the most voluminous one devoted to front end of the line (FEOL) cleaning. The number of papers in this section indicates that much attention is still focused in improving these front end processes. It also testifies to the fact that a large amount research and development is still needed not only to improve performance of FEOL cleans , but also to optimize these operations to lower the cost of ownership (COO) through the use of less chemicals, less water, employing simpler chemistry, yet having lower defect levels,

The papers presented in the section on back end of the line (BEOL) cleaning shows the growing need to develop copper cleaning technology that is compatible with the low density, low k interlayer dielectrics common today on advanced processes. A separate section is devoted to the problems of resist stripping and responds to the growing need to control side wall polymer removal . A section on the fundamentals of particle removal yields insight on how to meet the decreasing defect levels that technology roadmaps are requiring. Finally, there is a section on analytical studies, that further contributes to the technical literature on a range of subjects, important to wafer cleaning.

We would like to take this opportunity to thank all symposium authors and participants who turned this symposium into yet another very informative and productive gathering of researchers and engineers involved in wafer cleaning technology in advanced IC manufacturing. In particular, we would like to thank our colleagues who assisted us in editing this volume and who chaired the symposium sessions. Moreover, our thanks are due to the invited speakers for their excellent contributions and to all the participants for their encouragement and support. We are looking froward to the next symposium in this series in the Fall of 2001.

Richard E Novak
Jerzy Ruzyllo
Takeshi Hattori

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FACTS ABOUT THE ELECTROCHEMICAL SOCIETY, INC.

The Electrochemical Society, Inc., is an international, nonprofit, scientific, educational organization founded for the advancement of the theory and practice of electrochemistry, electrothermics, electronics, and allied subjects. The Society was founded in Philadelphia in 1902 and incorporated in 1930. There are currently over 7,000 scientists and engineers from more than 70 countries who hold individual membership; the Society is also supported by more than 100 corporations through Contributing Memberships.

The Technical activities of the Society are carried on by Divisions and Groups. Local Sections of the Society have been organized in a number of cities and regions. Major international meetings of the Society are held in the Spring and Fall of each year. At these meetings, the Divisions and Groups hold general sessions and sponsor symposia on specialized subjects.

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FRONT END OF THE LINE (FEOL) CLEANING

ADVANCED CLEANING STRATEGIES FOR ULTRA-CLEAN SILICON SURFACES

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ABSTRACT : A lot of effort was spent over the last years to develop cleaning strategies that combine a high performance with a low chemical and DI-water consumption. Some recent findings in this area are presented in this paper. The effect of metal contamination on the gate oxide integrity is investigated. The performance of a simplified cleaning process (IMEC-clean) in a prototyping line is illustrated. The importance of the final rinse step on the overall metal contamination level and the effect of the presence of a thin chemical oxide prior to oxidation are shown.

1. INTRODUCTION

Cleaning is the most frequently repeated step in IC-production. Over the last years a lot of research effort was directed towards the development of novel cleaning techniques that are more effective, inexpensive and have a lower environmental impact. After a brief discussion of the effect of metal contamination on the gate oxide integrity, some recent advances in the preparation of ultra-clean surfaces will be discussed.

2. EFFECT OF METAL CONTAMINATION

The behavior of several contaminants which are commonly found in cleanroom materials (Na, Mg, Cr, Zn, Ni, V, Mn) or may be used in future technologies (Ti, Sr, Ba, Pt, Co, Pb) was investigated [1]. Silicon wafers were cleaned using an IMEC-clean to obtain a contamination-free reference hydrophilic surface, i.e. below the detection limit of the VPD-DC-TXRF (about 5.10^8 at./cm^2). The contaminants were applied by spinning an acid solution (0.5M HNO_3 or 0.5M HCl) with 0.1 ppm or 1 ppm of metal added, resulting in metal contamination levels of approximately 10^{12} at./cm^2. For some metals also wafers with contamination levels of 10^{11} at./cm^2 were prepared. Subsequently 4.5 nm oxides were grown in a dry O_2 ambient at 800°C. It was observed that the contaminants used in this study do not lead to a significant difference in the final oxide thickness, except for Na which is known to enhance the formation of crystalline SiO_2 [2]. In most cases the contamination level decreases after oxidation. Figure 1 shows the amount of metals remaining in the oxide. The earth alkaline metals seem to remain mostly in the oxide layer, despite their high vapor pressure at 800°C, as well as high solid solubility. The remaining fraction of the transition metals depends on their solubility and diffusion constant in the silicon at the oxidation temperature. The solubility and diffusion constant of the various metals at 800°C are shown in figure 2. Metals can diffuse into the silicon substrate when their solubility and diffusion constant are sufficiently high. Significant levels of Na, Zn and Pb were found on clean wafers included during oxidation of contaminated wafers. This is in accordance with the relatively high contaminant loss after oxidation, and with the relatively high

vapor pressure for these elements. No significant cross contamination was found for other elements.

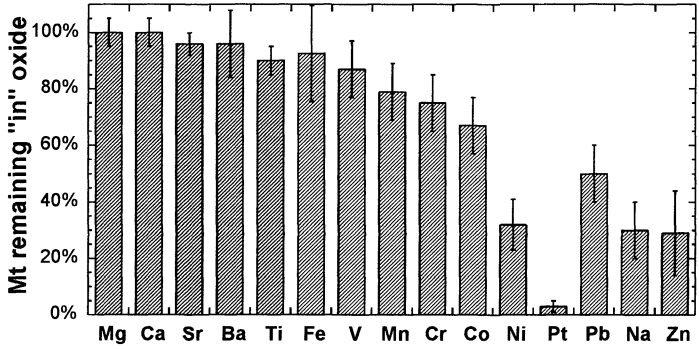

Figure 1 : Metal contamination remaining in the oxide after oxidation in dry O_2 at 800°C to a nominal thickness of 4.5nm. The metal remaining in the oxide is defined by the metal contamination in the oxide after oxidation (VPD-DC-TXRF) divided by the metal contamination on the surface before oxidation.

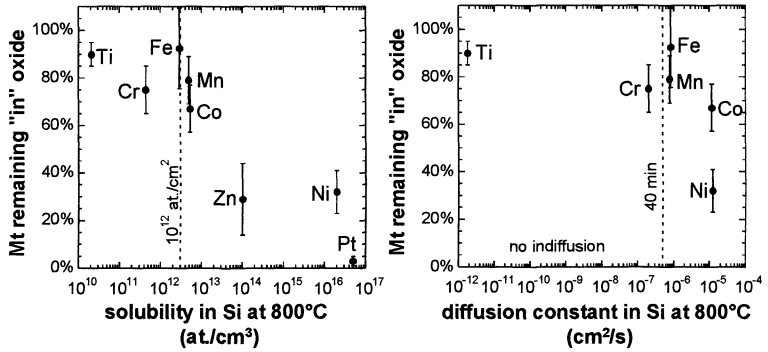

Figure 2 : Solubility and diffusion constant in Si for various metals. Solubility data from E.R. Weber, Appl. Phys. A 30-1 (1983).

The effect of the contaminants on the gate oxide integrity was evaluated by ramped breakdown (E_{BD}) tests. The results are summarized in figure 3. Capacitors with sizes ranging from 0.13 mm^2 to 4 mm^2 were used. For each condition two duplicate wafers were measured with at least 130 capacitors on each wafer. Defect densities were calculated with a yield criterion of 11MV/cm. All clean reference wafers have a very low defect density and, consequently, a high yield that is close to 100% for the 4 mm^2 capacitors. For the transition metal-contaminated wafers a varying defect density is found. Especially V, Ni and Co cause high defect densities, while Mn, Zn and small amounts of Ru do not have such a large impact. The group II elements tested in this experiment all cause a high defect density and smaller capacitors had to be used in the breakdown experiments. Special attention must be given to the effect of Ca, since this is a very commonly observed contaminant after cleaning and final rinsing, even in state-of-the-art production environments. It

was observed that even levels of 10^9 to 10^{10} Ca.atoms/cm^2 cause a noticeable degradation of the gate oxide integrity. These results indicate that the Ca-level on the Si-surface prior to gate oxidation must be controlled to very low levels.

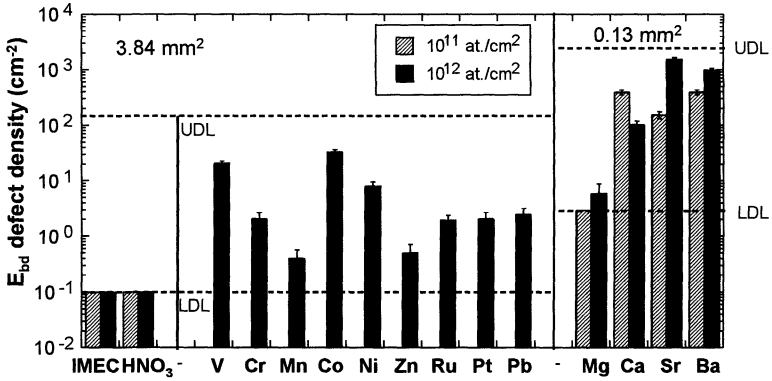

Figure 3 : E_{BD} yield at 11 MV/cm obtained from ramped voltage measurements for the wafers with various contaminants. The oxide was grown at 800°C to a thickness of 4.5 nm. Upper and lower detection limits of the E_{BD} defect density are determined by the size and number of the capacitors used.

3. WET CLEANING ROADMAP

The RCA-clean [3], first published in 1970, still forms the basis for most front-end wet cleans. A typical RCA-type cleaning starts with an SPM-step (H_2SO_4/H_2O_2) followed by a dip in diluted HF. The SC1-step ($NH_4OH/H_2O_2/H_2O$) removes particles while the SC2-step ($HCl/H_2O_2/H_2O$) is a metal removal step. The RCA-clean evolved at a time when the scale of the IC industry was much smaller and environmental restrictions were not yet strongly present. In view of the relatively large volume of high-purity chemicals and DI-water used, improved cleans were developed that have a lower environmental impact, are less expensive and can meet the increasingly more stringent process demands. A possible roadmap towards more efficient cleaning sequences is shown in figure 4.

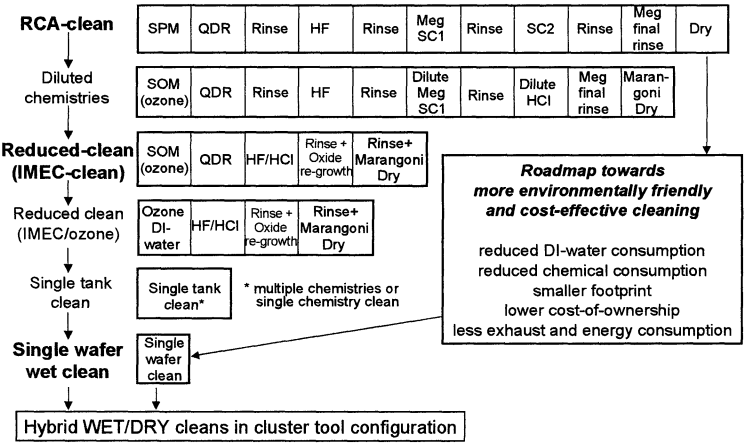

Figure 4 : Suggested roadmap towards cleans with lower chemical and DI-water consumption.

By using diluted chemistries in an RCA-type clean, a significant reduction in chemical consumption can be obtained. For example, it was shown that strongly diluted HCl mixtures are as effective to remove metals than the standard SC2 solution [4], but with a much lower chemical consumption. A large decrease in chemical and DI-water consumption can be obtained by using cleaning sequences with a reduced number of steps, such as the IMEC-clean [5]. Further reductions in chemical and DI-water consumption are possible by single chemistry and single wafer cleans. The development of hybrid wet/dry cleans that can be integrated into a cluster tool is very important in process steps where precise control of the chemical condition of the wafer surface is needed.

4. IMEC-CLEAN CONCEPT

The IMEC-clean concept [5] has been investigated in more detail over the past years. This cleaning concept is based on a two-step cleaning approach and is schematically illustrated in figure 5. In the first step of this clean, the organic contamination is removed and a thin chemical oxide is grown. An H_2SO_4/O_3 mixture can be used to this purpose but also ozonated DI-water can effectively remove organic contamination. The use of ozonated DI-water results in a further reduction of the chemical consumption and, even more importantly, of the DI-water consumption, since the difficult rinse step after the sulfuric acid bath [6] is avoided.

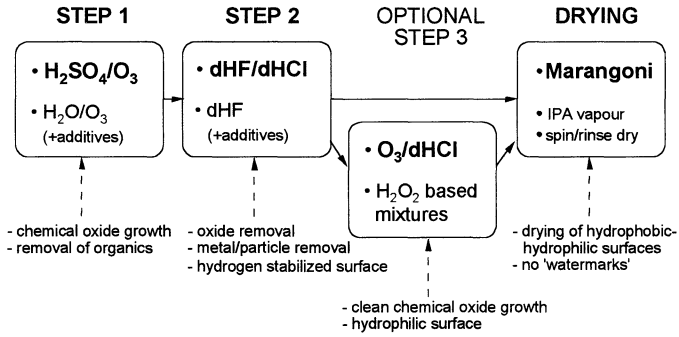

Figure 5 : Schematic illustration of the IMEC-clean concept.

In the second step of the IMEC-clean the chemical oxide is removed, simultaneously removing the particle and metal contamination, in a diluted HF/HCl mixture. This mixture suppresses the Cu-outplating that is commonly observed in metal contaminated HF-baths. This outplating is an electrochemical process that is limited by the minority carrier concentration at the surface and, therefore, depends on the illumination conditions [7]. The addition of small amounts of chloride to the HF increases the copper deposition due to a catalyzing effect. When a sufficiently large amount of chloride is added, as used in the proposed mixture, no copper deposition is observed on the Si-surface [8]. When a hydrophobic surface is required and a good drying technique for mixed hydrophobic/hydrophilic surfaces is available that does not generate drying spots, no further surface treatment is required. In case a hydrophilic surface is preferred, a third step can be added to re-grow a thin passivating oxide layer. Ozonated mixtures, such as $dHCl/O_3$, can be used to make the Si-surface hydrophilic at low pH values in order to avoid the re-introduction of metal contamination. Hydrophilic surfaces are typically easier to handle without particle recontamination and, therefore, generally provide better results.

5. IMPLEMENTATION OF THE IMEC-CLEAN

The IMEC-clean was implemented in an automated wet bench in the IMEC-prototyping line. The IMEC-clean recipe is summarized in table 1. The sulfuric acid/ozone mixture (SOM) at 90°C is followed by a quick dump rinse with hot and cold DI-water. The dilute HF (0.5%) mixture acidified with 0.5 molar HCl (pH=0.5) used in the second step is not only effective in reducing the risk of Cu outplating onto the silicon, as explained previously, but is also effective for other metal contaminants. Experiments showed that when the HF/HCl bath is spiked with a cocktail of 12 metals (Sr, Zn, Cr, Fe, Ti, Al, Ta, Ni, K, Mg, Ca and Cu), each at a level of 100 ppb in weight, the metal surface concentration on oxide and bare silicon wafers is still below 10^{10} at./cm^2. The final rinse includes ozonation of the DI-water to re-grow a chemical oxide, acidified with HCl to a pH=2 and the addition of megasonics. The ozone in this step can be left out when a hydrophobic surface (HF-last) is preferred. Finally a Marangoni drying is used at a pH=3.

Step 1	H_2SO_4/O_3	90°C	5 min
	3 quick dump rinse (hot/cold)	60°C/20°C	8 min
Step 2	dHF(0.5%)/dHCl(0.5M)	22°C	2 min

Step 3	Final rinse + O_3/HCl (megasonic energy)	20°C	10 min
Drying	Marangoni drying (with HCl addition)	20°C	8 min
Total cleaning time :			32 min

Table 1 : IMEC-clean recipe implemented in the automated wet bench.

In the HF/HCl step about 2 to 3 nm of the oxide is etched. This etching will break the Van der Waals force and allows the liquid to penetrate between the particle and the substrate. The HCl addition keeps the pH below the iso-electric point of silicon oxide, which ensures the particle removal by repulsive zeta potentials. As will be explained later in this paper, the low pH during rinse and dry is a very effective and low-cost solution to reduce recontamination of metals during these steps. Another reason for the low-pH rinse and dry is to keep the repulsive force of the zeta potentials on the particles and surfaces after the HF-dip. The HF will wet the surface and the particle (undercutting the particles), but the particles will stay very near the surface. By keeping this low pH during rinse and dry, no particle recontamination will occur [9].

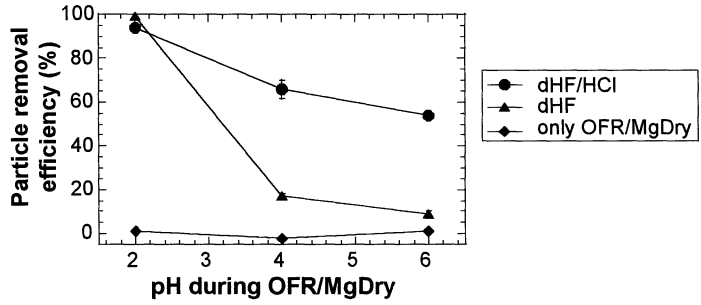

Figure 6 : Particle removal efficiency for alumina particles (0.1-0.3 μm) as a function of pH in the rinsing step of the IMEC-clean.

In figure 6 alumina particles were used to contaminate oxide surfaces. In the control experiment (rinse and Marangoni dry), no particle removal occurred. When an IMEC-clean is used and the rinse and dry is done at low pH, high particle removal efficiencies are obtained. However, when the pH during rinse and dry is approaching the more neutral pH, particle recontamination is observed. This is due to the fact that above pH=3, the potential of the oxide surface is negative while the zeta potential of alumina is still positive, resulting in a larger attractive force when the pH rises. It is therefore advised to use a low pH during the rinse. Adding megasonics to the final rinse step, gives a further improvement to the overall particle performance of the IMEC-clean [10].

6. PERFORMANCE OF THE IMEC-CLEAN

Very low metal contamination levels were consistently achieved with the IMEC-clean. A typical result is shown in table 2. Low final metal contamination levels were observed even on intentionally contaminated wafers.

metal	blank metal conc.	after IMEC clean

	(10^{10}at/cm^2)	(10^{10} at/cm^2)
K	<0.25	<0.25
Ca	9.65	<0.26
Cr	<0.08	<0.08
Fe	14.13	<0.04
Co	<0.17	<0.17
Ni	0.06	<0.01
Cu	<0.07	<0.07
Zn	3.92	0.12±0.02
Ta	0.09	0.04±0.01

Table 2 : Typical metal contamination (measured with VPD/DSE-TXRF) after an IMEC-clean sequence. The results are an average for 6 wafers divided over 3 cleans. In this test standard 1 ppb-grade chemicals were used.

The particle removal efficiency was tested in detail by using intentionally contaminated wafers with various types of particles on various substrate types. The results are presented in table 3. High particle removal efficiencies are found for all combinations of particle type and substrate surface. Also indicated in this table is the amount of material etched during the cleaning sequence. The 3.2 nm of thermal oxide which is etched during the IMEC-clean is comparable to the etching in typical RCA-cleaning sequences using heated SC1 solutions. Note, however, that the etching of TEOS is much faster than on thermal oxide and only a few seconds HF-dip is sufficient to remove particles from this material with a much smaller amount of etching.

substrate	**etching (nm)**	**particle removal efficiency (%) type of particles**		
		Si_3N_4	**Al_2O_3**	**silica**
bare silicon		100	100	99
TEOS film	12.8	99	100	100
thermal oxide	3.1	100	100	100
LPCVD nitride	0.8	98	100	94

Table 3 : Particle removal efficiency of the IMEC-clean for various particles on various substrates. The initial particle count varied between 1500 and 2500 particles per wafer. Also shown is the amount of material etched during the clean.

The IMEC-clean was found to introduce no Si-surface roughening, in contrast to the RCA-clean where the combination of chemical oxidation and etching during the SC1-step can cause Si-surface roughening. This is illustrated in the AFM results shown in figure 7.

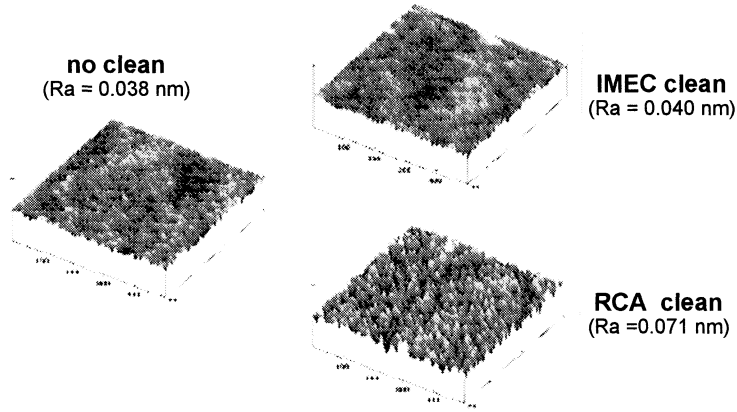

Figure 7 : Si-surface roughness (as measured with AFM) of the initial Si-surface ('no clean'), after an IMEC-clean and after an RCA-clean. The Ra value obtained from these measurements is also shown. The scale is: 500 nm XY - 1 nm Z

The performance of the IMEC-clean as implemented in the IMEC-prototyping line was monitored over an extended period of time. Two-weekly measurements of the final metal surface contamination were performed using VPD-DSE-TXRF. The results for Ca, Fe, Cu and Zn are shown in figure 8. The results indicate that very low levels of metal contamination, close to or below the detection limit of the analysis technique, were always obtained. This was also true for the elements not shown in this figure. This demonstrates the robustness of this clean in terms of metal contamination, even in an experimental environment were various new materials and processes were introduced during the time period of these results.

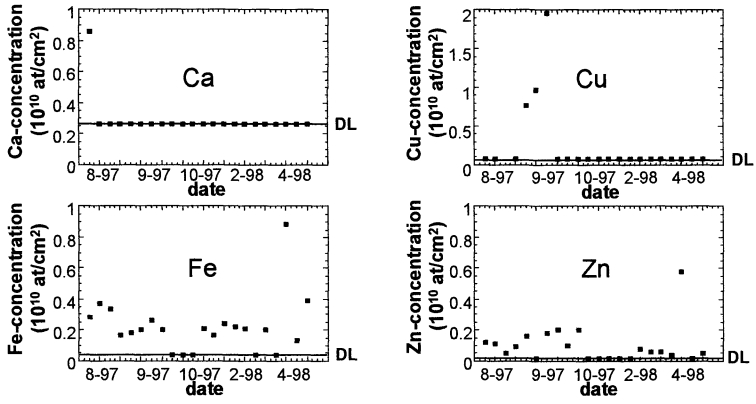

Figure 8 : Results of the two-weekly metal check of the IMEC-clean in the IMEC-prototyping line. Results are shown for Ca, Fe, Cu and Zn.

Also in terms of particle performance, excellent results were consistently achieved. The daily particle monitoring, shown in figure 9, show an essentially particle-neutral proc-

ess (mean : -2 ± 7 at $Ø_{LSE}$ > 0.2 μm). These results illustrate that the IMEC-clean is a very robust process with an excellent day-to-day performance.

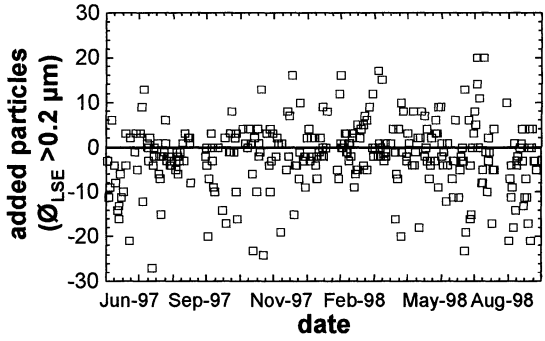

Figure 9 : Daily particle check of the IMEC-clean in the automated STEAG wet bench located in the IMEC-prototyping line. Particle densities were obtained using the TENCOR 6400.

Capacitor structures were made to investigate the gate oxide integrity after the IMEC-clean. The oxidations were performed in a clustered batch furnace. No Cl-containing species that could mask the effects of low levels of contamination were used in the oxidation ambient. Tests were performed on a weekly basis. The largest capacitor area available was 16 mm^2, which limits the lower detection limit of the defect density that can be measured with sufficient statistical significance to about 0.2 defects/cm^2. The defect densities, measured at 12 MV/cm in a ramp breakdown test, were consistently below or close to this detection limit. This illustrates that the IMEC-clean can be used as a cost-effective replacement for the RCA-clean with the advantages of much lower chemical and DI-water consumption, leading to important environmental and cost savings.

7. EFFECT OF CHEMICAL OXIDE ON THIN OXIDE GROWTH

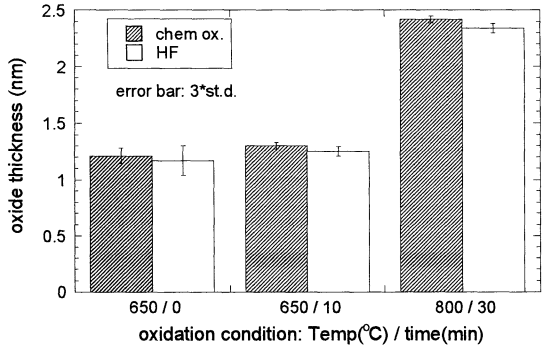

Figure 10 : Oxide thickness and thickness variation (3σ) for wafers without a chemical oxide (HF-last) or with a chemical oxide (SC2) prior to oxidation for various oxidation temperatures and oxidation times. Oxidations were performed in dry 10% O_2/N_2.

Advanced CMOS technologies require the growth of thin gate insulators with precise thickness control. When a HF-last process is used no chemical oxide is present on the wafer prior to oxidation. Other cleaning processes typically leave a thin chemical oxide on the silicon surface with a thickness that can be a significant fraction of the final thermal oxide thickness. The effect of the presence of this layer on the oxide thickness control and uniformity was investigated. Results are shown in figure 10. It is observed that on a HF-last wafer a thin thermal oxide of about 1.17 nm is grown during ramp-up in diluted oxygen. The presence of a thin chemical oxide, with an estimated thickness of about 0.6 nm, does not significantly influence this oxidation process. The error bars, which show the thickness variation (3σ) over the wafer, indicate in this experiment a slightly better uniformity for the wafers where a chemical oxide was present prior to the oxidation.

8. RINSING

Cleaning sequences normally end with rinsing and drying the wafers. Wafers are rinsed in water to remove reaction products and residual reactants. High purity DI water at near-neutral pH – depending on dissolved CO_2 – has been demanded for this application. Rinsing clean wafers in ultra-pure water results in a built up of metallic surface contamination [11, 12] on hydrophilic surfaces, particularly for Ca. Figure 11 shows the results of a first order model of a designed experiment in which the rinse water in the Marangoni drier was intentionally spiked with 2 w-ppb of Ca and varying amounts of HNO_3 [13, 14]. These final rinses were performed directly after immersion of clean wafers in either an SC1 or an SC2 mixture. It was found that the metal surface concentration drastically increases with decreasing HNO_3 spiking. The higher concentration found on the SC1-last cleaned wafers with respect to SC2-last cleaned wafers was attributed to the carry over of basic SC1 chemicals into the final rinse and dry tank.

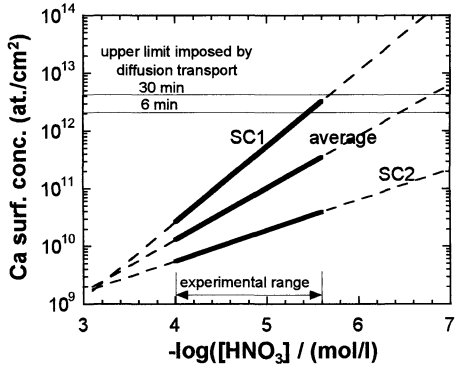

Figure 11 : Dependence of the final Ca surface concentration (equilibrium values) as a function of pH of the final rinse solution and of the last cleaning step prior to the rinsing. The rinse water was spiked with approximately 2 w-ppb of Ca.

Eperiments were performed to study the deposition of metallic contamination from weakly acidified rinse water onto hydrophilic silicon surfaces in more detail [13-15]. Wafers first received an IMEC-clean as a pre-clean ending with hydrophilic Si-surfaces from the O_3/HCl step. Different contaminants were applied : Al, Ba, Ca, Cr, Cu, Fe, K, Ni, Sr and Zn. The acidic solutions were made with HNO_3 and the wafers were exposed to solutions containing metallic contamination at pHs between 3 and 5.6 for various times. After

exposure to the solution, wafers were dried using a Marangoni dryer or spin dryer. Metal surface contamination was measured using Total X-Ray Fluorescence (TXRF) and Atomic Absorption Spectroscopy (AAS), pre-concentrating the metal using vapor-phase decomposition/droplet collection. It was found that the surface concentrations of the various metal contaminants can be related to the basic properties of the ions, namely the ratio of ion charge to ionic radius [15]. This is shown in figure 12 for a pH of 3.0 and 5.6. Ions existing as uncomplexed ions follow this trend relatively well. Elements that are complexed by OH^- (such as Al^{3+} and Fe^{3+} at higher pHs) show more variation.

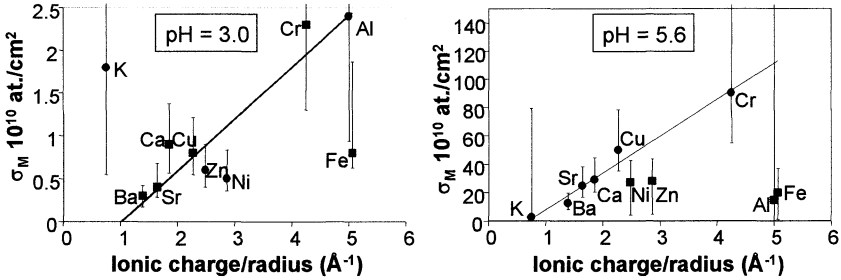

Figure 12 : Plot of equilibrium surface concentration of metal ions (•) and metal complexes (□) resulting from exposure to metals at $5x10^{-8}$ mol/L, 20 °C, and pH 3.0 and 5.6 against the ratio of ionic charge to radius. Line is least-squares fit. Error bars show 1-sigma error.

Another set of designed experiments was performed to investigate this in more detail. In these experiments higher $[H^+]$ also results in lower metal surface concentration, σ_M. The metal surface concentration was found to follow a power law of $[H^+]$ with exponent : -0.30±15. The σ_M was found to be a sub-linear function of the metal concentration in the solution, $[M^+]$. The time dependence of deposition was negligible for most elements. Only Cr, Fe and Al surface concentrations showed time dependence at pH > 5 only. This time dependence is attributed to transport (or diffusion) limited deposition [14].

A model for the adsorption of metallic ions onto hydrophylic surfaces resulting from wafer cleaning was developed. Si-OH groups act as weakly acidic ion exchangers [16-19]. The chemical oxide undergoes reactions with H^+ and other cations (e.g. metal ions), M^+, in the solution [15] :

$$\equiv SiO^-(s) + H^+(aq) \overset{K_H}{\Leftrightarrow} SiOH(s) \qquad (1)$$

$$\equiv SiO^-(s) + M^{n+}(aq) \overset{K_M}{\Leftrightarrow} SiOM^{(n-1)+}(s) \qquad (2)$$

K_H and K_M are the constants describing the attraction of H^+ and M^{n+} to the surface, respectively. It is assumed that multiple cationic species can adsorb to a limited number of surface sites with concentration, σ_0 [20]. Cations, M^{n+}, attach singly to these surface sites. This results in the following surface concentration balance :

$$\sigma_0 = \sigma_{SiOM} + \sigma_{SiOH} + \sigma_{SiO^-} \qquad (3)$$

where σ_{SiOM} is the surface concentration of the metal on the wafer surface. Combining the equilibrium expressions corresponding to reaction (1) and (2) with equation (3) yields the following expression for the metal surface concentration :

$$\sigma_{SiOM} = \frac{K_M[M^+]}{1 + K_H[H^+] + K_M[M^+]}\sigma_0 \qquad (4)$$

This model has also been expanded to describe more realistic situations with different metallic contaminants being present simultaneously [20].

Equation (4) implies a linear relationship between $1/\sigma_{SiOM}$ and $1/[M^+]$. The fit parameters can thus be easily obtained from an 'inverse' plot. Figure 13 shows the agreement between experimental data and the model of equation (4) in a conventional deposition plot [21]. This plot also shows why for the range of experimental conditions a sub-linear relationship was obtained from the DOE-model.

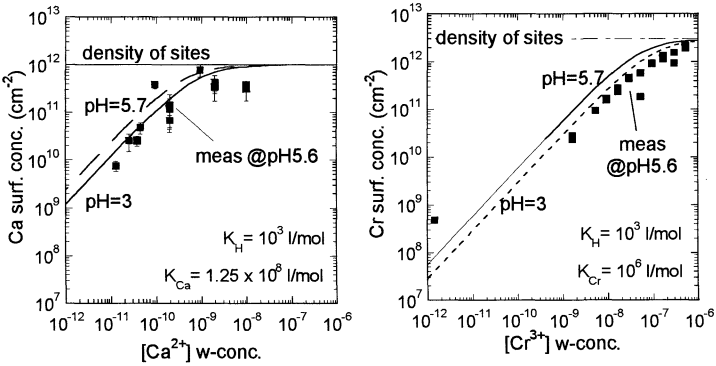

Figure 13 : Experimental results and the model of equation (4) for σ_{Ca} as a function of $[Ca^{2+}]$ weight- concentration [22] and σ_{Cr} as a function of $[Cr^{3+}]$ [21].

This work contributes in the design of an optimal rinsing process and helps to specify the required metallic purity of ultra pure water systems. For example, using this model for Ca, we find that to reach a purity level of 10^{10} at/cm^2 at pH 5.6, the maximum $[Ca^{+2}]$ that can be tolerated is only 15 ppt. To make the rinsing process cost-effective and robust it is recommended to slightly acidify the rinse water. The effect of this is shown in figure 14. This optimized rinsing has been implemented in the IMEC-clean and has demonstrated to yield excellent results in a production line over an extended period of operation.

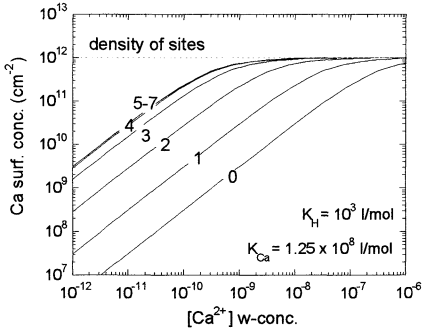

Figure 14 : Ca surface concentration as a function of Ca weight-concentration and pH of the rinsing liquid.

9. CONCLUSIONS

The effect of metal contamination was investigated. Some contaminants, such as Ca, Sr and Ba, were observed to lead to high defect densities. It was demonstrated that the IMEC-clean has an excellent cleaning performance and can be used as a cost-effective replacement for the commonly used RCA-clean. The importance of the rinsing step in controlling the final surface contamination was illustrated. A model was presented describing the metal deposition on hydrophilic surfaces as a function of the pH and the concentration of metal contaminants in the DI-water.

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THE EFFECT OF DILUTE CLEANING AND RINSING CHEMISTRIES ON TRANSITION METAL REMOVAL AND Si SURFACE MICROROUGHNESS

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ABSTRACT

We use synchrotron radiation total-reflection x-ray fluorescence (SR-TXRF) to determine the efficiency of several dilute cleaning and rinsing chemistries in removing surface transition metal contamination down to $8x10^7$ atoms/cm^2 concentration levels from both hydrophilic and hydrophobic silicon surfaces. The dilute chemistry investigated in this work includes HF, HCl, an HF and HCl mixture, DI(HCl), and DI(O_3). The changes in surface roughness are determined by atomic force microscopy (AFM).

From these experiments, we conclude that the best results can be obtained by use of a dilute HF-only or an (HF+HCl) process scheme. Incorporation of HCl into the process scheme can result in higher residual Cu levels and increased surface roughness. The use of an ozonated rinse offers no appreciable advantage with respect to metal contaminant removal.

INTRODUCTION

The continuous downscaling of device dimensions results in more stringent requirements of acceptable metallic contamination levels prior to gate oxidation as metal contamination in a metal-oxide-semiconductor device would degrade its electrical performance by creating charge generation-recombination centers.[1] Wet chemical processing has been the dominant wafer cleaning technology to remove damage and contamination introduced to the wafer surfaces from other fabrication processes, materials, and humans. A typical wafer plant processing 1500 eight-inch wafers consumes approximately 500 gallons of hazardous chemicals and 10-20 million gallons or more of ultra-pure water for rinsing and drying on a daily basis.[2] The increasingly stringent environmental, safety, and economic requirements in semiconductor manufacturing dictate the reduction of hazardous chemicals and ultra-pure water consumption for removing metallic and other contamination. To tackle the environmental challenges and improve wafer cleaning efficiency, various dry cleaning processes using excitation energies such as thermal,[3] plasma,[4] or short wavelength (ultraviolet, UV) radiation,[5,6] have been studied as a replacement for wet cleaning processes to reduce chemical consumption and remove contaminants at low temperatures. These dry cleaning processes have shown promise in complementing many wet chemical

cleans, yet the processing throughput needs to be further improved. The goal of this work is to evaluate *diluted* cleaning and rinsing chemistries to reduce chemical and water consumption and to assess their effectiveness in removing transition metal contamination from silicon wafer surfaces while preserving the smoothness of the epi-Si substrate.

The mechanism of metallic contaminant deposition on silicon surfaces has been shown to depend on the type of metals, chemical solutions, and substrates.[7,8,9,10,11,12,13] A metallic surface concentration level of 10^9 atoms/cm^2 is quoted in the SIA roadmap for device features less than 0.25 μm.[14] Achieving metallic concentration levels below 10^9 atoms/cm^2 poses challenges in both process development as well as usable analytical techniques for quantifying the low contaminant concentrations. In this work, we use synchrotron radiation total-reflection x-ray fluorescence (SR-TXRF) to measure surface concentration down to $8x10^7$ atoms/cm^2. The effectiveness of various wet chemistries in preserving surface smoothness is determined by atomic force microscopy (AFM).

EXPERIMENTAL

To assess the effectiveness of diluted cleaning and rinsing chemistries in removing transition metals, we first prepared two types of metal contaminated samples. The starting wafers were six-inch silicon (epi) wafers, which were either treated in diluted HF (15:1 deionized water to 49% HF) to remove the native silicon dioxide and yield a H-terminated surface or were used as received with the native silicon dioxide remaining. These two types of surfaces prior to contamination are referred to as "hydrophobic" and "hydrophilic" surfaces, respectively, in this work. The wafers were immersed for 5 minutes in a chemically spiked DI water bath which was prepared by adding 30 milliliters of a transition metal plasma standard solution (100 μg of Fe, Ni, Cr, V, Mn, Co, Cu, and Zn per milliliter in 5% HNO_3) to six liters of deionized water. The wafers were then rinsed with deionized water and spin dried.

The dilute cleaning and rinsing chemistries evaluated in this work include HF, HCl, an HF and HCl mixture, DI(HCl) and DI(O_3), as detailed in Table I with the processing steps.

Table I: Process sequences for removing metallic contamination

1	HF	OF DI	IPA dry		
2	HCl	QDR DI	IPA dry		
3	HF	OF DI	HCl	QDR DI	IPA dry
4	HF	OF DI(O_3)	IPA dry		
5	HF	OF DI(HCl)	IPA dry		
6	HF+HCl	OF DI	IPA dry		

Notes: (1) HF represents 0.5% HF at 23°C for 4 minutes.
(2) HCl represents 0.25% HCl at 70°C for 10 minutes.
(3) HF+HCl represents a mixture of 0.5% HF and 0.25% HCl at 23°C for 4 minutes.
(4) DI(O_3) and DI(HCl) represent O_3(g) and HCl(g) bubbled DI water.
The pH value of DI(HCl) is 1.9-2.0.
(5) OF and QDR represent an overflow rinse and six quick-dump rinses, respectively.
(6) IPA dry represents drying cleaned wafers in isopropyl alcohol vapor for 10 minutes.

The metal contamination level was measured by synchrotron radiation total-reflection x-ray fluorescence (SR-TXRF) at Stanford Synchrotron Radiation Laboratory (SSRL). A brief description of the synchrotron facility is included here, while the details can be found elsewhere.[15] The SR6-2 synchrotron beam at SSRL was focused with a platinum coated fused silica mirror, and then monochromated by two multilayers consisting of alternating layers of boron-carbide and tungsten to pass 11.1 keV radiation with a band pass of 280 eV. The beam is nearly 95% linearly polarized in the horizontal plane and impinges the vertically mounted wafer in vacuum at a grazing angle, which is determined using the theory of Born and Wolf.[16] The single element Si(Li) detector is positioned along the E-vector of the incident beam to minimize the scattered radiation into the detector. The transition metal contamination levels were quantified by integrating the peak intensity after a linear background subtraction under the fluorescent peak of interest. The minimal detection limit is determined to be $8x10^7$ atoms/cm^2.

The surface roughness of the epi wafers as-grown, as-contaminated, and as-cleaned was determined by atomic force microscopy (AFM) using a Digital Instruments Nanoscope III in tapping mode with etched Si tips. The initial surface roughness of the as-grown epi wafers was in 0.7 Å RMS.

RESULTS AND DISCUSSION

The primary metals deposited on both types of as-contaminated surfaces were V, Fe, and Cu (Figure 1a). Contaminant levels were in the 10^9 to 10^{10} atoms/cm^2 range, and are detailed in Table II. Other metals such as Ni and Zn also deposited on the hydrophobic surface. Metals appeared to preferentially deposit on the hydrophilic surface, consistent with the assertion that metal cations will preferentially adsorb at dissociated hydroxyl groups on the silicon surface, rather than at H-terminated sites.[17] The major difference between these two types of surfaces is that metals deposit *on*

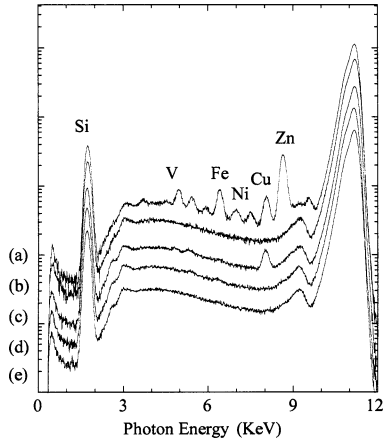

Figure 1: SR-TXRF spectra showing surface transition metal contaminant concentration of a) an as-contaminated hydrophobic surface, b) a contaminated hydrophilic wafer cleaned with an HF+DI process, c) a contaminated hydrophilic wafer cleaned with an HCl+DI process, d) a contaminated hydrophilic wafer cleaned with an (HF+HCl)+DI process, and e) a contaminated hydrophilic wafer cleaned with an HF+DI+HCl+DI process.

hydrophilic (native SiO_2) surfaces, but might *segregate at* the Si/SiO_2 interface after the H-terminated surface is reoxidized.

Dilute HF solution was found to remove transition metal contaminants most effectively among all chemistries investigated (Figure 1b). The metal removal is achieved primarily by etching the "native" silicon dioxide grown before or after the metal contamination. If metal contamination does not segregate during the reoxidation of hydrophobic surfaces, HF should be equally effective in removing metals from both hydrophilic and hydrophobic surfaces. The etching of silicon dioxide releases SiF_x, removes metals, and leaves the silicon surface terminated with hydrogen, which hinders the competitive adsorption of metal cations and makes metal replating on the surface difficult.[17] Indeed, as shown in Table II, we observed extremely low levels of Cu contamination on both hydrophilic and hydrophobic surfaces ($2.2x10^8$ and $1.3x10^8$ atoms/cm^2, respectively) after HF cleaning and DI rinsing, a decrease of two orders of magnitude from the as-contaminated wafers. Fe levels were also very low ($2.8x10^8$ and $2.0x10^8$ atoms/cm^2 for hydrophilic and hydrophobic surfaces, respectively). AFM evaluation of the surface morphology of these wafers shows no surface degradation resulting from exposure to dilute HF. The surfaces of dilute HF-cleaned wafers are identical in appearance to that of the starting epi substrate with clearly defined terraces (Figure 2a).

Table II: Summary of the transition metal contamination levels on both hydrophilic and hydrophobic surfaces

Process	Concentration ($x10^9$atoms/cm^2)		
	V	Fe	Cu
As-contaminated			
Hydrophilic	24	3.8	16
Hydrophobic	18	1.8	12
HF+DI			
Hydrophilic	--	0.28	0.22
Hydrophobic	--	0.20	0.13
HCl+DI			
Hydrophilic	--	0.48	6.0
Hydrophobic	--	0.22	0.76
(HF+HCl)+DI			
Hydrophilic	--	0.57	0.11
Hydrophobic	--	0.40	--
HF+DI+HCl+DI			
Hydrophilic	--	1.1	--
Hydrophobic	--	0.22	--
HF+DI(O_3)			
Hydrophilic	--	0.73	--
Hydrophobic	--	1.0	0.13
HF+DI(HCl)			
Hydrophilic	--	23	0.26
Hydrophobic	--	7.0	0.10

In addition to HF, HCl was also explored in cleaning transition metals from silicon surfaces. Dilute HCl solution was repeatedly found to remove most transition metal contaminants but Cu from both hydrophilic and hydrophobic surfaces (Figure 1c). The residual copper level on the dilute HCl-cleaned hydrophobic surface was several times greater than that found on the corresponding HF-cleaned wafer, and the hydrophilic surface had a Cu level an order of magnitude greater (Table II). The iron concentration of the HCl-cleaned hydrophilic surface, although about twice the value of the HF-cleaned hydrophilic surface, was still very low at 4.8×10^8 atoms/cm^2. The Fe concentration on the hydrophobic surface was comparable to that of the corresponding HF-cleaned wafer. Wafers cleaned in HCl would be unlikely to have fully hydrogen terminated surfaces. Chlorine to silicon bonds are polar and the negatively charged chlorine could attract and interact with metal cations and result in high levels of Cu redeposition and some Fe contamination, as observed experimentally.

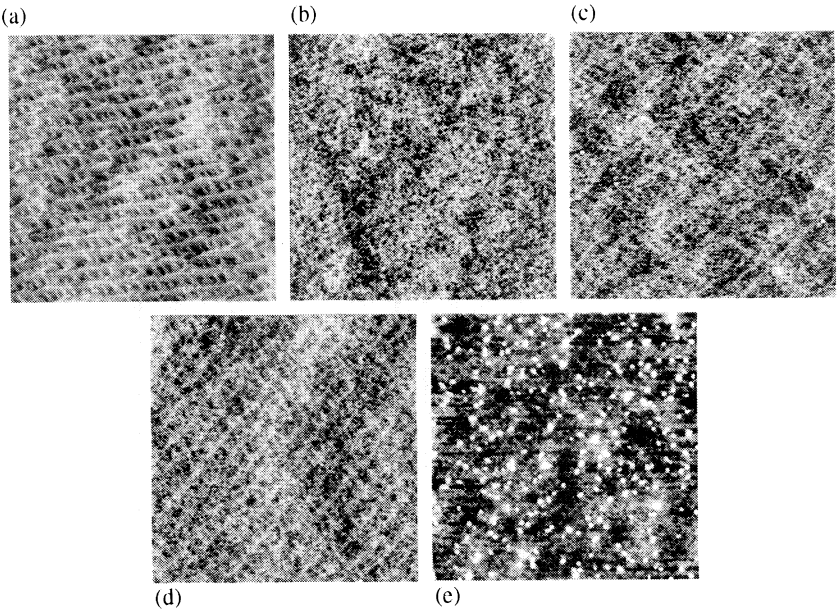

Figure 2: 2 μm x 2 μm AFM images of a) starting epi substrate, 0.7 Å RMS; b) a contaminated hydrophobic wafer cleaned with an HCl+DI process, 1.1 Å RMS; c) a contaminated hydrophilic wafer cleaned with an (HF+HCl)+DI process, 1.1 Å RMS; d) a contaminated hydrophilic wafer cleaned with an HF+DI+HCl+DI process, 0.9 Å RMS; and e) a contaminated hydrophilic wafer cleaned with an HF+DI(HCl) process, 2.2 Å RMS. The height scale for all images is 1 nm.

Dilute HCl cleaning also resulted in a marked roughening of the hydrophilic wafer surface as determined by AFM, an increase from 0.7 Å to 1.1 Å RMS. Examination of the AFM micrograph (Figure 2b) shows that the clearly defined terraces of the epi structure have been etched away. It is noteworthy that an uncontaminated hydrophilic wafer was *not* roughened by this process. The roughness of the hydrophobic surface was unchanged from that of the starting substrate.

To prevent the redeposition of the noble metals such as Cu, HCl was added to the HF solution to lower the pH of the solution and raise the redox potential.[18] An (HF+HCl) mixture was found to remove transition metal contaminants effectively and suppressed the redeposition of Cu by lowering the pH of the cleaning solution (Figure 1d). The Cu concentration on the hydrophilic surface was 1.1×10^8 atoms/cm^2, even lower than obtained with the dilute HF-only clean. For the hydrophobic surface, Cu was below the detection limit. However, low levels of Fe contamination were observed for both hydrophilic and hydrophobic surfaces (Table II). The contaminated hydrophilic surface was roughened by this process (Figure 2c), again increasing from 0.7 Å to 1.1 Å RMS. Although the terraced structure is still visible, a comparison with the starting substrate in Figure 2a shows that some of the detailed features have been etched away. No increased roughness was seen for the hydrophobic nor the uncontaminated hydrophilic surfaces with this process. This anomalous roughening of only the contaminated hydrophilic surface by these HCl-containing processes may be due to differences in the nature of the native oxide of the hydrophilic surface (as received) compared to that of the hydrophobic surface(regrown after chemically removing the initial oxide prior to contamination).

An HF+DI+HCl+DI sequential process (Figure 1e and Table II) yields comparable metal removal efficiency as an (HF+HCl)+DI process. Most of the metal is believed to be removed during the initial HF etching. Low levels of Fe contamination were again observed after the process. It is worth noting that wafers subjected to this sequential process were consistently roughened (compared to the starting wafer), regardless of whether the wafers were hydrophilic or hydrophobic, and the degree of roughening was independent of contamination (Figure 2d). The roughening from this process is not as severe as that seen for the contaminated hydrophilic surfaces exposed to HCl+DI and (HF+HCl)+DI, and only results in an increase to 0.8 - 0.9 Å RMS. In this case, the roughening appears to be due to the etching effect of HCl on the bare Si surface of the HF-cleaned wafer.

We also examined two modified chemical rinsing processes: DI(HCl) and DI(O_3). An HCl-spiked DI rinse after HF cleaning, while yielding Cu levels similar to that obtained with a regular DI rinse, resulted in high levels of Fe contamination on both hydrophilic and hydrophobic surfaces (Table II). These high iron levels could possibly be the result of exposing wafers with residual surface HCl to the stainless steel walls of the IPA dryer. The introduction of dilute HCl solution into the stainless steel IPA vapor dryer at high temperature (~80°C) could result in some corrosion of the walls of the dryer and lead to iron contamination on the wafer surface. In addition, this process caused substantial roughening of the wafer surface. Figure 2e shows the surface of a hydrophilic contaminated wafer after HF+DI(HCl) processing. This wafer had a surface roughness of 2.2 Å RMS, and the appearance of numerous tall asperities is a significant difference from wafers that were roughened by other processes that were evaluated. Asperities of this type were seen on both contaminated and uncontaminated hydrophilic and

hydrophobic surfaces, although they were much more numerous on the contaminated wafers. It is possible that this roughening is related to the corrosive effects of dilute HCl residual in the high temperature stainless steel IPA vapor dryer.

The use of an ozonated water rinse following HF offers no appreciable advantage with respect to metal removal or surface roughness. As can be seen in Table II, HF+DI(O_3) processing does not result in significant improvement of metal concentrations over the other processes evaluated. The roughness of the contaminated wafers was unchanged from that of the starting substrate. More work is underway to understand if the chemical oxide grown during this process yields superior quality oxides.[19]

CONCLUSIONS

We have evaluated the effect of dilute cleaning and rinsing chemistries on transition metal removal and surface microroughness for hydrophilic and hydrophobic silicon surfaces. In this study, the best transition metal removal results were obtained by use of a dilute HF-only or an (HF+HCl) process. The metal removal is achieved primarily by etching of the native oxide and concurrent dissolution of contaminants contained within. Incorporation of HCl into the process scheme can result in higher residual copper levels and/or increased surface microroughness. More work must be done to determine the contribution of the native oxide quality to the final surface roughness in order to understand why contaminated hydrophilic surfaces appear to be more susceptible to HCl-induced roughening. The use of dilute HCl rinses should be evaluated carefully with respect to equipment compatibility and possible corrosion issues. The use of an ozonated rinse offers no appreciable advantage with respect to transition metal contaminants.

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THE STCLEAN DUAL STEP CLEANING CONCEPT

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Abstract

RCA is well known to be very effective for both particle and metal removal, but reduction of chemical and DIW consumption is becoming more urgent for industry as well as reduction of equipment footprint. In this paper we propose a new dual cleaning sequence, composed by a diluted SC1 step and an ozonised rinse step with HCl spiking, that allows to reduce both the footprint and the chemical consumption. Morphological and electrical characterization showed better or equal performances than the RCA cleaning sequences.

INTRODUCTION

The replacement of the very effective cleaning cycles based on the historical RCA concept has become a necessity for the semiconductor industry since few years, in order to reduce the high costs related to the equipment footprint and the chemical / DIW consumption, as well as minimize the environmental impact of the device manufacturing technology.

Dual step cleaning sequences have been proposed by IMEC[1] (IMEC Clean), LETI[2] (DDC) and Ohmi Lab (FPMS), all based on the HF chemistry and extensively proven to be very effective in many fields of applications[3], both in terms of cleaning performances and cost reduction.

However, in several advanced semiconductor devices, like non-volatile memories (NVM) and logics, the use of multiple thin active dielectrics and of critical isolation techniques, makes the implementation of HF based cleaning sequences almost impossible[4]. In fact, the impact of the cleaning steps on the final oxide properties, including defectivity and thickness uniformity, is strongly enhanced by using such cleaning sequences and can become the most important degradation factor for 15-35 Å gate oxides. Moreover, as reported in Figure 1, when an oxide stripping process has to be performed, an SC1 step is recommended to avoid wafer cross-contamination problems[5], the so called "Holy Grail" effect.

The proposed cleaning sequence, called STCLEAN or STC, is still made of two steps, but based on a very diluted SC1 chemistry followed by an "Optimized DIW Rinse" (ODR) step, which includes O_3 injection and HCl spike. Megasonics are used in both SC1 and rinse tanks.

This sequence allows to reduce the number of tanks in conventional wet stations or the process time in single tank tools to the level of an HF based cleaning, without the above mentioned integration problems. Figure 2 shows some possible cleaning sequences, when a previously grown oxide, like a sacrificial oxide, has to be removed before the cleaning step. The complete sequential RCA cycle needs 7 steps, while an HF based cleaning requires 5 steps, if a surfactant addition is used as proposed in reference [4], or separated "oxide removal" and "cleaning" cycles. The STC uses only 5 steps without any need of separate etching tool, and can be implemented in conventional wet benches as well as in the latest generation hybrid tools. In case of wet benches the reduction of the number of tanks and the simplified hardware configuration clearly reduces the bench footprint, the complexity and the equipment downtime. The footprint saving is about 20%. If a cleaning sequence without oxide stripping is made, the RCA requires 5 steps, the STC 3 steps like the HF based chemistries, with a possible overall footprint reduction of about 25% for a standard wet bench.

EXPERIMENTAL

The cleaning characterization has been performed using 6" wafers on a STEAG AWP III automated wet bench. SC1 ratio was 0.25:0.5:5 (NH_4OH:H_2O_2:H_2O) at 50°C, with a VERTEQ Sunburst megasonics system. The tank used to perform the second step of the cleaning was a quartz overflow rinse tank, with a VERTEQ Sunburst megasonics system, HCl spiking and O_3 injection through a Sorbios static mixer. Ozone concentration was adjustable up to 30ppm.

The ODR recipe used during most of the tests is made by four steps, all done sequentially in the same tank without any crossing of the air/liquid interface. The first step is a high flow rinse to remove most of the SC1 from the wafers. During the second step the HCl is spiked into the tank and the ozone starts to be injected. In the third "soaking" step the DIW flow rate is strongly reduced and O_3 is continuously injected. The final step is a rinsing step, where most of the HCl residues are removed from the wafer surface. Megasonics are turned on in the whole process. O_3 concentration has been set to 5ppm in order to maintain the growth of chemical oxide on the silicon surface at reasonable levels.

The optimized recipe with the reported hardware configuration is summarized in the following table.

1	SC1 rinsing	DIW high-flow (25l/min)
2	HCl Spiking	DIW low-flow (4l/min)+HCl spikes+O_3
3	Soak	DIW low-flow+O_3
4	Rinsing	DIW high-flow

Morphological characterization

Particle removal efficiency has been tested on bare silicon wafers intentionally contaminated by silicon nitride and silicon dioxide powders in DIW[6]. As expected, due to the use of the same SC1 step, the particle removal efficiency is as good as a conventional RCA sequence (Figure 3). The use of SC1 allows to easily remove the critical nitride particles, while the HF based cleaning (Twin Clean, see reference [6],[8]) is slightly less efficient. On the oxide particles all kinds of cleaning sequences show a very high removal rate.

The rinsing step alone offers a rather good particle removal efficiency, but not enough to comply to current requirements. This proves that an SC1 step is strongly recommended when a high removal rate is required, regardless of the chemical nature of the particles.

Thanks to the improved analytic capabilities of the KLA-Tencor SP1, we can accurately estimate also the removal efficiency for very small particles (0.12-0.15µm). In this case the initial count before the wafer contamination must be taken into account, because -besides real removable defects- also LPDs originated by roughness and pitting belong to this size range.

Particle removal efficiency can thus be calculated according to the following relationship:

$$R.E\% = \frac{(LPD_{contam} - LPD_{init}) - (LPD_{final} - LPD_{init})}{LPD_{contam} - LPD_{init}} \cdot 100 = \frac{LPD_{contam} - LPD_{final}}{LPD_{contam} - LPD_{init}} \cdot 100$$

where LPD_{init} is the particle count before the contamination procedure, LPD_{contam} are the particles after the contamination and LPD_{final} are the particles after the cleaning.

In this relationship it is supposed that the initial counts are all related to roughness or pitting. In case this assumption is not satisfied, removal efficiency can be higher than 100%. Figure 4 shows the normalized removal efficiency for particles with size between 0.12 and 0.15µm. Both RCA and STC are clearly very efficient for silica and nitride removal, even for such small particle sizes.

Wafers for metal removal efficiency were contaminated by a procedure which consists of dipping the test wafers in a nitric solution with the requested quantity of contaminant already dissolved [5]. Iron concentration was measured by ELYMAT (diffusion length) while copper contamination was measured by TXRF.

When replacing the conventional SC2 with a much more diluted solution, one of the main issues is related to the metal removal capability. Iron removal efficiency has been tested and compared to a conventional SC2 process and to an HF based cleaning.

The rinse recipe for this test uses 100ml of HCl for either the STC and the HF based cleaning. As shown in Figure 5 the iron removal rate of the HF based cleaning is very high, giving overall the best performances. Anyway the STC can also provide excellent results, that confirm the capacity of such a diluted HCl concentration in removing most of the iron present on the wafer surface.

As shown in Figure 6, copper is very easily removed by the O_3 injection during the rinsing step[7]. Even a very small amount (1ppm) of ozone in water gives results comparable to a standard SC2, and 15 ppm are enough to guarantee a Cu removal below the TXRF detection limit.

Copper removal efficiency of the overall cleaning sequence is shown in Figure 7. Five ppm of ozone are injected for either the STC and the HF based cleaning. Copper is reduced below the TXRF Low Quantification Level (LQL) for all the cleaning sequences.

Surface roughness is very low because of the ozonated rinse that acts as a smoothing agent [8]. No major differences were found between RCA and STC.

Rinsing Efficiency

Because in the STClean the HCl is directly injected into the rinsing DIW, it is important to verify that there are no chlorine residues after the rinsing step. For this purpose it was performed a surface ToF-SIMS analysis (CAMECA ToF-SIMIS, using Ga ion beam). The ToF counts were normalized by the ^{30}Si signal. The Cl and ^{37}Cl signals are reported in Figure 8. The residual Cl ions are less than the ones left by the reference RCA cleaning. This fact can be related to the low HCl concentrations used in the ODR step, respect to the one used in the reference RCA.

Chemical saving and throughput considerations

The estimated chemical and DIW consumption, the cycle time and the throughput are reported in the following table for RCA and STC for the utilized hardware configuration.

	RCA	STC
DIW cons. (l/batch)[1]	350	150
HCl cons. (ml/batch)	400	100
H_2O_2 cons. (ml/batch)	660	260
NH_4OH cons. (ml/batch)	130	130
Cycle time (min)	35	25
Throughput (w/hour)	200	>250

[1] *rinse steps only.*

The STC allows a reduction of the DIW consumption of more than 50%. The HCl consumption can be reduced of 75%. Peroxide is used only in the SC1 step and the consumption is less than 50% of the standard RCA.

Another major improvement is the cycle time that can be reduced of about 30%. This reduction can drastically improve the throughput of single tank tools, reducing the gap with a conventional wet station. In case of the utilized hardware setup, the throughput can be improved of about 25%.

Electrical characterization

Electrical properties of active oxides were evaluated using ERCS, CCS and TDDB techniques, showing no major differences for the STC respect to the standard RCA in terms of both the intrinsic and the extrinsic quality. ERCS for a tunnel oxide is reported in Figure 9. No relevant differences are evidenced between the two splits for both intrinsic and extrinsic distributions.

The impact of STClean on the yield of an advanced Flash Memory device is reported in Figure 10. For this trial all the cleaning steps until the silicide deposition were tested, cleaning half of the lot by RCA and half by STC. Yield results are slightly better for the STC than the RCA reference for the prime yield (no redundancy), the total yield and the yield after bake (used to check possible charge retention problems), confirming the full compatibility with the existing process flow and the possibility for a complete replacement of the conventional RCA sequence.

CONCLUSIONS

The new proposed cleaning sequence, called STCLEAN or STC, gives many advantages compared to a conventional RCA cleaning, mainly for the reduction of chemical and DIW consumption and the increased throughput. The complete feasibility has been demonstrated by analyzing particle and metal behaviors as well as the electrical impact on active oxides and NVM device yield.

HF based cleaning sequences also provide excellent intrinsic performances, but they suffer of major process integration problems in a typical device process flow, due to the presence of an etching chemistry. No modifications of existing process flows are required with the STC, since it is fully compatible with the standard RCA.

ACKNOWLEDGMENTS

Authors would like to acknowledge F.Tardif (TXRF measurements), L.Polignano (ELYMAT measurements), F.Zanderigo (ToF SIMS measurements) and G.Girardi (yield analysis).

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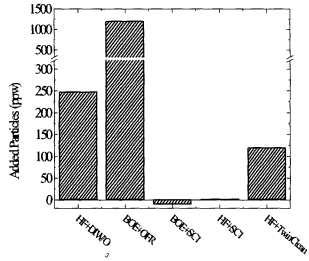

Figure 1 Particle addition after HF etching

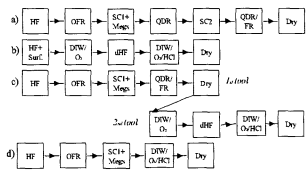

Figure 2: cleaning sequences
a) RCA with embedded HF strip
b) Twin Clean with HF/surfactant strip
c) Twin Clean with external HF strip
d) STC with embedded HF strip

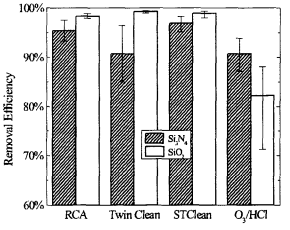

Figure 3. Particle removal efficiency on Si_3N_4 and SiO_2 powders >0.15µm.

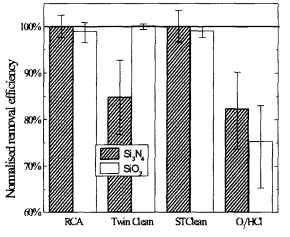

Figure 4 Particle removal efficiency on Si_3N_4 and SiO_2 powders.

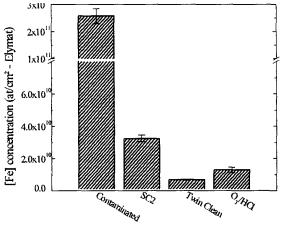

Figure 5. Iron removal efficiency

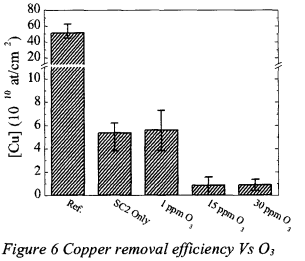

Figure 6 Copper removal efficiency Vs O_3 concentration

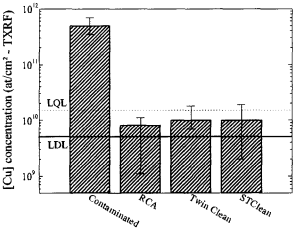

Figure 7. Copper removal efficiency

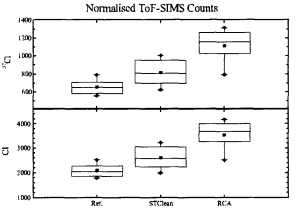

Figure 8 Cl residues after rinse

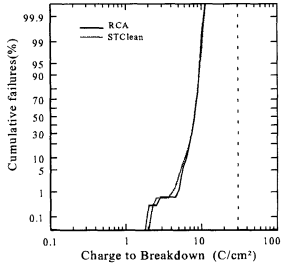

Figure 9 ERCS for a tunnel oxide (thickness ~100Å)

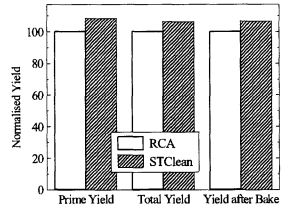

Figure 10 Normalised yield. Comparison between RCA and STClean

SILICON CRITICAL CLEANING WITH OZONE, HF AND HCL IN A SPRAY PROCESSOR

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ABSTRACT

Ultra pure deionized water with high concentrations of dissolved ozone gas (DIO_3) has been investigated for use in silicon critical cleaning. This work is centered on eliminating the need for sulfuric acid (H_2SO_4), hydrogen peroxide (H_2O_2) and ammonium hydroxide (NH_4OH) previously required in wet cleaning. These three chemicals are replaced by DIO_3, which, when used in conjunction with hydrofluoric acid (HF) and hydrochloric acid (HCl), provides a powerful and inexpensive cleaning process. The new process utilizing DIO_3 is shown to be equal to or better than standard cleaning processes in particle performance, residual metallics and surface roughness.

INTRODUCTION

The use of DIO_3 in silicon critical cleaning has been studied for several years (1, 2, 3 and 4). It was initially used to replace hydrogen peroxide in the well-known piranha or sulfuric acid – hydrogen peroxide mixture (SPM) and was referred to as the sulfuric acid-ozone mixture (SOM). DIO_3 has also been used as an agent for re-oxidation of a silicon surface after HF processing. Until recently, IC manufacturers have preferred to stay with the well-known RCA cleaning chemistry which is comprised of the Standard Clean 1 step (SC1) followed by the Standard Clean 2 step (SC2) for silicon critical cleaning. SC1 uses NH_4OH and H_2O_2 mixed with DI water for formation of a chemical SiO_2 layer and particle removal. SC2 uses HCl and H_2O_2 mixed with DI water for removal of metallic contamination. Some manufacturers have started using diluted versions of the RCA chemistry, but the use of DIO_3, HF, and HCl as a complete replacement of SPM, SC1 and SC2 has not yet been widely accepted in semiconductor manufacturing.

The use of DIO_3, HF, and HCl in various combinations and sequences has recently been studied in immersion systems for its effectiveness in silicon critical cleaning (3). These chemicals have also been studied in a single-wafer spin processor (4). In this study, the effectiveness of DIO_3, HF, and HCl for silicon critical cleaning was evaluated in a spray processor.

EXPERIMENTAL

DIO_3 is generated using a newly developed technology that allows high concentrations of ozone (60 to 120 ppm) to be dissolved in water at room temperature under pressurized conditions (2 to 3 bar). The spray processor is ideally suited for utilizing this type of DIO_3 because the pressurized state can be maintained until the solution is dispensed onto the wafer surface. Less than 20% of the dissolved ozone is lost to the gas phase during the short contact time with the wafer surface, thus maintaining high ozone concentrations at the wafer surface.

Various dispense sequences were evaluated. Most process sequences began with DIO_3 treatment at a concentration of 50 to 60 ppm. This step replaces the traditional SPM step for removal of trace organic contamination. After a short cold rinse, dilute HF was dispensed to remove native, chemical, or sacrificial oxide and to expose the bare single-crystalline silicon surface. During the HF dispense step, HCl can also be dispensed to facilitate trace metals removal. After another short cold rinse, DIO_3 was again dispensed to grow a clean, passivating oxide layer. HCl can also be dispensed during this final DIO_3 step to facilitate further trace metals removal.

The light-point defect (LPD) monitor wafers in this experiment were 200-mm n-type epitaxial-ready bare silicon wafers. Particle challenge wafers were fabricated using 200-mm prime bare silicon wafers and a wet deposition technique to deposit silicon nitride (Si_3N_4) particles. LPDs were measured using a KLA-Tencor Surfscan® SP-1 TBI surface inspection system for LPDs greater than or equal to 0.12 μm with a 3-mm edge exclusion.

RESULTS

A simple sequence of DIO_3 - HF - DIO_3 adds less than 35 defects greater than or equal to 0.12 μm to clean monitor wafers. This sequence can also remove 95% of 0.12-μm Si_3N_4 particles with starting counts of about 2,000. Typical dispenses were three minutes for each DIO_3 step and one minute for the HF step.

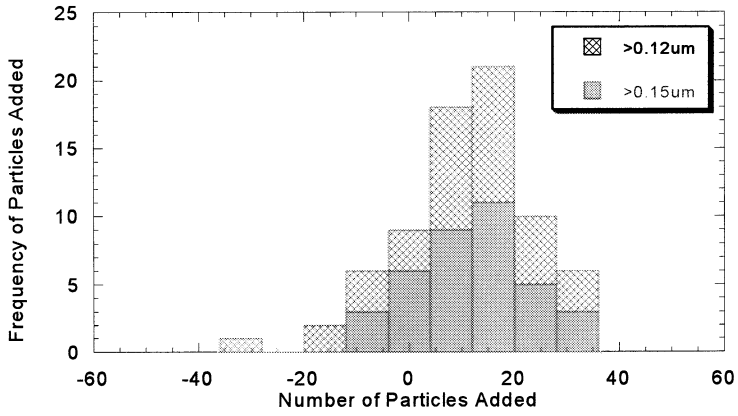

Figure 1: Particle data collected from DIO_3-HF/HCl-DIO_3 on new epitaxial grade wafers.

Si_3N_4 particle removal efficiency was measured for s everal DIO_3 processes and compared to the standard B-clean process. Particles greater than or equal to 0.12 μm on 200-mm wafers were measured. Figure 2 shows the results obtained on wafers challenged with 2,000 Si_3N_4 particles. As expected, rinse-dry only and DIO_3 rinse-dry only did not remove any challenge particles (not shown). Particle removal efficiency was relatively low for a short, two-step process of dilute HF for one minute followed by DIO_3 for three minutes and rinse-dry (designated F-O). Removal efficiency increased when an additional DIO_3 step was added at the beginning (O-F-O).

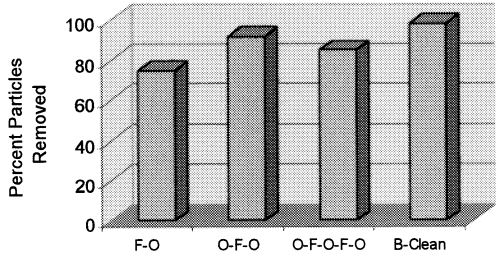

Figure 2: Si_3N_4 particle removal starting with 2,000 challenge particles greater than 0.12 μm in size on 200-mm wafers. B-clean designates the standard cleaning sequence of SPM-HF-RCA. For the ozonated water sequences, O = DIO_3 (60 ppm, 3 min) and F = dilute HF (100:1, 1 min).

Atomic force microscopy (AFM) was used to examine the surface roughness of various processes. Two different experiments were conducted, the first (Figure 3) was used to determine if HCl in either of the last two steps of the O-F-O process caused an increase in surface roughness. The data collected indicates that neither process (O-FC-O, nor O-F-OC) has detrimental effects on surface roughness.

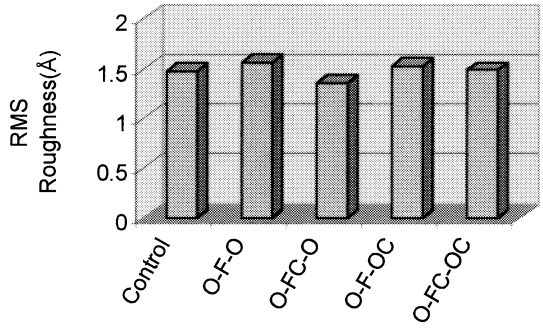

Figure 3: AFM surface roughness measurement after various process sequences [O = DIO_3; F = HF, C = HCl].

In another test, the effect of repeated cleaning on silicon surface roughness was examined using three bare silicon wafers. First, all three wafers were exposed to the O-FC-O process three times, then one wafer was removed. Next, the remaining two wafers were exposed three more times to the same process and upon completion of this phase, a second wafer was removed. Finally, the last wafer was exposed to the O-FC-O process three more times. The results are summarized in Figure 4, indicating that after even nine exposures to the O-FC-O process, wafers do not experience an increase in surface roughness. Figure 4 indicates that surface roughness may be decreased with repeated exposure to the O-FC-O process.

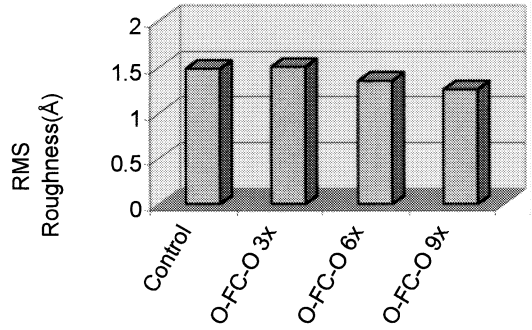

Figure 4: AFM surface roughness after repeated exposure to the O-FC-C process sequence [O = DIO_3; F = HF, C = HCl].

Overall cleanliness of the ozone processes and ozone generator has been examined using residual metallic contamination testing. Here, the same four processes evaluated for surface roughness are tested for metallic contamination at the wafer surface. DIO_3 is created near point-of-use from clean DI water and a filtered, clean source of O_3, making DIO_3 itself very clean. This, and the fact that DIO_3 has near-neutral pH, ensures that surfaces stay free of metallic contamination during the cleaning sequence as shown in Table I. In these tests the wafers were not purposely challenged with metal contamination.

However, the control wafer did show low levels of Al and Cu contamination, which appear to have been removed by the DIO_3 cleaning sequences.

Table I. VPD-ICP-MS measurement of surface metals after various sequences. Virgin prime 200-mm test wafers were used to gauge levels of residual metallic contamination following various DIO_3 processes. Values are $x10^{10}$ atoms/cm^2. [O = DIO_3; F = HF, C = HCl].

Element	*Al*	*Ca*	*Cr*	*Cu*	*Fe*	*K*	*Na*	*Ni*	*Zn*
O-F-O	<0.5	<0.5	<0.1	<0.1	<0.3	<0.5	<0.5	0.061	<0.1
O-FC-O	<0.5	<0.5	<0.1	<0.1	<0.3	0.97	<0.5	<0.05	<0.1
O-F-OC	<0.5	<0.5	<0.1	<0.1	<0.3	<0.5	<0.5	<0.05	<0.1
O-FC-OC	<0.5	0.52	<0.1	<0.1	<0.3	<0.5	<0.5	<0.05	<0.1
Control	0.68	<0.5	<0.1	0.56	<0.3	<0.5	<0.5	<0.05	<0.1
Detection	0.5	0.5	0.1	0.1	0.3	0.5	0.5	0.05	0.1

Figure 5 shows the formation of chemical oxide after HF has been used to remove silicon dioxide and expose a bare silicon surface. Measurement of oxide thickness by ellipsometry indicates that a self-limiting, 9 to 10-angstrom thick, oxide layer grows on the silicon surface during a two-minute exposure to 50 ppm DIO_3. This is essentially the same time for a self-limiting oxide layer to grow during exposure to APM. Achieving the self-limiting thickness is important to minimize surface contamination as explained by Nelson (5). The exact nature of the mechanism for contamination and therefore prevention of contamination is not understood, however experimental data indicates that the post process particle counts are lower on wafers that have a thicker chemical oxide (figure 6).

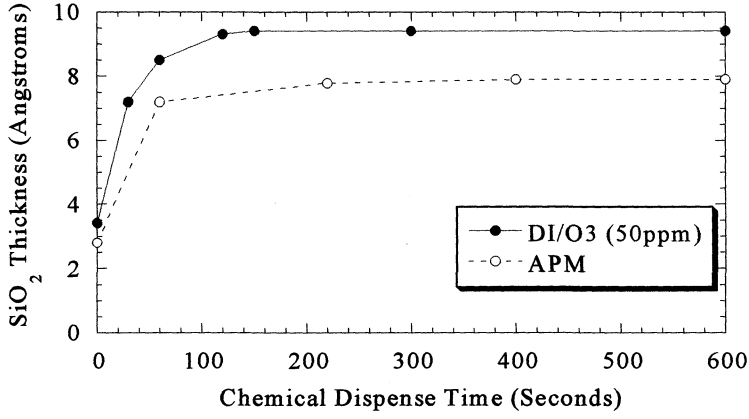

Figure 5: Comparison of the SiO_2 chemical oxide thickness formed by either an APM or DIO_3 solution (5). The DIO_3 oxide is slightly thicker because of the lack of an etchant such as ammonium hydroxide in the APM solution.

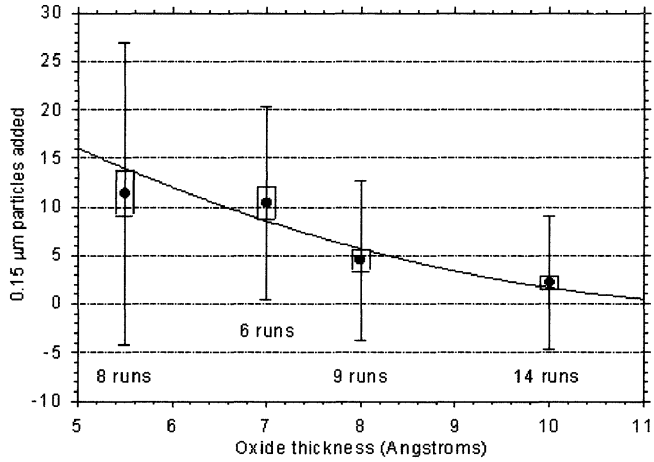

Figure 6: Particle performance as a function of chemical oxide thickness grown by the DIO_3 process. Data indicates that as oxide thickness increases, fewer particles are detected on a wafer surface.

ENVIRONMENTAL ADVANTAGES

The environmental advantages of DIO_3 processing are achieved via reductions in water and chemical usage. Correlations between water usage and process time (6) show reductions in process time are directly related to reductions in water usage. While water usage for a typical B-clean is about 3.8 liters per wafer per run, the O-FC-O process uses just 1.7 liters per wafer per run. Chemical usage is lowered because NH_4OH, H_2SO_4 and H_2O_2 are eliminated. Since the ozone process used to replace the B-clean only requires small amounts of HF and HCl, we see the chemical usage is lowered from 0.037 liters per wafer per run for the B-clean, to 0.0006 liters per wafer per run for the O-FC-O process.

Therefore, the environmental advantages of DIO_3 are centered on reductions in water and chemical usage. DIO_3 also reduces the rinsing requirements, and hence reduces the amount of water needed for critical cleaning. These reductions help lower the volume of waste generated by the process to a degree that scales with the reduction in water usage(6). These three key factors added together show that the DIO_3 processes are considerably more environmentally friendly compared to standard process chemistries.

CONCLUSION

Eliminating the use of NH_4OH, H_2SO_4, and H_2O_2 from critical cleaning is one of the major benefits of using DIO_3. Because of the high purity oxygen and water used to generate DIO_3, wafers are found to be free of common metallic contaminants compared to the reference processes that require the use of conventional cleaning chemistries. Surface roughness has been examined and data shows that even after repeated exposures to the DIO_3-HF+HCl-DIO_3 process, there is no measurable increase in roughness. Both particle removal and particle adders match the performance of reference processes such as the B-Clean. This work has shown the practical benefits of using DIO_3 for critical cleaning, offering equal or better process performance with reduced chemical and water usage.

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ADVANCED WET CLEANING METHOD WITH ONE TENTH QUANTITY OF CLEANING SOLUTION

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The advanced wet cleaning method relates to the fluid feed nozzle with ultrasonic that is employed for removing contaminants from the surfaces of the substrates during processes for manufacturing LCD or ULSI. In this method, the pressure among feeding and discharging cleaning solution and ambient air is balanced. This balance causes to feed adequate thickness of cleaning solution to remove particles from the substrate and to discharge waste solution and removed particles. The cleaning solution consumption of this method is less than 1/10 of conventional shower type nozzle with ultrasonic that has been popular in LCD fabrications. We named the nozzle using this method BPP-nozzle. The BPP-nozzle with ultrasonic and hydrogen-dissolved ultrapure water can remove PSL particles from above 30000 to about 100 in the Si-wafer cleaning.

INTRODUCTION

In the semiconductor industry, the "RCA cleaning method" has been used in wet cleaning processes. This method was established in 1970 by W. Kern and co-workers as a useful and actual cleaning method by summarizing empirical knowledge in this field at that time (1). But recently reduction in chemical and ultrapure water (UPW) consumption has become a more and more important issue. At the same time, a more efficient medium for the wet cleaning process is also needed to realize a higher level of cleanliness of ULSI devices. Many studies have been actively done to reduce the chemical concentration in the cleaning solutions (2,3), while many studies have also been done to maintain its abilities to remove contaminants. In these resent circumstances studies have shown that the wet cleaning method in use with ultrasonic wave irradiation is operated with very little chemical and UPW at room temperature (4-6). But the reduction in the cleaning solution of the ultrasonic wave irradiation cleaning method is not adequate now.

On the other hand, in the next generation of TFT-LCD fabrication, the panel size becomes bigger by using a 1m-scale glass substrate. As for the small or medium size panel, they are required higher pixel densities. The current requirement of a cleaning process for such fabrication is a high cost performance, that is, high cleaning efficiency, high throughput, small footprint, reduced consumption of UPW and other solutions which is an environment-friendly manner.

A shower type ultrasonic nozzle has been applied to the wet cleaning process of TFT-LCD fabrication; however, it faces difficulty in its use in the next phase fabrication line.

To maintain the uniformity of a cleaning power along the shower type ultrasonic nozzle, for instance, a bigger size of glass substrate should be used which causes difficulty. The shower type ultrasonic nozzle of 1m-scale cannot be made under present technology. If a 1m-scale shower type nozzle is made, it will also be a big problem because 1m-scale shower type nozzle needs 100-liter cleaning solution per minute.

To solve the above problems, we aimed to enhance the cleaning efficiency and reduce the cleaning solution by investigating the mechanism of an ultrasonic cleaning method (7,8).

In this study, we propose an advanced wet cleaning method using BPP-nozzle that is a completely different type of conventional ultrasonic nozzle and UPW with hydrogen gas, and application of the new wet cleaning process in TFT-LCD and ULSI fabrication.

THE ADVANCED WET CLEANING METHOD (BALANCED PUSH-PULL NOZZLE METHOD WITH ULTRASONIC)

In TFT-LCD and ULSI fabrication, in order to realize the ultra clean surface, the items such as (i) particle free, (ii) metal free, (iii) organic free, (iv) moisture free, (v) surface micro-roughness free, (vi) native oxide free, (vii) perfect hydrogen termination and (viii) charge-up free should be satisfied (9). Particle Free, Metal Free and Organic Free are particularly important in TFT-LCD fabrication. Removal mechanism of those contaminants is shown in Figure 1. This study concentrates on particle removal.

Two major steps are in particle removal. At first, particles have to lift off from the substrate by mechanical force, such as by ultrasonic wave or brush scrub, and/or chemical etching. Next, the ζ-potential of both the particles and the substrate have to have same polarity in cleaning solution in order for particles not to re-adhere onto the substrate (10).

The advanced wet cleaning method does just the same as the mechanism of particle removal above the substrate. An ultrasonic wave is used in the method in order for the particles to lift off from the substrate surface. The schematic diagram and the photograph of Balanced Push-Pull nozzle (BPP-nozzle) are shown in Figure 2 and 3 respectively. The Balanced Push-Pull nozzle method with ultrasonic has basically an introducing path of the cleaning solution, a discharging path of the

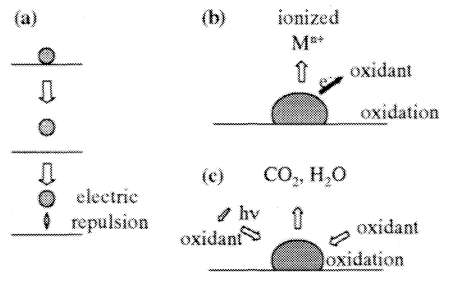

Figure 1. Contamination removal mechanism
(a) Particle: 1) Lift off and 2) prevent from re-adhering with electric repulsion
(b) Metallic contamination: Ionizing with oxidant
(c) Organic contamination: oxidation with light / oxidant

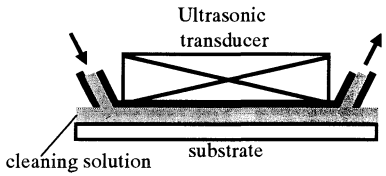

Figure 2. The schematic diagram of Balanced Push-Pull Nozzle.
The points of this cleaning method are;
(1) Pressure balance of feeding and draining
(2) The gap between nozzle and substrate.

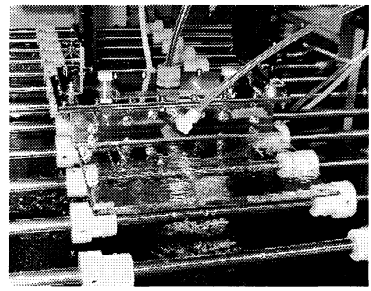

Figure 3. Photograph of BPP-Nozzle(D)

waste solution and a cleaning space with an ultrasonic transducer. First, the cleaning solution is introduced to make adequate thickness on the substrate in order for the particles to lift off from the substrate surface. This thickness is equivalent to the gap between the bottom of the BPP-nozzle and the substrate surface. This time 1MHz ultrasonic is used, so the gap is chosen within a range from 1mm to 8mm. The pressure balance between the introducing of the cleaning solution and the discharging of the waste solution is controlled. The balance between the pressure of the wet cleaning solution in contact with the substrate surface and atmospheric pressure is also controlled. The pressure balance causes it to drastically save the cleaning solution, and to be a mechanism of particle removal above the substrate.

The schematic diagram of the dual type BPP-nozzle (BPP-nozzle (D)) is shown in Figure 4. When the substrate is gone thorough the gap between the upper nozzle and the lower nozzle, the surface and the back surface of the substrate is cleaned at the same time.

In this study 3 type BPP-nozzle was used. One was a single type (80mm by 200mm), and another was a dual type (80mm by 200mm) the another was dual type (80mm by 850mm.)

On the other hand, the schematic diagram of the conventional shower type ultrasonic nozzle is shown in Figure 5. The conventional nozzle needs a large consumption of the cleaning solution (0.5~1 liter / cm·min.) Therefore, if a 1m-scale conventional shower type ultrasonic nozzle is used, a consumption of the cleaning solution will be about 50~100 liter/min cleaning solution.

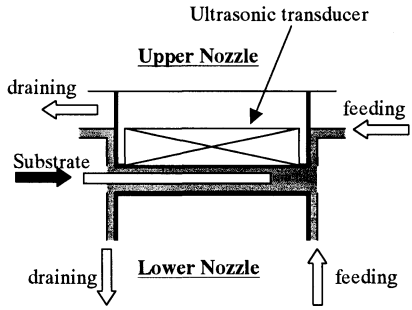

Figure 4. The schematic diagram of BPP-Nozzle(D)

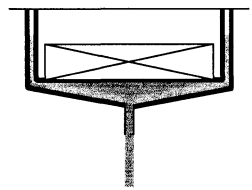

Figure 5. The schematic diagram of conventional megasonic nozzle

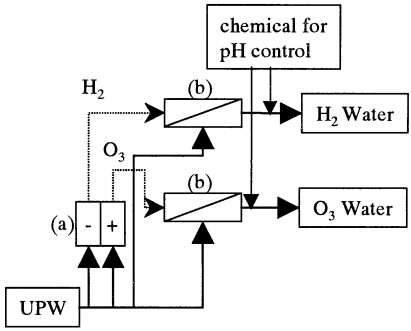

Figure 6. The schematic diagram of gas-dissolved water producing system.
(a) electric cell (b) gas dissolving module

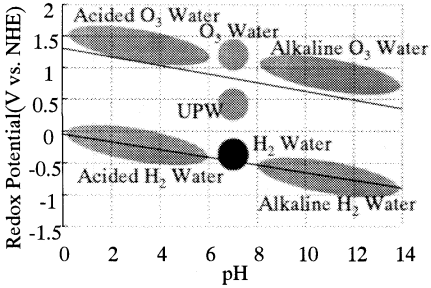

Figure 7. Chemical Properties of gas-dissolved Water

The reason for a large consumption of the cleaning solution in the conventional nozzle is that the cleaning solution imparted with an ultrasonic wave is feed via the slit which is from the opening space to feed the cleaning solution onto the substrate. The width of the slit is within a range of 1.5mm to 2mm at 1MHz ultrasonic wave.

Cleaning solution

In this study, we used UPW and hydrogen-dissolved ultrapure water (H_2Water) as cleaning solution of particle removal (7). The schematic diagram of gas-dissolved ultrapure water producing system (used to produce H_2Water) is shown in Figure 6. The property of gas-dissolved ultrapure water supplied by at producing system is shown in Figure 7. The pH and ORP (oxidation-reduction potential) can be selected by controlling the concentrations of chemicals and the quantity of dissolved gas. The pH of particle removal solution, pH9-10, is region in which the ζ-potential of both the particles and the substrate are kept negative. We presume that the reductive potential and increased cavitation, when it is used with ultrasonic, provided by dissolved hydrogen in the H_2water are the essential factors for its cleaning ability.

CLEANING ABILITIES OF BPP-NOZZLE WITH ULTRASONIC

Removal of particle contaminants from glass substrate

6inch×6inch rectangular glass substrates were provided. The substrate surface that had been stained by immersing glass substrate into UPW containing Al_2O_3 particles was used to evaluate the cleaning abilities of the BPP-nozzle with ultrasonic. The number of particles on the entire surface of the substrate after staining was measured, giving a result of over 50000 particles. Only particles having a size of at least 0.5μm on the upper surface of the substrate were measured.

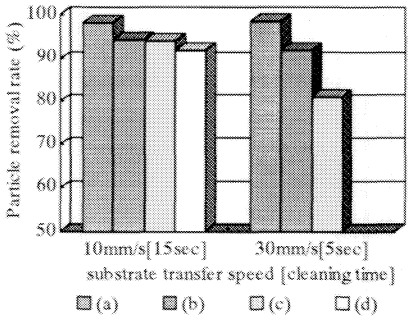

Figure 8. Cleaning efficiency of BPP-Nozzle(S).
Particle :Al_2O_3 Substrate:6"Glass substrate measure 0.5μm or above particle
(a) 1MHz BPP Nozzle, H_2Water (pH10) 1L/min
(b) 1MHz BPP Nozzle, UPW 1L/min
(c) 1MHz Conventional shower Nozzle,UPW 15L/min
(d) 1.6MHz Conventional shower Nozzle,UPW 13L/min

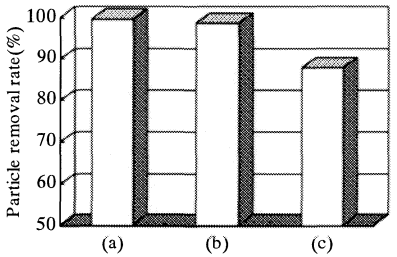

Figure 9. Cleaning efficiency of BPP-Nozzle(D)
Particle: Al_2O_3 Substrate: 6"Glass substrate measure 0.5μm or above particle
(a) BPPNozzle 1MHz H_2Water 0.7L/min 5sec
(b) BPPNozzle 1MHz UPW1L/min 15sec
(c) Conventional shower nozzle UPW 10L/min 15sec

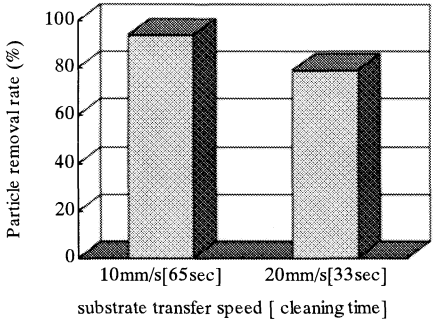

Figure 10. Cleaning efficiency of BPP-Nozzle(D)
Particle :Al_2O_3 Substrate: 550*650mm Glass substrate
Nozzle: BPPN 1MHz, 1200W measure 1μm or above particle
Cleaning solution: UPW 10L/min (both surface)

The cleaning efficiency of the BPP-nozzle (single type, 80mm by 200mm) is shown in Figure 8. There are the referential data of the conventional nozzles in Figure 8. In this figure, there is not data of the conventional nozzle with H_2water, because the gas-dissolved water producing system cannot product a large consumption of a cleaning solution (over 10liter/min) that the conventional nozzle required.

It is clear that the cleaning ability of the BPP-nozzle is superior to the conventional nozzles popularly used in TFT-LCD fabrication and that alkaline H_2water has excellent cleaning abilities at high cleaning speed such as 30mm/sec. That is to say, a 1m-scale substrate can be cleaned within about 30 seconds. The cleaning solution consumption of the BPP-nozzle is actually 1/10 lower than that of conventional nozzles.

The cleaning efficiency of the BPP-nozzle (dual type, 80mm by 200mm) is shown in Figure 9. It is clear that the BPP-nozzle (dual type) method resulted in almost 100% cleaning efficiency while the conventional nozzle method resulted in about 80%, although it used ten times as much cleaning solution as the novel method did.

The cleaning efficiency of the BPP-nozzle (dual type, 850mm) are shown in Figure 10. The 850mm length BPP-nozzle could be made in present technology. In this experiment, only particles having a size of at least 1.0μm on the upper surface of

substrate were measured.

It is shown that the long size BPP-nozzle (such as 850mm) can clean large area substrate enough.

Removal of particle contaminants from Si-wafer

5inch Si-wafers were provided. The substrates that had been stained by immersing into DHF (0.5%HF) containing PSL particles such as 0.178μm in diameter were used to evaluate the cleaning abilities of the BPP-nozzle with ultrasonic. The number of particles on the entire surface of the substrate after staining were measured, giving a result of over 30000 particles. Only particles having a size of at least 0.160μm on the upper surface of the substrate were measured.

The cleaning efficiencies of the BPP-nozzle (dual type, 80mm by 200mm) and other nozzles are shown in Figure 11. As the referential nozzle, the point type ultrasonic nozzle that has been used in ULSI fabrications is used. Figure 11-(1) shows cleaning efficiency of the BPP-nozzle using UPW. It is clear that the BPP-nozzle resulted in more than 99% cleaning efficiency while the conventional shower type nozzle resulted in less than 90%, and the conventional point type nozzle scarcely removed PSL particles. Figure 11-(2) shows the cleaning efficiency of the BPP-nozzle using alkaline H_2water. The BPP-nozzle method has an excellent performance.

CONSIDERATIONS OF THE CLEANING ABILITIES OF BPP-NOZZLE METHOD

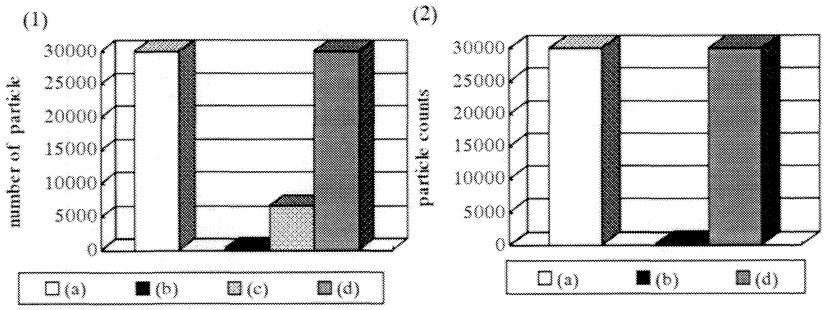

Figure 11. Cleaning efficiency of BPP-Nozzle(D)
Particle: PSL adhered in DHF Substrate: 5" Si-wafer
Cleaning solution: (1) UPW (2) H_2Water(pH 10.2) Cleaning time: 15sec
measure 0.16μm or above particle
(a)Before cleaning (overflowed at 30000 counts)
(b)BPPN 1MHz 300W 0.7L/min (substrate moving speed 10mm/s)
(c) Conventional shower type nozzle 10L/min 200rpm
(d) Conventional point type nozzle 2L/min 600rpm

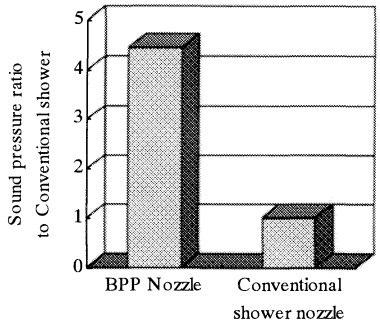

Figure 12. Sound pressure of conventional shower and BPP Nozzle

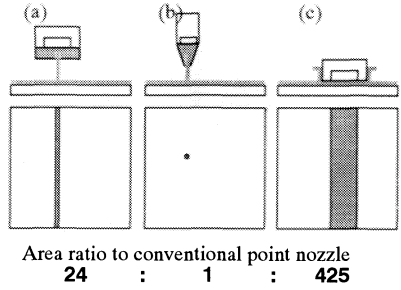

Figure 13. Megasonic irradiation area
(a) Conventional shower type nozzle
Water flow width 1.5~2mm
(b) Conventional point type nozzle
water flow ϕ4mm
(c) BPP Nozzle
transducer width 35mm

To make the reasons of the excellent cleaning abilities of the BPP-nozzle method clear, we measured sound pressure of the BPP-nozzle and the conventional nozzle. The results are shown in Figure 12. The sound pressure of the BPP-nozzle was about 4 times the sound pressure of the conventional nozzle. In this study the ultrasonic transducer in the BPP-nozzle was same as the ultrasonic transducer in the conventional shower type nozzle. The power loss of the conventional shower type nozzle is large.

Figure 13 shows the area that is cleaned in a unit of time by each nozzle method. The area that is cleaned in a unit of time by the BPP-nozzle method is the largest in this experiment. The higher sound pressure and the cleaning area in a unit of time are reasons of excellent cleaning abilities of the BPP-nozzle method.

CONCLUSIONS

The excellent cleaning abilities of the BPP-nozzle method in removing particle contaminants in LCD and ULSI fabrications and the excellent abilities of them in reducing a consumption of cleaning solution have been described. This novel cleaning technology will be soon applied to commercial plants and succeed in drastically reducing the chemicals and the UPW consumption.

We have found that 1m-scale substrate is cleaned within 30sec by 1/10 cleaning solution of the

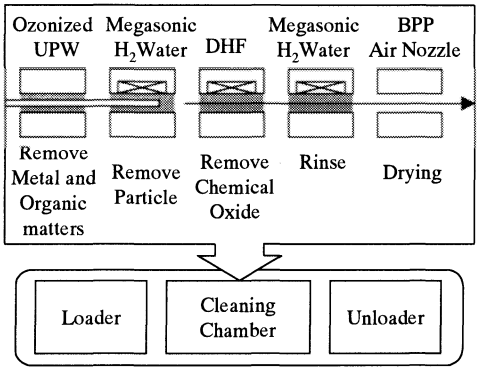

Figure 14. The new wet cleaning system

conventional method. It is shown in Figure 14 that we propose the new cleaning concept of BPP-nozzles. With clarification of details of the cleaning effects and progress in the application, the BPP-nozzle method will expand its roles in the future wet cleaning processes in LCD and ULSI manufacturing industries to harmonize manufacturing activities and environmental protection.

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TOTAL ROOM TEMPERATURE WET CLEANING PROCESS BASED ON SPECIFIC GASES DISSOLVED ULTRAPURE WATER

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An advanced total room temperature wet cleaning process (UCT cleaning) based on specific gases dissolved ultrapure water was developed. It is very simple process consisted of 4 steps only as follows; ozonated ultrapure water cleaning, small amount of ammonia added hydrogenated ultrapure water with megasonic irradiation cleaning, hydrofluoric acid and hydrogen peroxide mixture cleaning and hydrogenated ultrapure water rinse. In this process, any organic chemicals such as surfactant are not used in order to easily reclaim used water after cleaning. This cleaning technology is also effective for promoting ESH (Environment, Safety and Health) in semiconductor manufacturing, the reason why the usage of chemical and water used for wafer cleaning can be drastically reduced. The newly developed UCT cleaning process is very suitable for contamination-free surface as well as cost reduction for the future device fabrication.

INTRODUCTION

As semiconductor devices are scale down, ultra clean surface becomes even more important. In device fabrication, conventional RCA cleaning process and slightly changed one have been continuously used for past three decades[1]. They consume very large amount of chemicals and ultrapure water (UPW).

It was supposed that a drastic change for realization of ecological and high performance process was necessary. From this motivation, we have developed a total room temperature wet cleaning process, namely UCT (Ultra Clean Technology) cleaning process in 1995[2] based on mechanism of impurities adsorption and removal from silicon surface. It was an innovative process using very small amount of chemicals and UPW.

Conventional UCT cleaning process consisted of following 5 steps;

(1)ozonated ultrapure water (O_3-UPW): for removing organic impurities and noble metal

(2)HF+H_2O_2+UPW+surfactant with megasonic (mega hertz level ultrasonic) irradiation (FPMS+MS): for removing particles, metallic impurities and chemical oxide simultaneously

(3)O_3-UPW again: for removing residual chemicals such as surfactant, and etc.

(4)diluted HF (DHF) : for removal of chemical oxide

(5)final rinse

The application of O_3-UPW, surfactant and megasonic irradiation was innovative in this cleaning process. However there was some problems caused from application of surfactant.

After FPMS cleaning for removing particles, metallic impurities and chemical oxide simultaneously, the residual surfactant should be removed by O_3-UPW. The chemical oxide grown by O_3-UPW at next step is removed by DHF, resulting hydrophobic surface. Therefore, more simple cleaning process has been requested. In order to reduce process step, we developed a new cleaning technology using hydrogenated ultrapure water (H_2-UPW) with megasonic irradiation in 1997[3]. In this paper, we will present the experimental results of more simple total cleaning process based on UCT cleaning with H_2-UPW technology

ADVANCED UCT CLEANING

Design of The Process

First, H_2-UPW was tried to apply as a substitution of the surfactant in FPMS solution. FPM+H_2-UPW+MS cleaning, however, could not show good performance in terms of particle removal efficiency. It was recognized that H_2-UPW+MS cleaning was available to remove only particles with megasonic irradiation or other physical power in the phase of particle lifting off from silicon wafer surface. We found that H_2-UPW does not have specific ability to prevent adhesion of particles on silicon wafer surface.

It was recognized that FPM+H_2-UPW can not prevent re-adhesion of particles well since FPM is an acidic solution in which particles and silicon surface has a different polarity of zeta potential. To prevent adhesion of particles on silicon wafer in H_2-UPW cleaning, adding a small amount of alkaline (e.g. ammonia) to have same zeta potential between silicon surface and particles are required.

In UCT cleaning process, the most important step in the whole process was FPMS+MS treatment to remove particles, metallic contaminants and native oxide on Si surface simultaneous.

However, in advanced UCT cleaning, the purpose of the second step separated particle removal by small amount of ammonia added H_2-UPW+MS as a second step, and metallic impurities removal by FPM solution as a third step. Even though ammonia in cleaning solution is used in this new designed process, the concentration of ammonia is just 1ppm which is the concentration required to adjust pH value from 9 to 10. It is not necessary to rinse by UPW between this second step and the third step. Organic chemical free cleaning was realized by separation from FPMS+MS to small amount of ammonia added H_2-UPW+MS and FPM cleaning.

Totally, we succeeded in making more simple cleaning process which is consisted of only 4 steps. Table 1 shows advanced UCT cleaning process

Role of Each Step

First Step: O_3-UPW for Removing Organic Contaminants and Noble Metals. O_3-UPW can remove organic impurities and noble metals such as Cu and Ag, as well-known[1,4,5].

Preparation of organic contamination-free surface at first step is very important for

following steps, because cleaning solution can contact organic free silicon surface well. Figure1 shows reduction of contact angle on silicon wafer surface after O_3-UPW cleaning. Figure2 represents removal efficiency of Cu contaminants on bare silicon surface by O_3-UPW cleaning. It is found that 5ppm O_3 dissolved UPW at room temperature can remove Cu contaminant more effectively than conventional SC2 (HCl-H_2O_2-UPW) cleaning with a mixing ratio of 1:1:6 at 40C.

Second step: small amount of ammonia added H_2-UPW+MS cleaning for removing particles. The removal efficiency of Al_2O_3 particle more than 0.2 um by 1ppm-NH_3 added H_2-UPW+MS was presented[3]. It is found that Al_2O_3 particles more than 0.12 micron can be removed perfectly as well as more than 0.2 um as shown in Fig.3. Moreover, Fig.4. displays the removal rate of dried silica (SiO_2) particles from wafer as a model after CMP process, and it is confirmed that SiO_2 particles more than 0.12 um is removed very effectively by ammonia added H_2-UPW+MS.

A neutral H_2-UPW+MS without any ammonia dosing is also effective to remove SiO_2 particles from wafer surface. It is supposed that the silicon oxide surface and the silica slurry have electrical repulsive force after lifting off, the reason why the zeta potential of oxide surface and slurry has same polarity. Figure 5 shows relationship between pH and zeta potential of some materials in aqueous solution, and Figure 6 shows a model of behavior of Al_2O_3 and SiO_2 particles near wafer surface.

SiO_2 particles on wafer surface are perfectly removed by H_2-UPW+MS in 10 seconds only even in case of solution without adding any chemical in it. Any SiO_2 particles, however, were not removed by only UPW+MS or 1ppm-NH_3 added UPW+MS cleaning.

It is supposed that dissolved hydrogen is available to detach particles from wafer surface with megasonic irradiation or other suitable physical power. Small amount of ammonia (less than 5ppm) added H_2-UPW does not etch silicon oxide surface substantially. It was also confirmed that flatness of the wafer surface after cleaning by small amount of ammonia added H_2-UPW+MS is not changed at all.

Third step: FPM for removing metallic impurities. Two mechanisms for the adsorption and desorption of metallic impurities on silicon wafer surfaces : 1) Noble metals with a higher electronegativity than that of silicon such as Cu, Ag, and Au take electrons from the surface to form direct chemical bonds with surface. and 2) Base metals, with a lower electronegativity than silicon such as Fe, Ni, Cr, Al, Ca, Na, K and etc. are easily ionized in the solution and included in the native or chemical oxide on the surface from which these metals are easily removed with the native or chemical oxide by dilute HF treatment. In device fabrication, it is required to removed irrespective of the kinds of metallic impurities.

FPM solution with oxide etching capability and higher redox potential value is recognized as most effective solution to remove them.[4,6].

Fourth step: H_2-UPW+MS for final rinse, suppression of native oxide growth and particle re-adhesion and enhancement of hydrogen termination. From first through third steps, all impurities are removed from wafer surface. Purpose of fourth step is removal of residual chemicals such as HF and H_2O_2 without generating any contamination on silicon surface. The H_2-UPW is more effective to suppress native oxide growth in rinse step than well-known de-oxygenated UPW. By employing MS irradiation, H_2-UPW can also protect particles re-adhesion.

Moreover, it is confirmed that H_2-UPW and hydrogen radical drying can enhance hydrogen termination of silicon surface. Figure 7 shows hydrogen termination level after rinsing and drying.

This advanced UCT cleaning process is designed to apply it to pre-cleaning of gate oxidation process, obtaining contamination-free silicon surface after final rinse step. Both of H_2-UPW and O_3-UPW produced by the gas dissolving system using proper materials can be applied even in the final rinse step since they continuously maintain a high grade purity.

SUMMARY

An advanced UCT cleaning process which consists of total four steps with H_2-UPW cleaning technology was established by improving conventional UCT cleaning process. It is very simple process without using organic chemicals such as surfactant. Except third step of all processes, only small quantity chemical in specific gases dissolved UPW (O_3-UPW and H_2-UPW) is used. The wasted water from first, second and fourth steps in this process can be very easy to reclaim and reuse. Even in batch type cleaning process, fresh O_3-UPW and H_2-UPW can be used by one pass style like as UPW rinse without consuming the amount of UPW.

We suppose that the advanced UCT cleaning process will be adopted in future device fabrication to realize cost reduction and promotion of ESH (Environment, Safety and Health) in semiconductor manufacturing.

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Table 1 Advanced UCT Cleaning Process (4 steps)

Step	Purpose
‡ O3-UPW □ (O3: 5ppm) □ «	Organic, Noble Metal Removal
‡ H2-UPW + MS □ (H2: 1.2□ 1.6ppm, pH9.3) □ «	Particle Removal
‡ FPM □ (0.5%HF + 0.5%H2O2) □ «	Metal,Chemical Oxide Removal HydrogenTermination
‡ H2-UPW + MS (H2: 1.2□ 1.6ppm)	Final Rinse Prevention of Native Oxide Growth and Particle Re-Adhesion

Reference: Conventional UCT Cleaning Process

‡ O3-UPW (O3:5ppm) □ «	Organic, Noble Metal
‡ APMS+MS HF/H2O2/H2O/Surfactant + Megasonic □ «	Particle, Metal, Chemical Oxide
‡ O3-UPW □ «	Chemical residue, Surfactant
‡ DHF + O3-UPW □ «	Chemical Oxide
‡ H2-UPW Rinse	inal Rinse **Prevention of Native Oxide Growth**

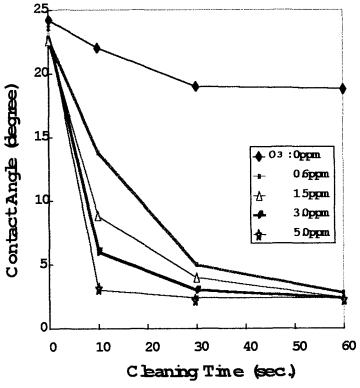


Figure 1 Contact Angle of Silicon Wafer Surface

Initial : silicon wafer exposed in clean room for 5days after SPM(H_2SO_4+H_2O_2)
cleaning : 1L/min. 500rpm

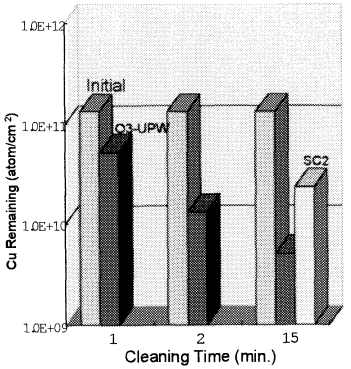


Figure 2 Cu Contaminants Removal by O3-UPW

O_3-UPW : 5ppm-O_3, 4ppm-HCl, 25 □ □
SC2 : HCl : H_2O_2 : H_2O = 1:1:6, 40 □ □

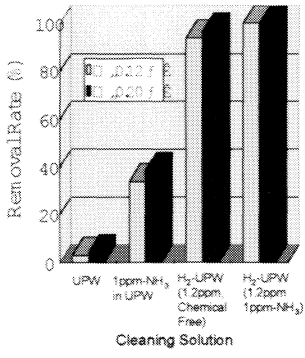
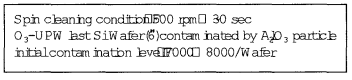


Figure 3 Removal Effitiency of Al2O3 Particle



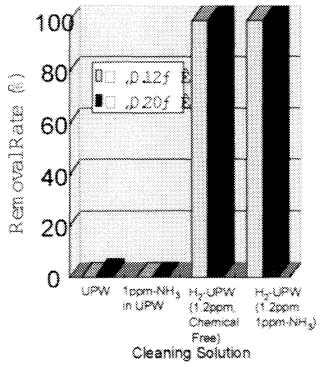
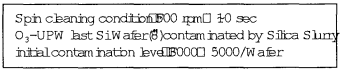


Figure 4 Removal Efficiensy of Dried Silica Slurry for CMP Process



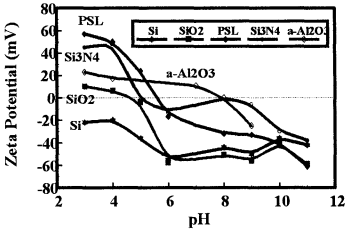


Figure 5 Relationship between pH and zeta potentias of some materials in aqueous solution

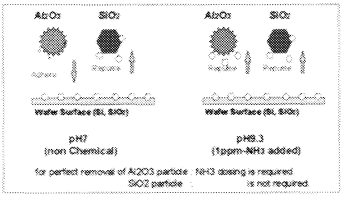


Figure 6 Model: Particle adhesion and Repulse on wafer surface

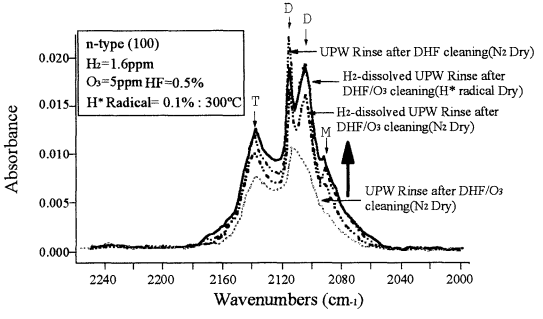


Figure 7 Increase of Hydrogen Termination by H2-UPW Rinse and hydrogen radical drying

ON-PRODUCT EVALUATION OF WAFER-SURFACE PRECLEAN PROCESSES ON CMOS GATE-OXIDE INTEGRITY

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ABSTRACT

Significant improvements in gate-oxide dielectric integrity have been electrically quantified in a CMOS semiconductor manufacturing environment. A primary improvement in gate-oxide integrity has been attributed to the application of megasonic agitation in traditional tank SC-1/SC-2 wafer-surface cleaning solutions used immediately prior to gate oxidation. A secondary gate-oxide improvement has been attributed to the use of an IBM-patented tank SP(F)M solution that exhibits unique chemophobic wafer-surface wetting characteristics. This paper compares two industry-standard wafer-surface preparation process-cleaning options and summarizes experimentally obtained on-product electrical test site data.

INTRODUCTION

At a previous Electrochemical Society (ECS) meeting, monitor-wafer experimental findings were presented which demonstrated significant and repeatable particulate-based, wafer-surface foreign material reductions with the application of megasonic agitation to industry-standard SC-1 and SC-2 cleaning solutions. At a subsequent ECS meeting, a second and independent monitor-wafer experimental finding was presented that demonstrated additional and repeatable small-particle, wafer-surface foreign material reductions with the reversal of wafer-surface wetting properties of a traditional tank-based SPM cleaning solution. This paper discusses on-product, in-line electrical test site data from the combination of these two independent findings. The information presented represents some of the seminal work for IBM's advanced thin-gate oxidation preclean wafer-surface preparation processes in manufacturing today.

BACKGROUND

The experimental application of megasonic agitation techniques to industry-standard SC-1/2 wafer-cleaning solutions has proven to be extremely beneficial for lowering wafer-surface particle defect-density levels (1). Another group of experiments with dip-tank sulfuric-acid : hydrogen-peroxide mixtures (SPM) also demonstrated additional wafer-surface foreign material as well as time-dependent wafer-hazing benefits (2). These benefits resulted from the addition of very small quantities of a fluorine-containing compound to SPM solutions to form an SP(F)M solution (3). Adding fluorine caused the wafer-surface wetting properties of the SP(F)M solution to be completely reversed from chemophilic to chemophobic. This result was seen with bare silicon as well as silicon-dioxide wafer surfaces.

MEGASONIC SC-1 / SC-2 WAFER-CLEANING SOLUTIONS

Spray wet-chemical processing has been demonstrated to remove a large percentage of optically measurable particles from wafer surfaces. However, experiments have shown that, although spray tools are good for metal and organic removal from wafer surfaces, they do not efficiently remove very small particle-based contaminants with a high degree of efficiency (1). Because of the classic fluid-dynamic boundary-layer phenomena, contamination can be trapped in the laminar layer at the wafer surface despite high-velocity and high-volume chemical sprays and extensive subsequent DI-water rinsing.

Figure 1 shows very small particles being trapped in the laminar/turbulent boundary layer of a fluid on a wafer surface. The wafer surface defect magnification effect of the conformal deposition characteristics of polysilicon low pressure chemical vapor deposition (LPCVD) is also shown.

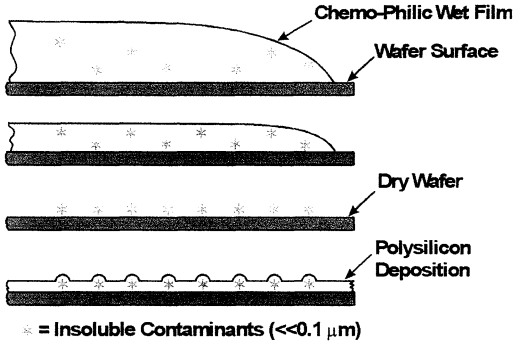

Figure 1. Insoluble contaminants in a chemical solution.

Megasonic wafer-cleaning technology greatly reduces traditional fluid-dynamic wafer-cleaning limitations and focuses attention where it belongs, at the wafer surface. Utilizing the incompressibility and excellent energy transmissibility of liquids in conjunction with the chemical-cleaning and gas-evolving properties of SC-1/SC-2 solutions, major reductions in particle-based wafer surface defect densities have been achieved at IBM's advanced semiconductor manufacturing facility in Essex Junction, Vermont

Figure 2 demonstrates the monitor-wafer foreign material (FM) removal efficiency of various megasonic power levels in an SC-1/2 tank versus SC-1/2 spray wet chemical processor. At higher power levels, the first-order FM removal efficiency of a megasonic SC-1/2 system is much improved over an SC-1/2 wet chemical spray processor.

The chemical conditions were:

1) Megasonic SC-1 tank: Temp: 55C, 5:1:1 (H_2O:NH_4OH:H_2O_2), 10-min immersion
2) Megasonic SC-2 tank: Temp: 55C, 5:1:1 (H_2O:HCl:H_2O_2), 10-min immersion

The SC-1 and SC-2 tank processes were previously optimized for efficient FM removal from the wafer surface. Standard deionized (DI) water overflow rinses and a centrifuge dryer were used.

Figure 3 illustrates wafer FM levels after polysilicon deposition of the monitor wafers used in the experiment of Figure 2. These wafers were processed through a 430nm polysilicon LPCVD process to magnify the size of particles present on the wafer surface. Figure 3 data show significantly lower FM remaining on the wafer surface when compared to spray chemical SC-1/2 processing at all megasonic SC-1/2 power levels.

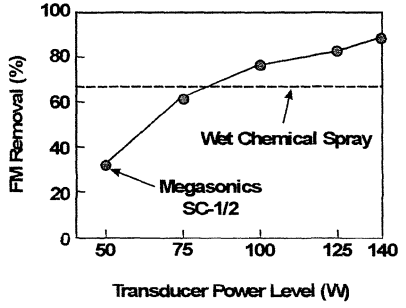

Figure 2. FM removal efficiency vs. tranducer power.

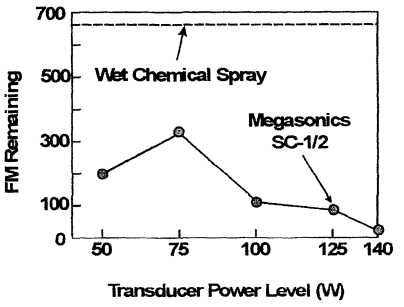

Figure 3. Comparison of remaining FM and transducer power after polysilicon deposition.

The SC-1 and SC-2 wet chemical tank processes for this experimentation were done in an IBM-customized tank design. The design incorporated bottom-mounted, direct-coupled, tantalum-covered megasonic transducers with 140 watts of input power at a frequency of about 0.95MHz. Cassettes of 25 wafers were fully immersed in the solutions and cycled over the megasonic transducers using an external chain-drive mechanism.

SPM VERSUS SP(F)M WAFER-CLEANING SOLUTIONS

A standard SPM solution is a nominal mixture of sulfuric acid and hydrogen peroxide in a range of chemical proportions. When used in a dip-tank application, the solution is heated and maintained at a temperature of between 90C to 130C. In spray wet-chemical applications, the temperature of the SPM mixture is controlled by the instantaneous heat of reaction of the chemical ratio being sprayed and chemical atomization pressures used.

The SP(F)M solution is an IBM-patented solution that varies only slightly from the standard SPM solution in that it has a small quantity of a fluorine-containing compound added to the solution during the initial formulation of the solution (3). When formulated as prescribed, SP(F)M solutions exhibit vastly different wetting properties on wafer surfaces exposed to it. While an SPM solution is chemophillic and tends to readily adhere to wafer surfaces, an SP(F)M solution is highly chemophobic and will not adhere to silicon or silicon-dioxide wafer surfaces. An SP(F)M solution immediately beads and drains from a wafer surface as the wafer is removed from a solution-containing process tank.

The reversal of wafer surface wetting properties of the SP(F)M solution has been shown to eliminate large quantities of very small particles, probably silicates, from the wafer surface. Due to their small size (<0.1μm), these wafer surface particles are not easily measured with traditional light-scattering inspection tools. In many cases, these particles only appear after subsequent wafer processing. This is especially true with the conformal film deposition characteristics of polysilicon deposition (Figure 3). Because sulfuric acid has a highly viscous nature, it is difficult to filter effectively and troublesome to rinse from a wafer surface.

The scanning electron microscope (SEM) micrographs in Figure 4 show bare silicon monitor wafers exposed to either SPM or SP(F)M solutions and then moved through the same process run for polysilicon LPCVD. The SP(F)M tank processing was done in a non-recirculated, batch-processing immersion tank. The solution was initially mixed in a 4:1 ratio of sulfuric acid and hydrogen peroxide, respectively, with a small quantity of fluorine containing compound added during initial mixing. The tank temperature of the solution was controlled to 95C with installed electrical heaters. Immersion time in the SP(F)M solution was three minutes.

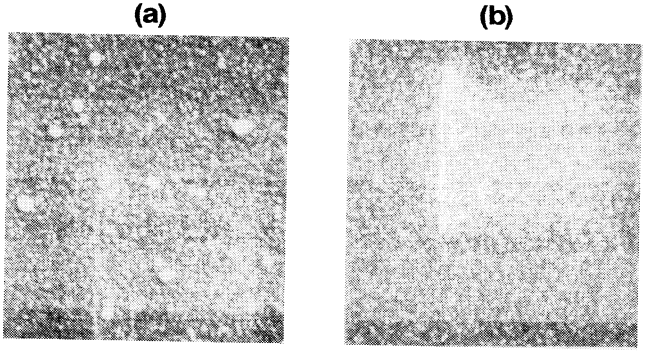

Figure 4. SEM Micrographs: (a) Tank SPM cleaned wafer post polysilicon deposition; (b) Tank SP(F)M cleaned wafer post polysilicon deposition

ON-PRODUCT EXPERIMENT 1

Two on-product experiments were conducted to evaluate potential gate oxide dielectric integrity improvements using the SP(F)M and megasonic SC-1/2 cleaning processes. A spray chemical-based process of record (POR) SPM + DHF + SC1/2(5:1:1, 60C) and immersion-tank-based SP(F)M + DHF + megasonic SC1/2 wafer-cleaning processes were compared.

In the first experiment, four lots of CMOS manufacturing product wafers were split. The first split was performed at the ion-implant screen-oxidation preclean step. Here an earlier sacrificial oxide is stripped and the ion implant screen thermal silicon dioxide grown. With subsequent standard product processing, the lots were split identically at the gate dielectric thermal oxidation preclean step. Here the screen oxide is stripped and gate

dielectric grown. Each of the four product lots contained two splits of 10 wafers each, or 40 wafers per experimental split.

The four product lots were then processed as normal manufacturing product without further experimental work. The lots were processed from the 13.5nm gate dielectric oxidation step to the first photo-mask level of device interconnect metalization (M1). A special M1 mask was designed, built and used for testing to electrically connect a large number of gate oxide structures within each chip.

After the M1 step, ten chips on each wafer within each product lot were electrically tested in-line for gate-oxide integrity; both N-FET's and P-FET's on the device were included. Voltage breakdown data were then summarized by experimental split. Summary data from each experimental split represents about 400 data points of integrity for a very large number of gate-oxide structures and corresponding effective area.

EXPERIMENT 1 RESULTS AND DISCUSSION

Table 1 is categorized by the level of electrical voltage applied across the tested gate-oxide structures. The range of $0 < X < 3.6V$ is considered to be the Time Zero, or T-Zero, yield of the 3.6V device. The voltage range of $3.6V < Y < 15V$ is considered to be the tunneling yield, or point at which the oxide conducts current or leaks electrical charge. Data in the table are for the N-Well (P-FET device) regions of the chips tested. The non-N-Well ion-implanted regions (N-FET devices) were not at issue and unaffected by the experimental processing.

Table I. Spray vs. tank-megasonic gate oxide integrity.

Voltage Stress Fallout Range (V)	**Spray Processing SPM + DHF + SC1/2(%)**	**Tank Processing SP(F)M + DHF + MEG SC1/2(%)**
T-Zero: $0 < X < 3.6$	93.8	100
Tunneling: $3.6 < Y < 15.0$	63.8	100

The table 1 data show significant improvements in on-product device electrical test site yield for the immersion tank SP(F)M and megasonic SC-1/2 processes when used in both the screen oxide and gate oxide preclean processes. The POR electrical data for the spray chemical processor experimental splits (SPM and SC-1/2 processes) was typical of the CMOS devices at the time.

ON-PRODUCT EXPERIMENT 2

The improvement in gate oxide test site yield observed in the original on-product experiments invited a second evaluation. The immersion tank SP(F)M and megasonic SC-1/2 processes were used at BOTH screen oxidation and gate oxidation preclean. Therefore, determining which process, SP(F)M or megasonic SC-1/2, or which process step, screen oxidation preclean or gate oxidation preclean, had the biggest benefit to gate oxide integrity could not be identified.

In the second experiment, three additional lots of identical CMOS manufacturing product wafers were experimentally split at the same two thin-oxide preclean sectors.

However, for work at the screen-oxidation preclean and gate-oxidation preclean split that follows, each of the process steps (e.g., spray SPM, tank SP(F)M, spray SC-1/2, megasonic SC-1/2) were controlled separately versus POR processing. An "All POR" experimental control cell was also included. The experimental table was developed and is shown in Table 2.

Table II. Matrix: oxidation preclean process used vs. product preclean step.

CLEANING EVALUATION **THIN-OXIDE PRECLEAN STEP**	Tank SP(F)M (only)	Megasonics SC-1/2 (only)	TANK SP(F)M + Megasonics SC-1/2	Process of Record (spray chemical only)
SCREEN OXIDATION (only)	Tank SP(F)M + Spray DHF + SC-1/2 @ Screen Ox	Spray SPM + Tank DHF + Meg SC-1/2 @ Screen Ox	Tank SP(F)M + DHF + MEG SC-1/2 @ Screen Ox	(not applicable)
	All-Spray @ Gate Ox	All-Spray @ Gate Ox	All-Spray @ Gate Ox	
GATE OXIDATION (only)	All-Spray @ Screen Ox	All-Spray @ Screen Ox	All-Spray @ Screen Ox	(not applicable)
	Tank SP(F)M + Spray DHF + SC-1/2 @ Gate Ox	Spray SPM + Tank DHF + Meg SC-1/2 @Gate Ox	Tank SP(F)M + DHF + Meg SC-1/2 @ Gate Ox	
SCREEN OXIDATION + GATE OXIDATION (combined)	Tank SP(F)M + Spray DHF + SC-1/2 @ Screen + Gate	Spray SPM + Tank DHF + Meg SC-1/2 @ Screen + Gate	Tank SP(F)M + DHF + MEG SC-1/2 @ Screen + Gate	Spray SPM + DHF + SC-1/2 @ Screen + Gate

With standard subsequent product processing, the three lots were split identically at the gate dielectric oxidation preclean step. Thus, each of the three product lots contained 10 splits of three wafers each, or nine wafers per experimental split. The lots were then processed as normal manufacturing product, without any further experimental work, from the 13.5nm gate dielectric oxidation step to M1 where the special M1 mask was used.

After M1, 10 chips on each wafer within each lot were electrically tested in-line for gate-oxide integrity. Voltage breakdown data were then summarized by experimental split. Therefore, the summarized data from each experimental split represents about 90 data

points of the gate-oxide integrity of a very large number of gate-oxide structures and corresponding gate-oxide effective area.

EXPERIMENT 2 RESULTS AND DISCUSSION

Table 3 data are categorized by the level of electrical voltage applied across the gate-oxide structure being tested

Table III. Gate oxide integrity preclean breakout matrix.

Process Step	Voltage Stress Fallout Range(V)	Tank SP(F)M + Spray DHF + Spray SC-1/2 (%)	Spray SPM + Tank DHF + Meg SC-1/2 (%)	Tank SP(F)M + Tank DHF + Meg SC-1/2 (%)	POR (All Spray) SPM + DHF + SC-1/2 (%)
Screen	0 < X < 3.6	98.6	93.8	98.4	n/a
(only)	3.6 < Y < 15.0	75.5	70.8	71.3	n/a
Gate	0 < X < 3.6	95	100	97.5	n/a
(only)	3.6 < Y < 15.0	75.1	97.2	96.2	n/a
Screen + Gate	0 < X < 3.6	96.7	100	100	98□
	3.6 < Y < 15.0	81.1	97.5	100	69.5

The on-product electrical test-site data of Experiment 2 in Table 3 shows a nearly identical gate-oxide yield result to that found in Experiment 1. Again, the spray-chemical POR cell electrical test-site yield was typical of CMOS product, and the all-experimental processing of tank SP(F)M + DHF + megasonic SC-1/SC-2 at both screen oxide and gate-oxide preclean repeated its significant positive result.

Finally, data in Table 3 answer the question of which process, SP(F)M or megasonic SC-1/2, or which process step, screen-oxidation preclean or gate-oxidation preclean, provided the biggest benefit to gate-oxide integrity in this experiment. A graphic display of the tunneling yield data from Table 3 shows it the best and is shown in Figure 5.

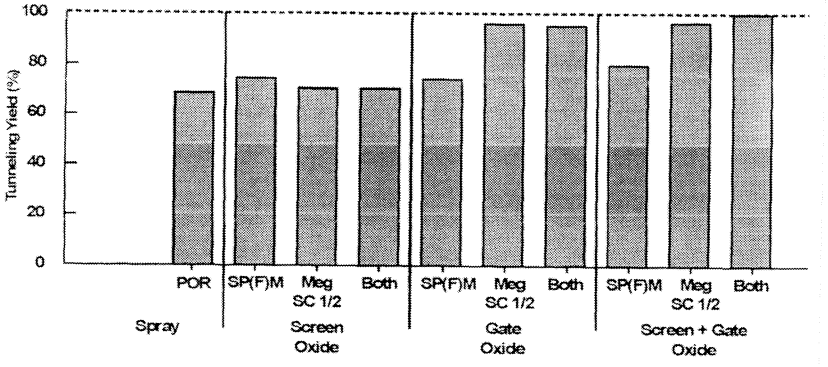

Figure 5. CMOS gate oxide tunneling yield vs. oxidation preclean.

Tunneling yield data show neither experimental processing at screen oxidation preclean nor the use of an SP(F)M solution resulted in any apparent first-order improvements in gate-oxide electrical test site yield. However, the use of megasonic SC-1/2 in place of the wet-chemical-spray SC-1/2 for the gate-oxidation preclean step resulted in a significant improvement in this test-site yield. Furthermore, our data show that all four experimental cells using megasonic SC-1/2 for gate-oxidation preclean were improved. Finally, to obtain optimal gate-oxide electrical test-site yield, both the SP(F)M and megasonic SC-1/2 had to be used in place of wet chemical spray at both the screen-oxidation and gate-oxidation preclean steps.

CONCLUSIONS

A useful method for on-product electrical testing of device oxide quality has been demonstrated. The influence of some thin-oxidation preclean wet processes on gate-oxide integrity as measured with in-line on-product electrical testing techniques was also described.

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EVALUATION OF ADVANCED PRE-GATE CLEANINGS

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ABSTRACT

In order to meet stricter wafer cleanliness requirements, emerging environmental concerns and more stringent cost-effectiveness criteria, wafer cleaning technology is moving slowly away from the conventional RCA-based processes. In this paper, the cleaning efficiency of different advanced pre-gate cleaning processes, all carried out in the same Wet Bench is compared. Dilute RCA, Diluted Dynamic Clean (HF/ Ozone- based process) and AFEOL (combination of diluted SC1, HF and Ozone chemistry) are evaluated in terms of metal and particle removal performance and major surface characteristics (surface roughness and minority carrier lifetime). Silicon and oxide consumption were also studied. Electrical evaluation was made on patterned Gate Oxide structures and electrical results from split lots with the optimized recipes are compared with those obtained with the conventional RCA process. Robustness of these three advanced cleaning processes is clearly established and we demonstrate that they perform at least as well as the standard RCA.

INTRODUCTION

Pre-gate cleaning is unanimously considered as one of the key parameters governing thin gate oxide integrity and hence final device performance and yield. However, despite increasingly stringent process demands (cf. SIA road map), the basic cleaning recipe has remained almost unchanged since 1965. The RCA clean [1], in its multiple forms, is still the choice of preference for FEOL cleaning sequences in IC manufacturing around the world. The reason is simple: concentrated $NH_4OH/ H_2O_2/ H_2O$ mixture (SC1) performs very well for particle removal, and so does the $HCl/ H_2O_2/ H_2O$ mixture (SC2) for metallic contaminants.

Recently cost-effectiveness and environmental concerns pushed considerable research efforts to optimize the RCA sequence and to develop alternative cleaning techniques. The first approach consists of diluting the SC1 and SC2 solutions, thus enabling important chemical savings at the same overall performances of the process. But implementation of diluted chemistries is not straightforward and there are many pitfalls to be avoided. Even then, some of the intrinsic limitations of the conventional RCA still remain valid for dRCA: high process temperatures (which is responsible for the major part of chemical consumption by evaporation) and multiple process steps. The use of diluted chemicals at room temperature represents another approach. The main new technological concepts have been introduced by IMEC [2], LETI [3] and professor Ohmi [4]. They all rely on HF-Ozone chemistry and include several sequences of ozonated water rinse(s) and dilute HF treatment(s). Basically the first Ozone step removes organics, noble metals, and

oxidizes the wafer surface. The subsequent HF step removes the oxide as well as any embedded particles and metals. An additional ozone step is usually implemented to convert the hydrophobic surface to a more stable hydrophilic one. The reluctance of IC industry to adopt these relatively new cleaning strategies (even if very good performances have been extensively reported) suggests that an alternative intermediate approach is needed.

In this paper, a dilute RCA is proposed and the implementation of it in the wet bench is discussed. We present the latest technical advances in DDC. We also introduce a new Advanced Front End of the Line Cleaning, AFEOL, which consists of a combination of an HF-Ozone and a dilute SC1 chemistry (one could call this an intermediate approach between the dRCA and the DDC process).

The exact process sequences are detailed in Table I. The cleaning robustness of these different advanced pre-gate cleanings is extensively analyzed and discussed.

EXPERIMENTAL

All processes were conducted in a fully automated GAMA-1™ wet station from AKrion on 200mm, CZ, p-type, 7-10 Ω.cm wafers from SEH. The chemical tanks are recirculated and filtered. The SC1 tank is equipped with a Phaser Water Coupled Megasonic (peak energy ~ 5W/cm2) and the HF-HCl rinse tank with a Direct Coupled Megasonic (peak energy ~ 10W/cm2).

Some wafers were intentionally contaminated with different types of particles (with various Zeta potentials) or metals (with different electrochemical properties) to compare the Particle Removal Efficiency (*PRE)* and the Metal Removal Efficiency (*MRE)*.

The contamination procedure for SiO_2 and Al_2O_3 particles is a short dip in DI water in which commercially available particles had been dispersed. Si_3N_4 contaminated wafers were obtained by dipping clean wafers in a static contaminated H_3PO_4 etch bath. Note that *PRE* is strongly dependent on initial counts and on the initial conditioning of wafers (cleaning before contamination). Therefore all experiments on contaminated wafers were carried out on samples from the same batch. Particle measurements were carried out on a TENCOR Surfscan 6200 (particle size: 0,16µm and upwards).

The procedure for metal contamination consists of an immersion in a SC1 solution (0,25/1/5 @ 25°C) previously spiked with standard Fe, Zn, Ni, Ca, ... solutions. Metallic contamination levels were detected by means of Vapor-Phase Decomposition TXRF (RIGAKU) and/ or VPD ICP (VARIAN). The detection limit of these techniques is $\sim 10^9$ atoms/cm^2 for the investigated elements (see Table II).

Non-contact methods for characterizing silicon surface properties after the cleaning process were used: Microwave PhotoConductivity Decay (µPCD) on a WT-85 Lifetime scanner from SEMILAB, and Surface Charge Profiler (SCP) on a SCP Model 100 from QC SOLUTIONS.

Wafer surface roughness was analyzed by means of Atomic Force Microscopy (Nanoscope III from DIGITAL INSTRUMENTS), rms roughness and number of "high peaks" being estimated from several 1µm × 1µm scans recorded in tapping mode. Some wafers were intentionally "roughened" in a 1% HF solution to generate "high peaks" on the silicon surface. Afterwards the "high peak removal ability" of the different cleaning processes was measured.

Etch rates and global process consumption of silicon and equivalent thermal oxide were determined with a 1280 KLA-TENCOR spectroscopic ellipsometer.

Finally, 70Å gate oxide structures of various area were patterned on split lots. Dry oxidation processes were prefered (no HCl species in the furnace) and conventional electrical tests were carried out on wafers after PolySilicon deposition and etch (test for EBD, QBD, Breakdown voltage, defect density).

RCA	Time (min)	Goal
SC1 0.25/1/5 @ 65°C	10	Particle removal
Hot rinse	10	rinse
SC2 1/1/5 @ 50°C	10	Metals removal
Hot rinse	10	rinse
Final rinse	10	rinse
IPA DRY	7	Dry
	57	

d RCA	Time (min)	Goal
dSC1 0.25/1/20 @ 65°C	10	Particle removal
Hot rinse	7,5	rinse
dSC2 1/0/250 @ 65°C	10	Metals removal
Hot rinse	5	rinse
IPA DRY	7	Dry
	39,5	

DDC	Time (min)	Goal
O_3 10ppm	5	CHx + noble metal
HF-HCl 1/1/100 @ 23°C	0,5	Chem. oxide + metals removal
Rinse (0.01% HCl)	3	rinse
O_3 3ppm	7	Particle removal
HF-HCl 1/1/100 @ 23°C	0,33	
Rinse (0.01% HCl)	3	rinse
O_3 5ppm	7	Final Passivation
IPA DRY	7	Dry
	33	

AFEOL	Time (min)	Goal
O_3 10ppm	5	CHx + noble metal
dSC1 0.25/1/20 @ 65°C	7,5	Particle removal
Hot rinse	7,5	rinse
HF-HCl 1/1/100 @ 23°C	0,5	Chem. Oxide + metal removal
Rinse (0.01% HCl)	3	rinse
O_3 5ppm	7	Final Passivation
IPA DRY	7	Dry
	37,5	

Table 1: *Description of different cleaning recipes studied. (Shaded cells indicate megasonic activation during the sequence)*

RESULTS AND DISCUSSION

Particle contamination removal

We investigated both the particle addition on clean bare silicon wafers (initial count < 10 Lpds @ 0,16μm) and the PRE of different particle types.

- In the SC1 chemistry, particles are removed by the continuous oxidizing and etching effect of the NH_4OH/ H_2O_2 mixture, the ratio of these chemicals being the critical parameter since it determines the chemical dissolution rate of the surface layer to which the particle is attached (under-etching mechanism). While optimizing the dilute SC1 solution, the NH_4OH/ H_2O_2 ratio was kept constant which has proven to result in a similar etch behaviour of Si and SiO2 up to 0,25/1/500 [5]. An optimal working point at 0,25/1/20 was clearly established for the removal of all particle types we investigated (confirmation of a previous result obtained on Al_2O_3 slurries [5]).

As can be observed from fig. 1B, this optimized dilute SC1 (used both in dRCA and AFEOL sequences) outperforms the conventional concentrated SC1 step. This, on first sight, strange behaviour is explained by the fact that the propagation of megasonic energy is enhanced at higher chemical dilution ratios due to lower gas bubble formation [6].

- Earlier, HF-based chemistries (DDC) didn't perform as well as expected [7]; this was mainly due to hardware limitations. As can be seen on Fig. 1A, the use of new carriers drastically reduces the particle adders and the Direct Coupled Megasonic energy used during the Ozone + HCl rinse cycles has a major impact on the overall PRE. Under these

conditions, excellent particle removal results are obtained by combining the under-etching effect (Ozone/ HF sequence) and the Zeta potential control (HF-HCl mixture).
Note that these hardware improvements also affect the AFEOL cleaning since it prevents any particle (re)contamination of the wafers after the dilute SC1 step.

Finally, if we compare the four cleaning processes (Fig. 1B), the conventional RCA is obviously the lesser performer.

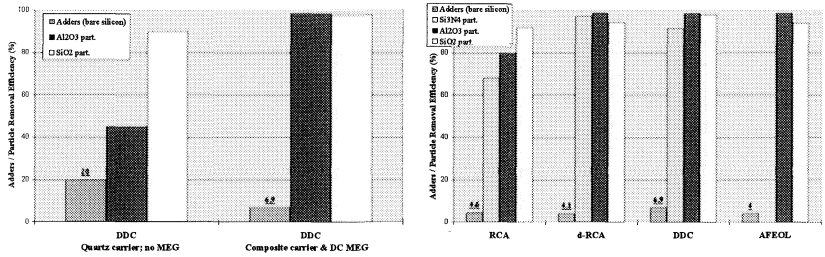

Fig. 1: *Particle performances measured @ 0.2μm (except adders @ 0.16μm). Left (1A): Improvement of HF-based chemistry. Right (1B): Comparison of different cleanings.*

Recently, the understanding of the fundamental of particle// substrate interactions has progressed significantly (influence of ionic strength, Zeta potential, temperature, megasonic, dissolved gas, ... [8]). Taking into account these parameters in the advanced cleanings cycles will be crucial for future developments. On the other hand, diluting the SC1 even more immediately raises some critical issues for chemical concentration control systems and megasonic technology (frequency, power) [6].

Metal contamination removal

Provided that high process temperature is maintained, strongly diluted HCl mixtures (up to 1/1000) are as effective in the removal of metals as the standard concentrated SC2 solution [9,10]. Optimizing the dilute SC2 solution, we fixed the HCl/ H_2O_2/ H_2O ratio at 1/0/250 (peroxide is completely left out) and increased the temperature to 65°C (pH ~1,4). This moderate dilution ratio enables us to keep the chemical concentration in the bath under tight control by conductivity control (ICE™ regulation system) with a bath lifetime exceeding 2 days.

- Metallic contamination levels on cleaned "out of the box" wafers (VPD-TXRF or VPD-ICP measurements) are below detection limits of these techniques for all four cleaning processes. Table II presents the residual contamination levels measured after cleaning wafers that were first contaminated in a "spiked" SC1 solution. As is shown, all processes indicate good and even excellent abilities to remove high initial contamination levels (up to 10^{13} at./cm^2). Unfortunately, since most of the residual levels are at or below the detection limits of the available analysis techniques, a relevant comparison between the MRE of the different cleaning sequences is impossible.

*1E9at/cm2	Ca	Fe	Cr	Ni	Zn
LLD	1.4	2.1	0.16	0.06	1.1
Init. cont. level	9300	2050	13	17	17500
Post RCA	6.8	< lld	na	0.64	< lld
Post d-RCA	< lld	< lld	0.25	0.28	< lld
Post DDC	1.5	2.6	0.48	0.18	< lld
Post AFEOL	5.3	2.5	0.53	0.18	< lld

Table II: *Residual metallic contamination levels (after cleaning intentionally contaminated wafers).*

- SCP and μ-PCD measurements were also carried out. Indeed these techniques are very sensitive to metallic contamination (especially to iron for μ-PCD) and can be used for controlling the cleaning robustness [11].
Surface lifetime data measured by SCP and μ-PCD are reported in table III (τ_{scp} correspond to surface recombination lifetime, $\tau_{\mu pcd}$ to minority carrier lifetime). A noticeable difference appears between the wafers which are treated with a RCA/ dRCA clean or a DDC/ AFEOL clean. The distinction is even more pronounced for initially contaminated wafers (initial contamination levels are the same as those given in Table II). This indicates that the residual metallic contamination for these two groups of processes is slightly different. However one should keep in mind that in a first order approximation, $\tau_{\mu pcd}$ is inversely proportional to iron concentration: $[Fe] = (\tau_{\mu pcd})^{-1} * 5.10^{11}$ [11]. Hence the difference of 50μs measured by μ-PCD only represents a variation from 2.5 to 3.3 $*10^9$ at./cm^2. As mentioned above, in this range, the variations are hardly detected by analytical techniques.

Life time (μs)	SCP "Out of the box" Wafers	μ-PCD "Out of the box" Wafers	μ-PCD Met. conta. Wafers
RCA	18	191	168
d-RCA	39	180	166
DDC	56	203	209
AFEOL	68	201	216

Table III: *SCP and μ-PCD Life-Time measurements.*
SCP characterization is performed just after cleaning. μ-PCD measurements are carried out after oxidation (a thermal process is required to drive the surface Fe into the bulk of silicon).

At this point we can conclude that there is no major metallic contamination (removal) concern for any of the cleaning processes: **Alternative cleanings perform as good as conventional RCA process**, at least to the $1*10^9$ at./cm^2 level.
In the case of DDC and AFEOL processes, the key feature is the presence of chlorides in both the HF step and the final passivation step. In the dilute RCA approach, the critical parameter is the temperature. However when diluting the SC2 even further, metallic

(re)contamination during the final rinse can become an issue. Then the injection of trace amounts of HCl during the final rinse would be recommended.

Silicon Surface Roughness

To which extent Si surface roughness affects the gate-oxide integrity is still a controversial issue. Indeed when "unrealistic roughening" of the silicon surface is obtained (either by long treatment in BHF [12], or in hot DI water [13] or in alkali solution [14]), a yield loss is detected. On the other hand, the correlation between rms roughness and intrinsic oxide performances is not so clear when relatively smooth surfaces (low rms roughness) are involved [10]. This is actually the case since the rms roughness values we measured were between 0.9 to 1.3Å for RCA, dRCA or DDC clean and slightly higher for AFEOL ~2Å (HF RCA sequence also leads to ~2Å).
However what can drastically affect the intrinsic properties of gate oxide structures is the presence of high peaks on the silicon surface [15]. Therefore the ability of a cleaning process to smoothen an artificially roughened surface is very important. As is shown in Fig. 2, the DDC process is very effective from this point of view. The AFEOL cleaning is able to reduce the number of high peaks as well, but this is not the case for RCA nor dRCA process.

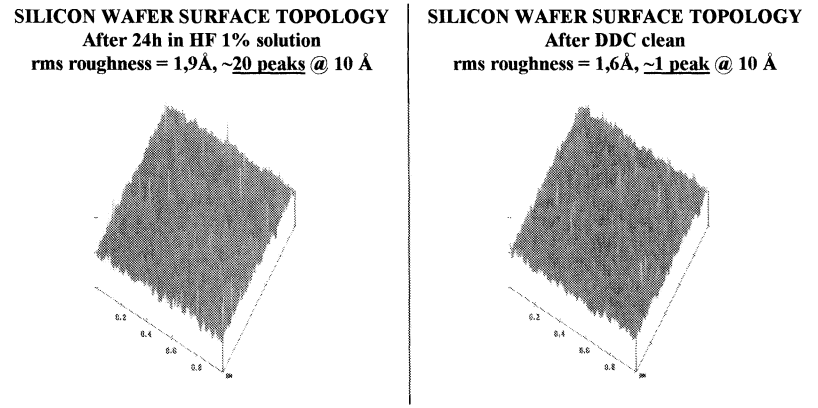

Fig. 2: *"High peak removal efficiency" of HF-Ozone based chemistry.*
Left side: artificially roughened sample with more than 20 peaks higher than 10Å on the silicon surface.
Right side: same sample after the DDC clean; just one peak higher than 10Å is remaining.

It was demonstrated earlier that strong oxidants such as Ozone or SPM drastically reduce the number of high peaks [15]. The occurrence of two active Ozone steps in DDC explains its ability to smoothen the surface and "cut" the high peaks.

Silicon and oxide consumption

For future generation devices and especially in the case of Silicon On Insulator technologies, tight control of oxide and silicon consumption (both in terms of global consumption and reproducibility) will become an important parameter.
From Table IV, there is only a slight difference between RCA and dRCA' etch rates: this is consistent with the fact that the NH_4OH/ H_2O_2 ratio is the same in the two SC1 solutions. Note that silicon consumption is ~20Å, a value which is commonly recognized as a "criteria" to obtain good particle removal efficiency [16].
During the DDC process, only ~10Å of silicon is consumed, during the two oxidation steps by ozone [15]. We demonstrated earlier that since the etching mechanism is intrinsically self-limited, the silicon consumption is practically insensitive to process parameter deviation (temperature, ozone and HF concentration, process time) and very reproducible. This is not the case in SC1 chemistry since silicon and oxide consumption are very sensitive to the NH_4OH/ H_2O_2 ratio. Therefore these cleanings are far more demanding as regards chemical concentration and temperature control systems.
Unfortunately, the two clear advantages of the DDC process mentioned above are somehow counterbalanced by a relatively high oxide consumption due to the two HF steps. Work is in progress to validate a DDC recipe using a more diluted HF-HCl solution.
Finally, the AFEOL process which includes dSC1 and HF-Ozone steps also cumulates the corresponding etch rates.

	RCA	d-RCA	DDC	AFEOL
Silicon (Å)	**20**	**21**	**12**	**25**
Silicon Oxide (Å)	**11.5**	**10**	**74**	**51**

Table IV: Silicon and oxide consumption of the global processes.

Electrical tests

At LETI site for more than 3 years, split lots are run in order to compare the final electrical performances of 70A gate oxide structures. The oxide is grown using dry or wet oxidation process on either DDC- cleaned or RCA- cleaned wafers. For this study, the AFEOL and d-RCA processes have been included into the loop.
- The cumulative results of Charge to Breakdown measurements are shown in Fig. 3.

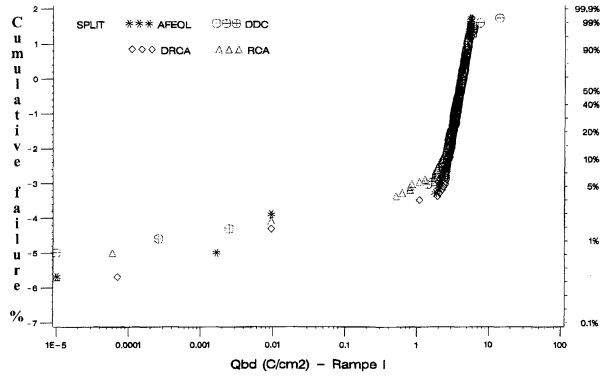

Fig. 3: *QBD distribution of 70Å gate oxide structures. (capacitor area = 0,07mm^2; 74 dies/ wafer; 4 wafers/ split lot).*

The QBD distributions plots are very similar and there is no significant variation between the different splits (neither in the intrinsic breakdown part, nor in the extrinsic tail of the distribution). Note that electrical tests give sharp Weibull diagrams, indicating a very good uniformity of the gate fabrication process. Therefore, a direct comparison between the mean value of the distribution is meaningful.

- Mean QBD values are represented in Fig. 4, the left side of the graph corresponding to the Weibull distribution shown above.

From this graph, it seems that Gate Oxide Integrity is slightly lower when the conventional RCA process is used. This trend was confirmed on several batches, on capacitors of various sizes.

The good positioning of the DDC process was already demonstrated [15], and is due to the high quality of the chemical oxide layer grown in acidified ozonated DI water [17,18]. The AFEOL cleaning process ends with the same HF-Ozone sequence: the final chemical oxide being the same, the electrical performances are also very good. As regards the dilute RCA process, we have yet no clear understanding of why it performs better than the RCA clean.

On the right side of Fig. 4, we present mean QBD values measured on wafers which were first metal-contaminated, and then cleaned (with the four different sequences), oxidized and patterned.

As is shown, QBD are not much affected by the initial contamination, so the robustness of all four cleaning processes is clearly established. However, the relative positioning of the different recipes is rather "surprising". At this point, much more data are needed to statistically confirm the result. Work is in progress and new results will be presented during the conference.

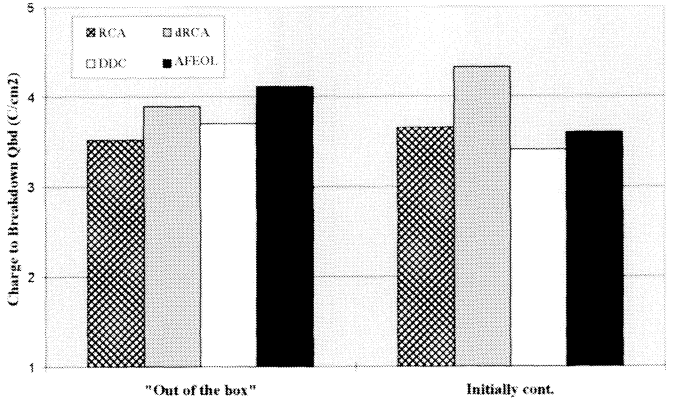

Fig. 4: *Comparison of Charge to Breakdown mean values on 70A gate oxide structures. (capacitor area = 0,07mm^2; 74 dies/ wafer)*
"Out of the box" stands for prime wafers which are cleaned and oxidize (4w/ split)
"Initially cont." concerns wafers which are first metal contaminated, then cleaned and oxidized (2w/ split).

CONCLUSION

Performances of the three alternative cleaning processes detailed in Table I have been measured and compared to the standard RCA clean.
On full sheet wafers, the Particle Removal Efficiency, the Metal Removal Efficiency and the "surface characteristics" we obtained with these advanced processes are at least as good as with the RCA process (more often better). Their robustness has been demonstrated on patterned wafers by testing 70Å gate oxide structures from several batches.
The new AFEOL sequence cumulates the reliability of the SC1 chemistry to remove the particles (actually an optimized dilute SC1) and the reliability of the ozone chemistry to insure a perfect passivation of the final silicon surface. Since the metallic contamination is also well-controlled, this process may represent a soft and reliable transition towards more advanced cleaning strategies (DDC process, IMEC-clean, ..).
The electrical results confirm that the dRCA, the DDC or the AFEOL cleaning processes can be used as cost effective replacement for the conventional RCA clean, with the advantage of a much lower chemical consumption, lower footprint and higher throughput.

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THE EFFECT OF COPPER CONTAMINATION FROM HF AND APM ON THE INTEGRITY OF 3 NM GATE OXIDES

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When copper contamination from a contaminated ammonium hydroxide peroxide mixture (APM) cleaning solution occurs, deposition of more than 7 x 10^{10} atoms/cm^2 is required before the gate oxide integrity is affected. Copper precipitation at the Si-SiO_2 interface when cooling silicon from the oxidation temperature to room temperature is responsible for the reduced yield for this contamination condition. Copper deposition from contaminated hydrofluoric acid (HF) solutions results in oxide lifetime degradation for 3 nm oxides even when less than 1 x 10^{10} atoms/cm^2 is deposited. Roughening of the silicon surface during the deposition is responsible for the deterioration of oxide quality, leading to reduced time to breakdown. Thus, removal of the copper after the contamination has occurred does not lead to a recovery of the oxide quality. Copper contamination already present on a silicon surface and then immersed in uncontaminated HF can have the same effect on oxide lifetime.

INTRODUCTION

The use of copper as interconnect material has led to a renewed interest in the effect of incidental copper contamination on device yield. Particularly the effect on gate oxide integrity (GOI) is of concern. When copper contamination of a silicon wafer occurs in a contaminated cleaning solution of ammonium hydroxide peroxide mixture (APM or SC1 clean), the copper is incorporated into or adsorbs onto the chemical oxide grown during the cleaning step. Copper present on a silicon surface readily diffuses into the silicon bulk during subsequent heat treatment [1]. It can cause gate oxide defects by precipitating at the Si/SiO_2 interface upon cooling. There is general agreement that copper deposition from hydrofluoric acid (HF) onto silicon occurs via an electrochemical redox reaction [2]. Copper ions are reduced to copper metal (Equation 1). However, there is another cathodic reaction. Hydrogen evolution (Equation 2) is catalyzed by the presence of copper on the silicon surface and dominates the cathodic current response (that is, the rate of reaction 1 is much greater than the rate of reaction 2) [3,4]. Silicon dissolution is the anodic reaction (Equation 3).

Cathodic reactions:

$$Cu^{2+} + 2e^- \rightarrow Cu \quad [1]$$

$$Cu + 2H^+ + 2e^- \rightarrow Cu + H_2 \quad [2]$$

Anodic reaction:

$$Si + 6HF \rightarrow H_2SiF_6 + 2H^+ + H_2 + 2e^- \quad [3]$$

Because the hydrogen evolution reaction occurs at copper contaminated sites, it can occur even when the HF itself is not contaminated (note: it can also occur on silicon but is quite slow). The only requirement is that copper be present on the silicon wafer with electrical contact between the two materials.

The situation of a silicon wafer in copper contaminated HF is best described using a mixed potential diagram (Fig. 1). Such a diagram is commonly called an Evans diagram. In accordance with the Tafel equation, polarization lines are linear when the current density is plotted on a logarithmic scale. Copper contamination allows a significant amount of hydrogen evolution to occur, and therefore causes a shift to larger cathodic current densities. The increased cathodic current density in turn results in an increase in the corrosion potential E_{corr}, as has been observed experimentally [5,3].

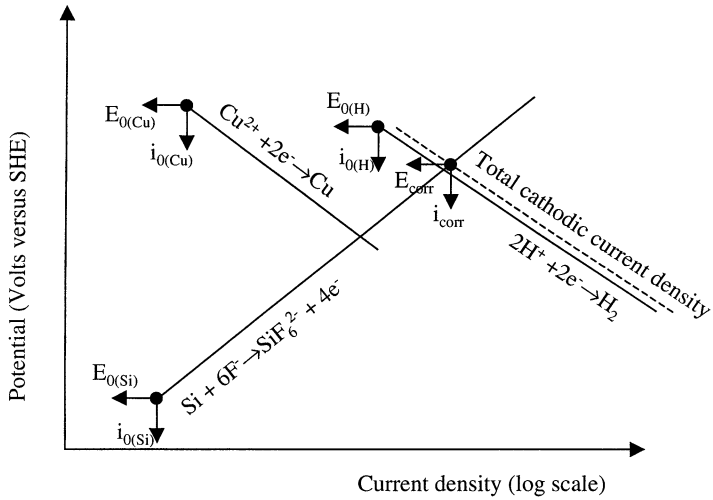

Fig. 1. Schematic mixed potential diagram for the couple of copper and silicon in dilute HF containing copper ions. The hydrogen evolution reaction on copper dominates the cathodic current.

Anodic and cathodic currents must be equal under open circuit conditions. Since small amounts of copper contamination result in relatively large cathodic currents, a substantial amount of anodic silicon dissolution occurs when silicon is contaminated with small amounts of copper. This anodic dissolution can lead to roughening of the silicon surface. When copper contamination of a silicon wafer occurs in contaminated HF, an additional gate oxide defect mechanism is possible: Surface roughening.

EXPERIMENTAL

Silicon (100) 150 mm diameter Cz grown wafers were used. All wafers were p-type (1-16 Ω-cm). Wafers received a pre-clean consisting of 10 minute immersion in a sulfuric acid peroxide mixture (SPM) at 95 °C (H_2SO_4/H_2O_2 volume ratio 4/1) followed by a HF (1%) dip for 3 minutes at room temperature. Wafers were rinsed in an overflow rinse tank for 10 minutes after each bath.

Wafers were contaminated with copper using either a copper spiked APM or HF bath. The APM solution ($NH_4OH/H_2O_2/H_2O$ volume ratio 1/1/5 at 75 °C) was contaminated with copper to a level of 10 ppb or 100 ppb. Wafers were immersed for 10 minutes. The HF solution (1%) was contaminated with copper to a level of 4 ppb or 40

ppb. Wafers were immersed for 1 minute with clean room lights on. Wafers were rinsed in an overflow rinse tank for 10 minutes after contamination.

In some cases, the copper was removed from the contaminated surface using a hydrochloric acid peroxide mixture (HPM, also called SC2). The HPM solution ($HCl/H_2O_2/H_2O$ volume ratio 1/1/5 at 75 °C) was able to remove copper contamination introduced onto the silicon surface with contaminated HF (3×10^{11} atoms/cm^2) to below the practical detection limit of Total-reflectance X-ray Fluorescence (TXRF) which, is on the order of 1×10^{10} atoms/cm^2.

To test the effect of copper contamination on silicon wafers in uncontaminated HF, wafers were contaminated with copper on the backside only. A 12.5 nm pad oxide was grown and the front side of wafers was coated with photoresist. The backside of the wafers was contaminated using copper contaminated buffered HF (BHF) to a level of 2×10^{14} atoms/cm^2. The photoresist was removed using acetone. Some wafers were then placed in an uncontaminated HF solution for 10 minutes. The copper was removed from all wafers with backside contamination using SPM. The SPM solution was, like the HPM solution, able to removed copper contamination to below the practical detection limit of TXRF. Wafers received a final HF dip (5 minutes) prior to gate oxidation.

Thin 3 nm oxide layers were grown by thermal oxidation at 800 °C in diluted oxygen (10% O_2 in N_2). Aluminum gate capacitors were formed by thermal evaporation using a shadow mask. The defect density was determined using a ramped voltage test with a threshold breakdown field of 12 MV/cm on circular capacitors with 5 mm diameter. Time dependent dielectric breakdown (TDDB) measurements were made to compare oxide lifetimes at a constant voltage of 4.2 V on circular capacitors with 1 mm diameter.

RESULTS

The defect density for samples contaminated using an APM solution is shown in Fig. 2. As copper is added, the defect density stays low until a certain copper concentration on the surface is reached, at which time the defect density increases abruptly. The copper surface concentration at which an abrupt increase in defect density occurs lies between 6.7×10^{10} and 2×10^{11} atoms/cm^2. This is close to the threshold where copper contamination starts to affect GOI for 4.5 nm oxides when the contamination is introduced after gate oxidation on the backside of the wafer (2×10^{11} atoms/cm^2) [6]. Since the thresholds for defect density is similar for the different contamination condition, the mechanism responsible for the defects is probably also the same. Copper has long been known to precipitate readily in silicon, and causes gate oxide defects by precipitating at the Si/SiO_2 interface [7]. It is probably the limit for precipitation that is responsible for the copper threshold.

Figure 3 shows that time to breakdown is not affected by copper contamination levels that are insufficient to affect the defect density. A copper precipitate near the Si/SiO_2 interface is required to cause a gate oxide defect for copper contamination from APM solutions. Therefore copper is not expected to affect gate oxide lifetime beyond the defect density which is also observed during ramped voltage stress.

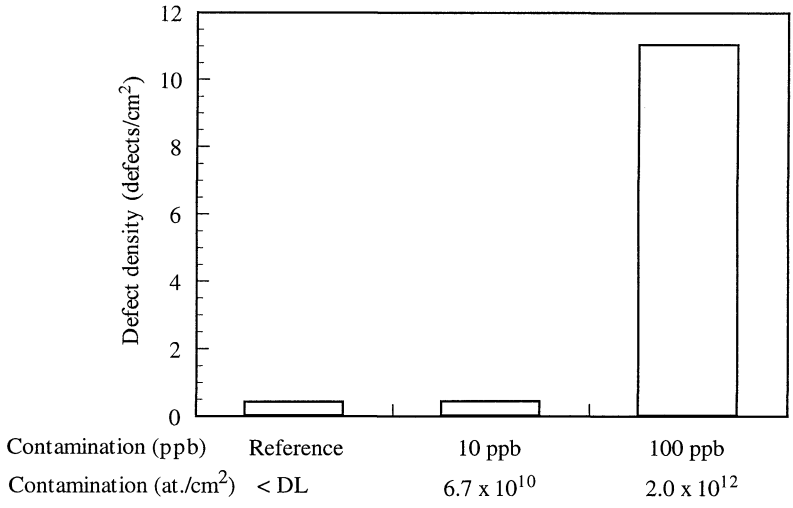

Fig. 2. Defect density of 3 nm oxides with copper contamination introduced onto the silicon surface with contaminated APM (Detection Limit = DL = 1 x 10^{10} atoms/cm^2).

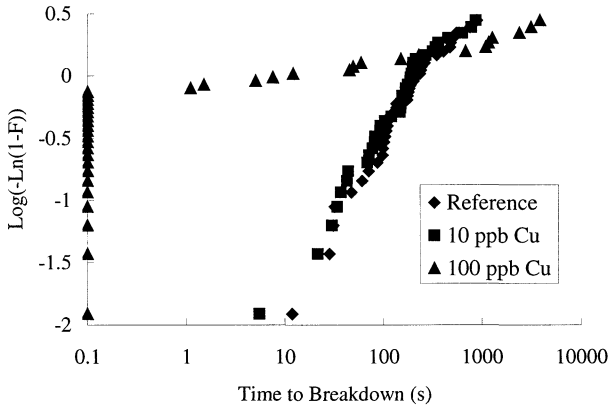

Fig. 3. TDDB of 3 nm oxides with copper contamination introduced onto the silicon surface prior to oxidation with APM contaminated with different amounts of copper. The stress voltage was 4.2 V. Capacitor area is 7.85 x 10^{-3} cm^2.

The defect density for samples contaminated with a HF solution is shown in Fig. 4. The defect density of samples cleaned after contamination is also shown. As copper is added, the defect density stays low until a certain copper concentration on the surface is reached, at which time the defect density increases abruptly. The copper surface concentration at which an abrupt increase in defect density occurs is smaller than 4.5 x

10^{10} atoms/cm^2. Removing the copper from the silicon surface after contamination from HF has occured does not allow the defect density to recover. This means that the surface has been irreversibly damaged.

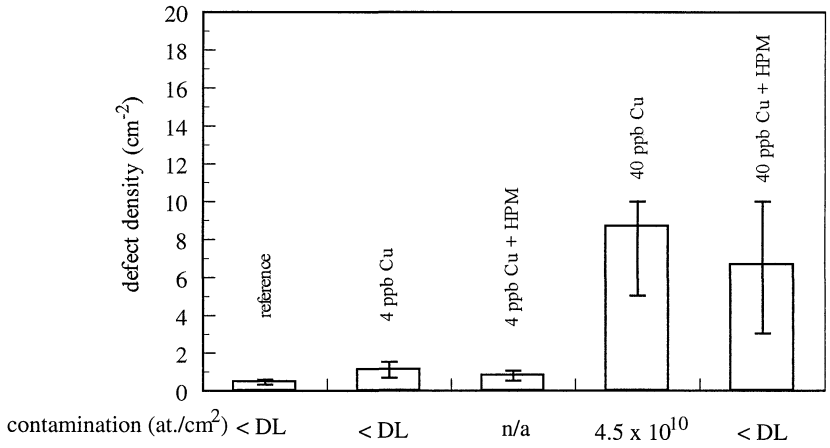

Fig. 4. Defect density of 3 nm oxides with copper contamination introduced onto the silicon surface prior to oxidation with HF contaminated with different amounts of copper. Copper was removed from some samples using HPM. The concentrations of copper just prior to oxidation as measured by TXRF are shown. The detection limit (DL) is 1 x 10^{10} atoms/cm^2.

The copper surface concentration at which an abrupt increase in defect density occurs is different for HF and APM contaminated samples. The defect mechanism must therefore be different for the two solutions. Constant voltage stress revealed that the oxide lifetime is reduced substantially when very small amounts of copper (< 1 x 10^{10} atoms/cm^2) are present on the HF contaminated samples (Fig. 5). This is not observed for the APM contaminated samples (Fig. 3). When the copper is removed using a Hydrochloric Peroxide Mixture (HPM), the oxide lifetime, like the defect density, does not recover (Fig. 6).

Atomic Force Microscopy (AFM) measurements confirm that the roughness has increased as a result of treatment in copper contaminated HF. It also shows that this damage is not removed by subsequently removing the copper (Fig. 7).

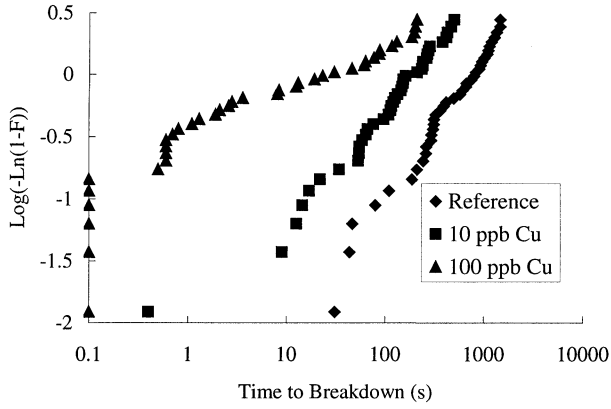

Fig. 5. TDDB of 3 nm oxides with copper contamination introduced onto the silicon surface prior to oxidation with HF contaminated with different amounts of copper. The stress voltage was 4.2 V. Capacitor area is 7.85 x 10^{-3} cm^2.

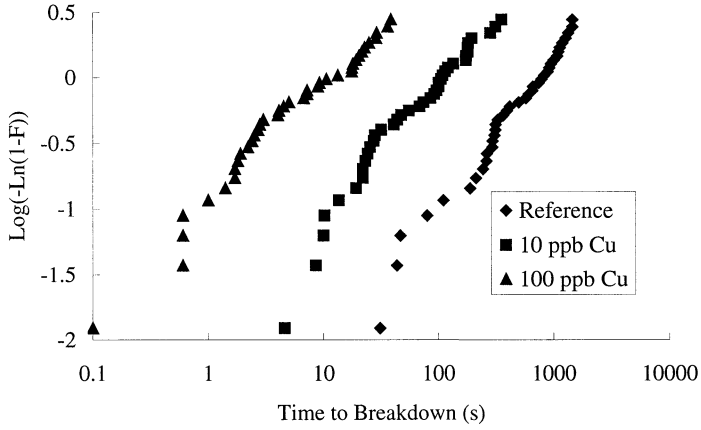

Fig. 6. TDDB of 3 nm oxides with copper contamination introduced onto the silicon surface with HF contaminated with different amounts of copper. Contamination was removed prior to oxidation using HPM. The stress voltage was 4.2 V. Capacitor area is 7.85 x 10^{-3} cm^2.

Wafers that were contaminated on the backside with copper and immersed in uncontaminated HF also have reduced oxide time to breakdown. If the contamination is removed prior to HF immersion, no such degradation is observed (Fig. 8). The copper contamination on the backside of the wafer allows significant hydrogen evolution to occur in uncontaminated HF. This polarizes the wafer sufficiently to allow anodic silicon

dissolution to occur on the front. AFM images of the front side of such samples confirm that roughening does indeed occur under these experimental conditions.

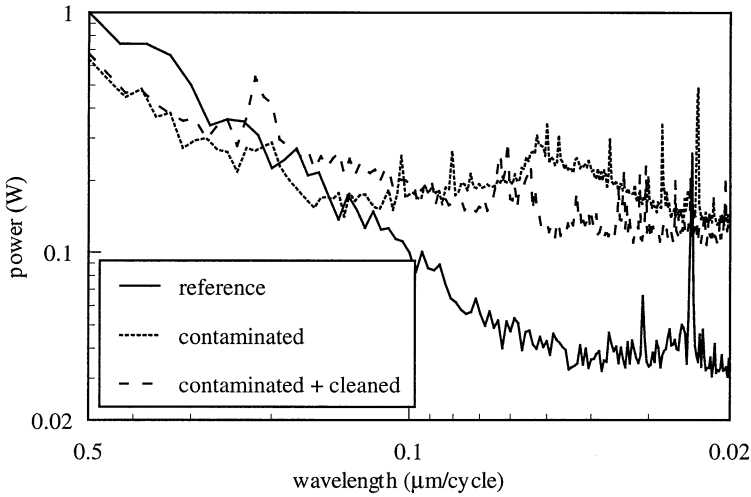

Fig. 7. Power Spectral Density of AFM images (3 µm by 3 µm scans) of a reference silicon surface, one that has been contaminated with Cu using contaminated HF and one that was cleaned after such contamination. The surface is roughened by contamination in the 0.1 – 0.02 µm/cycle range. The roughness is not removed by cleaning.

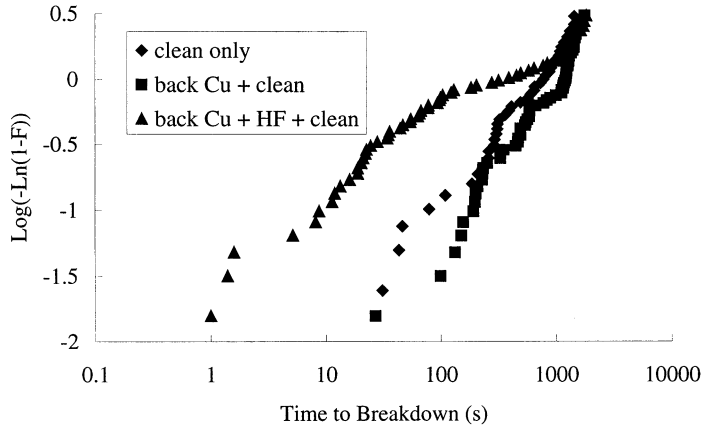

Fig. 8. TDDB of 3 nm oxides with copper contamination introduced onto the backside of the silicon for some samples. Samples that were immersed in HF with the backside copper contamination still present have reduced oxide lifetime. The stress voltage was 4.2 V. Capacitor area is 7.85 x 10^{-3} cm^2.

CONCLUSIONS

The mechanism responsible for gate oxide degradation due to copper contamination is different when the contamination occurs in HF than when it occurs by other means. Copper contamination affects gate oxide integrity by precipitating near the Si/SiO_2 interface. The threshold copper concentration at which gate oxide integrity is compromised due to copper contamination from APM (resulting in copper precipitation after oxidation), is larger than 7×10^{10} atoms/cm^2 for 3 nm oxides.

When silicon is immersed in copper contaminated HF or when copper contaminated silicon is immersed in uncontaminated HF, hydrogen evolution readily occurs. The resulting anodic silicon dissolution causes roughening of the silicon surface. AFM images confirm that such roughening does indeed occur. Less than 10^{10} atoms/cm^2 of copper contamination can cause enough roughening of the silicon surface to reduce oxide lifetime of 3 nm oxides. The damage can not be reversed by removing the copper in a subsequent cleaning step. These results imply that a robust cleaning procedure should incorporate a copper cleanup step prior to any HF step.

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PROPERTIES OF CHEMICAL OXIDES FROM PRE-GATE CLEAN PROCESSES AND THEIR ROLE IN THE ELECTRICAL THICKNESS OF THERMALLY GROWN ULTRATHIN GATE OXIDES

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ABSTRACT

Wet chemistry cleaning processes traditionally used prior to gate oxidation can result in the growth of chemical oxides of up to 1.5 nm as measured by ellipsometry. These chemical oxides have been considered to appreciably influence the subsequently prepared gate dielectric thickness. The issue is of particular concern for Sub-180 nm MOSFET design rules requiring gate oxides of less than 3.0 nm for traditional oxide-poly gate stacks, and interfacial oxides of less than 1 nm for high-K gate stacks. In this paper, the effect of various pre-gate clean strategies that generate chemical oxides of up to 1.2 nm on the electrical thickness of 2.5, 3.5 and 4.5 nm gate oxides was systematically studied. The growth kinetics of thermal oxides on wafers with different surface terminations at room and elevated temperatures was also investigated. It was found that the impact of chemical oxides on the thickness of thermally grown gate oxides > 2.5 nm is minimal. There is compelling evidence suggesting that the chemical oxide is very likely composed of aggregates of highly hydrated molecular silicic acid clusters formed in the aqueous oxidative medium, and that these silicic acid molecules are dehydrated and densified during thermal oxidation to form stoichiometric SiO_2.

INTRODUCTION

Sub-180 nm MOSFET design rules require ultrathin gate oxides of less than 3.0 nm for traditional oxide-poly gate stacks, and interfacial oxides of less than 1 nm for high-K gate stacks. These oxides represent physical thicknesses of less than 10 monolayers of SiO_2. Atomic-scale control of oxide thickness, therefore, is becoming critical to achieving designed device performance. Cleaning processes traditionally used prior to gate oxidation can result in the growth of chemical oxides of up to 1.5 nm as measured by ellipsometry. Thus the chemical oxide thickness appears to be approaching the equivalent gate oxide thickness. The presence of chemical oxides, therefore, becomes a serious concern in the control of the thickness and electrical characteristics of advanced gate dielectrics. These chemical oxides conceptually should have appreciable influence over the resulting oxide thickness following gate oxidation, but the degree of this influence as gate oxide thickness decreases is not well understood. As a consequence, HF

last processes are becoming the norm of pre-clean treatment for the preparation of advanced gate stacks, particularly as the gate dielectrics are scaled to sub-100nm technologies where high K materials are needed to achieve required equivalent oxide thickness < 2.0 nm.

Chemical oxides addressed in this study are generated by aqueous oxidative chemistries such as SPM (sulfuric acid and hydrogen peroxide mixture), APM (ammonia and hydrogen peroxide mixture), HPM (hydrochloric acid and hydrogen peroxide mixture) and DI/O_3 commonly used in semiconductor manufacturing processes. Some investigations of effects of presence or absence of chemical oxides prior to gate oxidation have been undertaken. Bayoumi et al demonstrated that the presence of chemical oxides has an negligible impact on the final gate oxide thickness, metallic contamination and various electric parameters including gate oxide reliability and basic electrical characteristics of Si-SiO2 interfaces for 3.0 nm gate oxides [1]. Depas et al showed that chemical oxides have only minor influence to the final thickness and electrical characteristics of 1.5 to 3.0 nm gate oxides grown using a cluster furnace [2]. Takano et al reported that the chemical oxides generated by SPM, APM, HPM, DIO_3 and H_2O_2 were an important factor contributing to the superior electrical quality of a 6.0 nm gate oxide [3].

In this study, effects of various pre-gate clean strategies on the electrical thickness of 2.5, 3.5, and 4.5 nm gate oxides were systematically examined, and the growth kinetics of oxides on wafer surfaces with different surface terminations at room and elevated temperatures were investigated to gain a better understanding of the impact of pre-existing chemical oxides on the thermal oxide growth.

EXPERIMENTAL

200 mm p-type silicon wafers were used for this study. Device wafers used for electrical characterization were p/p+ epi substrate.

The pre-gate clean experiments for device wafer preparation were carried out on a TEL UW8000 wet station in conjunction with other associated process tools. The pre-cleans for oxide thickness monitor wafers for part of the kinetic study were performed with an FSI Mercury Spray Acid Processor and an Excalibur HF Vapor tool.

The thickness measurements for all the chemical oxides and some of the thermally grown gate oxides were performed with a fixed angle single wavelength ellipsometer. An average thickness was obtained from multiple wafers with a 9-point data set collected for each wafer.

For electrical characterization, MOS capacitor structures ranging from 10^{-5} to 10^{-3} cm^2 were among the devices used in this study. Wafers were processed through sacrificial oxide strip prior to gate pre-clean. Subsequently, a wide range of pre-gate clean strategies, including HF-last, HF/HCl-last, SC2-last, and DI/O_3-last chemistries, was employed. These strategies resulted in different surface terminations and chemical oxides. Gate oxides were then grown and 250 nm polysilicon gate electrodes deposited. Capacitors were tested, and electrical oxide thicknesses were determined from C-V

measurements at - 3 V in accumulation mode. The electrical thickness was subjected to quantum effect corrections as appropriate.

RESULTS

Table 1 shows the electrically derived gate oxide thickness (not corrected for quantum mechanical and poly depletion effects) corresponding to pre-clean recipes employed. The oxides were prepared using a wet (steam) oxidation process at 850 °C. The chemical oxide thickness, based on ellipsometry measurements, was found to be up to 1.2 nm for wafers pre-treated by DI/O_3 last recipes, less than 0.4 nm for wafers pre-treated with HF or HF/HCl last recipes, and 0.6-1.0 nm for SC2 last recipes (**Table 2**). In general, wafers with HF-last and HF/HCl-last pre-gate cleans featured the lowest electrical gate oxide thickness, and wafers with SC2-last pre-gate cleans featured the highest electrical thickness. This trend holds for all the gate oxides targeted to 2.5 nm, 3.5 nm, and 4.5 nm, with the hydrophilic-last cleans resulting in an eventual gate oxide thickness of about 0.0 to 0.10 nm thicker than the hydrophobic-last cleans. Interestingly, a sequence of SC1 + DHF + SC2 resulted in an electrical oxide thickness very similar to HF-last, suggesting that it is the SC1 step and not the SC2 step that is primarily responsible for chemical oxide growth. In general, the thickness variation of the gate oxides is less than 0.1 nm for all the targeted thickness examined.

Table 1 Electrical thicknesses of gate oxides obtained following different pre-gate clean recipes. The thickness is directly derived from C-V measurement without correction for quantum effect

Recipe	2.5 nm	3.5 nm	4.5 nm
HF Last A	31.9	40.6	50.1
HF Last B	31.8	40.9	50.3
HF Last C	31.8	40.6	50.3
HF Last D	31.8	40.6	50.4
HF/HCl Last A	31.9	40.7	50.2
HF/HCl Last B	31.8	40.3	49.9
HF/HCl Last C	31.7	40.3	49.8
SC2 Last A	32.3	41.1	50.8
SC2 Last B	31.8	40.5	50.6
SC2 Last C	32.3	41.4	51.3
DI/O3 Last A	32.3	41.1	50.8
DI/O3 Last B	32.2	41.0	50.8
DI/O3 Last C	32.0	40.9	50.8

Figure 1 gives oxidation kinetics of oxide growth for wafers pre-cleaned by selected recipes listed in **Table 1**. The thickness used is corrected for quantum effect. It is apparent that the growth of gate oxide is almost perfectly linear with respect to the duration of oxidation, indicating that the oxidation process is controlled by direct reaction between Si and oxidizing species as predicted by the Deal-Grove model [4]. Moreover, there are two groups of distinct straight lines nearly parallel with each other within the thickness range studied. One group represents wafers processed by HF and HF/HCl last pre-clean chemistries (lower line) and another group by SC2 and DI/O_3 chemistries (upper line). The vertical spacing between the two parallel straight lines is ~ 0.04 nm, reflecting how insignificant is the contribution of pre-existing chemical oxides to the thickness of thermally grown gate oxides. The parallel nature of the straight lines also shows that the growth rate of the oxide is virtually identical for all the different pre-clean chemistries employed. The results also suggest that the chemical oxides behave very differently from the thermally grown oxide in that a layer of pre-existing chemical oxide up to 1.2 nm acts as if it did not exist in thermal oxidation.

Table 2 Chemical oxide thickness by pre-clean chemistries as measured by ellipsometry

Pre-clean Chemistries	HF Last	HF/HCl Last	SC2 Last	DIO_3 Last
Chemical Oxide Thickness (nm)	~ 0.4	~0.41	0.6-1.0	~1.2

Figure 2 shows the growth of native oxide at room temperature in a fab atmosphere. At this temperature and with ~0.2 atm O_2 being the oxidant, Si oxide growth is slow and the growth process can be effectively magnified and readily monitored. The wafers pre-cleaned by RCA chemistry had roughly 0.6 nm chemical oxide grown. The wafers pre-cleaned by RCA and followed by a HF vapor treatment had an extremely thin residual chemical oxide averaged at 0.03 nm as measured by ellipsometry. At the very beginning of the oxidation, the difference in chemical oxide thickness between the two types of wafers is ~ 0.5 nm. The oxide growth was continuously tracked hourly right after the pre-clean, and then monitored daily as oxidation slowed down. One can see that the initial slope of the thickness vs. time curve for the HF vapor pre-treated wafers is much steeper than that for wafers covered with 0.6 nm chemical oxide. This indicates that in the first hours the growth rate is faster for the HF vapor pre-treated wafers than the wafers covered with a layer of chemical oxide. As the trend continues, the difference in oxide thickness narrows and the two curves converge after about 390 hours of oxidation and oxides grow to ~0.9 nm oxide.

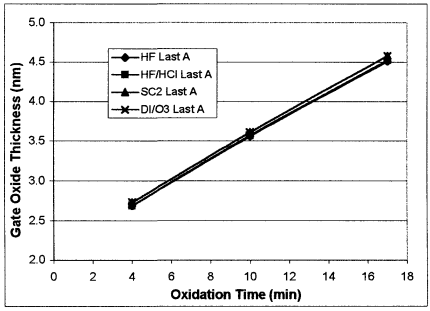

Figure 1 The kinetics of thermal oxide growth at 850 °C for wafers pre-cleaned by selected clean chemistries listed in Table 1

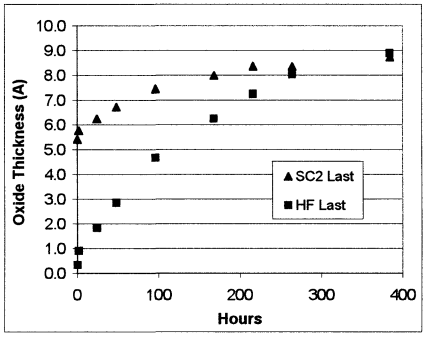

Figure 2 The impact of chemical oxide on the kinetics of oxide growth at room temperature in a fab atmosphere.

To gain compositional insight and determine the effects of a non-oxidative high temperature exposure, freshly prepared chemical oxides and native oxides grown for 240 hrs after cleaning were flash annealed to 400 °C for 30 seconds in an N_2 atmosphere. It was found that the thickness decreased for both the fresh chemical oxide and the native oxide, indicating possible compositional and structural changes, the desorption of adsorbed species, or both (**Figure 3**). The results are still consistent with those presented in **Figure 2**.

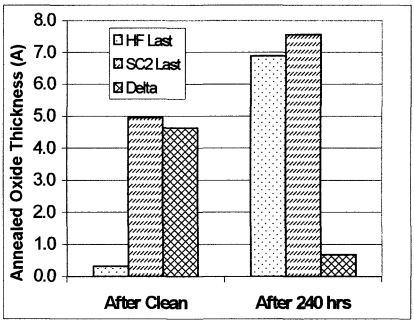

Figure 3 Oxide thickness 240 hrs after clean as compared with that right after the clean specified. Measurements were performed after a 400 °C anneal for 30" in N_2 atmosphere to desorb moisture and organics and to densify oxides

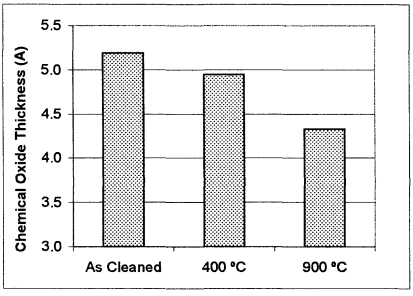

Figure 4 The change of chemical oxide thickness as measured by ellipsometry after annealing at elevated temperatures. Wafers were annealed for 60 s in N_2 for chemical oxide densification

The effect of annealing on the freshly prepared chemical oxide is illustrated in **Figure 4**. All the annealing was performed in N_2 for 60 seconds, and the oxide was annealed at 400 °C and 900 °C, the latter of which is often the temperature used for annealing thermally grown oxide to obtain a high quality gate oxide. Significant changes in ellipsometric thickness were observed as the annealing temperature was increased. The thickness of the chemical oxide decreases monotonically as the annealing temperature increases, suggesting strongly that certain compositional and structural changes may have taken place.

DISCUSSION

The composition of chemical oxides generated in wet oxidative chemistries has been studied extensively. XPS, EELS and ATRIR have been used to probe elemental composition and extract information on chemical bonding. XPS showed that Si in the chemical oxide is largely fully oxidized Si^{+4} with some partially oxidized Si^{+x}, where $x<4$. EELS and IR study showed that there are clear signatures of O-H stretching, indicating the presence of -OH groups [5, 6 and 7].

The findings of this study and others have shown that chemical oxides contribute only a very moderate increase to the thickness of subsequently grown thermal oxides. This is true regardless of the preparation conditions of both the chemical oxide and the thermal oxide. Possible explanations would be that the chemical oxide acts as a diffusion barrier, thus slowing the thermal oxidation rate, or the oxide grows faster on HF last processed wafers. However, our results indicate that the oxidation kinetics for 2.5 to 4.5 nm oxides fall in the linear regime of the Deal-Grove model for the temperatures used. Thus the process is reaction limited and the chemical oxide can't be acting as a diffusion barrier. It should be pointed out, however, that at ambient temperature the chemical oxide *does* appear to act as a diffusion barrier in the formation of native oxides and the native oxide growth seems to grow faster on the surfaces free from chemical oxides (**Figure 2**). Another possible explanation, consistent with observed results, is that the chemical oxide thickness

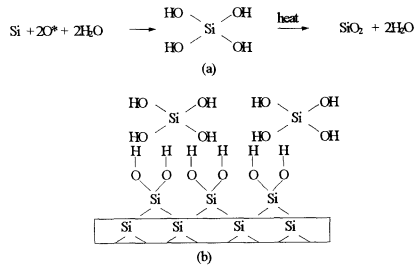

Figure 5 Suggested Model for the chemical oxide formation in an oxidative aqueous medium. (a) formation of silicic acid molecules and SiO_2 after a thermal treatment. (b) chemical oxide is a highly hydrated SiO_2, or aggregates of silicic acid clusters

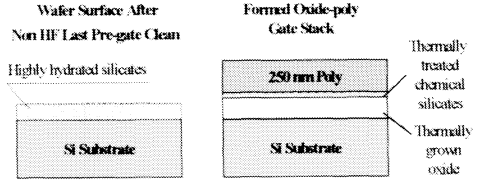

Figure 6 The role that a chemical oxide plays in a thermal grown gate oxide

suggested by ellipsometry is misleading because the compositional and optical properties of chemical oxides differ from those of thermal oxides, and that high temperatures will densify the chemical oxide (**Figure 4**). In fact, it is well known that the oxidation of a Si surface in an aqueous medium is likely to form silicic acid as described in **Figure 5** [8]. Thus it is likely that the a chemical oxide is composed largely of aggregates of molecular silicic acid clusters instead of networked SiO_2 to form a layer measured as up to 1.5 nm thick by ellipsometry. Each silicic acid molecule, upon subsequent thermal treatment, will lose two H_2O and the thickness of the chemical oxide will subsequently decrease such that it eventually accounts for only <0.1 nm of the total gate oxide (**Figure 6**). The effects of thermal treatment on chemical oxides observed here are consistent with this argument, assuming that the ellipsometric measurements are not significantly affected by compositional changes in the chemical oxide. Chemical oxides may also undergo some dehydration at room temperature, which could contribute to the apparent slow growth of native oxide observed in a fab atmosphere (**Figure 2**).

The question of whether an HF-last clean is required prior to formation of thin gate oxides or high-K gate stacks has received considerable attention in recent years. HF-last processed surfaces can present difficulties in manufacturing due to their vulnerability to contaminants such as particles and watermarks. The results of this study suggest that, at least in terms of eventual gate oxide thickness, there is no significant difference between an HF-last clean and a chemical-oxide last clean prior to gate oxidation. The results, of course, do not preclude the possibility of other differences, such as interface trap density or carrier mobility, between devices formed using different pre-gate cleans.

CONCLUSION

- The effect of chemical oxides as thick as 1.2 nm on the electrical thickness of thermally grown gate oxides > 2.5 nm is minimal. The contribution of chemical

oxides generated in a wide range of pre-gate clean chemistries is generally < 0.05 nm irrespective of the targeted gate oxide thickness.

- At temperatures (e.g., the room temperature) that are significantly lower than the gate oxidation temperature, the oxide seems to grow faster on the HF last processed wafer surfaces than those covered by a layer of chemical oxide in the very early stage of the oxidation. The oxide growth slows down and the thickness for wafers of both terminations converges and becomes comparable when the oxide reaches ~0.9 nm.
- The chemical oxide are very likely composed of aggregates of highly hydrated silicic acid molecular clusters formed in an aqueous oxidative medium, and that these silicic acid molecules are dehydrated, densified and physically shrunk during thermal oxidation to form stoichiometric SiO_2.
- The contribution of chemical oxide generated in oxidative pre-gate clean chemistries to the thickness of gate oxides < 2.0 nm may not be as significant as conceived. For the high K gate dielectric stacks, the current practice of HF last pre-gate clean processing for the preparation of advanced gate stacks to achieve an equivalent oxide thickness < 1.5 nm may not be necessary from the dielectric thickness consideration.

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WET PREPARATION OF ATOMIC-SCALE DEFECT-FREE HYDROGEN-TERMINATED SI WAFER SURFACE

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ABSTRACT

We tried to develop a new wet preparation method for an atomically defect-free Si wafer surface. In conventional atomically smooth treatment using NH_4F aqueous solution, dissolved oxygen was revealed to form defects on the Si (111) surface. We achieved the formation of an extremely atomically smooth hydrogen-terminated surface with good periodic step/terrace structure. Moreover, the ordered surface structure was confirmed to be fabricated all over the wafer surface. It was found that the terrace width could be controlled by setting a suitable off-angle in the wafer-polishing process. The atomic–scale defect-free hydrogen-terminated wafer surface with periodic step/terrace structure is greatly expected to be useful as a well-defined substrate for nanostructure fabrication and high-quality film deposition and to be useful in many other research fields.

INTRODUCTION

Throughout the past decade, Takahagi [1] and Chabal [2] first reported the hydrogen-termination of the HF-etched Si surface, and furthermore Takahagi [1, 3] discovered hydrogen-passivation phenomenon. These research results now have become an essential concept for the development of a new preparation technique in Si device production processes. Moreover, Higashi developed a novel preparation technique to obtain an atomically smooth Si (111) surface with mono-hydride-termination by treatment in a buffered HF or NH_4F aqueous solution [4,5].

Scanning Tunneling Microscopy (STM) atomic images of the surface prepared by NH_4F treatment show unfortunately many defects, such as etch-pits on a terrace and kinks in a step-edge [6, 7]. Until now, we have found hardly any research work that has achieved preparation of a defect-free hydrogen-terminated Si surface. The development of a new preparation method of a defect-free Si surface is greatly expected. In this work, we tried to develop a new wet process for preparation of an atomic-scale defect-free Si surface in a wafer size. The Si wafer surface, which will have an ordered terrace and step surface structure, may be a useful substrate for nanofabrication and many other processes [8, 9].

EXPERIMENT

We used a n-type Si (111) wafer specially polished for the present work. The samples were cut with various miscut angles off the (111) plane in two types crystallographic directions, <11-2> and <-1-12>. Organic contamination was removed by treatment in boiling H_2SO_4:H_2O_2 = 3 : 1 solution after washing in acetone. The native oxide layer on the Si surface was removed by immersion in a 5% HF solution after removal of organic contamination. Finally, the Si wafer was immersed in a 40% NH_4F solution.

In this study, both the complete removal and the prevention of re-absorption of organic contamination on the Si surface during the wet treatment were very important. This is because residual organic contamination acts as a etching-mask, brings inhomogeneous etchings, and finally makes irregular morphology on a wafer surface. Then we used ultra-pure water with total organic carbon (TOC) less than 4ppb, and vessels and tweezers were used immediately after being cleaned in a boiling sodium peroxodisulfate aqueous solution also followed by rinsing with ultra-pure water. Boiling sodium peroxodisulfate aqueous solution is a strong oxidant and decomposes the organic contamination on the surface of the vessels and so on, into carbon dioxide and water. The surface morphology was observed by ultra-high vacuum scanning tunneling microscopy (UHV-STM) and atmosphere atomic force microscopy (AFM), and a chemical structure of the surface was also measured using polarized Fourier transfer infrared spectroscopy (FT-IR) in attenuated total reflection mode (ATR). A surface elemental composition was monitored using X-ray photoelectron spectroscopy (XPS).

RESULTS AND DISCUSSION

Development of a New Wet Treatment Using NH_4F

Figure 1 shows the STM images of the Si (111) surfaces prepared by NH_4F treatment. The Si surfaces cut 1° off in the <11-2> direction have an atomically smooth surface. Treatment times, which were optimized at the solution temperature of 20 °C and 72 °C,

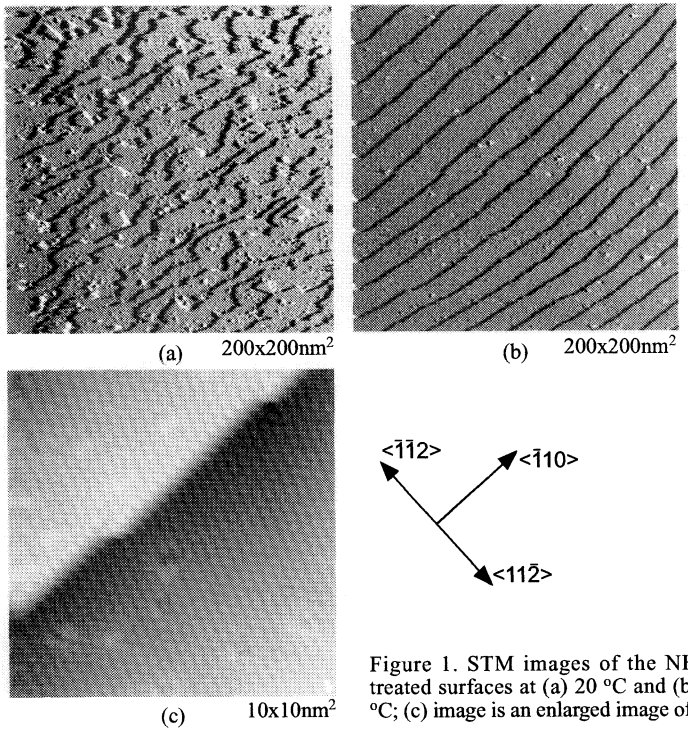

Figure 1. STM images of the NH_4F-treated surfaces at (a) 20 °C and (b) 72 °C; (c) image is an enlarged image of (b).

were 6 min and 30 sec, respectively. The surface prepared using the conventional treatment in NH_4F at 20 °C showed step/terrace atomic scale smoothness, but also many atomic-scale irregular structures, such as etch-pits and kinks. The existence of many kinks on step-edges results in non-linear step-edges. FT-IR-ATR measurement of the surface suggested that the surface was almost terminated by a mono-hydride structure, the same as the result of IR measurement by Higashi [4].

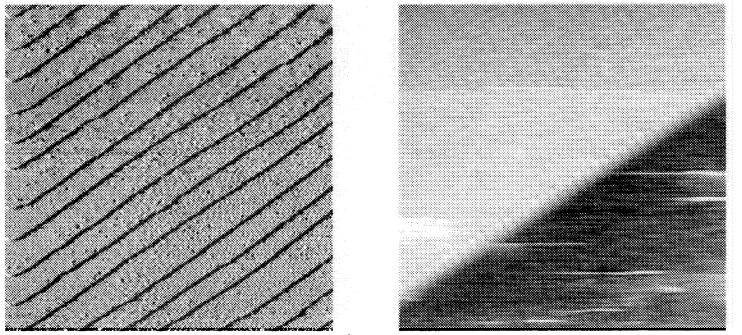

Figure 2. STM images of a wafer treated by NH_4F solution with DOC of 0.1 ppm prepared by N_2 bubbling at 20 °C.

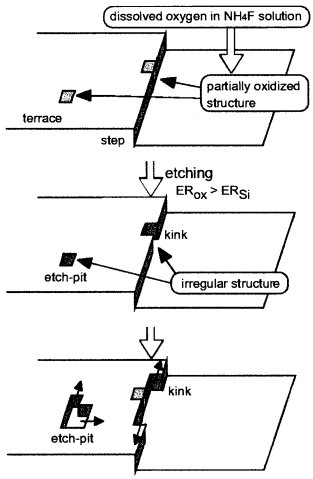

Figure 3. Schematic model of the partial oxidation on an Si surface by oxygen in NH_4F solution.

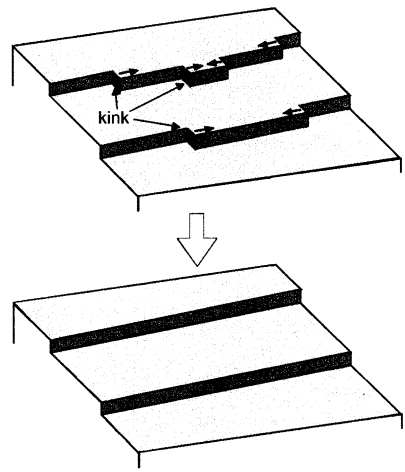

Figure 4. Schematic model of the generation mechanism of new defects on the Si surface by NH_4F etching of oxidized parts.

On the other hand, the surface treated at 72 °C had extremely little crystallographic defects such as etch-pits or kinks and also had straight step-edge lines and a homogeneous periodic step/terrace structure. All steps were observed to have a bilayer step structure with a height of 0.31 nm. The surfaces were also confirmed, by FT-IR-ATR and XPS measurements, to be terminated by a mono-hydride structure and to be free of organic contamination. Terminal-hydrogen atoms can be clearly seen in an enlarged STM atomic image as shown in Figure 1. Hydrogen atoms in step-edges are ordered in a straight line along the <-110> direction. We found that etching using hot NH_4F aqueous solution extremely improves the regularity of the Si (111) surface structure.

We tried to make clear a mechanism for the reduction of crystallographic defects such as kinks and etch-pits on the surface by the hot NH_4F treatment. At first, the dissolved oxygen concentration (DOC) in NH_4F solution at 72 °C was measured to be 1.8 ppm, which was lower than the 5.0 ppm concentration found at 20 °C. In order to confirm the effect of the dissolved oxygen, we tried treatment using the NH_4F solution with low DOC prepared by nitrogen gas bubbling. In spite of the treatment temperature of 20 °C, a wafer surface treated by NH_4F solution with a low DOC of 0.1 ppm had a morphology similar to that of the surface prepared by hot NH_4F treatment as shown in Figure 2. Oxygen dissolved in NH_4F solution proved to make an irregular structure on Si surfaces.

Dissolved oxygen is considered to form a partially oxidized structure as shown in Figure 3. The etching rate of the oxidized part in NH_4F solution is presumed to be higher than that of an Si metal part by etching rate measurement. A new irregular structure spreads from new etch-pits and kinks formed on traces of etched parts. Therefore, NH_4F treatment is considered to be able to remove crystallographic defects, but dissolved oxygen in the treatment solution induces new defects. The production process of surface defects by

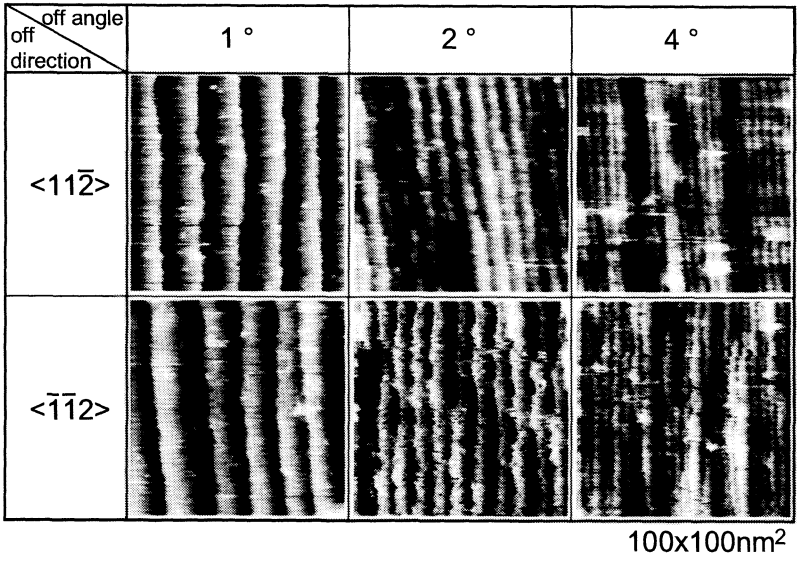

Figure 5. AFM images of the surfaces with various off-angles.

dissolved oxygen is considered to antagonize to reduction process of defects by NH_4F etching.

In the following, we discuss the mechanism of reducing kink structures. As shown in Figure 4, di-hydride structures on kink parts are considered to be selectively etched by NH_4F etchant. Then, etching proceeded along to the step-edge line direction. When the etching lines coming from both the right and left meet, the kink structure vanished and the step-edge became smooth. This kink-vanishing phenomenon is considered to occur at all regions of the Si wafer surface in the NH_4F etching process.

Wafer-Size Self-Organization of the Ordered Si Surface

We examined the surface morphology of the samples having various off-angles in both directions of <11-2> and <-1-12>. Figure 5 shows AFM images of the surfaces with various off-angles. The step lines run along the <-110> direction, and a step/terrace period is almost uniform on the whole surface. Terrace width is decreasing with the increasing of the off-angle. Figure 6 shows a relationship of a terrace width obtained from AFM images and an off-angle measured by the double crystal mode of X-ray diffraction (XRD). The solid line is the terrace width calculated from the off-angle assuming uniform step/terrace and bilayer step surface structure. The terrace width obtained from AFM images coincides well with the calculated value. It was found that the step/terrace period could be controlled by polishing the wafer surface in a suitable off-angle condition.

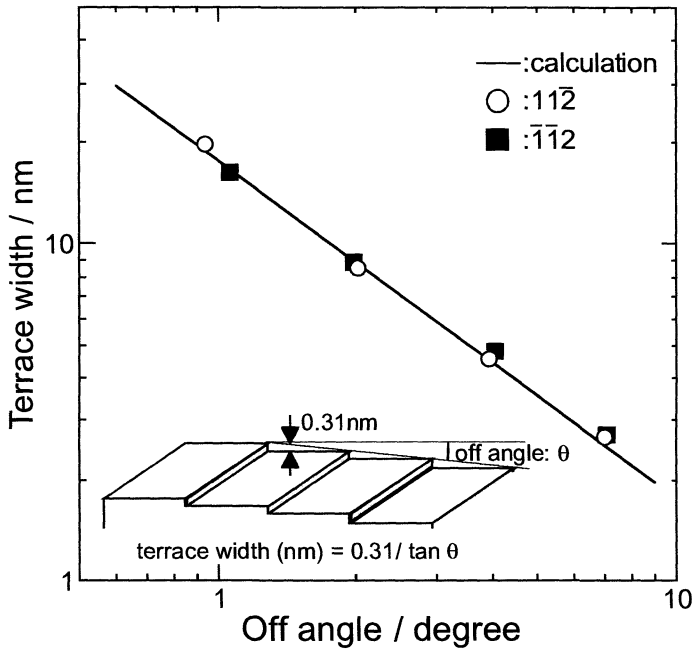

Figure 6. Relationship of an average terrace width in AFM images and the off-angle measured by XRD.

We tried to form the periodic step/terrace structure in a wafer size. Figure 7 shows the AFM images observed at 9 points on the surface of a 4-in wafer with an off-angle of 1° in <11-2> direction treated by hot NH_4F solution. The same regular morphologies are observed at all points. In Figure 8, a similar result was confirmed on the wafer miscut to <-1-12> direction. It was confirmed that the periodical structure in a wafer size could be formed by wet process. An extremely large number of step lines (5×10^6) at regular intervals of about 20 nm exist on the Si wafer surface. We think that the wafer specially polished for the present work has a uniform miscut angle on the whole surface.

In the AFM observation, the completed periodic step/terrace Si surface structure appeared to be in a steady state; also, the etching process completely stopped. Why are the extremely ordered surface structures self-organized on a whole wafer surface? Generally, entropy contained in a system decreases in a self-organization process. Therefore, in order to decrease free energy, enthalpy of the system must decrease. In a typical self-organization process such as crystal growth, the formation of attractive interaction of atoms or molecules achieves a decrease in internal enthalpy of the system. But in the present case, we find no interaction bringing self-organization on an Si surface. We presume that etchant migration on the terrace plays an important role, but the detailed mechanism has not been clarified until now.

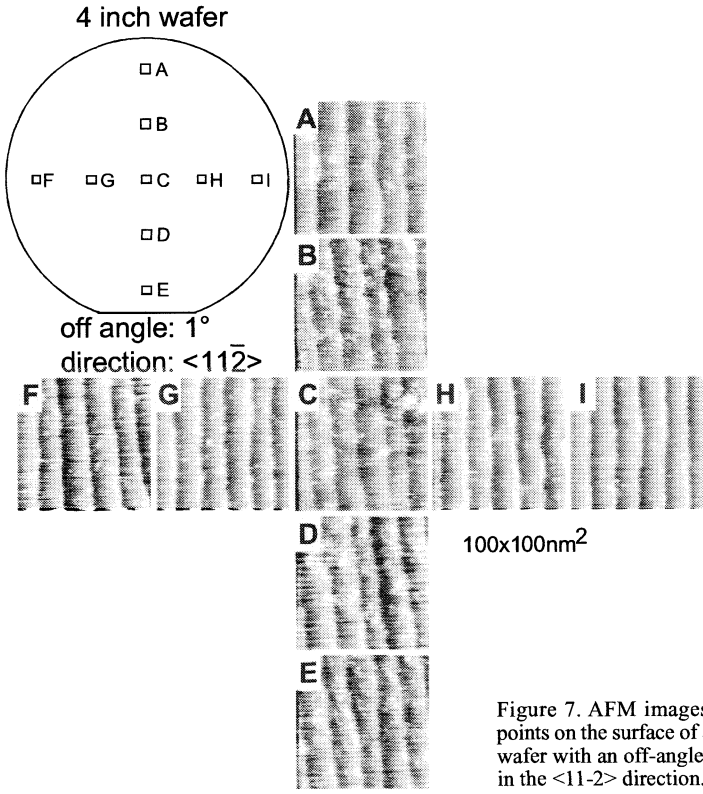

Figure 7. AFM images at 9 points on the surface of a 4-in wafer with an off-angle of 1° in the <11-2> direction.

We succeeded in developing a wafer-size wet treatment technique for preparation of a periodic clean Si (111) surface with a very small amount of atomic-scale defect. The wafer is greatly expected to be useful as a well-defined substrate for nanostructure fabrication, high-quality film deposition, and many other research fields. The hydrogen-terminated surface will be used as a hydrophobic substrate. In addition, after oxidation the hydrogen termination surface also changes to an oxide surface, but the periodic atomically smooth surface was confirmed to be retained. Then we will use the wafer as a hydrophilic atomically smooth substrate with periodic morphology.

Chemical Structure on the Smoothed Si Surface

Chemical structures of the surfaces miscut in <11-2> and <-1-12> directions were analyzed using polarized FT-IR-ATR. In order to enhance the IR spectra signal of the step-edge's structure, a wafer with an off-angle of 4° was used. Figure 9 shows STM images of the surface inclined to <11-2> and <-1-12> directions with an off-angle of 4°. The terminal hydrogen atoms can be clearly observed in both surfaces. Irregular structures such as etch-pits and kinks were hardly observed in a 10 nm square area. Hydrogen atoms in step-edges

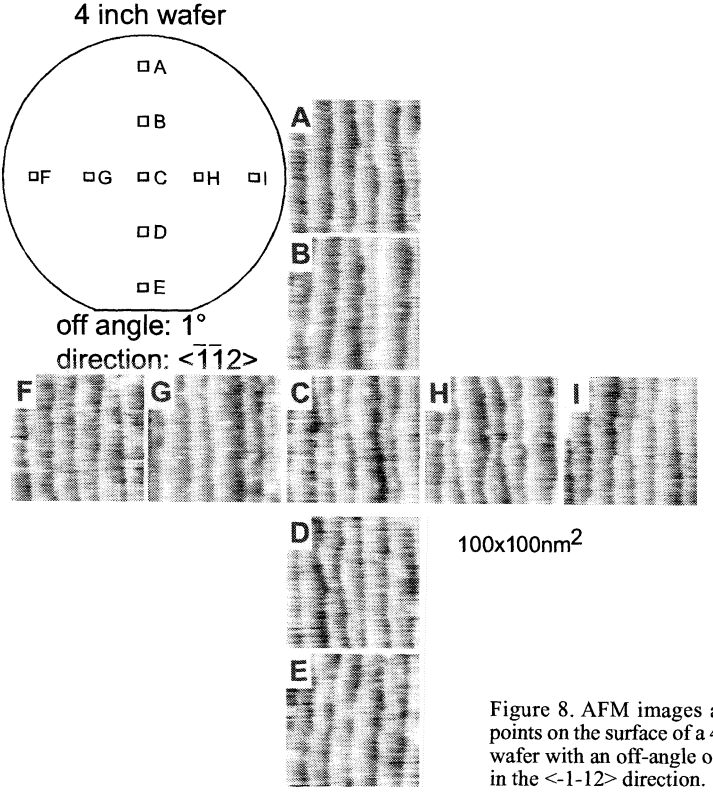

Figure 8. AFM images at 9 points on the surface of a 4-in wafer with an off-angle of 1° in the <-1-12> direction.

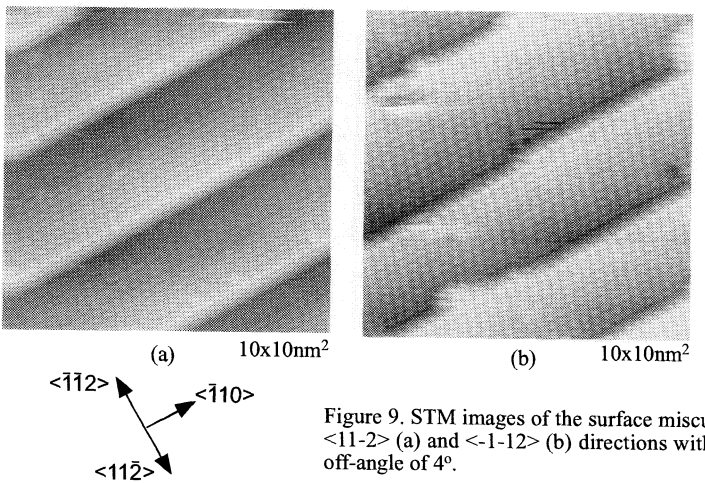

Figure 9. STM images of the surface miscut to <11-2> (a) and <-1-12> (b) directions with an off-angle of 4°.

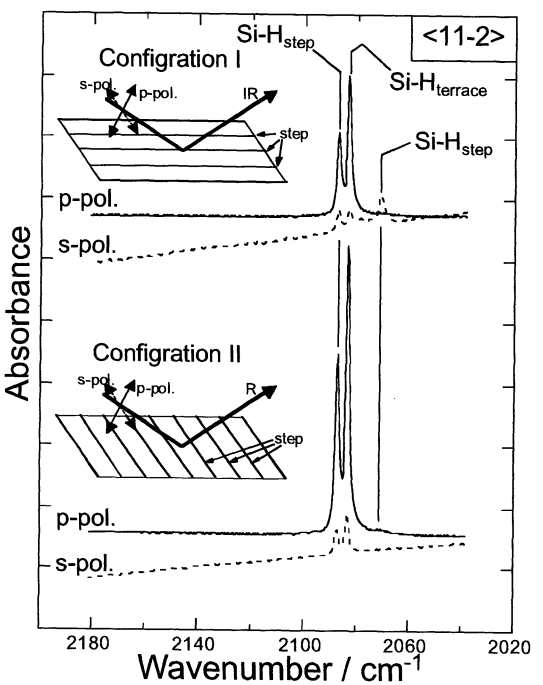

Figure 10. FT-IR-ATR spectra of the hydrogen-terminated Si (111) surfaces miscut to <11-2> directions with an off-angle of 4°.

are ordered in a straight line along the <-110> direction. The crystallographic consideration suggests that when the step-edge is run along the <-110> direction, the chemical structures of the step-edge on the inclined Si (111) surfaces to the <11-2> and <-1-12> directions are mono-hydride and di-hydride, respectively.

Figure 10 and 11 show FT-IR-ATR spectra of the surfaces with an off-angle of 4°. Upper side spectra were observed when IR incidence was parallel to step-edge, and lower side spectra were observed when IR incidence was normal to step-edge. These IR measurement setups are called configuration I and configuration II, respectively. Solid lines were p-polarized spectra, and dotted lines were s-polarized spectra. In case of the surface miscut to the <11-2> direction, p-polarized spectra measured in both configurations are of similar shape, and had two peaks, at around 2084 and 2087 cm^{-1}. These peaks were assigned to Si-H structure on the terrace and on the step-edge, respectively. In s-polarized spectra, a peak around 2070 cm^{-1} was not observed at configuration II. This result suggests no bond has a parallel component to a step-edge.

In case of the surface inclined to the <-1-12> direction, peaks of Si-H on the step-edge at 2087 and 2070 cm^{-1} were not observed, and three new peaks at 2094, 2100 and 2134 cm^{-1} were observed. These three peaks were assigned to Si-H_2 structure on the step-edge. These

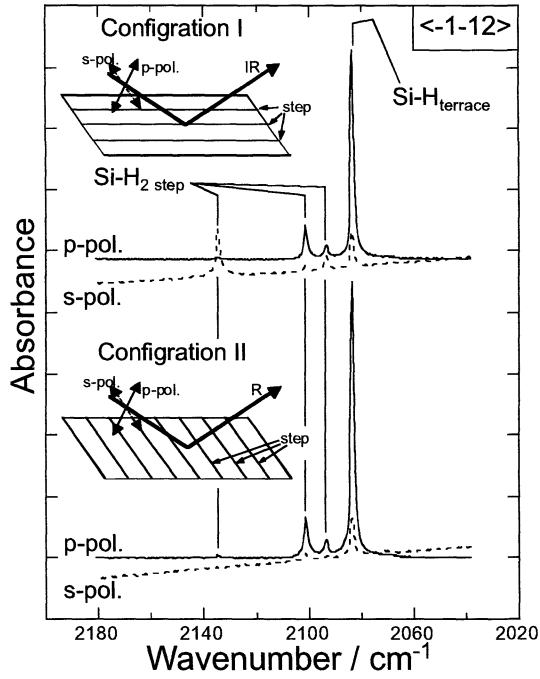

Figure 11. FT-IR-ATR spectra of the hydrogen-terminated Si (111) surfaces miscut to <-1-12> directions with an off-angle of 4°.

peaks were hardly observed in s-polarized spectra of configuration II. This result means that an Si-H bond in the step-edge has no parallel component. Therefore, the structure of the step-edge on the Si (111) surface miscut to the <-1-12> direction is the vertical type di-hydride structure.

CONCLUSIONS

We succeeded in preparing an atomic-scale defect-free hydrogen-terminated Si (111) surface with a periodic step/terrace structure using a newly developed, organic-contamination-free treatment procedure on a laboratory scale. In the preparation, we used an NH_4F aqueous solution with a low DOC such as a hot NH_4F solution. It was revealed that the dissolved oxygen forms a partially oxidized structure on the Si surface, and that new defects arise from the oxidized part. It was also found that the Si (111) surface was self-organized to the step/terrace structure, the period of which was fixed by polishing the wafer at a suitable off-angle. The ordered structure was confirmed to be fabricated in a wafer size.

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Attaining Clean Silicon Surfaces through Protective Oxidation and Hydrogen Termination

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Pretreatment before epitaxial furnace insertion was successfully performed for protective oxidation by ozonized ultra pure water and hydrogen termination by diluted HF. Pretreatment included heat treatment in hydrogen. These two pretreatment methods were closely examined in terms of meeting quality and throughput requirements for low temperature epitaxial growth. Specific quality measures included evaluation of surface cleanliness and micro-roughness after pretreatment. For both processes, a clean and smooth surface was obtained by removing the protective oxide in heat treatment at 950℃ in hydrogen. Pretreatment time varied for both processes, 5 min for protective oxidation and approximately 1 min for hydrogen termination. This time was derived for actual conditions including epitaxial growth itself, thereby simulating the actual production environment.

INTRODUCTION

The formation of thin protective oxide films proves to be an effective approach for preventing scratches and chemical absorption of contaminants on clean silicon surfaces during handling. For very controlled environments, hydrogen termination through diluted HF treatment can be performed in the last cleaning step, provided careful handling maintains a clean surface until insertion into the epitaxial growth furnace.

Though surface cleaning[1,2] using ozonized ultra pure water has been examined in recent years, the formation of thin protective films[3] by ozonized ultra pure water, its subsequent removal, and the effects on epitaxial growth, are rarely reported.

We have demonstrated that this pre-epitaxial cleaning method suitably prepares wafers for epitaxial furnace insertion, through evaluation of oxygen and carbon on the silicon surface by small angle incident X-ray photoelectron spectroscopy (SAI-XPS)[4]. Evaluations were made at each step of cleaning by ozonized ultra pure water. We have also presented the results of stable protective oxide formation by ozonized ultra pure water[5].

This experiment examines the feasibility of both protective oxide formation and hydrogen termination to obtain clean silicon surfaces by hydrogen heat treatment as a suitable means of pretreatment for relatively low-temperature epitaxial growth.

EXPERIMENTAL

The hybrid system used for evaluations in this experiment is constructed by an X-ray photoelectron spectroscopy (XPS) system and chemical vapor deposition (CVD) system

as shown in Fig. 1. This construction allows repeated measurements without exposing the wafer to air. The XPS system (JEOL Ltd.) is equipped with a 10kV, 30mA, monochromated Alk α (1486.6eV) X-ray source. The X-ray incident angle was 5° relative to the silicon surface, and the takeoff angle was 85° . The CVD system (Eiko Co. Ltd.) was used to heat the wafer underside by induced infrared rays of a halogen lamp through a quartz rod. Wafer temperature was measured by an infrared thermometer. The silicon wafers used were 20 mm diameter, (100) orientation, boron doped on the range of 6×10^{17} atoms/cm^3.

Fig. 2 shows the experimental procedure. For both protective oxidation and hydrogen termination, the first step consisted of wafer cleaning by using 6 ppm ozonized ultrapure water(UPW), evaluation of organic contamination, and soaking in 0.5% diluted HF(DHF) to remove the natural oxide. The above cleaning was repeated twice. A protective oxide 0.7-0.8 nm thick was then formed by dipping in 6 ppm ozonized ultra pure water for 5 min. For one set of wafers, hydrogen termination was used to remove the protective oxide by dipping in 0.5 % diluted HF for 1 min. (Fig. 2b). For both sets of wafers, the oxygen and carbon concentration on the wafer surface were measured immediately with the XPS. The wafer was then transferred to the CVD chamber. The wafers were then heat treated 0 to 15 min at a pressure of 300, 600 or 760 torr, at 900 to 950℃, supplying 1 slm purified hydrogen gas. The wafers were again transferred to XPS for immediate measurement of oxygen and carbon on the wafer surface. The surface micro-roughness was measured by atomic force microscopy (AFM), (Nanoscope, Digital Instruments mnfr.), both before and after the heat treatment in hydrogen.

A series of runs consisting of pretreatment followed by epitaxial growth at 950℃ was performed. The source gas for silicon epitaxial growth was SiH_4 and the pressure was regulated to either 300 or 760 torr. The properties evaluated for the epitaxial layer include surface micro-roughness by AFM, transition width of boron by secondary ion mass spectroscopy (SIMS), (CAMACA mnfr., IMS-4f Cs^+), and crystal structure examination by transmission electron microscopy (TEM), (Hitachi mnfr., H-9000NAR).

RESULTS AND DISCUSSION

Protective Oxidation

The results of surface conditions for varying heat treatment conditions are shown in Fig. 3. The horizontal axis shows temperature of hydrogen heat treatment, and the vertical axis shows the treatment time. The graph shows the time to attaining a clean surface over the two axis parameters for 3 different pressures. A clean surface was defined as the disappearance of light elements such as oxygen or carbon as measured by XPS spectrum. We can observe that the process of protective oxidation removal is temperature dependent. At 900℃, approximately 15 min is needed to obtain a clean surface. However, at 950℃ a clean silicon surface is reached in about 3 min. The removal process of protective oxide film was analyzed using Si_{2p} and O_{1s} spectra of XPS. Fig. 4 shows the spectra after heat treatment in hydrogen at 950℃, 300 torr, for the protective oxidation process. Each spectra shows: (a) the protective oxide film immediately after formation, (b) 2 min heat treatment in hydrogen, and (c) 3 min heat treatment in hydrogen. A shifted peak of Si_{2p} due to oxidation is clearly observed at an energy range of about 103 eV for which the oxide thickness was estimated as 0.7 to 0.8 nm. A large peak of O_{1s} caused by chemical oxidation was detected. Though the shift peak of Si_{2p} disappeared at 2 min heat treatment given in Fig. 4b, a slight O_{1s} peak was

still detected. The Si_{2p} spectrum indicates that oxide film removal seems to have been achieved, but the slight O_{1s} means that oxygen atoms remained on the silicon surface. For 3 min heat treatment given in Fig. 6c, O_{1s} was not detected and a Si_{2p} peak is caused only by the existence of Si-Si bonds in bulk silicon. Over a wide scanning spectrum(0 to 1000 eV) no other elements were detected. A clean silicon surface in terms of light element (oxygen, carbon) removal is determined to have been attained when these conditions are satisfied. For heat treatment conditions of 950℃, 760 torr, the spectra behavior exhibits almost the same characteristics, for which a clean surface is determined to have been attained.

In order to prevent slip generation and metal contamination on silicon surfaces, further lowering the temperature for the entire process is desirable. However lower temperatures incur the trade-off of extended process times and poor throughput, as well as quality degradation, all of which are not acceptable in commercial applications. The temperature of 950 ℃ and time of 3 min for this experimental process satisfactorily addresses this trade-off, compared to the conventional epitaxial process which achieves a clean surface by 1 or 2 min heat treatment in hydrogen at 1100℃. Furthermore, the conditions of this experiment carry the merit of shorter heating ramp-up and ramp-down times.

Next, for this protective oxide removal scenario the surface micro-roughness was measured. Fig. 5 shows AFM images for: (a) the protective oxide film immediately after formation, (b) 2 min heat treatment in hydrogen at 950℃, 300 torr, and (c) 3 min heat treatment in hydrogen at 950℃, 300 torr. A smooth surface was observed for protective oxidation given in Fig. 5a. For the 2 min heat treatment given in Fig. 5b, a slight degree of surface roughness was observed. At this time a small O_{1s} peak was detected by XPS. This can be interpreted as the existence of a few island-like oxides on the silicon surface remaining during the last stages of protective oxide decomposition. Finally, a smooth surface was achieved at 3 min heat treatment in hydrogen given in Fig. 5c. A smooth surface was also obtained by 3 min heat treatment at 950℃, 760 torr.

One of the essential prerequisites for successful epitaxial growth at low temperatures is a smooth and clean wafer surface just before growth is begun. These experimental results show that this prerequisite was fulfilled by approximately 3 min heat treatment at 950℃.

Hydrogen Termination

The hydrogen termination process for silicon wafers was performed by the method given in Fig. 2b. The XPS spectra for silicon surface of hydrogen terminated wafers are shown in Fig. 6. A Si_{2p} shift peak and slight O_{1s} peak were observed after diluted HF treatment, shown in Fig. 6a. The silicon surface treated by diluted HF was not perfectly hydrogen terminated because oxygen remains on the surface. Therefore, we can infer that Si-O-H bonds[6] were formed on the silicon surface. No other elements were detected on XPS spectra. The time to attain a clean surface was measured in the same manner as procedure ***Protective Oxidation*** of this report. As shown in Fig. 6b, there was no temperature dependence between treatment time and clean surface realization, with a clean surface obtained by heat treatment in less than 1 min.

The surface micro-roughness as measured by the AFM was smooth, and unchanged after heat treatment. This smooth surface was achieved in 1 min, at 950℃, 760 torr.

For commercial production, the hydrogen termination process offers the advantage of shortened pre-epitaxial treatment time. However, after pretreatment the oxidation of

silicon advances as time lapses, adversely affecting the epitaxial process. Therefore, starting the epitaxial process immediately after hydrogen termination is highly desirable.

Epitaxial Layer Properties

To summarize, for protective oxidation process a clean and smooth surface was attained in around 3 min heat treatment in hydrogen at 950℃. For hydrogen termination by diluted HF, a clean surface was attained in around 1 min heat treatment. In addition to pretreatment, the feasibility of high quality epitaxial growth using these pretreated wafers was evaluated. The pretreatment time was determined by section ***Protective Oxidation*** of this report for protective oxidation and section ***Hydrogen Termination*** for hydrogen termination. A satisfactory epitaxially grown layer was achieved for a heat treatment of 5 min for protective oxidation process. The additional time over 3 min per section ***Protective oxidation*** is thought to be due to the omission of the ramp-down process. In the pretreatment experiments the wafer reached room temperature before XPS measurement, and during heating ramp-down time oxidation removal seems to have continued. For pretreatment and epitaxial growth performed consecutively there is no need for ramp-down since processing occurs at the same temperature in the same furnace, so the pretreatment time becomes longer.

The properties of the epitaxial layer grown at 950℃ are shown in Table 1. Pretreatment time by the protective oxidation process was 5 min. The transition width for a pressure of both 300 and 760 torr was a very narrow. The surface micro-roughness was less than 0.1 nm, very smooth. On the other hand, when the hydrogen terminated wafer was immediately inserted into the CVD chamber, a high quality epitaxial layer was obtained for any pretreatment time over 1 min. The epitaxial layer properties characterizes a perfect single crystal, with smooth surface and narrow transition width of boron dopant.

The protective oxidation and hydrogen termination processes developed here are suitable for relatively low temperature epitaxial growth.

SUMMARY

For pretreatment before epitaxial furnace insertion, protective oxidation by ozonized ultra pure water and hydrogen termination by diluted HF were easily performed. After this pretreatment of the silicon wafer which includes heat treatment in hydrogen, the resultant surface cleanliness and micro-roughness were evaluated. For the protective oxidation process, a clean and smooth surface was obtained by removing the protective oxide in approximately 3 min heat treatment at 950℃ in hydrogen. For the hydrogen termination process, a clean and smooth surface was obtained in less than 1 min of heat treatment.

For the protective oxidation process, a high quality epitaxial layer was grown for a heat treatment over 5 min, at 950℃ using SiH_4 gas. For hydrogen termination, a high quality epitaxial layer was grown for a heat treatment less than 1 min.

Both processes enabled successful epitaxial growth at 950℃, offering two pretreatment methods suitable for high quality epitaxial layers.

ACKNOWLEDGMENTS

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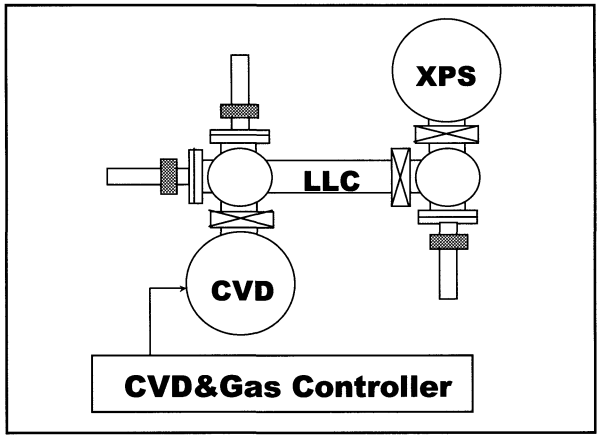
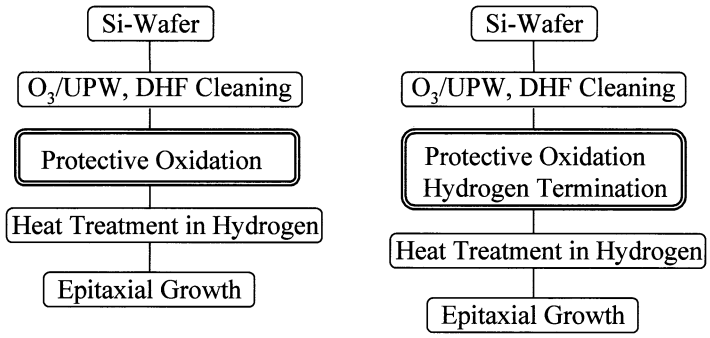


Fig.1 Experimental equipment for epitaxial process development



(a) Protective oxidation process (b) Hydrogen termination process

Fig.2 Experimental procedure

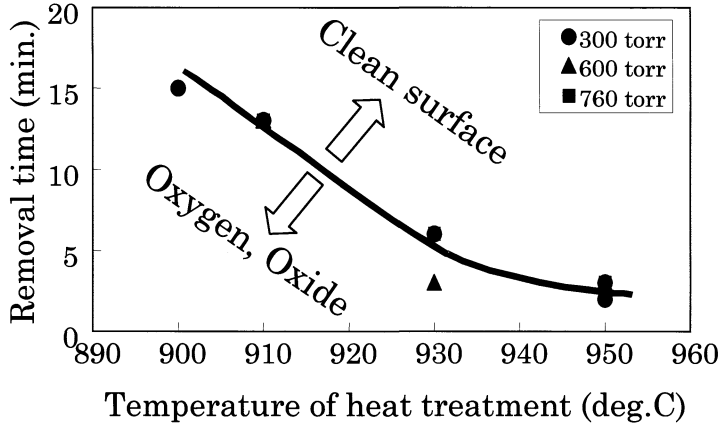
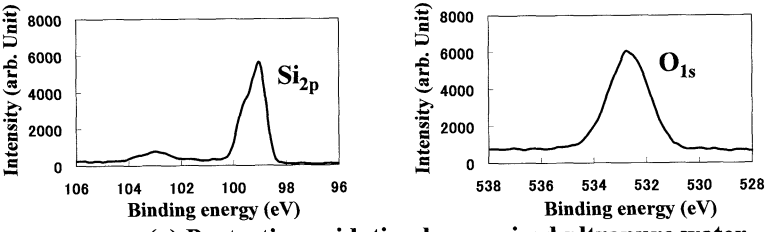
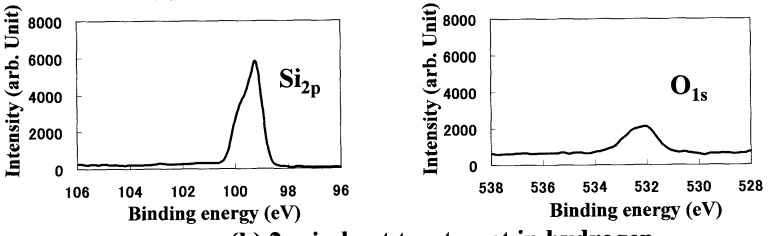


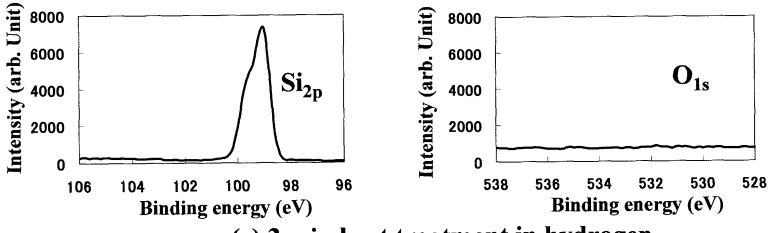
Fig.3 Surface condition after heat treatment in hydrogen



(a) Protective oxidation by ozonized ultrapure water

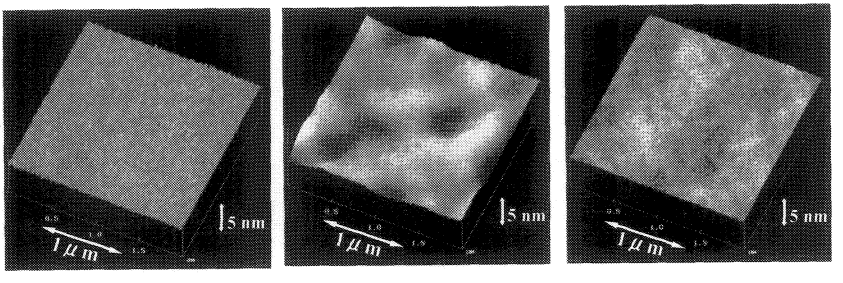


(b) 2 min heat treatment in hydrogen



(c) 3 min heat treatment in hydrogen

Fig.4 XPS-spectra of protective oxidation process (950℃, 300torr)

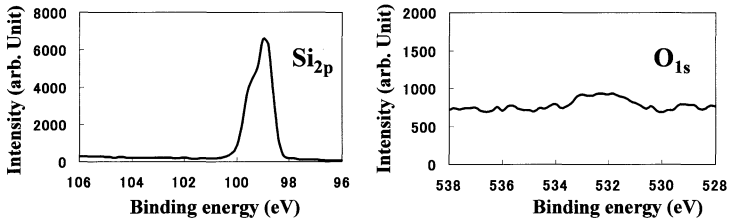


(a) Protective oxidation by ozonized ultra pure water

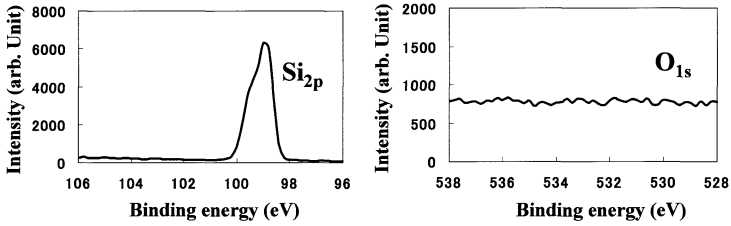
(b) 2 min heat treatment in hydrogen

(c) 3 min heat treatment in hydrogen

Fig.5 AFM images of protective oxidation process (950℃, 300torr)



(a) Hydrogen termination by ozonized ultrapure water



(b) 1 min heat treatment in hydrogen

Fig.6 XPS-spectra of the hydrogen termination process (950℃, 300torr)

Table1 Epitaxial layer properties

Pre-treatment	Epitaxial growth	RMS (nm)	T.W. (μ m)
Protective Oxidation	950℃, 300torr	≦0.1	~0.2
	950℃, 760torr	≦0.1	~0.2
Hydrogen Termination	950℃, 300torr	≦0.1	~0.2

CLEANING FOR DEEP-SUBMICRON STRUCTURES.

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We report methods for analyzing remaining metallic contamination and residual ions in deep-submicron-diameter holes with high aspect ratios. The method is based on conventional atomic absorption spectrometry (AAS), and uses device patterns with high density contact holes. With this method, metallic contamination on the order of 10^{10} atoms/cm^2 can be easily analyzed inside 0.1 μm-diameter holes. The residual ions in the fine holes can be detected by thermal desorption spectroscopy (TDS). We made it clear that the conventional DIW rinsing after SPM treatment is insufficient for 0.1μm-diameter hole by using the TDS analysis and the simulation. The electrolytic ionized pure anode water can more effectively rinse than DIW rinsing in 0.1-μm-diameter holes with an aspect ratio of 10.

1. Introduction

In order to achieve high reliability of next-generation device characteristics, it is needed to suppress micro-contamination and to control device profile inside fine structures such as deep-submicron contact holes. For the purpose, it is required of cleaning to remove various contaminants without causing surface etching, profile deformation, or degradation of film characteristics.

As the countermeasures, choosing cleaning chemicals and conditions can control the structure profile and chemical residue. New chemicals with additives, such as surfactants or chelating agents, have been proposed and may improve penetration and contamination removal efficiency. Even with the new chemicals, complete contamination control inside deep-submicron structures has not been achieved. Further improvement in cleaning technology is necessary.

To find a suitable cleaning process for fine structures, a method of examining contamination inside the structures is needed. The conventional technology for metallic contamination analysis, however, has not sufficiently satisfied such a requirement. For example, an analysis method with high sensitivity, such as total reflection x-ray fluorescence (TXRF), or inductively coupled plasma mass spectrometry (ICP-MS), cannot be applied for analyzing the inside of deep-submicron structures. Methods which can be used for analyzing structures, such as field emission Auger electron spectroscopy (FE-AES), do not have a sensitively of less than 10^{14}atoms/cm^2. The developing analysis technologies for deep-submicron structures is also necessary.

First, this paper reviews various issues of cleaning inside deep-submicron structures. Next we explain our proposed analysis methods for the remaining metallic contamination and the residual ions in deep-submicron-diameter holes with high aspect ratios. We report analysis results, an approach to effective rinsing and simulation results for residual ions in deep-submicron holes.

2. Issues of Cleaning inside Fine Structures

Inside deep-submicron structures, cleaning has the following issues and problems seen in Fig.1.

(a) Penetration and displacement of chemicals

It has been reported chemicals can penetrate into fine structures by wet etching reactions.[1,2] In the case of general wet cleaning, however, simulation studies showed that liquid does not easily penetrate into and exchange inside fine structures.[3,4]

(b) Metallic contamination and particles

Metallic contamination in fine structures causes leakage current or degradation of dielectric characteristics. Particles inside fine structures induce contact failure.

It has reported more metallic contamination remains as hole-diameter becomes smaller.[5] It has reported intentional particle contamination inside deep-submicron holes may remain even after APM (NH_4OH/ H_2O_2/H_2O) cleaning.[6]

(c) Deposition films

During dry etching, deposit films are often generated inside fine structures. Composition and amount of the deposit depend on dry etching gases, conditions, and etched materials.

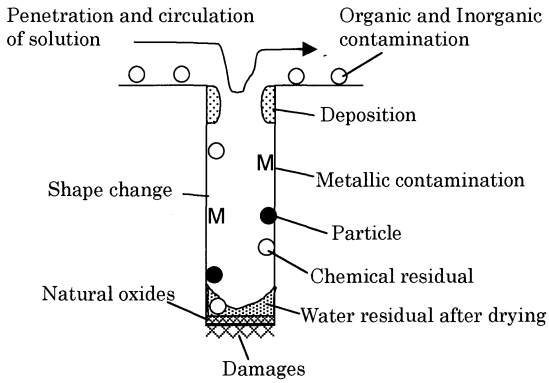


Fig.1 Issues and problems of cleaning inside deep-submicron holes.

(d) Residual chemicals

Some cleaning chemicals remain on surfaces. After SPM cleaning and hot DI water rinse, there are SOx residue of the order of 1E13 ions/cm^2 or more on flat surfaces. The amount of the SOx residue on a surface with deep-submicron holes is more than 10 times than that on a flat surface.[7]

(e) Profile deformation

Cleaning chemicals such as APM or diluted HF have etching property. The etching ability is essential to remove particle and natural oxide, but it causes profile deformation. The hole-side-wall deformation during cleaning, caused by different etching rates for

layered materials.[6] Such deformation may cause short circuit, leakage current, or contact failure.

(f) Damaged layer

The surface of submicron contact-hole bottom is damaged during dry etching or ion implantation. The contact resistance of poly-Si plug/n+-Si contact-holes changed with/without chemical dry etching (CDE).[8] CDE removes dry-etching damage. It is seen the damaged layer induces the contact resistance increase. In this case, the contact resistance increase is due to the interface oxide.[8]

(g) Drying efficiency

It has been reported water drops remain inside fine structures after spin drying.[3] Such residual water causes thick natural oxide layer called water mark. The contact resistance of poly-Si-plug/n+-Si contact holes dried by using spin drying is higher than that by using IPA-vapor.

(h) Chemical contamination from ambience

It becomes increasingly important to suppress contamination from the atmosphere. The amount of SO_4, NH_4 and organics on surfaces depends on cleaning processes and post-cleaning ambience.[9]

3. Metallic contamination in deep-submicron holes

In order to guarantee sufficient cleanness in fine structures, the contamination analysis technology inside fine structure is needed. We have reported an analysis method for the remaining metallic contamination and the residual ions in deep-submicron-diameter holes with high aspect ratios[5].

3.1 Analysis method for the metallic contamination in deep-submicron-diameter hole.

The method is based on conventional atomic absorption spectrometry (AAS), and uses device patterns with high density contact holes. With this method, metallic (Fe) contamination of the order of 10^{10} atoms/cm^2 can be easily analyzed inside 0.1 μm-diameter holes with aspect ratios of 10.

Figure 2 shows the experimental procedure for the quantitative analysis of metallic contamination in submicron structures; for example, Fe contamination inside a hole structure. Both types of SiO_2 films with holes (a) and without holes (b) were treated simultaneously. First the samples were intentionally contaminated with Fe solution. Next the contaminated samples were cleaned by an SPM solution for 10 minutes and were rinsed in DI water. After rinsing, the SiO_2 films of samples (a) and (b) were completely etched off by a DHF solution. The amount of Fe in the etching solution was analyzed by AAS.

The measured amounts of metallic contamination, in this experiment the amount of Fe, are to be treated as follows. The total amount of Fe contamination on the sample (a), with holes, can be expressed as;

A = the amount of Fe remaining on SiO_2(film surface + hole-side-walls + hole-bottoms) + the amount of Fe in SiO_2 film.

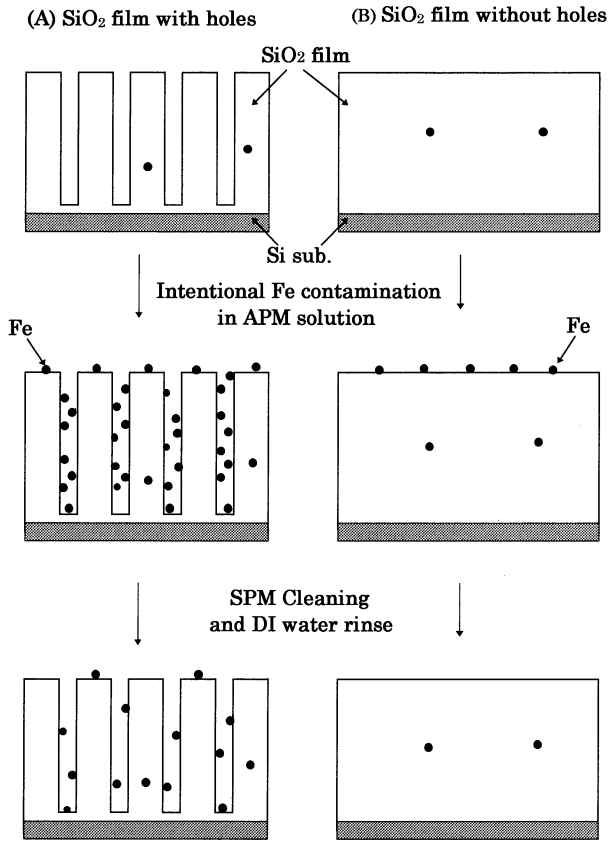
The total amount of Fe contamination on sample (b), without holes, can be expressed as;

B = the amount of Fe remaining on SiO_2 (film-surface) + the amount of Fe in SiO_2 film.

Therefore, the amount of Fe remaining inside the holes (hole-side-walls + hole-bottoms) is given by

$$C \approx A - [B \times \{1 - \text{hole area ratio on the sample (a) surface}\}] .$$

The difference in SiO_2 film volume between samples (a) and (b), due to the volume of holes in (a), is negligibly small.



A = the amount of Fe remaining on SiO_2 (film surface + hole-side-walls + hole-bottoms) + the amount of Fe in SiO_2 film.

B =the amount of Fe remaining on SiO_2 (film-surface) + the amount of Fe in SiO_2 film.

Inside the holes (hole-side-walls + hole-bottoms)

$C \approx A - [B \times \{1 - \text{hole area ratio on the sample (a) surface}\}]$

Fig. 2 Method for quantitative analysis of metallic contamination inside submicron structures. Fe contamination in holes is shown as an example.

3.2 Analysis results

The Fe concentration inside the holes (hole-side-walls + hole bottoms) calculated by using the measured results by AAS and Equation C is shown in Figure 3. As the hole diameter decreases, the remaining Fe concentration increases larger, although the surface area inside the holes decreases. The Fe concentration remaining inside the 0.2μm-diameter holes was 5.1×10^{10}atoms/cm^2 and was about 3 times greater than that remaining on the film surface. In samples with 0.1μm holes, the Fe concentration remaining in the holes was 2.8×10^{11} atoms/cm^2 and was about 16 times greater than that on the surface. The results show the concentration of Fe contamination, which still remains inside the holes after SPM cleaning and DI water rinse, drastically increases with decreasing hole diameter.

The hole area ratios were about 1.2% for the 0.1μm-diameter samples. The minimum area ratio required for analysis is about 1%, which is sufficient for analyzing devices such as 256M bit or 1G bit DRAMs with a minimum hole area of about 2%. The analyzing method can be effectively applied to device failure analysis and the development of new cleaning processes.

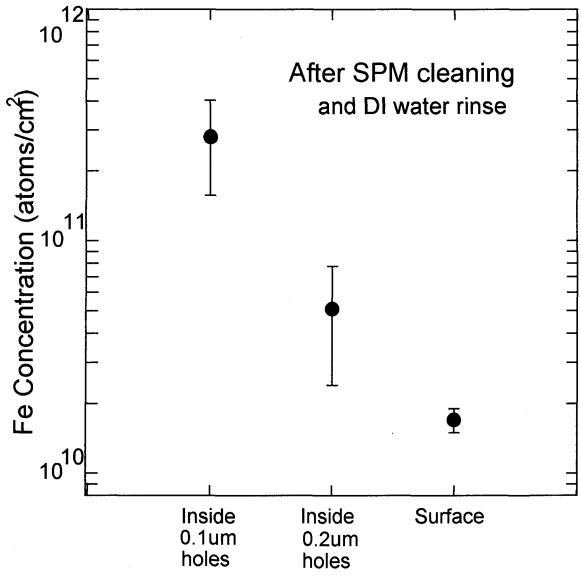


Fig.3 Fe concentration inside holes (hole-side-walls + hole bottoms) calculated by using the measured results from AAS.

4. Residual ions in deep-submicron holes

Residual ionic contamination, such as SOx species remaining on surfaces after SPM (H_2SO_4 / H_2O_2) treatment for resist removal and cleaning, is one serious problem. This is because SOx species tend to remain on surfaces even after rinsing. Such residual SOx easily induces metallic contamination[10]. Thus, in order to achieve high level of cleanliness in fine structures, reducing residual SOx in the fine structures is a very important issue. In this study, we report an analysis method and results, an approach to effective rinsing and simulation results for residual SOx ions in deep-submicron holes.

4.1 Analysis method by using Thermal Desorpsion Spectroscopy (TDS)

Thermal desorpsion spectroscopy (TDS) can be applied for analyzing the contamination produced in contact-holes, By heating sample wafers, thermal desorpsion can be observed regardless of surface structures. By using this characteristics of TDS, we applied TDS for analyzing residual species in deep submicron holes.

Figure 4 shows the experimental procedure for the analysis of ion contamination in submicron structures; for example, SOx contamination inside hole structures. SiO_2 films with a high density of holes (a) and SiO_2 films without holes (b) were prepared. Both types were treated simultaneously. The samples were immersed in SPM solution (H_2SO_4: H_2O_2 = 5:1, 100℃, 10 min) and rinsed by overflow of DIW (5 min).

The measured amounts of ion contamination, in this experiment, TDS intensity of SO, are to be treated as follows.

The total amount of residual SO on the sample (c), with holes, can be expressed as;

D = the amount of SO remaining on SiO_2(film surface + hole-side-walls + hole-bottoms)

The total amount of residual SO on sample (d), without holes, can be expressed as;

E = the amount of residual SO on SiO_2 (film-surface).

Therefore, the amount of SO remaining inside the holes (hole-side-walls + hole-bottoms) is given by

$$F \approx D - [E \times \{1 - \textit{hole area ratio on the sample (c) surface}\}] .$$

TDS intensity for unit area of sample surface was obtained for each sample (the samples with 0.1-μm- and 0.4-μm-diameter holes) by using the total area of the hole-inside.

Figure 5 shows TDS spectra of SO (m/e=48) for SiO_2 films with 0.2μm-diameter holes (a) and without holes (b). The samples were cleaned by SPM at 100℃ for 10 minutes and were rinsed in hot DIW for 5min. The TDS spectra of SO (m/e=48) were measured in the temperature range from 200℃ to 800℃. The large TDS peak for hole sample (a) was observed near 350℃.

4.2 Dependence the amount of residual SO on SPM temperature.

The SiO_2 films with 0.2μm-diameter holes and the SiO_2 films without holes were cleaned by SPM at 80℃～130℃ for 10 minutes and were rinsed in hot DIW for 5min. Figure 6 shows the dependence of SO peak intensity on SPM cleaning temperature for samples with holes and without holes. The peak intensities for sample with holes were larger than that for samples without holes. The intensity increases drastically with decreasing SPM cleaning temperature for both samples, especially for the sample with the holes.

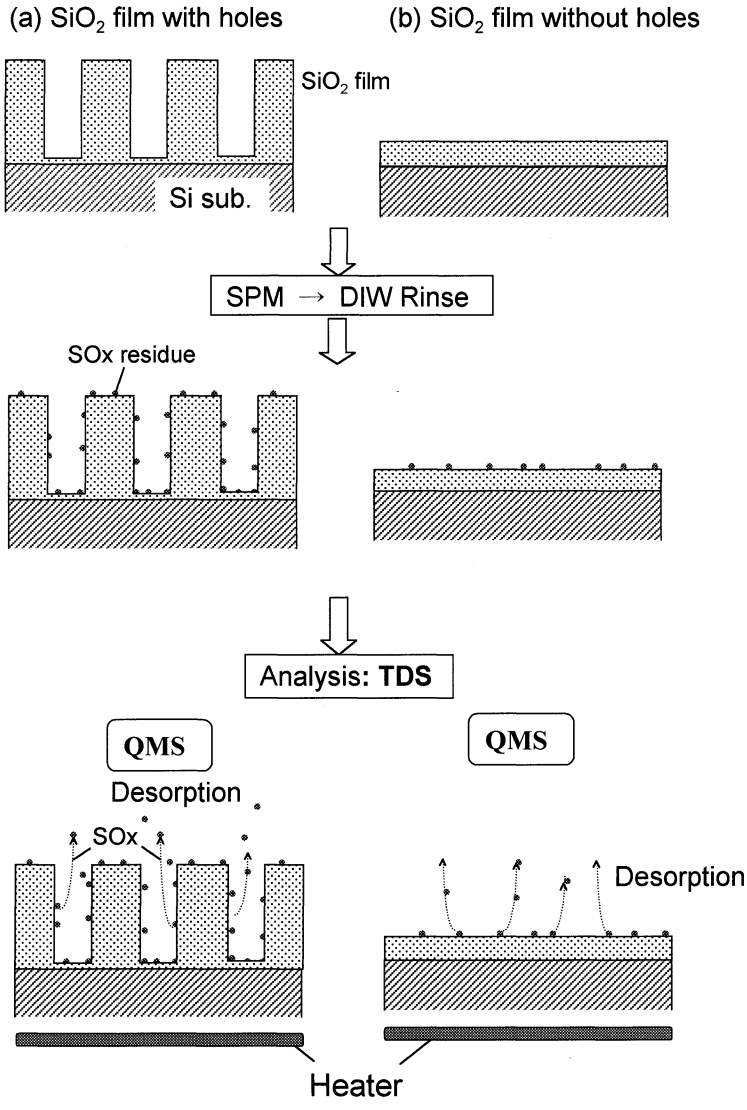


Fig. 4 Analysis method for residual ions in deep-submicron holes using Thermal desorpsion spectroscopy (TDS).

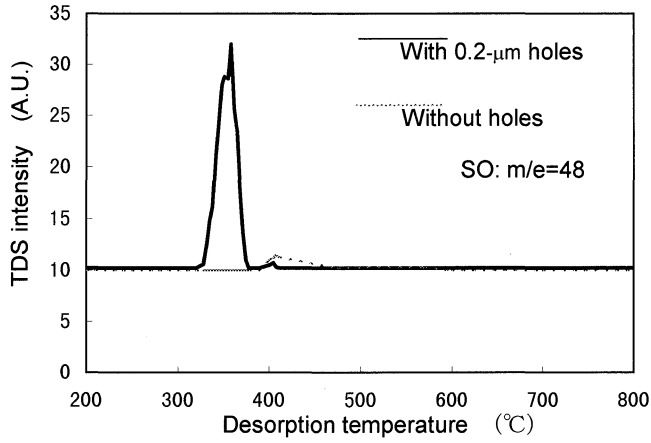


Fig. 5 TDS spectra (SO:m/e=48) for samples with 0.2-μm-diameter holes and without holes after SPM treatment and rinsing in DIW.

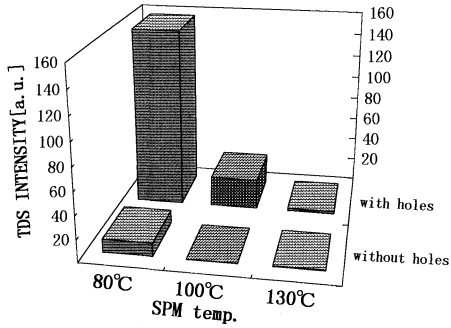


Fig. 6 The dependence of SO peak intensity on SPM cleaning temperature for samples with holes and without holes.

4.3 Dependence of the amount of residual SO on hole diameter.

The SiO_2 films with 0.1μm- and 0.4-μm-diameter holes were cleaned by SPM at 100℃ for 10 minutes and were rinsed in DIW for 5min. Figure 7 shows the TDS spectrum (SO) intensity for unit area of sample surface depending on hole diameter. The intensities were calculated the amount of residual SO inside each diameter-holes by the equation F. The TDS (SO) intensities for the samples after the DIW rinse dramatically increase with decreasing hole diameter. The result shows the rinsing effect reduces with smaller diameter hole.

4.4 An effective rinsing in deep-submicron holes using pure anode water[11)]

We show there are much residual SOx in smaller holes of deep-submicron diameters after the conventional DIW rinsing as shown Figure 7. We have proposed an effective rinsing process which uses the electrolytic ionized pure-anode water (pure-anode water) for the residual SOx inside the fine holes[12)]. The pure anode water is generated on the plus side by electrolysis pure water. TDS spectrum (SO) intensity after pure anode water rinsing showed little dependence on hole diameter. The pure anode water rinse can reduce the amount of residual SO in 0.1-μm-diameter holes down to below 1/6 compared with the conventional DIW rinse. Thus, inside the deep-submicron-diameter holes with a high aspect ratio, pure anode water can rinse the residual SOx more efficiently than conventional DIW can.

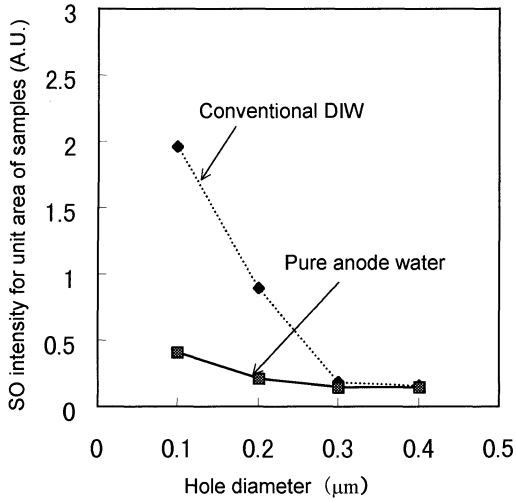


Fig. 7 TDS spectrum (SO) intensity for unit area of samples depending on hole diameter after SPM treatment and rinsing in (a) conventional DIW and (b) Pure anode water .

We speculate there are two reasons for the rinsing effect of pure anode water. First, we have reported that the number of OH radicals (•OH) in pure anode water is larger than that in DIW[13]. The OH radical is a very active oxidizing species. Such radicals are thought to be effective in removing residual SOx. The hole-diameter effect, however, cannot be sufficiently explained by existence of OH radicals. Then the second reason is supposed as follows. The cluster size of water molecules of the pure anode water is thought to become smaller, by electrolysis, than that of DIW and therefore the pure anode water can easily diffuse into and out of the deep-submicron holes. With these characteristics, the anode water can easily enter into the deep-submicron hole and can effectively remove the residual SOx inside holes with the active oxidizing species.

4.5 Simulation of residual ionic concentration inside holes[14]

Dependence of residual ionic concentration on holes diameter was calculated by using a fluid simulator. The concentration of SOx was calculated under the assumption that the diffusion velocity reduce in proposition to the quadratic function of distance from the wall. The concentration was calculated for 0.1μm～0.4μm –diameter hole with 1μm depth.

Figure 8 (a) and (b) show the dependence of the concentration of SOx ion at the center of hole-bottom and at the center of hole side-wall on the rinsing time for each hole diameter, respectively.

As the hole diameter decreases, the concentration of SOx ion increases in the case of both the bottom and the side wall. Especially, the rinsing efficiency drastically lows at the bottom center of the 0.1μm-diameter hole as shown Figure 8(a). This indicates the conventional DIW rinsing for 10min (600sec) is insufficient for 0.1μm-diameter holes with an aspect ratio of 10.

5. Conclusions

We proposed the methods analyzing for the remaining metallic contamination and the residual ions in deep-submicron-diameter holes with high aspect ratios. The first method is based on conventional atomic absorption spectrometry (AAS), and uses device patterns with high density contact holes. With this method, metallic (Fe) contamination on the order of 10^{10} atoms/cm^2 can be easily analyzed inside 0.1-μm-diameter holes with aspect ratios of 10. The second method uses thermal desorption spectroscopy (TDS) to detect the residual ions in fine holes.

We made it clear that the conventional DIW rinsing after SPM treatment is insufficient for 0.1μm-diameter hole by using the experimental result and the simulation. As one of countermeasures, we proposed a cleaning technology using the electrolytic ionized pure anode water, which can more effectively rinse and remove SOx species after SPM treatment than conventional DIW rinsing in 0.1-μm-diameter holes with an aspect ratio of 10.

These analysis methods for fine structures are useful for the practical investigation of contamination control and cleaning processes of ULSI devices. Such a new technology of rinsing after chemical cleaning is useful for manufacturing next-generation fine structure devices.

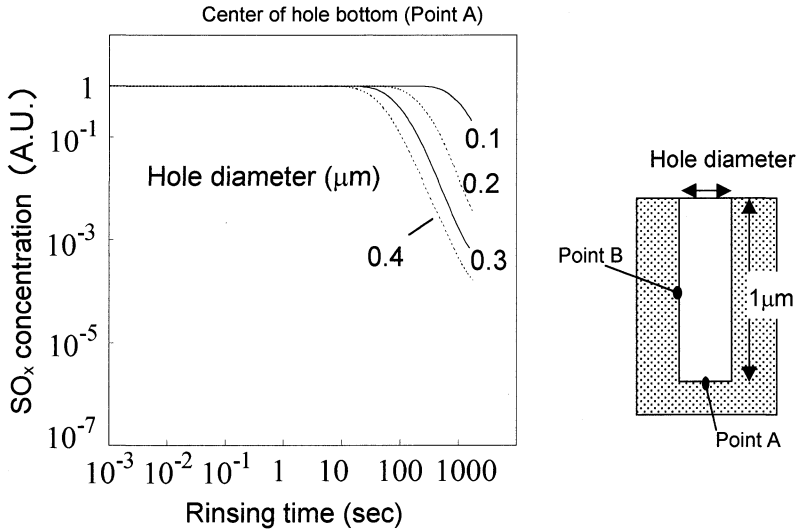


Fig. 8(a) Dependence of the concentration of SOx ion at the center of hole bottom on the rinsing time for each hole diameter.

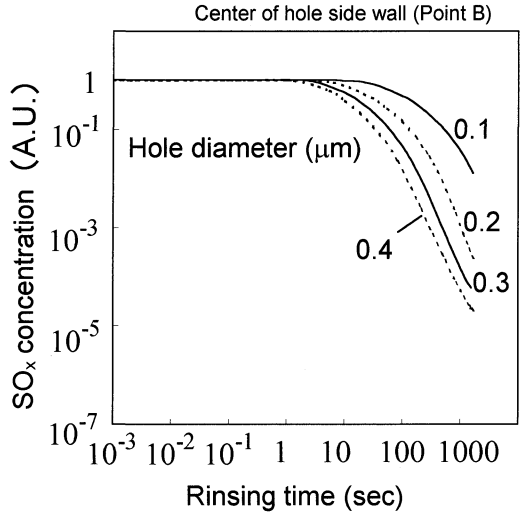


Fig. 8(b) Dependence of the concentration of SOx ion at the center of hole side wall on the rinsing time for each hole diameter.

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EVALUATION OF CHELATE ADDED APM CLEANING SOLUTION

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ABSTRACT

Wafer cleaning studies have been performed so as to understand the influence of chelate additives on metal contamination in diluted APM (NH4OH/H2O2/H2O) cleaning solutions. Catechol showed the best efficiency in the removal of metal contaminants on wafer among various clelate additives examined in this work, and no deterioration effects such as particles and organic contamination on wafer were found. 200 ppm of catechol in APM was enough to reduce metallic contamination on wafer from $1X10^{13}$ atoms/cm^2 to $1X10^{10}$ atoms/cm^2. The pre gate oxide cleaning by APM solution with 200ppm of catechol showed compatible result to cleaning by APM solutions followed by dilute HF in terms of minority carrier lifetime. It was also found that APM cleaning solution with 200ppm catechol improves the dielectric breakdown characteristics through TDDB test.

INTRODUCTION

As the packing density increases in VLSI manufacturing process, the wafer cleaning process is of importance in view point of device yield and reliability. Over the last quarter century, Si substrate surfaces have been cleaned by RCA cleaning procedure, where the process consists of sulfuric-peroxide (SPM), ammonia-peroxide (APM), and hydrochloric-peroxide (HPM)[1]. Though, there are several advantages in applying RCA cleaning to wafer cleaning process, simplified and modified wet cleaning process are needed for higher productivity and lower cost [2]. Especially, APM cleaning solution is known to be effective in removing polymers and particles on Si wafer, but it also has several critical problems such as metal recontamination and degradation of Si surface micro-roughness [3]. To prevent roughness of Si surface and metal re-adsorption in the APM solution, more diluted chemistry and the studies for new additives are needed. Akiya et. al. developed modified APM cleaning solution, which is composed of, NH4OH, H2O2 and chelating agent, to solve metal recontamination problems[4]. In this work, we examined various chelate agents to choose better chelate agent in terms of metal contamination and deterioration affects such as particles and organic contamination. We also determined the optimum concentration of the chelate agent in APM solutions, and proved the cleaning ability of the chelate added APM solution by comparing minority carrier lifetime and

dielectric breakdown characteristics with normal APM solutions.

EXPERIMENT

Variation in the surface concentration of Fe, Ni, Cr Al and Cu due to the APM treatment was examined. Polished (100) Si wafers, 6 inches in diameter and P-type, 10 ohm·cm were used in the present experiment. APM solution was prepared by mixing de-ionized water with H2O2 solution(30%) and NH4OH solution(30%). The APM treatment was followed by QDR and rinsing with de-ionized water for 10 min. In order to examine the adsorption of metals in APM solution, the standard solution for the atomic absorption spectrochemical analysis containing metallic impurities were intentionally added to the APM solution. Wafers preliminary cleaned by the RCA cleaning process were used in this adsorption experiment. Moreover, for testing metal removability of chelate-added APM solution, metal contaminated wafers which were prepared by dipping in the intentionally contaminated APM solution were dipped into the APM solution with various concentrations of chelate agent in the range of 0 to 500ppm. The APM solutions with chelate agent were prepared by mixing NH4OH(30%) solution in which chelate agent was dissolved with H2O2(30%)/H2O mixture solution. Various chelate agents such as carboxylic, phosporic acid and hydroxyl aromatic types were examined. The surface concentration of the metals on wafer was measured by atomic absorption spectroscopy and total reflection X-ray fluorescence method. The detection limit for Fe,Ni,Cu,Al and Cr is about 10^9atoms/cm^2. Additionally, to check out the etch rate and particles in APM solution, ellipsometer and particle counter were used.

RESULTS AND DISCUSSION

Table.1 shows the metal contamination level of Si wafer which was cleaned with APM solution, with volumetric ratio of 1:4:20 for NH4OH : H2O2 : H2O and the treatment temperature and time was 70°C and 10 min, respectively. Metal contamination level was analyzed with Atomic Absorption Spectroscopy. As shown in table.1, Al, Ni and Fe contamination level of Si wafer surface after APM treatment is relatively high with 10^{11}atoms/cm^2 because the solubility of metals in alkaline solution is very low. Additionally, the influence of impurity concentration in SC1 solution on the surface cleanliness of wafers was examined for Fe and Al. The results are shown in fig.1. Etch APM solution that has different metal contamination level was made by treating different numbers of implanted dummy wafers. As treating the implanted wafers in APM solution, the metal contaminant accumulation in APM solution was lineally increased, and the contamination level on the wafer was also lineally increased up to a level of 10^{13}atoms/cm^2. These results indicate that the metal contaminants accumulation and readsorption on the wafer can easily occur in the APM solution that has the pH value of around 10.

We evaluated the effects of some chelate agents on metal removal from the Si surface in APM solution. From the screening test for several chelate agents which included carboxylic acid type, hydroxyl aromatic type and phosphoric acid type, catechol showed

the best complexing ability with Fe as shown in fig. 2. The initial metal contamination level around 10^{13}atoms/cm^2 was decreased down to a concentration level of 10^{10} atoms/cm^2 with 200ppm of catechol added APM solution. Fig.3 shows metal removability of catechol added APM solutions for different catechol amounts. We contaminated p-type(100) silicon wafers with metal standard solutions up to the level of $1x10^{12\sim13}$atoms/cm^2, then cleaned with catechol added APM solution. It shows that 200ppm of catechol in APM solution is enough to remove Fe, Al contaminants on wafers. Fig. 4 showed us that there were no changes in particle characteristics and etch rate by adding catechol to the APM solution. To assure the surface condition after catechol added APM cleaning, SCA (Surface Charge Analyzer) analysis was carried out. The results are shown in fig.5, 6. The test wafers were made by different cleaning method prior to 100 Å gate oxidation. The wafer that was cleaned with catechol-added APM solution shows the lowest interface trap charge and highest minority carrier lifetime. These results indicate that catechol could effectively prevents metal adsorption in APM solution and leaves no organic residues on the wafers.

Thin gate oxides (40 Å) Qbd were also measured to evaluate the effect of catechol added APM solution on the electrical property of semiconductor device as shown in fig.7. The wafer cleaned by catechol added APM solution shows better Qbd characteristics than one by normal APM solution. This difference is related to the condition of silicon surface as revealed by SCA and AAS characterization.

CONCLUSION

In this work, we have found that 200ppm of catechol in the APM solution is enough to prevent metal contaminants re-adsorption from the contaminated APM solution, and there were no deterioration effects such as particles and organic residues on wafer from catechol in APM solution. We also confirmed the cleaning effect of catechol added APM solution for thin gate oxide pre-diffusion process by observing longer minority carrier lifetime and more stable dielectric breakdown characteristics than the normal APM solutions.

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Table.1 The metal contamination level on the Si surface after APM cleaning

Metal	Na	Al	Fe	Ni	Cu	Zn
Surface Concentration (10^{10}atoms/cm^2)	10.5	14.2	7.5	4.4	2	2.5

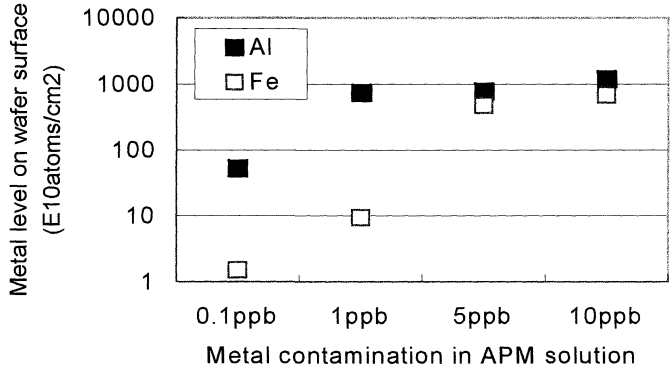

Fig.1 Metal contaminants accumulation and readsorption in APM solution

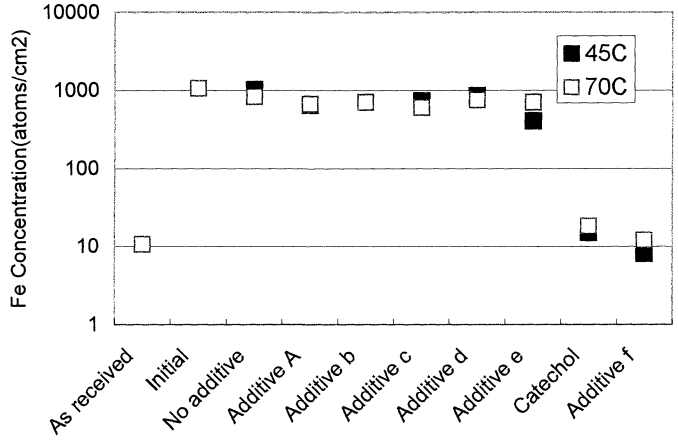

Fig.2 The effect of 200ppm catechol on removal of Fe in the APM solution

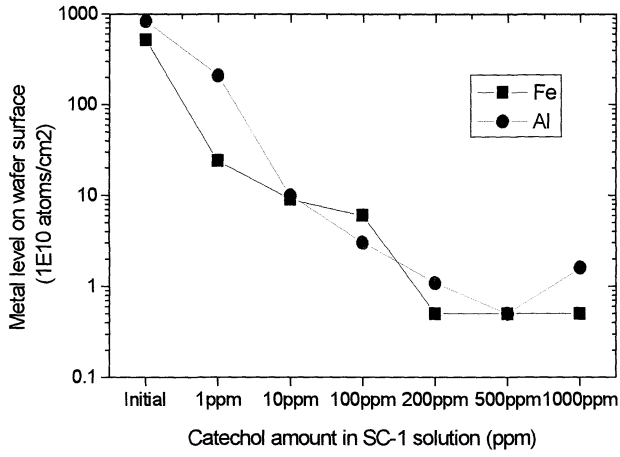

Fig.3 The dependence of metal(Fe, Al) contaminants removability on Catechol amount in APM solution

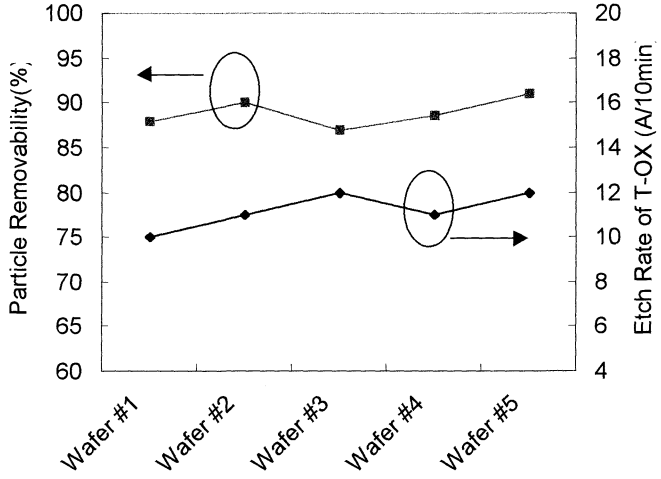

Fig.4 Particle removability and etch rate of 200ppm catechol added APM solution

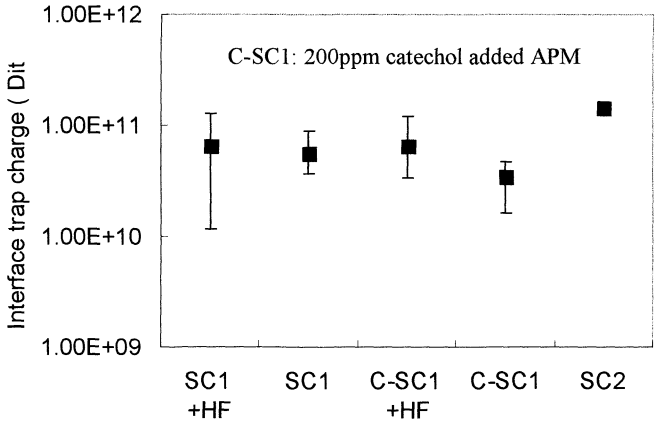

Fig.5 The dependence of gate oxide interface property on pre-cleaning process(Interface Trap Charge)

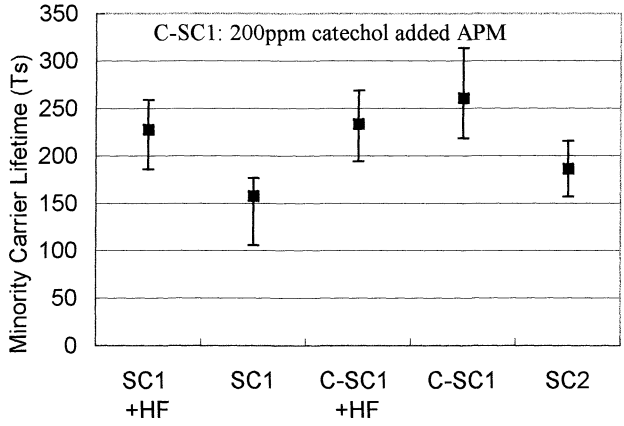

Fig.6 The dependence of gate oxide interface property on pre-cleaning process

(C-SC1 is catechol added SC-1)

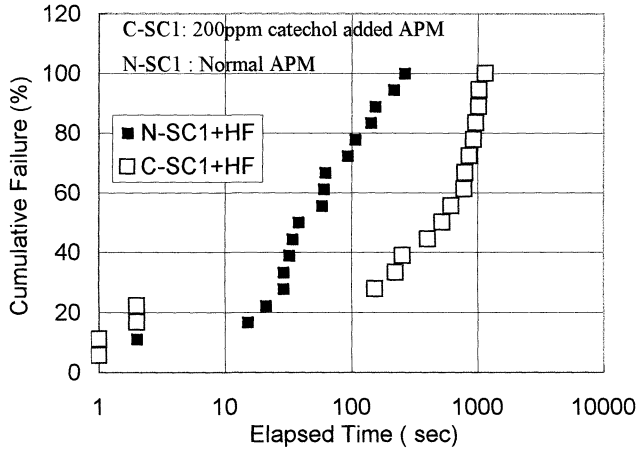

Fig.7 The dependence of thin gate oxide (40A) reliability on pre-cleaning process (@Room temp, -6.1V)

THE CONTROL OF DISSOLVED GASES IN AQUEOUS-BASED SEMICONDUCTOR PROCESSING

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ABSTRACT

Wet cleaning of wafers during the semiconductor production process often requires uniform removal of a few nanometers of material. Ideally, a single cleaning chemistry can be found that etches all exposed features at a comparable rate. Etch rates near 1 nm/min are desired for batch process and near 10 nm/min for single-wafer processes. A mixture of 500:1 DHF (dilute HF) with dissolved oxygen controlled near parts-per-million (ppm) levels has been found to meet these requirements for post copper CMP (chemical-mechanical polishing) cleans with exposed SiO_2, Ta/TaN and Cu metal. A more aggressive clean using DHF and HCl with controlled oxygen has proved very effective at removing copper contamination from the backsides of wafers when covered by a Si3N4 layer acting as an efficient barrier against Cu diffusion into the Si..

INTRODUCTION

Figure 1 shows the cross section of a post Cu CMP device. Cleaning requires solvation of surface ionics along with the dissolution of approximately 5 nm of the surface to undercut and remove particles, remove surface damage and expose imbedded ions. Both DHF (dilute HF) and NH_4OH have been used as cleaning etchants in oxide CMP. Like the NH_4OH-based SC-1, DHF is effective in removing particles from bulk SiO_2 and "bare" silicon with a native oxide (1). DHF is preferred over NH_4OH because metal ions tend to be more soluble in acidic solutions. Also, the range of oxide etch rates available with DHF is considerably larger than those with NH_4OH solutions.

The etch rates of oxides in DHF vary dramatically with their chemical composition and deposition conditions. Ideally, it would be possible to control the oxide etch rate by the concentration of DHF and control the copper etch rate with a second, independent variable. Figure 2 shows the results of cleaning metallic copper deposited on hydrophobic silicon from a copper-spiked HF solution (2). SC-2 solutions with varying HCl and H_2O_2 flows and a total flow of 1,760 ml/min were dispensed in the nitrogen-purged environment of a spray acid processor. The concentration of HCl had little effect on the total Cu removed as measured by TXRF. The concentration of H_2O_2 also had little effect, as long as some H_2O_2 was present. Even concentrated HCl solutions did not remove metallic copper in the nitrogen atmosphere without the addition of an oxidant. HCl solutions in an air ambient, however, do remove copper metal from wafers (3). It may be possible to

control the etch rate of copper in DHF solutions by varying the concentration of dissolved oxygen in the solution.

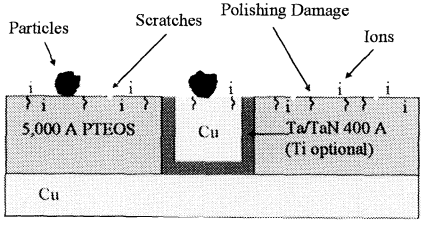

Figure 1: Cross section of a typical post Cu CMP device showing typical contamination and surface damage.

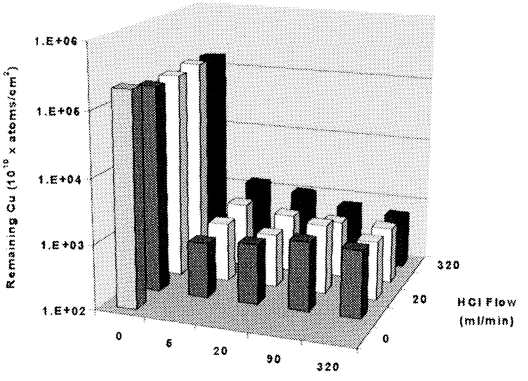

Figure 2: Removal of copper metal by SC-2 as a function of HCl and H_2O_2 concentrations as measured by TXRF.

After the surface has been cleaned and annealed, a thin Si_3N_4 "cap" or "etch stop" layer is deposited which seals the copper metal (Figure 3). Copper contamination, however, may still exist on the back of the wafers due to handling, the CMP process or the anneal process. Due to the fact that the stepper is shared between "copper" and "non-copper" metal devices, this backside contamination must be controlled to avoid any cross Cu contamination. At this point, the entire wafer is encased with Si_3N_4 and a more aggressive cleaning chemistry can be used, so the addition of HCl to the HF:O_2 mixture was investigated.

THEORY

Equations 1 to 3 are the individual chemical reactions believed to take place when etching copper in a DHF solution with dissolved oxygen. Figure 4 shows the solution pH as a function of concentration for HCl and HF. The pH of the HCl solutions in Figure 2 range from approximately –0.25 to 1.5. In this range, little effect of pH is seen on the total copper removed. Therefore, Reaction (3), whose rate is expected to be proportional

to $[H^+]^2$, is apparently not the rate-limiting reaction. While not investigated in this work, it is presumed that Reaction (3) is also not the rate-limiting reaction in the case of copper removal by DHF solutions near pH 2.

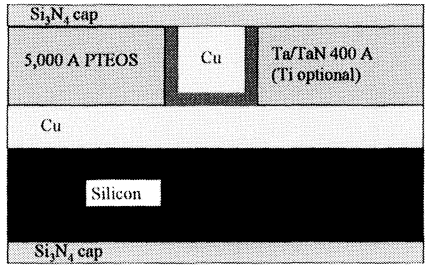

Figure 3: Patterned wafer after CMP, clean and nitride cap deposition.

$$O_2(g) \rightarrow O_2(aq) \quad [1]$$

$$2Cu(s) + O_2 \rightarrow 2CuO(s) \quad [2]$$

$$CuO(s) + 2H^+(aq) \rightarrow Cu^{++}(aq) + H_2O \quad [3]$$

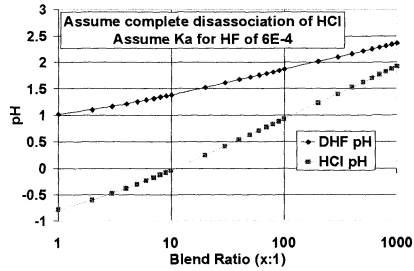

Figure 4: pH as a function for concentration for HCl and

The large increase in copper removal shown in Figure 2 of between 0 and 5 ml/min H_2O_2 in the SC-2 mixture indicates the possibility of controlling the copper etch rate by controlling the oxidizing species. Figure 5 shows the Pourbaix diagram for copper (4). Corrosion of copper in acidic aqueous solutions is *thermodynamically* favorable when the oxidation-reduction potential (ORP) of the solution E is greater than approximately 0.1 V.

The ORP of the acidic solution can be calculated using the Nernst equation applied to the chemical equilibria in Equation 4 (5). O_2 concentrations ranging from saturated to 1 ppb (a typical lower limit to O_2 concentration) give solution ORPs from 1.24 to 1.17 V. This range of ORPs and pH levels near 2 is marked by the small, dark rectangle centered above the word "corrosion" in the acidic portion of the Pourbaix diagram (Figure 5). This parameter space, used in this experiment, is entirely within the "corrosion" or etching regime. Therefore, etching of copper is *thermodynamically* favorable. We must consider kinetic limitations to estimate the reaction rate.

$$O_2 + 4H^+ + 4e^- \leftrightarrow 2H_2O \qquad E^0 = 1.229\ V \qquad [4]$$

The reaction rates for the reactions in Equations 1 and 2 are expected to be linear with O_2 concentration. Given the diffusion coefficient D for O_2 in water of 2×10^{-5} cm^2/sec, it is possible to estimate the flux of O_2 to the surface (6). Assuming 5 ppm of dissolved O_2 and a 10^{-3} cm boundary layer, the O_2 flux at the surface would be 10^{15} atoms/cm^2•sec. This flux is sufficient to support a 6-nm/min Cu etch rate.

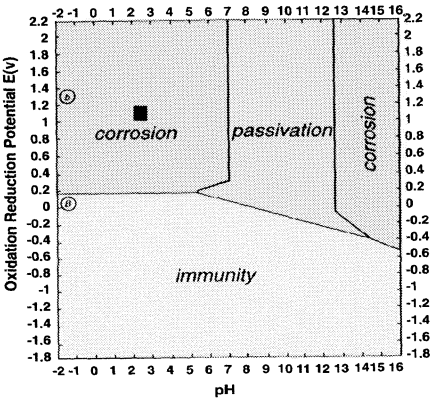

Figure 5: Pourbaix diagram for copper.

It is possible to determine whether the rate-limiting step is the diffusion of O_2 to the surface (Eq. 1) or the reaction of O_2 and Cu at the surface (Eq. 2) by measuring the variation in reaction rate with temperature. The rate of diffusion varies linearly with temperature, or 3% with a 10° C increase near ambient (6). Chemical reaction rates typically grow exponentially with temperature and can double with each 10° C increase. The solubility of O_2 in water also varies with temperature. The experiments to identify the rate-limiting step were not performed in this work.

A more aggressive cleaning solution can be used when removing backside copper contamination because the wafer is entirely encapsulated in Si_3N_4 and all exposed copper compounds are to be removed completely. The addition of HCl is expected to increase the removal rate of copper compounds by two mechanisms. First, the strong acid HCl will greatly reduce the pH of the solution (Figure 4) and will, therefore, increase the rate of dissolution of CuO(s) shown in Equation 3. Second, HCl acts as a complexing agent for Cu^{++} ions, effectively removing them from the cleaning solution. A third increase is expected due to heating the solution from ambient to 70° C, which will increase the etch rate of the nitride. It is not known whether shifting the balance between the various HF species (HF, F^-, H_2F_2, HF^-) with pH will improve removal (7). However, it is known that the selectivity between oxide and nitride can be reduced by using heated dilute HF.

EXPERIMENT

Etch experiments were carried out in a MERCURY® MP Surface Conditioning System, a centrifugal spray acid processor (8). In the acid processor, four cassettes of 25 wafers are mounted on a turntable in a sealed chamber. Cleaning chemistries and rinse water are atomized onto the wafers from spray posts mounted at the center of the chamber (near the axis of rotation of the turntable) and on the outer chamber wall. When the DHF etchant is atomized, the tiny drops of liquid have a very high surface-area-to-volume ratio. The dissolved O_2 concentration in the DHF nearly equilibrates with the atomizing gas before striking the surface. The concentration of dissolved O_2 in the DHF can be controlled by the volume fraction of O_2 in the atomizing gas.

If very precise control of the dissolved O_2 is necessary, the DHF can be equilibrated with the O_2 in the atomizing gas in a commercial "degassification" module normally used to remove dissolved oxygen. If the O_2:N_2 blends in the degassification module, the atomizers and the chamber volume are matched, the O_2 concentration in the DHF will remain in equilibrium with the matched gas and then will remain constant throughout the system. Figure 6 shows the plumbing modifications to the spray processor for control of dissolved O_2. The degassifier was not used in this experiment.

Using the hardware of Figure 6, 500:1 DHF at 21° C was dispensed on 200-mm wafers for varying times for post-Cu CMP cleans. The total gas flow used for atomization was held constant at 140 lpm. Oxygen flow rates in this gas varied from 4 to 40 lpm with the balance being nitrogen. This resulted in a blend that was 2.8% to 29% O_2 by volume in N_2. The mass loss of Cu was determined either by weighing the wafer before and after each etch on an analytical balance or by directly measuring the thickness loss with x-ray fluorescence.

Two types of Cu challenge wafers were prepared for backside cleaning studies. First, in the spin (tournette) method, a 0.016 M Cu solution in 5M HNO_3 was dispensed on stationary wafers with each film type for 60 seconds. The wafers were then spun dry at 400 rpm. While the form of this copper contamination is artificial and may not represent contamination encountered in production, the method provides repeatable copper contamination levels near 10^{14} atoms/cm^2.

A second type of backside cleaning challenge wafers was prepared by exposing clean wafers to the ambient of a copper physical vapor deposition (PVD) tool. Wafers were placed in the chamber of an Applied Materials P5000 PVD system under flowing H_2 at 200° C for 80 seconds. Residual copper in the chamber contaminated the wafers to levels above 10^{15} atoms/cm^2. X-ray fluorescence (XRF) measurements indicated that the copper was primarily metallic, although some copper-fluorine bonds were also detected. It is not known to what extent the copper diffuses into the film. The surface of the film must be etched away to remove indiffused copper.

Pre-clean and post-clean levels of copper were measured by total-reflection x-ray fluorescence (TXRF). As TXRF cannot be performed on the rough backsides of wafers, all measurements were performed on the front (device) side of the wafers. Cleaning tests

were performed with the wafers inverted in the process cassette to determine backside cleaning efficiency.

The hardware indicated in Figure 6 was used to dispense a mixture of 2,000 cc/min of 500:1 DHF blended with 125 cc/min of HCl. The wafers were exposed to this mixture at 70° C for 4.5 minutes followed by DI water rinsing and a spin dry in a nitrogen atmosphere. The acid solution was atomized by a blend of 4 l/min O_2 and 136 l/min N_2 (2.9% O_2). The cleaning efficiency was determined by TXRF measurements before and after the clean.

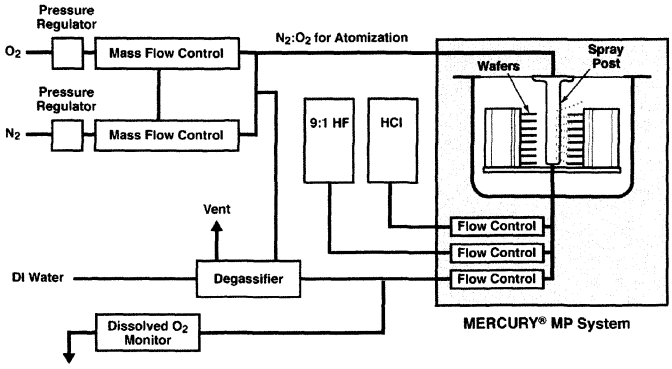

Figure 6: System to control precisely the dissolved gas concentration of liquids in a spray processor. Initial experimental work utilized rotometers in place of the mass flow controls to control the O_2:N_2 blend.

RESULTS

Figure 7 shows the amount of bulk Cu removed after 4.5 min in 500:1 DHF as a function of O_2 flow. The etch rate is linear with O_2 concentration for this post-Cu CMP clean. The positive extrapolated etch rate at zero oxygen flow may be related to the etching of the native oxide that spontaneously forms on exposure of copper to air. Table 1 shows the total removals in 4.5 minutes of various films in 500:1 DHF with 4 l/min O_2, 136 l/min N_2 atomization flow (2.9% O_2).

Figure 8 shows the removal efficiency of copper from various films by 500:1 DHF at 70° C with 4 l/min O_2, 136 l/min N_2 atomization (2.9% O_2). HF:O_2 is sufficient to remove copper nitrate from any of the films and copper metal from the oxide films. HF:O_2 does not, however, totally remove the copper deposited on nitride wafers in the P5000 process. HCl was added and the mixture heated to 70°C to increase the copper removal efficiency. Figure 9 shows the copper removal efficiency for a 4.5-minute exposure to the HF:O_2 and HF:HCl:O_2 chemistries. The backside copper contamination is removed completely by the hot HF:HCl:O_2 chemistry. Table 1 lists the various films and the Ångstroms removed by the HF:HCl:O_2 process.

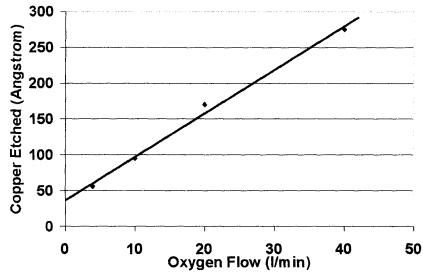

Figure 7: The etch rate of Cu in 500:1 DHF as a function of O_2 flow.

Table 1: Etch rates of films in DHF:O_2.

Substrate	Amount etched In Å HF:O_2 at 21° C	Etch rate In Å/min HF:HCl:O_2 at 70° C
Thermal oxide	8	15 ± 2 Å
TEOS oxide	38	20 ± 1 Å
Silane oxide	26	20 ± 2 Å
APCVD Si_3N_4 (Low Density)	27	19 ± 1 Å
LPCVD Si_3N_4	5	19 ± 1 Å
TaN	0	± Å
PVD copper	57	100 ± 20 Å
ECD copper	59	100 ± 20 Å

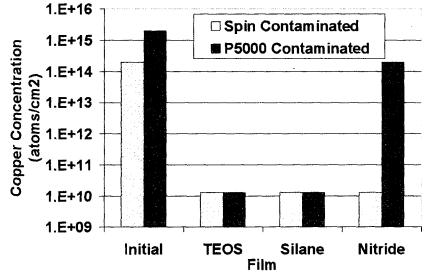

Figure 8: Removal efficiency of copper from various films with HF:O_2.

CONCLUSIONS

The etching of Cu metal in solutions of 500:1 DHF is linear with the concentration of dissolved O_2. Copper removal from 4 to 27 nm in a 4.5-min etch are controllable with O_2 concentrations of 2.9% to 29% by volume in N_2. The linear behavior indicates that the reaction is limited either by the transport of O_2 to the surface or the reaction of O_2 and Cu at the surface to form CuO. This DHF:O_2 chemistry shows great promise for post Cu

CMP cleans. The more aggressive HF:HCl:O_2 clean at 70° C was very effective in removing gross copper contamination from the backside of the wafer.

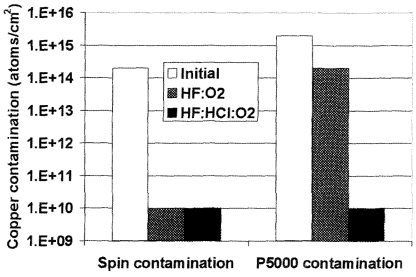

Figure 9: Removal efficiency of copper from nitride with HF:O_2 and HF:HCl:O_2.

ACKNOWLEDGMENTS

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ULTRAVIOLET LIGHT STIMULATED HALOGEN CHEMISTRY ON CLEANING SILICON SURFACES

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The effect of ultraviolet light stimulated halogen chemistry on the removal of copper and carbonaceous contamination from silicon surfaces is determined as a function of gas chemistries, processing pressure, temperature, and UV light intensity and wavelength. At an initial metal contamination level of $10^{13}/cm^2$, metal removal efficiency depends strongly on the processing temperature, moderately on the UV intensity and exposure time. Copper removal to the detection limit of XPS is observed at elevated temperature (~110°C) with some surface roughening due to etching of silicon. Copper removal efficiency is inversely proportional to the chlorine pressure at room temperature but independent of the chlorine pressure at higher temperatures (~110°C). Reduction of copper oxidation states upon UV radiation indicates the formation of surface species with higher volatility. Synchrotron-TXRF is used to quantify the metal removal efficiency at realistic metal contamination levels ($<10^{11}/cm^2$), and similar dependencies on process pressure and temperature were observed.

INTRODUCTION

The continuous scaling of device dimensions and the increasingly stringent environmental, safety, and economic requirements dictate more effective surface cleaning/preparation methods prior to gate oxidation/dielectric deposition. Considerations include more reliable dielectric/silicon interfaces, the reduction of hazardous chemicals, and ultra-pure water consumption. The acceptable metallic contamination level prior to gate oxidation has become so low (3×10^8 atoms/cm^2) that it poses challenges not only to process development but also to surface analytical techniques in quantifying the contamination concentration[1]. Metal contamination in a metal-oxide-semiconductor device degrades its electrical performance by creating charge generation-recombination centers, and/or affecting the oxide breakdown strength[2].

Wet chemical processing has been the dominant wafer cleaning technology to remove damage and contamination introduced to the wafer surfaces from other fabrication processes, materials, equipment, and humans. However, a typical wafer plant processing 1,500 eight-inch wafers daily consumes approximately 500 gallons of

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hazardous chemicals and 10-20 million gallons or more of ultra-pure water for rinsing and drying[3]. To tackle the environmental challenges and improve wafer cleaning efficiency, various dry cleaning processes using thermal[4], plasma[5], or short wavelength (ultraviolet, UV) radiation[6,7]excitations, have been studied as a low temperature replacement for wet cleaning processes to reduce chemical consumption. Dry cleaning can reduce chemical consumption by a factor of 1,000 or more, and lower the amount of ultra-pure water needed to rinse the wafers, and has shown comparable efficiency in removing surface contamination except for alkali metals (such as Ca, Na) and particles. These dry cleaning processes complement many wet chemical cleans, yet the mechanisms by which the contaminants are removed from silicon surfaces and their effect on the resulting electrical property of the device are not well understood.

In this work, we studied the effect of ultraviolet (UV) light stimulated halogen chemistry on metal and carbonaceous contamination removal from silicon surfaces, as a function of gas chemistries, processing pressure, temperature, and UV light intensity and wavelength. X-ray photoelectron spectroscopy (XPS), synchrotron total reflection x-ray fluorescence (Synchrotron-TXRF), and atomic force microscopy (AFM) have been utilized to determine surface termination, chemical states, contamination concentration and roughness induced by the process.

EXPERIMENTAL SETUP

The experimental apparatus consists of an analytical chamber on which x-ray photoemission spectroscopy (XPS) is equipped to allow determination of chemical composition and states: A process chamber, a loadlock chamber, and the XPS chamber are connected by gate valves to allow transferring samples under high vacuum without ambient contamination and sample analysis before and after the process. A monochromatic Al Kα source at 1486.6 eV was used, and the pass energy was typically set at 23.5 eV to obtain high-resolution photoemission spectra. The process chamber is made of ceramic, with opening ports and O-ring grooves cast-formed into the ceramic material. An array of holes is opened on two sides of the ceramic chamber to allow uniform gas distribution and pumping. The chamber is then compression fitted to stainless interface plates via Teflon coated O-rings to allow vacuum seals against the gate valves. Halogen gases (Cl_2) are introduced to the chamber from one side of the hole array, and pumped from the other side. A UV grade sapphire window with >80% transmission between 250-800 nm is used atop through which the UV lights transmit and

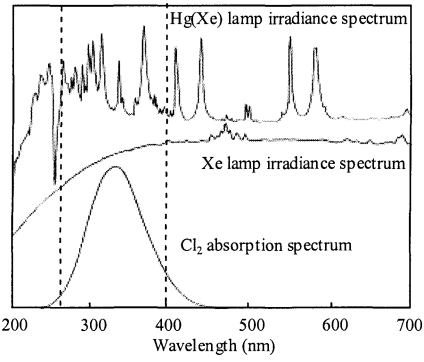


Figure 1: The radiation spectra of two UV light sources used in this work. The Cl_2 absorption spectrum is shown for comparison.

radiate the sample surface. A heating stage with a resistive heater enclosed inside hard-anodized aluminum is used to control and measure the temperature of the sample via electrical feedthroughs.

The UV light source used in this work is a 200W Xe or Hg(Xe) source. Their radiation spectra are shown in Figure 1 with the Cl_2 absorption spectrum. A monochromator is available to allow selection of nearly monochromatic light (FWHM ~15nm). Photons with energy between 250-400 nm dissociate molecular chlorine, generating atomic chlorine by two possible pathways[8]:

$$Cl_2(^1\Sigma_g^+) + h\nu \rightarrow Cl_2(^3\Pi_{o^+u}) \rightarrow Cl(^2P_{3/2}) + Cl(^2P_{1/2})$$
$$\rightarrow Cl_2(^3\Pi_{1u}) \rightarrow 2\,Cl(^2P_{3/2})$$

Two competing mechanisms on the surface would consume the generated atomic chlorine: formation of metal chloride and silicon chloride. Atomic chlorine has been demonstrated to etch silicon slowly[9,10] near room temperature since silicon chlorides are volatile. However, most of the metal chlorides are not volatile at near room temperature.[11] Therefore, mechanisms such as lift-off of metal chlorides during etching of silicon, and formation of metal-Si-Cl complexes have been proposed to explain the observed reduction of metal concentration after a UV/Cl_2 process.[12] The goal of this work is therefore to understand the mechanism by which metal is removed from the silicon surfaces.

In addition to *in situ* XPS analysis, synchrotron radiation total-reflection x-ray fluorescence (SR-TXRF) at Stanford Synchrotron Radiation Laboratory (SSRL) has been used to determine lower transition metal concentrations *ex situ*. A brief description of the synchrotron facility is included here, while the details can be found elsewhere.[13] The X-ray in SR6-2 synchrotron beamline at SSRL are focused with a platinum coated fused silica mirror, and then monochromated by two multilayers consisting of alternating layers of boron-carbide and tungsten to pass 11.1 keV radiation with a band pass of 280 eV. The beam is nearly 95% linearly polarized in the horizontal plane and impinges the vertically mounted wafer in vacuum at a grazing angle.[14] A Si(Li) detector is positioned perpendicular to the sample to minimize the scattered radiation into the detector. The minimal detection limit of most transition metals has been determined to be 3×10^8 atoms/cm^2.

To assess the effectiveness of UV/Cl_2 cleaning in removing transition metals, we chose to first investigate copper removal efficiency since copper has higher electro-negativity than silicon and easily precipitates onto silicon surfaces from a HF solution. The six-inch silicon (epi) wafers were cleaned in diluted HF (15:1 deionized water to 49% HF) to remove the native silicon dioxide and then immersed in a copper atomic absorption standard solution (1000 μg of Cu per milliliter in 5% HNO_3) for one day, rinsed with deionized water and dried with N_2. The concentrations of copper on the surface were determined by XPS and calibrated with SR-TXRF analyzed Cu-implant standards to be 10^{13}-10^{14} cm^{-2}. Note that the copper contamination levels studied here are high so that we can use XPS to quantify the copper removal efficiency. A realistic copper contamination level seen during microelectronic fabrication is on the order of

10^{11}-10^{12} cm^{-2}. As shown in Figure 5, copper appears to be either metallic or in its +1 oxidation state at a concentration level below 3×10^{13} cm^{-2} and is further oxidized to its +2 oxidation states (accompanied with the shake-up XPS satellites) at higher coverage. In fact the formation of $CuCl_2$ is thermodynamically favored in the presence of chlorine.[15] Note that the wafer surface roughness remained unchanged after the copper contamination. Some samples with extremely low concentrations of copper (below the detection limit of XPS) were studied with SR-TXRF to assess the metal removal efficiency at even lower coverages of copper.

RESULTS

The effect of substrate temperature on the cleaning efficiency with UV/Cl_2 was investigated with an initial metal contamination level of $10^{13}/cm^2$. The evolution of the Cu(2p) photoemission spectra as a function of temperature is shown after the contaminated samples were exposed to 100 mtorr Cl_2 and broad band UV radiation for ten minutes at various temperatures (Figure 2). Copper dichlorides (Cu^{+2}) were formed after UV/Cl_2 exposure, and copper removal, to the detection limit of XPS, was achieved above 110°C. The amount of copper removed from the silicon surfaces was quantified with XPS as shown in Figure 3. At the two different pressures of chlorine studied, copper removal exhibits a strong dependence on high process temperatures (~110°C), with significant surface roughening due to etching of silicon. The root-mean-square of the surface roughness changed from 1Å to 4Å between 70°C and 110°C, as shown in Figure 3. Because surface roughness at SiO_2/Si gate interface affects the charge mobility dramatically[16], we must consider surface roughness when optimizing the effectiveness of copper removal at high temperatures. However, the copper contamination levels studied here are much higher than a realistic copper contamination level during microelectronic fabrication, so that copper removal to a concentration level of 1×10^{12} cm^{-2} or below can be achieved near room temperature without increasing the surface roughness. Copper removal efficiency improves

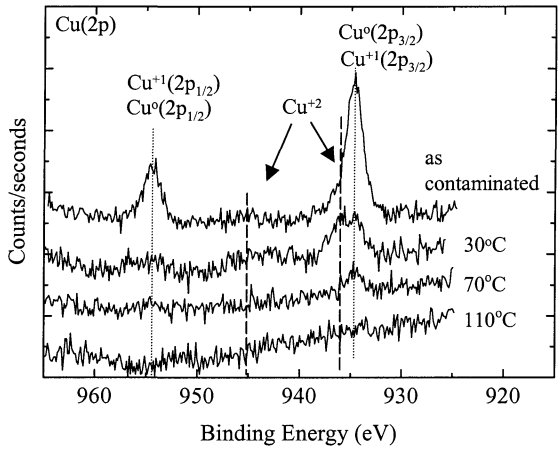
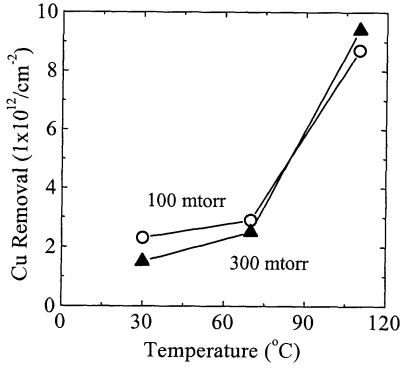


Figure 2: The amount of copper removal as a function of substrate temperature at 100mtorr Cl_2 pressure.

moderately with increased UV intensity and exposure time at temperatures near 30°C (not shown). This is attributed to the higher concentration of reactant, atomic chlorine, generated by UV radiation.



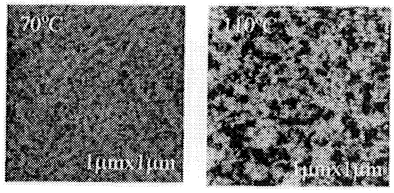


Figure 3: The concentration of copper removed from silicon surface at two chlorine pressures as a function of temperature (left). Silicon surface is significantly roughened at above 100°C, as measured by atomic force microscopy (above).

The effect of chlorine pressure is shown in Figure 4 for various temperatures. Copper removal efficiency is inversely proportional to the chlorine pressure near room temperature but independent of the chlorine pressure at higher temperatures (~110°C). Note that below XPS detection limits copper removal was observed at ~110°C, so the amount of copper removed at different pressures reflects the difference in initial copper contamination concentrations. The improved copper removal efficiency at low chlorine pressure (low concentration of reactant) can be explained by the formation of copper monochloride which has a higher vapor pressure and is likely to form trimers[17] with even higher vapor pressure than the formation copper dichloride. Moreover, copper removal was observed when the copper was first chlorinated with chlorine in the absence of UV radiation and then exposed to UV in the absence of chlorine. This suggests that UV radiation either stimulated the desorption of copper chlorides, or reduced the copper chlorides to a state (+1) which is more volatile.

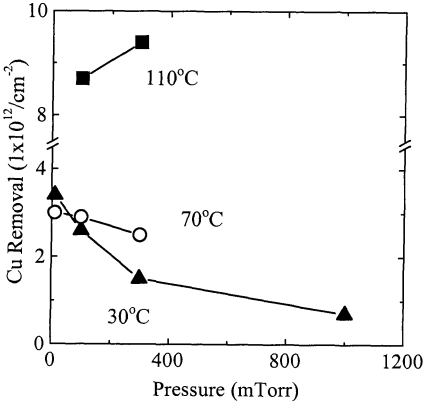
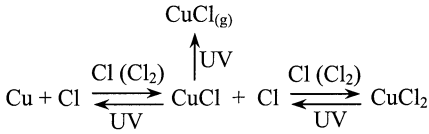


Figure 4: The concentration of copper removed from silicon surface at three substrate temperatures as a function of chlorine pressures.

A possible mechanism for metal removal has been proposed[18], where the formation of volatile copper monochloride is affected by both UV radiation and chlorine pressure:



Reduction of copper (+2) to copper (+1) or metallic copper has been observed with radiation of X-ray[19,20], electrons[21], ions[22], photons[23] (Hg lamp) or simply heating[24]. It is believed that the reduction of the copper oxidation states depends upon the wavelength (energy) of the radiating UV light.

To assess the effect of UV illumination on surface photolysis, specific wavelengths of UV radiation were selected with a monochromator to radiate the copper contaminated silicon samples. The samples were first exposed to Cl_2 under broad band UV radiation to form $CuCl_2$ on the surface, as shown in Figure 5. Subsequently the sample was exposed to 330 nm and 240 nm wavelengths light respectively. Approximately 10% of the copper was removed with no observable amount of Cu(+2) by XPS, indicating the reduction of $CuCl_2$ or its desorption stimulated by 330 nm and 240 nm UV illumination. This contrasts the previously reported results where only 240nm UV radiation caused $CuCl_2$ reduction.[7] Note that the energy provided by 240nm UV radiation is close to 5eV, which is much greater than the Cu-Cl bond strength (~3.8eV). Further experiments are underway to understand the UV wavelength dependency in copper removal. It is worth noting that no measurable amount of carbon was observed after UV/Cl_2 processing at any Cl_2 pressures and temperatures studied, making this process ideal for pre-gate oxidation cleaning to remove metal and carbonaceous contamination simultaneously.

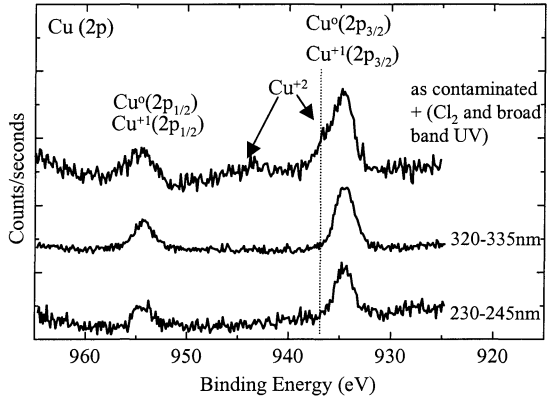


Figure 5: Cu(2p) photoemission from samples exposed to chlorine and broadband UV radiation, followed by either 320-335 nm or 230-245 nm light exposure in the absence of chlorine.

Synchrotron-TXRF has been used to quantify the metal removal efficiency at metal contamination levels more typically encountered during device fabrication ($<10^{11}/cm^2$). The results are summarized in Figure 6 showing the effect of process temperature and pressure. The copper removal efficiency increases as the chlorine pressure decreases near room temperature, but exhibits little dependence on pressure at

higher temperatures. More copper is removed at higher temperature, consistent with the results observed with XPS at higher copper coverages. These results suggest that the copper removal mechanism is likely to be applicable at very low copper coverages.

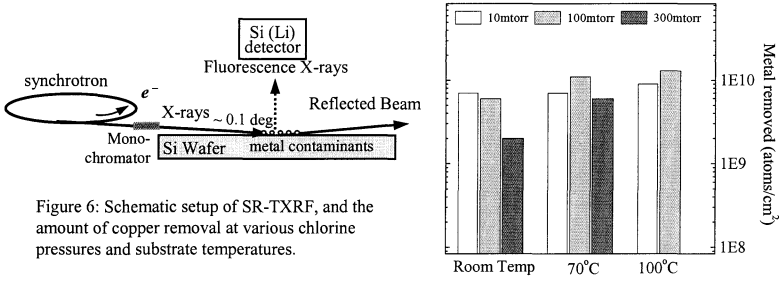


Figure 6: Schematic setup of SR-TXRF, and the amount of copper removal at various chlorine pressures and substrate temperatures.

CONCLUSION

The effect of ultraviolet (UV) light stimulated halogen chemistry on copper and carbonaceous contamination removal from silicon surfaces as a function of gas chemistries, processing pressure, temperature, and UV light intensity and wavelength. At an initial metal contamination level of $10^{13}/cm^2$, metal removal efficiency depends strongly on the processing temperature, moderately on the UV intensity and exposure time. Copper removal to the detection limit of XPS is observed at elevated temperature (~110°C) with some surface roughening due to etching of silicon. Copper removal efficiency is inversely proportional to the chlorine pressure at room temperature but independent of the chlorine pressure at higher temperatures (~110°C). Reduction of copper oxidation states is observed at specific UV wavelengths and indicates the formation of surface species with higher volatility. No significant surface roughening is observed by this process at temperatures below 70°C. Similar dependencies in copper removal on process pressure and temperature were observed at realistic metal contamination levels ($<10^{11}/cm^2$), as determined by SR-TXRF.

ACKNOWLEDGEMENTS

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THE ROLE OF OXIDE IMPURITIES IN SURFACE RESIDUE NUCLEATION DUE TO ANHYDROUS HF/METHANOL VAPOR PHASE CLEANING

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Chemical oxides on Si were etched with anhydrous HF/methanol vapor phase chemistries. Passivating oxide layers were grown with varying recipes of the RCA clean. Atomic Force Microscopy (AFM) was used to characterize the vapor etched surfaces. High densities of large residue islands were observed after vapor etching of RCA chemical and SC-1 oxides. These residue islands are distributed randomly upon the Si surface. The average island height and lateral width are 6 nm and 40 nm, respectively. Smaller residue islands were observed after vapor etching oxides grown in SC-2 solutions. The average island height and lateral width are 1.3 nm and 20 nm, respectively. Surface residue was not observed as a result of vapor etching oxides grown via dilute SC-1 solutions. These results imply that the SC-1 chemical solution (H_2O:NH_4OH:H_2O_2) may be incorporating impurities in the RCA chemical oxide, which remain on the Si surface after vapor phase cleaning. Lack of an SC-1 process appears to result in minimal surface residue.

INTRODUCTION

Surface residue islands as a result of vapor phase cleaning with HF/alcohol vapor chemistries have been observed with atomic force microscopy (AFM) (1-2). The residue islands are attributed to non-volatile impurities incorporated in the SiO_2 microstructure. The formation of residue islands is unique to oxides vapor etched with HF/alcohol chemistries. Vapor phase cleaning requires the formation of an adsorbed layer of HF and solvent (H_2O or methanol) in order for oxide etching to occur (3). For the HF/H_2O vapor chemistry, once the passivating oxide is removed the condensed layer of HF and H_2O can no longer be maintained on the surface due to surface tension effects (4). However, for the HF/methanol vapor chemistry, a condensed layer of alcohol can be maintained upon the oxide-free H-terminated Si surface (5). Due to this physical property, it has been suggested that residue island formation is initiated by the presence of an adsorbed layer of alcohol on the Si surface (2). An adsorbed alcohol layer allows interactions between alcohol molecules and nonvolatile impurity complexes. These molecular interactions are manifested through the formation of hydrogen bonds between the alcohol molecules and the electronegative element of the impurity complexes. Nitrogen impurities in the SiO_2 microstructure have been suggested as the impurity responsible for interactions leading to surface residue formation (2). Nitrogen incorporation into the SiO_2 microstructure may occur during various cleaning and processing steps.

A model has been proposed to explain the formation of the residue islands (2). The proposed mechanism for residue island nucleation is made up of 4 steps: 1) formation of

an adsorbed layer of alcohol on the Si surface, 2) hydrogen bonding between N-Si impurity complexes and alcohol molecules, 3) diffusion and interaction of the impurities, 4) nucleation and growth of the residue islands.

Given the model for residue formation we investigate methods to reduce residue island formation by decreasing the amount of nitrogen contamination incorporated into the SiO_2 passivating layer. In this study we explore using wet chemistries with minimal amounts of nitrogen in the aqueous solution. The SC-1 solution in the RCA chemical sequence consists of H_2O, H_2O_2, and NH_4OH (6), and it is suggested that NH_4OH incorporates nitrogen impurities into the SiO_2 microstructure as the passivating oxide layer is grown. Performing an HF dip between the SC-1 and SC-2 solutions should remove the chemical oxide that forms in the SC-1 solution and may reduce nitrogen contamination. This would result in the SC-2 chemistry (H_2O:HCl:H_2O_2) growing the passivating oxide layer without the N containing oxide after the SC-1 step. Another alternative is to employ a dilute SC-1 solution (50:1:1, H_2O:NH_4OH:H_2O_2). Dilute RCA chemistries are becoming more common as replacements to the original concentrations of the RCA chemistry (5:1:1) (7,8). Compared to the standard SC-1 solution, dilute SC-1 chemistries have shown comparable removal of organic contamination and particles from the Si surface (9). The use of a dilute SC-1 chemistry may reduce the amount of nitrogen contamination incorporated into the SiO_2 layer, while still removing organic and particle contamination.

In this study we investigate vapor phase cleaning employing anhydrous HF/methanol vapor phase chemistries for the removal of oxides grown with alternative RCA chemistries. We observe differences in the size and density of the surface residue by changing the passivating oxide preparation chemistry. Atomic force microscopy is used to observe and characterize surface morphology as a result of vapor phase cleaning.

EXPERIMENTAL

In this study 4-inch diameter p-type Si (100) wafers were used. Passivating oxides were grown on the substrates prior to the vapor phase cleaning process. The passivating oxides were grown by alternative RCA cleaning chemistries (Table 1). In order to remove the native oxide, out of the box wafers experienced a 2% HF dip followed by a 2 min DI H_2O rinse prior to chemical oxide growth. Wet chemical treatments grew ~ 1.5 nm thick oxides, as measured by ellipsometry. Each step consisted of a 5 min dip in each chemical followed by a 5 min DI rinse. There were two control surfaces in this study. The control surfaces experienced a standard RCA clean: SC-1 (5:1:1) + SC-2 (5:1:1) at 70 °C. Following oxide growth, one control surface experienced a 30 sec HF dip and one control surface experienced a 5 min vapor etch at 25 Torr.

After passivating oxides were grown, the wafers were loaded into a loadlock connected to a 6-port single wafer processing clustertool. The loadlock pumped to ~ $5x10^{-6}$ Torr prior to transfer into the waferhandler. The waferhandler base pressure was ~ $6x10^{-8}$ Torr.

Table 1. Modified RCA wet chemical cleaning processes used as alternative recipes for the formation of passivating oxides on Si surfaces.

A	SC-1 5:1:1 (H_2O:NH_4OH:H_2O_2) @ 70 °C
B	SC-2 5:1:1 (H_2O:HCl:H_2O_2) @ 70 °C
C	SC-1 + 30 sec HF dip + SC-2 @ 70 °C
D	Dilute SC-1 (50:1:1) @ 70 °C
E	Dilute SC-1 (50:1:1) + SC-2 (5:1:1) @ 70 °C

Vapor phase cleaning was accomplished in a system based on an Advantage 2000 system donated by Genus Corporation. The system has been modified to be high vacuum compatible and to handle the chemistries employed in this study. The chamber is a single wafer stainless steel chamber with a SiC dome. The system employs anhydrous hydrogen fluoride (AHF) delivered from a gas cylinder and methanol vapor vacuum evaporated from a teflon coated stainless steel sampling cylinder. The AHF gas flow range is from 0 to 500 sccm and is controlled by a mass flow controller (MFC). The methanol gas flow range is from 0 to 67 sccm. Nitrogen was used to establish the desired process pressures and was used to purge the system prior to wafer transfer. Nitrogen flow range is from 0 to 1 SLM controlled by an MFC. Process gases are delivered via a teflon injector into the process chamber. The process pressure is regulated using a downstream throttle valve and is measured by a baratron gauge. System base pressure is ~ $2x10^{-7}$ Torr and wafer transfer pressure is typically $3x10^{-6}$ Torr. The wafer sits horizontally, face up, in the process chamber and etching occurs at ambient temperature (~ 22 °C) with process pressures ranging from 0.5-100 Torr. In this study, wafers were vapor cleaned at 25 Torr for 5 minutes.

After the wafers were processed they were transferred out of the cluster-integrated vapor cleaning system and examined with atomic force microscopy. A Park Scientific atomic force microscope, in contact mode, was employed to measure surface roughness and used to study the surface morphology. Typical scan sizes used to characterize the cleaned surfaces were 2 x 2 μm^2 with 256 x 256 data points. Scans were performed in the center and edge of each wafer. Silicon nitride tips with a 4.1 N force constant were used for surface scanning. The lateral resolution of the AFM is ~ 1-2 nm. The vertical resolution of the AFM is sub-nm. Long range surface variations were removed from the images using a 2nd order polynomial fit. The Root Mean Square (RMS) roughness values were then calculated for each of the scanned surfaces. Accuracy of the RMS roughness values is ± 0.05 nm.

RESULTS AND DISCUSSION

The results of anhydrous HF/methanol vapor phase etching of oxides grown with the RCA chemistry and alternative preparation chemistries are summarized in Table 2.

Residue island formation was observed as a result of vapor etching RCA chemical oxides and SC-1 oxides (Fig. 1). Residue island dimensions and density are comparable for etching RCA and SC-1 chemical oxides. For both oxides, the average residue island height and lateral dimension are 6.0 nm and 40 nm, respectively, and the RMS roughness values are ~ 0.75 nm. The RMS roughness values excluding the surface residue are ~ 0.25 nm. Smaller residue islands are observed as a result of vapor etching passivating oxides grown in SC-2 solutions (Fig. 2). The observed residue is only on the order of 1.0-2.0 nm in height and 15-20 nm in lateral dimension. The RMS roughness values for these surfaces range from 0.11-0.14 nm. Residue islands are not observed as a result of vapor etching oxides prepared via dilute SC-1 (50:1:1) solutions (Fig. 3). The RMS roughness values for these surfaces range from 0.10-0.12 nm. The RMS roughness value for an HF dipped surface is ~ 0.11 nm.

Table 2. Process parameters, residue island density, average residue dimensions, residue height range, and RMS values for chemical oxides vapor etched at 25 Torr for 5 minutes.

Preparation Chemistry	Residue Density (island #/4μm^2)	Average Residue Dimensions lateral/height	Range of island height	RMS Roughness
SC-1 + SC-2 "RCA Clean"	90	35 nm / 6.1 nm	4.0-8.0 nm	0.69 nm
SC-1	80	40 nm / 6.0 nm	4.0-7.9 nm	0.79 nm
SC-2	58	20 nm / 1.5 nm	1.0-2.0 nm	0.11 nm
SC-1 + HF dip + SC-2	34	15 nm / 1.1 nm	0.8-1.4 nm	0.14 nm
Dilute SC-1	n/a	n/a	n/a	0.10 nm
Dilute SC-1 + SC-2	n/a	n/a	n/a	0.12 nm

The different oxide preparation chemistries have shown a significant effect on residue island formation. Vapor etching passivating oxides grown in 5:1:1 SC-1 solutions resulted in a high density of residue islands. Vapor etching passivating oxides grown in 5:1:1 SC-2 solutions resulted in a reduced amount of surface residue. Vapor etching passivating oxides grown in 50:1:1 SC-1 solutions did not appear to result in surface residue.

Previous research from our group attributes the formation of surface residue islands to the presence of nitrogen impurities in the oxides (2). Based on this, the absence of large residue islands in the vapor etched SC-2 and dilute SC-1 oxides compared to the RCA and SC-1 oxides may be attributed to a reduction in nitrogen contamination in the passivating oxide layers. The AFM results showing residue island formation indicate that the SC-1 chemical solution incorporates N defects into the SiO_2 microstructure as the Si surface is chemically oxidized. Because the SC-2 solution does not etch SiO_2 nitrogen

contamination is not removed with the immersion of the SC-1 oxide into the SC-2 solution. In contrast, if an SC-2 oxide were immersed into an SC-1 solution, SiO_2 etching (due to NH_4OH) and regrowth (due to H_2O_2) is expected to occur (10). In this case the regrown oxide would likely be contaminated with N due to the NH_4OH component of the SC-1 solution. These results indicate that nitrogen contamination in the oxide may be increased or decreased by varying the concentration of NH_4OH in the SC-1 chemical solution.

The smaller residue islands observed after vapor etching an SC-2 oxide may be due to N contamination in the oxide. However, this is not likely since vapor etching oxides grown in the dilute SC-1 chemistry result in residue-free surfaces. The SC-2 chemistry is not designed to remove organic contamination from the Si surface, whereas the SC-1 chemistry is designed to remove organic contamination. In this case, the surface residue may be due to organic contamination, which remained on the Si surface prior to oxide growth in the SC-2 solution. It is observed that the surface that experienced the SC-1 and HF dip prior to the SC-2 solution resulted in a reduced density of surface residue compared to the SC-2 only surface. Vapor etching an oxide surface grown in the dilute SC-1 + SC-2 chemistry results in residue-free surfaces. In this case, the use of the dilute SC-1 chemistry is necessary to remove organic contamination prior to the vapor etch.

Manipulation of the RCA chemistry provides options for the preparation of passivating oxide layers with reduced nitrogen contamination. An HF dip between the SC-1 and SC-2 steps results in reduced residue formation. If this is not desirable, then the employment of a dilute SC-1 solution in place of the standard SC-1 concentration is an option. Vapor etching dilute SC-1 and dilute RCA chemical oxides resulted in residue-free surfaces. It should be noted that the use of dilute RCA chemistries is often employed for the pre-gate oxidation clean (7,8,11-13).

CONCLUSIONS

The formation of residue islands is observed for HF vapor phase etching of chemically oxidized Si surfaces. Different oxide preparation chemistries have shown a significant effect on residue island formation. It was observed that residue island density and size were comparable after vapor etching RCA and SC-1 chemical oxides. Vapor etching passivating oxides grown with an SC-2 solution results in minimal surface residue. Vapor etching oxides grown with a dilute SC-1 solution does not result in observable surface residue. These results further support the hypothesis that N contamination in SiO_2 is the impurity which leads to residue island formation. It is suggested that N contamination is incorporated into the oxide due to NH_4OH in the SC-1 chemistry. Growing wet chemical oxides in an SC-2, a dilute SC-1, or a dilute RCA chemistry significantly reduces the amount of N contamination in the oxide. Manipulation of the RCA chemistry provides options to prepare passivating oxide layers that will not result in surface residue formation due to HF/methanol vapor phase cleaning.

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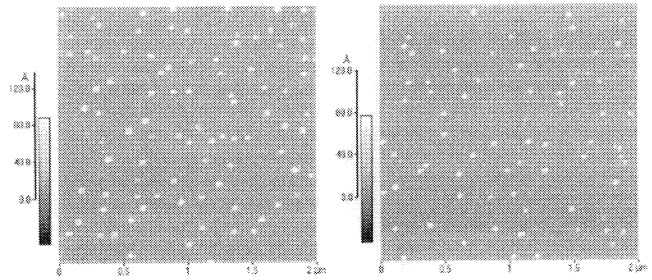
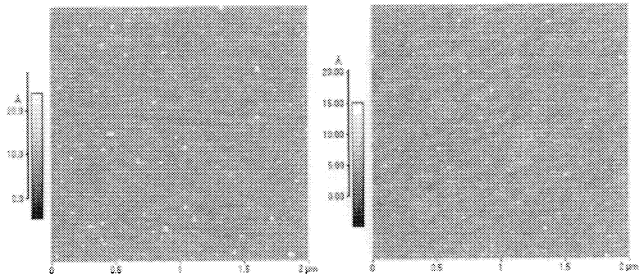


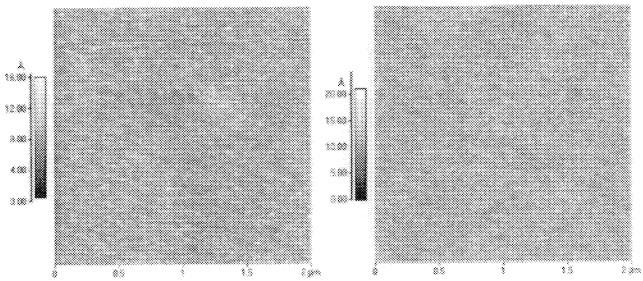
(a) (b)

Figure 1. AFM images displaying surface residue as a result of vapor etching a) RCA chemical oxides, and b) SC1 chemical oxides.



(a) (b)

Figure 2. AFM images displaying surface morphology as a result of vapor etching chemical oxides grown via a) SC-1 + HF dip + SC-2 and b) SC-2.



(a) (b)

Figure 3. AFM images displaying surface morphology as a result of vapor etching chemical oxides grown via a) dilute SC-1 and b) dilute SC-1 + SC-2.

LOW-TEMPERATURE ATMOSPHERIC AMBIENT RAPID LAMP CLEANING OF SILICON SURFACES

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This experiment is concerned with control of organic contaminants accumulated on the silicon surface during wafer storage using white light illumination from a halogen lamp in ambient air. The results obtained using TOF-SIMS, contact angle and surface charge measurements indicate effective removal of surface organic contaminants using this treatment. The effectiveness of this method was demonstrated to be comparable to UV/oxygen exposure and thermal annealing using a hot plate.

INTRODUCTION

Surface contaminants encountered in microelectronics manufacturing can be considered in terms of those added to the surface during processing and those added during wafer storage. The first group concerns contaminants originating from the process gases, chemicals, and equipment and includes organic and metallic contaminants as well as particles and moisture. The second group concerns contaminants from the storage and shipping environment including clean room air, containers, boxes, and cassettes. Assuming storage is taking place in a particle-free environment the contaminants originating from storage include primarily organic contaminants (1) and moisture (2). Hence, these two can be considered to be key contributors to the surface aging process, which may then interfere with subsequent processes or measurements such as ellipsometric measurements as well as non-contact measurements of electrical characteristics of the surface (3). It appears that at present the most common solution to the problem of surface deposits accumulated during wafer shipment and/or prolonged storage is a surface cleaning using standard wet chemistries. This routine is time and resource consuming and as such should be replaced with simpler and less involving methods of surface refreshing. Alternative approaches considered include the use of ozonated deionized water (1), UV/O_2 exposure or low temperature annealing in an oxidizing ambient all of which also include dedicated equipment and add considerable time to the manufacturing sequence.

The goal of this study was to investigate the effect of a photo-thermal treatment in an air ambient on the Si surface using a laboratory version of a commercial Rapid Optical Surface Treatment (ROST) system (4). The focus of this investigation is on the monitoring of changes in organic contaminants coverage of the Si surface resulting from this treatment following wafer storage in plastic boxes as well as in clean room air.

EXPERIMENTAL

The silicon wafers in this experiment were p-type, (100), with resistivity of 1-10 ohm-cm. The ROST system used in this study is a laboratory version of a commercial system. It includes a single 600 watt halogen lamp to which the wafer surface is exposed in an enclosed chamber in the ambient air (Fig. 1). The closed loop wafer temperature control system allows pre-setting the wafer temperature up to 300 °C. In this experiment the time of exposure did not exceed 120 seconds. Silicon wafers subjected to the lamp treatment were either as received from the manufacturer in plastic boxes or wafers taken out of the box and stored for a prolonged period of time in clean room air. In both cases fully hydrophylic surfaces were expected. This treatment was compared with two other methods of organic removal. The first method consisted of a hot plate anneal in the ambient air at 300 °C for 5 min., while the second involved a 5 min. exposure in a UV reactor, also in ambient air.

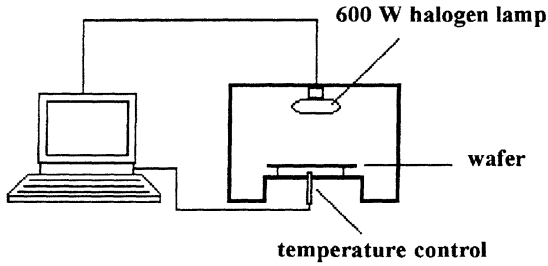

Figure 1 Schematic of the ROST system.

Characterization techniques employed in this study included non-contact measurements of electrical characteristics of the Si surface using the SPV-based Surface Charge Profiling (SCP) method. In earlier studies this method did demonstrate high sensitivity to the varying conditions of Si surfaces resulting from cleaning (5, 6). Furthermore, static SIMS and TOF-SIMS (Time-of-Flight Secondary Ion Mass Spectroscopy) were used to evaluate the effect of the ROST process. The bulk of the results of this investigation were obtained using contact angle measurements. Following cross referencing of SCP and TOF-SIMS results with the results of contact angle measurements this last method was determined to be an effective indicator of the presence of organic contaminants on the hydrophylic surfaces.

RESULTS AND DISCUSSION

The lamp's setting was selected to heat the Si surfaces at 300 °C for various times. Initially evaluation of the ROST treatment was carried out by means of surface charge measurements using the SCP method. It was demonstrated earlier that the prolonged storage of Si wafers in shipping boxes as well as in clean room air results in the addition of negative charge to the Si surface (5). Organic contaminants are believed to add negative charge to the surface while a clean, hydrophylic surface typically features a high positive

charge (5). As seen in Fig. 2 the density of surface charge increases as a function of ROST time which may be interpreted in terms of the removal of negative charge from otherwise positively charged Si surfaces and taken as an indication of effective volatilization of organic contaminants accumulated on the Si surface during storage.

A silicon surface, which is covered with an oxide and free from organic contaminants typically features a low wetting angle. A departure from this condition is observed as a result of wafer storage, and this can be attributed to surface contamination with organic contaminants, mainly hydrocarbons. Measurements of contact angle should therefore provide a reliable measure of the degree of surface coverage with organic contaminants following the ROST treatment. Figure 3 shows variation of the contact angle as a function of time of the lamp exposure at 300 °C for wafers stored in a box and wafers stored in the clean room air. As seen in this figure an approximately 60 sec. exposure is sufficient to get the contact angle to the value expected for a clean oxide-covered Si surface. For exposures longer than this a contact angle value < 5° is established

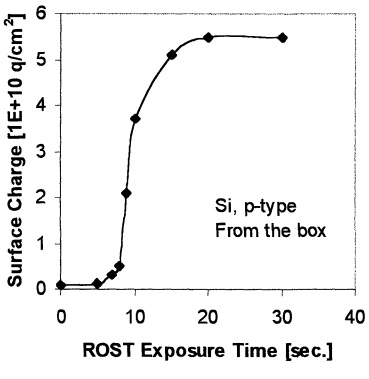

Figure 2 Surface charge vs ROST exposure time at 300 °C.

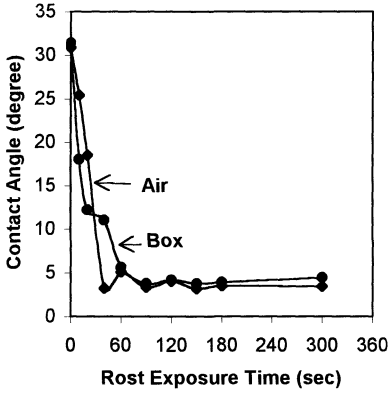

Figure 3 Contact angle vs ROST exposure time at 300 °C on wafers stored in a shipping box or clean room air.

which is an indication of an organic-free hydrophylic Si surface.

In order to confirm contact angle measurements the results of a 60 sec ROST exposure were studied by means of TOF-SIMS, which is considered to be an adequate tool for the detection of hydrocarbons on Si surfaces. The measurements were performed on wafers stored in clean room air one of which received a 60 sec ROST exposure. Figure 4a shows the resulting changes in the amounts of accumulation on the Si surface of three common organic contaminants. In all three cases a significant decrease in surface concentration is noted confirming contact angle results that suggested organic volatilization resulting from the ROST process. In contrast to organics, however, a 60 sec ROST exposure does not seem to have an effect on the surface moisture represented by Si-OH and Si-H groups (Fig. 4b). No clear trend was observed in this case confirming the results of static SIMS characterization also carried out in this investigation. Our previous

studies indicate that in the temperature range used in this process significantly longer times are needed to reduce the concentration of moisture physisorbed on hydrophylic Si surfaces while the chemisorbed moisture cannot be completely removed from these surfaces

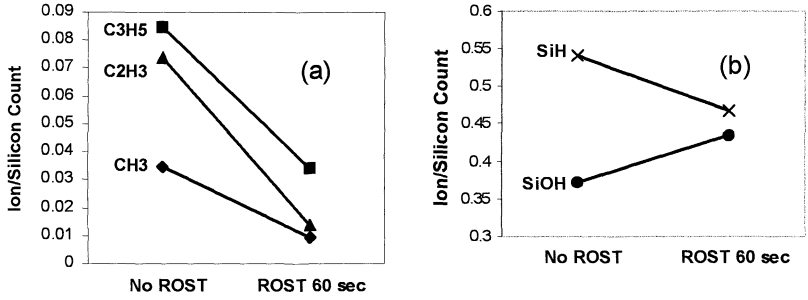

Figure 4 TOF-SIMS results for surfaces with and without 60 sec ROST process.

without etching of the native oxide (2). One should also consider the possibility that hydrogen resulting from organics volatilization reacts with ambient oxygen adding to surface moisture.

In order to further confirm the ROST's ability to volatize organic contaminants experiments with Si surfaces purposely contaminated with organics by immersion in Iso-Propyl Alcohol (IPA) were performed. Figure 5 shows values of contact angle following various surface treatments. The increase in contact angle following a 3 minutes long immersion in IPA indicates the addition of organic contamination to the surface while a subsequent ROST reduces it again to the level expected for a clean hydrophylic surface. This confirms the correlation of the contact angle with the level of surface organics coverage the the removal of the organics due to the ROST treatment.

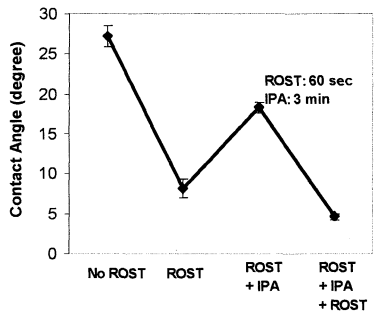

Figure 5 Contact angle results before and after ROST, IPA immersion and subsequent ROST.

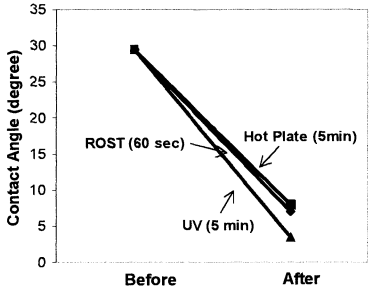

Figure 6 Contact angle results after ROST, hot plate anneal or UV/Cl exposure.

In the final stage of this experiment a comparison of the ROST with two other methods of organic removal was carried out. The first method consisted of a hot plate anneal in the ambient air at 300 °C for 5 min., while the second involved a 5 min. exposure in a UV reactor, also in ambient air (7). As shown in Fig. 6 the three methods caused a similar decrease in the contact angle, which indicates similar organics removal efficiency for these methods. The problem with the hot plate treatment, however, is that by heating the back surface of the wafer it requires additional time to accomplish volatilization of hydrocarbons on the front surface. The UV treatment also has its limitations as it does not only require a 5 min. long treatment, but also must be performed in a vented enclosure due to ozone generation. In this context ROST seems to offer the quickest and easiest to implement approach to organic contaminants removal.

SUMMARY

The experiments carried out in this investigation demonstrated that a 60 sec Rapid Optical Surface Treatment (ROST) using a halogen lamp in ambient air is effective in removing hydrocarbons from Si surfaces that likely were deposited during wafer storage. The organics removal efficiency of this treatment is comparable to other treatments that require additional time and/or equipment. This indicates that the surfaces of Si wafers stored for an extended period of time in shipping boxes can be returned to their starting condition as a result of a brief ROST exposure.

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Characterization of Co Contamination on Si Surfaces with relevance to Co Silicides

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ABSTRACT

For the evaluation of Co contamination and its removal in fab environments, Co contamination behaviors on Si wafers were characterized. Through this work, it was found that (1) high levels of Co contamination on oxide and nitride wafers occurs from SC1 solutions containing Co rather than from SC2 or DI water, (2) for RCA cleaned wafers, the removal of Co contamination may be achieved using dilute HCl solutions, while for oxide and nitride wafers, cleaning using SC1-SC2 solutions removed Co below a level of $1x10^{10}$ atoms/cm^2, (3) the dissolution of Co silicide in SC1 and SC2 solutions is extremely low and hence Co contamination due to silicide dissolution in cleaning solutions should not be a factor, and (4) the dissolution of Co film in SC2 solutions is almost complete within 5 minutes, but in SC1 solutions, Co films dissolve slowly. It was also found that adsorption of Co species is capable of reversing the zeta potential, and Co contamination affects oxide quality through the degradation of lifetime.

1. INTRODUCTION

Before any new materials are introduced into the wafer fab, a cross-contamination is always one of great concerns. For example, a Co silicide has been widely investigated to integrate in microelectronic devices [1]. Co, one of the fast diffusing transition elements can be treated as a harmful metallic contaminant such as a Cu or Ni to cause the degradation of device performances. However, there are no clear data addressing Co contamination behaviors on Si wafers upon wafers are exposed to Co contaminated environments and Co contaminant removing techniques using solutions available in fab areas. To obtain information for these fundamental issues, the characterization work for Co contamination and Co removal was carried out. In the Co silicide process, the Co that does not react with Si during the RTA process is removed by a wet etch step. Co, when dissolved as an aqueous specie, may adsorb on the field oxide and/or the nitride spacer around the silicide contact area. Also, there is a concern about a cross contamination of Co by unexpected processing or introduction of Co wafers into Co restricted areas.

The objective of the present work was to understand the fundamental nature of interaction of aqueous cobalt species in SC1 and SC2 solutions with oxide, nitride, and

RCA cleaned wafer surfaces and to suggest strategies to remove cobalt contaminants on surfaces. In this work, 5 different areas were focussed: (1) the amount of Co deposited on Si wafers, (2) cleaning methods using chemicals available in the fab such as RCA solutions to remove Co contaminants from Si surfaces, (3) the amount of dissolution of Co from Co film and Co silicide film in aqueous solutions, (4) the electrokinetic behaviors of Co contaminants, and (5) the effect of Co contamination on carrier lifetime.

2. EXPERIMENTAL PROCEDURES

Most of the experiments were conducted on oxide wafers (1000 Å), nitride wafers (920 Å), and RCA cleaned Si wafers. Co contamination on wafer surfaces was performed by immersing wafer samples in a quartz bath containing Co at a predetermined temperature (29±2 or 52±2 °C). After contamination, wafer samples were rinsed in overflow DI water until the resistivity reached ≥17 MΩ-cm, and the Co surface concentration on Si surfaces was measured using a TXRF technique. For Co removal evaluation, several cleaning recipes based on individual cleaning step or combination of cleaning steps using dilute HF, SC1 or SC2 solution (1:4:20) were applied at 29 or 55 °C. For the measurement of the rate of Co dissolution in aqueous solutions (SC1, SC2 or DI water), 300 Å thick Co deposited wafers and Co silicide wafers (150A Co/80A Ti deposition – RTA1-Selective Etch-RTA2 process) were used. After immersing wafers in solutions, liquid samples were collected as a function of immersion time and analyzed by ICP-MS. The zeta potential measurement of oxide wafer samples in the presence of cobalt ions was carried out using a Brookhaven-Paar streaming potential analyzer with a specially designed cell. For streaming potential measurements, a narrow flow channel was created between two wafer samples, separated by a PTFE gasket. The streaming potential was measured using two platinum electrodes. For the measurement of carrier lifetime, a commercially available non-contact analyzer was used for ~40Å thick thermal oxide wafers prepared after contamination intentionally. For the comparative works, Fe and Ni contaminated oxide wafers were also prepared.

3. RESULTS AND DISCUSSION

The Co contamination tests on oxide, nitride, and RCA cleaned wafers in SC1 maintained at 29 ^{0}C were conducted, and the results are shown in Fig. 1. In these tests, an immersion time of 5 min was used, and the wafers were spin dried after DI rinse. In the entire concentration range of 0.1 to 50 ppm, the RCA cleaned wafers suffered the least amount of contamination less than $1x10^{12}$ atoms/cm^2. The contamination levels on oxide were higher than those on the nitride wafers under identical conditions. Cobalt contamination followed the order, Oxide> Nitride>RCA cleaned wafers.

The effect of increasing the temperature of the SC1 bath to 52 ^{0}C on Co contamination is shown in Fig. 2. The wafers were rinsed and dried after contamination experiments. Increase of solution temperature appeared to decrease the cobalt contamination on thermal oxide and nitride surfaces. Even at the elevated temperature, the level of contamination on RCA cleaned surfaces was significantly lower than that on

oxide and nitride surfaces, at 5 ppm of Co concentration. However, at a low Co concentration (i.e., 0.5 ppm), the difference in Co surface concentration was not clear as found for high Co concentrations.

The next series of tests were focussed on the determination of Co contamination from SC2 solutions. In Fig. 3, Co contamination on different types of wafers is plotted as a function of solution Co concentration at 29 °C. Co contamination on nitride surfaces was below the detection limit. On both thermal oxide and RCA cleaned surfaces, Co levels were only in the 10^{10} atoms/cm^2 level, much lower than what was measured in SC1 solutions. The effect of temperature on contamination was also studied for 10 ppm Co solutions and the results are also plotted in Fig. 3. Even at the higher temperature of 52 °C, Co contamination on all the surfaces remained very low. The contamination of Co from DI water was also carried out for oxide and nitride wafers. As shown in Fig. 4, Co contaminations less than ~$6x10^{10}$ atoms/cm^2 were found on all Si wafers contaminated in DI water containing less than 10 ppm. These values were very similar values as those for wafers contaminated in SC2 solutions. However, these values were much less than those for wafers contaminated in SC1 solutions.

The difference in Co contamination from SC1 and SC2 solutions can perhaps be explained by the nature of Co species present in acidic SC2 and alkaline SC1 solutions. In SC2 and DI water, Co should be present in the form of Co^{++}, whereas in SC1 solutions, Co should be present as $Co(NH_3)_6^{++}$, Co_3O_4 or $Co(OH)_2$ species depending on pH values of solutions. This can be seen from *Eh-pH* (Pourbaix) diagram prepared under conditions of 10^{-4} and 1 mole/l of Co and NH_3 at 50 °C for Co as shown in Fig. 5. In the case of hydrolyzable metal ions such as Co^{++} and Fe^{+++}, it is well known that their adsorption on SiO_2 is very pH dependent and sharply increases near a solution pH where the ions begin to hydrolyze.

The adsorption behavior of Co can be understood from the electrokinetic properties of oxide wafers in the presence of dissolved Co in solutions. The electrokinetic characteristics (zeta potential) of oxide wafers are displayed in Fig. 6 as a function of solution pH in the presence of Co (5 ppm) in solution. It may be discerned from this figure that the isoelectric point (IEP) of oxide wafer occurs at a solution pH of approximately 3.5 in the absence of any cobalt in solution. The presence of cobalt in solution affected the zeta potential of SiO_2 at solution pH values greater than 4. In the presence of dissolved Co in solution, two points of zeta potential reversals (change in sign of zeta potential) occurred, one at pH close to 3.5 and the other at a pH of approximately 8.5. These data indicate that cobalt adsorbs on silicon dioxide when its zeta potential is negative and the adsorbed cobalt forms an insoluble surface hydroxide at alkaline pH values. As may be seen from the Eh-pH diagram, Co added to the solution can be in the ionic or solid form depending on the pH and the presence of ammonia. Since the surface concentration of Co under these conditions is only of the order of 10^{12} atoms/cm^2, the formation of cobalt hydroxide on the surface is most likely to be very patchy.

The kinetics of Co contamination of surfaces from SC1 solutions containing 1 ppm of Co was investigated at 29 and 52 °C. At 29 °C, contamination on nitride and RCA cleaned wafer surfaces occurred rapidly and reached a limiting value within five minutes. On oxide wafer surfaces, contamination peaked out around five minutes but decreased slowly at long contact times. The adsorption kinetics data obtained at 52 ^{0}C as shown in Fig. 7 indicate that contamination on nitride and chemical oxide surfaces decreases slowly from a peak value when immersion time is increased. The time dependence of Co uptake from SC1 solutions may be explained as due to two competing processes, adsorption of Co complex such as a $Co(NH_3)_6^{++}$ and removal of adsorbed Co due to the etching of the oxide in SC1. In electrochemical investigations of Fe uptake by silicon in SC1 solutions, such a "peaking out" of mixed potentials has been observed [2].

As mentioned above, very low levels of Co contamination was occurred in acidic solutions. Thus, Co contaminated wafer samples for cleaning experiments were prepared by immersing the wafers in SC1 solutions containing 10 ppm of Co for 5 min. The removal of Co contamination from wafer surfaces was attempted in dilute HCl solutions (1:5 and 1:50 $HCl:H_2O$) and in SC2 solutions (1:1:5 and 1:1:50 $HCl:H_2O_2:H_2O$) maintained at 29 °C. Cleaning experiments were also performed using dilute HF and combined solutions of SC1 and SC2 solutions at 55 °C as shown in Table 1. From the results of the cleaning experiments carried out in dilute HCl solutions, two conclusions can be drawn: (1) 1:50 HCl solution is almost as effective as 1:5 HCl solution, and Co levels on RCA cleaned surfaces can be reduced from ~ 10^{11} atoms/cm^2 to below detection limit. (2) Cleaning with HCl solutions cannot remove Co on oxide and nitride wafers to detection limit as on RCA cleaned wafers. Co levels on oxide and nitride can be reduced from ~100x10^{10} atoms/cm^2 to levels of ~ 10^{10} atoms/cm^2. Fig. 8 shows the cleaning results for Co contaminated wafers with SC2 solutions. There does not appear to be any significant additional advantage in using SC2 solutions in place of dilute HCl solutions. This is understandable from the Pourbaix diagram for cobalt-ammonia-water system (Fig. 5) which shows that at pH values below 4, Co^{++} ions are the dominant species in solutions. For the complete removal of Co from oxide and nitride surfaces, cleaning experiments based on high temperature (55°C) of SC2 (1:1:5) solutions were performed. The results are shown in Fig. 8. It may be seen from this figure that no beneficial effect was found for 1:1:5 SC2 in removing Co. To remove Co with slight etching of wafer surface, wafers were cleaned with a serial cleaning with SC1 and SC2 with and without a dilute HF (100:1 for 20 sec) step. The results are also shown in Fig. 8. Wafers cleaned with SC1-SC2 showed residual Co levels less than 1x10^{10} atoms/cm^2 of Co. In the case of wafers cleaned with dil HF-SC1-SC2, Co contaminant below a detection limit was measured.

Co levels in solutions will depend on the extent of dissolution of Co and Co silicide in SC1 and SC2 solutions during processing. Hence, the kinetics of dissolution of Co and Co silicide films was investigated in SC1 and SC2 solutions at 25 ^{0}C using Co deposited wafers and Co silicide wafers. In these experiments, 2 wafers were conditioned in 4.2 liter of SC1 or SC2 solutions, and the amount of Co dissolved in solutions were measured as a function of time. In the case of Co silicide wafers, no measurable dissolution of Co silicide occurred in these solutions. The kinetics of dissolution of Co from Co deposited wafers is presented in Fig. 9. In SC2 solutions, complete dissolution

of Co, which would correspond to ~ 800 ppb in solution under the solid/liquid ratio used in the experiments, occurred. In SC1 solutions, Co dissolution occurred slowly and only 20% was dissolved after 20 minutes of contact with the solution.

Fig. 10 shows bulk recombination lifetime of 40Å thick oxide wafers with or without contamination of metallic contaminants. It may be seen from this figure that Co contaminant significantly reduced recombination time as Fe contaminant. A similar trend was also found for Ni contaminated oxide wafers.

Table 1, Cleaning recipes used for Co removals from Si wafers

Cleaning Recipes	Cleaning Sequences	Remarks
1:50 HCl at 29C	only dilute HCl (1:50)	at 29 °C
1:5 HCl at 29C	only dilute HCl (1:5)	at 29 °C
1:1:50 SC1 at 29C	only dilute SC2 (1:1:50)	at 29 °C
1:1:5 SC1 at 29C	only SC2 (1:1:5)	at 29 °C
1:1:5 SC1	only SC2 (1:1:5)	at 55 °C
SC1-SC2	SC1 (1:1:5) - SC2 (1:1:5)	at 55 °C
Dil HF-SC1-SC2	HF (100:1)-SC1 (1:1:5) – SC2 (1:1:5)	HF at 25°C, and SC1 and SC2 at 55 °C
Dil HF	only HF (100:1)	at 25°C

4. SUMMARY

Based on the results of this work, the following conclusions can be made:

(i) Co contamination of oxide and nitride wafers occurred from ammoniacal solutions such as SC1 solutions containing Co; under identical solution conditions, the extent of contamination followed the order, oxide>nitride>RCA cleaned surfaces

(ii) Co contamination occurred rapidly for all 3 different surfaces.

(iii) The removal of Co contamination from RCA cleaned wafer may be achieved using dilute HCl solutions; the use of SC2 instead of dilute HCl did not offer any significant advantages.

(iv) Cleaning using SC1-SC2 solutions removed Co on oxide and nitride wafers below a level of $1x10^{10}$ atoms/cm^2.

(v) Electrokinetic data indicated that adsorption of dissolved cobalt species was capable of reversing the zeta potential of thermal oxide. This behavior can be understood from Eh-pH diagram of Co in the presence of NH_4OH.

(vi) The dissolution of cobalt silicide in SC1 and SC2 solutions was extremely low and hence Co contamination due to silicide dissolution in cleaning solutions should not be a factor.

(vii) The dissolution of Co film in SC2 solutions was almost complete within five minutes, but in SC1 solutions, Co films dissolved slowly; Co contamination during the removal of Co films was likely to occur in ammoniacal solutions

(viii) Co contamination affected oxide quality by the degradation of carrier lifetime.

ACKNOWLEDGEMENT:

I would like to acknowledge Cynthia Gonsalves for her invaluable TXRF works and would like to extend my thanks to Paul Besser and Franklin Crawford for the preparation of wafers used for this work.

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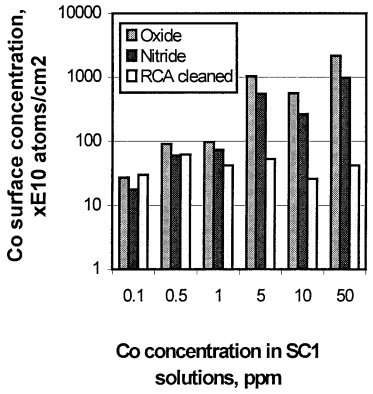

Fig. 1, Co contamination levels on oxide, nitride and RCA cleaned wafers in Co containing SC1 solutions.

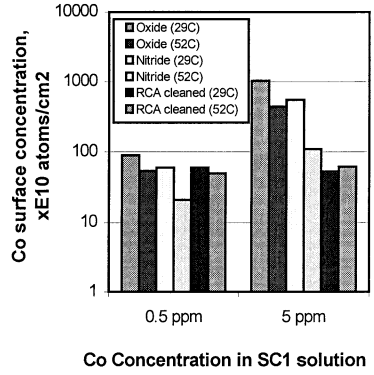

Fig. 2, Co contamination levels on oxide, nitride and RCA cleaned wafers in Co containing SC1 solutions at two different solution temperatures.

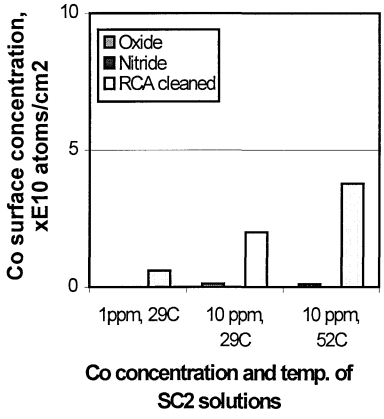

Fig. 3, Co contamination levels on oxide, nitride and RCA cleaned wafers in Co containing SC2 solutions at two different solution temperatures.

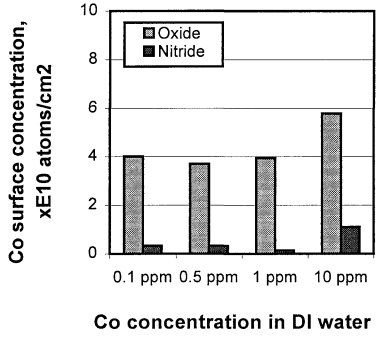

Fig. 4, Co contamination levels on oxide and nitride wafers in Co containing DI water.

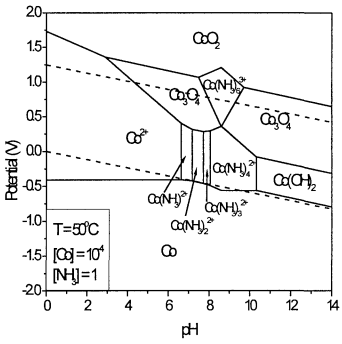

Fig. 5, Eh-pH diagram of Co.

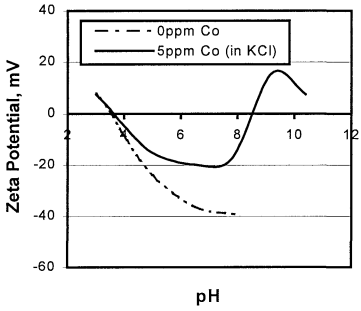

Fig. 6, Elctrokinetic behaviors of oxide wafers with and without addition of Co.

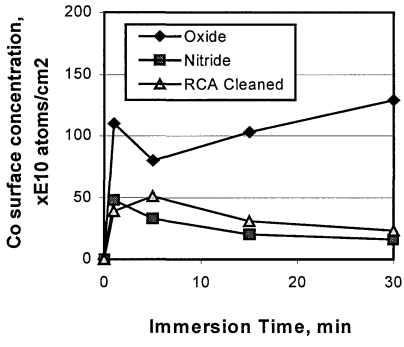

Fig. 7, Co contamination on oxide, nitride and RCA cleaned wafers as a function of time at 52 °C.

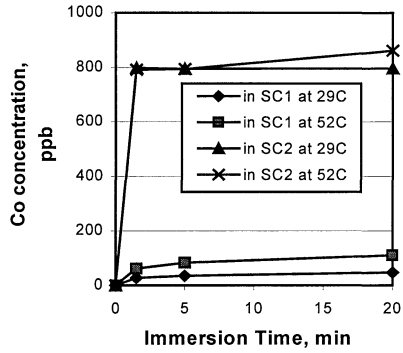

Fig. 9, Co concentration dissolved from Co films in SC1 and SC2 solutions as a function of immersion time at 2 different temperatures.

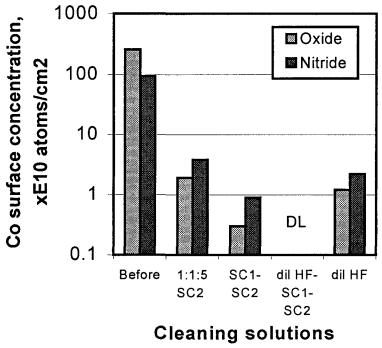

Fig. 8, Co contamination levels on oxide, nitride and RCA cleaned wafers before and after cleaning with dilute HF, SC1 and SC2 solutions

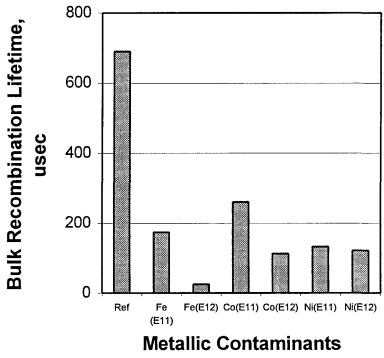

Fig. 10, Comparative bulk recombination lifetimes for oxide wafers contaminated with metallic contaminants.

THICKNESS DEPENDENT SENSITIVITY OF GATE OXIDES TO SURFACE CONTAMINATION

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In contrast to submicron geometry MOS devices which feature ultra-thin gate oxides power MOSFETs require gate oxides in the thickness regime from 30 nm to 70 nm. In this experiment the response of thin and thick oxides to surface contaminants is investigated. It is demonstrated that the response is relatively independent of oxide thickness when the same temperature of oxidation is used to grow thick and thin oxides. However, gate current instabilities in the pre-breakdown field regime were observed in the case of thin oxides grown on Si surfaces featuring an increased level of metallic contaminants, but were not observed for thick oxides.

INTRODUCTION

Following MOSFET scaling the thickness of gate oxides has been continuously shrinking. This trend has been accompanied by a growing awareness of the adverse effect of contaminants present on the Si surface prior to thermal oxidation on the integrity of the gate oxide and the quality of the Si/SiO_2 interface. As a result, the correlation between surface contaminants such as metallic and organic impurities and characteristics of thin gate oxides as well as guidelines concerning the highest allowable surface concentration of each contaminant are well established. What went seemingly unnoticed in the process, however, is the potential difference in the response to surface contaminants of very thin oxides (< 10 nm) and thick oxide (> 30 nm). For years, our attention has been focused primarily on the former which are technology drivers in advanced MOS and CMOS processing for logic and memory applications. On the other hand, there exist other families of MOSFETs, most notably discrete power transistors, in which in order to support gate voltages > 30 volts reduction of the gate oxide thickness is not desired. Consequently the gate oxides in this class of devices are rarely thinner than about 50 nm. Oxides in this thickness regime have received much less attention regarding the correlation between the condition of the Si surface prior to thermal oxidation and their electrical characteristics. What follows is the possibility that the requirements regarding surface cleaning procedures prior to ultra-thin and thick oxide growth may not be the same, and hence, cleaning procedures in the latter case may be optimized to meet the specific needs of thick gate oxide processing.

The goal of this experiment was to investigate the difference between thin and thick oxides in sensitivity to the level of surface contamination present on Si surfaces prior to oxidation. The incentives to undertake this research were two-fold. First, it has become apparent that the understanding of the effect of surface contaminants on the electrical

characteristics of thick oxides requiring high temperatures of oxidation and long oxidation times is not sufficient. Second, our early experiments led us to the conclusion that in some aspects the effect of surface contaminants on the electrical properties of thermal oxides may not be the same across the range of oxide thickness. This study is an attempt to clarify these observations focusing primarily on metallic surface contaminants.

EXPERIMENTAL

In this experiment 150 mm, p-type, (100) Si wafers are used. The degree of surface contamination was varied by means of wet chemical treatments applied prior to thermal oxidation. Specifically, procedures ending with an APM step and APM + HF:HCl:H_2O were employed expecting higher concentrations of metallic contaminants, most notably Al and Fe, in the former case. The first step in each cleaning sequence was a SPM treatment. Table 1 gives details of all wet cleaning steps applied in this study.

Table 1 Details of Wet Cleaning Steps Applied In This Study.

SPM	H_2SO_4 : H_2O_2 (1:4), 8 min.
APM	NH_4OH : H_2O_2 : H_2O (1:1:5), 40 °C, 8 min.
HF/HCl	HF : HCl : H_2O (1:1:100), room temperature, 8 min.

Following wet chemical treatments wafers were subjected to thermal oxidations resulting in oxides varying in thickness from 14 nm to 62 nm. Oxidations were carried out at 1000°C in either O_2 or O_2 + TCA. Subsequently, either Al-gate sputter deposited or n^+ implanted poly-Si gate MOS capacitors were fabricated. In the latter case MOS structures were processed in windows etched in a field oxide. Devices with two different gate contact areas were investigated. The electrical characteristics of gate oxides were obtained from gate oxide integrity (GOI) evaluation. In addition, TXRF and ELYMAT surface characterization were applied prior to gate oxidation in order to investigate the effect of surface condition resulting from the two different cleaning sequences used in this study.

RESULTS AND DISCUSSION

In order to confirm increased contamination resulting from the APM-last process as opposed to the HF/HCl-last process (Table 1) TXRF characterization of the respective surfaces was carried out. As expected, an increased level of surface metallic contaminants was observed in the former case (Table 2). In particular, the level of Fe was two orders of magnitude higher for the APM-last treated surfaces. The same difference is expected for Al contamination, although this effect could not been confirmed using TXRF due to the insufficient sensitivity of this technique to Al. Higher contamination with metals was also

concluded from the decreased diffusion length measured by ELYMAT on the APM-last treated surfaces (Table 2).

Table 2 The results of TXRF and ELYMAT characterizations for APM-last and HF/HCl-last surfaces.

TXRF Characterization (10^{10} atoms/cm^2)

Element	SPM + APM	SPM + APM + HF/HCl
Fe	219.0	2.1
Ti	2.1	1.9
Ni	2.9	2.7
Cr	0.3	< 0.7
Co	< 0.1	< 0.1
Cu	0.1	2.1
Zn	13.9	< 0.1

ELYMAT characterization

Diffusion Length	138 μm	636 μm

The next step in this investigation was to determine the effect of the higher surface contamination level on the electrical integrity of thick and thin oxides. Fig. 1a shows the distribution of oxide breakdown events in the case of 61.3 nm thick gate oxides while Fig. 1b shows the same for gate oxides 15.6 nm thick. In each case the breakdown field was determined at the current density of 1mA/cm^2. Comparing these two figures the following can be noted. First, a shift of breakdowns to lower values of electric field is observed in

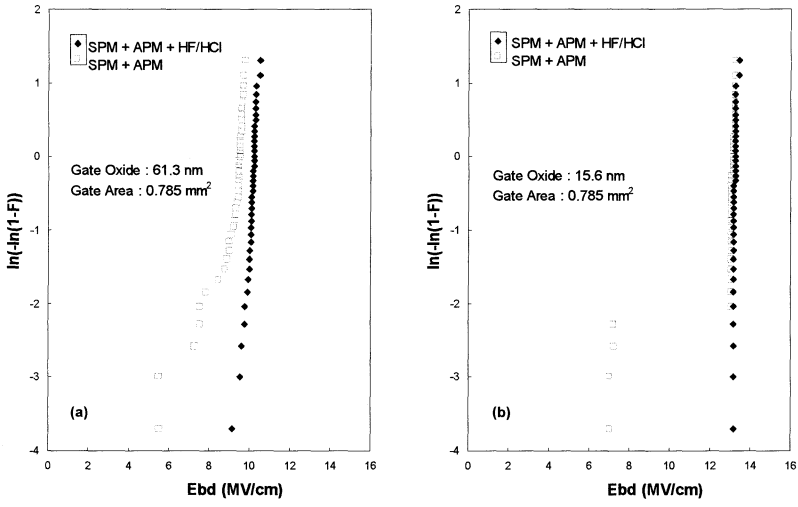

Fig. 1 Distribution of oxide breakdown events in the oxides grown on APM- and HF/HCl-last treated surfaces (a) 61.3 nm oxide, (b) 15.6 nm oxide.

the case of thick oxides for both APM- and HF/HCl-last surface treatments. This shift is due to the higher number of traps and defects incorporated in the thicker oxide, which reduces the oxide resistance to the electric field [1]. Second, the effect of different surface cleaning is shown in the shift of E_{bd} distributions in the case of thick oxides (Fig. 1a). Lower breakdown fields for oxides grown on APM-last treated surfaces are likely due to the increased concentration of Al in the oxide in this case and the resulting differences in oxide thickness [2] (not monitored in this experiment) causing a difference in the distribution of breakdown events. Furthermore, as depicted in Fig. 1, the distributions of oxide breakdown events in the case of APM-last treated surfaces show low-field breakdowns in the case of both thin and thick oxides. These breakdowns seem to appear at the same electric field in the oxide regardless of its thickness. Therefore, it is likely that they are caused by an effect independent of oxide thickness and controlled mostly by temperature such as increased concentration of Fe related charge traps at the Si-SiO_2 interface. As seen in Table 1 the concentration of Fe in the case of the APM-last treated surface is two orders of magnitude higher than that in the case of the HF/HCl-last treated surface. It should be noted at this point that although low field breakdown events do appear at the same electric field for thick and thin oxides their adverse effect on oxide reliability is relatively more pronounced in the latter case due to the higher intrinsic breakdown field of thin oxides.

As informative as they are, distributions of oxide breakdown effects do not show the complete picture of the effects occurring in the oxide at high electric fields which may have an effect on the oxide reliability. This is because they do not show the exact behavior of current in the oxide at electric fields approaching breakdown. The changes of oxide current as a function of electric field in the oxide exemplifying results obtained in this experiment are shown in Fig. 2 for thin and thick oxides in the case when a metallic

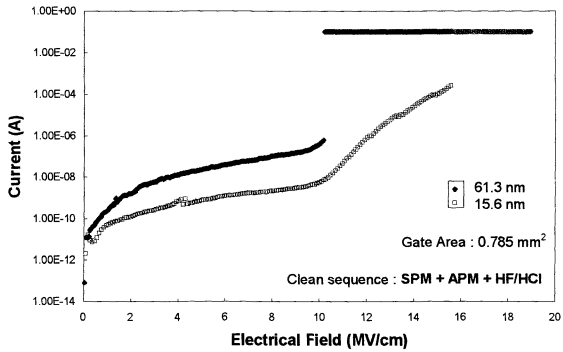

Fig. 2 I-E plot for 61.3 and 15.6 nm oxides grown on SPM + APM + HF/HCl cleaned surfaces in dry O_2 .

contaminants controlling HF/HCl step was performed at the end of the cleaning sequence.

As seen in Fig. 2 up to approximately 10 MV/cm the current plots for thick and thin oxides show similar behavior. At this point hard breakdown occurs in the case of thick oxides while thinner oxides sustain increased current, probably related to Fowler-Nordheim tunneling, and exhibit hard break down at a substantially higher field. This behavior is somewhat altered in the case where the APM step in the cleaning process is not followed by the additional HF/HCl treatment (Fig. 3). In this case unstable current characteristics are observed in the pre-breakdown regime in the case of thin oxides. As shown in Fig. 3, two different types of characteristics were observed indicating the role metallic contaminants may play in this case.

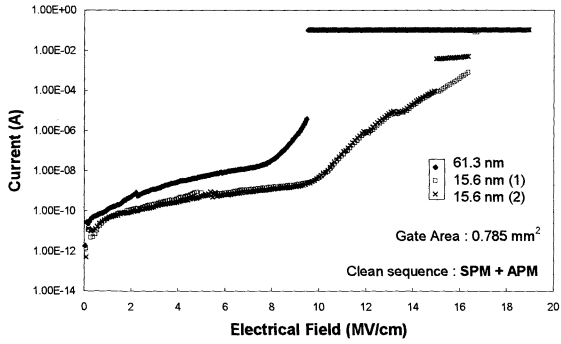

Fig. 3 I-E plot for 61.3 and 15.6 nm oxides grown on SPM +APM cleaned surfaces in dry O_2.

During the next stage of this experiment the same pre-oxidation procedures were applied, but TCA was added to the oxidation ambient for the purpose of complexing and/or volatilization of metallic contaminants. Fig. 4 and 5 show current-electric field characteristics for SPM + APM + HF/HCl and SPM + APM wet cleaning sequences respectively. These two plots demonstrated two important points. First, the addition of TCA did not affect in any significant manner the near-breakdown current in either thick or thin oxides in the case the HF/HCl step was implemented at the end of the cleaning sequence (Fig. 2 and 4). This is an indication that, as noted earlier the HF/HCl step is effective in controlling metallic contamination resulting from the APM exposure.

Second, addition of TCA to the oxidation ambient did not alleviate current instabilities in the pre-breakdown regime in the case of thin oxides and had no clear cut positive effect on the current flow in thick oxides (Fig. 3 and 5). Most importantly, however, these results once again indicate a less pronounced effect of surface metallic contaminants in the case of thick oxides. It is proposed that at least part of this is due to the shear difference in oxide thickness. In the case of thin oxides the probability of charge transfer from the gate to the substrate via interface traps and traps in the bulk of the oxide is obviously higher than in the case of thick oxides. Hence, at high electric fields in the

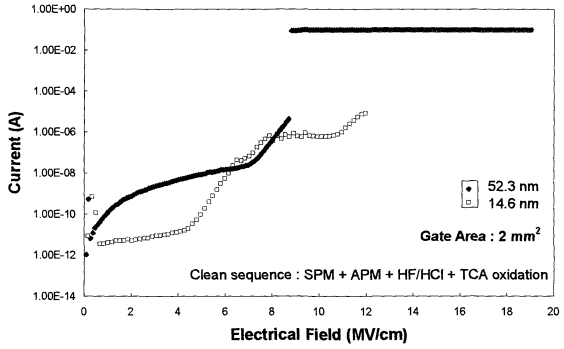

Fig. 4 I-E plot for 52.3 and 14.6 nm oxides grown on SPM + APM + HF/HCl cleaned surfaces in O_2 + TCA.

oxide the same concentration of interface and bulk traps is more likely to affect current characteristics in thinner oxides.

CONCLUSIONS

An overall conclusion from this experiment is that the extent to which surface contaminants affect oxide characteristics depending on its thickness should be considered differently when: (i) different oxide thicknesses are accomplished by varying oxidation time at the same temperature of oxidation and (ii) different oxide thicknesses result from differences in oxidation temperature. In this investigation the former case was considered.

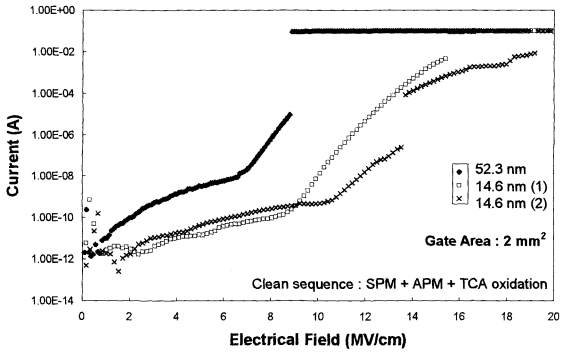

Fig. 5 I-E plot for 52.3 and 14.6 nm oxides grown on SPM + APM cleaned surfaces in O_2 + TCA.

A somewhat higher tolerance to surface contamination observed in this experiment for thicker oxides is believed to be mainly the result of longer distances between the gate contact, trap centers, and the substrate in thicker oxides making charge transport across the oxide more difficult. Otherwise, it is postulated that the degree of tolerance to surface metallic contaminants is not as much affected by oxide thickness as it is by the temperature at which thin and thick oxides are grown. This is because the temperature of oxidation is playing a role in defining the effect of the given type of contaminant. This concerns not only metallic impurities, but also the effect of surface carbon may be different in the case of temperatures above and below silicon carbide formation (around 850°C). Consequently, the effect of the same surface contaminants in a thin oxide grown at low temperature and a thick oxide grown at a higher temperature may be entirely different.

It is believed that through better understanding of the effects considered in this investigation pre-oxidation surface treatments design specifically to meet the requirements of thick gate oxide processing may be devised.

ACKNOWLEGMENTS

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FRONT END OF LINE WET PROCESSING FOR ADVANCED CRITICAL CLEANS

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ABSTRACT

The use of ultra-dilute (>/= 300:1), single pass RCA cleaning chemistries has been shown to be effective for front end of line applications. This process is attractive because of it's simplicity, performance, and cost. The use of megasonics is shown to be essential for effective particle removal. Surface microroughness and defect density increases are negligible. Trace surface metals contamination is at or below detection levels. UPW usage and cycle time are significantly reduced by application of megasonic quick dump rinsing. Further improvements in water usage can be realized by reducing wafer spacing. For HF last processes the use of STG drying eliminates water spot defect formation.

INTRODUCTION

The requirements for front end of the line cleaning in state of the art processes include low FM (foreign material) defect addition, the ability to remove FM (as measured by high particle removal efficiency), low surface metal and ionic contaminant levels, removal of trace organic material, and minimal increase in surface microroughness (1). Additionally the drive to lower manufacturing costs and reduce wastes has added the requirement to drastically lower the consumption of chemicals and ultra pure water (UPW). Cost factors also require the footprint and capital cost of wet process tools to decrease in order to reduce their overall cost of ownership (CoO).

Recent information has shown that RCA type cleans are equivalent in performance to HF last processes for pre-gate oxidation in the current generation of devices (2). Also the use of ultra-dilute, single pass, RCA chemistries (>/= 300:1) has been shown to be equivalent to that of dilute RCA chemistries (~80:1) in the key performance areas (3).

The use of megasonic energy is central to the success of ultra dilute chemistries in advanced cleaning strategies. Cavitation is believed to be one of the dominant mechanisms in megasonic cleaning. Sonoluminescence measurements indicate that a peak in cavitation density occurs close to the air liquid interface in megasonic baths (4). The use of a tube style transducer in combination with a quick dump valve makes possible movement of this interface across the surface of the wafer (5).

The quick dump megasonic rinsing technique has been shown to significantly reduce the time required for rinsing as measured by solution pH. In the post SC2 application

significant reduction in submicron LPDs was demonstrated with the use of the quick dump megasonic rinsing technique as a final step (6). Rinsing is enhanced because of a reduction in the boundary layer thickness caused by the action of the megasonic energy, allowing for more efficient transfer of the solute to the bulk solution which can then be carried away through the dump rinse action (7). The use of megasonics during the fill portion of the quick dump rinse cycle also has a positive impact on particle removal (8).

HF last cleaning is required because of process steps where complete removal of native oxide and hydrogen termination in device active areas are desired. The wafer surface created by HF last processes consists of adjacent hydrophilic and hydrophobic regions in proportions that depend upon the particular device layout and structure.

The formation of water spots has been described by the coalescing film model (9). Following HF last processing rinse water reacts with the wafer surface, causing silica concentration to increase. After removal from the final rinse bath water droplets form in the high contact angle, hydrophobic surface regions. These water droplets are trapped in device topography that has an effectively lower contact angle. As evaporation occurs silica concentrates in the trapped droplets until particles nucleate and deposit on the surface to form water spots. In order to prevent water spot formation water must be removed from the surface of the wafer while preventing droplet formation, trapping, and deposition of silica from solution. Drying technologies which take advantage of the surface tension gradient effect (STG) have been shown to be effective in this application (10).

EXPERIMENTAL

Equipment

The equipment used for this work consisted of a glove fit PVDF tank equipped with a megasonic transducer, quick dump rinse valve, and insitu chemical and UPW injection ports. Precision syringe type metering pumps were used to inject ammonium hydroxide, hydrogen peroxide, non-ionic surfactant, and HCl as required by the process recipe. A PLC based controller was used to sequence the chemicals, ambient and heated UPW, megasonic transducer, and quick dump rinse valves. A separate tank equipped with a filtered recirculation loop and temperature control system was used for the dilute HF portion of the process. A molded PFA carrier designed for minimum contact with the wafers, zero shadowing of the megasonic energy, and ease of drying was used to support the wafers. A Yield Up model Omega 2000 STG dryer equipped with specially designed supports for the wafer carrier was used for drying. Wafers were transferred between the megasonic equipped process tank, dilute HF bath, and dryer manually; however all techniques and processes are compatible with fully automated robotic transfer systems

Process Sequence

Details of the ultra-dilute RCA clean sequence are presented in Table I (11). The total cycle time for all steps shown is approximately 21 minutes.

Table I: Details of Ultra-dilute RCA Clean Recipe steps

Name	Chemical *	Volumetric Ratios	Temperature Range(C)	Comments
Vc1	DI H_2O NH_4OH H_2O_2 Surfactant	300 1 2 0.5	55 - 65	single pass, insitu chemical injection, megasonic pH ~9.5
Rinse	UPW	N/A	ambient	megasonic QDR
Vc2	DI H_2O HF	100 1	20 - 25	recirculated, filtered, temp. controlled bath
Rinse	UPW	N/A	ambient	overflow
Vc3	DI H_2O NH_4OH H_2O_2 Surfactant	1000 1 5 2	ambient - 65 (ramped)	single pass, insitu chemical injection, megasonic pH ~5.3 - 5.9 (prior to NH_4OH injection)
Rinse	UPW	N/A	ambient	megasonic QDR
Vc4	DI H_2O HCl	1000 1	45 -55	single pass, insitu chemical injection, megasonic pH ~2.2 - 2.8
Rinse	UPW	N/A	ambient	megasonic QDR

* Initial chemical concentrations as follows: NH_4OH - 30 wt%, H_2O_2 - 30 wt%, HCl - 37 wt%, surfactant - 100:1 volumetric dilution with UPW, HF - 49 wt%.

The Vc1 step is a an ultra-dilute mixture of ammonium hydroxide, hydrogen peroxide, and non-ionic surfactant that is dispensed at a nominal temperature of 60C. The purpose of the Vc1 step is to remove particles and trace organics while minimizing etching of the surface.

The Vc2 step is a dilute HF dip which is used to remove trace metals and thin layers of oxide. This step is generally performed in the recirculated, filtered, and temperature controlled bath; however the chemical injection technology described above is compatible with insitu dispense of the HF in the megasonic equipped bath. For this work a 30 second dip time and 100:1 volumetric dilution with UPW was used; however in practice this concentration and exposure time can vary with the amount of oxide removal required and the uniformity specification. In advanced applications where low removal rates and non-uniformity are required more dilute formulations are typically used.

The Vc3 step is used to passivate the surface after the dilute HF step. Non-ionic surfactant and hydrogen peroxide are first dispensed at ambient temperature to wet the

surface and form a thin native oxide layer. Because the pH is low the native oxide is formed without addition of trace metals to the surface. Temperature is then ramped to 60C to complete passivation. Ammonium hydroxide and megasonics are then added for additional particle and trace organic removal once the passivation has been completed.

The Vc4 step consists of ultra-dilute HCl at a nominal temperature of 50C that is used in conjunction with megasonics to further lower the trace metal concentration on the surface. A final step consisting of an ultra-dilute HF dip and overflow rinse is incorporated for HF last processes.

RESULTS AND DISCUSSION

Rinsing

The Vc1, Vc3, and Vc4, rinse steps are performed in the megasonic equipped bath using the megasonic quick dump rinse and fill technique. Figure 1 compares overflow and quick dump rinsing techniques with the megasonic. The use of the megasonic quick dump rinse and fill technique allows for complete rinsing to occur after only 4 dump and fill cycles. The result is a reduction in UPW consumption during the rinse of up to 85% as compared to the overflow technique.

The rinse following the Vc2 step is also performed in the megasonic tank; however megasonics are not used and rinsing is performed by the overflow technique. In this case it is not desirable to rinse to neutral pH since it is advantageous from a surface metals addition standpoint to begin the Vc3 step in the low pH range. This coincidentally is favorable for conservation of UPW.

Particle Addition

To test particle addition prime P-type 100 wafers with out of box starting LPD counts less than 50 at a threshold of 0.12 microns as measured on a Tencor model 6200 laser scanner were used for evaluation. 2 wafers were run through multiple passes of the process along with clean filler wafers. Separate tests were run for both the non-HF last and HF last process sequences. These results are shown in Figures 2a and 2b.

Particle Removal

It is well known that particle removal efficiency in SC1 cleans is enhanced by the use of megasonics. Figure 3 shows that the particle removal efficiency of silicon nitride particles is negligible when the megasonic is not used in the ultra-dilute RCA clean process. In this case only the Vc1 process sequence was tested.

The use of half spaced wafer processing can reduce UPW consumption by 50%, since twice as many wafers can be processed in each run. In order to test the effect of reduced wafer spacing a comparison was made of silicon nitride particle removal efficiency for full spaced wafers (0.25") vs. half spaced wafers (0.125"). The results shown in Figure 4 indicate that removal efficiency is equivalent using the standard process.

Trace Metals

Tests for trace metals addition were run on the non-HF last process sequence. Results were obtained using the VPD-ICPMS technique. The control was an out of box prime wafer that was not processed. In Table II these results are compared to the specification for 0.13 micron process technology published in the 1997 SIA Roadmap (1). The results show that the ultra-dilute RCA process meets the requirements for all critical metals where the detection level of the measurement is below the specification limit. The specification for Ca, Fe, K, and Na is below the test method detection level, so it is not known if the result meets the requirement.

Table II: Trace surface metals as measured by VPD-ICPMS for ultra dilute RCA cleaning process (E10 atoms/cm2).

Element	Detection Level	0.13 micron Spec. (1)	Control	Sample	Result vs. Specification
Ca	0.5	0.2	4.9	<DL	Unknown
Co*	0.01	0.2	0.05	<DL	Pass
Cr	0.1	0.2	<DL	<DL	Pass
Cu	0.1	0.2	<DL	<DL	Pass
Fe	0.3	0.2	<DL	<DL	Unknown
K	0.5	0.2	14	<DL	Unknown
Mo*	0.05	0.2	<DL	<DL	Pass
Mn*	0.05	0.2	7.6	<DL	Pass
Na	0.5	0.2	20	<DL	Unknown
Ni	0.05	0.2	<DL	<DL	Pass

Asterisk (*) indicates these elements tested in a separate sample.

Surface Microroughness

Surface microroughness was evaluated by AFM. Figures 5a and 5b show the results on an out of box prime wafer before and after exposure to the ultra-dilute RCA clean sequence. The increase in RMS surface microroughness in this case is negligible at 0.1 Ang.

Water Spots

Patterned 200mm wafers were inspected for water spots at 50x to 200x using an optical microscope following HF last processing. The STG drying sequence was as follows: 1) wafers are introduced into an overflowing rinse bath; 2) the rinse bath is sealed with a lid equipped with manifolds for IPA and heated nitrogen dispense; 3) a mixture of nitrogen and IPA is introduced through the lid while the rinse water is drained at a controlled rate; 4) after the chamber is completely drained the IPA flow is turned off and a high flow of heated nitrogen is used to complete the drying process.

HF last testing showed that water spot free drying and acceptable FM levels could be obtained over a wide range of process conditions for full spaced processing; however water spots were observed in the center of the half space processed wafers. A typical water spot defect is illustrated in Figure 6. The following measures were taken to improve the process: 1) a supplemental flow of heated nitrogen was added during step 3 of the drying process; 2) the flow of IPA was increased; 3) the drain rate was reduced.. Figure 7 shows the effect of drain rate on the number of water spots observed.

CONCLUSIONS

1) The ultra-dilute RCA clean performance for FM addition, particle removal, trace surface metals, and surface microroughness is suitable for advanced, critical processes. 2) The megasonic quick dump rinse technique provides significant savings of UPW and improves cycle time; 3) The use of half spaced wafer processing can provide for additional savings of water and chemicals while retaining performance. 4) Optimized STG drying allows for water spot free HF last processing.

ACKNOWLEDGEMENTS

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FIGURES

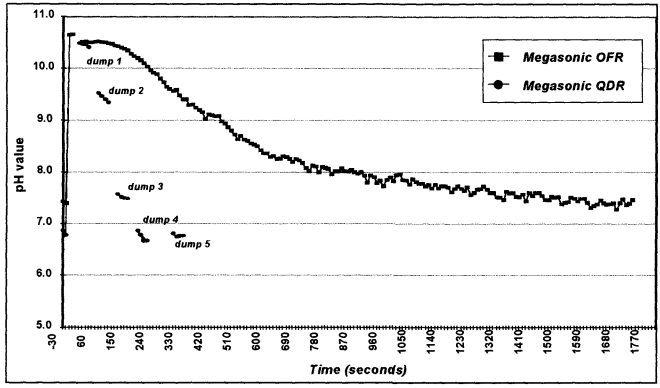

Figure 1: Comparison of megasonic overflow and megasonic QDR.

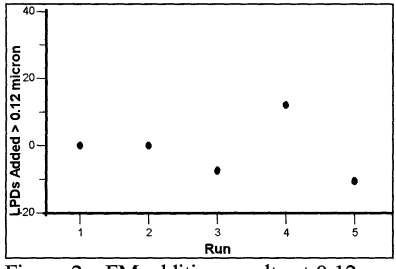

Figure 2a: FM addition results at 0.12 micron threshold for ultra dilute RCA process and STG dry

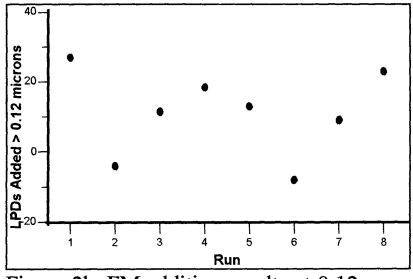

Figure 2b: FM addition results at 0.12 micron threshold for ultra dilute RCA process with HF last and STG dry

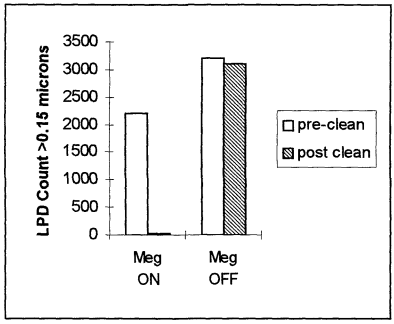

Figure 3: Effect of megasonic on Si3N4 particle removal for Vc1.

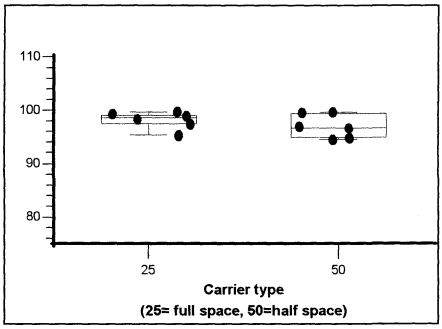

Figure 4: Silicon nitride particle removal efficiency (%) at 0.15 microns for full spaced and half spaced wafer processing.

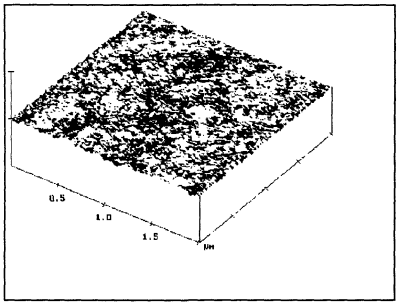

Figure 5a: AFM image of silicon surface prior to clean. RMS microroughness is 0.6 Ang.

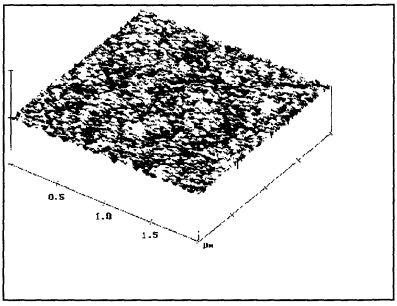

Figure 5b: AFM image of silicon surface after ultra-dilute RCA process. RMS surface microroughness is 0.7 Ang.

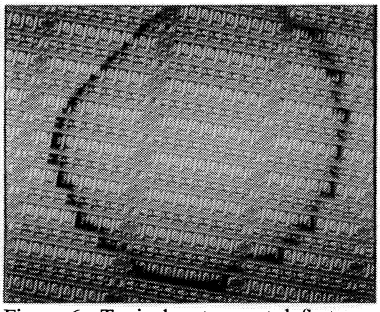

Figure 6: Typical water spot defect.

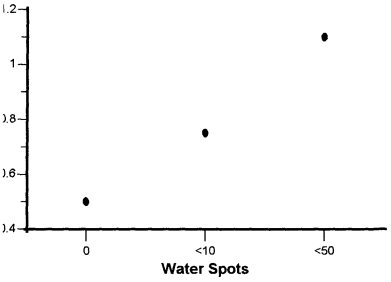

Figure 7: Water spots vs. drain rate (mm/sec) for half space processing..

CARRIER INDUCED SILICON PITTING IN HF-RCA CLEANING SEQUENCES.

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INTRODUCTION.

Wafer carriers used in conventional wet benches are well known to be a source of many dangerous issues on wafer surface [1]. In particular, care must be paid during carrier manufacturing, since pressure gradients as well as non-perfectly controlled cooling rates might induce local porosity in carrier walls. Pores could absorb chemicals from process tanks or vapors from the wet bench environment, and subsequently release it on the wafers, thus generating micro-corrosion. Effects of micro-corrosion have been evaluated by haze measurements, AFM and ToF analysis.

EXPERIMENTAL SETUP.

Three different cleaning sequences have been tested on a STEAG 3rd generation Automatic Wet Processor (AWP): RCA, HF+RCA, and SOM+HF+RCA. Details of sequences are illustrated in Table 1. In addition, a simple rinse sequence (10 minutes in high-flow, 18°C de-ionized water) has been checked.
P-type, CZ (1.7÷2.5 Ωcm), 150 mm bare silicon wafers were used for tests.
Haze measurements have been performed on a KLA-Tencor SP1 laser particle counter [2]. Surface roughness has been measured by an Autoprobe LS Automatic Force Microscope (AFM) manufactured by Park Scientific Instruments. ToF analysis has been performed using a ToF-SIMS IV produced by Ion-Tof Cameca.

EXPERIMENTAL RESULTS.

Wet benches can generally process batches composed by 50 wafer. A single batch can be realized either with two 25-slot carriers (Fig. 1) or with a single carrier (Fig. 2), able to accommodate 50 wafers together. Usually, carriers are made of fluorinated compounds (PTFE or PFA), due to their properties of mechanical and chemical resistance with respect to the hostile environments in which they must operate (acid/alkaline baths, high temperature).
In Fig. 3 and 4 are reported haze[2] maps obtained scanning "front" wafers loaded respectively in a 25-slot carrier and in a 50-slot carrier ("exposed" wafers). The wafers underwent a HF+RCA sequence. Darker areas correspond to surface without haze, lighter areas to highly hazy surface. It is easily observed how hazy surface corresponds to areas "shielded" by the carrier endwalls.

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[2] *Haze* is related to surface roughness. Since a wafer surface is not ideal, part of the incoming light is deflected from specular reflection by surface contamination (particles), roughness or waviness of the surface. Light diffused by particles generates high-frequency signals, while surface waviness or roughness determine low-frequency detector outputs. Actually, haze is measured in ppm of light diffused in non-specular directions with respect to the incoming light flux.

In 50 wafer carriers, turning 50th wafer frontside rear (Fig. 5), or loading test wafer in slot 49 with a dummy wafer to protect them from exposure to carrier wall (Fig. 6) did not give results similar to exposed wafer (i.e. some haze was detected). Anyway, in all cases, hazy features were not displayed and haze maps are comparable to bare silicon (Fig. 7).
Loading test wafer in slot 1 with polished face exposed to carrier walls gave rise to haze maps with a reduced haze region (Fig. 8), altough absolute haze value in these region is similar to the ones obtained on exposed front wafers).
RCA cleaned wafers loaded correctly in slot 50 (Fig. 9) gave as well silicon surface without haze. The same was recorded for a simple rinse sequence (Fig. 10) – see previous section.
Using a SOM+HF+RCA sequence, hazy regions over exposed wafer simply disappeared (Fig. 11).
In addition to haze measurements, particle contamination has been checked for different sequences: results of this test are shown in Fig. 11. Apparently, the HF+RCA sequence displays the worse behavior, either for exposed or unexposed wafer. All other sequences show similar effects. In Fig. 12 all haze results are summarized.

DISCUSSION.

The parameter of interest in analyzing haze maps is not the average value (since large areas of wafer surface show haze values typical of a bare silicon/RCA cleaned wafer), but the peak haze. Peak haze is simply the maximum haze value detected by the SP1. Haze scanning recipes have an "autobinning" feature, which sets the maximum haze interval to 0.15÷0.16 ppm: any area with a haze greater than 0.16 ppm is put in the "above range" bin, and amount of the surface with haze above range is reported by the tool. Fig. 13 shows the relative amount of surface characterized by an "above range" haze for exposed and protected wafers. It is easily seen that exposed wafer show a larger hazy area. In Fig. 14 an AFM picture of hazy areas is reported. Haze is determined by round holes in the surface, a few angstroms deep and some microns large. The mechanism of this round-shaped corrosion has not pointed out yet.
Small portions of frontside and rearside carrier wall have been cut and analyzed with ToF-SIMS: results are reported in Fig. 15. In this graph the amount of NH_x radical found on carrier walls is plotted as a percentage of C_xF_y peaks detected by ToF. No quantitative analysis was possible due to the fact that ToF calibration for organic material is very difficult. It is apparent that frontside carrier wall absorbed a NH_x quantity an order of magnitude greater than rearside wall. At present, it is not clear how the ammonium radi cal were absorbed, whether in SC-1 bath or from environment.
The macromechanism of the haze increase during HF+RCA sequences is illustrated in Fig. 16: absorbed ammonia is released during HF dip, when wafer surface is hydrophobic and thus bare silicon is exposed to the etching action of NH_4^- radical. In SOM+HF+RCA sequence, instead, the highly oxidizing initial step protects silicon surface with a thin layer of chemical oxide, while high temperature helps in "extracting" ammonia from the carrier; since surface is protected, no etching reaction can take place.

FURTHER DISCUSSION AND CONCLUSIONS.

Fluorinated hydrocarbons are characterized by C-F bonds; these bonds strenghten the thermo-mechanical characteristics and resistance to the action of chemicals they are immersed in. The use of these compounds in microelectronic industry as a material to build wafer carriers has been suggested by these properties; nevertheless, there are some drawbacks: particle generation due to friction, contamination of wafers, etc. Among

these, a major issue is represented by the porosity these materials possess, in such a way that some chemical can be absorbed and subsequently released over the wafer surface, causing haze problems. In order to overcome such a problem, carrier manufacturers suggest to periodically clean up carriers with different procedures [3], [4], [5], [6], [7], [8].

Actually, from the results so far illustrated, it is difficult to attribute the asymmetrical haze generation to a problem of 'natural' chemical absorption: a better understanding of the mechanism can be obtained looking at fabrication procedures of fluorinated hydrocarbons manufacts.

Bulk fluorinated hydrocarbons objects fabrication start by raw material granular powders [9], [10]. These powders are loaded into molds whith the shape of the desired object; pressure is applied (up to 4000 psi, depending on the process). After that, a sintering process takes place: it is generally composed by at least four thermal cycles:

1. sample heating to a temperature T_1 ($300°C<T_1<400°C$)
2. hot temperature treatment at temperature T_1
3. sample cooling to a temperature T_2 ($T_2 \approx 300°C$)
4. sample cooling to room temperature (with a different rate)

(between cycle 3. and 4., other cooling cycles can take place). After that, and if needed, additional machining gives the manufact the required shape.

Sintering temperature and cooling conditions determine mechanical characteristics and permeability of the compoud to the desired extent. Tight control of sintering and cooling condition plays a key role when final quality of the manufact is taken into account: temperature gradients have locally a deleterious effect over mechanical characteristics, and pressure gradients during the premold phase cause a non uniform increase in porosity. Another source of problems is the machining itself: if the blades are not clean, local contamination can be transferred to the manufact.

The root cause of the pitting phenomena observed is most likely the onset of pressure gradients along thecarrier mold. Even if the micromechanism of pitting has not been found out, the key role played by HF is clearly apparent. A high temperature oxidizing step before HF dip is instrumental to prevent surface corrosion; nevertheless, growing interest for an environmental friendly cleaning process is pushing towards low temperature, sulphuric-free and dilutes chemistries. So, tight process control of carrier manufacturing must be required in order to avoid overall disuniformities along the carrier itself and between different carriers. A viable alternative is represented by new generation hybrid tools or single tank tools, in which carriers are absent (and thus any possible problem related to their usage is eliminated).

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Authors are fully indebted to Dr. Francesco Cazzaniga (STMicroelectronics, Materials Characterization Lab) for AFM measurements and Dr. Federica Zanderigo (STMicroelectronics, Materials Characterization Lab) for ToF-SIMS analysis. They also would like to thank Dr. Francesca Illuzzi (STMicroelectronics, Materials Characterization Lab) and Dr. Miracca (AUSIMONT CRS) for the useful discussion about fluorinated materials, and their manufacturing procedures. Last but not least, Mr. Giancarlo Perfetti (Politecnico di Milano, Materials Engineering) was very helpful in finding documentation on PTFE and PFA.

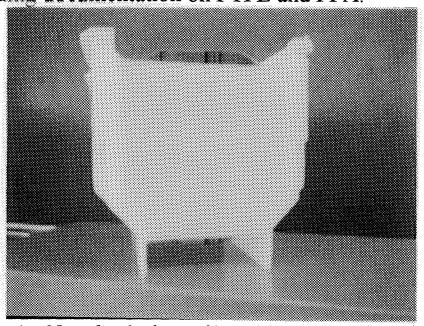

FIG. 1. *25-wafer high profile PFA carrier. A wafer is correctly loaded in slot 25 with polished face pointing towards carrier endwall.*

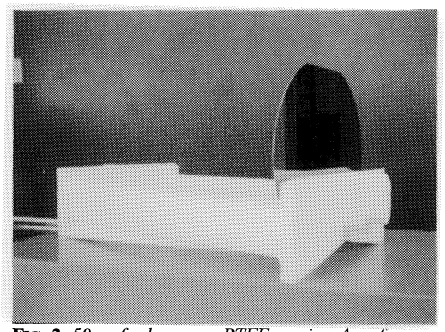

FIG. 2. *50-wafer low mass PTFE carrier. A wafer Is loaded in slot 50 with front exposed.*

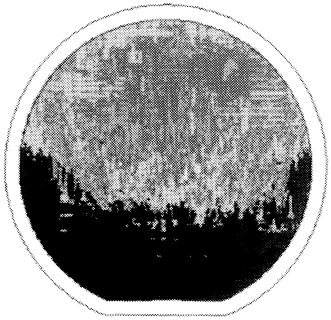

FIG. 3. *Haze map of a frontside wafer loaded on a 25-wafer high profile PFA carrier. Light grey area is high haze surface. "Streaks" are a footprint of bath hydrodynamics.*

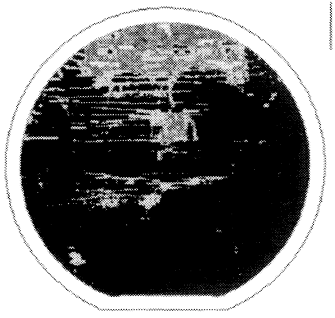

FIG. 4. *Haze map of a frontside wafer loaded on a 50-wafer low mass PTFE carrier. Light grey area is high haze surface. Hazy area is corresponding to wafer region "shielded" by carrier endwall.*

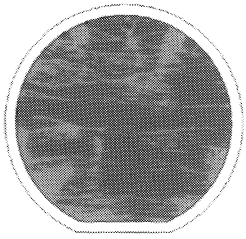

FIG. 5. *Haze map of a wafer front-loaded (slot 50), turned frontside rear. A very light (in quantity and quality) corrosion effect is noticed in top region.*

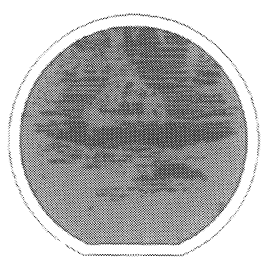

FIG. 6. *Haze map and histogram of a wafer rear-loaded (slot 1), turned frontside rear (mirror polished face is exposed to carrier rear endwall). Some haze is observed in top region.*

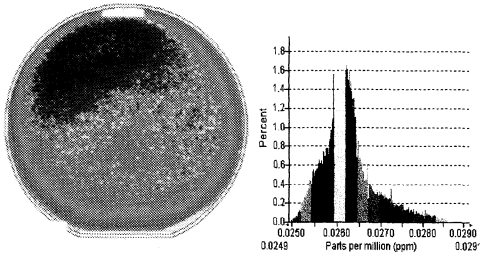

FIG. 7. *Haze map and histogram of a bare silicon, non-processed wafer. Notice histogram x-axis scale.*

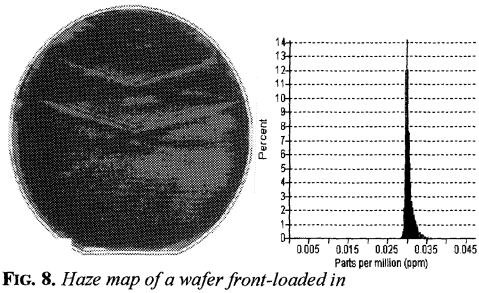

FIG. 8. *Haze map of a wafer front-loaded in slot 49 with a dummy wafer loaded in slot 50. No major effect is detected.*

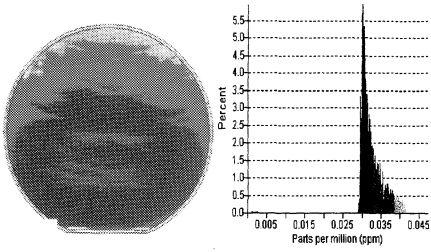

FIG. 9. *Haze map and histogram of a RCA processed bare silicon wafer.*

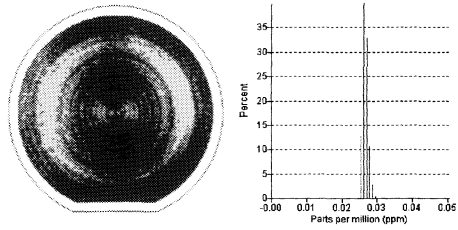

FIG. 10. *Haze map and histogram of a wafer processed with a simple rinse sequence (10' high-flow OFR).*

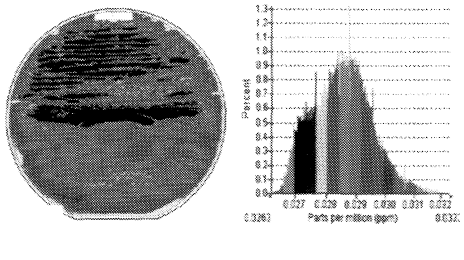

FIG. 11. *Haze map and histogram of a bare silicon wafer, frontside loaded in slot 50, processed with a SOM+HF+RC Sequence. Notice histogram x-axis scale.*

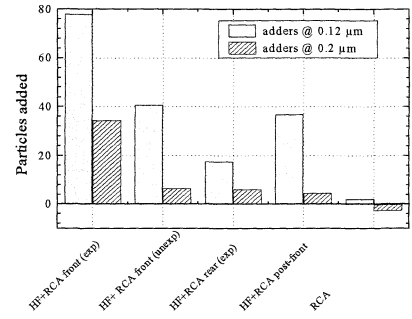

FIG. 12. *Particle contamination induced by various sequences tested. In all cases, the sequence HF+RCA shows the worse performances for wafers loaded in front positin or in immediately subsequent slot.*

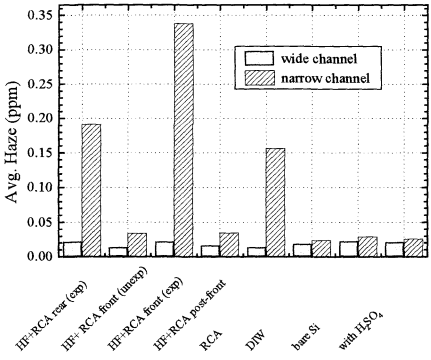

FIG. 13. *Avg. haze vs. different cleaning sequences. Both SP1 detection channels (wide, with a collection angle between 25° and 70°, and narrow, with a collection angle between 5° and 20°) are displayed. Most sensitive collection angle is narrow channel. HF+RCA sequences show the highest values.*

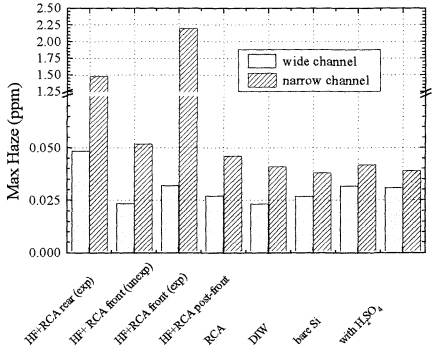

FIG. 14. *Max. haze (i.e. "haze peak") vs. different cleaning sequences. Both SP1 detection channels) are displayed. Again, HF+RCA sequences show the highest value recorded by narrow channel (2 orders of magnitude with respect to non-HF sequences or SOM).*

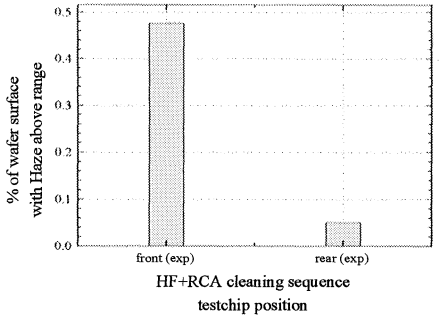

FIG. 15. *Graph showing the percentage of wafer surface whose haze is above binning (> 0.16 ppm), as a function of testchip positon along the carrier. Wafers have been exposed to carrier endwall.*

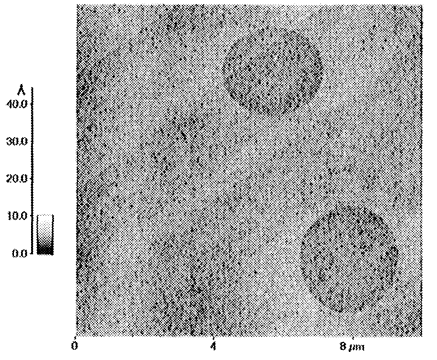

FIG. 16. *AFM picture of high haze region (see Fig. 4). Holes in surface are clearly visible.*

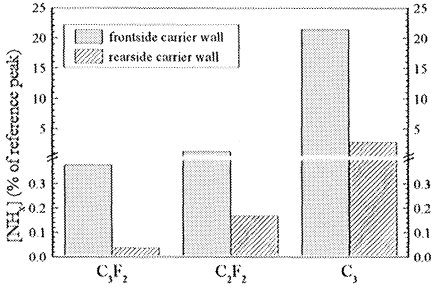

FIG. 17. *Ammonia absorbed by carrier walls expressed in percentage of C_xF_y peaks.*

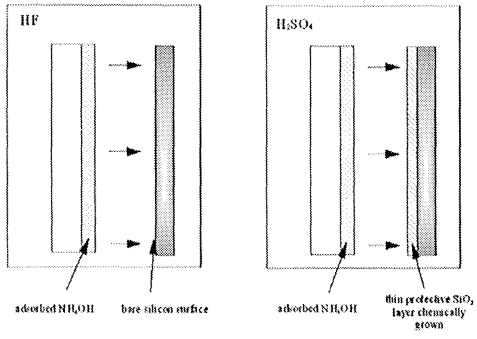

FIG. 18. *Explanation of the etching mechanism in HF solution and silicon surface protection in SOM solution.*

Sequence	Chemical Bath							
	SOM		HF		SC-1		SC-2	
	96% H_2SO_4, 90 ppm O_3		1:20 (HF:DIW)		0.25:0.5:5 (NH_4OH:H_2O_2:H_2O)		1:1:5 (HCl:H_2O_2:H_2O)	
	temperature	*diptime*	*temperature*	*diptime*	*temperature*	*diptime*	*temperature*	*diptime*
RCA					50°C	7'	50°C	5'
HF+RCA			25°C	2'	50°C	7'	50°C	5'
SOM+HF+RCA	100°	4'	25°C	2'	50°C	7'	50°C	5'

TABLE 1. *Cleaning sequences tested during experiments.*

AN ULTRADILUTE AMMONIA PROCESS FOR PARTICLE REMOVAL

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ABSTRACT

A new particle removal process has been developed that utilizes a cascading flow of ultradilute point-of-use-generated ammonium hydroxide solution at ambient temperature with megasonic energy. Particle removal efficiencies were obtained for a variety of materials and particle mean diameters. The influence of the temperature, megasonic energy, and the presence of ammonia on particle removal was investigated. It is postulated that this process employs the megasonic energy to detach particles from wafer surfaces while the ammonium hydroxide solution creates the appropriate wafer and particle zeta potentials that prevent particle reattachment, and the cascade overflow transports the particles out of the cleaning system.

INTRODUCTION

Mixtures of hydrogen peroxide and ammonium hydroxide, commonly referred to as Standard Cleaning Solution 1 (SC-1), have been the fluid of choice since the 1970s (1) for removing particulate contamination from semiconductor wafers. The SC-1 process is believed to detach particles through surface etching and prevent their reattachment through electrostatic repulsion. Particle detachment improvement has been reported when megasonic energy is employed (2).

Researchers have reported that 10 Å to 20 Å of surface etching is needed to obtain good particle removal (3). On the other hand, care must be taken to avoid excessive etching that could roughen the surface and lead to detrimental gate performance (4). The etch rate is controlled by the oxidation of silicon by the hydrogen peroxide, and surface etching of the oxidized silicon by the ammonium hydroxide. Etch rate increases with temperature and ammonium hydroxide concentration, and decreases with hydrogen peroxide concentration (5). A certain critical hydrogen peroxide concentration is required to prevent attack of the underlying silicon. This presents a control challenge, since hydrogen peroxide naturally decomposes. So it would be advantageous if hydrogen peroxide were not required.

Silicon and silicon dioxide surfaces are negatively charged in high-pH solutions such as SC-1. This is also true for many particles commonly found in semiconductor processing environments. The surface and particle will repel one another because they possess charges of the same sign. However, the high ionic strength of SC-1 solution significantly reduces the strength and range of the repulsion (6). Hence, a low-ionic-strength analog of the SC-1 solution would be preferred.

It is well-known that due to the high pH of SC-1 solutions, metals present in the SC-1 become incorporated into the surface oxide. Therefore, it is common practice to follow SC-1 with an acidic solution to remove these metals (7). A preferred approach would be to clean with a single pass of metal-free chemicals.

This paper reports on an alternative to the SC-1 process that is intended to emulate the particle removal capability of the SC-1 solution without its contamination, cost and instability issues. This process utilizes a single-pass cascade overflow of an ultradilute point-of-use-generated ammonium hydroxide solution in conjunction with megasonic energy. This process has significant advantages over the standard SC-1 process. Surface etching is reduced by limiting the ammonia concentration and temperature and applying this process only to oxidized surfaces. Excellent metallic contamination performance is expected, since only ultraclean DI water and gaseous NH_3 are used in the process. Superior particle reattachment performance is expected because this cleaning solution has a much lower ionic strength than SC-1 and thus has a stronger particle-surface repulsion force. Further, chemical costs and costs of chemical disposal are reduced since no hydrogen peroxide or concentrated ammonium hydroxide is used as raw materials.

EXPERIMENTAL PROCEDURE

Screening experiments were conducted first to identify the primary controlling factors of the process. A standard process was developed based on the results and evaluated for cleaning performance.

Cleaning Apparatus

Wafers were processed in a YieldUP 6200 Immersion Cleaning System. This is a two-tank system in which the particle removal process is conducted in the first tank, and the final rinse and dry is conducted in the second tank. The first is a quartz tank with a cascade/overflow design and a megasonic transducer liquid-coupled to the bottom of the tank as illustrated in Figure 1. Ammonia gas is injected and dissolved into the DI water stream (< 150 ppm) prior to entering the bottom of the tank. The second tank is a standard YieldUP STG™ rinse/dry tank that uses a cascade overflow of DI water followed by a drain step using an isopropyl alcohol-induced surface tension gradient. A hot nitrogen gas drying step completes the rinse/dry cycle.

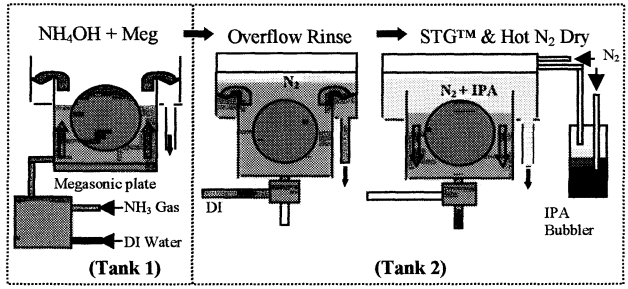
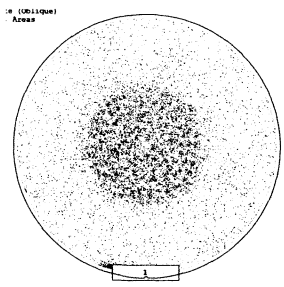


Figure 1. The two-tank ultradilute NH_4OH + megasonic particle removal process.

Screening Experiments

Experiments were conducted on wafers intentionally contaminated with particles to observe the effects of ammonia, temperature and megasonic energy on particle removal. The 200-mm wafers used for this set of experiments were prepared using an MSP-2300 Particle Deposition System. This technique has been previously described by Liu, et al (8). The MSP system was used to deposit SiO_2, Si_3N_4 or W particles on separate wafers. Approximately 20,000 to 25,000 particles in the diameter size range of 60 nm to 300 nm were deposited over the entire wafer surface. Particle counts before deposition (N_i), after deposition (N_d) and after cleaning (N_c) were measured utilizing a KLA-Tencor Surfscan SP1^{TBI} as shown in Figure 2. Particle removal efficiencies were calculated as percent removal using the following formula:

$$\% \text{ Removal} = [(N_d - N_c) / (N_d - N_i)] \times 100\%$$



Size Range (nm)	Count
60 - 120	16,312
>120	7,785
Area count	954
Total count	**24,097**

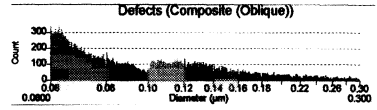


Figure 2. Particle maps and size distributions for a W-deposited wafer before cleaning.

Four identical groups of wafers containing one wafer of each particle type in addition to one clean monitor wafer were subjected to different cleaning recipes. The following four cleaning recipes were used:

- Run 1: the standard process that utilized an ~ 50 ppm NH_3/DI water mixture at ~ 60°C with ~ 350 watts of megasonic energy.
- Run 2: the same as Run 1 except it was conducted at ~ 20°C (room temperature).
- Run 3: the same as Run 1 except there was no NH_3 in the DI water flow stream.
- Run 4: the same as Run 1 except there was no megasonic energy.

Process Performance Demonstration

Based on the results of the screening experiment and other tests, a standard process (YP-1) was developed. This process utilized ~ 110 ppm NH_3 in 60°C DI water with ~ 450 watts of megasonic energy. This process was evaluated for particle removal efficiency, native oxide etching, surface roughening and metallic contamination.

Particle removal tests were conducted on the following three groups of 200-mm wafers:

- Prime monitor wafers with fewer than 150 particles (< 150 nm) per wafer
- Wafers that were intentionally contaminated with 3,000 to 4,000 nitride particles (< 150 nm)
- Wafers that had been used as particle monitors for a variety of deposition process tools, and that had 5,000 to 60,000 particles (< 150 nm) each

The intentionally-contaminated wafers were prepared by cleaning prime 200-mm wafers with an FSI B Clean in a MERCURY® Surface Conditioning System, a spray tool, and then immersing them into a solution containing suspended silicon nitride particles. Wafers were processed and analyzed at a customer location using a KLA-Tencor Surfscan SP1.

Native oxide etch loss was evaluated by placing six virgin prime 200 mm wafers into the system. After each of the six consecutive room temperature process runs one wafer was removed and measured . Oxide thicknesses were measured at 49 points, using a Nanospec 8300XSE ellipsometer. Oxide loss was calculated as the difference between the average oxide thickness before and after processing.

Surface roughening was measured on the wafer before and after cleaning, using a Digital Instruments Dimension 7000. This instrument has a resolution of 0.1 Å in the Z-axis and was calibrated against VLSI Surface Topography Standard STS-1800. Data accuracy in the Z-axis is better than 1%. Surface roughness measurements were taken in a 2 μm x 2 μm area in the center of the wafer. Metallic contamination was measured on the wafer before and after cleaning, using a TREX 610-T TXRF instrument.

RESULTS AND DISCUSSION

Screening Experiments Results

Particle removal efficiencies of the four process runs for particles with diameters greater than 60 nm and 120 nm are summarized in Figure 3. The 20°C (room

temperature) process yielded higher particle removal efficiencies than the 60°C process for all particle types and sizes. Most researchers have reported that particle removal efficiencies increase with an increase in process temperature when utilizing SC-1 chemistries. This is commonly believed to be due to the increase in surface etch amount with an increase in temperature. However, Resnick (2) reported that at high megasonic energies excellent particle removal in the range of 25°C to 65°C is achieved regardless of temperature.

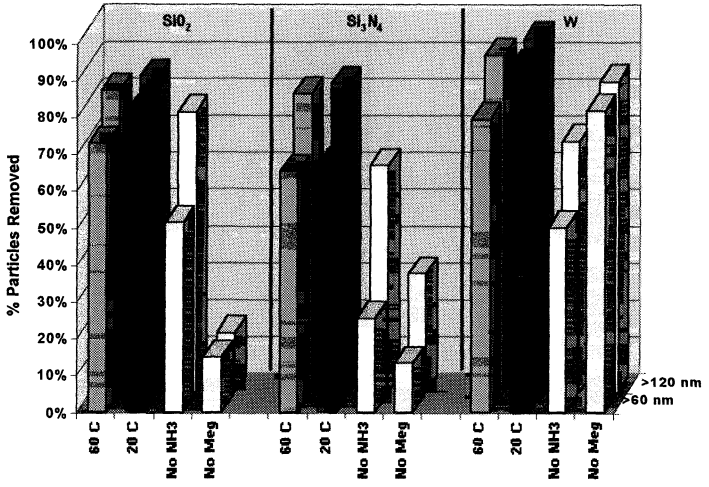


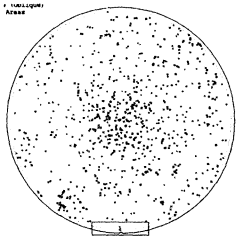
Figure 3. Particle removal efficiencies for dry-deposited particles.

All particle types showed a significant decrease in particle removal in the absence of NH_3 (Run 3). Particle maps of the monitor and SiO_2 particle wafers for Run 3 are given in Figure 4. Prior to processing, there were approximately 817 particles randomly distributed on the monitor wafer, while the SiO2 wafer had over 80% of its 25,510 particles evenly distributed within a half radius distance from the center of the wafer. After processing, both wafers had the same order of magnitude of particles, as each other, evenly distributed across their entire surfaces. These results suggest that the megasonic energy detached a large number of the surface-bound particles. The particles then entered a well-mixed chamber where a large number then re-deposited on all wafer surfaces. These results are consistent with those previously reported by Li, et al. (9).

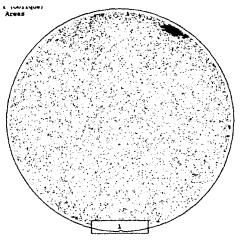
Without megasonic energy, the SiO_2 and Si_3N_4 particle removal efficiencies were significantly lowered. W particles were also detrimentally affected but to a much lesser degree. This is a surprising result since one would expect the W particles to be effected more than the SiO_2 and Si_3N_4 particles because W has a larger van der Waal's attraction force than the other particle types.

Results from the Screening Experiments suggest that this ultra-dilute ammonium hydroxide + megasonic process relies on the megasonic energy to detach surface-bound

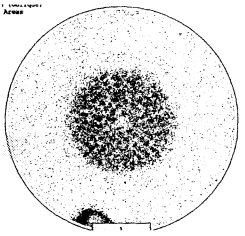
particles and the high pH of the ammonium hydroxide solution prevents their reattachment.



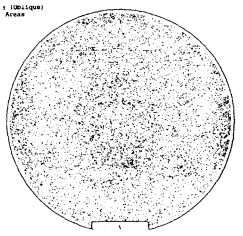
Monitor wafer before clean without NH_3
Defects: 817 @ > 60 nm; 34 @ > 120 nm



Monitor wafer after clean without NH_3
Defects: 11,459 @ > 60 nm; 2,167 @ > 120 nm



SiO_2 Particle wafer before clean without NH_3
Defects: 25,510 @ > 60 nm; 14,539 @ > 120 nm



SiO_2 article wafer after clean without NH_3
Defects: 14,464 @ > 60 nm; 3,585 @ > 120 nm

Figure 4. Particle maps of the monitor wafer and SiO_2 particle wafer before and after processing without the presence of ammonia (Run 3).

Process Performance Demonstration Results

Every wafer tested had a significant number of its particles removed. The entire population had a > 99% particle removal efficiency as seen in Figure 5. The prime monitor wafers with 150 particles per wafer had 20% to 50% of their particles removed. The intentionally contaminated wafers with 3,000 to 4,000 nitride particles, as well as the particle monitor wafers with 5,000 to 60,000 particles each, typically had > 99% of their particles removed.

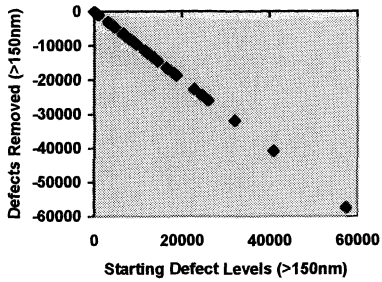


Figure 5. Particle removal by ultradilute ammonium hydroxide.

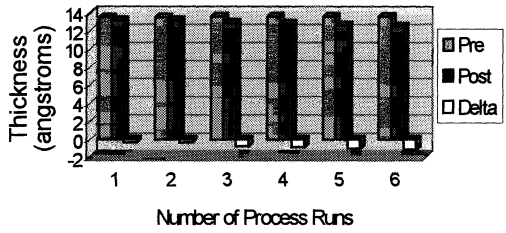


Figure 6. Native oxide loss from six consecutive room temperature YP-1 process runs.

After six process runs (room temperature, 110 ppm NH_3 and 450 W megasonic energy) ~ 1 Å of the native oxide was removed (Figure 6). The native oxide etch data suggests that very little etching, if any, is required for this particle removal process. A single process run at 60°C can remove as much as 7 Å of native oxide.

Surface roughening experiments were conducted on prime wafers by subjecting them to repetitive cycles of the cleaning process. After a single cleaning cycle the wafers remained hydrophobic. Figure 7 shows RMS, Ra and Rmax values actually decreased. These results, along with those of Figure 6, show that the cleaning process did not breach the native oxide layer and a smooth surface was maintained. However, if too many cleaning cycles are performed, the native oxide will eventually etch away and result in attack of the underlying silicon surface.

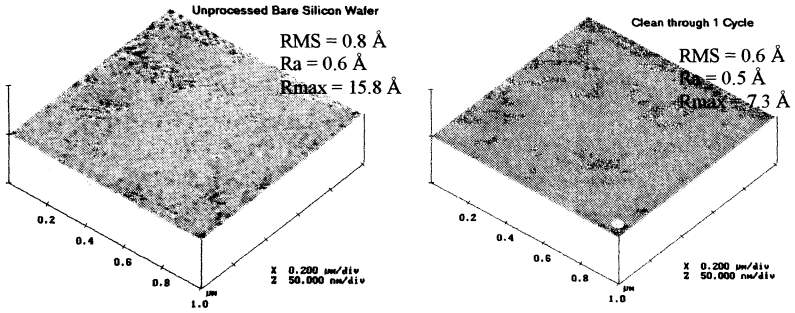


Figure 7. AFM characteristics before and after cleaning.

Metallic contamination tests were conducted by performing TXRF measurements on one prime wafer before and after processing. The results, given in Figure 8, shows that no metallic contamination was detected on the wafer either before or after cleaning.

		K	Ca	Ti	Cr	Mn	Fe	Ni	Cu	Zn
Pre Clean	Cen.	<9	<6	<3	<1.5	<1.3	<1.1	<0.9	<0.7	<1.4
	Mid.	<7	<4	<5	<1.1	<1.0	<0.8	<0.7	<0.6	<0.8
	Bot.	<7	<6	<4	<1.5	<1.3	<1.1	<0.9	<0.8	<1.0
Post Clean	Cen.	<9	<6	<4	<1.5	<1.3	<1.1	<0.9	<0.8	<1.3
	Mid.	<7	<5	<2	<1.2	<1.0	<0.9	<0.7	<0.6	<0.8
	Bot.	<7	<5	<5	<1.5	<1.3	<1.1	<0.9	<0.8	<1.0

Figure 8. TXRF results before and after cleaning expressed as 10^{10} atoms/cm^2.

CONCLUSIONS

A new process (denoted "YP-1") has been developed as an alternative to the traditional SC-1 cleaning process. In contrast to the SC-1 process, the YP-1 process relies to a much lesser extent on surface etching to effect particle removal. Particle detachment occurs primarily by megasonic energy and the prevention of particle reattachment by the presence of ultradilute ammonium hydroxide. This new process has essentially no chemical cost except that of the DI water, ammonia gas and nitrogen gas. It is very efficient at removing particle contamination while not roughening the surface or depositing metallic contamination.

ACKNOWLEDGMENTS

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PHOTORESIST STRIPPING AND POLYMER REMOVAL

THE EFFECT OF TEMPERATURE ON AN OZONATED WATER PHOTORESIST STRIP PROCESS

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The effect of temperature on removal of two I-line photoresists from silicon wafers using ozonated DI water in a spray processor is investigated. It is observed that, with all other parameters being constant, higher temperatures result in faster removal of photoresist. Over the temperature range 21° Celsius to 46° Celsius, the data follows an Arrhenius relationship. The activation energy of I-line photoresist removal using ozonated water is calculated to be 0.17-eV. Both I-line resist are found to have the same activation energy for removal with DIO_3. This activation energy is to low to be accounted for by the effect of temperature contributing to the breaking of chemical bonds in the resist, which takes about 1-eV of energy. We will discuss several possible explanations for the low activation energy.

INTRODUCTION

We have shown that the removal of photoresist from one wafer at a time by ozonated water (DIO_3) is limited by diffusion of ozone (O_3) to the resist surface (1,2). This phenomenon occurs for two reasons. First of all, O_3 is a metastable molecule and has a fast reaction rate with some bonds in the photoresist. Secondly, the concentration of O_3 that can be dissolved in DI water is between 10-ppm and 100-ppm, a very low value. The rate limiting step of a multiple wafer system used in these experiments may be different.

Matthews has reported achieving faster resist removal rates at DI water temperatures below room temperature in an immersion system (3). As with most gases, at reduced water temperatures the solubility of O_3 in the water is increased. Matthews reports achieving DIO_3 concentrations of 70-ppm to 100-ppm at temperatures down to 5° Celsius. The higher DIO_3 concentration results in faster photoresist removal. However, in an immersion system the effects of temperature and O_3 concentration are not independent so it is not possible to process at high temperatures and high DIO_3 concentrations at the same time.

Oya et. al. have reported an activation energy for photoresist removal with DIO_3 in an immersion system of 0.28-eV (4). However because the DIO_3 concentration in the bath were not be held constant as the temperature changed they have assumed a direct proportionality between DIO_3 concentration and resist removal rate in the calculation of their activation energy. They argue that based on the activation energy of photoresist removal with DIO_3, sub-ambient temperatures may not be the optimal conditions for removing resist in a bath.

EXPERIMENT

200-mm diameter silicon wafers were coated with resist and hardbaked. One resist used was TOK-3450 with an average initial thickness of 7460-Å. The manufacturer of the other I-line resist is not known, we will refer to it simply as generic I-line resist. This generic I-line resist had an average initial thickness of 9965-Å. The resist thickness was measured on a Rudolph Caliber 300 ellipsometer which uses a HeNe laser and IR laser. The standard optical constants, for both resists and the substrate, from the systems database were used. Forty-nine point measurements with a 5-mm edge exclusion were made over the wafer surface. Because of increased noise in the measurement of the resist thickness after DIO_3 processing these measurements were taken twice and the average of the two measurements at each point was used.

High concentration DIO_3 is generated by contacting high concentration O_3 gas with room temperature (21.5° Celsius) DI water at a pressure of 2.5-bar gauge (36.3-psig). Because the DIO_3 is produced under pressure, the solubility of O_3 in the water is increased. The concentration of the DIO_3 is controlled by the ozone generator system to 60-ppm.

Wafers were processed in an FSI MERCURY® MP Surface Conditioning System. This system can process one-hundred 200-mm wafers at a time. Resist coated wafers were placed in slot 5 of a cassette in the system with all other slots containing a bare silicon wafer. DIO_3 was dispensed at a flow rate of 15-liters/minute from the center spraypost onto the wafers from specially designed nozzles to maintain the maximum concentration of O_3 in water. In addition to the flow of DIO_3, DI water of various temperatures was dispensed from a different set of holes in the spraypost onto the wafers. The flow of this water was 7.6-liters/minute and the temperature can be changed from 21.5° Celsius up to 95° Celsius. The resulting temperature of the co-dispensed DIO_3 and hot DI water onto the wafer surface was calculated based on the flow rates and temperatures of the two components. Experiments were done at both 3-minute and 10-minute DIO_3 dispense times. The turntable and wafers were rotated at 500-rpm during the DIO_3 dispense to achieve efficient diffusion of the O_3 to the resist surface.

RESULTS

All experiments in this report used a co-dispense of 15-liters/minute DIO_3 flow at 21.5° Celsius and 7.6-liters/minute DI water flow at temperatures from 21.5° Celsius up to 95° Celsius. Because the mixing of the DIO_3 and hot DI water occurs on the surface of the wafers, effects of higher temperatures on O_3, such as decomposition and lower solubility, were ignored because they occur on a time scale much longer than the time that the DIO_3 is on the wafer surface. Because the experimental conditions for the different tests have the same flow and the same DIO_3 concentration on the wafer surface with only the temperature changing no assumptions are needed in the analysis of the activation energy of DIO_3 in removing photoresist. Using this co-dispense method, both high temperatures and high O_3 concentrations can be achieved at the same time.

Figure 1 shows the effect of DIO_3 dispense time on the generic I-line resist thickness, when subjected to a co-dispense of DIO_3 and hot DI water with the DI water heater

temperature set at 95° Celsius. Figure 2 shows the effect of DIO_3 dispense time on the TOK-3450 resist thickness, when subjected to a co-dispense of DIO_3 and hot DI water with the DI water heater temperature set at 95° Celsius. The curve labeled "Average (49)" is the average of all 49 points measuring the resist remaining on the wafer surface. The curve labeled "Maximum (5)" is the average of the five thickest places on the wafer, which would be at the side farthest from the spraypost. The curve labeled "Minimum (5)" is the average of the five thinnest places on the wafer, which would be at the side closest to the spraypost. Because the DIO_3 first comes into contact with the photoresist at the side of the wafer closest to the spraypost, the resist is removed more quickly here. The curve labeled "Maximum (5)" shows an initially slow removal rate that increases after the initially steep "Minimum (5)" curve has flattened out, illustrating the fact that the resist farthest from the spraypost is not aggressively attacked until the resist closest to the spraypost has been removed. Over a short period of time, when the resist has not been completely removed from any part of the wafer, the resist removal as a function of time should be the most linear and give the most accurate answer for the activation energy. Using data from a longer dispense time could give inaccurate values for the activation energy because of the complication of the resist removal not being linear with time. Comparison of the activation energy for different resists when processed for a longer period of time will be valid. Because the goal of the process is to eventually remove all the resist, the activation energy over a longer period of time is important for understanding and improving the process.

Figure 3 shows an Arrhenius plot for the generic I-line resist using a 3-minute co-dispense of DIO_3 and DI water at temperatures of 21.5° Celsius and 95° Celsius. Four resist wafers were processed at each temperature. The error bars represent the one-sigma standard deviation of the data. The effect of the temperature on the resist removal rate and the calculation of the activation energy is statistically significant. The activation energy is calculated from these curves to be 0.17-eV. The Arrhenius equation is given in Equation 1 where k is Boltzmann's constant, T is the temperature in Kelvin, Ea is the activation energy, R is the removal rate, and A is a rate constant.

$$R = Ae^{-(Ea/kT)} \qquad [1]$$

Figure 4 shows the average thickness of the generic I-line resist and the TOK-3450 resist remaining on the wafers after a 10-minute co-dispense of DIO_3 and DI water at six temperatures from 21.5° Celsius up to 95° Celsius. With all other parameters held constant, more resist is removed as the temperature increases meaning that the resist removal rate is faster with increasing temperature.

Figure 5 shows an Arrhenius plot for the generic I-line resist and the TOK-3450 resist using a 10-minute co-dispense of DIO_3 and DI water at six temperatures from 21.5° Celsius up to 95° Celsius. Given the noise in the data that is plotted in figure 3, only a single straight line fit to this data is statistically significant. For the longer dispense, the calculated activation energy is 0.05-eV for the generic I-line resist, which is even lower than the activation energy for the 3-minute DIO_3 dispense. The activation energy for the TOK-3450 resist for the 10-minute dispense is 0.06-eV, essentially the same as the activation energy of the generic I-line resist.

Compared with a process using only room temperature DIO_3, the increase in temperature as a result of co-dispense of hot DI water results in an increase in resist removal. The average resist removal rate of four different resists is shown in figure 6 using a 5-minute dispense time. The room temperature process was a dispense of only DIO_3 at 15-liters/minute 60-ppm. The hot process was a co-dispense of DIO_3 and hot DI water resulting in an on-wafer temperature of 46° Celsius. Because in each test the hot process removes the resist more quickly, the effect on the resist removal process from the additional thermal energy is stronger than the effect of O_3 concentration dilution that the additional flow of unozonated water introduces. Even though the additional hot DI water dilutes the O_3 concentration, the amount of O_3 getting onto the wafer surface as measured in moles or grams will be the same in both processes. It is possible that in the 100 wafer system the resist removal is limited by the amount of O_3 on each wafer because the O_3 is divided onto 100 wafers.

DISCUSSION

Two effects observed in our data need to be explained. First, the activation energy for photoresist removal with DIO_3 is low compared with the energy required to break chemical bonds in the resist. Second, higher temperatures increase the removal of resist by a significant amount. Three theories are presented to explain these observations.

First, the low activation energy could simply mean that the removal of large amounts of organic material from a surface with DIO_3 is rate limited by diffusion, even in the multiple wafer system used for these tests. In a mass transfer controlled process, the biggest effect of temperature is on the diffusion coefficient, which in liquids increases proportional to T in Kelvin (5). The effect on the mass transfer rate by increasing the temperature is not sufficient to account for the increase in the resist removal rate. This does not means that the process is not mass transfer limited, only that the increased resist removal rate by increasing the temperature is not due to changing the mass transfer.

A second possible explanation is that OH radicals ($OH^{\cdot}$) are formed as an intermediary step in the attack of the photoresist. Because the $OH^{\cdot}$ are highly reactive, the activation energy will be low. In this case, an increase in the temperature would increase the resist removal rate by increasing the rate of the intermediary reaction $O_3 \rightarrow OH^{\cdot}$.

A third possibility is that resist removal does not require complete oxidation of the resist but only requires that the oxidation proceeds to render the organic water soluble. At higher temperatures, larger molecules of the organic resist will become water soluble, so more resist will be removed for every O_3 molecule that reacts at the wafer surface. For example if at 21.5° Celsius an organic molecule that is C_x large is removed from the wafer surface, then at 46° Celsius and organic molecule that is $C_{1.6x}$ large being removed would fit out removal rate data.

CONCLUSIONS

The method of co-dispensing DIO_3 and hot DI water from different nozzles of a spraypost in a spray processor allows both high temperatures and high O_3 concentrations to be achieved at the same time. Over the temperature range 21° Celsius to 46° Celsius, the resist removal rate follows an Arrhenius relationship within the noise of the measurement. The activation energy of the generic I-line photoresist removal using a 3-minute dispense of DIO_3 is calculated from the data to be 0.17-eV. The activation energy for removal of TOK-3450 resist is found to be the same as for the generic I-line resist for a 10 minute DIO_3 dispense. Compared with a process using only room temperature DIO_3, the increase in temperature as a result of co-dispense of hot DI water results in an increase in resist removal.

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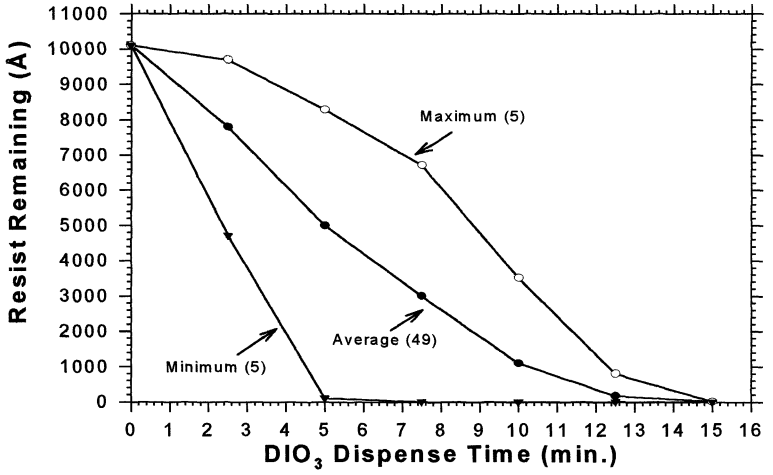

Figure 1: Time behavior of removing the generic I-line resist with DIO_3 and hot DI water at 95° Celsius. Average (49)" shows the average of all 49 points on the wafer. "Maximum (5)" shows the 5 thickest places on the wafer. "Minimum (5)" shows the 5 thinnest places on the wafer.

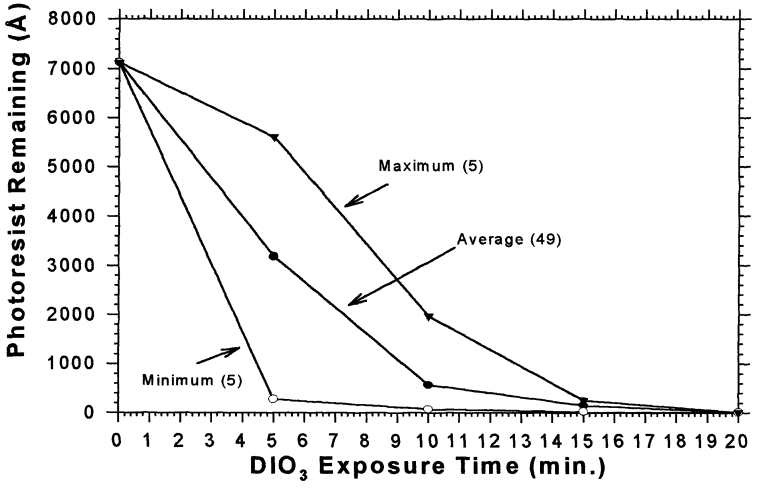

Figure 2: Time behavior of removing TOK-3450 resist with DIO_3 and hot DI water at 95° Celsius. Average (49)" shows the average of all 49 points on the wafer. "Maximum (5)" shows the 5 thickest places on the wafer. "Minimum (5)" shows the 5 thinnest places on the wafer.

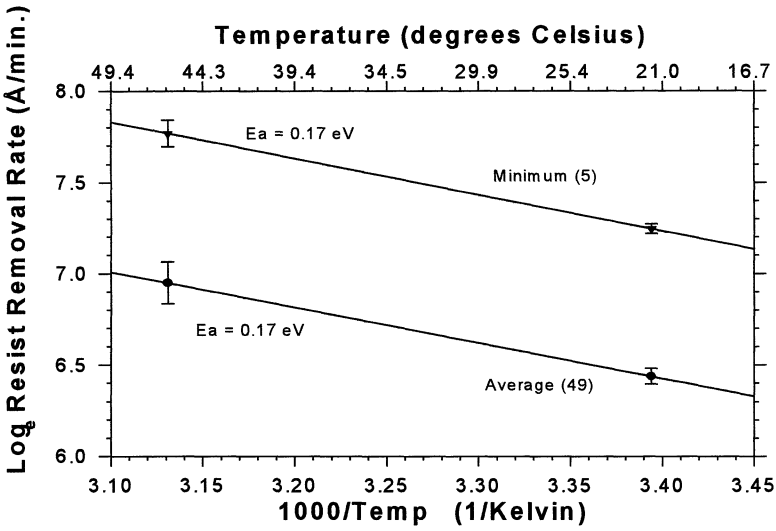

Figure 3: Arrhenius plot of the generic I-line resist removal using 3 minute co-dispense of DIO_3 and DI or various temperatures.

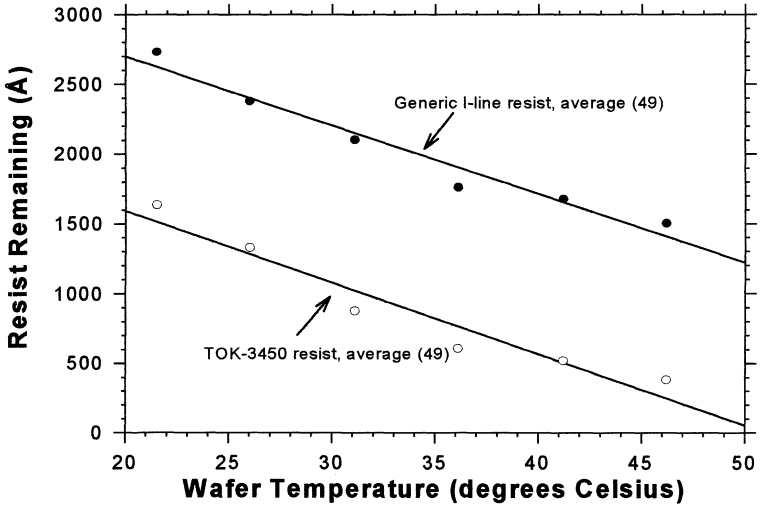

Figure 4: Average amount of photoresist remaining after 10 minute co-dispense of DIO_3 and DI of various temperatures.

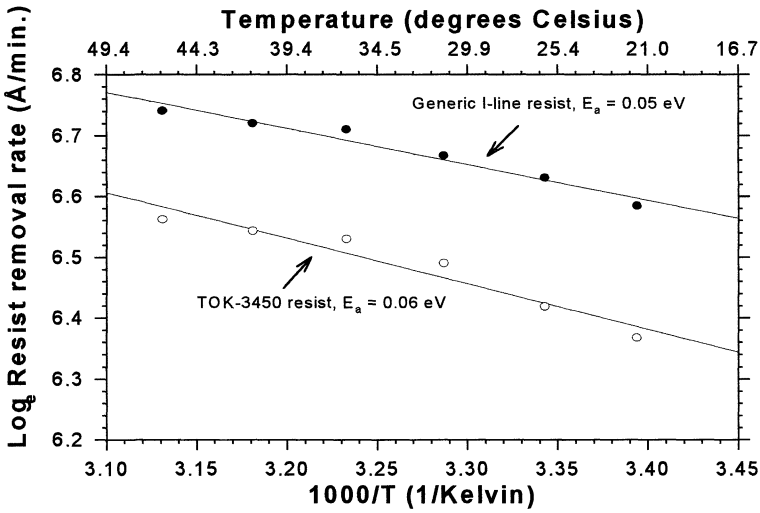

Figure 5: Arrhenius plot of the generic I-line resist and TOK-3450 resist removal using 10 minute co-dispense of DIO_3 and DI or various temperatures.

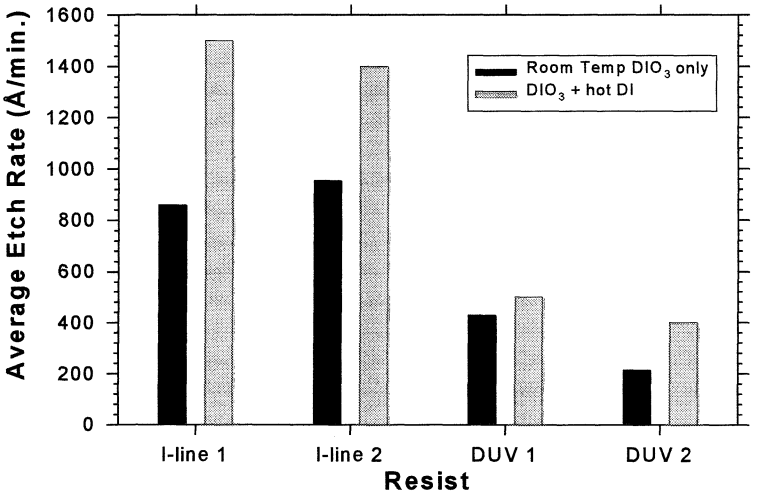

Figure 6: Comparison of room temperature DIO_3 only dispense with co-dispense of DIO_3 and DI water at 95° Celsius using a five minute dispense on four different resists.

Integrated Aqueous/Ozone Process for Plasma Etch Residue and Photoresist Removal

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Abstract
A completely aqueous process for the removal of post plasma etch and photoresist residues combines Arch Chemicals Microstrip 5002 with an ambient temperature, boundary layer ozone/DI water rinse. The integrated process, called MicrOzone, is designed to follow a downstream oxygen ash process for photoresist removal and is implemented in a Semitool Spray Solvent Tool. This process was tested on post via etch and post metal etch device structures. Microstrip 5002 effectively removes post plasma etch residue, but has no resist removal capability. The results demonstrate that the ambient temperature and boundary layer ozone/DI water rinse process offers efficient removal rates for post plasma etch and ash residues with no damage to devices for both via and metal levels. Advantages of this integrated process include improved process margin against incomplete photoresist ashing, reduced environmental impact, and both reduced costs and enhanced throughput, from the elimination of organic solvent intermediate rinse requirements and from the elimination of special disposal requirements.

Introduction
A completely aqueous backend cleaning process for post plasma etch residue and photoresist residue removal has been investigated as a replacement for a hydroxylamine based organic solvent cleaning process. This process, called MicrOzone, consists of an aqueous residue cleaning step, followed by an ambient ozone/DI water rinse step. This process has been evaluated in a Semitool Spray Solvent Tool (SST) specifically configured for ozone applications. Empirical data demonstrates MicrOzone to remove resist, exposed to typical plasma and ash processes, at rates allowing for the design and integration into a manufacturing process flow. The data also shows effective removal of both post via etch and post metal etch residues.

Prior investigations for contact via and metal layers were performed at an elevated process temperature of 95°C. Complete removal of photoresist residue at via and metal layers (>2K Å) was demonstrated with electrical measurements indicating no damage to via device structures. However, critical dimension (CD) results indicated that there was a slight CD loss at this process temperature. [1]

The objective of this investigation was to demonstrate the effectiveness of an ambient ozone/DI water process at photoresist removal without attack of metal or significant CD reduction. Comprehensive physical and electrical characterization data demonstrating manufacturing feasibility of this low cost process is presented.

Cleaning Chemistries
Traditional hydroxylamine/organic solvent residue cleaning chemistries are highly alkaline and can result in corrosion of Al-Cu interconnects in the presence of water. This requires the use of an intermediate solvent rinse to neutralize pH prior to contact with water. This intermediate rinse step, typically isopropyl alcohol (IPA), is placed between the residue removal and the DI water rinse steps. Both the organic solvent cleaner and the intermediate rinse chemistry must be captured for disposal.

MicrOzone integrates Microstrip 5002 at 65°C and an ambient boundary layer ozone/DI water rinse. Microstrip 5002, which contains hydroxyl ammonium sulfate and tetra-methyl ammonium hydroxide, is a

slightly acidic buffered solution. Therefore, it does not require an intermediate rinse step prior to the final DI water rinse. All wastes can be disposed of in acid-neutralized waste water streams.

Microstrip 5002 is designed for post plasma etch residue cleaning. The removal of etch residues is possible due to the hydrogen ion contained in Microstrip 5002. The hydrogen ion cleaves Al-O-Al bonds, rendering residues containing these bonds soluble in the chemical solution. Ozone and DI water processes are highly investigated cleaning methods for the removal of organics from wafer surfaces. The most common, being ozone dissolved into DI water. Two possible reaction mechanisms are:

(1) $-C- + 2O_3 \rightarrow CO_2 + 2O_2$
(2) $-CH_2- + 3O_3 \rightarrow CO_2 + 3O_2 + H_2O$

The solubility limits for ozone in DI water establish reaction rates that are impractical for bulk removal of organic resists or contaminants. Also, transport of ozone through the water, which is the carrier media for the active species $+O_3$, is inefficient and further slows the reaction rate.

MicrOzone incorporates a simple and very unique method to deliver O_3 to the wafer surface called the boundary layer method. [2] The boundary layer method uses the spin speed and DI water flow parameters of the SST to set up a thin and uniform layer of water on the wafer surfaces. Ozone is then simply introduced as a gas into the process chamber. The ozone can be transported more efficiently and with greater concentration through the thin water layer. Reactants are shed off the wafer surface with the constantly replenished water layer. This technique largely eliminates the process restrictions imposed by the limited solubility of ozone in water. The limitation is no longer one of solubility, but of diffusion rate. The diffusion rate is a function of the temperature of solution, the thickness of the boundary layer, which is also the diffusion barrier, and the concentration gradient across the boundary layer. Increasing the ozone gas concentration creates more of a gradient and hence, provides the driving force for diffusion. Elevated temperature will increase the reaction kinetics with no adverse impact from decreasing gas solubility with temperature.

Experimental Approach

Evaluation was done using emulator wafers from which via resistance, metal line-width data, and probe yield data could be obtained. Wafers from the same lots were used to obtain SEM characterization of the process. The via emulator lot, X9848834, was processed up to both post via1 and top via etch resist strip and the metal emulator lot, X9847841 was processed up to post top metal etch resist strip at which point the processing summarized in Table 1 was performed. Partially ashed wafers were included to demonstrate the ability of ozone at resist removal. Fully ashed wafers were included to investigate the impact of ozone exposure on via resistance, metal CD's, and yield in normal process conditions.

Table 1: Experimental runs for post etch polymer and resist strip removal

Wafer	Etch	Ash	Residue Clean	Ozone/DI	Figure
X9848834-4,13	Via1	50%	None	No	
X9848834-1,2,3	Via1	100%	Standard	No	
X9848834-14,15,16,18	Via1	50%	Standard	No	
X9848834-5,6,7	Via1	100%	MS5002	No	
X9848834-9,10,11	Via1	100%	MS5002	Yes	
X9848834-19,20,21,24	Via1	50%	MS5002	Yes	
X9848834-8	Tvia	50%	None	No	Fig. 1(a), (b)
X9848834-1,2,3	Tvia	100%	Standard	No	
X9848834-12,17	Tvia	50%	Standard	No	Fig. 1(c)
X9848834-5,6,7	Tvia	100%	MS5002	No	
X9848834-9,10,11	Tvia	100%	MS5002	Yes	
X9848834-22,23	Tvia	50%	MS5002	Yes	Fig. 1(d), (e)
X9849841-16	Metal	50%	None	No	Fig. 1(f)
X9849841-7,8,9	Metal	100%	Standard	No	
X9849841-17,18,19,20	Metal	50%	Standard	No	Fig. 1(g)
X9849841-10,11,12	Metal	100%	MS5002	No	
X9849841-13,14,15	Metal	100%	MS5002	Yes	
X9849841-21,22,23,24	Metal	50%	MS5002	Yes	Fig. 1(h)

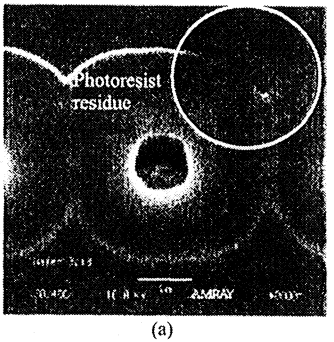
The vias were etched in a single wafer reactive ion etcher (RIE) through 1.2 to 1.5 microns of plasma enhanced chemical vapour deposited (PECVD) tetra-ethyl-ortho-siloxane (TEOS) as the inter-metal-dielectric on a metal stack of tungsten. Following the etch, the wafers were ashed in downstream oxygen at an approximate wafer temperature of 250°C. The 2-micron metal stack, which consists of a TiN anti-reflective coating (arc) on TiN/Al-Cu deposited on TEOS, was etched in an RIE batch processor and ashed in downstream oxygen at an approximate wafer temperature of 250°C. Partial ash consists of ashing for half the time of the regular production recipe.

The standard residue strip process is a hydroxylamine chemistry followed by an intermediate IPA rinse prior to a DI rinse and spin dry. The wafers receiving the proposed MicrOzone process were exposed to Microstrip 5002 at 65°C for 15 minutes followed by ozone/DI at room temperature for 1 minute at low speed and 13 minutes at high speed followed by a spin dry.

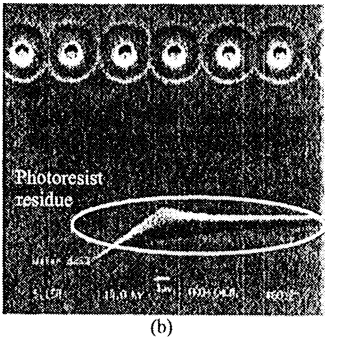
Results and Discussion

SEM photographs were taken at both the via1 and top via levels. However, to demonstrate the ability of the ozone resist removal, the top via level, with 50% of the standard ash time, was selected due to greater quantities of photoresist residues remaining at this process step.

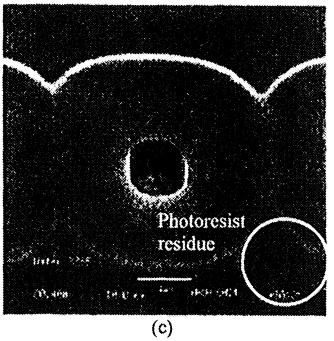
Figures 1(a) through (h) show the SEM results for the process conditions summarized in Table 1.



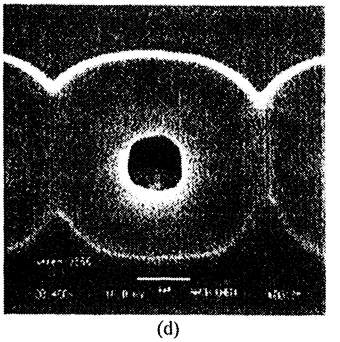
(a)



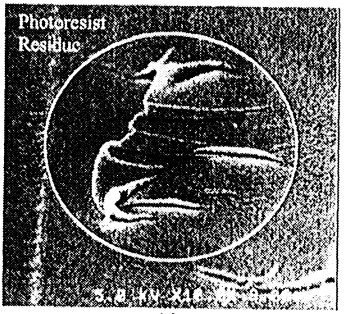
(b)



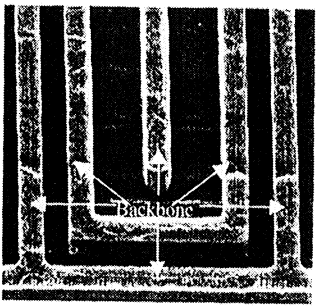
(c)



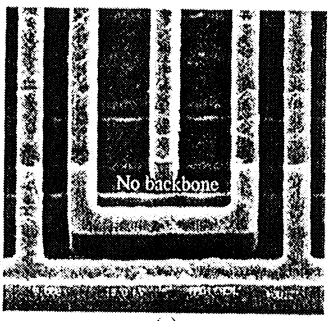
(d)



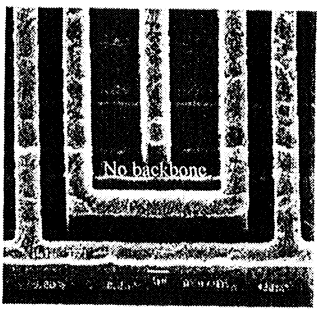
(e)



(f)



(g)



(h)

SEM analysis of the top via layer was done for several lots including the emulator lot. Figures 1(a) and (b) are representative of the typical amount of un-ashed resist seen on all of these wafers. SEM cross-section revealed that the thickness of the resist before residue strip was ~5000 Å, (range = 7000 Å). After the standard polymer removal process, the wafers were relatively clean with minute traces of resist remaining as shown in Figure 1(c). After the MicrOzone process, the vias sampled for SEM were clean as shown in Figure 1(d); however, there were trace amounts of resist seen in the field as shown in Figure 1(e). SEM cross-section of the wafers cleaned with both the standard process and the MicrOzone process revealed that the thickness of resist remaining was ~1120 Å and ~840 Å respectively.

The partially ashed wafers from the emulator lot at the top via level cleaned with the MicrOzone process demonstrated substantial resist removal rates; however, not all the resist was removed. This indicates that a longer time is necessary at the ozone/DI process step for this level. Therefore, the remaining wafers at top via intended for 50% ash were processed at 100% ash so that the electrical and yield data could still be obtained for the via1 level. Electrical and yield data is only provided for the top via level for fully ashed conditions demonstrating the impact from ozone exposure for normal conditions.

Resist residue was not observed at the top metal level after 50% ash as shown in Figure 1(f). The SEM image, however, does show the post plasma etch polymer "backbone" that results from the top metal etch process. It is demonstrated that both the standard and the MicrOzone processes remove the polymer "backbone" in Figures 1(g) and (h). Physical characterization by SEM analysis confirms that wafers cleaned with MicrOzone after metal etch are indistinguishable from wafers in the same lot processed with the standard post metal etch residue clean. Therefore, damage to the metal structures from the MicrOzone process is not indicated.

Figures 2 and 3 show graphically the impact on via resistance for the via1 and top via levels (50% ash omitted for the top via level). Via resistance measurements were obtained by full wafer testing 95 sites per

wafer. Via resistance specifications for via1 and top via are 0.8+/-0.5 ohms/cm^2 and 0.9+/-0.6 ohms/cm^2 respectively. Via resistances for both the via1 and top via levels are well within specification for all resist strip cases. The results for the Microstrip 5002 process and the MicrOzone process do not vary significantly from the standard process. Clearly the MicrOzone process does not electrically damage the vias.

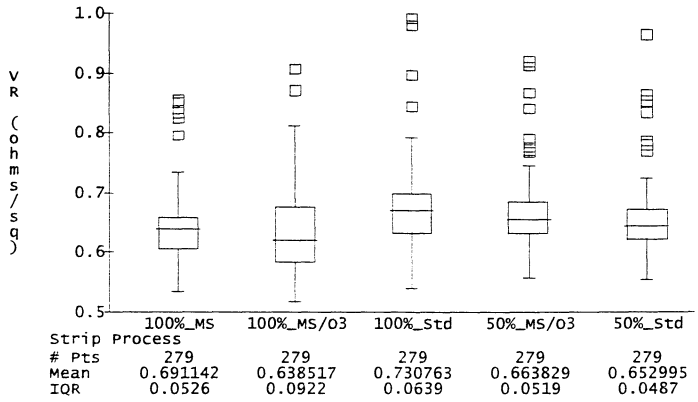


Fig. 2 Via1 resistance results for various resist strip processes

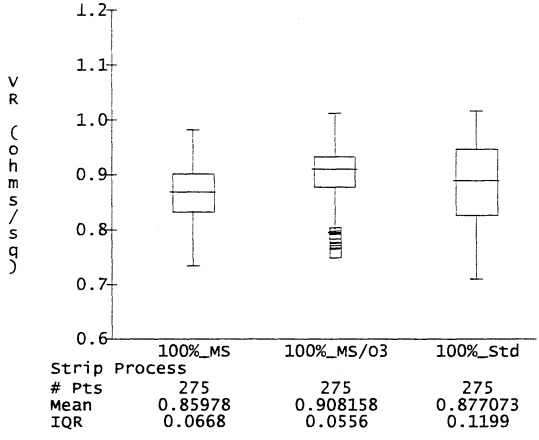


Fig. 3 Top via resistance results for the various resist strip processes

Figure 4 shows the line-width data for the standard process, the Microstrip process, and the MicrOzone process. The CD measurements were obtained from 5 sites per wafer, on all portions of the wafer. CD results for X9849841-17,18,19, and 21,22,23 are not available due to a processing failure. The specification for the top metal line-width is 1.2 +/- 0.4 microns. The CD results for the MicrOzone process are comparable to those for the standard process. These results indicate that the MicrOzone process and the Microstrip process do not cause line-width loss.

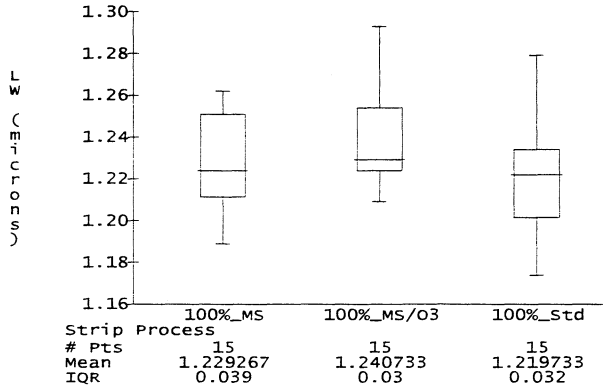


Fig. 4 Line-width results for the various resist strip processes

Wafers from both lots X9838834 and X9849841 were further processed and tested for wafer yield. The results for the via emulator lot are shown in Figure 5. Each box represents the yield results for one wafer. Results for the metal emulator lot were unavailable. It is noted that a higher yield was obtained for wafers processed with MicrOzone than for the standard process of record. It is further noted that there is no significant difference in the yield results for wafers processed with Microstrip 5002 compared to the standard process. Also interesting, is that a higher mean yield was observed for both of the splits processed with the non-standard ash process (50% ash).

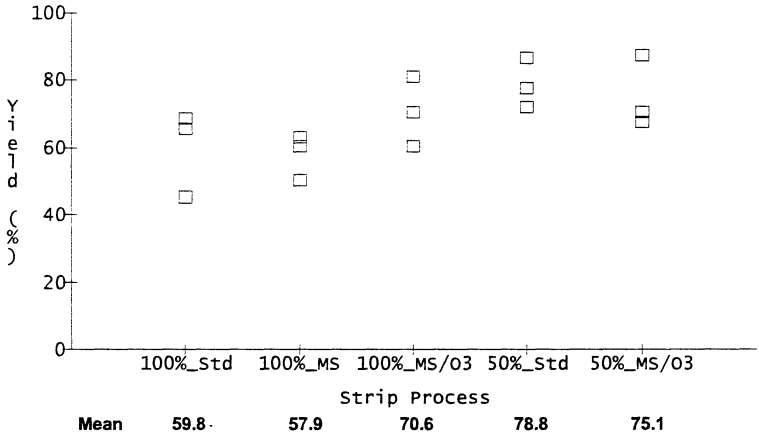


Fig. 5 Probe yield data for via emulator lot at various resist strip processes

Conclusions

The proposed MicrOzone process consisting of the integration of Microstrip 5002 and an ambient temperature ozone/DI process in a Semitool SST, was successfully demonstrated. The MicrOzone process as tested was effective for resist removal operating at ambient DI water temperature at both via and metal levels and is safe for post via etch processing and post metal etch processing. Increasing the ozone process time to guardband against the variability in the ash process would not be favorable, however, increasing the photoresist etch rate of the ozone/DI portion of the process would be advantageous. This would shorten the MicrOzone process cycle and enhance the process margin against incomplete resist removal. Further work will investigate increased ozone concentrations with the use of a higher output ozone generator, and the effects to post plasma photoresist residue etch rates, via resistance, and metal damage.

References:

[1] W. Kleemeier, et al., Solid State Phenomena, Vols. 65-66, 143-152 (1999)
[2] E. Bergman, et. al., MRS 1999 Spring Meeting Abstracts, 262 (1999)

APPLICATION OF MOIST OZONE GAS PHASE FOR REMOVAL OF RESIST AND ORGANIC CONTAMINATION IN A NOVEL TANK TYPE PROCESSOR

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Abstract: The use of ozone dissolved in ultrapure de-ionized water for the removal of photo resist has been found to be less effective than sulfuric acid based processes. To overcome the main detractor, the low concentration of ozone at the wafer surface the application of ozone in a moist atmosphere has been studied in order to define and characterize the efficiency of resist removal in a wet process tank environment. Basic dependencies of temperature, ozone concentration and humidity were evaluated, as well as the impact of rinse steps during and after the ozone treatment. It was shown that strip rates of > 300 nm/min for typical types of photo resists after various conditions can be achieved and a complete resist removal process including UPW rinse of less than 10 min is possible in wet bench applications. CoO reduction of 10 – 20% are achieved compared to sulphuric based strip processes.

INTRODUCTION

The removal of organic contamination and photo resist with sulphuric acid based mixtures in today's S/C processing is a well established but expensive process step. Replacing the peroxide in the SPM (Piranha-) mixture by ozone has shown comparable results for organic contamination, however for resists strip the long recovery time of the bath after the strip in unsatisfactory [1,2]. As a low cost alternative dissolved ozone in UPW has been investigated for both cleaning of organic contamination including post ash flakes and photo resist removal. While principal feasibility could be shown in a wide range of temperatures due to the limited solubility of ozone in de-ionized water the removal rate and repeatability especially for pre treated (i.e. baked and/or implanted) resist was significantly worse than the SOM or SPM alternatives. Even at sub-ambient temperatures the maximum solubility ozone is in the order of 100 PPM only and cannot overcome the loss in reaction speed [3]. High temperature applications are even more inefficient, since hardly any ozone can be solved at 70° C or more. One proven [4,5] possibility of using ozone for resist strip is to provide the oxidator in a moist atmosphere at elevated temperatures. While hydroxyl ions seem to be necessary to initiate the reaction the reduced or missing boundary layer at the wafer surface in a vapor will provide ozone concentrations in the percentage range directly to the resist surface even at higher temperatures. Removal rates of >300 nm/min in simple tank like setups have been shown as well as in spray processors [6].

This work is focussing on the application of moist ozone processes in a tank module that is compatible with conventional or reduced bath wet equipment. An immersion tank processor was designed , in which the controlled moist ozone environment could be setup and optimized with respect to the critical parameters for resist stripping. The goal was to prove the feasibility of using immersion type tanks for resist stripping without sul-

phuric acid within at least the cycle time of typical SPM or SOM processes, and characterize the full process window for baked, hardened and implanted resist for full batch processing. The targeted module design should be upgradable or even compatible with existing module for Piranha or SOM strip and provide the same or better process stability. Finally the effect of rinsing in the same module, as integrated part or after the process is not yet well characterized. Since this might have a huge impact on the practical use of the technology, this was included in the study as well.

EXPERIMENTAL PROCEDURE

The experimental work was performed in two main phases: The principal process conditions for resist stripping in a moist ozone atmosphere in a process tank were evaluated at the interuniversity microelectronic centre (IMEC) in Leuven, Belgium, using a PVDF tank suitable for 150 mm wafers. The tank was closed, but not sealed with a lid and connected to hot and cold de-ionized water supply. A schematics of the setup is shown in Fig. 1. The ozone was provided by an ASTEX-SORBIOS ozone generator and either directly supplied to the process tank or bubbled through an external vessel, containing boiling UPW. The ozonized vapor was transferred through a flow control valve into the tank. Additionally pure nitrogen gas could also be introduced for controlled gas transfer of the atmosphere. The temperature in the tank was adjusted by the incoming hot vapor and heated tank walls. The resist coated wafers were placed into the empty tank before the ozone and/or vapor was supplied and remained in this special atmosphere between 2 and 10 minutes. Optionally the tank could be used at the end of the rinse process as an cascade to rinse the wafers after the moist ozone treatment.

In a second phase the results of the feasibility study were transferred to a production capable batch module for 200 mm wafers. This setup used a vessel similar to the one described above for the vapor supply, additional gaseous ozone and nitrogen lines as well as a controllable exhaust line. The temperature control in the process area is achieved with indirect water heating surrounding the process from all sides, which allowed process temperatures from ambient to 90° C within an accuracy of +-2° C. Ozone concentration and gas flow were measured as well as the nitrogen flow for dilution and humidity, if applicable. Liquid UPW could be supplied through spray nozzles as conventionally used in wet benches. Drain was possible via an overflow rim as well as a drain line in the bottom of the tank.

Table 1: Resist types and pre-treatments

	Thickness	Softbake	Hardbake	UV harden	P implant A	P implant B
		90°, 30 sec	150°, 90 sec	150°,60 sec	1e13/cm²	5e14/cm²
IX-845	1200 nm	X	X	X	X	X
TOK 022	1200 nm	X	X	X		X
APEX /E	800 nm	X				
PEK 1507	700 nm	X				
UV 6	800 nm	X	X			X

For testing bare silicon wafers were used, coated with various types of photo resist and pretreatment (table 1). Strip rates were measured for softbaked (90°, 30 sec), hardbaked (150°, 90 sec), DUV hardened and P-implanted (1e13 – 5e14 at/cm²) resist using a PLASMOS ellipsometer. Particles of size 0.15 μ and above were measured with a TENCOR 6420.

RESULTS

Critical parameters for moist ozone strip:

In the first set of experiments wafers coated with 1.2 μ soft- and hardbaked IX845 resist were processed sequentially in increments of 2 and 3 min. Fig. 2 shows that the removal process at 80° is completed after app. 5 min. Most areas on the wafers were already cleared after 2 minutes in the moist ozone atmosphere. Different to the sulphuric driven strip, where the resist is delaminated from the wafer surface and subsequently oxidized in the liquid, with moist ozone it is removed layer by layer as observed in chemical etching. As expected the etch rate was found to be strongly dependent on the pretreatment. A drop in reaction speed of a factor of two was observed from softbaked to medium implanted resist. However as shown in Fig.3 even with DUV hardening and 1e14 at/cm² 150 keV phosphorus implantation the removal rates of app. 200 nm/min are feasible within a 10 min. process time for mass production. Improvements in performance of 20 – 30 % were seen with increasing the temperature from 80° to 100° in the process tank. Although further improvements are expected at higher temperatures this could not be proven due to the limitation of the tank setup.

The ozone concentration near the wafers is influenced by two major factors, the accessibility of ozone gas to the organics at the wafers surface through the boundary layer [4,5] as well as the amount of ozone in the tank itself. The latter is determined by the ozone concentration in the supply line, any dilution by non reactant gases like air or N_2 and the exchange rate of the atmosphere through the exhaust system. In immersion tank systems non sealing lids are used to control the exhausting fumes within the module to prevent cross contamination and harm to the environment. For the moist ozone application it turned out critical to minimize the exhaust during the process to extend the residence time of the ozone as much as possible. Exhaust rates of more than 600 l /h reduced the reaction rate by about 90 %. Thus the exhaust of the tank was limited to gases that escaped to the outer tank surrounding. Fig. 4 shows the impact of the flow rates of the O2/O3 gas into the systems. For two different types of resist (I-Line and DUV) it was seen that the overall reactivity increases with the flow, however the best uniformity is achieved for same O_3 concentration with mediate rates of about 5-7 l/ min. While quick mass transfer accelerates the process the slower exchange rate of the atmosphere provides a better gas distribution over the whole tank volume at lower flows. Thus the optimum strip process with respect to ozone flow was evaluated for different positions of the ozone supply Results are shown in Fig.5. Huge differences in removal rate and uniformity were seen for various positions of the ozone inlet. Optimization of the flow distribution clearly appears to be the more sensitive parameter than the flow rate itself. Therefore for shortest process times the design of the tank and ozone supply system is critical.

The control of humidity inside the process module is the key to provide optimum boundary layer conditions. While a low concentration of hydroxyl ion reduce the reactivity of the ozone with the organic chains significantly, a wet atmosphere results in a wet layer

of water on the wafers and therefore prevent the ozone to diffuse through this layer. It has been seen that too strong condensation or droplets fully stop the strip process, and stripes of residues are left where the ozone could not attack the resist. The surface temperature of the wafers must be at or above the temperature of the atmosphere in the vessel, which was achieved by a preheating phase in the tank before the moist atmosphere is introduced. Providing an ozonized vapor flow at temperatures above 90° at constant flows resulted in higher flow rates than providing the moist atmosphere directly out of heated UPW below the wafers. The optimal concentration is defined by the state of equilibrium between condensation onto and evaporation from the wafer surface. This was found to be at saturated or slightly supersaturated conditions in the vessel.

Particle performance:

The particle performance of the moist ozone process has been studied in comparison to standard rinse and clean recipes. Clean wafers of less than 30 particles of size 0.15 µ or bigger were used to determine the cleanliness of the process. The tests were done with and without filler or resist wafers in the tank. The results are shown in Table 2. While the introduction of the UPW (without ozone or dilution with nitrogen) did not contribute particles within the statistics, a slightly increase of the particle level was observed when the ozone was switched on. A subsequent overflow rinse after the moist ozone strip cleaned up the contamination to the incoming level, in case of an SC1 cleaning step (dilution 40:2:1 @ 50° C for 5 min) even slight particle reduction was observed.

Table 2: Summary of particle results

Test	specification	mean delta	Sigma
1	10 min ovfl. rinse	1	3,8
2	UPW vapour (80°, 10 min)	3	4,7
3	O3 gas 9 l/min, 5 min	10	9,1
4	O3 gas 9 l/min, 15 min	6	7,1
5	UPW - O3; 2 l/min, 10 min	11	10,1
6	UPW - O3; 4 l/min, 10 min	20	13,7
7	UPW - O3; 10 l/min, 10 min	10	4,2
8	repeat test 7 + 10 min rinse	4	4,4
9	repeat test 8 + 10 min SC1	-2	3,8

Effect of intermediate rinses:

Mass transfer of already dissolved resist is an important factor to speed up the resist removal process. Visual inspection of incompletely processed wafers after 3 min. of process time, i.e. with part of the resist still remaining on the wafers has shown that the adhesion of the organic is dramatically reduced even before the complete layer is removed. Dipping pre stripped wafers in an overflow rinse sometimes resulted in full delaminating of the residual layer without further ozone treatment. Therefore the implementation of intermediate rinses has been studied to further reduce the process time. A short spray rinse (3 - 5 seconds) was applied to the wafers in regular intervals of app. one minute. The liquid was simultaneously drained to minimize the amount of liquid in the tank at any time. It was found that in addition to rinsing at the end of the strip process for cleaning intermediate rinsing can shorten the total process time of even implanted resist by up to 30%. It is

assumed that after a short time (app. 30 sec.) the top layer of resist is saturated with C-C bonds that impact the diffusion of the ozone and reduce reactivity. Best results were achieved when the conditions in the tank are set up in a way that the liquid can evaporate quickly from the wafer surface to re-establish the boundary conditions for optimal ozone diffusion to the organics. This was achieved by keeping the wet phase of the process much shorter than the moist phase.

CONCLUSIONS

The application of moist ozone resist removal in an immersion type process environment has been studied. It was shown that even for medium implanted resist up to 5e14 at/cm² repeatable strip rates of more than 250 nm/min can be achieved which allows for a total process time of less than 10 minutes for most resist types (Fig. 6). Even for heavier implanted resist types moist ozone stripping appears feasible, at least in combination with a pre-ash step, that breaks the by implantation crusted top layers of the resist. Critical parameters for this application is a fully controlled moist ozone atmosphere with respect to ozone concentration and residence time as well as humidity at temperatures of >80°C within the tank. This process provides huge benefits with respect to cycle times and cost. Table 3 shows a comparison with major cost factors between the conventional SPM or SOM processes to the moist ozone process. Reduction of manufacturing cost by 0.11 US$ (SPM) or 0.05 US$ (SOM) per wafer processed are calculated on the bases of chemical cost of 5 US$ / liter. Further work needs to focus on shorten the process time even for 1e16 at/cm² implanted resists with higher temperatures or trace chemicals added to the rinse steps as well as applying this technology to multi-chemical baths.

Table 3: Cost of Ownership comparison of moist ozone vs. SPM and SOM process

	SPM (9:1)	SOM	O_3 vapour
	125 deg. + Quick Dump Rinse	110 deg. + Quick Dump Rinse	+ Ovfl. Rinse
H_2O cons. (l/batch)	220	220	150
H_2SO_4 cons. (l/yr.)	28000	15700	0
H_2O_2 cons. (l/yr.)	4100	0	0
Thruput (waf./hr.)	220	220	300
Footprint	2 modules	2 modules	1 module

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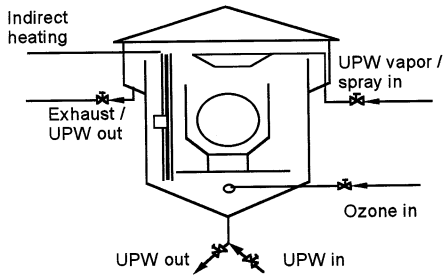

Fig. 1: Schematics of process tank setup

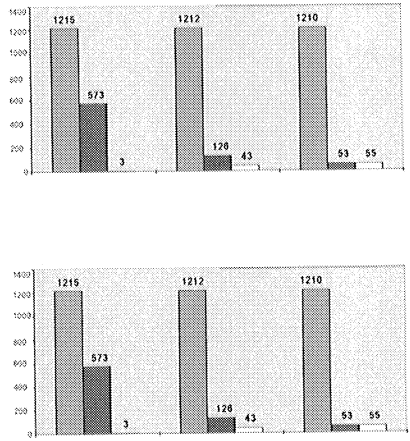

Fig.2: Resist removal rates at 80°C with moist ozone process for soft-baked (a) and hard-baked (b) IX-845 resist.

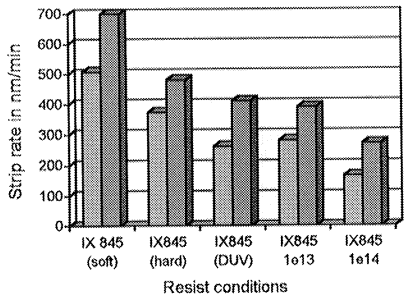

Fig 3: Strip rates as function of resist pre-treatment at 80°C and 100°C tank temperature

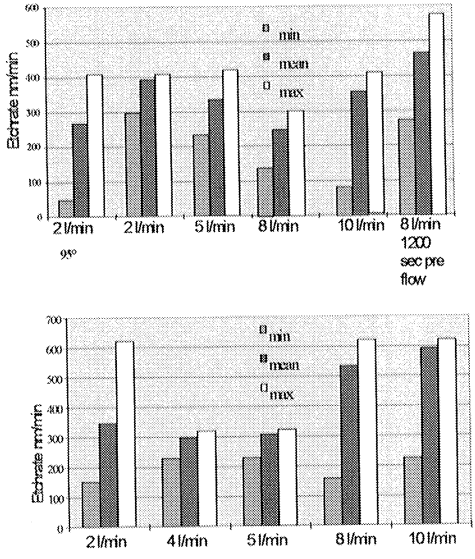

Fig 4. Resist removal rate vs Ozone Flow for soft-baked (a) and implanted (1e13 P @ 100KeV) (b) IX 845 resist

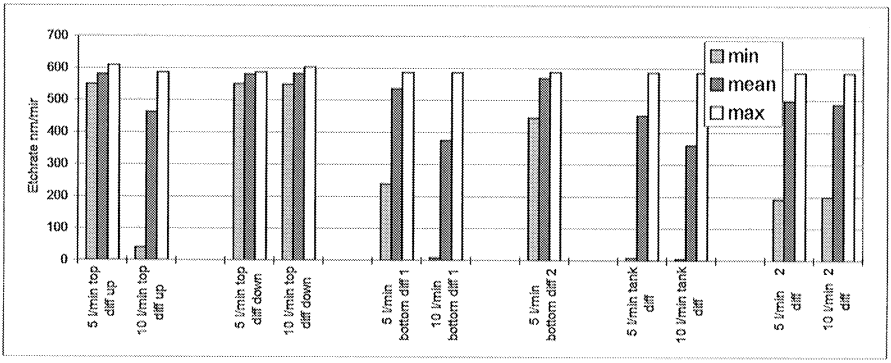

Fig. 5: effect of different ozone diffuser geometries on resist removal rate

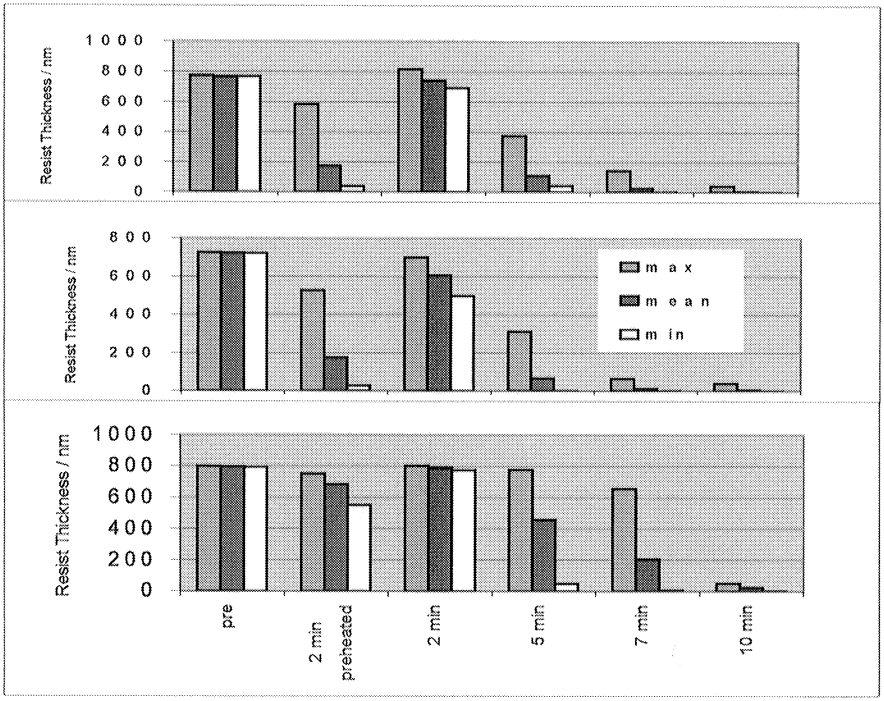

Fig. 6: Resist removal for different types of resist:
(a) APEX / E (0.8 μ) (b) PEK1507 (0.7 μ) (c) UV 6 (0.8 μ)

APPLICATION OF OZONATED AQUEOUS SOLUTIONS TO PHOTORESIST STRIP AND ASH RESIDUE REMOVAL FOLLOWING PLASMA POLYSILICON ETCHING

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Wet cleaning using ozone-deionized water has been receiving increasing attention in the last few years. This paper describes the unique FEOL application of boundary layer diffused ozone in hot deionized water (HydrOzone™) toward the stripping of photoresist, organic BARC and etching residue immediately after the plasma etching of polysilicon gate. The removal of the residues after an oxygen plasma treatment is also explored using ozone-deionized water accompanied by dilute ammonium hydroxide.

INTRODUCTION

In the manufacturing environment of wafer fabs, addressing the cost of ownership of the equipment and the process, the environmental impact from cleaning processes and the treatment and disposal of chemical wastes is receiving increasing attention. Indeed, the waste disposal costs, corrosiveness and the presence of particles from the use of sulfuric peroxide mixtures (SPM) have prompted the ongoing migration toward the use of ozone-deionized water for photoresist stripping, [1] organic contaminant removal and oxidation of silicon to grow an ultrathin layer of oxide after HF-last wet cleaning. [2]

The application of ozone in a liquid solution requires a balance between the increased solubility of ozone at lower temperatures and the increased reaction rates at higher temperatures. Recently, ozone has been applied on the immersion systems through injection into cold deionized water (DIO3) [1] and into hot deionized water but with the wafers placed above the ozonated water in a quartz container. [3] In the latter technique, the exposure of the wafers to moist ozone ambient leads to the condensation of a thin boundary layer on the wafer. In another recent application, the use of ozone-deionized water in a spray system has demonstrated a mechanism whereby the ozone is believed to diffuse through a thin boundary layer rather than becoming soluble in the boundary layer. [4] This HydrOzone™ process enables the use of higher temperatures relative to the conventional aqueous ozone processes, which consequently enhances the stripping rates of the photoresist to between 300 and 500 nm/minute.

A recent post polysilicon etching polymer removal process has shown the removal of carbon-based and sidewall residue using oxygen ashing, SC-1 and SPM. [5] The cleaning

sequence is tedious and costly from the manufacturing point of view. The application of the HydrOzone™ process in a spray chamber is an attractive alternative to replace oxygen ashing. Furthermore, an added impetus would be the exploration of the HydrOzone™ process toward the removal of the organic BARC and the etching residue.

EXPERIMENTAL

The transistor gate was fabricated on eight-inch p-type silicon wafers with (100) orientation. Both the gate silicon dioxide and polysilicon were grown in a TEL furnace. Deep ultraviolet (DUV) photoresist and organic BARC were used for patterning. The etching of the organic BARC and polysilicon was achieved on the Lam Research TCP9400 using hydrogen bromide and oxygen (for organic BARC), chlorine, hydrogen bromide and oxygen (for main etching) and hydrogen bromide (for over-etching). In one approach, the photoresist and organic BARC was stripped (ashed) on the Mattson ICP using oxygen plasma, followed by the HydrOzone™ process. In the alternative approach, the photoresist, organic BARC and the etching residue were subjected to the HydrOzone™ process. In-line SEM pictures were taken on a Hitachi S8820. Energy dispersive X-ray (EDX) studies were performed on a Philips XL30 using 5 KeV acceleration voltage.

The HydrOzone™ process was performed in a Semitool Spray Acid Tool (SAT), consisting of an enclosed Teflon® process chamber and rotor capable of processing up to 25 wafers at one time. The wafers were rotated within the chamber while a temperature controlled aqueous spray was delivered to the wafer surface. The temperature of the deionized water was set at 95°C. Simultaneously, dry ozone gas was also introduced into the process chamber, creating an ozone-rich environment in proximity to the wetted wafer surface. Upon conclusion of the process, deionized water was introduced followed by the purging with nitrogen until the ozone concentration in the chamber was reduced.

RESULTS AND DISCUSSION

HydrOzone™ Process

The key to the HydrOzone™ process control lies in controlling the boundary layer. This is accomplished by controlling the following important parameters: flow rate of the aqueous solution delivered to the process chamber, the manner in which it is delivered (spray pattern and pressure) and the rotational speed (rpm) at which the wafers are rotated. This combination is used to define the liquid boundary layer on the wafer surface. The objective is to create as thin and as uniform of a layer as possible. This is critical, since the HydrOzone™ process is not concerned with the solubility of ozone *in* the aqueous film, but is instead promoting diffusion of gaseous ozone *through* the boundary layer. This technique disconnects the ozone solubility from the temperature, thereby achieving strip rates that are much higher than conventional ozone-water processes. The mechanism is aptly illustrated in Figure 1.

- O_3 from the saturated environment diffuses through the thin boundary layer of water produced by rotation of the wafer in the presence of hot water
- Ozone attacks the hydrolyzed C-C and C-H bonds, effectively removing the organic contamination

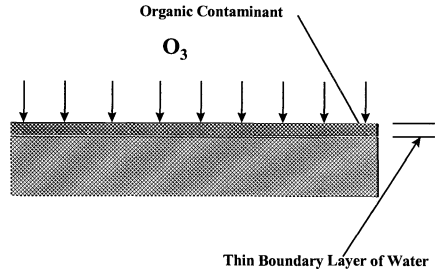

Figure 1. Ozone diffusion through a thin boundary layer

Once the temperature/solubility disconnection is achieved, the goal would be the achievement of the following: the minimization of the boundary layer which acts as a diffusion barrier, the maximization of temperature to accelerate the reaction kinetics, and the maximization of the ozone flow and concentration delivered to the process chamber in order to create a concentration gradient which will drive the ozone diffusion to the wafer/photoresist surface. Thus, high temperatures may be used to promote reaction kinetics without the adverse impact on ozone solubility that is normally encountered. Additives such as ammonium hydroxide may also be used in order to enhance specific cleaning applications such as ARC layer removal without adverse impact on the photoresist strip rate.

This process eliminates the need for stabilization time in order to achieve bath saturation, recovery time for the bath after processing, or even the need to monitor and control dissolved ozone in the aqueous stream, since ozone solubility becomes irrelevant. The result is that strip rates in excess of 800 nm/minute have been demonstrated on a number of photoresist types and treatments.

Appearance of the residue after etching and after oxygen ashing

The HydrOzone™ process was introduced in two different processing scenarios:

(i) etching → HydrOzone™ process

(ii) etching → oxygen ashing → HydrOzone™ process

The first process sequence evaluates the capability of the ozone-deionized water toward the removal of DUV photoresist, organic BARC and etching residue while the second process sequence evaluates the capability of the same solution toward the removal of etching residue.

Figure 2 shows the top-down scanning electron micrographs of the appearances of the residue on a large polysilicon pad feature after etching and after oxygen ashing. With regards to the latter, the residue manifests itself distinctively as a collapsed "fence" (sidewall) along the edge and a "cap" on the polysilicon surface. It is interesting to note that the "cap" residue is located some distance from the edge of the pad feature. EDX studies on the "cap" residue reveals the presence of the carbon and silicon. For the etched polysilicon that did not undergo oxygen ashing, the appearance of polysilicon pad is nothing more than an opaque patch of photoresist and organic BARC, with the "fence" residue clinging to the edge of the photoresist in the form of a dark strip. An independent FESEM cross-section determines the photoresist and organic BARC remaining to be about 4000 Å.

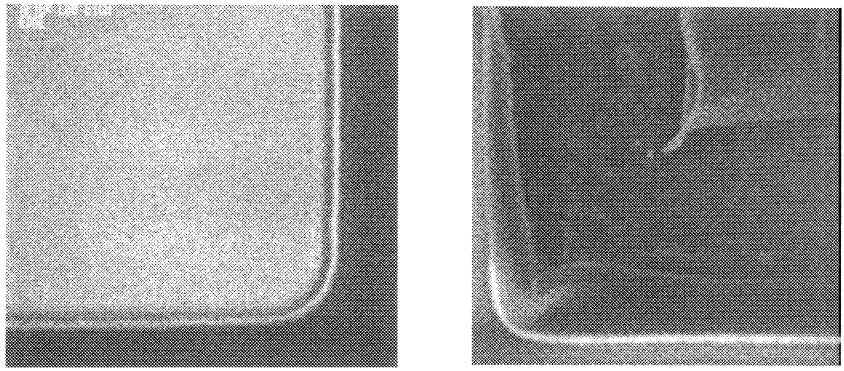

Figure 2. Appearance of the polysilicon feature after etching (left) and after oxygen ashing (right).

HydrOzone™ Processing After Etching

The etching of the organic BARC and polysilicon was accomplished on Lam Research TCP9400 using gas chemistry selected from chlorine, hydrogen bromide and oxygen. After etching, the wafers were transferred to the Spray Acid chamber for the HydrOzone™ process.

Figure 3 shows the result upon the application of a five-minute and fifteen-minute HydrOzone™ process. The photoresist and organic BARC was significantly removed after five minutes, and is confirmed by EDX studies, which show only the presence of silicon.

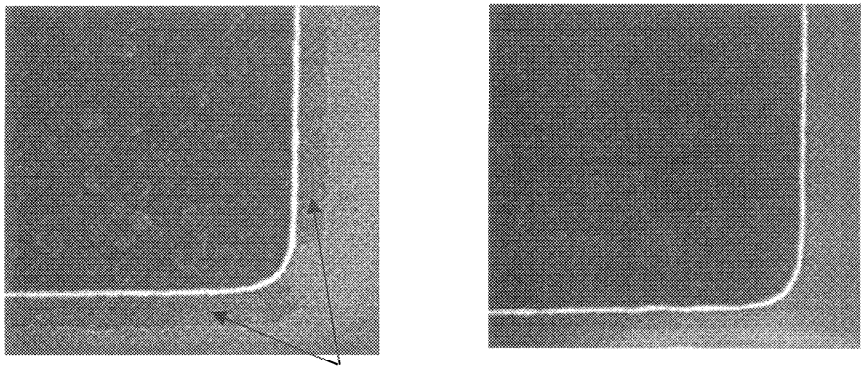

Figure 3. HydrOzone treatment after 5 minutes (left) and 15 minutes (right). The 15-minute process completely removes the DUV photoresist, organic BARC and the etching residue. The arrows point to the remnants of the sidewall "fence" after the 5-minute processing.

The reactions for the oxidation of photoresist and organic BARC would be:

(1) $-C- + 2O_3 \rightarrow CO_2 + 2O_2$
(2) $-CH_2- + 3O_3 \rightarrow CO_2 + 3O_2 + H_2O$

Upon closer scrutiny, it can be seen that portion of the sidewall "fence" still remains after 5 minutes of HydrOzone™ treatment, although its presence appears to have been dwindled. The sidewall "fence" is further reduced after 10 minutes of HydrOzone™ processing and completely disappears after 15 minutes.

The mechanism for the removal of the DUV photoresist, organic BARC and the etching residue using ozone-deionized water solution appears to be due to the strong oxidizing effect of the ozone and the bulk transport dynamics of the spray technology. Significantly, the simultaneous removal of the three components after etching suggests that the HydrOzone™ process could potentially replace the sequence of oxygen ashing, SC-1 and SPM and thereby reducing cycle time and chemical costs.

HydrOzone™ Processing after Oxygen Ashing

As shown in Figure 2, oxygen ashing removes the photoresist but leaves behind the etching residue in the form of a "fence" (sidewall) and a "cap". Based on EDX studies and our previous study, [5] the cap is deduced to be the organic BARC, which has changed its chemical nature and hardened by the high temperature during oxygen ashing. It was previously shown [5] that the sidewall "fence" was removed using SC-1 while the hardened organic BARC layer was removed using SPM. It would be interesting to see if the removal could be achieved using HydrOzone™.

The following experiments were first conducted with ozonated water on the wafers:
(i) 5-minute ozone-deionized water (HydrOzone™)
(ii) 10-minute ozone-deionized water (HydrOzone™)
(iii) 15-minute ozone-deionized water (HydrOzone™)

It was observed under the scanning electron microscope that the both the sidewall "fence" and the "cap" residue could not be completely removed in all the experiments. It is unsurprising that the "fence" residue could not be removed since the oxygen plasma may have thoroughly oxidized the sidewall "fence" to that of silicon oxide and attempts to remove the residue by a second oxidizer (i.e. ozone) would not succeed. However, the fact that the carbon-based "cap" residue was not removed by ozonated water seems to suggest a mechanism that is different from that of SPM.

Nevertheless, it was previously shown that the mechanism for the removal of the sidewall residue was due exclusively to the ammonium hydroxide in SC-1. [5] An attempt using solely dilute ammonium hydroxide (0.01 weight % in deionized water) for 15 minutes failed to remove both types of residue. It was then decided to see the resultant effect from the introduction of dilute ammonium hydroxide (NH_4OH) simultaneously into the spray chamber along with ozone and the heated deionized water in the following experiments:

(iv) 10-minute ozone-deionized water with 0.01 weight % of NH_4OH (HydrOzone(+)™)

(v) 30-minute ozone-deionized water with 0.01 weight % of NH_4OH (HydrOzone(+)™)
(vi) 15-minute ozone-deionized water with 0.05 weight % of NH_4OH (HydrOzone(+)™)

As evidenced by Figure 4, the introduction of 0.01 weight % of ammonium hydroxide produces further chemical disintegration of both "fence' and "cap" residues. However, increasing the cleaning duration three fold did not improve the removal. It was decided that the weight percentage of ammonium hydroxide should be increased to 0.05%. Indeed, the removal of the residue is improved but a complete removal was still not achieved. Although complete removal is possible with further increase in the concentration of ammonium hydroxide, it is pertinent to remark that ammonium hydroxide also etches the exposed thermal oxide next to the polysilicon gate. In fact, the etching rate of thermal oxide is about 0.2 Å/minute for a 0.01 weight % ammonium hydroxide solution at 95°C. Furthermore, ammonium hydroxide is known to etch and roughen silicon surface. Thus a higher concentration may produce undesirable roughening of the polysilicon and enhance the profile of any microtrench at the foot of the polysilicon gate.

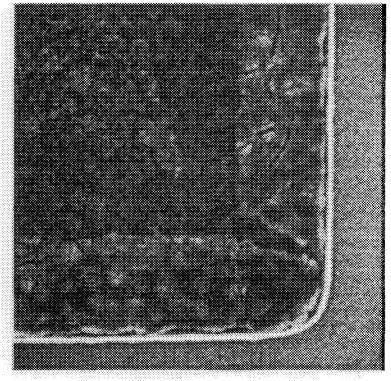

Figure 4. Disintegration of the carbon-based BARC and the sidewall "fence" residues upon addition of 0.01% NH_4OH to the ozonated water at 95°C.

The fact that the carbon-based BARC material could not be removed by ozone but gradually disintegrates by ozone-dilute ammonium hydroxide is interesting. The mechanism is unclear at this point but may be due to the provision of radical initiator (OH^-) from ammonium hydroxide in a weakly alkaline pH, which subsequently enhances the concentration of OH radicals. [3,6]

HydrOzone™ Process after Silicon Nitride Etching

Although this paper has focussed on the application of HydrOzone™ process for post polysilicon etch cleaning, it is pertinent to comment that the HydrOzone™ process has also been successful in removing the DUV photoresist, organic BARC and the minimal sidewall residue after the etching of and organic BARC and silicon nitride (using fluorocarbon chemistry).

CONCLUSIONS

The controlled boundary layer stripping method using ozone at high temperature (HydrOzone™) has been demonstrated to concurrently remove photoresist, organic BARC and the sidewall etching residue after the plasma etching of polysilicon. The success of HydrOzone™ represents significant cost savings and eliminates the concerns of waste disposal as it replaces the sequence of oxygen ashing, SC-1 and SPM. For samples that underwent oxygen plasma treatment after etching, a dual ozone-dilute ammonium hydroxide chemistry has been shown to be promising in the removal of the carbon-based and sidewall residues.

ACKNOWLEDGEMENTS

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POST NITRIDE-STI TRENCH ETCHING (INCORPORATING DUV RESIST AND BARC) POLYMER CLEANING

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The FEOL cleaning of residue after the etching of the nitride and the silicon trench is challenging in view of two etching approaches: a single equipment etching approach and a dual equipment etching approach. The first approach produces the conventional polymeric residue from etching and interestingly, a carbon-based residue in the form of "turtle-shell" and "vein". While the residue from etching can be removed using dilute HF, a sulfuric-peroxide mixture (SPM) cleaning is required to accomplish the removal of the carbon-based residue. An alternative cleaning sequence removes the thick etching residue immediately after etching, which may enhance the surface area for the oxygen radicals to react with the photoresist. The dual equipment approach results in only a "pillow-shaped" carbon-based residue, which can be removed using SC-1.

INTRODUCTION

The rapid advent of CMOS technology into the quarter micron device regime and beyond has led to several new integration schemes. Amongst these integration schemes is the shallow trench isolation (STI). There are many challenges in the integration of the shallow trench isolation and thus the etching of the nitride, pad oxide and silicon cannot be underestimated. The stringent control of the critical dimension (CD) of the silicon nitride and the slope of the trench have placed demands on the appropriate selection of the etching chemistries and etching equipment. Furthermore, the control of CD necessitates the implementation of advanced deep ultraviolet (DUV) lithography for high resolution patterning using chemically assisted photoresist. [1] In most cases, a bottom antireflective coating (BARC) is required to eliminate the linewidth variations that result in notching and to increase the exposure latitude and final resolution. [2]

Collectively, both lithography and etching performances have significant bearings on the removal of polymer. Indeed, it was shown previously that the DUV resist / BARC lithography scheme results in the generation of interesting residues after the etching of polysilicon. [3] The residues were effectively removed using a combination of SC-1 and sulfuric-peroxide mixture (SPM). The present paper focuses on the polymer cleaning methodology after etching of the silicon nitride/pad oxide film stack and the silicon trench in sub-quarter micron CMOS technology.

EXPERIMENTAL

The nitride-silicon trench was fabricated on eight-inch p-type silicon wafers with (100) orientation. The thin silicon dioxide was grown in a furnace at 800°C while the subsequent silicon nitride was deposited in a furnace with dichlorosilane and ammonia as the precursors. Deep ultraviolet (DUV) photoresist and organic BARC were used for patterning. The etching of silicon nitride and the silicon trench can be accomplished in two approaches.

In the "single equipment etching approach", the etching of the BARC, silicon nitride, silicon dioxide and silicon was performed on the Lam Research TCP9400. The etching chemistry comprises four-step gas chemistry:
(i) Chlorine and oxygen, for etching of organic BARC,
(ii) Carbon tetrachloride (CF_4), hydrogen bromide and oxygen, for silicon nitride
(iii) Carbon tetrachloride (CF_4) and trifluoromethane (CHF_3), for the etching of silicon dioxide, and
(iv) Chlorine, hydrogen bromide and oxygen, for the etching of silicon.

In the "dual equipment etching approach", the BARC, silicon nitride and silicon dioxide were etched on the TEL Unity DRM (using CHF_3 and oxygen, and CHF_3 and CF_4) after which the silicon trench was etched on the TCP9400 (using chlorine and hydrogen bromide). The DUV photoresist was removed on a Mattson ICP by turning on an oxygen plasma for 25 seconds. SC-1 cleaning was performed on a FSI Mercury MP Spray Processor at room temperature. Processing of sulfuric-peroxide mixture (SPM) at 120 °C was done on a wet bench. Dilute hydrofluoric acid (100:1) cleaning was performed either on the spray processor orthe wet bench. Buffered oxide etchant (BOE) cleaning was achieved on the wet bench or a single wafer spin etcher. In-line SEM pictures were taken on a Hitachi S8820. Energy dispersive X-ray (EDX) studies were performed on a Philips XL30 using 5 KeV acceleration voltage.

RESULTS AND DISCUSSION

"Dual Equipment Etching Approach"

The "dual equipment etching approach" entails the etching of BARC, silicon nitride and silicon dioxide in one etcher and the etching of silicon in another etcher. The separate etching allows better CD control during the etching of the silicon nitride.

(a) Post-nitride etching cleaning. Figure 1 shows the top view of the large silicon nitride features after the ashing of the photoresist. There is a distinct "pillow" shaped residue on the square pad. EDX studies performed on this residue reveals the presence of silicon, nitrogen and carbon, which attributes the residue to the remains of the organic BARC layer.

Careful scrutiny of the large feature reveals the absence of a sidewall residual film "fence" or "veil". Separate SEM studies confirms the absence of the sidewall film before oxygen ashing. The undesirable stoppage of the etching (due to polymer build-up) and the requirement for vertical etching profile (greater than 86 degrees) has meant the tuning of the

etching recipe to incorporate high CF_4:CHF_3 ratio and RF power. Minimal sidewall residual film is thus produced. Extension of the ashing duration from 25 seconds to one minute does not produce further receding of the organic BARC. The mechanism for the incomplete coverage of the BARC is unclear but may be due to the shrinkage of the material during ashing accompanied by hardening.

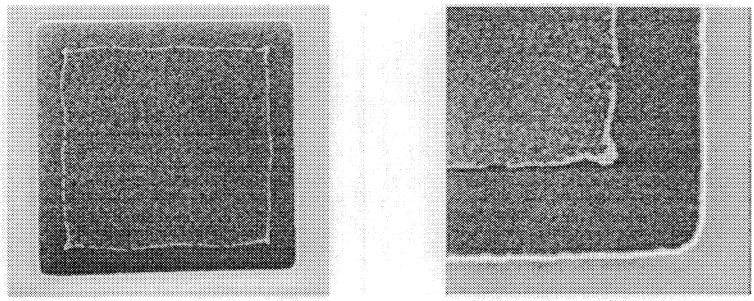
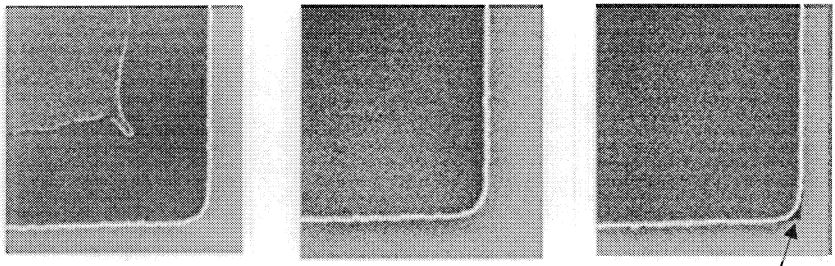


Figure 1. Top-down SEM micrographs showing residue at large silicon nitride features after photoresist ashing (40 K magnification for left micrograph and 80K magnification for right).

The organic BARC layer can be removed by SC-1. Interestingly, Figure 2 demonstrates that the removal mechanism for SC-1 is due exclusively to ammonium hydroxide. Concentrations of 100:1, 50:1 and 10:1 of the latter removed the residue, but trenching of the silicon at the corners and curved edges of all the features were observed. This is attributed to the lack of sufficient polymer at these locations and the high etching rate on silicon of pure ammonium hydroxide to SC-1. Dilute ammonium hydroxide has been documented to cause pitting and surface roughness on silicon and the addition of an oxidizing hydrogen peroxide (as in SC-1) reduces the surface roughness.



(a) 13:2 H_2O_2 (b) 100:1 NH_4OH (c) 14:1 NH_4OH, with trenching

Figure 2. The sidewall polymer removal using hydrogen peroxide (left), 100:1 ammonium hydroxide and 10:1 ammonium hydroxide. Trenching (indicated by arrow) is observed at the corner of feature.

The above renditions depict the sequence after nitride etching to be:
BARC/silicon nitride/silicon dioxide etching → oxygen ashing → SC-1
An additional sulfuric-peroxide mixture (SPM) may be used after the SC-1 cleaning.

(b) Post STI trench etching cleaning. It has been documented that chlorine-rich silicon oxide film is formed from the etching of the polysilicon using a hydrogen bromide/chlorine/oxygen etching chemistry. [3] Our previous work has shown that the etched residue could be removed using SC-1. [4] In the present case where the similar chemistry is used albeit on silicon substrate and a silicon nitride hardmask, it is expected that a similar composition of residue (additionally with nitrogen) may be present on the trench wall and surface.

Interestingly, while SC-1 (at room temperature) could not remove the residue, dilute hydrofluoric acid performed an efficient removal of the residue. Figure 3 depicts the residual removal in a spray processor. Since the subsequent step of dilute hydrofluoric acid did not involve IPA vapor drying technology, watermarks were observed occasionally on the wafers. Hence a combination of dilute hydrofluoric acid and SC-1 was chosen to remove these etching residues and watermarks.

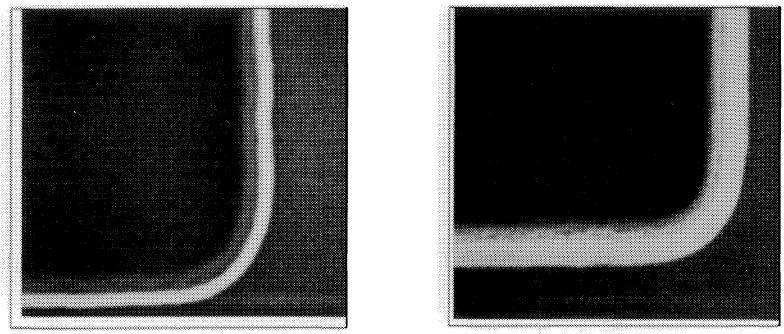


Figure 3. Scanning electron micrographs showing residue before cleaning (left) and residue removal after a 40-second dilute HF (right).

The sequence for post silicon trench etching is thus STI trench etching → dilute HF → SC-1

"Single Equipment Etching Approach"

In the "single equipment etching approach", the etching of the BARC, silicon nitride, silicon dioxide and silicon was performed in one single etcher.
Interestingly, a polymeric residue having two appearances was observed after oxygen ashing under the optical microscope: "turtle-shell" along the edge and "vein" at the center. These residues are reminiscent of those seen previously after polysilicon etching. [4] As shown in Figure 4, although the "turtle-shell" residue is irregular at the large silicon nitride pads and other structures, it seems to take on an uncanny regular pattern at certain silicon nitride structures. EDX studies (Figure 5) reveal the presence of only carbon, nitrogen and silicon on the "turtle shell" pads.

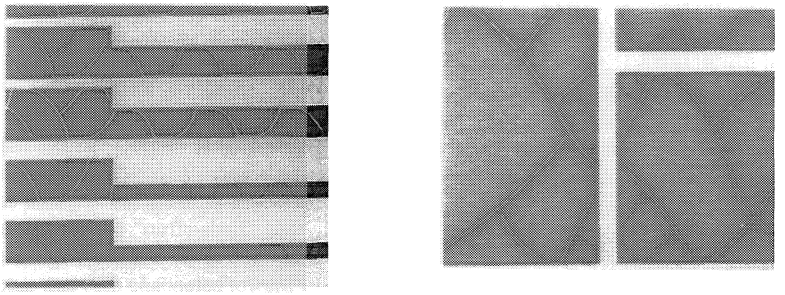


Figure 4. Regular and irregular "turtle-shell" residue at the silicon nitride features.

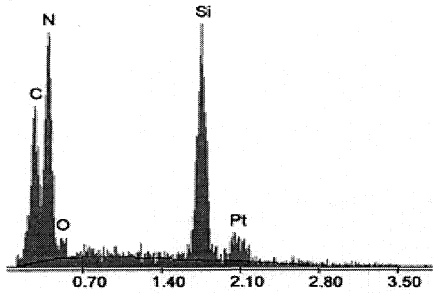


Figure 5. EDX spectrum of "turtle shell"

Besides the aforementioned carbon-based residue, the typical polymer or passivation film that results from the etching is also present. Unlike its counterpart from the two-step etching, a sidewall "fence" can be observed on the large pads as shown in Figure 6. This observation may be due to the relative larger amount of polymer generated in a single etching step process. However, in the smaller features, the "cap" and the 'fence" residue are generally indistinguishable.

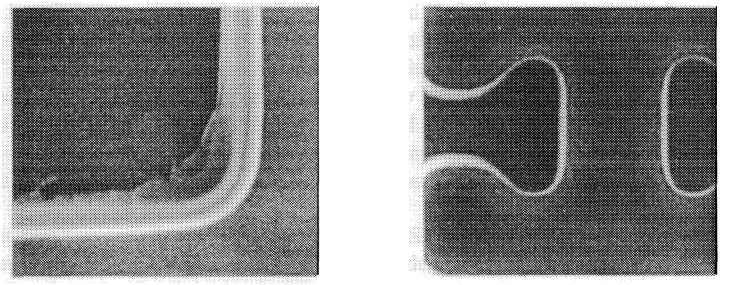


Figure 6. Collapsed sidewall residue "fence" along the edge of the silicon nitride/silicon pad and the indistinguishable residue on smaller feature.

Initial efforts to eliminate the carbon-based residue were concentrated on the ashing. Four approaches were attempted. The first approach was to lengthen the duration of the oxygen ashing. Despite lengthening the duration sevenfold (to three minutes), the residue could not be removed. A twice repetition of the oxygen ashing yielded the same observation. It was thought that the high temperature of the ashing process hardened or burnt the BARC. Nevertheless, the "turtle-shell" and "vein" residue still remained after the lowering of the temperature from 250 °C to 100 °C. Since the dry ashing could not remove the residues, the impetus was then channeled toward wet cleaning.

It has been shown that a SC-1 followed by SPM cleaning sequence worked well for the removal of carbon-based residues and etching residues for post polysilicon etching. Interestingly, the application of the SC-1-SPM sequence after oxygen ashing did not remove the residues. Neither did a reversed SPM-SC-1 cleaning sequence. As evidenced by Figure 7, cracking of the residue was observed. Nevertheless, based on the success of the cleaning in the "dual equipment etching approach", dilute hydrofluoric acid was tested and found capable of removing the residue. The carbon-based residue was then removed by SPM.

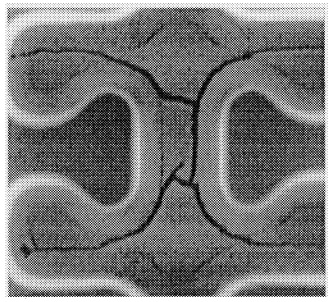
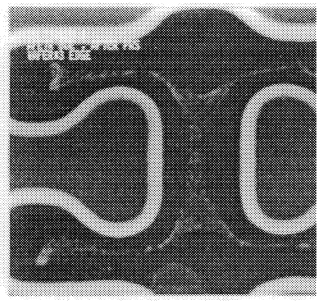
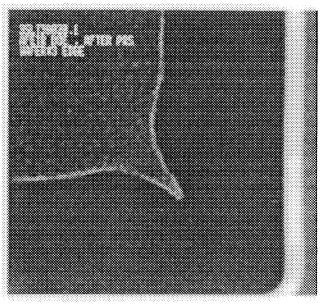


Figure 7. Cracking in the residue after SC-1 and SPM cleaning

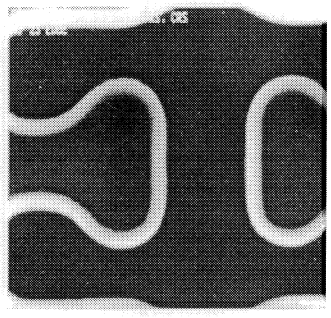
It became apparent that the "turtle-shell " and "vein" residue may have been formed due to the ineffective penetration of the oxygen radicals to the BARC. In other words, when the "cap" and "fence" residue was removed immediately after etching, the surface area for the oxygen radicals would then be enhanced and may overcome the kinetics of the hardening (and cracking) process. This methodology was tested out in the following sequence: etching → BOE → oxygen ashing. Indeed, optical microscope inspections confirm the absence of the "turtle-shell" and "vein" residues upon completion of the processing sequence.

Interestingly, as shown in Figure 8, top view SEM inspections reveal the presence of residue on all features, in particular the "pillow" residue on the square pads. The occurrence of the "pillow" residue is reminiscent of the residue observed earlier after silicon nitride etching in the "dual equipment etching approach". Indeed, EDX studies confirm the residue to be composed of silicon, nitrogen and carbon. Apparently, the kinetics of the hardening of the organic BARC is still faster than the reaction of the BARC with the oxygen radicals, despite the increased surface area after the removal of the etching residues. The residues after the oxygen ashing in the in the etching → BOE → oxygen ashing cleaning





Above: etching → BOE dip → oxygen ashing



Etching → BOE dip → oxygen ashing → SPM

Figure 8. SEM micrographs' showing the small nitride-trench features after BOE dip → oxygen ashing (top two) followed by SPM treatment (bottom center).

methodology can be removed using SPM. An alternative cost–effective methodology to produce a residue-free surface is to replace the oxygen ashing with SPM in the following sequence: etching → BOE → SPM. Furthermore, dilute hydrofluoric acid could be used in place of BOE but may cause delamination of the photoresist. [5]

Overall, three cleaning sequences have been found for "single equipment etching approach":

1) SiN/BARC/SiO/Si etching → oxygen ashing → dilute HF → SPM
2) SiN/BARC/SiO/Si etching → BOE or dilute HF → oxygen ashing → SPM
3) SiN/BARC/SiO/Si etching → BOE or dilute HF → SPM

CONCLUSIONS

Besides the conventional etching residue, an additional type of residue has been found when the DUV resist/organic BARC lithography scheme is employed for the etching

of the silicon nitride/silicon dioxide/silicon stack. This residue is carbon-based from the EDX studies and manifests itself in different forms depending on the etching approach ("single etching equipment approach" or the "dual etching equipment approach"). The following cleaning sequences have been found successful in the removal of the residue for the two etching approaches:
"Dual etching equipment approach":
BARC/silicon nitride/silicon dioxide etching → oxygen ashing → SC-1 followed by STI trench etching → dilute HF → SC-1
"Single etching equipment approach":
etching → oxygen ashing → dilute HF → SPM or etching → BOE or dilute HF → oxygen ashing → SPM or etching → BOE or dilute HF → SPM

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Room Temperature Photoresist Stripping and Residue Removal Technology

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We developed a new technology which perfectly strips stiffened resist after the ion implantation. This is a method for irradiating the solution which adds an isopropyl alcohol (IPA) and a potassium hydroxide (KOH) to the ultrapure water with megasonic. When the cleaning is carried out by irradiating the solution of IPA concentration 50wt% and KOH concentration 4.5wt% with 1MHz megasonic wave for 4 min, the resist on silicon substrate with the size of 30×30mm is perfectly removed. Moreover, a IPA/KF/megasonic cleaning has a excellent removal efficiency for resist residue remained on metal lines after the oxygen plasma ashing.

INTRODUCTION

As a resist residue remained on substrate surface after lithography process contains a large of contamination sources such as organics, metals, and etc, therefore, it should be perfectly removed from the substrate surface. In order to remove resist residue from substrate surface, A sulfuric acid and hydrogen peroxide mixture (SPM) cleaning (4:1) is recently used in the wet cleaning process [1]. This generates a large of

chemical fume from wet station because it is the high temperature cleaning processing at 90~130°C, which it is required for increasing the capacity of clean room air conditioning. The control of chemical mixing ratio is very difficult and resulting from degradation of process re-producibility and requiring continuous spiking of H_2O_2 into the system. A room temperature resist stripping technology without chemical vapor generation, therefore, is requirement for future device fabrication. Moreover, The most important issue for resist removal is that cleaning solution has an excellent performance for the resist removal after the ion implantation. The resist by ion implantation becomes a carbonic polymer structure which is non- stoichiometric structure with a deficiency of hydrogen content and is reported that removal efficiency is drastically degraded [2]. SPM cleaning can not perfectly remove the resist from the substrate surface, even if ashing process is added as previous step before SPM cleaning. In order to meet this requirement, we developed a new technology which strips the resist by IPA/KF with megasonic irradiation at room temperature [3]. An Arsenic (As) on wafer surface used in these experiments is implanted with a dose of 10^{15}atoms/cm^2. In order to easily penetrate chemical solution inside resist, a resist coated surface is intentionally drawn a line by using a diamond pen. As the result, the size of the resist which is coated on the substrate surface is 30 x 30mm. Figure 1 shows the dependence of ion-implanted resist stripping by IPA/KF/megasonic irradiation as a function of increasing dipping time. However, it takes around 28 min to remove resist from substrate surface.

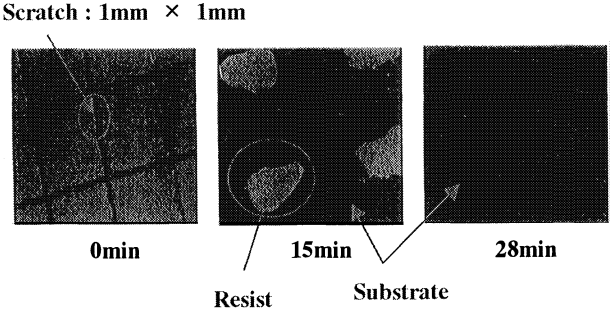

Figure 1. Ion-implanted resist stripping by IPA/KF/megasonic

We evaluated other chemical which contains a 10wt% KF and 1wt% H_2O_2 added ultrapure water with megasonic irradiation[4]. In this paper, a new and simple cleaning for stripping resist at room temperature is described.

EXPERIMENT

1. Resist stripping after ion-implantation

By coating the positive resist on 3000Å SiO_2 surface, after the baking, phosphorus was implanted with dose of 5×10^{15}atoms/cm^2. The sample was used at the size of the 30x30mm. The experiment was carried out in the cleaning bath tank in which 1MHz megasonic irradiation for all conditions was added. The temperature of cleaning solution in bath is controlled by filling ultrapure water between tank and outer tank in the inside in megasonic wave. The surface observation used optical microscope MX50 made of the Olympus Optical Co.,Ltd. The wettability of cleaning solution for the resist surface used contact angle meter made of Kaimenkagaku Co.,Ltd.

2. Resist residue removal on metal lines

After the metal etching, the oxygen plasma ashing for removing of resist which adhered on the wiring was treated for 3 min. The samples was cleaned by using 10wt% KF and 1 wt% H_2O_2 mixture solutions with megasonic irradiation and 20wt% IPA and 4.5wt% KF mixture solutions with megasonic irradiation, respectively. The surface observation was carried out by scanning electron microscope (SEM) inspection.

RESULTS AND DISCUSSION

1. Resist stripping after ion-implantation

Figure 2 shows optical microscopic images after IPA/KOH/megasonic cleaning which is done in the mixing ratio of 24wt%/4.5wt% and megasonic frequency with 1MHz. Resist on substrate surface starts to be removed in 3 minutes and is completely removed in 10 minutes. We suppose that it was stripped without dissolving into CO_2 and H_2O because cleaning is done at room temperature. That is, resist is floated by solution diffusion into inside interface between surface and resist. Figure 3 shows the optical microscopic images of resist removal efficiency as a function of time when IPA concentration in solution increased to 50wt%. With resist removal as a start in 1 min, it can be perfectly removed in less than 4 min.

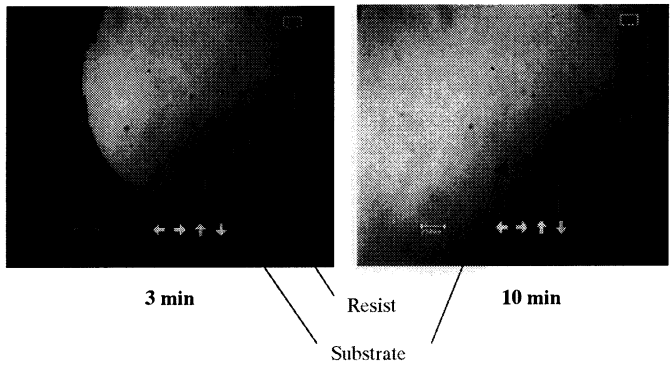

Figure 2. Ion-implanted resist stripping by IPA/KOH/megasonic. IPA: 24wt%.

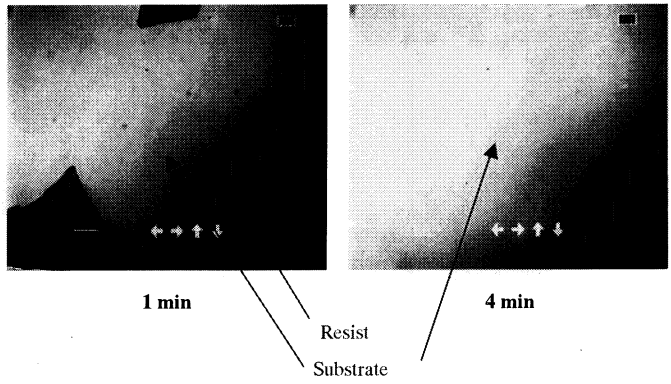

Figure 3. Ion-implanted resist stripping by IPA/KOH/megasonic. IPA: 50wt%.

The resist stripping rate drastically increase according to increasing the IPA concentration in solution. For the sample in which this resist has been added, there has no pattern, and does not completely put scratch in the resist surface. Figure 4 shows dependence of contact angle on implanted resist surface on cleaning solutions. The contact angle after IPA/KF solution treatment has the highest value compared to other conditions. For implanted substrate surface contrary to crystalline silicon surface, the difference of contact angle is decreasing the reason why it has many defect sites. The contact angle of substrate surface after IPA/KF or KOH solution treatment was not changed so much. However, it was drastically decreased after solution treatment which

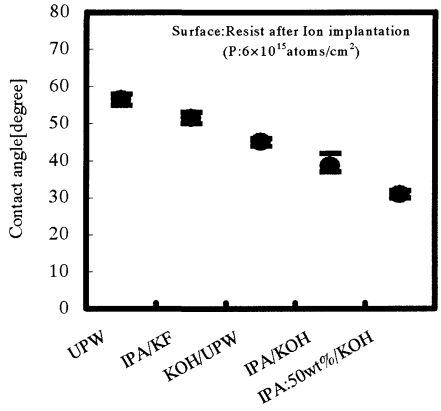

Figure 4. Contact angle of cleaning solutions on ion-implanted surface. IPA:24wt%, KOH: 4.5wt%.KF: 4.5wt%.

contains IPA solution in KOH. Especially, contact angle after IPA solution in KOH with the IPA concentration of 50wt% is reduced to below 30° . We suppose that the value of this contact angle is in accord with resist stripping efficiency. The solution with having capability of contact angle reduction has a good cleaning efficiency for removing of resist from substrate surface. We studied the reason that IPA/KOH/megasonic cleaning has a good efficiency. The resist was dissolved by 2.38wt% TMAH used the development process. In the case of positive resist, the part of which the light was irradiated can be developed. On the other hand, negative resist can be developed that dissolving the part of which the light is not irradiated. Since it is originally soluble for the alkali, such process has been established on the resist. We considered that resist stripping might be possible using the phenomenon. OH^- not contacts each other with the novolac resin, because the photosensitizer does not change in indene carboxylic acid, when the light is not irradiated. Therefore, the resist is not dissolved. The resist is not neutralized. The experiment which did foregoing by assuming that stripping progresses by impossibly sending and contacting OH^- using the penetration capacity of the IPA in the resist, was evaluated. The resist could be splendidly removed. However, the organic polymer in the resist becomes the carbon structure that the hydrogen component was remarkably lacking. And whether it dissolves in the stripper is uncertain for the question, when ion was implanted. However, in the current, originally organic polymer has remained on the layer under the surface hardening layer, and the part is penetrated with the IPA, OH^- goes, and it considers that the resist might be made to dissolve from the inside. It is not clear yet that study of the mechanism will be necessary in future.

Though in the place, potassium (K) is used in stripper, it is ionized by the oxidation power of the hydrogen ion, because the oxidation-reduction potential (ORP) of K is lower than that of hydrogen ion of aqueous solution. Therefore, its removal is very ease even in the ultrapure water. The K removal deposited on SiO_2 surface is possible by the hot ultrapure water[5]. However, it is necessary to investigate the process of greatly influencing the device performance like a gate oxide film in detail. A chemical lifetime of IPA/KOH should be investigated because the resist does not perfectly dissolve for room temperature treatment. Therefore, its residue in solution should be removed by a using the filter, and it may be possible to recycle the stripper as cleaning solution without changing chemical concentration for room temperature treatment. In this study, striping test is carried out at 30mm square 1 sheet only. In order to apply for real production, stripping should be carried out by the increase the number of treated wafer sheets and on the base of wafer level. Moreover, the investigation of the surface micro roughness with megasonic irradiation will be also advanced in future.

2. Resist residue removal on metal lines

Figure 5 shows SEM images on metal lines after various cleaning treatments. The SEM photos of upper side is the before and after the oxygen plasma ashing on metal line for 3 min. A whitely linear resist residue is observed on the metal surface. The resist residues of metal line surface after the oxygen plasma ashing, however, was perfectly cleaned by megasonic irradiation by KF/H_2O_2 (10wt% KF and 1wt% H_2O_2) and IPA/KF (20wt% IPA and 4.5wt% KF) solution for 1 min only.

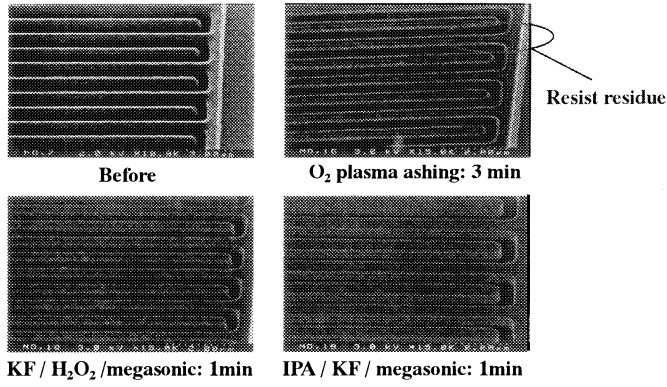

Figure 5. SEM images of resist residue removal.

From this research, we confirmed that a IPA/KF/megasonic irradiation and a KF/H_2O_2/megasonic irradiation cleaning on metal lines have an excellent resist removal efficiency. However, It also remains unclear the resist removal mechanism on metal lines. The study for removal mechanism will be carried out in the future.

CONCLUSIONS

We demonstrated a new technology which perfectly strips stiffened resist after the ion implantation. When the cleaning is carried out by irradiating the solution of IPA concentration 50wt% and KOH concentration 4.5wt% with 1MHz megasonic. It was confirmed that the resist on the sample of 30mm square which injected P to 5×10^{15}atoms/cm^2 perfectly remove in 4 minutes. It proved that the value lowered on the wettability of the IPA/KOH solution to ion-implanted resist surface, when the contact angle was investigated. Then, the stripping mechanism OH^- penetrated with the IPA in the resist inside, and it guessed that the resist was made to dissolve from the inside and the resist stripping progresses. And, it was possible to perfectly remove by irradiating the solution which mixed 20wt%IPA and 4.5wt%KF with 1MHz megasonic wave, for resist residue on metal lines.

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REMOVAL OF NOVOLAC-BASED PHOTORESIST FILM USING LOW MOLECULAR WEIGHT ALCOHOLS

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A new method to remove photoresist at low temperatures using low molecular weight alcohols (e.g., iso-propanol) is described. This process produces a clean, dry surface in a single step; no additional rinsing or drying is required. Results of atomic force microscopy (AFM) analysis show no appreciable change in micro-roughness of aluminum, silicon or silicon dioxide surfaces. X-ray Photoelectron Spectroscopy (XPS) of post isopropanol-treated surfaces indicates that contamination levels are similar to those resulting from RCA cleans. Ion implanted (2E12 and 2E15 atoms/cm^2) photoresist can also be stripped at room temperature by this process.

INTRODUCTION

Surface cleanliness plays a vital role in the production yield of semiconductor devices. With the approach of Giga Scale Integration, the number of cleaning steps will increase along with the number of other processing steps. In addition, one of the most repetitive steps in microelectronic device fabrication is photolithography. A critical step in this photolithographic process is stripping of the photoresist layer. Photoresist stripping refers to the complete removal of post etch or post implanted photoresist layers without attacking or altering the substrate or underlying films. This underlying material could be silicon, poly-silicon, aluminum, various silicides, silicon nitride, silicon dioxide, etc. Unless the procedure is properly implemented and controlled, photoresist-stripping processes can cause contamination and device damage. Currently, photoresist is stripped primarily by two methods:[1] dry stripping (generally uses downstream oxygen-based plasmas), and liquid stripping (includes organic strippers and ozonated aqueous chemistries)

Plasma ashing of photoresist using downstream O_2-based plasmas has received significant attention mainly due to the high stripping rates (~1-3μm/min) that can be achieved by this technique. However, this method is capital intensive and can cause damage to film surfaces and devices[2]. Plasma ashing may also result in resist popping and incomplete removal[2]. In addition, plasma ashing can cause incorporation of contaminants, which greatly reduces device reliability and carrier lifetimes. The source

of the contamination is frequently the photoresist material, which may contain metals and alkali ions such as Fe, Cu, Na, and K.

Liquid stripping methods that use organic solvents, reactive aqueous strippers, or sulfuric acid/hydrogen peroxide mixtures (SPM) are the most common techniques for resist stripping. As in the case of dry resist stripping, there are drawbacks associated with liquid stripping. For instance, stripping solutions are often toxic and corrosive, which results in high disposal and handling costs. In addition, a residual photoresist layer may remain on the wafer surfaces; this is especially true for resists exposed to plasma or ion-implantation processes. Stripping solutions also lose potency with time and accumulated contamination in the solutions can be a source of particles[1]. The wet stripping method is typically followed by de-ionized water rinsing and drying steps. A significant cost in device fabrication relates to the use of large amounts of de-ionized water for rinsing.

Low molecular weight alcohols, especially isopropyl alcohol (IPA) are widely used in microelectronics fabrication. IPA is the most commonly used solvent in 'solvent vapor drying' techniques. Iso-propanol successfully replaces water on the wafer surface because of its much lower surface tension (20 dynes/cm^2 versus 65 dynes/cm^2) and lower boiling point compared to water.[3] Furthermore, IPA and IPA-H_2O solutions are often used to remove static charges from surfaces.[4] Experimental measurements indicate that IPA liquid can completely remove both positive and negative charges.[4] In addition, IPA is believed to have the capability to remove particles from the wafer surface. One approach to particle removal uses an IPA spray along with centrifugal force to dislodge particles from the wafer surface.[5] Another approach assumes that the observed meniscus at the IPA/water interface is responsible for entrapping and transporting particles as the wafer is pulled out of the IPA bath. Dielectric breakdown measurements of the devices that use a final rinse in boiling IPA during fabrication indicate that low electric field breakdown of the capacitors is eliminated, suggesting that IPA is capable of removing particles smaller than 0.22 μm. Vapor phase decomposition total reflection x-ray fluorescence (VPD-TXRF) measurements indicate that a final rinse in boiling IPA reduces potassium, calcium, copper, and sulfur residues.[6]

In this paper, the use of low molecular weight alcohols, in particular IPA, for photoresist removal is described. The process developed eliminates the need for separate rinsing and drying operations and thereby reduces the total number of processing steps and the volume of de-ionized water used. In addition this process is vacuum compatible and can be integrated in to 'cluster-tool' processing technology.

EXPERIMENTAL PROCEDURES

Shipley 1813 photoresist was coated to a thickness of 1.5 μm directly onto an HMDS primed thermally grown silicon dioxide surface. The photoresist was then soft baked at 90° C on a hot plate for two minutes. I t was then patterned and developed, and then hard baked at 120° C on a hotplate for two minutes. For surface analyses, samples of size 1cm×1cm were placed into a reactor designed for liquid and vapor phase cleaning. This reactor, which has been described previously[7], was composed of two chambers. The inner chamber can be pressurized to 3000 psi and the outer chamber can be evacuated to 10^{-8} torr. Such capability permitted direct integration of this chamber and thus the silicon

sample, with another processing step or with surface analysis chambers. A sample was placed on a stainless steel sample stub, the inner chamber closed, and IPA was introduced into the inner chamber. The chamber temperature was maintained at 25 °C and 1 atm. The flow rate of alcohol was controlled at 2-5 ml/min. After photoresist was removed, the inner chamber was evacuated in order to evaporate residual solvent from the sample and obtain a clean, dry surface. The sample was then transferred to the surface analysis system (XPS), under vacuum, without exposure to atmosphere. In certain studies, samples were placed in a bath of specific alcohol (ethanol, n-propanol or iso-butanol) for a specified time; they were removed, dried with nitrogen, and immediately transferred into the ultra-high-vacuum chamber of the X-ray photoelectron spectrometer (XPS) for surface analysis.

In order to investigate the utility of this alcohol-based stripping method, removal of photoresist from patterned surfaces was studied. A photomask pattern was designed to create a wide variety of patterns as shown in Figure1. The smallest feature size in this mask is 3 μm.

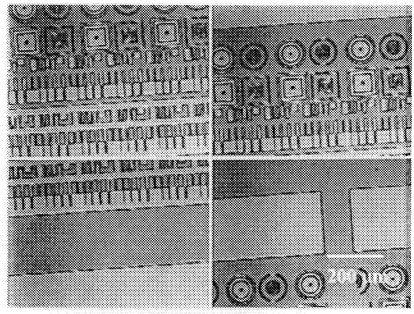


Figure1: Patterned Photoresist

A high-pressure reactor with a sapphire window was fabricated to allow in-situ observation of the interaction between photoresist and the alcohols (Figure 2). The fluid inside this reactor can be pressurized to 2000 psi using a syringe pump.

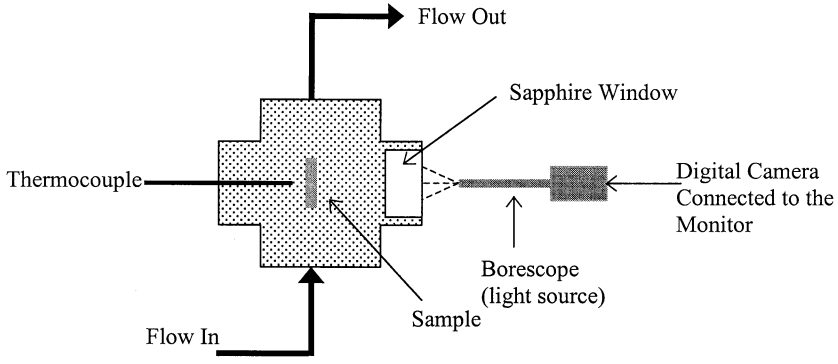
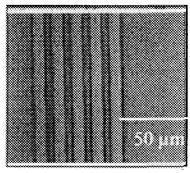


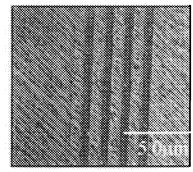
Figure 2: High-pressure reactor with a sapphire window and a borescope to view sample surfaces

RESULTS AND DISCUSSIONS

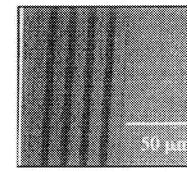
The channels in the patterned resist as shown in Figure 3(a), are 10 μm wide and photoresist is present in the non-patterned section of the sample, and in the channels between the patterns as indicated. In Figure 3(b), swelling of the entire photoresist layer is observed after 1 minute of exposure to IPA at room temperature and atmospheric pressure. After 3 minutes of exposure to IPA, the photoresist has been removed from most of the sample; however, resist remains in the patterned channels. This suggests that it is more difficult for the alcohol to attack pattern edges than non-patterned surfaces. Such observations indicate that at least part of the removal mechanism involves 'peeling' of the organic film due to penetration of the alcohol beneath the film. Each pattern edge acts as a barrier to solvent penetration, thereby decreasing removal rates in the channels. The patterns diminish with increased exposure time to the alcohol and are completely stripped (Figure 3(e)), after 6 min of exposure to IPA at room temperature.



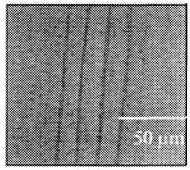
(a) No treatment



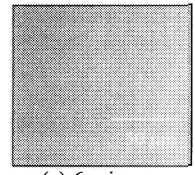
(b) 1 min.



(c) 3 min.



(d) 5 min.



(e) 6 min.

Figure 3:
Micrographs of various surfaces (a) Untreated Photoresist Film, (b), (c), (d) and (e) after exposure to IPA (40X magnification).

Photoresist removal rates are obtained by removing the samples at various time intervals and measuring the thickness of the remaining photoresist layer via profilometry. The removal rate for IPA is initially high (1±0.2 μm/min) but the rate decreases with decreasing photoresist thickness. Since IPA swells organic materials, the high initial removal rate may be due to the fact that IPA easily swells the upper portion of the photoresist, thereby enhancing the removal rate. However, this rate decreases for the portion of the resist near the surface, where photoresist adhesion to the substrate inhibits swelling. The removal rate increases as the process temperature is increased from 25°C to 50 °C; for example, with IPA, the average rate of removal increases from 0.25 μm/min to 0.5 μm/min. However, this removal rate decreases significantly when the alcohols are heated above their boiling point. This observation indicates that both the solubility and the surface tension of the liquid play important roles in the removal process. The overall rates of photoresist removal with various alcohols are given are given in Table I.

Table I: Rates of removal of photoresist by different alcohols @ 25 °C

Alcohols	Time of Removal (min)	Average Rate of Removal
Iso-Propanol	6.0 + 0.25	0.25 + 0.10
Ethanol	2.25 + 0.25	0.75 + 0.10
n-Propanol	5.75 + 0.25	0.3 + 0.10
2-Butanol	8.5 + 0.5	0.2 + 0.10

X-Ray Photoelectron Spectroscopy Study of Surface

X-ray Photoelectron Spectroscopy (XPS) analysis results of carbon concentrations on silicon dioxide surfaces after photoresist stripping with alcohols are shown in Table II.

Table II: Atomic carbon percent on the surface from XPS

Solvent Used	Process Time(min)	Atomic Percent Carbon
Untreated Photoresist		83.7
Iso-Propanol	6	9.4
Ethanol	3	29
n-Propanol	6	24.9
2-Butanol	9	28.5
RCA Cleaned Surface	30	7.5

XPS studies of bare silicon samples treated with IPA show a marked decrease in carbon content relative to silicon samples that had been exposed to the atmosphere for thirty minutes. This observation indicates that IPA is capable of removing adventitious carbon as well as novolac-based photoresist. XPS analyses demonstrate that of the alcohols investigated, 2-propanol (IPA) leaves the least amount of residual carbon on the surface. A further indication of complete photoresist removal is given by the absence of a π-π^* transition in the XPS spectra of the treated samples. This shake-up structure usually appears on the high binding energy side of the main photoelectron peaks,[6] and is common for core level spectra of aromatic (e.g. phenyl-containing) and unsaturated polymers. As shown in Figure 3, the π-π^* transition is present as a low intensity broad peak at a slightly higher binding energy (288 eV) than the carbon peak (284.8 eV) in the photoresist spectrum. This shake-up peak due to the phenyl ring in the novolac resin decreases with increasing treatment time (Figure 3), and disappears when the photoresist film has been removed.

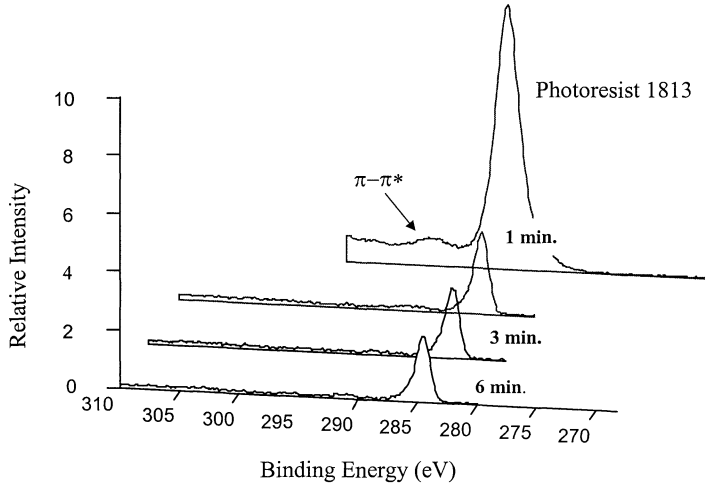


Figure 4: Carbon C1s XPS spectra for various exposure time to IPA

Effect of Alcohols on Surface Micro-roughness

Surface micro-roughness, particularly at the Si-SiO_2 interface, is detrimental to MOS device characteristics[9]. Wet cleaning methods often result in increased surface micro-roughness, due to the non-uniform etching of surfaces by the chemicals used[10]. Atomic Force Microscopy (AFM) analyses show no significant increase in surface micro-roughness of SiO_2 surfaces after 30-minute exposures to the four alcohols studied. AFM analyses also indicate that prolonged exposure (30 minutes) of 3 μm thick evaporated aluminum layers to these alcohols does not cause changes in the surface micro-roughness. Finally AFM images of post-resist-stripped samples relative to pristine SiO_2 surfaces immersed in IPA, do not show changes in the surface micro roughness.

Ion Implanted Photoresist

Ion implantation is used extensively for accurate control of impurity incorporation in semiconductor substrates. The process generally uses a photoresist mask for selective area ion implants. The high ion dose and energy used during the implant results in the formation of a carbonized "crust" that makes resist stripping difficult[11]. This toughened resist is typically removed by plasma stripping followed by exposure to H_2SO_4/H_2O_2 solutions (SPM) at elevated temperature (120 °C). The disadvantages associated with such approaches have already been discussed. Using the IPA process described above, photoresist exposed to low-level boron and phosphorous implants can be removed. For

instance, photoresist samples implanted with boron or phosphorous to the level of 2×10^{12} cm^{-2} at an energy of 80keV, are removed in 8 min. (B) or 10 min. (P) when exposed to IPA at 25° C. The longer treatment time necessary for phosphorous-doped resist may be due to the higher degree of carbonization caused by the phosphorous dopant[12]. It is believed that the higher atomic weight of phosphorous relative to that of boron results in lower impact velocity at the photoresist surface for the same ion energy. Thus a thinner but higher carbon content layer is formed that is more resistant to alcohol attack. XPS analyses of the post-IPA treated samples indicate that 10 ± 0.5 atomic percent carbon remains on the surface of the IPA treated samples.

Iso-propanol did not significantly attack photoresist layers containing 2×10^{15} atoms/cm^2 of boron or phosphorous ions at room temperature. In this case, the upper layer of the photoresist is carbonized and roughens significantly due to the higher implant doses. Therefore, it is more difficult for the alcohol to penetrate the top portion of the photoresist. At 50°C, the larger photoresist patterns are removed in 10 minutes, but the smaller patterns (less than 50 μm), especially the enclosed ones, remain on the surface. A combination of elevated pressure (60 psi) and elevated temperature (50°C) is useful for removal of this hardened photoresist. It is believed that the pressure gradient on the surface of the photoresist assists incorporation of the alcohol, possibly through pinholes or weak spots in the crust, to the underlying virgin photoresist layer. T he then alcohol then dissolves the underlying photoresist. This creates a stress on the film leading to the removal of the photoresist film. According to the insitu monitor, the removal mechanism consists of " roll off "the film from the edges of the large blocks of photoresist. Figure 5 shows the penetration of alcohol through the film and dissolution of the underlying layer.

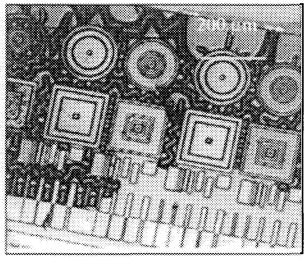


Figure 5a: Effect of IPA on ion-implanted (10^{15}atoms/cm^2) photoresist at 50° C and 60 psi.

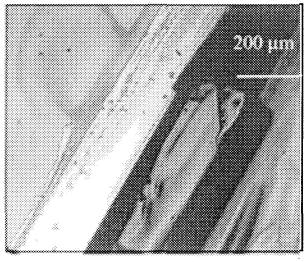


Figure 5b: Peeling of ion- implanted (10^{15}atoms/cm^2) photoresist.

CONCLUSION

Resist stripping using low molecular weight alcohols such as IPA at room temperature may offer substantial advantages to current stripping methods. For instance, this method of using IPA eliminates the need for additional rinsing and drying steps after resist removal, since IPA, because of its high surface tension, acts as an effective drying agent. The same is true for other alcohols, although stripping rates are lower than are those obtained with IPA. Because IPA does not roughen silicon dioxide or aluminum surfaces, this method may offer advantages relative to plasma removal.

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HF ETCHING

THE CONTROL OF ETCHING RATE FOR VARIOUS SiO_2 FILMS

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ABSTRACT

The etching rate control of various SiO_2 films (Thermal Oxide, CVD-TEOS, BPSG, BSG, PSG and AsSG) was studied. It has been demonstrated that the selective and non-selective etching can be achieved by the suppression of the HF and NH_4HF_2 dissociation. BSG and BPSG are etched selectively in the low relative dielectric constant-solvents containing HF. Every SiO_2 films are etched non-selectively in the low dielectric constant-solvents containing NH_4HF_2.

1. INTRODUCTION

For the SiO_2 wet etching, HF-H_2O(DHF) and HF-NH_4F-H_2O(BHF) are generally used. The several studies for the mechanism of SiO_2 etching by BHF have been done[1-3]. It has been cleared that the etching species for SiO_2 is HF_2^-. The various SiO_2 films such as thermal oxide, CVD-TEOS(Chemical Vapor Deposition-Tetraethoxysilane), BPSG(Boron Phosphorus Silicate Glass), BSG(Boron Silicate Glass), PSG(Phosphorus Silicate Glass) and AsSG(Arsenic Silicate Glass) are used in semiconductor manufacturing. These oxide films are formed as several layers on Si wafer surface. When the bottom of contact hole is cleaned, doped oxide and non-doped oxide are exposed to cleaning solution at the same time. As the dimension scales down, the control of etching rate of various SiO_2 films is very important. In this study, we attempted to control the etching rate of various SiO_2 films by the dissociation control of HF, NH_4F, HF_2^- and NH_4HF_2. The dissociation control has been done by using the solvents which have low relative dielectric constant, instead

of H_2O which is generally used for the solvent of DHF and BHF.

2. EXPERIMENTAL

Etching rates were measured for thermal oxide(THOX), annealed LPCVD-TEOS(TEOS), non-annealed BSG, annealed BPSG, PSG and non-annealed AsSG films. The oxide thickness were measured by ellipsometer Auto EL III(produced by Rudolph Research) . Acetic acid, tetrahydrofuran(THF), isopropyl alcohol(IPA), acetone, ethanol and methanol were used for the solvents which have low relative dielectric constant. 50wt%HF, 40wt%NH_4F, NH_4F(solid) and NH_4HF_2(solid) were used for etching species. The every etching was performed at 25℃ for prescribed time. The etching rate was defined as the decrease of film thickness in a unit time.

3. RESULTS AND DISCUSSION

3.1 The etching of THOX, BPSG and BSG by DHF and BHF.

Figure 1 shows the dissociation form and equilibrium constants of HF in H_2O. As shown in Fig.1, HF dissociates into H^+ and F^-. And F^- combine with the undissociated HF to form HF_2^-. Figure 1 also shows the calculated concentrations of HF, HF_2^-, H^+ and F^- in 1wt%HF aqueous solution by using these equilibrium constants. As the result, HF concentration is highest, and the value is 0.408mol/kg. The concentration of HF_2^- which is dominant etching species of SiO_2 is only 0.041mol/kg. Figure 2 shows the dissociation form and equilibrium constants of BHF in H_2O. As shown in Fig.2, NH_4F dissociates into NH_3^+ and F^-. And F^- combines with the undissociated HF to form HF_2^-. Figure 2 also shows the calculated concentrations of HF, HF_2^- H^+ and F^- in 1wt%HF-40%NH_4F aqueous solution by using these equilibrium constants. In these calculation α (the dissociation constant of NH_4F)was assumed 0.5. The concentration of HF_2^- is much higher than the 1wt%HF aqueous solution.

Table I shows the etching rates of BSG, BPSG and THOX in HF aqueous solutions. Table I also shows the selectivity of BSG and BPSG to THOX.

Table I Etching Selectivity of BSG, and BPSG to THOX

Chemicals	BSG (Å/min)	BPSG (Å/min)	THOX (Å/min)	Selectivity (BSG/THOX)	Selectivity (BPSG/THOX)
1wt%HF-H_2O	380	530	60	6.3	8.8
2wt%HF-H_2O	750	1140	120	6.3	9.5
5wt%HF-H_2O	2000	2930	320	6.3	9.2

As shown in Table I, selectivity of BSG and BPSG to THOX are 6.3 and 8.8 in 1wt%HF aqueous solution. The etching rates of BSG and BPSG are higher than the etching rate of THOX. In the case of 2wt%HF and 5wt%HF aqueous solutions, the etching rates of all oxide films are higher, while the etching selectivity to THOX

hardly change. From these results and calculated concentration shown in Fig.1,it is considered that BSG and BPSG are mainly etched by undissociated HF and THOX is mainly etched by HF_2^- as known.

Figure 3 shows the dependence of etching rates and selectivity on NH_4F concentration. HF concentration was 2wt% and the temperature was adjusted to 25℃. BSG and THOX were evaluated. For THOX, by the addition of NH_4F, the HF_2^- are produced and the etching rate increases. The etching rate has maximum when the NH_4F concentration is about 20wt%. When the NH_4F concentration is more than 20wt%, the etching rate of THOX decreases even though the HF_2^- concentration is stable. It has been reported that the mobility of HF_2^- decreases due to the NH_4^+ increase[3]. For BSG, the etching rate decreases as the NH_4F concentration increases. It is considered that this is attributable to the decrease of undissociated HF concentration. Because the undissociated HF is combined with F^-. Figure 4 shows the dependence of etching rates on NH_4F concentration. HF concentration was adjusted to 0.25wt% or 1.0wt% and the temperature was controlled at 25℃. BPSG and THOX were evaluated. The etching rate of BPSG similarly decreases as the NH_4F concentration increases. However, when HF concentration is 0.25wt% and NH_4F concentration is 0-10wt%, the etching rate of BPSG increases. It is considered that the etching of Si-O by HF_2^- mainly occurs comparing with the etching of B-O by undissociated HF in the case of very low HF concentration. As the NH_4F concentration increases the etching rates of BPSG and THOX approach each other. Especially when the HF concentration is 1wt% and NH_4F concentration is 40wt%, the etching rate of BPSG and THOX are almost equal.

3.2 Selective etching of BSG and BPSG.

From the results shown in 3.1, we studied the selective etching of BSG and BPSG by the suppression of HF dissociation.

We also studied the selective etching of BSG and BPSG by using the solvents which have low relative dielectric constant instead of H_2O. When there are two materials which have electric charge q_1,q_2 at the distance of r in the liquid dielectric(solvent), the force f between two materials are shown in the equation bellow.

$$f = q_1 q_2 / 4\pi\varepsilon_0\varepsilon_r r^2$$

(ε_0:dielectric constant of vacuum ε_r:relative dielectric constant)

The force between two materials is proportional to the reciprocal of relative dielectric constant of solvent. From this fact, the interaction between two materials which have electric charge is strengthened as the relative dielectric constant decreases.

Consequently, when the HF is added to the solvents which have low relative dielectric constant, the attractive force between H^+ and F^- is strengthened and the undissociated HF concentration increases. As a result, it is expected that the BSG and BPSG are etched selectively.

Selective etching of BSG and BPSG are performed by using the solvents; CH_3COOH(ε r:6.15), THF(ε r:7.6), acetone(ε r:20.7), IPA(ε r:19.9), ethanol(ε r:24.6) and methanol(ε r:32.7) which have low relative dielectric constant compared with H_2O(ε r:78.3). Table 2 shows the selective etching of BSG and BPSG to THOX by the low relative dielectric constant-solvents containing HF.

Table II Selective etching of BSG and BPSG to THOX by the low relative dielectric-constant solvents containing HF

Solvents	BSG (Å/min)	BPSG (Å/min)	THOX (Å/min)	Selectivity (BSG/THOX)	Selectivity (BPSG/THOX)
IPA	330	330	6	55	55
CH_3COOH	7800	9700	130	60	75
THF	510	330	3	170	110
CH_3OH	170	230	3	57	77
C_2H_5OH	250	210	7	36	30
$(CH_3)_2CO$	410	250	3	137	83
H_2O	2160	2930	320	6.8	9.2

As shown in this Table, the selectivity of BSG and BPSG to THOX are much increasing in every solvents which has low relative dielectric constant. Especially, in the case of using THF of which relative dielectric constant is 7.6, it is possible that the selectivity of BSG to THOX increases to 170 and the selectivity of BPSG to THOX increases to 110. In the case of using CH_3COOH which have lowest relative dielectric constant, the etching rates of every film is very high and the selectivity are lower than the case of using THF. It is considered that the dissociation of HF is varied because the CH_3COOH is acid itself and dissociate into CH_3COO^- and H^+. And in the case of using alcohol, the selectivity are not increasing compared with the other solvents even though the relative dielectric constant is low. Compared acetone(ε r:20.7) with IPA(ε r:19.9), the selectivity in the case of using acetone are much higher than the case of IPA. It is also considered that the dissociation of OH group to O^- and H^+ influences.

3.3 Non-selective etching of BPSG and THOX.

It was described that the selective etchings of BSG and BPSG are possible by the suppression of HF dissociation in low relative dielectric constant-solvents. We studied the non-selective etching of BPSG and THOX by using the low relative dielectric constant-solvents containing NH_4HF_2. At present the non-selective etching

of BPSG and THOX is performed by increasing NH_4F concentration and decreasing HF concentration in BHF(e.g. HF:0.25wt%, NH_4F:40wt%). When the NH_4F concentration increases to 40wt%, the selectivity of BPSG and THOX can be low because undissociated HF concentration is low and HF_2^- concentration is high. Especially, when the HF concentration is 1wt%, the selectivity of BPSG to THOX is almost 1. However, it is not possible to use the cleaning of contact hole because the etching rate is too high(150A/min to THOX). From these results, it can be expected that the non-selective etching of BPSG to THOX is achieved by the production of only HF_2^- which is dominant etching species to SiO_2.

Table III shows the etching rates of BPSG and THOX by the low relative dielectric constant-solvents containing NH_4HF_2 or NH_4F. Table III also shows the selectivity of BPSG to THOX. As shown in this table, when the NH_4HF_2 is added to ethanol and IPA or the NH_4F is added to CH_3COOH, the selectivity of BPSG to THOX can be almost 1 and the etching rates can be low. When the NH_4HF_2 is added to H_2O, NH_4HF_2 dissociates into NH_4^+ and HF_2^-, and HF_2^- dissociates into HF and F^-. Therefore non-selective etching of BPSG to THOX is not possible. However, in the case of NH_4HF_2 addition to low relative dielectric constant-solvents, the dissociation of NH_4HF_2 is controlled. Because the binding energy of NH_4HF_2 is large, NH_4HF_2 dissociates slightly into NH_4^+ and HF_2^- .

Table III Non-selective etching of BPSG and THOX by low relative dielectric constant-solvents containing NH_4HF_2 or NH_4F

Solvent		Solute	Etching Rate		Selectivity
Solvent (Relative Dielectric Constant)	H_2O (%)		BPSG (A/min)	THOX (A/min)	(BPSG/ THOX)
IPA(19.9)	1.5	NH_4HF_2	52	58	0.90
IPA(19.9)	1.0	NH_4HF_2	18	19	0.95
CH_3COOH(6.15)	0.0	NH_4F	67	72	0.93
Ethanol(24.6)	1.5	NH_4HF_2	18	16	1.13
H_2O(78.3)	97.72	NH_4HF_2	358	44	8.14

And the other dissociation is not occur. Therefore, the framework of Si-O bond is only etched by HF_2^-, as a result non-selective etching can be achieved. It is considered that in the case of NH_4F addition to the CH_3COOH, because the dissociation constant of NH_4F is lager than that of CH_3COOH, the F^- from NH_4F combines with the H^+ form CH_3COOH to form only HF_2^-. As a result non-selective etching can be achieved.

TableIV shows the etching rate of various oxide films and selectivity to THOX by the IPA containing NH_4HF_2 and HF(0.25wt%)-NH_4F(40wt%)-H_2O.

As shown in this Table, in the case of IPA containing NH_4HF_2, it is possible that the selectivity of every oxide films to THOX are almost 1. As described above, in the case of NH_4HF_2 addition to low relative dielectric constant-solvents, the NH_4HF_2

only dissociates to NH_4^+ and HF_2^- . Therefore, the framework of Si-O bond is only etched by HF_2^-, as a result non-selective etching of every oxide film can be achieved. However, in the case of HF(0.25wt%)-NH_4F(40wt%)-H_2O, HF as well as HF_2^- consist in the solution. The selectivity become large under the influence of the property of oxide films.

Table IV Etching rate of various oxide films and selectivity to THOX by the IPA containing NH_4HF_2 and HF(0.25wt%)-NH_4F(40wt%)-H_2O.

NH_4HF_2-IPA-H_2O

	THOX	TEOS	BSG	BPSG	PSG	AsSG
Etching Rate(A/min)	38	47	48	39	43	40
Selectivity to THOX	-	1.24	1.26	1.03	1.13	1.05

HF:0.25%,NH4F:40%(200:1 BHF)

	THOX	TEOS	BSG	BPSG	PSG	AsSG
Etching Rate(A/min)	43	61	93	66	75	120
Selectivity to THOX	-	1.42	2.16	1.53	1.74	2.79

4. CONCLUSIONS

It has been studied that control of the etching rates of various oxide films by using the solvents which have low dielectric constant instead of H_2O which is generally used for the solvent of DHF and BHF. As the result, it has been demonstrated that the etching selectivity of doped oxide films to non-doped oxide films could be controlled almost 1 by the addition of NH_4HF_2 to the solvents which have low dielectric constant. It has been also demonstrated that the etching selectivity of BSG and BPSG to non-doped oxide films could be increased exceedingly by the addition of HF to the solvents which have low dielectric constant. These chemicals can be used for the cleaning of contact hole or selective removal of BSG and BPSG.

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$$HF \leftrightarrow H^+ + F^- \quad K_1=[H^+][F^-]/[HF]=0.0013$$

$$HF + F^- \leftrightarrow HF_2^- \quad K_2=[HF][F^-]/[HF_2^-]=0.104$$

Calculated Concentration 1wt%(0.5mol/kg)HF-99wt%H_2O

	Concentration
HF	0.408 mol/kg
HF_2^-	0.041 〃
H^+	0.051 〃
F^-	0.010 〃

Fig.1 Dissociation of HF in H_2O

$$HF \leftrightarrow H^+ + F^- \quad K_1=[H^+][F^-]/[HF]=0.0013$$

$$HF + F^- \leftrightarrow HF_2^- \quad K_2=[HF][F^-]/[HF_2^-]=0.104$$

$$NH_4F \leftrightarrow NH_4^+ + F^- \quad \alpha=[F^-]/[NH_4F]$$

Calculated Concentration
1%(0.5mol/kg)HF-40%NH_4F(10.81mol/kg)-59%H_2O

	Concentration
HF	0.010 mol/kg
HF_2^-	0.492 〃
H^+	2.7×10^{-6} 〃
F^-	4.916 〃

※) Calculated for $\alpha=0.5$

Fig. 2 Dissociation of BHF in H_2O

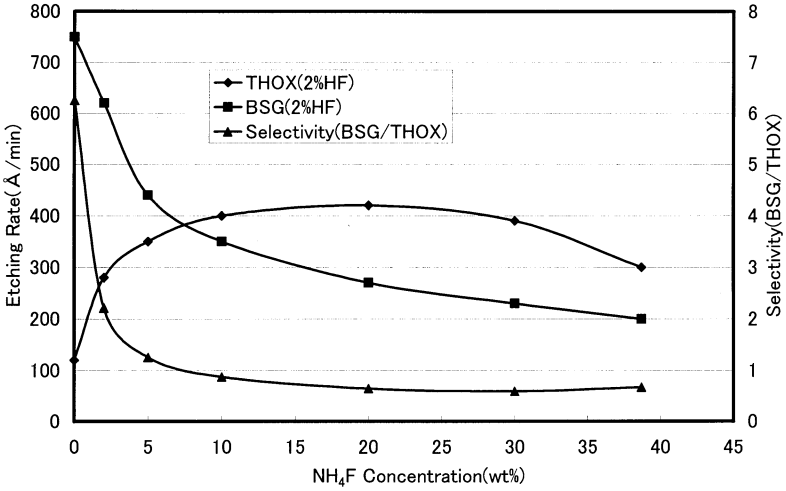

Fig.3 Dependence of etching rates and selectivity on NH_4F concentration(25deg.)

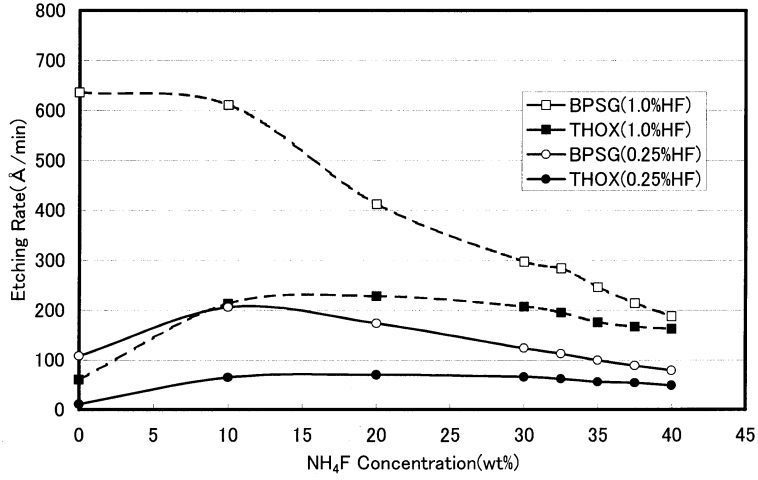

Fig.4 Dependence of etching rate and selectivity on NH_4F concentration(23deg.)

HF CONCENTRATION CONTROL IN IC MANUFACTURING

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ABSTRACT

The etching of SiO_2 layers from silicon surfaces is one of the most critical steps in wet processing technology. Although numerous studies have been performed to analyze the mechanisms and kinetics of these processes, little attention has been given to monitoring and controlling the chemical concentrations in the process baths. Chemical concentration control is becoming crucial to wafer processing in order to obtain consistency and more cost-effective IC manufacturing. This paper demonstrates the use of conductivity sensors to monitor and control the concentration of HF etching solutions. Effects of etch byproducts on the conductivity measurements have been investigated. Once the etch byproducts are characterized and accounted for, results showed that a much more stable etch process can be obtained and the bath life can be extended even in the presence of etch by products.

INTRODUCTION

Life of etching baths can be extended for longer periods of time if an accurate and continuous control of chemical concentrations is provided [1]. Compared to standard analytical techniques for chemical concentration e.g. NIR, UV spectroscopy [1], conductivity cells provide fast, very cost-effective, and real-time control of HF concentration. If the temperature is held constant, and the conductivity of the HF solution is maintained, the etch rate of SiO_2 can be accurately controlled as well [1].

Electrodeless conductivity sensors were used to accurately monitor and control the concentration of HF acid during the etching of thermal oxide from silicon surfaces [1]. However, the etch by-products can affect the linear conductivity-concentration relationship. This effect is magnified when etching thick oxide layers in dilute HF baths. A correction must be developed to correlate the amount of SiO_2 etched with the change in conductivity [2]. Results showed that these techniques are suitable for monitoring and controlling the etch rate in IC manufacturing environment.

EXPERIMENTAL

The experiment was performed on Akrion's Fully Automated GAMA wafer processing station in the Class 1 Application Laboratory at Akrion. Fifty 200-mm wafers with sufficient amounts of thermal oxide on both sides were prepared for the test. A standard HF process tank was used. The etching process was conducted at 21°C in an initially mixed 100:1 (H_2O:HF) HF bath. The conductivity sensor for monitoring the HF bath was calibrated and the reading for the aforementioned HF concentration typically

ranged from 6600 to 6800 μS/cm at 21°C. In addition, the bath's conductivity and temperature were recorded by a PC with automated data acquisition software.

For the test of etching process characterization, a lot of 50 oxide wafers were immersed in the HF bath for 3 hours, without deionized water or HF injection, followed by rinse and dry. The characteristic curve of conductivity versus etch time under the specific system setting was developed and used as a key parameter for the control scheme.

For the test of new algorithm evaluation, a batch of 50 oxide wafers was processed in the HF bath followed by rinse and dry. This process sequence was repeated, without chemical changeout, for 23 test runs. The chemical process time of each run was 25 minutes, which was estimated to have etched the oxide of 560 Å in thickness in a fresh HF bath. The actual etch rate for each run, however, was obtained using an ellipsometer to measure the oxide thickness change of the test wafers. The control system was activated to let the system spike whenever needed.

RESULTS AND DISCUSSION

Results showed that the etch by-products have an effect on the linear dependence of conductivity and HF concentration. Since HF is consumed in the reaction, one would expect that the conductivity should drop as wafers are introduced into the bath. However, it was observed that conductivity increased with the amount of SiO_2 etched in the bath while the oxide etch rate drops as shown in figure 1. This observation was again confirmed by immersing 50 oxide wafers (8") in the 0.5% HF bath for an extended time and monitoring the change in conductivity as illustrated in Fig. 2. The amount of SiO_2 can be calculated and the relationship of conductivity versus the amount of dissolved SiO_2 can be simulated as shown in Fig. 3.

Process Characterization

From Fig. 2 and 3, it is obvious that the bath's conductivity increased with process time regardless of the consumption of HF by oxide etching. The mass of dissolved SiO_2 from both sides of the wafers can be calculated as follows:

$$\text{Mass} = (\pi/4) \times D^2 \times (t \times 2) \times \rho \times N, \text{ where } t = ER \times \text{time} \quad (1)$$

where D is the diameter of the wafer; t is the removed oxide thickness on one side of the wafer (which can be obtained by multiplying average etch rate (ER) with the time), ρ is the density of the thermal oxide, and N is the number of wafers being processed. With the equation, process time can be converted to the dissolved SiO_2 mass, and the relationship of conductivity versus SiO_2 mass can then be plotted (Fig. 3). Using linear regression analysis, the slope of fitted data for the conductivity increment was estimated as 97.5 μS/cm·g, and it would serve as a key parameter specifying the process characteristics under the present sensor setting and test conditions.

Recognizing the trend of conductivity increment with the accumulation of dissolved SiO_2, a new control scheme was developed for the controlling software to prevent the system from being misled by the sensor to do unnecessary spikes. This can be expressed as follows:

$$\text{Conductivity}_{(n+1)} = \text{Conductivity}_{(n)} + (K \times \text{Mass}_{(n)} \text{ of dissolved } SiO_2) \quad (2)$$

where K is the slope of the conductivity/mass characterization curve, and n is an integer representing the n^{th} etching step since the HF bath is mixed. Given an estimated amount of oxide thickness to be removed, the conductivity setpoint would be renewed, according to equations 1 and 2, after each single etching process is completed. As such, the conductivity increment resulting from the effect of the dissolved oxide would be offset by the algorithm.

Evaluation of the Modified Control Scheme

Based on the findings shown in Fig. 3, the K value for the formula of the new algorithm was determined as 100, and was incorporated into the control scheme for the evaluation tests. The recorded conductivity readings, including those in the overnight process-free period, are presented in Fig. 4 showing the track of conductivity variation in detail.

In general, the new algorithm did govern the system to respond more properly than the old algorithm. For example, there would be no HF spike after Run #8 if the conductivity setpoint had not been reset with the incremental change by the new algorithm, and the etch rate thus would not have returned to the target value from 520 Å/25min at Run #6. The dramatic decrease of the etch rate starting from Run #5 to run #8 was due to disabling the process for a period of 5 minutes. With the exception of Runs #5 to #8, the bath conductivity for most of other runs actually increased faster than the predicted increment. This observation suggested that the conductivity/mass slope obtained from the 3-hour characterization test was unable to loyally reflect the dynamic nature of the process and oxide-induced conductivity change in a prolonged period. A more adequate slope parameter for better applications, therefore, needs to be identified. Analysis based on the experimental data obtained may provide a reasonable approach for the estimation. By neglecting the etch-rate trough (Runs #5 to #9), a line can be drawn across the actual conductivity data points in Fig. 4 from Run #1 to #13, reflecting a constant conductivity increment as 80 μS/cm per run. The corresponding etch rates for these processes (i.e. Runs #1 to #4 and #10 to #13) are relatively stable, with a value of about 560 Å/25min. Similarly, a line can also be drawn across the conductivity points from Runs #17 to #23 which show fairly constant etch rates of 530 Å/25min. The conductivity increment for these runs is 65 μS/cm per run. To have the new algorithm work properly, the setpoint increment should be consistent with the conductivity increment to offset the oxide effect. The setpoint change between two consecutive runs is thus identified ranging from 65 to 80 μS/cm per run for the specific experimental setting. We combine Eqs. 1 and 2 and convert them to a different form;

$$\Delta \text{ (Setpoint)} = K \times \text{Mass} = K \times (B \times t) \quad (3)$$

where B is a material constant including wafer diameter, density, lot size, etc. In the algorithm evaluation test, Δ (Setpoint) was 48 μS/cm per run with K = 100 μS/cm·g and t = 560 Å. Since B is fixed, a new slope parameter based on the data analysis aforementioned can be obtained; i.e. K = 166 μS/cm·g for Runs #1 to #13, or K = 143 μS/cm·g for Runs #17 to #23. An average K value of 155 μS/cm·g, therefore, may be used for the next experimental verification.

With a suitable K value incorporated into the algorithm, the adjustment of process parameters of the HF tank such as spike interval and duration and upper/lower conductivity control bands would then become significant in maintaining a stable HF concentration for oxide etching. During the course of the present experiment, the DI water replenishment was most frequently observed. The loss of bath liquid is mainly due to liquid evaporation and dragging by the product/carrier. The former is a time-dependent process at a constant bath temperature, while the latter would be determined by the throughput for a fixed carrier and lot size (surface area). The evaporation rate of the bath was estimated to be about 130 ml/hr. while the liquid carried away by the product/carrier was estimated as 70 ml per lot. These values plus the HF spike rate of about 7 ml/sec, whenever required, would provide a baseline for the determination of some process-specific settings.

Recognizing the trend of conductivity increment with the accumulation of dissolved SiO_2, a new algorithm was developed to prevent the system from injecting unnecessary HF or water. Given an estimated amount of oxide thickness to be removed, the conductivity setpoint would be renewed after each single etching process is completed. As such, the algorithm would offset the conductivity increment resulting from the effect of the dissolved oxide, and the control system would meet the process requirements. The modification enabled the system to respond more accurately compared to the situation where the effect of etch by-products was neglected. As shown in figures 5 and 6, the etch rate stayed within limits for almost 7 days.

Analysis

The total molar conductivity of a solution is based on each ion's individual conductivity contribution for infinitely dilute solutions. When solutions become more concentrated, ion-ion interactions increase. These interactions, as well as the presence of other species (primarily HF_2^-, H^+, and F^-), lead to an observed (measured) conductivity value of approximately 6200 µS/cm for 1:100 HF:H_2O mix. Nevertheless, it is plainly shown that the conductivity of a freshly mixed solution is primarily based on the concentration of H^+, or in this case the 0.6 moles present in a solution of 50 liters.

At this point, the amount of chemical byproduct formed in an HF etching reaction needs to be determined. Using the chemical reaction equation below:

$$6HF + SiO_2 >>>>>> H_2SiF_6 + 2\,H_2O \qquad (4)$$

To etch 560 Å from two sides of 50 (200 mm) wafers, the total amount in grams of SiO_2 removed will equal to 0.399 grams (density = 2.27 g/cm^3) of SiO_2 or 0.00664 moles.

Since HF is being consumed, or 0.00664 moles x 6 = 0.04 moles for each run of 50 wafers, the concentration of H^+ and F^- will also be smaller. However, this amount when compared to initial amount of HF (11.45 moles) can be significant after processing many wafers in the HF bath. The slope (or correction factor) from figures 2 and 3 was obtained assuming a constant etch rate during the 3 hour test period (equivalent to 7 manufacturing runs i.e. 180 min / 25.667 min. per run = 7 runs). However, that is not true since the HF is being consumed. It is estimated that about 2.45% of the HF were consumed during the

immersion test as can be seen from figures 2 and 3. A quick estimate of the ratio between the etch byproduct and the total concentration of the conductive species $[H^+]$ (from both HF and H_2SiF_6) can be summarized in the following example (0.5% HF in 50 liter bath):

Run #	HF, moles	HF, moles/l	H_2SiF_6, moles	$[H^+]$, moles/l
0	11.45	0.229	0.0	0.01284
7 (no spike)	11.17	0.223	0.04648	0.01364
7 (HF spike)	11.45	0.229	0.04648	0.01380

It can be easily seen from the table above that the contribution of H_2SiF_6 to the conductivity as represented by $[H^+]$ for these 7 runs is (0.01364-0.01284)/0.01284 = 0.062 or 6.2%. This increase in the conductivity of the byproduct (H_2SiF_6) must be accounted for i.e. this increase should be eliminated in order for the conductivity to remain as a true indication of the HF concentration. In addition, the decrease in HF concentration during these runs must be also compensated for in order to maintain a constant etch rate. Thus, an additional correction factor was used on top of that obtained from figure 2 and 3 to compensate for the consumed HF and offset the increase in conductivity due to the etch byproducts. Clearly, a correction to the conductivity measurement is deemed necessary. These estimates are in good agreement with manufacturing data. As shown in figures 5 and 6, the etch rate is within the manufacturing acceptable range once the proper correction is made.

CONCLUSIONS

Results showed that controlled HF processes were significantly improved when compared to conventional processes without concentration control. The effect of etch by-products was correlated with the change in HF conductivity and has to be considered in the control scheme. When etching thick oxides in dilute HF solutions, the linear properties of bath conductivity versus HF concentration would be considerably affected by the accumulation of dissolved ionic products. The development of an empirical relationship between the bath conductivity and the amount of etched oxides was found necessary. Validation testing of the developed algorithm to retain stable etch rates in an extended HF bath life has been conducted on a production tool. The on-site experiment demonstrated the effectiveness of the new algorithm in achieving etch rates in a 585 Å ± 2.5% range over 7-day bath life. However, extending the bath life greater than 7 days is not recommended due to 1) the risk of building up high levels of contaminants in the bath, and 2) the possible breakdown of the linear assumption between the mass of etched oxides and bath conductivity.

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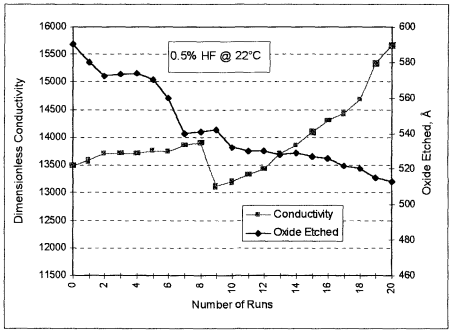

Figure 1: Effect of Dissolved SiO_2 on Etch Rate and Bath Conductivity

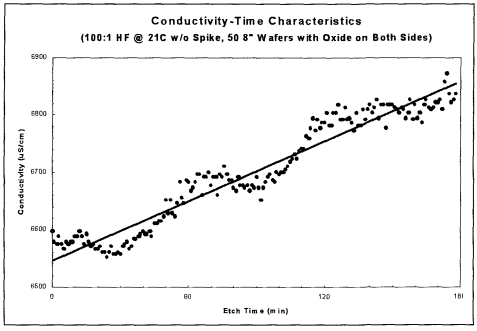

Figure 2: Characterization of Conductivity versus time in DHF processes.

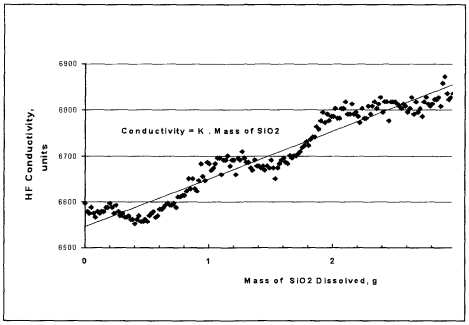

Figure 3: Characterization of Dissolved SiO_2 in DHF processes.

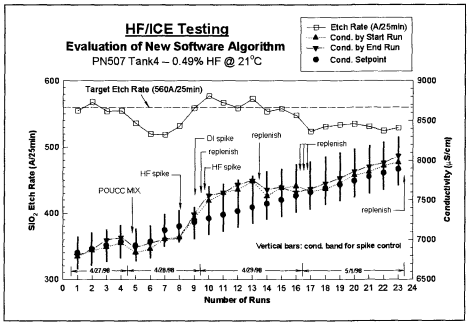

Figure 4: Etch Rate versus Time with Conductivity Corrected.

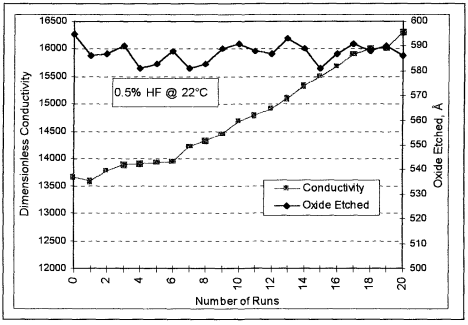

Figure 5: Stability of SiO_2 Etch Rate with Modified Algorithm.

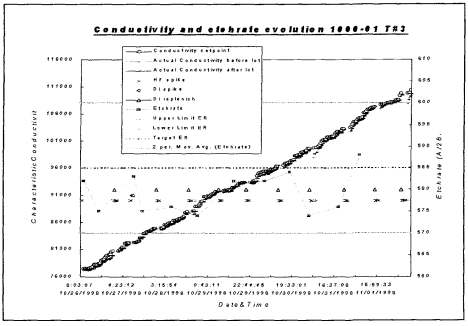

Figure 6: Stability of SiO2 Etch Rate in DHF processes during IC Manufacturing.

ETCHING SILICON NITRIDE AND SILICON OXIDE USING ETHYLENE GLYCOL / HYDROFLUORIC ACID MIXTURES

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ABSTRACT

Concentrated (49%) aqueous HF and ethylene glycol solutions were investigated for a wet strip process requiring a LPCVD Si_3N_4 to thermal SiO_2 etch rate selectivity of between 1 and 2. Si_3N_4 etch rates of higher than 20 nm per minute were also desired to obtain high throughputs on the single-wafer spray tool. Water, temperature, and HF concentration were found to play a significant role in defining both the etch rates and etch-rate selectivity of LPCVD Si_3N_4 and thermal SiO_2 films. The desired Si_3N_4 : SiO_2 selectivity was achieved at low HF concentrations; at higher HF concentrations, the selectivity decreased rapidly below 1. Water additions to the system produced similar results. Particulate contamination levels were also significantly reduced when a deionized water rinse was used.

INTRODUCTION

As integrated circuit devices continue to use chemically vapor-deposited (CVD) Si_3N_4 and SiO_2 film stacks, the need to develop and improve upon selective etching of either of these films continues. The use of high-aspect ratio trenches in integrated circuit devices has made selective nitride-to-oxide etching a beneficial step in improving the ability to fill the trenches with dielectric by laterally etching both the nitride and oxide films away from the opening of the trench. A nitride-to-oxide selectivity of greater than 1 is required to pull back the nitride and prevent undercutting of the underlying oxide layer.

Several different HF and hydroxylated organic solvents have been previously identified as etching CVD nitride films faster than oxide films at temperatures above 80 °C. While much has been studied on HF etching of oxide in aqueous solutions, little is understood about the effects solvents have in suppressing the normally high oxide etching ability of HF. This paper addresses the characteristics of both HF/polyethylene glycol-200 (PEG 200) and HF/ethylene glycol solutions and suggests a possible mechanism.

EXPERIMENTAL TECHNIQUE

HF/ethylene glycol solutions were prepared by mixing a specified volume of concentrated (49%) aqueous HF with semiconductor grade ethylene glycol. The ethylene glycol used had less than 1% water. HF/PEG 200 solutions were prepared by mixing a specified volume of concentrated (70%) aqueous HF with semiconductor grade PEG 200. The PEG 200 also had less than 1% water.

For the etch rate tests, the Si_3N_4 monitors were prepared by depositing 175nm of LPCVD (770 °C, 115 m Torr) nitride on bare silicon wafers. The wafers were then processed through a 5nm HF oxide etch and megasonic SC-1/SC-2 clean to remove surface particles. The SiO_2 monitors were prepared by growing approximately 350 nm of thermal oxide on bare silicon wafers in a wet oxidation at 1050 °C at atmospheric pressure. The monitor wafers were measured using an ellipsometer. Fifteen sites were measured edge to edge across the middle of a wafer, and film removal was measured at each site. The average was calculated from the 15 differences in film thickness.

All etch rate tests, except the beaker tests, were performed on a SEZ single wafer spray tool, with temperatures measured at the medium tank, not at point of use.

RESULTS/ DISCUSSION

LPCVD nitride and thermal oxide etch rates were characterized for concentrated (49%) aqueous HF solutions in different ethylene glycols. The dependence of oxide and nitride etch rates on HF concentration at 80 °C for PEG 200 and ethylene glycol is shown in Figures 1 and 2, respectively. Both the nitride and oxide etch rates increase with rising HF concentration in both solvent solutions. However, the rate of increase for the oxide etch is quicker than that of the nitride. A transition point can be seen in the ethylene glycol system where the oxide etch rate eventually exceeds the nitride etch rate. This was also seen in the HF/PEG 200 system when an excess of HF was added to the system; however, the HF concentration was never quantified for these results.

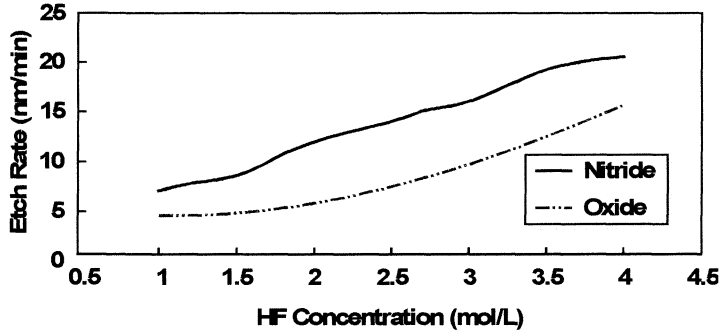

Figure 1. Etch rate of HF/PEG 200 as a function of HF concentration.

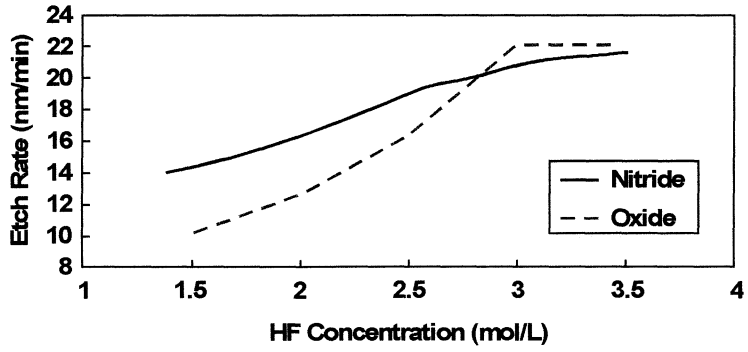

Figure 2. Etch rate HF/ethylene glycol as a function of HF concentration.

A temperature study between the range of 75 °C to 85 °C was also done on 3M HF/ethylene glycol solutions to study the effects temperature has on the CVD nitride and thermal oxide etch rates. The results are shown in Figure 3. As expected, the CVD nitride and thermal oxide etch rates decreased with decreasing temperature; however, at this concentration, the nitride-to-oxide selectivity remained fairly constant.

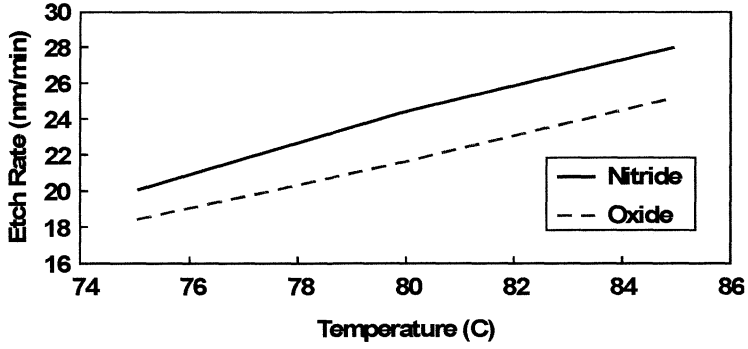

Figure 3. Etch rate HF/ethylene glycol as a function of temperature.

The results in Figure 3 show the potential that HF/solvent systems have for tailoring nitride and oxide etching for a variety of purposes. It is advantageous to have higher oxide and nitride etch rates to reduce overall processing times. However, bath life times are also a factor, and reducing the HF concentration and temperature needed to obtain a desirable etch rate helps to extend the bath life in a recirculated system because less HF is lost during processing. Temperatures between 75 °C and 85 °C and concentrations between 2 M and 3M were found to be optimum for creating a stable recirculated mixture with minimal HF spiking to maintain nitride and oxide etch rates at 20 nm/minute and 17 nm/minute, respectively.

Additional etch rate tests were performed with HF/glycol/ water mixtures to study the effect of water concentration. Table 1 shows both nitride and oxide etch rates achieved in different HF/PEG 200 mixtures at 80 °C; S is the nitride-to-oxide etch rate selectivity. The water concentration was varied by two methods: using a different wt % concentration of HF and a polyethylene glycol of a different water volume. The water-free PEG 200 mixtures used polyethylene glycol distilled by the chemical manufacturer to remove any water. The PEG 200 used in the third mixture contained 2% water by volume.

Table I. Etch rates of CVD nitride and thermal oxide in different HF/ PEG 200 mixtures

	PEG 200 water-free/ HF 70%			**PEG 200 water-free/ HF 49%**			**PEG 200 / HF 49%**		
[HF] (M)	Oxide (nm/min)	Nitride (nm/min)	S	Oxide (nm/min)	Nitride (nm/min)	S	Oxide (nm/min)	Nitride (nm/min)	S
1	1.5	1.1	0.73	1.7	2.8	1.65	4.2	7	1.67
1.5	2.9	1.7	0.58				4.3	8.4	1.95
2	5.9	5.3	0.9	5	14.3	2.86	5.5	11.8	2.15
2.5	7.9	7.4	0.94				7.3	13.9	1.9
3	9.3	9.4	1.01	12.8	14.3	1.12	9.5	15.6	1.64
3.5	9.3	12	1.29				11.9	18.8	1.58
4	12.8	12.6	0.98	17.3	12.2	0.71	15.1	19.6	1.3

It appears that water plays a role in defining the etch characteristics of the solution because the lowest CVD nitride and thermal oxide etch rates and nitride-to-oxide selectivities were found in the PEG 200 water-free/ HF (70%wt) solutions. A minimal amount of water is necessary to achieve nitride-to-oxide selectivities greater than 1. With increasing water concentration, both the oxide and nitride etch rates are higher for the corresponding HF concentrations. While these tests show that water is necessary for etching both oxide and nitride, they do not show the entire picture. Table 2 shows etch rates of PEG 200 and ethylene glycol mixtures in beaker tests with water concentration varying on a larger scale.

Table II. Etch rates (nm/min) of CVD Si_3N_4 and Thermal SiO_2 in HF/ glycol/water solutions.

Mixture	Si_3N_4 etch rate (nm/min)	SiO_2 etch rate (nm/min)	Etch Rate Selectivity Si_3N_4:SiO_2
3M HF/Ethylene glycol	31	26	1.2
3M HF/ Ethylene glycol 10% vol. H_2O	32	55	0.6
3M HF/ PEG 200	29	19	1.5
3M HF/ PEG 20010% vol. H_2O	33	43	0.77

For a given HF concentration in a solvent system, excess water clearly accelerates the oxide etch rate relative to the nitride etch rate. Given what is known of oxide etching, these results are not surprising. In an aqueous system, ionization of HF proceeds in two steps (2):

$$H_2O + HF \leftrightarrow H_3O^+ + F^-$$

$$HF + F^- \leftrightarrow HF_2^-$$

HF_2- is known to be primarily responsible for etching oxide. Water acts as a Bronsted-Lowry base, accepting a proton from HF. For ionization of HF to occur in a HF/ glycol mixture, either water or glycol would need to be a proton acceptor. The results in Table 2 and Figure 3 suggest that very little disassociation of HF occurs without the presence of water; therefore, the proton acceptor in the solution is not the solvent.

While the solvent does not appear to play a role in the disassociation of HF, it does play a role in defining the etch characteristics of the solution. The results in Table 2 suggest that water in an ethylene glycol mixture is more available for interaction with HF than in a PEG 200 mixture. It seems most probable that the solvent is absorbing water and, consequently, preventing disassociation of HF.

It is important to note that with rising HF concentration, both the nitride and oxide etch rates increase. The rate of increase for the oxide etch rate is much faster, suggesting that, while HF_2- is responsible for oxide etching, it is not responsible for nitride etching.

Beaker etch rate tests were also performed with different chemicals to better understand the species involved in nitride etching. Several different types of HF/ ethylene glycol solutions were prepared, and etch rate removals performed at 90 °C. The results of these experiments are listed in Table 3. All ethylene glycol solutions used were 3M HF.

Table III. Etch rates (nm/min) of CVD Si_3N_4 and thermal SiO_2 in HF/ethylene glycol solutions.

Mixture	Si_3N_4 etch rate (nm/min)	SiO_2 etch rate (nm/min)	Nitride-to-Oxide Selectivity
3M HF/ ethylene glycol	31	26	1.2
3M HF/ ethylene glycol (10% volume H_2O)	32	55	0.6
3M HF/ ethylene glycol (1M HCl)	27	76	0.4
3M HF/ ethylene glycol (0 .1 M HCl)	30	24	1.25
3M HF/ ethylene glycol (1 .5M NH_4F)	30	64	0.5

A small increase in the nitride-to-oxide etch rate selectivity was observed with small additions of HCl. However, with larger volumes of HCl, there was a remarkable increase in the oxide etch rate which lowered the etch rate selectivity. While an increase of selectivity seems intuitive with small additions of HCl due to reduced HF ionization, the mechanism occurring at very large volumes of HCl in solution is unknown. As was reported by Deckert (1), NH_4F additions drops the nitride-to-oxide selectivity remarkably. This corresponds with what is known about buffered oxide etching (mentioned above).

CONCLUSIONS

Concentrated (49%) aqueous HF and ethylene glycol solutions have been characterized for their nitride and oxide etching properties. The effects of temperature, HF concentration, and water were defined for both ethylene glycol and PEG 200 systems. Temperature had little effect on the nitride-to-oxide etch rate selectivity but enhanced both the nitride and oxide etch rates.

Water and HF concentration played an essential role in oxide and nitride etching in the hydroxylated solvent mixtures studied. While necessary for nitride and oxide etching, an abundance of water or HF promoted the oxide etch rate significantly enough to lower the nitride-to-oxide etch rate selectivity below 1.

Overall, a process was developed that can easily adjust etch rates and nitride-to-oxide selectivity. This provides the flexibility to tailor a process to several different situations where it is advantageous to etch both CVD Si_3N_4 and SiO_2 at rates closer than what is normally achieved by dilute HF solutions.

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Etching mechanism of Si and SiO_2 in the SC1 solution

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Abstract

The effects of ionic species and molecules in the SC-1 solution on the silicon and silicon-dioxide substrates have been studied. The silicon surface is etched by not only hydroxide ions but also ammonia molecules, depending on the pH of the solution. The main etching species is the ammonia molecule in SC-1 solutions at pH>10, and at pH<10, the hydroxide ion becomes dominant. In the solution of pH 10.5, the etching speed of silicon by the ammonia molecule is approximately five times faster than that of the hydroxide ion.

Silicon oxide is etched by hydroxide ions but the etching speed of SC-1 solutions is faster than that of ammonium hydroxide solutions when the pH is the same. The hydroperoxide ion may play am important role on the etching rate.

The concentration of ammonia molecules and hydroperoxide ions must be specified when the composition of SC-1 solutions is optimized.

Introduction

In semiconductor manufacturing, RCA cleaning(1) is widely used for removing particles and metallic contamination. Among the cleaning steps, the mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and water, known as SC-1 solution is good for removing particles and has become the most important cleaning technique in the manufacture of sub-micron devices. On the other hand, SC-1 cleaning is associated with the degradation of surface smoothness. An increase of silicon surface micro-roughness results in a reduction in the breakdown of electric field intensity (E_{bd}) and time dependent dielectric breakdown (Q_{bd})(2)(3).

Although there have been many literatures reports that optimized the composition of the SC-1 solution to remove particles without degrading the surface smoothness(4)(5), very few reports have studied the mechanism of etching of silicon in the SC-1. In this study, the effects of ionic species and molecules on the etching rate of silicon in various alkaline solutions were measured and the etching species were determined.

Experimental

SC-1 solutions were prepared by mixing de-ionized water with an NH_4OH solution (28%) and a H_2O_2 solution (30%). The water was heated to a temperature such that the addition of NH_4OH and H_2O_2 resulted in 80°C solutions. The pH of the solutions was measured by a pH meter, Beckman 44.

The etching rate of silicon was measured by the procedure as in Fig. 1. Silicon

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wafers, CZ(100) p-type, were thermally oxidized to a depth of 50nm and 1 mm line and space photo resist patterns were formed. The masked wafers were then treated in buffered hydrofluoric acid (HF=2.3%, NH_4F=38%) for 5 minutes to remove the thermal oxide. The silicon wafers were treated in the solutions after removal of the photo resist. The oxidized layer was removed by the buffered hydrofluoric acid and the etched depth was measured by an atomic force microscope (AFM), Digital Instruments Nano-Scope 3. The infrared spectrum (IR) of silicon surfaces was taken with Bio-Rad Digilab FTS-60A using ATR accessory with a germanium prism.

Results and discussion

In alkaline solutions such as potassium hydroxide (KOH) or tetramethyl ammonium hydroxide (TMAH), the etching species of silicon is hydroxide ions(6)(7) and the reaction speed is expressed as equation[1].

$$\text{Reaction speed (or Etching rate)} = a \times [OH^-]^b \qquad [1]$$

a , b : constants.

$[OH^-]$: Concentration of hydroxide ions

Fig. 2 shows the relationship between the logarithm of the etching rate and the log of the $[OH^-]$ from either KOH or TMAH solutions. The etching rate increases as increasing the concentration of hydroxide ion. Since the reaction speed is expressed as equation 1, a linear relationship is observed in Fig. 2. This is well established in micro machining with KOH or TMAH. In contrast, there is not the linear relationship in NH_4OH solutions as shown in Fig. 3. The logarithm of the etching rate shows distinct slopes; one at $\log[OH^-]<-4$ and the other at $\log[OH^-]>-4$. This implies that two etching species exist in the NH_4OH solution, they are hydroxide ions and ammonia molecules. The etching species in the later region may be NH_3 molecules because they have a unshared electron pair that can cause nucleophilic reaction with silicon(8). Fig. 4 shows the relationship between the logarithm of the etching rate and the log of the $[OH^-]$ in dimethylamine solutions that also have an unshared electron pair. The same distinct slopes are observed as in NH_4OH solutions.

The effect of NH_3 molecule concentration on the etching rate of silicon is shown in Fig. 5. The concentration of NH_3 was changed by addition of NH_4Cl to NH_4OH solutions and the pH is adjusted at 9 and 10. A linear relationship is observed, and it does not depend on pH. Moreover, the slope or reaction order is the same as that of NH_4OH and the etching speed is expressed as equation [2].

$$\text{Etching speed} = 5.2 \times [NH_3]^{0.54} \qquad [2]$$

From these facts, it can be determined that the etching species at $\log[OH^-]>-4$ is the NH_3 molecule. On the other hand, the etching speed determined by hydroxide is expressed as equation 3. The etching by the ammonia molecule ion at pH10.5 ammonia solution is approximately five times faster than that of the hydroxide.

The silicon surface etched by ammonia molecule is evaluated with IR and AFM. Fig. 6 is the IR spectrum of silicon etched in diluted ammonium hydroxide solution at pH of 10.5. With increasing etching time, the silicon di-hydride peak at 2150cm-1 decreases and the silicon mono-hydride peak emerges at 2050cm-1(9). Further etching produces

pyramid like bumps as in Fig. 7. These facts indicate that the Si(111) surface emerges by etching the Si(100) surface in the NH_4OH solution as etched in strong alkaline solutions such as KOH or TMAH(10). Fig.8 shows the relationship between the surface roughness and etched depth in NH_4OH compared to KOH and TMAH. The surface roughness increases with the etching depth and the degree of the roughening is independent of the solution. Since the dominant etching species in the ammonium hydroxide solution is the ammonia molecule, it is said that ammonia molecules degrade the surface smoothness of silicon as well as hydroxide ions. Note that the number of ammonia molecules in the SC-1 solution is approximately 5,000 times more than hydroxide ions.

In case of using SC-1 solution at higher than pH10, surface roughening by ammonia molecule must be taken into account and the concentration of ammonia molecule must be specified.

Silicon dioxide is etched by hydroxide ions (11). The logarithm of the etching rates either NH_4OH or the SC-1 solutions are plotted against the log of the $[OH^-]$ in Fig.9. The linear relationship is observed in all the solutions expressed as in equations [3] and [4], but the reaction order of the SC-1 solutions is different from that of KOH and NH_4OH. The etching rate in the SC-1 solution is higher than in ammonium hydroxide solution at the same pH.

SC-1:

$$\text{Etching rate} = 3.6 \times [OH^-]^{0.7} \quad [3]$$

KOH and NH_4OH :

$$\text{Etching rate} = 9.4 \times [OH^-]^{1.1} \quad [4]$$

The $[HO_2^-]$ may play an important role in SiO_2 etching in the SC-1 solution and the effect is currently being studied.

As indicated above, concentrations of ionic species and molecules in the solution must be specified to prevent roughening the silicon surface or excess etching of silicon oxide. The important thing in calculating the concentration is that semi-empirical factors are required. Although the diluted SC-1 solutions are used in semiconductor manufacturing these days, the ionic strength of the solutions is too strong to apply Devi-Fukkel theory (12). Fig. 10 demonstrates the deviation of the calculated pH and actual value in NH_4OH and H_2O_2 solutions. Good agreements are observed in both solutions at low concentration. As the concentration is increased, the deviation becomes obvious.

Conclusions

The etching species of silicon in the SC-1 solution has been determined. The main etchant is the ammonia molecule in the solutions at pH>10, and at pH<10, the hydroxide ion becomes dominant. Ammonia molecules roughen the silicon surface as well as hydroxide ions. To maintain the surface smoothness during SC-1 cleaning, the concentration of ammonia molecule must be minimized.

Silicon oxide is etched by hydroxide ions but the etching speed of SC-1 solutions is faster than that of ammonium hydroxide solutions when the pH is the same.

Concentrations of ionic species and molecules in the solution must be calculated precisely to prevent roughening the silicon surface or excess etching of silicon oxide. The

important thing to note calculating the concentrations is that semi-empirical factors are required because the ionic strength of the SC-1 solutions used in the semiconductor manufacturing is so strong that Devi-Fukkel equation can't be applied.

Acknowledgements

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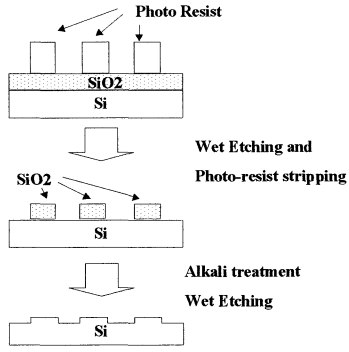

Fig. 1 The process flow for measuring etching rate of silicon

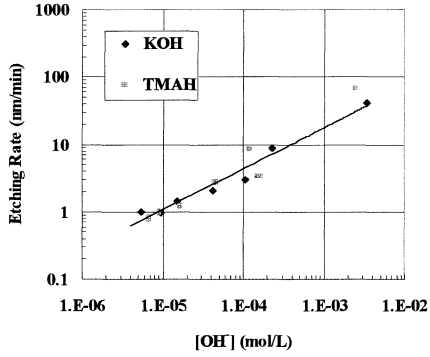

Fig. 2 Etching Rate of silicon in dimethylamine solutions

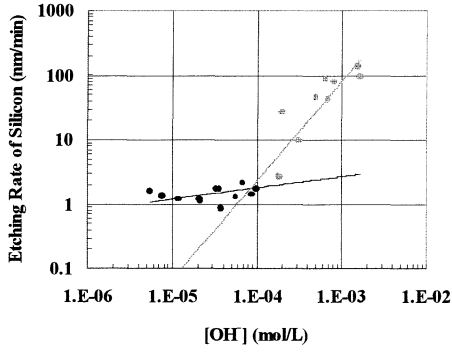

Fig.3 Etching Rate of silicon in dimethylamine solutions

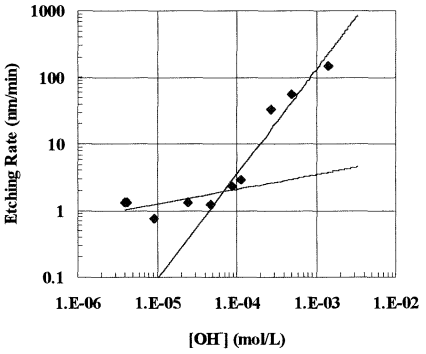

Fig. 4 Etching Rate of silicon in dimethylamine solutions

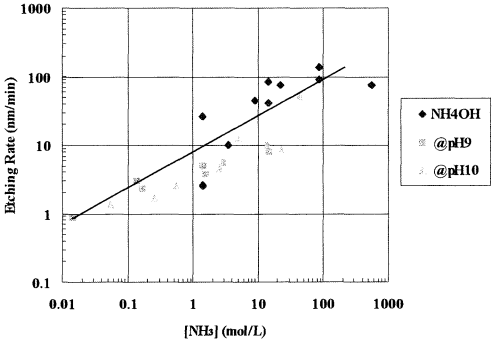

Fig. 5 The Effeect of NH3 molecules on the etching rate of silicon

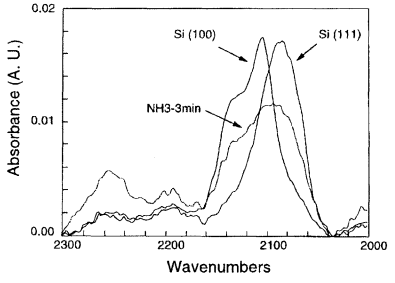

Fig.6 IR spectrum of silicon after NH4OH treatment

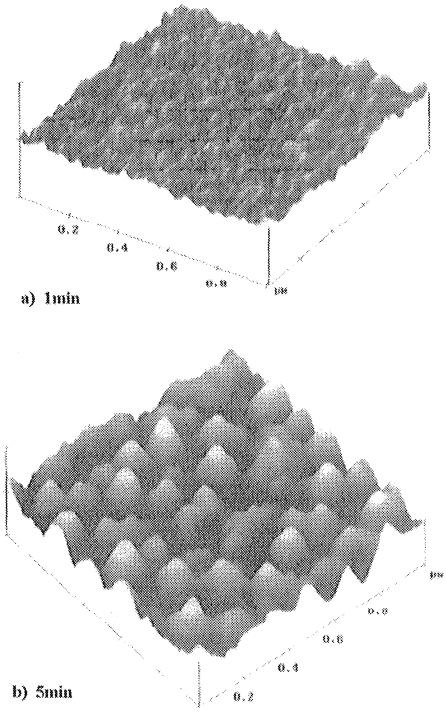

Fig. 7 AFM pictures of the silicon surface etched by NH3

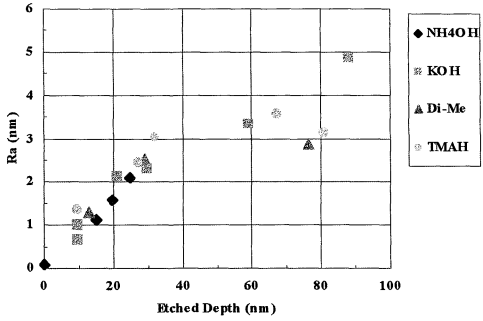

Fig. 8 The relationship between the surface smoothness and etched depth in various alkaline solutions

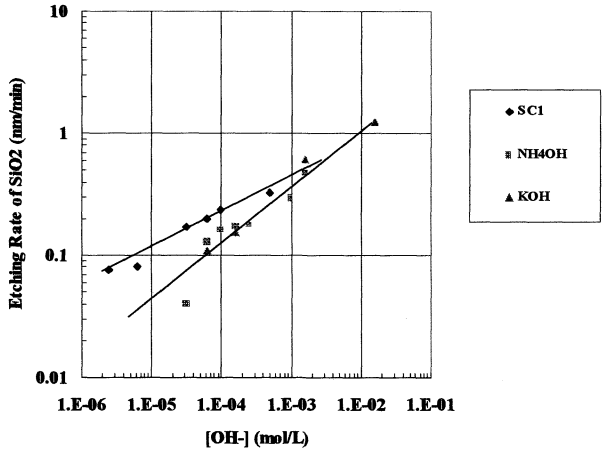

Fig.9 Etching rates of SiO2 in alkaline solutions

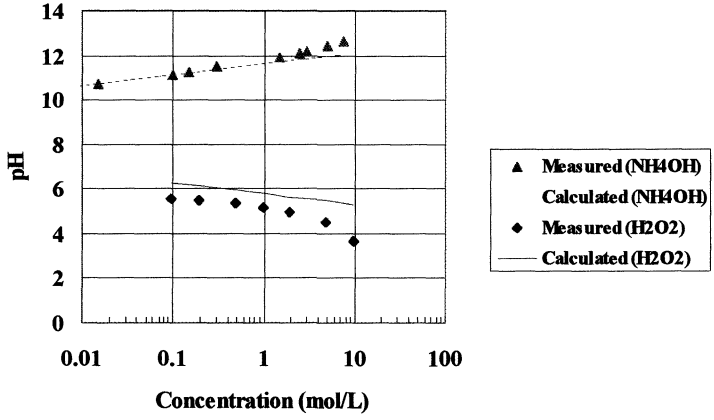

Fig. 10 The comparision of pH between measured and calculated values

DEPENDENCE OF COPPER IMPURITY REMOVAL EFFICIENCY ON SUBSTRATES ETCHING RATE FOR VARIOUS SUBSTRATES IN HYDROFLUORIC SOLUTIONS

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ABSTRACT

We have investigated the removal efficiency of copper impurities on various surface crystal structures. The study reveals that it depends on surface crystal structure. The copper impurities on phosphorus doped amorphous silicon (a-Si) are hardly removed by a hydrofluoric acid-hydrogen peroxide mixture (FPM) cleaning while are easily removed on single crystalline silicon (c-Si). A hydrofluoric acid-hydrogen peroxide mixture with non-ionic surfactant (FPMS) cleaning, however, can efficiently remove copper contaminants on both c-Si and a-Si surfaces. We suppose that both silicon etching by FPM solution and surface passivation by surfactant are essential to remove copper contaminants on a-Si surface. The etching rate difference of c-Si and a-Si surfaces has a relationship of interaction force between substrate and copper particles. This is attributed to the difference in crystalline structure between c-Si and a-Si.

INTRODUCTION

As the requirements for device performance and reliability have become stringent in the gigascale integration (GSI) silicon devices, wafer cleaning technology to produce ultraclean wafer surface is critically important [1]. It is well known that metallic contaminants on silicon surface are fatal to semiconductor device [2-3]. Therefore, it is seriously required to control metallic impurities on the wafer surface at least until their level does not affect device characteristics [4]. In most of the reported studies for metallic impurities, c-Si surface was selected as a substrate, whereas semiconductor device is

composed of various films such as a-Si, poly-Si, oxide, nitride, and metallic films. It is not clear whether the adsorption characteristics and the removal efficiency on various films are same or not compared to that on c-Si surface.

From the continuous research on metallic impurities versus substrate conditions, however, we found evidence of two kinds of important data that gave results for Cu impurities. These results can be easily extended to other impurities of noble metals with high Oxidation Reduction Potential (ORP) values, such as Ag and Au. First, the adsorption characteristics of Cu impurity on a-Si surface of various film surfaces is quite different from that on c-Si [5-6]. Second, the Cu impurity on a-Si is not removed by RCA cleaning solutions such as SPM, SC-1, and SC-2 cleanings which are currently used for device fabrication [7]. FPMS cleaning, however, can only remove Cu impurity from both c-Si and a-Si surfaces. In this paper, a new model for its removal on silicon substrates is described.

EXPERIMENTAL

A phosphorus doped amorphous silicon (a-Si) film in this study was deposited in a hot wall type low pressure chemical vapor deposition (LPCVD) system, which deposition temperature was 510°C. It is using Si_2H_6 *in-situ* doped by a 1% diluted PH_3 gas with nitrogen and the c-Si (n-type Cz, phosphorus doped Si (100) 7-12 Ω.cm) was used as a reference. They were firstly cleaned with a sulfuric acid-hydrogen peroxide mixture (SPM, H_2SO_4/H_2O_2 = 4/1 at 90°C) to remove metallic and organic impurities on the surface. The native oxide grown during SPM cleaning was etched off by 1min dip in a 0.5% HF solution. The Cu concentration in the solution was set to 1 ppm Cu using $CuCl_2$ in ultrapure water (UPW) with a resistivity of 18.2 MΩ.cm for all dipping solutions. Samples were dipped for 3 min, rinsed for 10 min in UPW and dried using ultrapure nitrogen gas. The metallic contamination level on the substrate was measured by a Total Reflection X-Ray Fluorescence (TRXRF) with an incident angle of 0.05 degree and X-ray excitation of 30 kV and 200 mA. Surface morphology after contamination was observed by a Scanning Electron Microscope (SEM) with normal incidence angle. Finally, X-Ray Photoelectron Spectroscopy (XPS) for native oxide thickness measurement was carried out in a Scienta ESCA-300 system with monochromatic Al-Kα and acceptance angle of 3.3 degree. Take-off angle was adjusted to 5 degree and yield of $Si_{2p3/2}$ peak was set over 10^5 counts per second (CPS).

RESULTS AND DISCUSSION

Figure 1 shows the Cu impurity removal efficiency on c-Si surface versus various HF solution cleanings such as a dilute HF (dHF), FPM, and FPMS. On c-Si surface in FPM and FPMS solution with more than 500 ppm HF concentration, the Cu impurities are perfectly removed, while in dHF only is rarely removed irrespective of HF concentration.

The Cu removal efficiency on c-Si seems not to be related to the presence of surfactant in FPM solution. Figure 2 shows the dependence of Cu removal efficiency on a-Si surface on various HF solutions. It has different results between FPM and FPMS cleaning compared to that on c-Si. FPMS solutions with a high HF concentration more than 2.5 w.t % can remove the Cu impurity on a-Si surface, while FPM and dHF cleanings are not effective to remove it irrespective of concentration and cleaning time. A large number of Metallic Induced Pits (MIPs) on a-Si after cleaning in high HF concentration were observed by SEM inspection. From these results, we suppose that Cu removal from surface is decided by 3 kinds of key reaction rates, namely (a) the amount of electron tunneling from surface, (b) native oxide growth by Metal Induced Oxidation (MIO) between metallic impurities and substrate [8], (c) Cu dissolution reaction with pH and ORP values, and the amount of oxidants in HF solution (see fig.3). In order to explain removal rate of metallic impurity, we should consider the relationship among all reaction rates, because the removal efficiency is affected by all three reactions. These reactions are different when considering different metallic impurity species, their dissolution characteristics (pH and ORP values) and Fermi level difference between the impurities and the substrate chosen. The authors point out that the metallic impurity removal is increasing by acting on two different factors: the dissolution rate of metallic impurity has to increase and the interaction force between impurity and substrate has to decrease in order to allow a low occurrence of electron tunneling from the substrate.

Figure 4 shows the etching rate of Cu contaminated silicon surfaces in a 0.5% HF solution. Silicon surfaces before substrate etching were contaminated for 3 min in UPW spiked with 1000 ppm Cu using $CuCl_2$. The etch rate of a-Si surface is more than one order of magnitude faster than that of c-Si. It is supposed that the etching rate has a relationship of interaction force difference between substrate and Cu particles [9]. Figure 5 shows the etching rate of various substrates in dHF solutions. The etching rate of thermal oxide is not changed by adding H_2O_2 or surfactant in HF solution. The etching rate of c-Si and a-Si on adding surfactant in FPM solution, however, is suddenly decreased. This difference has a relationship with the oxidation rate of silicon or etching rate of native oxide by HF solution. Figure 6 shows native oxide growth on Cu-contaminated c-Si surfaces in a 0.5% H_2O_2 solution added with surfactant, which is much thicker than not-contaminated surface in the early stage. The native oxide growth rate showed a large decrease on adding the surfactant in a 0.5% H_2O_2. As far as Cu impurities are increasing the oxidation rate, silicon is consumed and native oxide grown by MIO is etched by HF. Since oxidation rate of silicon is reduced to one-third in the initial stage as is shown in fig.6, the etching rate in FPMS solution is also decreased. Figure 7 shows the etching rate of a sputter deposited Cu film for various HF solutions. On increasing HF concentration in FPM or FPMS solution added with 0.5% H_2O_2 concentration, the etch rate of the film is more and more faster, while it is not etched at all in dHF only solution. If this result is applied to the result of Cu particle removal on silicon surface, we suppose that cleaning solution should contain oxidants such as H_2O_2 and ozone to remove Cu particles. This is due to metallic copper dissolution reaction followed by oxidants dissolution reaction. The rate of oxidants dissolution reaction is decided on the amount of electron generated by Cu dissolution. On decreasing HF concentration in solution, Cu oxide or Cu hydroxide formation reaction instead of copper dissolution reaction is dominant. In the case of solution with a high pH value, Cu impurity removal efficiency is degraded. The etching rate reduction of Cu film with adding surfactant in FPM solution seems to be not so high. From these research, the dependence of copper impurity removal efficiency on substrate

etching rate for various substrates in hydrofluoric solutions is following. First, fig. 8 explains a key reaction on copper contaminated c-Si surface as a function of HF concentrations in various HF solutions. At the HF concentration below 50 ppm in FPM or FPMS solutions, main reaction is the Cu oxide or Cu hydroxide formation. Therefore, copper impurity can not be perfectly removed below detection limit even after 10 min dip. However, at high HF concentration, the reaction of copper dissolution is dominant because solution has a low pH value. The Cu removal reaction is proportional to dissolution rate of H_2O_2 in electron- and hydrogen-rich solution. Second, fig. 9 represents a key reaction on copper contaminated a-Si surface. At low HF concentration, metallic copper forms the Cu oxide or Cu hydroxide which is the same result as c-Si surface. However, at high HF concentration in FPM solution, copper impurity is not removed from the surface. It is different for the result of c-Si surface, because the FPM solution has a relationship of rapid etching rate on a-Si film compared to that of c-Si surface. We suppose that the amount of electron tunneling from substrate suppresses the dissolution reaction of Cu particles on surface. In FPMS solution, however, the surfactant added to the solution affects the amount of electron tunneling from substrate. In a high HF concentration, copper impurity on surface is removed to around level of 10^{10} atoms/cm^2. Both reactions (which are electron tunneling from surface and copper impurity dissolution reaction) should be controlled very precisely. Figure 10 shows the dependence of FPMS and of a surfactant-added dilute HF (DHFS) cleaning efficiencies on the amount of surfactant in solution. In order to remove to around the level of 10^{10} atoms/cm^2 of copper impurities from substrate, it is required to have more than 50 ppm in FPMS solution. On the other hand, impurities in DHFS solution are rarely removed from the surface irrespective of surfactant concentration.

We suppose that HF mixing chemical for removing Cu impurity from surface should have the function to prevent lifted copper particles from re-adsorption on substrates. Additionally, it should contain oxidants to remove copper impurities from the surface because they consume the electrons generated by Cu dissolution reaction.

CONCLUSION

The cleaning efficiency of Cu impurity on a-Si is quite different from that on c-Si. On a-Si, FPM cleaning can not remove Cu impurity though it is effective to remove Cu impurity on c-Si surface. FPMS cleaning with a high HF concentration, however, has a good efficiency on both c-Si and a-Si surfaces. The FPMS cleaning efficiency on a-Si can be explained by the fact that Cu dissolution reaction rate in solution is high, while the amount of electron tunneling from substrate is decreased. The experimental results in HF solutions are interpreted by 3 kinds of main reactions and not by the only characteristics of chemical solution such as pH and ORP values.

ACKNOWLEDGMENTS

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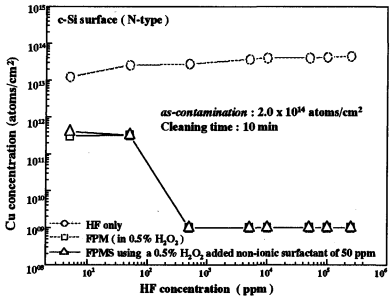

Fig.1 Residual Cu impurity on c-Si surface in HF solutions

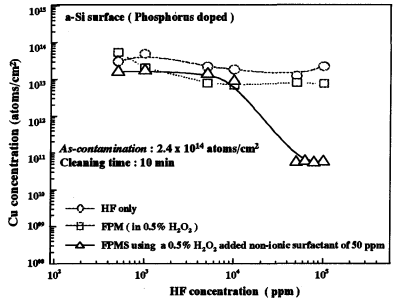

Fig.2 Residual Cu impurity on a-Si surface in HF solutions

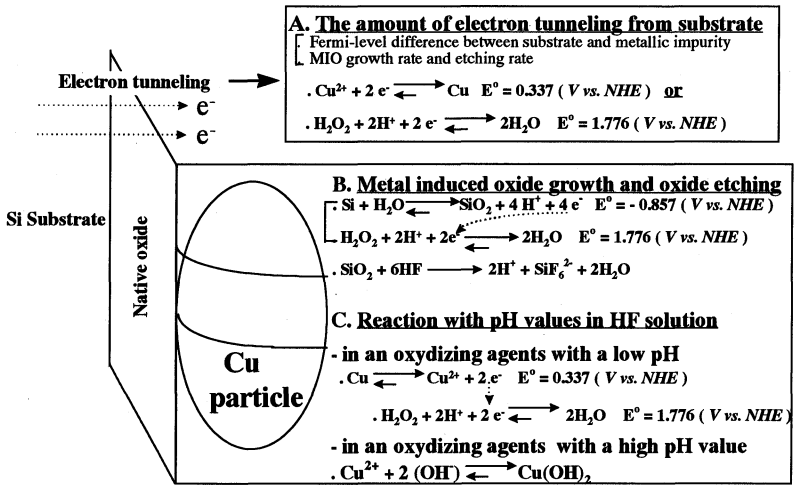

Fig.3 A model of Cu impurity removal effeciency from silicon substrate in various HF solutions

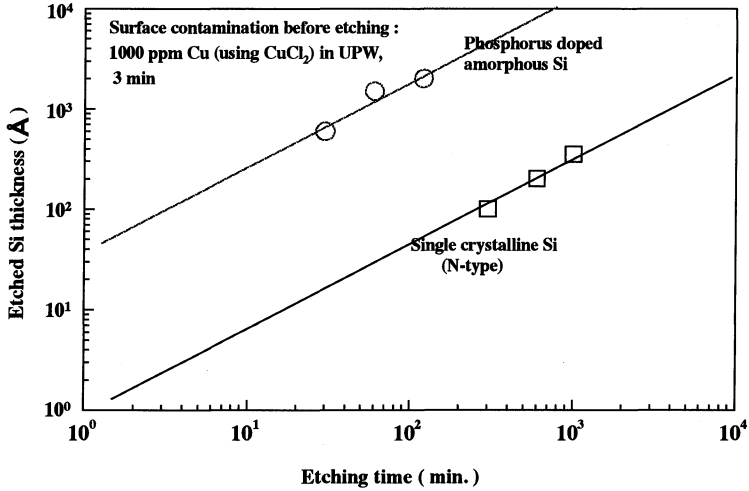

Fig.4 Etching rate of Cu contaminated Si substrates in a 0.5% HF solution

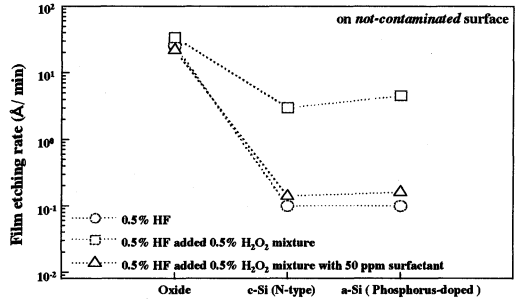

Fig.5 Etching rate of various substrates in HF solutions

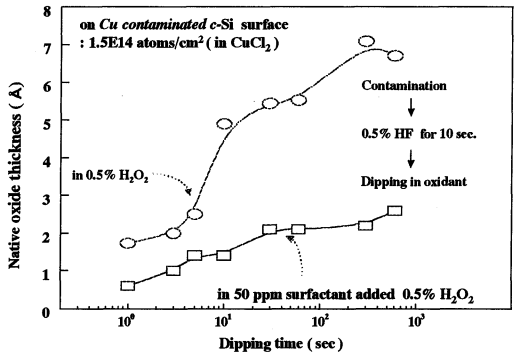

Fig.6 Dependence of native oxide growth on adding the surfactant in a 0.5% H_2O_2 solutions

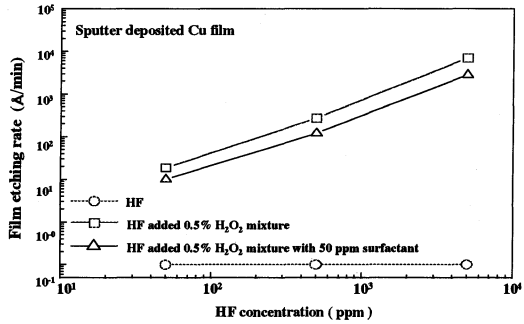

Fig.7 Etching rate of sputter deposited Cu film with various HF solutions

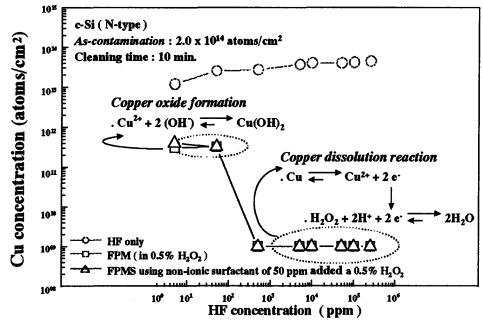

Fig.8 A key reaction on Cu contaminated c-Si surface as a function of HF concentration in various HF

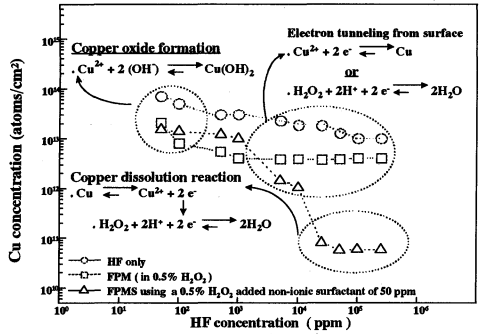

Fig.9 A key reaction on Cu contaminated a-Si surface as a function of HF concentration in various HF

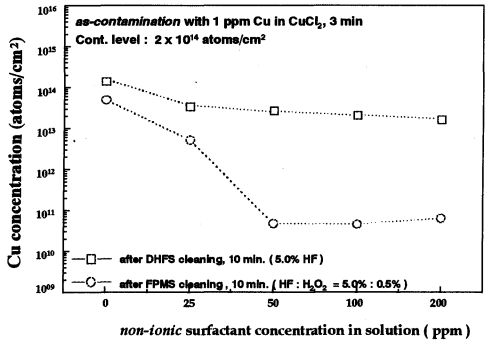

Fig.10 Dependence of Cu removal efficiency on the surfactant in solution

THE EFFECT OF pH ON THE UNIFORMITY OF ETHYLENE GLYCOL-HF ETCHES OF Si_3N_4

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ABSTRACT

$HF:H_2O$ solutions at ambient temperatures typically etch SiO_2 twenty times faster than Si_3N_4, severely limiting their use as Si_3N_4 etchants on device wafers. Dilute, high-temperature solutions of HF in ethylene glycol (EG) have far different etch properties. A 2:2:96 blend of $HF:H_2O$:EG at 80° C etches SiO_2 and Si_3N_4 at nearly equivalent rates. Unfortunately, the on-wafer etch uniformity of Si_3N_4 films is far worse than that of SiO_2 films etched under the same process conditions. It is theorized that either high fluoride consumption or the production of a "poison" in the Si_3N_4 etch process is responsible for this non-uniformity. This paper investigates the effects of bulk fluid transport near the wafer surface, and the use of HCl to counter high-pH etch poisons that affect the etch uniformity of Si_3N_4 films.

INTRODUCTION

Silicon nitride (Si_3N_4) is a commonly used thin film in the production of semiconductor devices. Wet etches of Si_3N_4 have traditionally been done with hot phosphoric acid (H_3PO_4, >130° C) or hot, concentrated HF (>5 wt% HF, >50° C). HF typically shows selectivity toward silicon dioxide (SiO_2) films present on the wafer, etching the oxide substantially faster than the nitride. This selectivity toward oxides allows the use of HF in wafer reclaim applications, but limits its use on device wafers. Hot phosphoric acid has good nitride:oxide selectivity. However, H_3PO_4 etching is dirty because its high viscosity and high use temperature make it difficult to filter. Despite these problems, hot phosphoric acid is currently the process of record for most nitride strips on device wafers.

While concentrated HF solutions etch oxides more quickly than nitrides, dilute, high temperature HF solutions etch nitrides and oxides at nearly the same rate. Solutions of 4 vol% of 49% HF in water near 90° C etch Si_3N_4 and thermally grown SiO_2 at comparable rates. The difficulty of working with aqueous solutions near their boiling points led workers to shift to the use of HF in high-boiling-point solvents with electrical properties similar to those of water. Ethylene glycol is commonly used as a solvent due to its high boiling point of 197° C, high flash point of 111° C, low cost and relative safety.

The shallow trench isolation process (STI) used in advanced devices requires the use of a wet etch with near 1:1 nitride:oxide selectivity (Figure 1). 96:4 blends of EG:HF near 80° C provide etch rates near 4 nm/min and >1.3:1 selectivity. Etches of thermal oxide films with EG:HF in a centrifugal spray processor in this work are stable, with on-

and 25 contained Si_3N_4 test wafers and slot 15 contained an SiO_2 test wafer. All other slots in the two cassettes contained filler wafers. Pre- and post-thickness measurements at 49 sites per wafer and a 3-mm edge exclusion were performed on a Rudolph Caliber 300 ellipsometer. Difference maps and statistics were derived by subtracting these maps on the ellipsometer. Non-uniformity statistics are calculated from the standard deviation (σ) of all points across the wafers:

$$\text{non-uniformity} = 100\% \times \sigma / \text{average etch} \qquad [2]$$

Hot DI water was used to preheat the wafers. A brief spin dry in nitrogen was used to remove the water from the wafers and chamber. It is necessary to remove this water because water contamination in the EG:HF etchant increases the etch rates and varies the nitride-to-oxide selectivity. Un-annealed Si_3N_4 and thermal SiO_2 were etched for 4 to 6 minutes with the center / side flow distributions listed in Table 1.

	On-wafer non-uniformity	
	Si_3N_4	SiO_2
Center dispense only	3.25%	1.39%
Side dispense only	1.90%	1.28%
Balanced center / side dispense	1.44%	1.50%
Balanced center / side dispense with HCl addition	0.48%	0.65%

Table 1: Process conditions and results

RESULTS AND DISCUSSION

Figure 2 shows the etch uniformity maps for nitride with the dispense of the EG:HF etchant from only the center spray post. In all figures, the center spray post is located near the arrow at the bottom of the wafer map and the centrifugal force from the rotation is nearly straight up on the image. Figure 2 shows a consistent decrease in the nitride etch rate with increased distance from the source of the etchant (the center spray post) with an overall etch non-uniformity of 3.25%. This behavior of faster etching near the source of fresh etchant is consistent with either the depletion or poison hypothesis - i.e., areas with fresh etchant would have less depletion of the HF and would etch faster. Likewise, areas with fresh etchant would have less poison in the etchant and would etch faster.

Figure 3 shows the etch uniformity of an oxide film under the same process conditions. The overall non-uniformity of the oxide etch is 1.39%, substantially better that that of the nitride. There is little evidence of any systematic decrease in etch rate with radius. The outer edge of the wafer, the area farthest from the spray post, had a significantly increased etch rate. This may be due to a small amount of residual water left from the hot DI pre-heat. Table 2 shows the effect of increased water content on the etch rates of nitride and oxide. While the etch rate of both films increases with water content, the oxide rate increases more quickly as evidenced by the reduction in

wafer etch uniformities similar to those obtained on SiO_2 with aqueous-based HF chemistries. Etches of Si_3N_4 films, however, showed much larger on-wafer non-uniformities than did oxide wafers under the same process conditions.

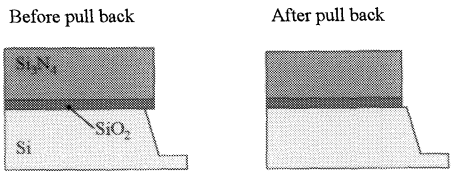

Figure 1: Shallow trench isolation pull-back etch

Two causes for this behavior have been proposed. First, it is possible that in equivalent etching of nitride and oxide on a volume basis (equal nanometers of film removed), the nitride etch requires a much larger quantity of fluoride. This larger fluoride demand could lead to a mass-transport-limited etch rate. Areas of the wafer with relatively high bulk transport, with large flows of fresh etchant, would etch more quickly than areas with low flows or a depleted etchant.

Second, it is possible that a reaction byproduct of the nitride etch acts to "poison" the etch. For instance, Si_3N_4 etching in HF may proceed as follows:

$$Si_3N_4 + 12HF + 4H_2O \rightarrow 3SiF_4 + 4NH_4OH \qquad [1]$$

If so, the weak base NH_4OH could act to poison the etch by the weak acid HF. High bulk transport would act to rinse away the poison, resulting in areas of faster etching. It may also be possible to counteract the chemistry of the etch poison. This experiment investigates the effect of the uniformity of bulk transport of the etchant on the on-wafer etch uniformity of SiO_2 and Si_3N_4 films, along with the use of HCl to counter any high-pH etch poisons.

EXPERIMENT

The experiment was performed in a MERCURY® MP Surface Conditioning System, a centrifugal spray processor. In the Mercury MP processor, four cassettes of 200-mm wafers are mounted on a rotating turntable. Process chemistries and rinse water are atomized with nitrogen and dispensed from either a center spray post mounted near the turntable's axis of rotation (spraying radially outward) or a spray post mounted on the side of the process chamber (spraying radially inward), or both. A recirculation system filled with EG:49% HF pre-blended to a 96:4 volume ratio provided a 6-liter/min dispense of etchant on the wafers. The etchant temperature was controlled at 80° C ± 0.5° C by a hot-water heat exchanger in the recirculation tank and an in-line infra-red heater.

Runs were performed with 25-wafer Fluoroware A192-81m low-profile cassettes with most of the webbing removed to enhance fluid flow. In one cassette, slots 1, 13, 24

selectivity. A local 0.5 vol% level of water contamination in the etchant would account for the increase in the etch rate at the outside of the wafer.

Blend - wt% EG:HF:H_2O	Appx. vol% H_20	Si_3N_4 Etched	SiO_2 Etched	Selectivity
96:4:0	2%	264.5	195.3	1.35
96:4:2	4%	307.7	263.3	1.16
96:4:6	8%	352.0	367.2	.95

Table 2: Variation in EG:HF etch rates with water contamination levels

Figure 4 shows the etch profile of a nitride wafer with EG:HF dispensed only from the side-bowl spray post mounted on the wall of the process chamber. The profile has an overall non-uniformity of 1.9% with clearly visible areas of excess etching near the bottom and open sides of the cassette. Note that the webbing of the cassette had been removed to allow the atomized spray of etchant to reach the wafer through the side of the cassette. The etch non-uniformity of an oxide film under these conditions was 1.28% with no obvious pattern. This data is also consistent with either the depletion or poison hypothesis.

Figure 5 shows the etch uniformity of a nitride film with a balanced dispense from both the side and center. The etch non-uniformity was improved to 1.44% with some excess etching near the spray post. The uniformity can probably be improved slightly by increasing the fraction of etchant dispensed from the outside of the wafer. Again, this data is consistent with either the depletion or poison hypothesis.

Figure 6 through Figure 8 shows the on-wafer non-uniformity, mean removal and nitride-to-oxide selectivity respectively of a 10-run passive data collection (PDC) using the balanced dispense of Figure 5. The process is quite stable with some variation in mean removal due to small variations in the average temperature during the etch. Adaptive process control is necessary to eliminate the effects of these variations.

Figure 9 shows the etch uniformity of a nitride film achieved with the balanced-dispense process used in the PDC above, but with the addition of 4 vol% HCl in the EG:HF blend (Table 1). The on-wafer non-uniformity improved three fold from approximately 1.5% to less than 0.5% 1σ with the addition of HCl. The SiO_2 etch non-uniformity (not shown) improved two fold, from approximately 1.34% to 0.65% 1σ. Clearly, both the flow dynamics of the etchant and the chemistry of the etchant play a strong role in determining the on-wafer uniformity performance when etching Si_3N_4 or SiO_2 with EG:HF:HCl chemistries.

SUMMARY

The dispense pattern of the etchant has been shown to be a critical factor in determining the etch uniformity of Si_3N_4 films in multi-position spray processors. A balanced dispense of etchant from spray posts, both near the center of rotation and

mounted on the side of the chamber, result in more than a two fold improvement in the on-wafer uniformity. The distribution of etchant did not have a strong effect on the etch uniformity of SiO_2 films. The addition of HCl led to a three fold improvement in Si_3N_4 etch uniformity and a twp fold improvement in SiO2 etch uniformity. The combination of an optimized dispense pattern and the addition of HCl allowed etching of Si_3N_4 with less than 0.5% 1σ non-uniformity.

ACKNOWLEDGMENTS

We thank Glen Steffen, Greg Nelson, John Willyard, Leo Lake, Mark Dahlberg and Nat Narayanswami, all of FSI International, each of whom made a critical contribution to the project.

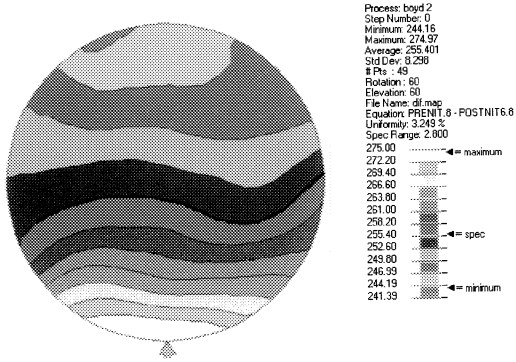

Figure 2: Si_3N_4 all center dispense, 3.25% non-uniformity.

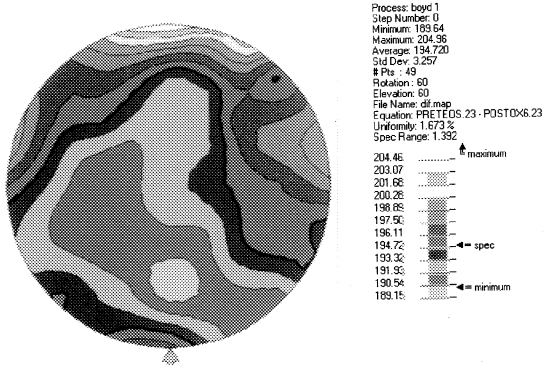

Figure 3: SiO_2 all center dispense, 1.39% non-uniformity.

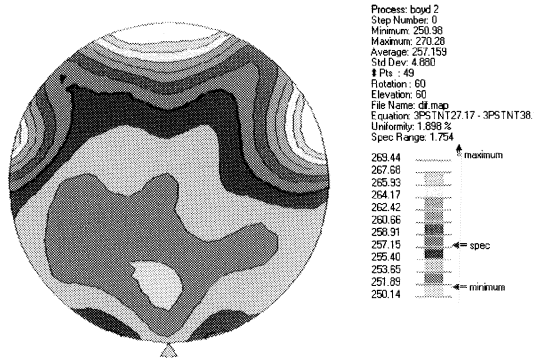

Figure 4: Si_3N_4 all side dispense, 1.90% non-uniformity.

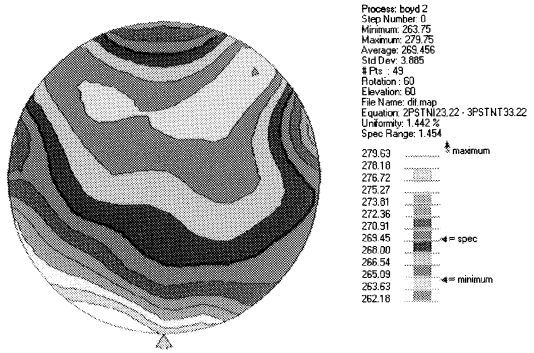

Figure 5: Si_3N_4 balanced dispense, 1.44% non-uniformity.

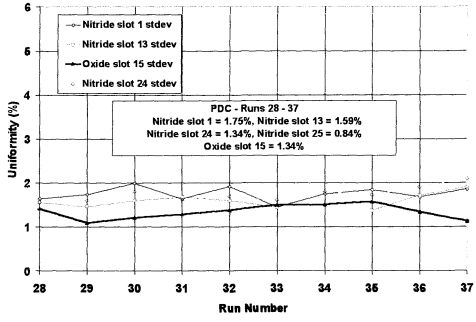

Figure 6: On-wafer non-uniformity, PDC runs

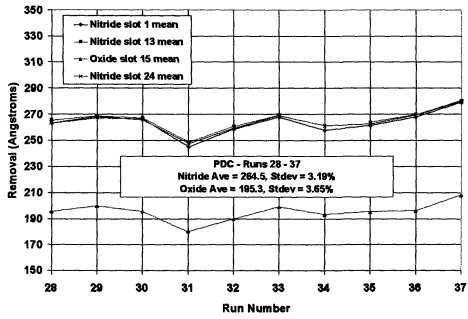

Figure 7: Mean removal, PDC runs

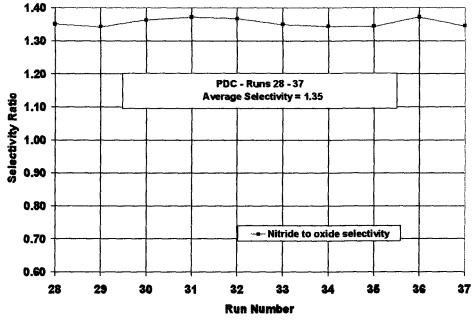

Figure 8: Nitride to oxide selectivity ratio, PDC runs

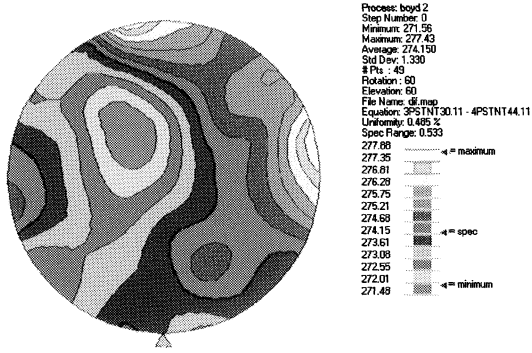

Figure 9: Si_3N_4 with EG:HF:HCl process, 0.48% non-uniformity.

OZONE CLEANING

The Reaction of Ozone and H_2O_2 in Ammonium Hydroxide (NH_4OH) Solutions and Their Reaction with Silicon Wafers

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The main purpose of this study was to evaluate the ozone chemistry in NH_4OH solutions in terms of oxidizing power when compared with H_2O_2 based NH_4OH solution. Above pH values of 9, the solubility of ozone in solutions was almost nil at room temperature. However, ozone was dissolved in NH_4OH solutions when the temperature of solutions was lowered to 10°C. Even though ozone was decomposed rapidly in NH_4OH solutions within a few minutes, the hydrophobic silicon became hydrophilic in O_3/NH_4OH solutions within 10 min. Chemical oxide grown in O_3/NH_4OH solutions at 10°C was thicker than one in SC1. The imaginary part of the pseudodielectric function at the energy of the E_2 critical point peak, ε_2, was determined by a variable angle spectroscopic ellipsometry (VASE) to evaluate the properties of the chemical oxides.

INTRODUCTION

The SC1 step in RCA cleaning process has been widely used for the removal of organic contaminants and particles on the silicon surface [1]. In SC1 solution, ammonium hydroxide etches silicon surfaces and hydrogen peroxide passivates the wafer surface and decomposes the organic contaminants on the wafer surface [2]. These two processes are known to be key mechanisms for the particle removal. The hydrogen peroxide in the SC1 solution prevents the ammonium hydroxide from etching the underlying silicon substrate. If sufficient hydrogen peroxide is not present in the solution, the silicon surface will be anisotropically etched and the surface roughness will be introduced [3]. To avoid the microroughness of surfaces, SC1 solution was suggested to have a low concentration of ammonium hydroxide and the lower temperature process [4]. The addition of megasonic energy during these processes has been proven to enhance particle removal [5].

The presence of H_2O_2 in SC1 solution might introduce issues such as the reduction of lifetime of cleaning chemicals, the metallic contamination on wafer surfaces and the increase of the waste treatment cost [6]. Because many disadvantages in the SC1 processing come from hydrogen peroxide, another approach has been proposed to use other oxidant, such as ozone, which is available without a huge consumption of chemicals and a bad influence on environment. However, attempts to replace hydrogen peroxide with ozone in SC1 have been unsuccessful because ozone is very unstable in the ammonium hydroxide [7].

Ozone chemistry has been widely used to strip the photoresist in wet cleanings. It was well known that ozone injected DI water and acidic solutions could remove the organic and metallic contaminants on the surface [8-9]. The application of ozone to wet

cleaning has advantages in maintaining chemical purity, recycling and lowering the cost of ownership in the light of the environmental issues in the next generation wet cleaning processing [10].

In this study, we investigated the reactivity of ozone in NH_4OH solutions and compared their behaviors to the reaction of H_2O_2 in NH_4OH. The solubility and lifetime of ozone were measured as a function of time and temperature. The chemical oxides grown in NH_4OH solutions were evaluated by spectroscopic ellipsometer(SE) to obtain information on their thickness and properties.

EXPERIMENTAL

Ozone generated in an arc discharge type generator (Fischer 502) was supplied to a cleaning bath as shown in Figure 1. Teflon tubing was used for all experiments to minimize the possible reaction with ozone. Ozone was supplied to the bath directly or to the circulation line. A chiller was used to control the temperature of solutions and 0.2μm filter was installed to remove the particles during the circulation of solutions. The concentration of ozone in NH_4OH solution was measured by an electrolytic analyzer (Obisphere 3600). Ultra high purity DI water (18.2 MΩ·cm, Millipore Milli-Q plus system) and semiconductor grade wet cleaning chemicals were used for the experiment.

pH and redox potential of DI water were measured by Orion Ag/AgCl electrode and Pt redox electrode with an Orion pH meter (Orion 520A). The solubility of ozone, pH and Eh were measured in various concentrations of NH_4OH solutions as a function of the ozone injection time and the temperature. For the experiments, silicon wafers (4″ p type, (100)) were precleaned in 4:1 piranha solution and followed by 0.5 % HF etching. The wettability of surfaces was measured by a static contact angle analyzer (Krüss G10) as a function of the treatment time in SC1 and ozone-injected NH_4OH solutions. Ellipsometric measurements were performed with a computer-controlled variable angle spectroscopic ellipsometer of the rotating analyzer type (J. A. Woollam Co.). In the spectroscopic scans, ellipsometric data were taken at an angle of incidence (70°) in the photo energy range of 1.5-5.5 eV at 0.01eV intervals. Chemical oxides were characterized by SE as a function of treatment time. Also a titration method using $KMnO_4$ was used for the measurement of H_2O_2 concentration in SC1.

RESULTS AND DISCUSSION

Figure 2 shows the changes of ozone concentration in NH_4OH solutions as functions of ozone-injection time and temperature of solutions. Because ozone decomposed rapidly in NH_4OH solution, the solubility of ozone in NH_4OH solutions was almost nil at room temperature. In NH_4OH solutions, possible reactions could be proposed as shown below [11].

$$NH_4^+ + 4O_3 = NO_3^- + 4O_2 + H_2O + 2H^+ \quad (1)$$

$$O_3 + OH^- = HO_2^- + O_2 \quad (2)$$

Even though much more complex reactions occur together in solutions, reaction (1) and (2) are dominant in NH_4OH solution and accelerates the decomposition of ozone. In

higher pH values than 9.5 in NH_4OH solutions, the solubility of ozone was increased in NH_4OH solutions when the temperature of solution was lowered to 10°C as shown in Figure 2(b). Although the solubility of ozone was increased at lower temperatures, pH values were higher than those at room temperature. It might be attributed to a slower decomposition of ozone at lower temperatures.

At a concentration of NH_4OH in O_3/NH_4OH solutions, pH and Eh were higher at lower temperatures as shown in Figure 3(a). It was very interesting to note that Eh at 10°C was much higher than at room temperature. Figure 3(b) shows the decomposition rate of ozone in different NH_4OH solutions as a function of time when NH_4OH was added in ozonated DI water. The initial ozone concentration in DI water was 12 ppm. The half life time of solutions was less than 1 min at room temperature for all NH_4OH concentrations investigated.

Hydrogen peroxide readily dissociates and forms water and oxygen in SC1 solution. The decomposition rate of H_2O_2 in SC1 was measured by a titration method as a function of temperature as shown in Figure 4. Half-life time of H_2O_2 at 50°C was 5 times longer than at 80°C. As the temperature of solution was increased, the decomposition rate of H_2O_2 as well as ozone was increased.

Hydrogen peroxide and ozone in solutions play a key role as oxidizing agents in cleaning solutions. When the silicon wafers were treated in these solutions, the hydrophobic silicon surface tends to change the hydrophobic silicon surface into hydrophilic. Figure 5 shows the change of contact angles in SC1 solutions as a function of the treatment time at 80°C. The silicon surface in SC1 solution was changed from hydrophobic (72°) to completely hydrophilic surface (< 5°) within 10 sec. Slightly higher contact angles on silicon were measured when wafers were treated in ozone injected NH_4OH solutions at room temperature as shown in Figure 6. Lower NH_4OH concentrations than 0.01 resulted in completely hydrophilic surface within 10 min. At 10°C, the change of contact angles on silicon surface in O_3/NH_4OH solution was similar to that in SC1 solution as shown in Figure 7. Thus, it was evident that the treatment in O_3/NH_4OH solution was able to change the silicon surface from hydrophobic to hydrophilic. The oxidation rate of silicon in O_3/NH_4OH solutions was dependent on the temperature of solution and an amount of NH_4OH in solution due to the magnitude of soluble ozone in it.

The etch rate of silicon in SC1 and NH_4OH solutions with and without injection of ozone was measured by the dissolution method as a function of temperature. NH_4OH solutions showed the severe etching of silicon surfaces at a rate of 25 Å/min even at 10°C as shown in Figure 8. The etch rate of silicon in SC1 was less that 1 Å /min at 70□. However, the etch rate of silicon in O_3/NH_4OH was too low to measure even at room temperature. Preliminary AFM study showed a much smoother surface on silicon treated in ozone injected NH_4OH solutions than in SC1.

The characterization of chemical oxides grown in SC1 and O_3/NH_4OH was performed by a spectroscopic ellipsometry (SE). The pseudodielectric function, $\langle\varepsilon(E)\rangle = \langle\varepsilon_1(E_1)\rangle + i\langle\varepsilon_2(E_2)\rangle$ can be obtained from measured spectral data. The imaginary part of the pseudodielectric function at the energy of the E_2 critical-point peak, $\langle\varepsilon_2(E_2)\rangle$, is

known to provide a sensitive and unambiguous indication of the sharpness of the dielectric discontinuity between the substrate and ambient, i.e., its value reflects not only the residual oxides and other overlayers but also the slevedge region, bulk degradation and microstructural effects. The SE measurements therefore yield direct information regarding the relative quality of surface regions prepared by different methods [12,13].

Figure 9 shows a plot of the $<\varepsilon_2 (E_2)>$ value as a function of the treatment time in SC1 at 80°C and O_3/NH_4OH solutions. The HF-pretreated sample resulted in a value of about 42. This value was considerably lower than that for the nearly ideal sample ($<\varepsilon_2 (E_2)>$ ~48) [14] due to the surface microroughness and H-adsorption on surface by HF etching [13,15-17] and the native oxide layer grown during SE measurement. The immersion of HF treated silicon in chemicals resulted in the rapid drop of $<\varepsilon_2 (E_2)>$ values. This decrease might indicate the growth of passivation oxide layer between silicon and ambient. The smallest decrease of $<\varepsilon_2 (E_2)>$ was observed in SC1 treated samples and the largest decrease was in ozone injected NH_4OH solutions at 10°C. Figure 10 shows the $<\varepsilon_2 (E_2)>$ spectra of silicon treated in cleaning solutions for 10 min as a function of photon energy.

The simulation of SE spectra on chemical oxides was performed to calculate the oxide thicknesses and resulted in 16 Å and 14 Å in SC1 at 80°C and O_3/NH_4OH at room temperature, respectively as shown in Figure 11. However as discussed in $<\varepsilon_2 (E_2)>$ values, much thicker oxide of 24 Å was measured on the chemical oxide grown in O_3/NH_4OH solutions at 10°C.

SUMMARY AND CONCLUSIONS

The decomposition of ozone in NH_4OH solutions was accelerated due to the reaction of ozone with OH^-, thereby the solubility of ozone in NH_4OH solution was very low at room temperature. The decrease of the solution temperature to 10°C significantly increased the solubility of ozone, pH and Eh values. Also the solubility of ozone in NH_4OH was strongly dependent on the concentration of NH_4OH. It was possible to passivate the silicon surface to hydrophilic surface in a NH_4OH solution at room temperature even though the solubility of ozone was less than 1ppm in it. The etch rate of silicon in O_3/NH_4OH solution was very small and did not introduce any surface roughness. SE analysis showed that comparable oxide thicknesses (14~16 Å) were measured on silicon surfaces when treated in both SC1 at 80°C and O_3/NH_4OH at room temperature. However much thicker oxide (24 Å) was grown in O_3NH_4OH solutions at 10°C.

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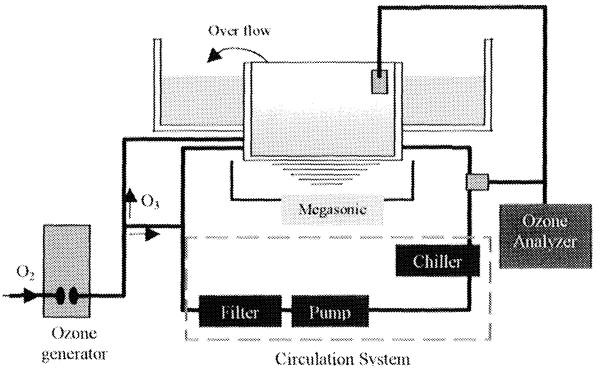

Figure 1. A schematic diagram of cleaning bath used for the experiment

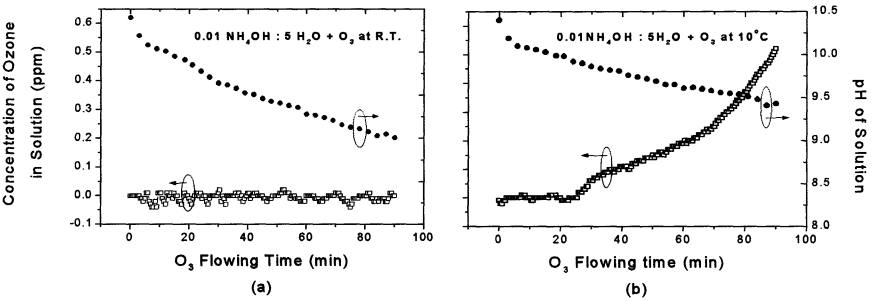

Figure 2. The change of solubility of ozone and pH as a function of ozone flowing time at (a) room temperature and (b) 10°C in NH_4OH solution

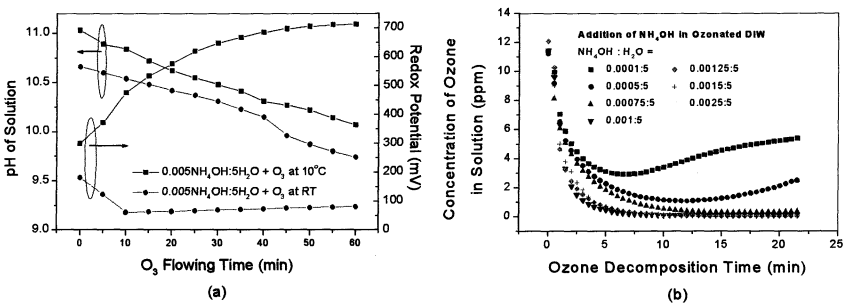

Figure 3. (a) The change of pH and Eh in ozone injected NH_4OH solutions as a function of ozone flowing time and (b) the concentration of ozone as a function of time at room temperature when NH_4OH is added in ozonated DI water

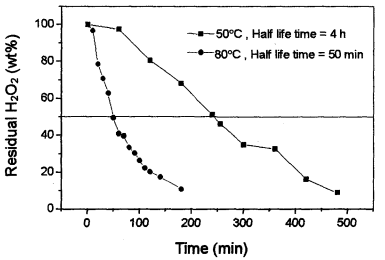

Figure 4. The normalized half life time of H_2O_2 in SC1 solutions as a function of time at 50°C and 80°C

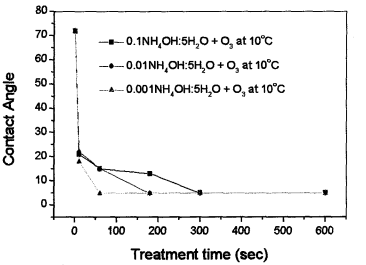

Figure 7. The change of contact angles as a function of the treatment time in O_3/ NH_4OH solutions at 10°C

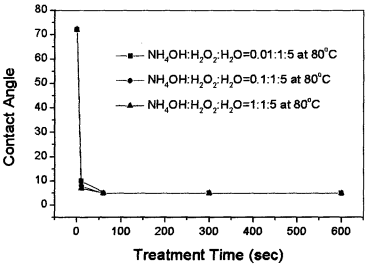

Figure 5. The change of contact angles as a function of the treatment time in various concentrations of SC1 solutions

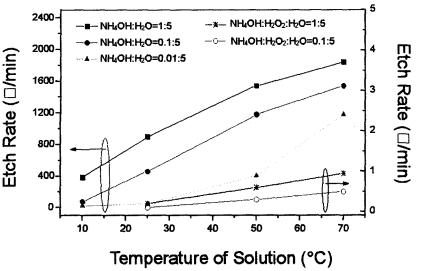

Figure 8. The etch rate of silicon in various concentrations of NH_4OH and SC1 solutions as a function of temperature

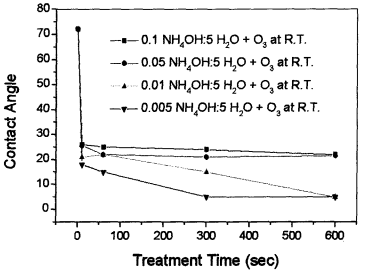

Figure 6. The change of contact angles as a function of the treatment time in O_3/NH_4OH solutions at room temperature

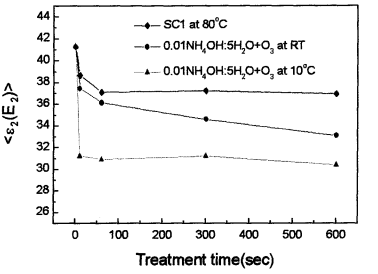

Figure 9. The $<\varepsilon_2(E)>$ values as a function of the treatment time in SC1 and O_3/NH_4OH solutions

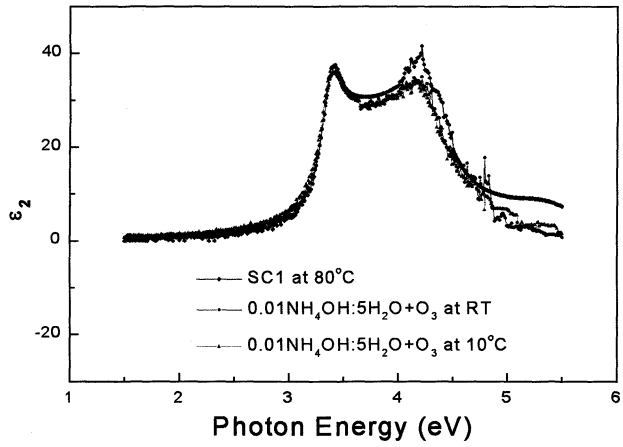

Figure 10. The $<\varepsilon_2(E)>$ spectra of silicon treated in SC1 and O_3/NH_4OH solutions for 10 min

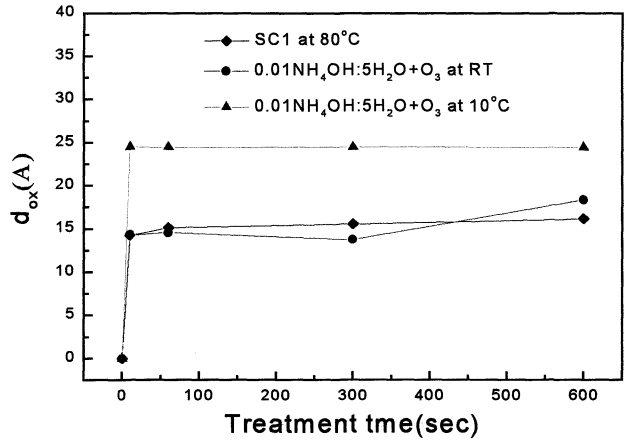

Figure 11. The calculated oxide thickness on silicon treated in SC1 and O_3/NH_4OH solutions as a function of treatment time

THE USE OF OZONATED HF SOLUTIONS FOR POLYSILICON STRIPPING

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ABSTRACT

Ozone-based HF chemistry is proposed to substitute the conventional HF/HNO_3 mixture for polysilicon stripping in wafer reclamation. The etching characteristics of ozonated HF solutions are investigated. Similar to its HF/HNO_3 counterpart, HF/O_3 was found to strip polysilicon films through a simultaneous oxidation-and-etching process. The strip rate was determined by the rate-limiting step in the competition between the oxidation and etching reactions; whichever slower would govern the overall kinetics. Because of the nonstop etching nature of the chemistry on both silicon and silicon oxides, the feasibility of the process application is evaluated, based on the etch selectivity between the polysilicon and the underlying thermal oxide.

INTRODUCTION

Mixtures of nitric acid (HNO_3) and hydrofluoric acid (HF) have been commonly used in the semiconductor industry to strip polysilicon films from process monitor wafers for wafer reclamation. In reclaiming factory, this chemistry is typically applied in concentrated forms, and thus the wafers are severely roughened and need to be polished afterwards. To reduce the turn-around time and costs, some IC manufacturers conduct in-house wafer reclaiming in which the polishing step is skipped. Due to the nonstop etching nature of HF/HNO_3 chemistry on silicon, the mixture in such application has to be diluted and the chemical ratio needs to be properly controlled to prevent the wafers from being damaged [1,2]. However, the exothermic reaction from HNO_3 mixing with water as well as the use of the dual acid chemistry increase the difficulty of maintaining the temperature and chemical ratio of the processing bath. In addition, a great deal of DI water is required after the process to rinse off the strong, viscous nitric acid. Also, the use of the hazardous HNO_3 always raises the concerns and costs in storage/handling, waste disposal, and personnel safety.

As has been well known as a strong oxidant [3], ozone may be an ideal alternative to substitute nitric acid for in-house poly stripping. Ozone can be constantly generated at a point-of-use basis and mixed with HF solutions in stable concentrations without causing temperature variation. Also, the single acid (HF) system can render electrodeless conductivity sensors applicable for fast, accurate, cost-effective monitoring and control of the concentration of HF acid during the stripping, accordingly extending the bath life [4]. Compared to HNO_3, additionally, ozone decades to oxygen quickly in atmosphere, significantly reducing the environmental concern. In this study, the etching characteristics and process effectiveness of ozonated HF solutions were evaluated to explore the feasibility of the proposed chemistry.

EXPERIMENTAL

The experiment was conducted on an AKrion's GAMA wet station in the Class 1 Applications Laboratory at AKrion LLC. Ozone was generated from oxygen gas using a commercial ozone generator and was introduced into hydrofluoric acid (HF) solutions through a liquid/gas mixer. The bath was recirculated at a fixed flow rate at 20°C during the stripping process. The concentrations of HF and dissolved ozone were varied from test to test for the characterization of poly etching.

150-mm silicon wafers coated with approximately 1000 Å (or 2000 Å) polysilicon films on 400 Å SiO_2 layers were used in this study. Recognizing the difficulty of producing uniform etching across a large surface area at high rates, smaller samples were used for the etch rate characterization test. A number of poly wafers were cut to ~ 25 mm × 50 mm coupons, and the sample was gripped by a piece of ¼" PFA tubing with a slotted end for immersion in the bath. On the other hand, full sheets of poly wafers were also tested to verify the actual stripping characteristics. Oxide etch rates were also characterized at different bath concentrations using thermal oxide wafers (> 1000 Å). The thickness of polysilicon films (or thermal oxide films) was measured with a Rudolph AutoEL II ellipsometer before and after each run of tests. Etch rates were then estimated based on the process time applied and the change of film thickness.

RESULTS AND DISCUSSION

Similar to how HF/HNO_3 chemistry has worked, ozonated HF solutions are anticipated to etch silicon based on the concept of a simultaneous process of oxidizing the Si with ozone and etching the SiO_2 with HF. According to the hypothesis, HF alone cannot strip the poly film but the oxide. Figure 1 shows a consistent result that the etch rate of polysilicon in HF was negligible regardless of the chemical concentration, while the thermal oxide etch rate was proportionally increased with the increase of HF concentration. Also note that whether the O_3 appears in the HF solutions did not influence the oxide etch rate; a linear regression analysis of the oxide etch data in Fig. 1 (with or without O_3) indicated a confidence level of 97.6%, suggesting that ozone was not involved in the oxide etching reaction.

By ozonating the HF solution, ploy etching seemed to become noticeable. Figure 2 shows that, at a HF concentration of 0.25%, 15 ppm of dissolved O_3 resulted in a poly etch rate of about 57 Å/min. Further increasing the ozone concentration in the HF, however, did not enhance the poly stripping in this situation (Fig. 2). The observations indicate that there must have existed a threshold value of ozone concentration for poly etching in the 0.25% HF solution. Beyond that value, the etching kinetics would be limited by the specific HF concentration.

On the other hand, with an O3 level of 55 ppm, the etching kinetics of poly films was dependent on the HF concentration ranging from 0.05 to 0.5%, as shown in Figure 3. The large data scattering, essentially resulting from non-uniform etching at high rates, started to appear at 0.5% HF and increased the difficulty and inaccuracy of film thickness measurement by the ellipsometer. Therefore, no small-coupon experiments were performed beyond 0.5% HF. Instead, full poly wafers were used to provide a qualitative

approach for the etching characteristics. Figure 4 shows the total amount of time required to strip the 1000 Å poly layer from the 150-mm wafer as a function of HF concentration. These results were then converted to etch rates and illustrated in Figure 5, with the data of small-coupon experiments (Fig. 3) included as reference. Since the full wafer etching data reflected the minimum rate on the wafer in a non-uniform etching situation, they may also be viewed as the lower-bound etch rates for the particular conditions (i.e. wafer size, tank configuration, fluid dynamics, chemical concentrations, etc.). From Figure 5, it is clear that the full-wafer poly etching reached to a plateau as the HF concentration increased. This suggested that there was also a rate-limiting step governed by the dissolved O_3 concentration (i.e. 55 ppm in this case) as long as the HF concentration reached a threshold value, similar to the phenomenon shown in Fig. 2.

As previously mentioned, poly stripping in HF/O_3 solutions is a simultaneous process of poly oxidation and poly-oxide etching. The experimental results (Figs. 2 and 5) have shown that this is a competition process between the oxidation reaction and the etching reaction. Whichever is slower would be the rate-limiting step and determines the overall poly etching kinetics. In this context, a solution with "high" O_3 level relative to HF concentration would always maintain a finite oxide layer on the silicon surface, while the solution with "low" O_3 level relative to HF concentration would produce bare Si surface. This inference has been proved by examining the surface hydrophobicity of poly samples after dipping into various solutions (corresponding to the conditions in Figs 2 and 5). The experimental observations are outlined in Table 1.

Table 1: The surface state of a poly sample after dipping into various solutions

O_3 level in 0.25% HF	Surface State	HF conc. with 55ppm O_3	Surface State
0 ppm (low O_3 vs HF)	hydrophobic	0.05 % (high O_3 vs HF)	hydrophilic
15 ppm (high O_3 vs HF)	hydrophilic	0.1 % (high O_3 vs HF)	hydrophilic
25 ppm (high O_3 vs HF)	hydrophilic	0.25 % (high O_3 vs HF)	hydrophilic
38 ppm (high O_3 vs HF)	hydrophilic	0.38 % (high O_3 vs HF)	hydrophilic
55 ppm (high O_3 vs HF)	hydrophilic	0.5 % (high O_3 vs HF)	hydrophilic
--	--	1 % (high O_3 vs HF)	hydrophilic
--	--	2 % (low O_3 vs HF)	hydrophobic
--	--	3.33 % (low O_3 vs HF)	hydrophobic

From a technological viewpoint, one of the most important factors determining the feasibility of HF/O_3 application in poly stripping is the etching selectivity between the poly film and the oxide film by the chemistry. Since there is an oxide layer underneath the polysilicon film and since the poly stripping is most likely a non-uniform process, the slowest etching spot on the wafer surface has to be completed before the oxide at the quickest etching spot is fully removed, in order to avoid the onset of attack on the silicon substrate. According to the etch rate results obtained from the experiments (Table 2), the HF/O_3 chemistry apparently shows the greatest poly/oxide selectivity (~8) in the HF(0.5%)/O3(55 ppm) mixing condition (at 20°C). In the worst-case scenario (i.e. the etching of poly and underlying oxide starts concurrently), the attack of silicon substrate would not occur except the poly to be stripped is more than eight-time thicker than the thermal oxide. In the case of this study, the poly film (1000 or 2000 Å) is only 2.5 to 5 time thick compared to the underlying oxide (400 Å), the stripping should be completed in 6 to 12 minutes (based on the lower-bound etch rate of 167 Å/min in the

HF(0.5%)/O3(55 ppm) solution) and the remaining oxide can be stripped in another dedicated HF tank in which the etching will stop at the oxide/silicon interface. Increasing the HF concentration greater than 0.5%, although enhancing the stripping efficiency, does not favor the etching performance since the selectivity decreases (Table 2 and Figure 6).

Table 2: Etch rates and selectivity of polysilicon and thermal oxide in HF with 55 ppm O_3 at 20°C

HF (%)	Etch Rate (Å/min)			Poly/TOX Selectivity
	TOX	Small Poly	Poly Wafer	
0.05	--	3.8	--	--
0.1	2.2	12.5	--	5.7
0.25	8.5	60	34	7.1 (4)
0.38	15.4	119	--	7.7
0.5	20.6	325	167	15.8 (8.1)
0.7	34.6	--	--	--
1	43.4	--	200	(4.6)
2	*88*	--	235	(2.7)
3.33	*146.5*	--	250	(1.7)

1. The etch rates of TOX in *Italic* are the extrapolated values from Figure 1.
2. The selectivity values in parenthesis are based on the lower-bound poly strip rates.

CONCLUSION

The etching behavior of ozone-based HF chemistry on polysilicon has been characterized at various O_3 levels and HF concentrations. Test results showed that the process was a competition between the poly oxidation by O_3 and poly-oxide etching by HF. At a fixed temperature, the slower rate in either of the two reactions determines the overall etching kinetics. Based on the experimental data, the process seems feasible when proper HF and O_3 concentrations are met; 1000 Å (or 2000 Å) poly films can be stripped in reasonable periods without fully etching the underlying thermal oxide and causing damages on the silicon substrate. The process can be implemented on existing AKrion's tools without major modifications. Given the benefits of easier bath's monitoring/control, saver to use, and more environmental friendly processes, the proposed chemistry appears to be promising to replace the conventional application of concentrated HF/HNO_3 mixtures for wafer reclaiming.

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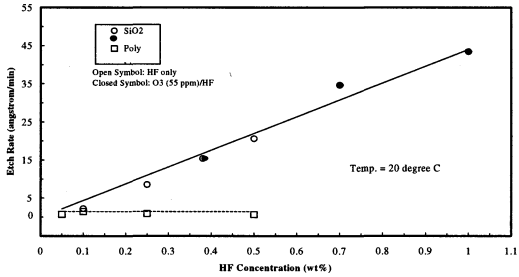

Figure 1: Etch rates of poly and SiO_2 versus HF concentration

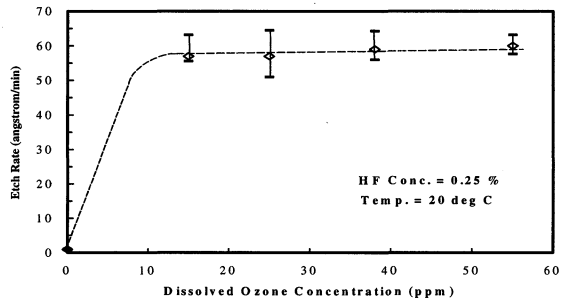

Figure 2: Etch rates of poly in 0.25% HF with various O_3 levels

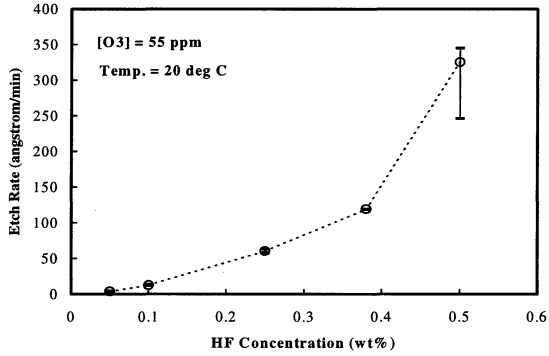

Figure 3: Etch rates of poly (small samples) in HF with 55 ppm O_3

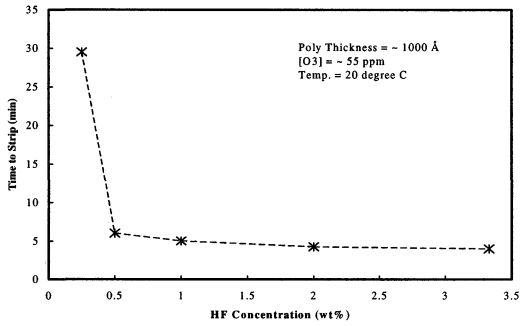

Figure 4: Etch time required for stripping entire poly wafers in HF/O_3

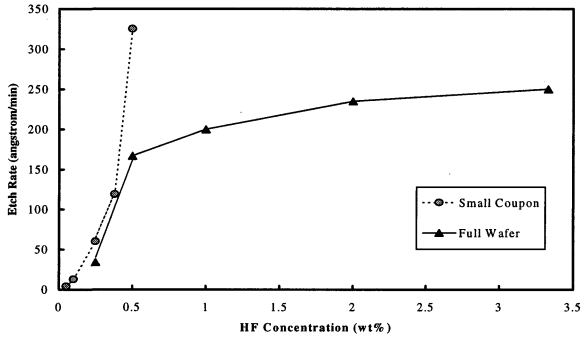

Figure 5: Etch rates of poly on full wafers in HF with 55 ppm O_3

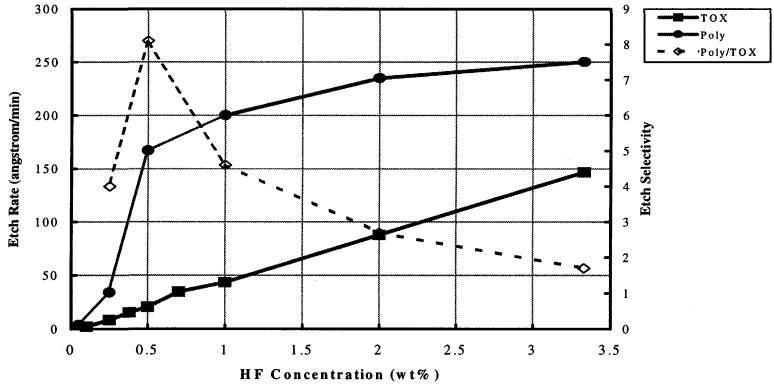

Figure 6: Etch rates and selectivity for poly and thermal oxide in HF with 55 ppm O_3

BACK END OF THE LINE (BEOL) CLEANING

AN ADVANCED BEOL CLEANING METHOD

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High-pressure liquid ammonia has been successfully used to clean post-ash residue from back end of line (BEOL) features: vias, trenches, and metal structures involving traditional oxide as well as the low-□ dielectric films. The advantage of using ammonia is that the wafers do not require a post-clean water rinse that could lead to corrosion of the metallic layer. Little changes are shown in the FTIR spectra and the index of refraction of low-□ materials upon exposure to liquid ammonia in the DFC system. The entire process involves using a plasma step to remove the bulk photoresist and pre-condition the residue then the liquid ammonia step. The plasma fluorinates residue and the breaks down the tough polymeric matrix, allowing the liquid ammonia to more easily dissolve the residue. The liquid ammonia has a low surface tension and viscosity allowing the liquid to easily penetrate deep via structures. Various mechanisms are proposed to remove the residue with the liquid ammonia process, both physical and chemical. The apparatus to process wafers safely using liquid ammonia at high pressure has been developed.

INTRODUCTION

The ability to clean a wafer of organic residue, particulate contamination, and metallic contamination without resorting to a solvent bath is a desired goal of many integrated circuit (IC) manufacturers. At present, all-dry post-etch ash and residue removal techniques have not yet been fully accepted for IC manufacturing. There are many known methods for an all-dry residue removal, but none has been successfully accepted into manufacturing. Some of the methods are laser based cleaning [1,2,3,4], cryogenic Ar/N_2 [5,6,7,8] or CO_2 [9] snowballs, high pressure SO_3 [10], or supercritical CO_2 [11,12].

One major reason that none of these all-dry clean concepts have been accepted into IC manufacturing is the driving force from a cleanliness standpoint. The cleanliness by these new technologies has not surpassed the ability to perform clean processes on traditional systems; such as wet surface conditioning, plasma ashers, and scrubbers. Additionally, none of these technologies has proven to be cost effective. Laser cleaning is an immature technology and extremely slow, less than 5 wafers per hour. Cryogenic Ar or CO_2 snowballs have limitations on the size of contacts the snowballs can penetrate and the surface tension of the liquid. While this technology has been demonstrated for post-chemical mechanical planarization (CMP), successful post-via etch cleans are in progress of being developed. Supercritical CO_2 has not yet proven clean enough for use in IC manufacturing, as organic materials are extremely hard to remove from CO_2. High pressure SO_3 is in the first stages of development, and SO_3 is not a desirable chemical to use in a fab.

The ability to implement a clean process on all of the new types of dielectric materials is critical. Plasmas, in particular oxygen plasma, may adversely effect the new low-□ dielectric constant materials in such a manner so as to modify the □-value, to augment the capacitance, and to change the bonding structure [13]. Wet chemistries employing water and solvents may also lead to modifications of the dielectric material [14]. Copper used for advanced technology interconnects is very susceptible to oxidation. Wet chemistries, both water and solvent, and oxygen plasma can cause the detrimental formation of a high-resistance layer. The ability to exclude any possible oxidizing material is imperative to the formation of reliable circuits.

Densified Fluid Cleaning (DFC) is a novel and unique dry cleaning method which has been applied successfully to BEOL post-etch residue removal. DFC is based on the application of liquid ammonia at high pressures and low temperatures to the wafer surface. DFC is a liquid-phase cleaning technology, similar to supercritical fluid applications. The liquid ammonia removes metallic and organic residues and particles from the wafer. A plasma pre-processing step may be coupled with the DFC step to improve the DFC efficiency. This paper will present the process applications and a proposed mechanism for the removal of residues with liquid ammonia.

EQUIPMENT

The DFC tool is composed of a high-pressure vessel and supporting components. Hot pressurized ammonia vapor is introduced into the reactor and condenses on the cooled wafer to form a thin liquid layer. Pressure in the reactor is controlled during the entire process at 10–25 atm (25 atm □ 300 psig). The platen is kept at a lower temperature (20–50°C) than surrounding reactor walls (80°C). The wafer is placed on a rotating platen with controlled speed (0-100 rpm). A megasonic device (837 kHz) with adjustable power (25–65 Watts) transfers mechanical energy to the wafer through the condensed ammonia.

Safety concerns are foremost with the DFC system. At 20°C ammonia gas starts to condense to a liquid at approximately 120 psig; the operating pressure of the DFC is 250 to 350 psig. Therefore, for safety considerations, the DFC process chamber must be able to withstand pressures up to 450 psig. In addition, the system must be equipped with an exhaust mechanism at critical locations on the DFC module that will mitigate the impact of accidental release of ammonia. All of the DFC components that handle or contain ammonia are designed with high factors of safety. Ammonia recycling is essential to low cost DFC technology. Recycling minimizes the cost of ownership and reduces the environmental impact of the process.

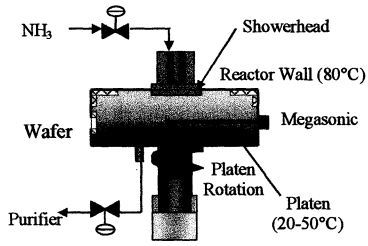


Figure 1. Schematic of the DFC tool.

RESULTS AND DISCUSSION

A multi-step process has been found to be optimal for cleaning the wafers. Figure 2 shows a schematic of the DFC process as a function of the chamber pressure.

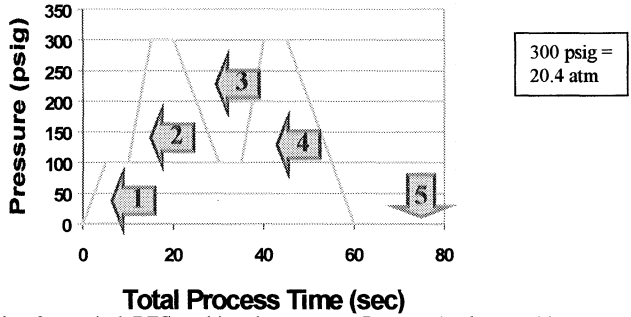


Figure 2. Schematic of a typical DFC multi-cycle process. Pressure is shown with respect to processing time.

1. The wafer enters the DFC chamber and is purged with nitrogen to remove any moisture and oxygen. Hot, high pressure, ammonia vapor then enters the chamber at a controlled pressurization rate.

2. The gaseous ammonia fills the chamber and the pressure rises. The vapor then starts condensing on the wafer surface. Upon condensing, a pressure plateau is reached as the liquid starts to form on the wafer. Once the liquid layer is formed, the pressure starts to rise again until the target pressure is reached. The pressure is controlled with a throttle valve, and the pressure is held steady between 5 sec and 30 sec. As soon as the ammonia is introduced into the chamber, the platen starts to rotate and the megasonic action is initiated.

3. The pressure is then decreased and the ammonia vapor exhausted from the process chamber. The pressure may be taken to atmospheric pressure or, as Figure 2 shows, to an intermediate pressure. Time control of the pressurization and depressurization step is possible.

4. A second cycle is then started. Multi-cycle processes are possible.

5. At the end of the process, the reactor pressure is released and the ammonia evaporates from the wafer surface. The ammonia is exhausted from the process chamber. This ammonia is available for re-circulation and purification. After atmospheric pressure is reached, a nitrogen purge is used to evacuate the any remaining ammonia in the process chamber. The wafer emerges clean and dry from the DFC tool with no need for additional water rinsing or drying process

Ammonia dissolves a broad variety of organic and inorganic substances and readily reacts with organometallic compounds. Ammonia reacts with alkali and alkali earth metals and forms complexes with many other metal ions, particularly transition metal ions like Cu and Co. This dual affinity towards organics and inorganics results in a strong interaction between ammonia and post-etch, metal-containing polymeric residues.

The high vapor pressure of ammonia (8.1 atm @ 20°C [15]), enables penetration in the gas phase into small voids such as vias. At elevated pressures the condensation occurs inside the voids, unlike traditional liquid cleaning methods which are based on liquid flow into voids. Ammonia also evaporates easily from the smallest voids, whereas liquid residues can be trapped inside. The low viscosity (0.141mPa*s @ 20°C) and low surface tension (18.05 mN/m @ 34°C [15]) of liquid ammonia enable wetting of the wafer surface and allows the liquid ammonia to penetrate high aspect ratio features and diffuse between small particles.

Studies have confirmed that liquid anhydrous ammonia does not damage materials commonly used for fabricating IC devices [16]. Materials tested include silicon where atomic force microscopy (AFM) after DFC exposure showed no change in the surface roughness. There is little change in the thickness or refractive index of oxides and low-□ inter-level dielectric (ILD) materials upon exposure of ammonia. Sheet resistivities of metals, such as Al, Ti, and TiN, also showed no change after exposure to DFC.

DFC has been successfully applied to remove heavy post-etch residue from via and metal layers after a low-temperature (< 80°C) photoresist (PR) removal step [17,18]. The liquid ammonia interacts both chemically and physically with the residues. The ammonia swells and partially dissolves the polymeric matrix causing fragmentation. Organo-metallic residue components, originating during the etch process, are extracted by ammonia from the sidewalls and bottom of the features. Additional mechanical energy is introduced to the wafer by megasonic excitation and the centrifugal forces detach the residue fragments from the wafer, enabling the particles to be carried away by the flowing ammonia.

Designed experiments were performed in the DFC tool to evaluate the influence of various process parameters on photoresist (PR) removal. In one experiment four factors were varied: megasonic power, ammonia pressure, total process time, and the number of pressurization cycles. The number of pressurization cycles and the megasonic energy were found to have the most influence on the photoresist removal. The other variables, total process time and ammonia pressure also showed some effects, but not to the magnitude of the number of process cycles or megasonics power.

Figure 3 shows the contour plot of the amount of photoresist removed with respect to the number of pressurization cycles and megasonic energy. The seven points (▪) scattered across the contour plot represent the actual experimental trials. Note at lower megasonic power the removal rate is enhanced. Either two or three pressurization cycles were found to be the optimum. Total process time is held constant in this contour plot, but there is little influence in total process time. Other experiments have shown that stabilizing the process at maximum pressure for 1, 10, or 100 seconds results in a small change in photoresist removal. Figure 2 shows an example of holding the maximum pressure of 300 psig for 5 seconds.

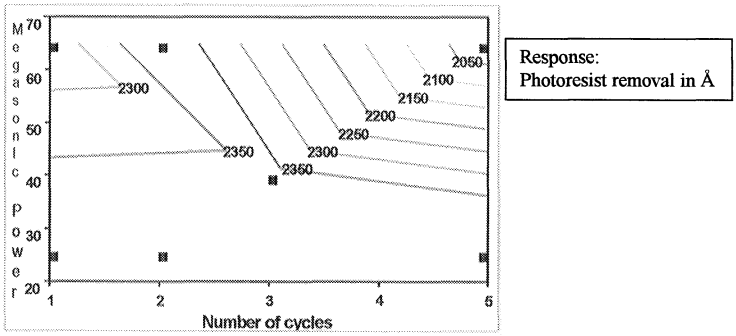


Figure 3. Representative contour plot of a DFC process experiment. The contour plot shows the effect of photoresist removal on the number of pressurization cycles and megasonics power at constant processing time.

Results of experiments show that increasing the reactor pressure causes more ammonia vapor to condense on the wafer surface, and thus, more PR to be solvated. One theory is that by increasing the pressurization rate, the ammonia can penetrate more efficiently into cracks or cavities of the PR prior to condensation. Higher rotation speed increases the centrifugal forces acting on the wafer and removes the liquid carrying PR material from the wafer surface, thus enabling fresh ammonia to condense on the wafer surface. Additional pressurizing cycles induce additional mechanical energy on the PR, causing it to swell, and hence to fragment, detach and be removed.

The mechanism of post-etch residue removal is suspected to be similar to the effect of removing particles from the wafer surface. Adhesion forces of the particle on the wafers surface are electrostatic, van der Waal, and magnetic [19]. Residue also may be chemically bonded to the underlying film. The residue in the via or on the metal sidewall, for example, is a matrix of organic material, metallic compounds, and silicon. To remove this matrix, which is usually a continuous film, the matrix must first be broken down into smaller particles. Once these particles are formed, conventional means may be used. In the case of covalent bonding of the particles on the wafer, silicon dioxide for example, a simple rinse, even with megasonics, is not enough to remove the particle. Plasma is used to physically break apart the residue from the surface by ion bombardment. In some cases the chemical reaction product is volatile. In other cases the particle remains on the wafer and can be removed by a simple rinse.

The mechanism proposed for removing the particle residue is a combination of megasonic action and a physical mechanism similar to thermophoresis. The megasonic action loosens the particle from the wafer surface due to the cavitation of fluid. The bubbles that are formed by the acoustic streaming violently implode and cause a shearing force that physically removes the residue [20]. Thermophoretic action is caused by a physical evaporation of the liquid ammonia which in turn causes a heat transfer to the

particle. This transfer of heat loosens the particle, and the fast flow from the cooler ammonia, as it is evaporating, washes away the particle [21].

The initial break-up of the residue, inside a via for example, is the reason the plasma pre-treatment is employed before the DFC process step. The reducing plasma pre-treatment ashes the photoresist, while not oxidizing the silicon in the residue The plasma step also partially breaks up the residue matrix. A reducing chemistry plasma is found to be optimum for many reasons: the silicon in the residue is not oxidized, the low-□ dielectric material is not augmented, and the photoresist is effectively removed at low temperatures.

Examples of FTIR (Fourier transform infrared) spectra of Allied Signal's HOSP™ low-□ material before and after exposure to liquid ammonia in the DFC are shown in Figure 4. There are only slight modifications of the vibration modes or bonding of the low-□ material after exposure to DFC. The peak that shows the most modification is the S-H at 2250 cm^{-1}. A slight decrease in the intensity indicating there is less Si-H bonding. The other peaks, C-H at 3000 cm^{-1}, Si-C at 1300 cm^{-1}, or Si-O at 1050/1120 cm^{-1}, show no augmentation that would indicate a reaction with ammonia. Note there is no water addition (peak at 3300 to 3600 cm^{-1}) or any indication nitrogen has been incorporated into the film. Other low-□ materials have been tested with similar results.

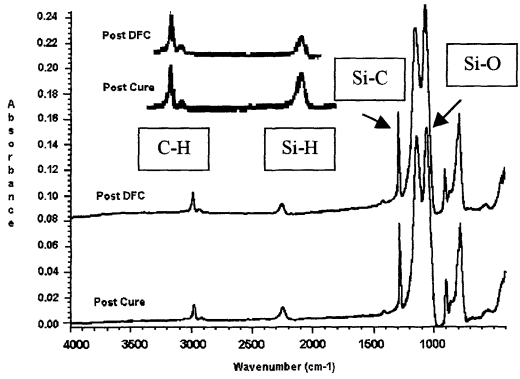


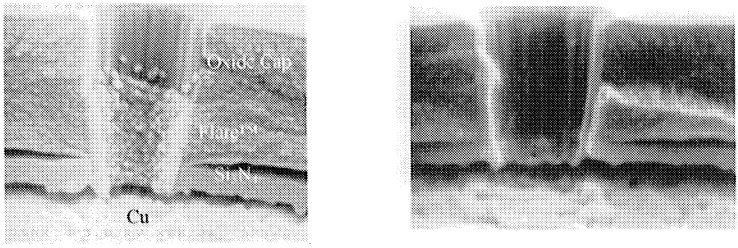
Figure 4. FTIR spectra of Allied Signal's HOSP™ low-□ material before and after exposure in the DFC system to liquid ammonia.

Low-□ material	Change in thickness (Å)	Change in refractive index	Delamination after boiling water
FLARE/Si	28	0.012	pass
FLARE/Nit	6	0	pass
SiLK/Si	48	0.006	N/A
PTFE/Si	-14	0.001	N/A
HOSP/Si	-104	0	pass
BCB/Si	4	0.002	N/A
Nanoglass/Si	69	-0.015	pass
Nanoglass/ox	92	-0.014	pass
Coral	60	0.0005	N/A

Table 1. Various low-□ materials and their change in thickness, index of refraction, and adhesion properties after exposure to liquid ammonia.

A table showing the changes in thickness, index of refraction, and ability to adhere to the underlying material is shown in Table 1. There is essentially no change in thickness or index of refraction of various low-□ after processing in the DFC chamber. For some of the less dense low-□ materials, such as HOSP™, the shrinkage is greater, perhaps due to the high processing pressures. Other low-□ materials that are less dense, such as Nanoglass, also experience a swelling of the film, perhaps due to the ammonia expanding into the less porous structure.

An example of the removal of post-etch residue using low-□ material is shown in Figure 5. The low-□ material is Flare™ and the underlying layer is Cu. The sidewall residue is apparent on the via wall. The polymer is imbedded with the sputtered copper from the via bottom. The sidewall and bottom residues were completely removed with the DFC in this concept and feasibility study and there is essentially no change in the via critical dimension. Flare™ is known to be attacked by oxygen plasma due to the high carbon content of the film, thus only the DFC without the plasma pre-processing step was used for this sample. The low-□ material stayed intact with treatment of liquid ammonia. Therefore, a clean process, such as the DFC, is advantageous when a clean method is required that does not effect the low-□ material. Table 1 shows minimal change in refractive index of the Flare™ and the FTIR spectra (not shown) also showed no change in the bonding structure.



a) Post-etch **b)** Post-clean

Figure 5. Example of a via cleaned with DFC. **a)** SEM micrograph (80KX) of the post-etch, pre-DFC cleaned wafer. **b)** SEM micrograph of the same sample after DFC clean.

CONCLUSIONS

DFC is an innovative liquid ammonia-based, low-temperature cleaning technology. The use of ammonia as the cleaning medium takes advantage of the positive aspects of both the properties of the vapor and liquid states. Enhanced diffusion into and out of the high aspect ratio via, coupled with the mechanical removal of residues by megasonic action and solvation, lead to a process that extends beyond the current wet clean capabilities.

The ammonia reacts chemically and physically with wafer residues and contaminants to remove them from the wafer surface. This action is further enhanced by the application of megasonic energy, which physical breaks apart the residue, and possibly by thermophoretic effects. Examples of using DFC successfully on via structures with low-□ materials have been shown. DFC has no adverse effects on the materials commonly used IC manufacturing, including various low-□ materials, oxides, and metals. A DFC-only process can be used when a film cannot be exposed to an oxidizing plasma or a water rise that could cause corrosion. The DFC system is manufactured to meet safety requirements. Safety interlocks are in place to allow high pressure processing and the use of liquid ammonia.

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MINERAL DIELECTRIC CLEANINGS DURING COPPER METALLIZATION PROCESSES

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Abstract

For 0.25 µm technologies Cu contamination on backend dielectrics has to be reduced to the 1^E13 at/cm^2 level at wafer front sides. After CMP and etching, local Cu contamination levels can be very high: 1^E14 to 1^E16 at/cm^2. Efficient cleanings therefore have to be performed. New cleaning processes to be developed paradoxically have to be efficient enough to remove Cu contamination and also preserve the Cu lines. Dissolved O_2 in HF-based chemistries performed in the dark gives satisfactory results (except after damascene etching for Cu contamination located on the side-walls) due to the combined effects of acidic dissolution, complexing and under-etching properties.

INTRODUCTION

Replacement of Aluminium by Copper for interconnects represents a potential gain in resistivity and electro-migration but also a new challenge in terms of cleaning. In this paper Copper contamination removal is studied on mineral damascene structures. First the critical backend steps where Copper contamination has to be well controlled are identified. Then different cleaning strategies are investigated and tested on patterned wafers.

CRITICAL BACKEND STEPS FOR COPPER CONTAMINATION

Copper effects on devices:

Interstitial Copper ion is known (1,2) as one of the fastest diffusers in Silicon. It can diffuse even at room temperature in the first microns of Silicon (3). In SiO_2 the diffusion coefficient is about 8 orders of magnitude lower than in Silicon (4) except if an electrical field assists diffusion. SiO_2 can therefore be used as a barrier when disposed at the wafer backside but not between two interconnection lines for example. New and conventional barriers such as TiN and Ta-TaN are efficient for Cu. The contamination risk is when Cu is present in Front End Of the Line steps where no barrier is provided and before barrier deposition in Back End Of the Line.

In FEOL devices the main detrimental effect caused by Cu is the junction leakage due to its diffusion and segregation in N+ areas (5). The minority carrier lifetimes are in practice not affected directly by Cu but by the defects it induces at low process temperature -250 °C (6). The Cu virus can be introduced by cross contamination, typically by contaminated backsides and bevels of BEOL wafers on shared analytical tools. Therefore, backside and bevel cleaning is one of the new plant protocols among others such as specific tools, separate cleanrooms, distinctively colored clothes, boxes, etc. An additional constraint to be considered in fabs introducing Cu consists in adding a barrier at

wafer backside such as SiO_2 and Si_3N_4 as from the first step of the incoming wafers. This protects against Cu diffusion from backsides. The backside and bevel contamination threshold levels for which the cross contamination risk during wafer handling becomes acceptable is not easy to determine. In this study this threshold has been arbitrarily chosen at 1^E11 at/cm^2.

In 0.25 µm BEOL devices, Cu contamination left by CMP on flat insulator surfaces was demonstrated to cause direct shorts between 2 Cu lines by percolation conduction when the Cu concentration is above the 1^E14 at/cm^2 range. The same amount of Cu was demonstrated to drastically accelerate aging of PECVD TEOS oxide in Bias Thermal Stress reliability tests (7).

Finally, for 0.25 µm technologies, Cu contamination must be under 1^E13 at/cm^2 at SiO_2 top and side-wall interfaces and lower than the 1^E11 at/cm^2 range at backside during Cu interconnect steps.

Residual copper contamination levels after different processes

The maximum residual Cu contamination levels observed after different backend steps are given in table I.

	CVD Deposition		After CMP		After Scrubber			After etching down to Cu line		
	Front	Back	Front	Back	Front	Back	Bevel	Top	Side	Back
Contamination max (at/cm^2)		* 1^E15	*** 5^E14	* 2^E14	*** 4^E13	* 2^E13	** 2^E14	*** 6^E14	**** >E16	* 1^E12
Nature	Cu°, CuF_2	Cu°, CuF_2	Cu°, CuO	Cu° CuO	CuO, Cu_2O	CuO Cu_2O	?	?	?	?

Table I: Residual Cu contamination levels as measured by *: TXRF, **: LPD-AAS, ***: TOF-SIMS, ****: TEM on SiO_2. The Cu natures were determined by XPS.

In Cu CVD the wafer backside can be greatly contaminated by Cu metal. (On the other hand, in Electro Chemical Deposition where the backside is protected; the residual contamination level is below the TXRF detection limits).

CMP leaves about 1^E14 at/cm^2 of Cu on both front and back sides. Then scrubber using 1% ammonia enables this contamination to be decreased by one decade. In fact this level results from an equilibrium between Cu removal and transfer of Cu from lines to neighboring insulators. Figure 1 simulates this behavior by scrubbing a clean wafer just after a wafer with a full sheet layer of Cu or W. This didactical experiment minimizes the actual Cu transfer between one line and the adjacent insulator. Bevels measured by Liquid Phase Decomposition technique are in the 1^E14 at/cm^2 range in terms of Cu contamination.

At the end of via etching Cu is projected from the underlying metal line on the side-walls (see figure 2) and to a lesser extent at the top surface (8). After etching, the nature of the top and side-wall Cu contamination is difficult to identify and probably depends on the plasma chemistry and the type of photo-resist.

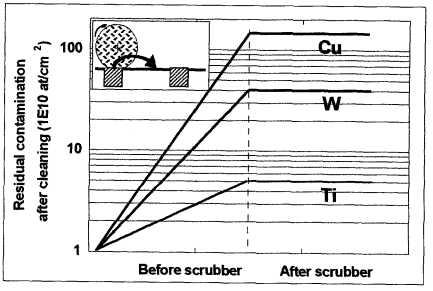

Figure 1: TXRF analysis of initially clean wafers scrubbed just after 1 wafer presenting apparent Cu, Ti or W layers.

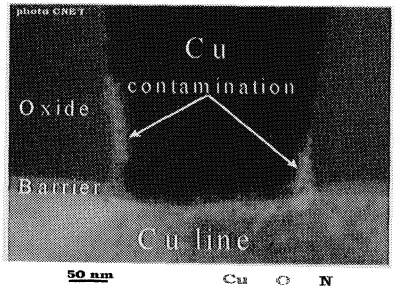

Figure 2: TEM elemental analysis after 0.25 µm via etching down to the Cu line.

Most of the measured Cu levels are far higher than the requirements. It is clear that the most difficult cleaning steps are after CMP and after via etching down to the underlying Cu line because in both cases Cu interconnects are in contact with the wet cleaning solutions. The challenge consists in removing Cu contamination without consuming Cu lines, barriers and insulators too much. Therefore conventional aggressive hot oxidant solutions (SC2, SPM, ...) are not suitable for this application. They can only be used for backsides in specific tools which are able to treat backsides only.

BASIC MECHANISMS FOR COPPER CONTAMINATION REMOVAL

In this first part Cu cleaning is studied on full sheet wafers presenting intentionally contaminated dielectric films. This preliminary step is necessary to understand the basic mechanisms. This structure is representative of backside surfaces only.

Cleanability of Si-based dielectric materials with respect to Cu

When Si atom clusters are available at the material surface to be cleaned, the Cu^{2+} ions that have just been removed can very quickly redeposit by oxidizing this free Silicon whatever the oxidant, complexing or acid properties of the cleaning solution. This is for example the case of some PECVD TEOS oxides which can contain non fully oxidized Si. As shown in figure 3 this type of surface can be cured by an oxidant anneal (wafers initially contaminated by spin coating technique). Another type of behavior was identified with SiON Anti Reflecting Coating where the top surface can be cleaned very easily but when the surface layer is removed (> 5 nm) the bulk of the SiON film is not cleanable. This behavior imposes its full elimination during the CMP step.

Copper oxide removal: CuO/Cu_2O

From Pourbaix diagrams (9) it is predicted that CuO and Cu_2O species are easy to dissolve in acid media: Cu_2O in diluted HF, H_2SO_4 and H_3PO_4, CuO in all diluted acids. This is confirmed by the tests shown in figure 4 where annealed PECVD TEOS oxide is initially contaminated by spin coating at 1^E13 at/cm^2 level. As determined by XPS (table I) this deposition technique deposits Cu species into a mix of both Cu oxidized forms. Whatever the cleaning tested 2 orders of magnitude of Cu contamination is removed. Nevertheless, the best results are obtained with HF-based chemistries which cumulate acidic solvation, complexing and under-etching properties.

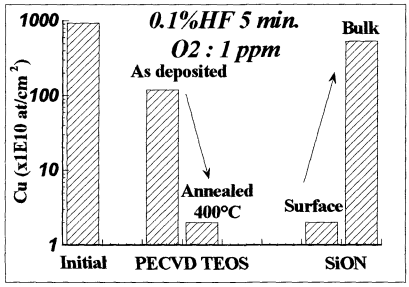

Figure 3 : Cu contamination cleaning behaviors of different materials.

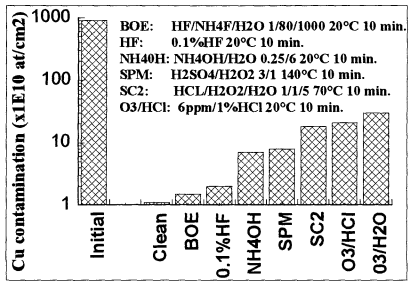

Figure 4: CuO/Cu_2O removal on annealed PECVD TEOS oxide.

Copper metal removal: Cu°

From reference (9) Cu° contamination can be removed by using a strong oxidant in acidic media. To preserve the outcropping Cu interconnects the oxidant etching speed has to be maintained at a low level. Finally the cheapest and most convenient way to remove Cu° contamination consists in adjusting the dissolved oxygen content in acid or highly complexing baths by O_2 bubbling (figure 5). The kinetics of the oxidation reaction written hereafter is slow enough to preserve the apparent Cu:

$$O_2 + 4H^+ + 4e^- \Leftrightarrow 2H_2O \qquad E° = 1.23\ V$$

$$x\,2\ \ [Cu \Leftrightarrow Cu^{2+} + 2\,e^-] \qquad E° = 0.34\ V$$

As seen in figure 6 different oxygenated cleaning solutions were tested on Cu° contamination deposited on silane oxide by CVD. Again diluted HF mixtures give the best Cu° removal efficiency due to their high complexing properties and to the under-etching effect. The higher the HF concentration, the longer the process time and the greater the removal efficiency (see figure 6). Hot phosphoric acid which does not attack Cu lines represents an interesting mixture as well. On the other hand, complexing alkaline mixtures such as ammonia or a commercial choline-based mixture which drastically reduce the passivation areas give modest efficiencies only, even after a long process time.

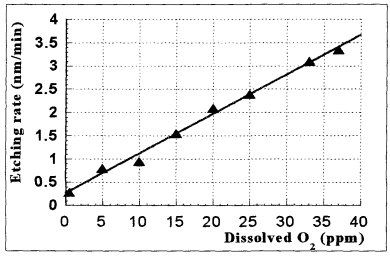

Figure 5: Use of O_2 dissolved in diluted acids (here 0.1%HF) to control the Cu° etching rate during cleaning.

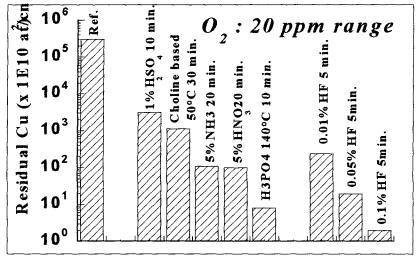

Figure 6: Cu° contamination removal on silane oxide in different mixtures (TXRF)

Other Cu species removal

During backend processes Cu can be present in other forms such as Cu salts, CuF_2, $CuCl_2$,... According to Pourbaix, these species are very easy to dissolve in acidic media. Furthermore Cu can be embedded in side-wall polymers or slightly diffused into materials. These types of Cu contamination may be present mainly after etching steps (presence of polymers and local high temperature) and after hot steps such as CVD deposition. They probably represent the most difficult Cu contamination type to remove.

Corrosion and photo-corrosion effects

Unlike Ti, Al, Ta and W, Cu oxides are not tight enough to prevent further corrosion from occurring. Even if passivation is established on full sheet Cu layers, it must be verified on actual devices. Indeed Cu passivation can be lost by the different potential induced by the presence of foreign metals. As an example the difference of behavior of Cu in HF-based chemistry (pH=7) with or without Titanium nitride is illustrated in figure 7. According to the Pourbaix Diagram, at this pH Cu is theoretically passivated by CuO as verified by the slight increase of the copper layer thickness. But in the presence of Titanium nitride Cu is severely corroded (1.5 hours in 0.1% HF + FNH_4 at pH=7).

Furthermore, another unexpected photo-corrosion effect has been observed on actual chips. As illustrated in figure 8, during the post-CMP cleaning step -1 minute- all the Cu in one particular type of line was removed (the 3 disclosed W plugs can be seen in the center of the picture) and re-deposited on the other Cu line type. The layout revealed that the first type of line was connected to the p-side of a junction whereas the second was connected to the n-side of this junction.

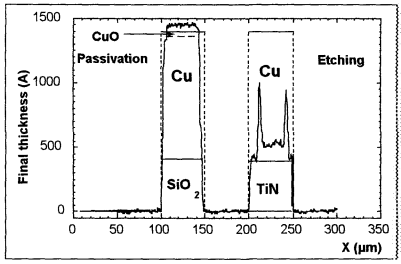

Figure 7: Profilometer results illustrating the difference of Cu etching rate in the presence or not of TiN.

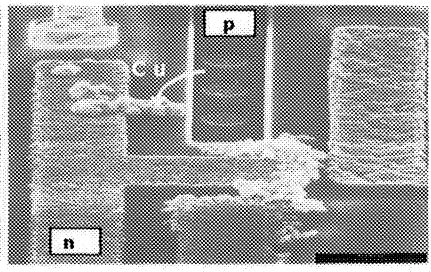

Figure 8: SEM view of the Cu line transportation during post-CMP cleaning by photo-corrosion effect.

This behavior is due to the difference of electrical potential created by the photons in the MOS junctions which act here as solar cells as soon as the lines -electrodes- are connected through the cleaning solution. As represented in figure 9, the electron/hole pairs photo-generated in the junction are separated by the presence of the junction electrical field. These carriers, in excess with respect to the thermodynamic equilibrium, induce a potential difference between the two sides of the junction. This potential increases with the light intensity and can theoretically reach in open-loop conditions a maximum value corresponding to the junction height (typically between 0.3V and 0.6V in Silicon). At this potential the electrical field in the junction is annulled which interrupts the electron/hole

separation mechanism. In short-circuit conditions photo-generated carriers are drained out to the external circuit. The current is roughly proportional to the light intensity.

In solution, photo-voltage and -current between electrodes are controlled by the different redox couples present in solution such as foreign ions, but also dissolved oxygen and water. At the electrode connected to the p-side of the junction, Cu is corroded by the oxidation reaction - Cu ---> Cu^{2+} + 2.e^- - while the soluble Cu^{2+} species can diffuse to the other electrode where the opposite reaction can occur: reduction of Cu^{2+} to its metallic form Cu°.

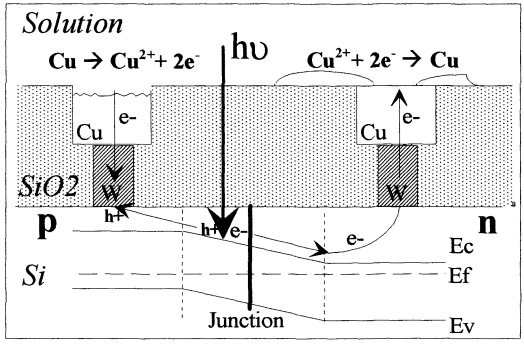

Figure 9: Schematic illustration of a photo-assisted corrosion phenomenon during damascene interconnect post-CMP cleaning.

The best methods of reducing this phenomenon consist in adding corrosion inhibitors and reducing the light as far as possible using for example closed chamber cleaning tools. The additives which allow this phenomenon to be reduced are presented in references (10) and (11).

CLEANING PERFORMANCES ON ACTUAL PATTERNED WAFERS

Cleaning tests were performed on 0.25µm-technology damascene structures using dielectric materials optimized in terms of cleanability.

Cleaning after Copper CMP

As defined earlier (12), cleanings after CMP processes have 3 main purposes: removing slurries, eliminating the damaged layer left by the force exerted by the pad and decreasing the Cu contamination at the top surface between Cu lines and from backsides and bevels. This paper deals with the Cu contamination step only. After CMP Cu contamination may be present as Cu oxides due to the use of oxidant slurries and also as Cu° particularly in topological depressions due to dishing effects. Indeed, as represented in figure 10, a dishing at the level immediately below can induce its own shape in the level above. If CMP over-polishing is not sufficient, large areas of Cu° may be left, generating catastrophic shorts.

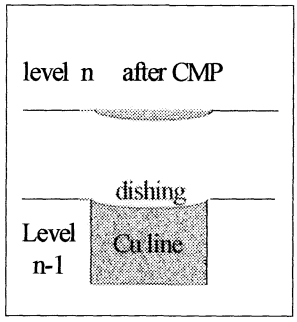

Figure 10: Residual Cu° remaining after CMP due to dishing at level n-1.

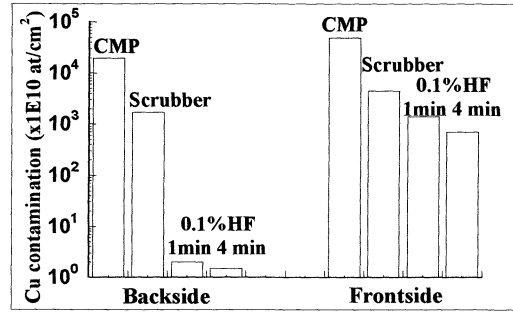

Figure 11: Cu contamination removal efficiencies obtained with HF cleaning solutions at both wafer back and front sides after Cu CMP.

After Cu CMP and scrubber, patterned wafers were cleaned by the best tested chemistry: dHF. Then large dielectric areas were analyzed by TOF-SIMS (90°). Figure 11 shows the Cu contamination removal obtained both on front side (Silane SiO_2) and backside (PECVD TEOS SiO_2). It is much easier to remove Cu contamination from wafer backsides than from high density interconnect areas. This difference of behavior may be attributed to a slight diffusion of Cu into the oxide at the end of the CMP which could explain the superiority of HF. A local precipitation is unlikely as a rough diffusion calculation shows that the Cu concentration a quarter of a micron from the etched Cu line is almost in the 50 ppm range i.e. well below the solubility limits of $Cu(OH)_2$ and CuF_2 in 0.1%HF ($D=1^{E}$-5 cm^2/s, etched Cu: 2 nm in 1 min.). Furthermore precipitation of Cu oxides in HF seems very difficult as they are very soluble.

Cleaning after via etching

In damascene technology, vias and lines are simultaneously etched down to the Cu of the previous interconnect level. Cu is pulverized on the side-walls and to a lesser extent at the top of the insulator surface. Figure 12 shows the removal efficiency of the best tested chemistry: dHF as measured by TOF-SIMS (30°).

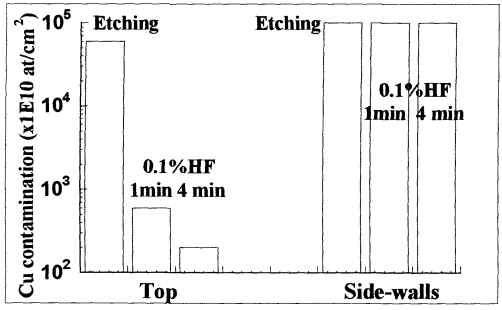

Figure 12: Cleaning efficiency of HF mixtures for top and side-wall contamination.

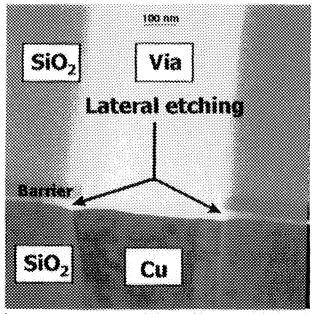

Figure 13: Parasitic effects of HF mixtures.

0.1%HF cleanings reduce back-side contamination as low as the results presented in figure 11 (cleaning after CMP). HF-based mixtures are therefore able to clean top and backside surfaces but not the side-walls. This may be due to slight diffusion of Cu and formation of Cu-polymer compounds. Reducing pre-treatments can be performed in this case. Anyway, HF concentration and process time have to be reduced in order to limit the parasitic etching effects particularly at the SiO_2/barrier interfaces (see figure 13).

CONCLUSION

For post-CMP and via etching, very diluted HF-based chemistries with dissolved oxygen performed in the dark or with strong corrosion inhibitors give the best results. Nevertheless after via etching it could be helpful to add a previous strong reducing treatment probably because Cu is mixed with side-wall polymers or located at a noticeable depth in the dielectrics.

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SiLK™ SURFACE CHEMICAL TREATMENT

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Abstract

In this paper we investigated the chemical compatibility of SILK™ for different possible cleaning solutions. Firstly the chemical stability of this material was evaluated by FTIR, XPS, index and thickness measurements. Then the electrical properties, such as dielectric constant, current leakage and breakdown time, were checked by C(V) measurements. As a result, HF and Ozone treatments have to be eliminated. Furthermore the cleaning solutions were tested in terms of Copper contamination removal by using TOF-SIMS and TXRF. As a conclusion, electrical results on Cu-SiLK interconnects show the necessity of cleaning after etching.

INTRODUCTION

As interconnect dimensions are becoming increasingly smaller, the resistive-capacitative (RC) delay has to be reduced as much as possible. The RC factor reduction can be achieved by a decrease of the metal line resistance and the capacitance of the InterLayer Dielectric (ILD) (1). The introduction of new materials and new architectures is a direct consequence of this necessity. Over the last few years, integration of Copper with silicon oxide in the so-called Damascene architecture and integration of low K with aluminium have been achieved. The final goal is the integration of both low K and Copper (2).

Indeed Copper improves circuit performance by lowering resistance, low K materials reduce capacitance. As Copper is universally well known as the natural substitute for Aluminium, on the other hand the choice of the low k material is still open (3). Today, many suppliers propose new low k materials: CVD oxides (with Fluorine or Carbon to reduce the dielectric constant), spin-on polymers and porous materials. Each new material represents a new challenge, in terms of reliability, manufacturability and integration. The actual dielectric properties of the material, its thermal and mechanical stability and overall compatibility with the new BEOL structures, the availability and economics of the deposition processes and the cost of the material itself have to be carefully considered. Among these new low K materials a completely polymeric material called SiLK™ is considered as one of the best candidates to replace Silicon oxide. At LETI the feasibility of a Copper/SiLK™ integration in a dual Damascene structure has been demonstrated (figure 1) (4).

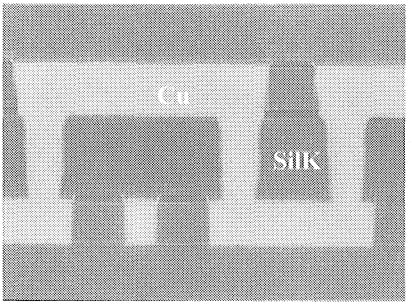

Figure 1 : SEM cross section observation of a Cu/SiLK™ DLM

SiLK™

SiLK™ is a recently developed non-fluorinated spin-on material supplied by the Dow Chemical Company. It has a dielectric constant at 2.7 and a thermal stability above 450°C (5). It adsorbs UV, enabling the ARC substrate to be eliminated. It is a weakly porous material (diameter pores smaller than 25Å and BET surface < 200 m^2/g). As shown in figure 2, the use of SiLK™ integrated with Copper enables a 40% gain to be made in terms of total capacitance (4).

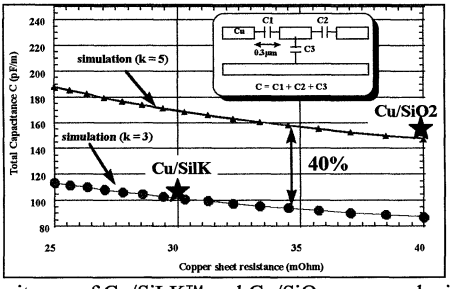

Figure 2 : Total capacitance of Cu/SiLK™ and Cu/SiO_2 compared with simulation results.

As SiLK™ is not a mineral dielectric, a new approach is necessary to find the adequate cleaning solutions.

WHY IS CLEANING REQUIRED AND WHEN ?

In the Cu-SiO_2 Dual Damascene architecture, the necessity of chemical cleaning to decontaminate the bottom of the via has been demonstrated (figure 3) (6). This is due to the fact that elimination of the SiN layer opening out on the Copper substrate pulverizes Copper on the edge of the vias. This Copper has to be eliminated before deposition of the barrier in order to avoid contamination of the oxides.

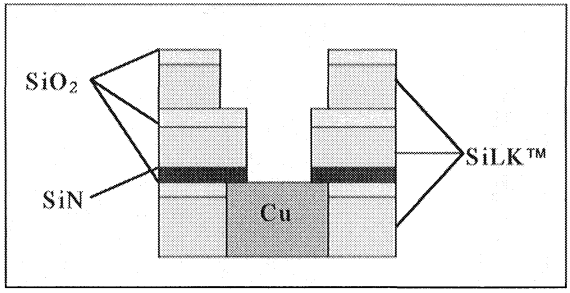

Figure 3 : Example of Dual Damascene structure after the etching process.

EXPERIMENTAL

For evaluation of the wet solutions, blanket wafers with SiLK™ I are used, spin-on deposited directly on silicon substrates, coated and cured at 450°C.

Different cleaning solutions were tested: NH_4OH, HF, HNO_3, H_2SO_4, O_3, IPA, Acetone, HCl, SC1, H_2O at 2 different concentrations (0.1% and 10%).

The chemical stability was evaluated by FTIR, XPS and reflectometry, the electrical characteristic by C(V) measurements, and the Cu contamination by TOF-SIMS and TXRF.

COMPATIBILITY OF CLEANING SOLUTIONS WITH SiLK™ MATERIAL

Surface modifications

No particular visual modifications of the SiLK™ surface were observed after 10 min in the different tested solutions, except in the case of HF treatment. The HF diffuses through the SiLK™ pores and attacks the interface, causing SiLK™ lift-off (figure 4). The interface is constituted by the adherence promoter and possibly by a small amount of native oxide.

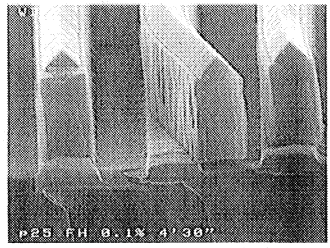

Figure 4 : SiLK lift-off due to HF solutions (SEM image).

No important variation of optical index or thickness was observed after each treatment.

The SiLK™ surface is normally hydrophobic after different chemical treatments, except after IPA and concentrated H_2SO_4. The hydrophilic modification of the SiLK™ surface after concentrated H_2SO_4 was also able to be understood using XPS (see next).

Chemical evolution

Among the tested solutions, only ozone treatment produces a sensitive FTIR spectrum evolution, as verified in figures 5 and 6. A peak corresponding to the ketone group is formed (peak at 1703 cm^{-1}) and a degradation of the ether function is highlighted.

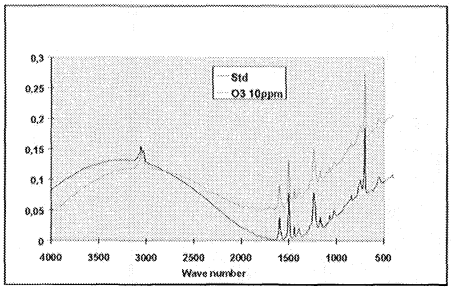

Figure 5 : FTIR SiLK spectrum before and after ozone treatment.

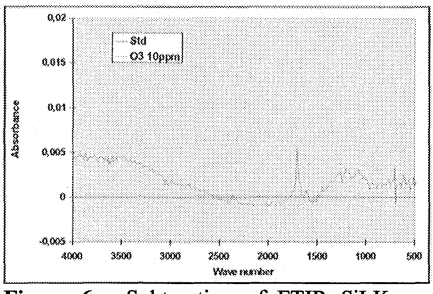

Figure 6 : Subtraction of FTIR SiLK spectrum before and after ozone treatment.

From FTIR analysis, it can be asserted that the chemical structure of SiLK™ remains unchanged in all cases except for ozone treatment.

From XPS analysis, no influence has been highlighted for the different treatments, except in the case of concentrated H_2SO_4 and ozone. After concentrated H_2SO_4 the ether group R-O-R' is transformed into polar termination R-OH, which explains the hydrophilic nature obtained, and into R-S at the surface. The ozone treatment increases the oxygen content, which could be correlated to formation of the ketone group.

Electrical properties

As illustrated in figure 7, no significant change of the dielectric constant was observed, except for the ozone treatment (ε=2.95). This change could be induced by the presence of the ketone group.

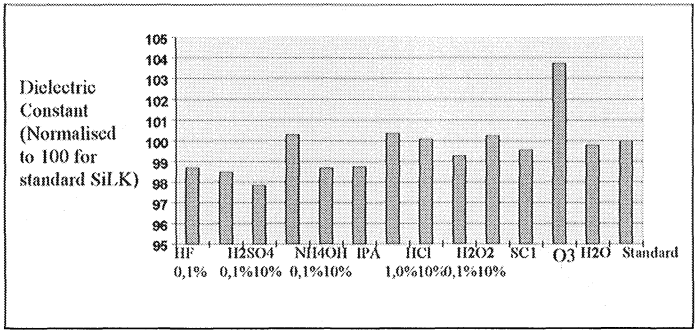

Figure 7 : Impact of cleanings on the SiLK™ dielectric constant.

The current leakage remains very low except for HF treatment (figure 8).

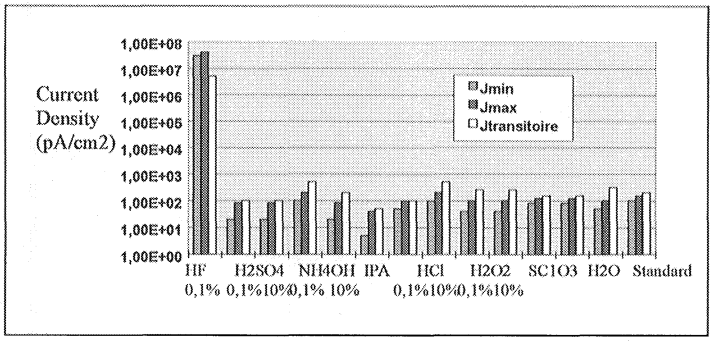

Figure 8 : Current leakage evolution after cleanings.

A significant decrease of the breakdown time was observed, under constant electrical field. In particular for HF, NH_4OH and HCl treatments.

INTENTIONAL COPPER CONTAMINATION

Different techniques were used to contaminate the SiLK™ surface with Copper.

Contamination by contact with a contaminated solution (until 1000 ppm in Cu) or by processing in an etching tool is not efficient ($\approx 1^E10$ at/cm²). This beahviour shows the robustness of this material for Cu contamination coming from solutions (CMP, cleaning, scrubbing...).

On the other hand contamination by passage in a Copper CVD reactor and by direct contact with Copper powder is highly efficient ($\approx 1^E15$ at/cm²). In the last two cases, TOF-SIMS analysis shows the presence of Copper inside the SiLK™ bulk, due to the passage through the pores.

Cu CLEANING INTO SiLK MATRIX

Different cleaning solutions have been tested on Copper contaminated SiLK™ substrates. Contamination on blankets was obtained by processing in a Copper CVD tool. The results are shown in figure 9.

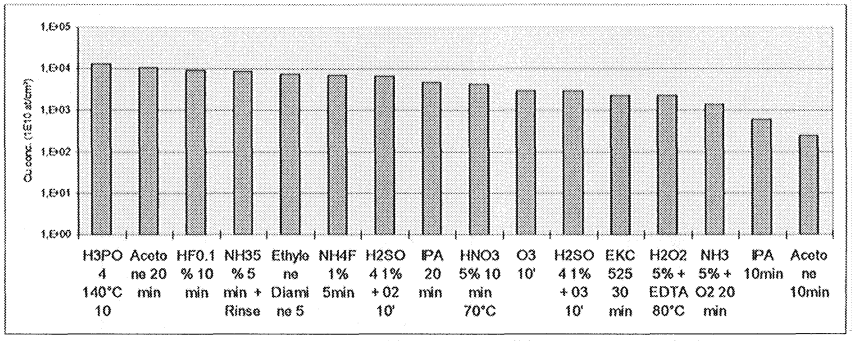

Figure 9 : Copper cleaning efficiencies of different tested solutions.

Contamination is difficult to eliminate, because of the probable presence of Copper inside the pores of the SiLK™. Also solutions normally able to strongly attack Copper, such as NH_4OH or H_3PO_4, are not efficient. Only the use of organic solutions allows cleaning down to some $1^E12at/cm^2$, as measured by TXRF. In spite of large variety of tested chemistries, an efficient solution able to remove Copper contamination deposited by Cu CVD tool has not been yet found.

Cu-SiLK™ INTEGRATION

During the Cu-SiLK™ integration, a commercial NH_4F based SiLK™ compatible stripping-cleaning process was used to remove the residues and reduce the copper oxide at the bottom of the vias, without SiLK™ profile degradation which occurs with diluted HF cleaning followed by reactive H_2 (figures 10a -10b).

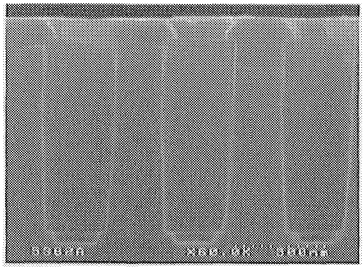

Figure 10a : SiLK™ profile degradation during HF cleaning followed by reactive H_2

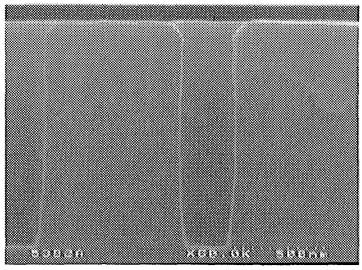

Figure 10b : SiLK™ profile after a SiLK™ compatible cleaning process

With this SiLK™ compatible cleaning process an improvement of the via resistance was obtained, as illustrated in figure 11, thanks to polymer and Copper elimination.

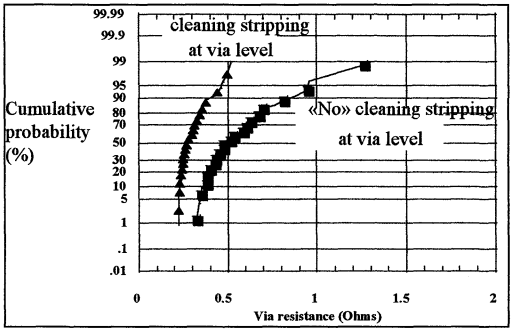

Figure 11 : 0.3µm Cu/Cu kelvin via resistance

CONCLUSIONS

Through the study of SiLK™ material, the cleaning of organic layers in microelectronic is opened up. It is now clear that organic materials present a completely different behaviour compared to mineral materials. This means a new approach in studying the wet chemical treatments. Among these, the use of new analytical tools is necessary. Moreover, the contamination removal by under etching is not possible. Strong chemical reagents are able to modify the polymer structure. In a possible Copper integration, Copper metallic contamination can diffuse in the material bulk. HF is completely avoided. Also O3 treatments are not allowed. Organic chemistries are compatible and lead to unexpected contamination removal efficiencies.

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RINSE CORROSION PREVENTION IN COPPER AND ALUMINUM BACK-END-OF-THE-LINE (BEOL) WET CLEAN PROCESSES

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ABSTRACT:

As critical dimensions continue to shrink, the impact of corrosion on metal features in back end of the line (BEOL) integrated circuit (IC) manufacturing processes becomes of greater concern. Corrosion that once occurred unnoticed will have widespread effects on IC performance today and in the future. A common type of corrosion that can occur in BEOL wet processing is often the result of the interaction between process chemical and ultrapure de-ionized rinse water (DIW).

In an effort to better understand this type of corrosion and ultimately arrive at a solution to the problem, this study examined the corrosive effects of a selection of commercial process chemistries with TiN, Al/Cu, and Cu using blanket metal films and an electrical test structure. The efficacy of a selection of organic and inorganic corrosion inhibitors added to rinse baths was also tested and shows promising results. The use of corrosion inhibitors in the rinse bath makes it possible to eliminate intermediate solvent rinses commonly used to reduce this type of corrosion. Furthermore, an automated system for delivery of selected corrosion inhibitors to DIW rinse baths to reduce or eliminate rinse corrosion was developed and is described in this paper.

INTRODUCTION:

New Materials and Methods of Corrosion

Advanced IC structures are becoming more complex to avoid yield losses caused by electromigration and interdiffusion{1,2}. Multilayer barrier metal schemes and metal alloys have been employed to reduce these problems but with these schemes has come a new set of concerns. These new concerns include problems associated with post metal etch cleans which address new forms of post etch and post ash residues. In many cases, these residues have proven difficult to remove and require more aggressive wet cleaning chemistries. Copper is a metal with many advantages when introduced as a metal interconnect in integrated circuits to enhance performance but the use of copper has also has introduced problems such as the tendency to corrode if not treated properly. This is because copper does not develop native oxide corrosion protection as readily as other metals such as aluminum. Corrosion of copper during via cleans in damascene and dual damascene process schemes can result in high contact resistance, undercutting and lift off of dielectric layers, and new organometallic etch residues, all of which can effect yield in the manufacturing process.

The new wet process cleaning chemistries developed for these metals and metal schemes may clean selective residues with low levels of metal corrosion during the clean but often result in corrosion to the metal when carried on the surface of the wafer into the

subsequent DIW rinse bath. With all metals and metal integration schemes, as critical dimensions shrink to 100nm and smaller, metal etch rates of even tenths of an angstrom per minute become problematic. With these concerns, this study examined the corrosion effects associated with a selection of commercially available post etch and post ash residue removal chemicals in combination with various metals in use today and the subsequent DIW rinse corrosion.

Metal Corrosion in BEOL Wet Processes

There are two primary modes of corrosion which occur during the post etch and post ash wet chemical cleaning processes on BEOL wafers. These are: 1) corrosion in the process chemistry and 2) corrosion during the subsequent DIW rinse. Although process chemistry corrosion can occur through similar mechanisms to rinse corrosion, it can usually be prevented through process development including, material considerations, and proper selection of residue removal chemistry.

Rinse corrosion is theorized to occur through one of numerous mechanisms under study. These mechanisms include: 1) Galvanic corrosion where two or more dissimilar metals are immersed in an electrolyte. Ultrapure DIW is a poor conductor of electrons, however when a small amount of process chemical is carried into the rinse bath, this carry-over may act as an electrolyte and promote corrosion between dissimilar metals. 2) Direct dissolution where the metal dissolves in the rinse water directly. The possibility of this type of corrosion is very small considering optimized rinse times and the materials typically used in the IC manufacturing process. 3) Latent corrosion can occur when plasma etch residues containing such organometallics as R-AlxCly react with atmospheric moisture or rinse bath water to release Cl- and form a corrosive species such as HCl {3,4}. This corrosion may be particularly pronounced when the metal dissolves in the presence of this species as in the case of aluminum. 4) Concentration cell corrosion occurs when a large difference in pH exists. This condition is likely in BEOL rinse baths where DIW exists near neutral pH and the process chemical carried into the rinse bath on the wafer surface may differ by as much as four or five pH units. 5) There exists the possibility of a chemical reaction between the process chemistry components and the DIW in the rinse bath. One example involves the amino- groups found in many process chemistries. This hydration, when combined in DIW rinse, forms an abundance of hydroxyl ions (Equation 1). These hydroxyl ions can promote oxidation of exposed metal on the wafer as suggested by Equation 2.

$R\text{-}NH_2(amine) + H_2O \leftrightarrow R\text{-}NH_3^+ + OH^-$	Hydrolyzed amine	Eq. (1)
where R is an organic		
$M^{+n} + nOH^- \leftrightarrow M(OH)_n$	Oxide formation	Eq. (2)
where M is a metal		

Current and Proposed Methods to Reduce Rinse Corrosion

It is apparent from earlier studies that the combination of process chemical in rinse baths can have a corrosive effect on metals {5,6,7}. These studies indicate that intermediate

rinses or additives to DIW rinse baths reduce or prevent rinse corrosion from occurring. Suggested approaches to reduce rinse corrosion include the use of intermediate, proprietary post strip rinses (PSR) or isopropyl alcohol (IPA) {7} between the process chemical and the DIW rinse.
Although these methods have shown to be effective in some cases, they add expense to the manufacturing process through direct cost, additional footprint of tools, throughput, safety and disposal concerns. Some researchers maintain the use of carbon dioxide gas bubbled into the rinse water is also {8} beneficial in the effort to reduce rinse corrosion. This technique has been in use for many years, but has not fully eliminated rinse bath corrosion issues. Other researchers suggest the addition of acids, such as HNO_3 in the rinse water {9} however the nitric acid must be maintained at very dilute concentrations and can only be used with appropriate metals. The IPA and PSR strategies may reduce corrosion through dilution of the corrosive substance and latent corrosion species or acting as a reduced source of hydroxyl ions (Equation 1). The nitric and carbon dioxide methods initially appear to simply balance the pH of the rinse and reduce concentration cell corrosion through simple acid base neutralization. With the industry drive toward copper metalization{10}, the potential dissolution of copper in nitric may outweigh the benefits; suggesting that other corrosion inhibitors should be investigated. This study focuses on rinse bath additives and an automated means to deliver them to rinse baths. A selection of organic and inorganic corrosion that are compatible with a variety of metals that may be used in IC manufacturing was also studied.

Delivery of Rinse Bath Additives

As part this study, a hardware solution to deliver corrosion inhibitors to rinse baths was developed. This hardware was designed to inject anti-corrosion chemical compounds into the DIW rinse during the initial phase of the rinse cycle. After a well defined time, T_0, the rinse is then transitioned to pure DI. In this manner, use of corrosion inhibitors selected for a given process may be optimized to minimize corrosion. The final rinse in pure DIW ensures that any inhibitor or by-product will be carried away from the wafer.

EXPERIMENTAL PROCEDURES:

Methods of Inducing Corrosion and Corrosion Measurement

Corrosion of metals is difficult to measure and the analysis of the rate of corrosion often relies on assumptions such as resistivity changes due to film thickness loss. Further complicating the measurement of corrosion are the large variations in concentrations of process chemicals and materials exposed to the affects of a corrosive environment. In an effort to most closely simulate process conditions, corrosion procedures in this study primarily consisted of two categories; 1) Rinse Bath Immersion and 2) Electrochemical Polarization. As the name implies, Rinse Bath Immersion simulates the actual process conditions with the exception of possibly greater immersion times to assure film loss above detection limits. Electrochemical Polarization is used to induce and measure

corrosion "in-situ". Rather than simulate a bath condition over extended periods of time, this electrochemical method accelerates corrosion through an applied potential.

1. Rinse Bath Immersion Testing.

This method involved immersion of samples for typical process times and slightly prolonged rinse times to ensure corrosion within detection limits. Metal samples were transferred from the process chemistry to either pure DIW rinse or to a DIW rinse + inhibitor which was then transitioned to a pure DIW rinse. Testing of all Rinse Bath Immersion samples consisted of four point probe analysis of blanket films, parametric probe electrical testing of serpentine structures, and FE-SEM imaging for visual confirmation.

Based on encouraging results from the study of blanket aluminum films, serpentine structures were fabricated and processed for 10 minutes then transferred to one of the described rinse baths for more typical rinse times as shown in Table I.

Table I – Aluminum Serpentine Rinse Conditions

Test	Corrosion inhibitor rinse contact time	DI water rinse time[a]
1 (control)	None	None
2	No inhibitor, straight to DIW with carry-over	10 minutes
3	Acetic acid (0.08M), 3 minutes	7 minutes
4	Nitric acid (0.10M), 3 minutes	7 minutes
5	IPA (neat), 3 minutes	7 minutes
6	CO_2 bubbled in DIW, 10 minutes[b]	
7	No inhibitor, straight to DIW with carry-over	5 minutes
8	Acetic acid (0.08M), 2.5 minutes	2.5 minutes
9	Nitric acid (0.10M), 2.5 minutes	2.5 minutes
10	IPA (neat), 2.5 minutes	2.5 minutes
11	CO_2 bubbled in DIW, 5 minutes[b]	

a) Two total rinse times were selected to test potential variations. b) Rinsed entirely with CO_2 sparge.

2. Electrochemical Polarization Testing

This technique is based on previous studies{5,6} and allows the use of pure process chemistry, dilute (2.5ppth) process chemistry, and process chemistry with added corrosion inhibitors. The 2.5ppth concentrations of process chemicals are used to simulate the carryover of process chemistry into the rinse bath as established previously{5,6,11}. The test matrix of material combinations is presented in Table II.

Table II – Electrochemical Test Matrix

Process Chemical (all at 2.5ppth)	Inhibitors Tested[a]
ACSI ST-250 Copper Film	BTA, DDA, CorFree
ACSI ST-250 Copper Film	No Inhibitor simulating normal rinse conditions
Ashland NP 970 Copper Film	BTA, DDA, CorFree, IPA, Nitric, Acetic, CO_2
Ashland NP 970 Copper Film	No Inhibitor simulating normal rinse conditions
EKC 640 Copper Film	BTA, DDA, CorFree
EKC 640 Copper Film	No Inhibitor simulating normal rinse conditions

a) BTA (benzotrizole) ~4mM, DDA (dodecanedioic acid) ~1.2mM, CorFree-DuPont ~0.4mM

The BTA, DDA, and CorFree were included in the 2.5ppth process chemical calculations and tested at ~4.0mM, ~1.2mM, and 0.4mM respectively.

It should be noted that the selection of the corrosion measurement method used for a particular sample depended upon the conditions under which the measurements needed to be acquired. No single method provided adequate results in all chemicals or under all conditions. When appropriate, FE-SEM images were used to assist in verifying test results.

Experimental Instrumentation, Corrosion Inhibitors and Process Chemicals

Blanket film corrosion testing involved four-point probe analysis using a Veeco Four Point Probe. Serpentine test structures were probed using an Alessi Probe Station and a Hewlett Packard 4155 Parameter Analyzer. The electrochemical polarization experiments utilized an EG&G Potentiostat with customized flat-cell and SoftCorr III corrosion software.

Rinse bath corrosion inhibitors were selected based on literature references, previous experimentation, and material considerations. The organic and inorganic inhibitors consisted of nitric acid, acetic acid, carbon dioxide, dodecanedioic acid (DDA), benzotriazole (BTA), and CorFree-DuPont.

The post ash and post etch residue removal chemistries were selected based on previous experiments and recommendations by the manufacturers. Ashland ACT 937 was selected specifically for traditional IC materials (TiN and Al/Cu alloy) while ACSI ST-250, Ashland ACT 970, and EKC 640 were used for copper films.

Metals were tested as deposited on silicon wafers and consisted of:
- Blanket aluminum alloy (0.5%Cu) sputtered to 7500Å on XYZ
- Blanket copper electrochemically deposited to 15000Å on copper seed and tantalum barrier
- Blanket titanium nitride barrier chemically vapor deposited to 1800Å on XYZ
- Serpentine test structure consisted of TiN/Al alloy/TiN layers with 0.35 μm linewidths

Automated Corrosion Inhibitor Delivery Test-bed

The fully automated chemical injection system was designed to inject and control the concentration of the anti-corrosive chemicals in the rinse tank during a set time, T_0. Closed loop control using conductivity and the ability to change concentration set-points between rinses are additional features of the test-bed hardware. Other concentration monitoring systems (such as IR or UV spectrometers) may also be used depending on the type of inhibitor being delivered to the rinse bath. The three primary components of this delivery system include: 1) Metering pump, 2) Concentration monitoring, 3) Feedback control. The concentrated corrosion inhibitor is pre-mixed with DI water (if necessary) and is maintained at a precise concentration ratio in a recirculation loop prior to injection into the rinse tank. This concentration ratio is continually monitored using conductivity and injected into the rinse tank during the time, T_0. Following this time, the system

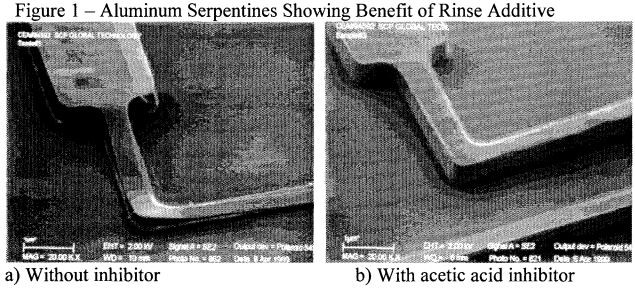
switches to a pure DI highflow for the remainder of the rinsing period to flush any potential by-products or contaminants.

RESULTS AND DISCUSSION:

1) Rinse Bath Immersion Results

The study of blanket aluminum using nitric acid, acetic acid and CO_2 rinse corrosion inhibitors and IPA as an intermediate rinse{5,6} was extended to aluminum serpentine test structures. The results showed that the DIW with carryover corroded the aluminum at an significant rate. This is similar to the blanket film results where virtually no aluminum remained (Figure 1).

Figure 1 – Aluminum Serpentines Showing Benefit of Rinse Additive



a) Without inhibitor b) With acetic acid inhibitor

Two rinse times (five and ten minutes) show magnitudes of difference in the resulting resistivities of the test structure (Table III). These results strongly suggest that process development to optimize rinse conditions can be crucial to avoid excessive rinse bath corrosion.

Table III – Aluminum/TiN Serpentine Probe Station Test Results

Condition	5-min. rinse time	10-min rinse time
Control	NO RINSE	68 kohm NO RINSE CONTROL SAMPLE
DI only with Carryover	**163 kohm**	**96567 kohm**
Acetic Acid	73 kohm	75 kohm
Nitric Acid	73 kohm	67 kohm
IPA	67 kohm	71 kohm
CO_2	70 kohm	68 kohm

2) Electrochemical Polarization Testing Results

The electrochemical results for copper are summarized in Table IV below. Corrosion rates obtained by electrochemical means are not absolute, but offer an excellent method to compare relative rates under similar conditions. It is significant to note the lack of effect pH has on the corrosion rates in Table IV. It has been demonstrated that pH has a significant effect on corrosion rates{12} however, Table IV illustrates variations in corrosion rates with little pH change when these organic inhibitors are used. Although pH and concentration of corrosive species have an impact on corrosion, it is apparent that simply neutralizing the rinse bath to pH 7 by adding the appropriate amount of acid (or

base) is not necessary as previously thought. Through the use of appropriate inhibitors, the pH of the rinse bath is of little concern and can remain close to the original process chemistry and still reduce the corrosion rate in the rinse. It is evident from Table IV that rinse corrosion of copper can be mitigated with the appropriate selection of rinse bath inhibitor.

Table IV – Copper Corrosion Rates using Inhibitors.

Condition	pH	Å/min
ST-250, 2.5ppth (no inhibitor)	8.0	12.
ST-250, BTA	7.8	<0.1
ST-250, DDA	7.9	3.
ST-250, CorFree	7.9	1.
EKC 640, 2.5ppth (no inhibitor)	6.5	0.4
EKC 640, BTA	6.3	<0.1
EKC 640, DDA	7.1	6.
EKC 640, CorFree	4.1	0.3
ACT 970, 2.5ppth (no inhibitor)	11.3	0.2
ACT 970, BTA	10.6	<0.1
ACT 970, DDA	10.7	0.2
ACT 970, CorFree	10.9	0.2

Automated Corrosion Inhibitor Delivery System

Results from a prototype system using nitric acid injection demonstrate that the system allows for precise dilution and control of the nitric acid from 70wt% to 0.007wt% with a +/- 10uS/cm control. This system provides efficient, programmable concentration control for delivery of corrosion inhibitors to the rinse bath.

Concentration control was obtained in this demonstration using conductivity monitoring, although UV-Vis, IR, and other methods are under consideration. Selection of concentration control methods should be based on the type of corrosion inhibitor, the concentrations desired, accuracy of the concentration level, and speed of the required control response. The ability to control concentrations and deliver those concentrations to a rinse bath allows for the introduction of this corrosion control technique to wet bench cleaning and rinsing systems. Elimination of the typical IPA intermediate rinse for corrosion control reduces footprint size, cost of ownership, flammability and safety hazards.

CONCLUSION:

This paper describes a form of corrosion that is known to occur on metal features during the rinse process after cleaning post ash and post etch residues from IC features. The interaction between the metal features, carry-over process chemical and ultra-pure rinse water can result in significant corrosion. Through electrochemical and rinse emulation studies, a method involving the addition of corrosion inhibitors to the DIW rinse bath has been demonstrated to reduce rinse bath corrosion dramatically. Acetic acid and benzotriazole have been shown to offer excellent rinse corrosion protection copper when used as additives to the traditional DIW rinse. Other inhibitors may be selected based upon the process chemical and specific IC features. A compact, automated delivery

system has been developed to deliver corrosion inhibitors to the rinse bath. The process concentration control of this system has demonstrated.
With the multitude of materials used in IC manufacturing today, the chemical systems involved in the corrosion of exposed metals on the wafer surface are no doubt very complex. Careful process development considering material, process chemical, and rinse conditions can prevent significant corrosive effects of traditional DIW rinses.

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YIELD ENHANCEMENT BY CRYOKINETIC CLEANING

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ABSTRACT

CryoKinetic cleaning is accomplished with inert gases, so it is safe to use anywhere in the IC manufacturing line. CryoKinetic cleaning is particularly suitable for cleaning wafer surfaces during the metallization and interconnect processes. The effectiveness of this cleaning technique has been demonstrated by reduction of measured in-line defectivity levels as well as by increase of electrical test yield and final chip yield. Recently, the CryoKinetic cleaning technique has been implemented in production after the via patterning process to improve normalized final yields by more than 5%. Also, effective cleaning with this technique has been demonstrated in the removal of aluminum oxide particles from wafer surfaces with metal patterns and in the removal of silicon oxide particles from patterned oxide on tungsten silicide surfaces. In addition, wafers have been effectively cleaned from very high levels of contamination such as that experienced when a silicon wafer breaks in a transport box or load lock.

INTRODUCTION

The increasing number of metallization levels and decreasing critical dimensions are making IC yields sensitive to ever-smaller particles. Yield losses due to defects at each metallization level multiply as the number of levels increase, making it important to identify and eliminate the defects causing yield loss.

To achieve minimum dimensions during interconnect and metallization processes, it is necessary to use plasma chemistries that cause sidewall polymerization which must be removed before the next level of metallization is deposited. The specialty chemistries commonly used for this purpose are effective at attacking and removing the sidewall residues, but are often less effective at carrying those residues away from the wafer surface. Chemicals normally used for particle removal during transistor fabrication are not applicable at this stage, because of exposed metal and the use of spin-on dielectrics in the dielectric stack.

Argon/nitrogen cryogenic aerosol cleaning, known as CryoKinetic cleaning, has been successfully implemented to remove defects commonly remaining on the wafer surface after via processing. CryoKinetic cleaning was evaluated with other cleaning techniques for use at the via level in a 0.25-μm production line and was found to be the

most effective at removing the defects and improving final wafer yield (1). Also, effective cleaning with this technique has been demonstrated in the removal of aluminum oxide particles from wafer surfaces with metal patterns and in the removal of silicon oxide particles from tungsten silicide surfaces with patterned oxide. CryoKinetic cleaning is particularly suitable for cleaning wafer surfaces during the metallization and interconnect processes since it is accomplished with inert gases which makes it safe to use anywhere in the IC manufacturing line. This technique has been studied extensively and has been shown to be nondamaging and noncharging to the wafer surface (2).

Another important yield issue in IC manufacturing is process yield. Sometimes, particular wafers or wafer lots are scrapped during processing because defect levels have become so high as to make it not economical to continue processing (i.e. projected final yield does not justify the added cost of finishing the wafers). Often, these wafers are scrapped because standard cleaning processes are not compatible with the wafers at that point in the manufacturing sequence. CryoKinetic cleaning provides a method to safely clean wafers at any point in the manufacturing sequence so that wafers or lots do not need to be scrapped, thus improving process yield. For example, high levels of silicon particle contamination caused by wafer breakage in a transport box or in a load lock have been effectively removed with CryoKinetic cleaning.

CRYOKINETIC CLEANING

CryoKinetic cleaning was introduced to IC wafer manufacturers in 1996. In CryoKinetic cleaning, the wafer surface is cleaned by an aerosol of microscopic argon/nitrogen ice crystals in a nonchemical, nondamaging process (2,3). A mixture of argon and nitrogen gases at approximately 70 psi is cooled to form a liquid/gas mixture. This mixture flows into a tube and is injected through tiny holes into the vacuum chamber. The flow is directed toward the wafer surface. As the liquid/gas mixture is injected into the vacuum chamber, the liquid portion expands and breaks up into small fragments. The small fragments undergo evaporative cooling, which causes them to freeze into solid crystals. These crystals range from less than 0.5 μm to more than 5 μm and can attain velocities of up to 100 m/s.

Contaminants are dislodged from the wafer surface mainly through momentum transfer from the ice crystal to the contaminant particle. Once dislodged, the contaminant particle is carried away from the surface of the wafer by thermophoretic and convective forces and is swept out of the cleaning chamber by a carefully engineered laminar flow field (4,5). The ice crystals simply undergo sublimation back to gas-phase argon and nitrogen in the exhaust.

YIELD ENHANCEMENT AFTER VIA PATTERNING

The via-patterning process sequence (resist patterning, plasma etching, resist ashing, and post ash solvent cleaning) often leaves defects on the surface of the interlevel dielectric. These defects can be composed of oxide or aluminum, as shown in Figure 1, and probably result from the various sidewall residues that are deposited during plasma etching of the via pattern (1). These types of defects affect the subsequent metal deposition and patterning sequence and can lead to electrical shorts and opens depending on where the defect falls in the metallization pattern. CryoKinetic cleaning was used to remove these defects after via patterning and before liner deposition and resulted in a reduction of defect levels and an increase in electrical and final test yield.

The CryoKinetic process was initially evaluated on several product lots that were split between standard processing and CryoKinetic processing. A 3-level metal product and a 5-level metal product were split at each metal level. Half of each lot saw the baseline via-patterning process for all via levels, and the other half of each lot saw the baseline via-patterning process with CryoKinetic cleaning for all via levels. A total of three lots were split for each product. Figure 2 shows a comparison of surface defect levels (approximate resolution of 0.2 μm) with and without CryoKinetic cleaning, both before and after the third-level via-etch process (1). Each defect map is the sum of all 36 wafers from the three split lots to better illustrate the defect reduction. On average, about 26 defects are detected on each wafer before the third-level via-etch process. After the baseline process, an average of about 29 defects are found on each wafer. After the baseline process plus CryoKinetic cleaning only 7.8 defects remain on avarage – a decrease of 69%. Clearly, the solvent cleaning process is unable to remove these surface defects, while the CryoKinetic cleaning process is much more effective. Some of the defects not removed by the CryoKinetic process are actually embedded in the dielectric layer, the results of defect formation during the deposition process.

A comparison of the normalized yield for each split lot is shown in Figure 3 (1). On average, the 3-level metal product saw a normalized yield improvement of over 6% while the 5-level metal product saw a normalized yield improvement of over 30%. The main driver for this yield improvement is a reduction in the defects in the subsequent metallization layer. Figure 4 shows the electrically measured defect density for each of the three lots in Figure 3(b). An average reduction of 0.015 defects/cm^2 was measured on these three split lots. This indicates that removal of defects reduced the occurrence of electrical shorts and opens in the metal layer that was deposited over.

After implementing the CryoKinetic tool in the production line, the reduction in defect density was clearly seen. Figure 5 shows the trend chart for defect density levels measured after the second- level via-patterning process. Clearly, the CryoKinetic cleaning process is effective at eliminating the occasional out-of-control defect levels as well as reducing the overall baseline defects level.

DEFECT REDUCTION ON VARIOUS SURFACES

The effectiveness of the CryoKinetic technique has also been demonstrated on metal patterned surfaces and on oxide patterned tungsten silicide surfaces. Similar to the via patterning process described above, wafers went through a metal-patterning process sequence (resist patterning, plasma etching, resist ashing, and post ash solvent cleaning) and were found to have high levels of defects remaining on the surface. Typical defects were found to consist mainly of aluminum oxide. CryoKinetic cleaning was able to reduce the total measured defect level on a sample patterned wafer from 2600 to 1200. The final defect level includes patterned and embedded (non-cleanable) defects.

Figure 6 shows the results of using CryoKinetic cleaning to remove oxide particles from an oxide patterned tungsten silicide surface. In this case, an oxide hard mask was patterned over tungsten silicide and then the photoresist was ashed from the oxide pattern. Figure 6(a) shows the large number of oxide defects left on the surface following the resist ashing process. After CryoKinetic cleaning, the defect level on this patterned wafer was reduced by 99% as shown in Figure 6(b).

DEFECT REDUCTION AFTER BROKEN WAFER CONTAMINATION

Occasionally during manufacturing a silicon wafer will break. Certainly, the impact for that particular wafer is catastrophic as the wafer can not be recovered and must be scrapped. However, the impact of that wafer breakage can be far more harmful depending on its proximity to other wafers when the breakage occurs. If the breakage occurs while the wafer is in a cassette with other wafers - in a loading station, a load lock, or a box - then all the other wafers are contaminated with very large numbers of silicon particles. If these silicon particles can not be removed, then the entire cassette of wafers must be scrapped. Depending on the type of product and how far along in manufacturing the breakage occurs, this can represent up to several hundred thousand dollars of lost revenue. Even if this occurs only once per month, it can have a tremendous impact on the profitability of an IC manufacturing line.

CryoKinetic cleaning is effective at removing these silicon particles. Figure 7(c) is an optical microscope image of a typical defect that was easily found on a metal patterned wafer that was exposed to a broken wafer. The wafer map shown in Figure 7(a) indicates over 4000 defects on the wafer surface before cleaning. Figure 7(b) shows that after CryoKinetic cleaning only 13 defects remain – a reduction of over 99%. Analysis of this data indicates that the number of defective die on this wafer was reduced from 88% to 2.4% .

SUMMARY

CryoKinetic cleaning is an effective technique for reducing defects and increasing product yields at virtually any point in the IC manufacturing process without risk of damage or chemical attack. The use of CryoKinetic cleaning has been shown to improve final test yields in production when implemented after the via patterning process. It has been shown to reduce defect levels after metal patterning and after oxide patterning on tungsten silicide. Also, wafer loss after exposure to broken wafer debris can be very costly. We have shown how CryoKinetic cleaning can be used to recover those wafers very easily, potentially saving IC manufacturers millions of dollars per year.

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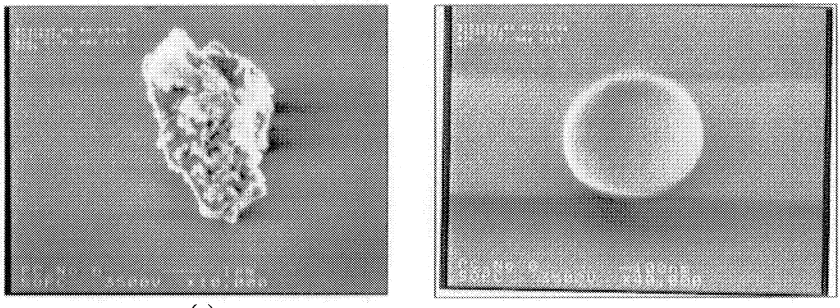

(a) (b)

Figure 1. Typical defects remaining on the wafer surface after via patterning were composed of (a) silicon dioxide or (b) aluminum. [Reference (1)]

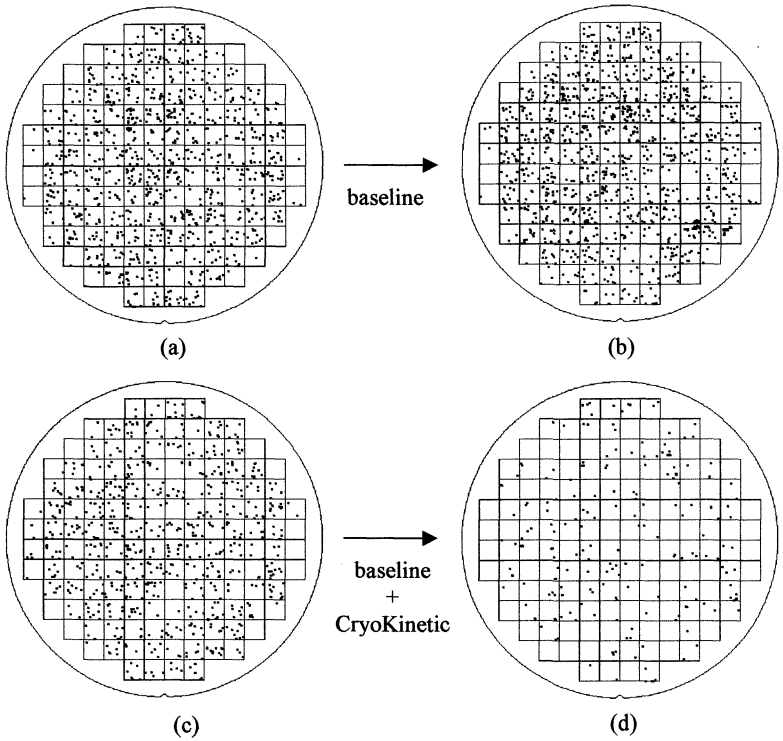

Figure 2. Defect maps from via-patterning split lots. Each map represents the sum of 36 wafers. Maps (a) and (b) show defect levels before and after third-level via etch baseline process. Maps (c) and (d) show defect levels before and after third-level via etch baseline process with the addition of CryoKinetic cleaning. [Reference (1)]

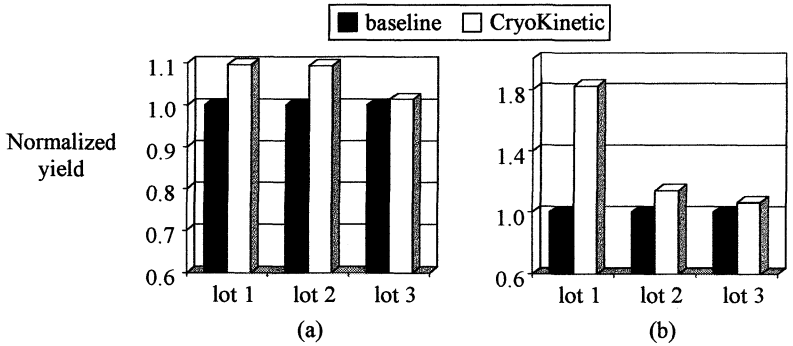

Figure 3. Split lot results showing normalized yield improvements for three split lots with (a) a 3-level metallization process and (b) a 5-level metallization process. [Reference (1)]

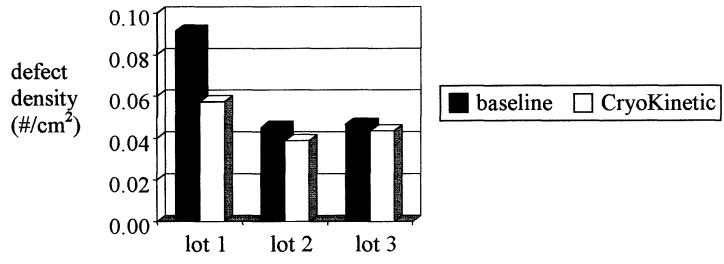

Figure 4. Electrical defect density at final test for 5-level metallization split lot. An average reduction of 0.015 defects/cm^2 was achieved with CryoKinetic cleaning. [Reference (1)]

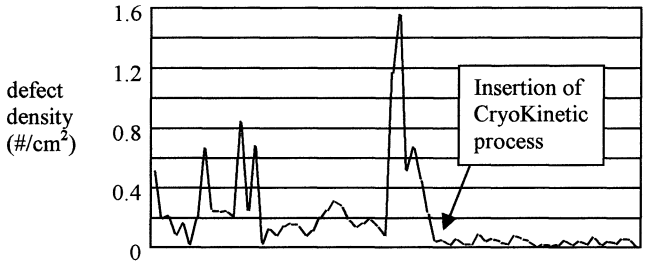

Figure 5. Trend chart showing the significant reduction of in-line TiN barrier defect density (#/cm^2) at the second via level after insertion of the CryoKinetic process into the production line. [Reference (1)]

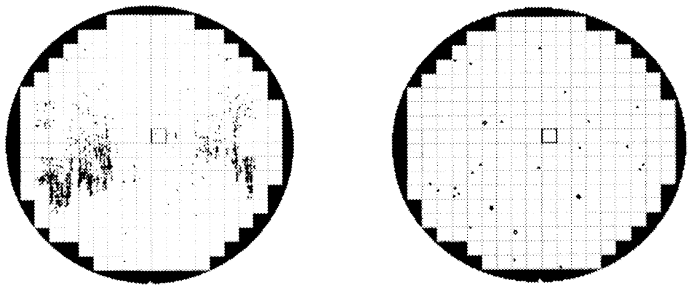

Figure 6. Removal of oxide defects from an oxide patterned tungsten silicide surface.
(a) Following oxide etch and photoresist ash, this wafer had 3090 defects.
(b) Cryokinetic cleaning reduced the defect level by over 99% to 26.
[Source: Wafertech]

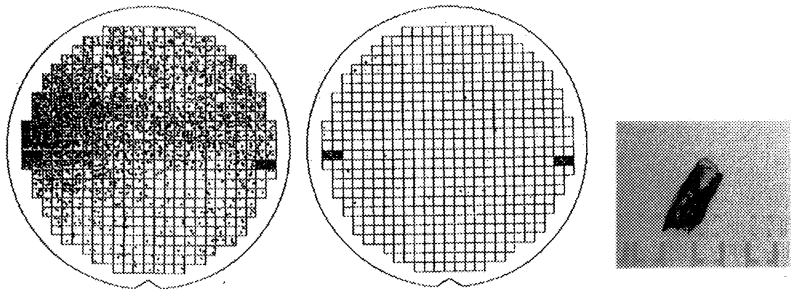

Figure 7. Removal of broken wafer debris from a metal patterned wafer. (a) The wafer initially had 4284 defects. (b) Cryokinetic cleaning reduced the defect level by over 99% to 13. (c) Typical silicon defect at 10X optical magnification (~2mm in size)

A NOVEL WAFER BACKSIDE SPIN-PROCESS CONTAMINATION ELIMINATION TECHNIQUE FOR COPPER PRODUCTION APPLICATIONS

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Interconnect delay begins to dominate overall device delay at 180 nm, making low resistivity copper highly desirable. Copper migrates very quickly in silicon; therefore, successful integration requires stringent control of copper cross-contamination from deposition equipment, electroplating tools, chemical-mechanical polishing (CMP) equipment, and all metrology tools shared by copper processed wafers. In this paper, data illustrating a highly effective means of eliminating copper from the wafer backside, bevel/edge, and frontside edge exclusion zone (0.5 mm – 3 mm), is presented. The data, obtained within the framework of standard and experimental copper/low-k device production at SEMATECH, quantifies the benefits of implementing the SEZ spin-process contamination elimination (SpCE) clean operation. Furthermore, this data confirms the feasibility of utilizing existing (non-copper) process equipment in conjunction with the development of copper applications by verifying the reliability and cost effectiveness of SpCE functionality.

INTRODUCTION

The transition from aluminum to copper contacts and from oxide to low-k (dielectric constant) interconnect materials indicates a fundamental change in back-end processing to dual-damascene (1). Low-k dielectrics not only improve speed through lower (resistance X capacitance) RC delay but also reduce cross-talk noise and alleviate power dissipation concerns (2). While new materials are being investigated as potential replacements for thermal silicon dioxide (SiO_2, k = 3.9) to reduce the capacitance component of RC interconnect delays, copper (Cu) is rapidly replacing aluminum as the main on-chip conductor. There are two main segments of the cost equation: interconnect layer and stack costs. A copper interconnect layer costs 20 percent less than a comparable aluminum one and a more dramatic cost reduction will be realized when designing and building copper devices requiring fewer layers than the aluminum counterpart (3). Copper is second only to silver for low resistance (< 2 μΩ-cm even when deposited in narrow trenches vs. > 3 μΩ-cm for aluminum alloys) and copper exhibits high resistance to electromigration along grain boundaries, enabling faster response and higher power density capability (4). However, copper is a fast diffuser with intrinsic diffusivity D_0 in silicon of 4 x 10^{-2} cm^2/s with activation energy, E_A = 1.0 eV (4). Migrating copper can "poison" a device, causing failure once it propagates into the active area (i.e., source/drain/gate region) of the transistor (5).

As semiconductor production facilities transition into the copper age, serious contamination monitoring and control procedures must be rigorously implemented. Noble metal contaminants such as Cu often prove to be the leading cause of device degradation (6, 7, 8, 9). At SEMATECH, not having a dedicated set of copper tools increased cycle time due to copper lots processing only one day per week through non-copper tools. Even if manufacturing facilities possess a dedicated Cu tool set, post copper tool cleaning and monitoring by total reflection X-ray fluorescence spectroscopy (TXRF) and vapor phase decomposition inductively coupled plasma mass spectrometry (VPD-ICP-MS) add to production cost. The solution is realized by implementing the SEZ Spin Processor 203® with its novel, single wafer, back surface spin-process contamination elimination (S_pCE) functionality. The capability of processing patterned wafers directly from copper tools and certifying processed lots as "Copper Free" for subsequent processing in non-copper tools provides immediate reductions in cycle time and monitor analysis costs. The tool features a clever sequence of picking wafers from a (potentially) Cu contaminated lot/cassette, loading in and out of the process chamber with edge contact only (ECO) grippers, and placing (with a clean end effector) into a clean cassette. This establishes the point of isolation in the fab and minimizes the risk of sharply reducing the frequency of contamination monitoring by TXRF and VPD-ICP-MS.

Spin-Process Contamination Elimination

S_pCE is a proprietary technology of the SEZ Group, and is being enhanced through testing and optimization efforts at SEMATECH. This process utilizes a liquid chemical solution dispensed on the surface of a spinning wafer to remove copper contamination from the wafer backside and bevel/edge. Additionally, the process may be applied to remove thermal oxide or nitride films on the wafer backside and controlled to perform a precision wraparound film removal etch (edge exclusion zone) on the frontside of the wafer. Typically, Cu particles are imbedded within the oxide and are effectively eliminated by removing approximately 200Å SiO_2 with a chemical blend that includes hydrofluoric acid (HF).

The wafer is suspended, device side down, above the process chuck on a nitrogen cushion (utilizing the Bernoulli principle) and is restrained on the chuck with locating pins at the wafer perimeter. The wafer is rotated with the chuck while the etch solution is dispensed from a radial oscillating overhead nozzle. The continuous fresh supply of chemical medium, utilizing a custom dispense pattern, is designed to generate a uniform etch-rate over the wafer surface and has been optimized to reduce stress-induced bow and warp associated with several experimental Cu/low-k products (10, 11). Solutions are recipe-selected from three local chemistry cabinets and may be routed to drain or re-circulated as indicated in figure 1. Controlling the simultaneous radial and tangential etchant flow along with the etchant viscosity and composition enables contamination, particles, and film removal from the back, bevel/edge, and front exclusion zone of the wafer without risk of damage to device structures.

EXPERIMENTAL SETUP

SEMATECH provides a combination of custom copper processing services including standard baseline material and a considerable number of novel processes, as well as

Figure 1. Spin Etch Technology Principle of Operation

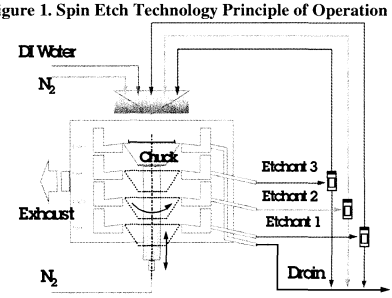


Figure 1. Chemistry / Tool Diagram

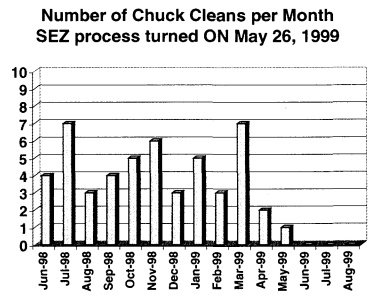


Figure 2. Litho Chuck Cleaning

material and tool development activities. The MicraScan III® deep-ultraviolet (DUV) step-and-scan lithography system has experienced reduced wafer throughput and stepper up-time performance due to a wide variety of incoming wafer quality issues. An incoming wafer back surface visual (pre-litho) inspection, under broadband "bright light" conditions, has been implemented. Table I illustrates the severity of the wafer quality problem prior to the introduction of the SEZ S_pCE process and the immediate and complete improvement in quality due to the S_pCE process.

Table I. Wafer Quality Results at Pre-Litho Inspection, with and without SEZ S_pCE

	Total Lots	# Failed	% Failed	# Passed	% Passed
Without SEZ	80	43	54	37	46
With SEZ	137	0	0	137	100

Frequency and duration of tool down-time, associated with chuck cleaning related to particle deposits and Cu contamination transferred from the back surface of wafers being processed has been at unacceptable levels. Figure 2 represents the beneficial impact of the introduction of the S_pCE process (May 26) regarding chuck cleaning frequency (- the MicraScan III experienced down time and processed fewer than average lots in August).

Copper Contamination Control

The National Technology Roadmap for Semiconductors (NTRS) has established target levels for critical and other surface metals. Critical metals include Cu which needs to be < 2.5×10^{10} atoms cm^{-2} for 250 nm device technology; < 1.3×10^{10} atoms cm^{-2} and < 1×10^{10} atoms cm^{-2} for the 180 nm and 150 nm technology nodes, respectively (12). It is common for wafers to require cleaning for a combination of problems such as particles, stress-induced bow and warp, and Cu contamination. Given the range of chemical etch parameter options available, the SpCE process effectively addresses this challenge.

Nitric acid (HNO_3) is an oxyacid and as such, is a strong electrolyte and a powerful oxidizing agent considered 100 percent ionized in aqueous solution (H_2O). The oxidation

number of N in HNO_3 is +5. The most common reduction products of nitric acid are NO_2 (oxidation number of N = +4). NO (oxidation number of N = +2), and NH_4^+ (oxidation number of N = -3) (13). Half reactions yielding common reduction products are:

$$NO_3^-(aq) + e^- + 2H^+(aq) \rightarrow NO_2(g) + H_2O(l) \quad [1]$$

$$NO_3^-(aq) + 3e^- + 4H^+(aq) \rightarrow NO(g) + 2H_2O(l) \quad [2]$$

Reaction equation [1] is predominant when concentrated (70%) HNO_3 reacts with copper:

$$Cu(s) + 4H^+(aq) + 2NO_3^-(aq) \rightarrow Cu_2^+(aq) + 2H_2O(l) + 2NO_2(g) \quad [3]$$

Reaction equation [2] is predominant when copper reacts with a mixture of equal volumes of concentrated HNO_3 and H_2O:

$$3Cu(s) + 8H^+(aq) + 2NO_3^-(aq) \rightarrow 3Cu_2^+(aq) + 4H_2O(l) + 2NO(g) \quad [4]$$

Nitric acid will oxidize most metals to the corresponding cations. Since the stronger oxidizing agent in HNO_3 is the NO_3^- ion (not H^+), the reduction product is NO_2, NO, or NH_4^+, not H_2 (13, 14, 15). Concentrated nitric acid is an extremely rapid etchant of Cu while HF is slow. Solutions of HF:HNO_3 are relatively fast and more controllable than straight HNO_3 with removal rate reduced by increasing the ratio of HF (14). The standard production recipe designed for a combination of incoming wafer issues, including Cu contamination, is sequential HNO_3 / HF (dilute) repeated twice. The process etches ≈ 200Å SiO_2 from the back surface. A wafer with 1kÅ of Cu seed deposition was processed on the front side and analyzed by TXRF. Table II contains the results of that demonstration. Two of three sites on the wafer were below the detection limit for Cu (1.0 $x10^{10}$ atoms cm^{-2}) and the wafer average of 1.6 $x10^{10}$ atoms cm^{-2} is far below the failure threshold of 50 $x10^{10}$ atoms cm^{-2} for Cu at back-end of the line operations.

Table II. TXRF Analysis of 1kÅ Cu Seed Removal by Standard Cu Clean (S_pCE) Recipe. Measurements x 10^{10} atoms/cm^2.

Slot 1	Fe	Ni	Cu	Zn
1	3	7	3	<
2	3	5	<	<
3	<	4	<	<
Lot Avg	2.7	5.2	1.6	1
Std Dev	0.6	1.3	1.1	0

Wraparound Etch Process Results

Failure to remove copper from the exclusion zone may not be detrimental to the device, as diffusion through tantalum nitride (TaN) is minimal below 400°C (16). During CMP processing, however, serious concerns remain for cross-contamination from the copper film to the bevel/edge. The scanning electron microscopy (SEM) tilted cross-section image of figure 3 illustrates the S_pCE wraparound process capability to remove copper film from the wafer frontside and expose the tantalum (Ta) barrier layer from bevel/edge to Cu film, resulting in an exclusion zone of 2.35 mm. The clearly defined line of transition from Cu to Ta is due to chloride crystal formation, on the partially etched copper, produced by a mixture of H_3PO_4:H_2O_2:HCl:H_2O in concentration ratio, (2:3:0.1:5). The amount of undercut may be adjusted from 0.5 mm to 3.0 mm. Particles in the exclusion zone were produced during SEM sample preparation and are not related to chemical processing. Figures 4, 5, and 6 represent different views of the same sample. Figure 4 is a high magnification edge-on cross-section illustrating the 10kÅ thickness of electroplated Cu copper. Figure 5 is an edge-on cross-section representing the resultant transition from 10kÅ electroplated Cu film, etched by H_3PO_4:H_2O_2:H_2O, (1:1:18), to the clean Ta barrier over a horizontal distance of 0.015 mm (15 μm). Figure 6 was obtained by tilting the sample of figure 5 to illustrate the typical line of transition produced and to show that, to the level of the resolution of the SEM, the microroughness of the etched transition slope is quite similar to that of the electroplated Cu film surface.

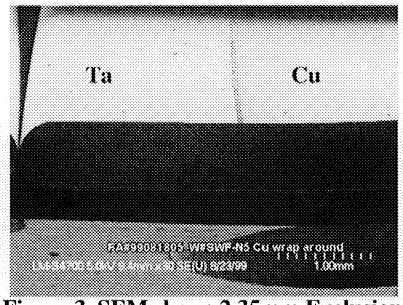


Figure 3. SEM shows 2.35mm Exclusion Region (Cu free) from wraparound etch

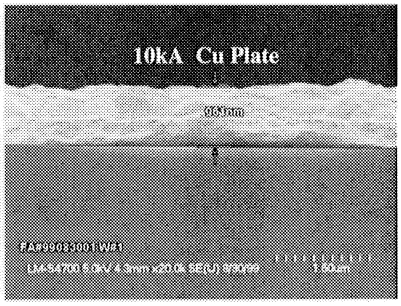


Figure 4. SEM shows 10kA Cu plate

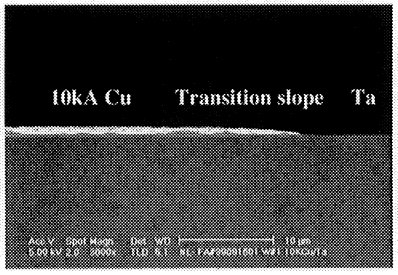


Figure 5. SEM illustrates etch profile from 10kÅ Cu to Ta layer in 15μm (0.015mm)

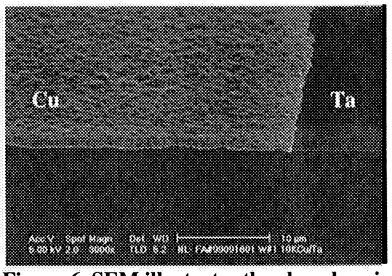
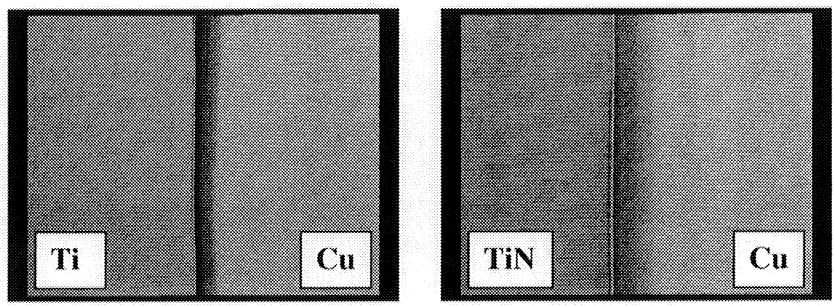


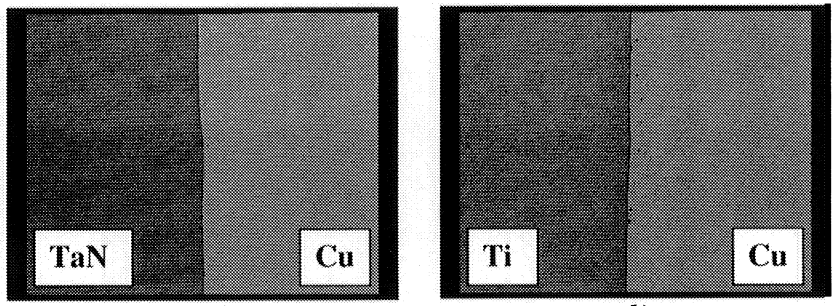
Figure 6. SEM illustrates the clean barrier layer and transition line to 10kÅ Cu plate

Wraparound etch experiments have been performed on wafers with combinations of copper seed and electroplated copper over various barrier layer materials including: Ta, TaN, titanium (Ti), and titanium nitride (TiN). Cu was also deposited directly on bare Si and SiO_2. These experiments were designed to provide a comparative analysis of the effects of various chemical compositions on the extent of the exclusion region produced and the quality of the resultant transition with regard to residue and corrosion. Four chemical mixtures were evaluated: *A*) H_2O_2:HCl:H_2O, (1:4:20), *B*) HNO_3:H_3PO_4:H_2O, (2:1:2), *C*) H_3PO_4:H_2O_2:HCl:H_2O, (2:3:0.1:5), and *D*) H_3PO_4:H_2O_2:H_2O, (2:3:5). Although the relatively high concentration of HCl and HNO_3 present in mixtures *A* and *B*, respectively, causes some irregularity of the etch transition line, the removal of copper is very aggressive; producing up to 5 mm copper free edge exclusion. The effort to completely eliminate corrosion, in the form of chloride crystal formation at the etched Cu transition, continues, along with the investigation to determine the limits of acceptable corrosion levels at the exclusion ring region of the wafer.



a) *b*)

Figure 7. Two microscope images of the Cu seed / barrier layer transition produced by SPCE wraparound processing with (C): H_3PO_4:H_2O_2:HCl:DI, (2:3:0.1:5). *a*) Si/Ox/Ti/Cu (25 X magnification) -Slight corrosion due to HCl at the Cu transition. *b*) Si/TiN/Cu (100 X magnification) -Residual free processed barrier and transition.



a) *b*)

Figure 8. Two microscope images of the Cu seed / barrier layer transition produced by SPCE wraparound processing with (D): H_3PO_4:H_2O_2:DI, (2:3:5). *a*) Si/TaN/Cu (25 X magnification) and *b*) Si/Ox/Ti/Cu seed (100 X magnification) - both samples are free of corrosion.

Chemical solutions *C* and *D* differ by the addition of a slight spike of HCl, to speed the reaction, in chemistry *C*. Figure 7 illustrates the effect of chemical medium *C* for Cu seed etch on Ti and TiN. The sample wafer incorporating Ti as the barrier layer (7 *a*) indicates very slight corrosion at the (Cu edge) transition while the TiN barrier sample, (7 *b*), remains corrosion free. Corrosion of metals is an electrochemical process, composed of anodic (metal oxidation) and cathodic (reduction) reactions occurring on the surface. The rates of the reactions are measured as current densities in units of A m^{-2} (17). On the Cu film, the anodic and cathodic current densities may vary arbitrarily from point to point as long as the total anodic and cathodic currents are equal. This variation is associated with local differences in pH and surface composition (defects). Corrosion can be controlled by slowing down either the anodic or the cathodic reaction, and by controlling the environment seen by the reaction surface. The reaction of chemical mixture *D* is less aggressive than the other solutions tested (particularly *A* and *B*). Without HCl, medium *D* produces the cleanest result as indicated by the smooth and straight transitions of figure 8 *a* (Cu deposited on TaN) and *b* (Cu deposited on Ti). Although a slight bubbling reaction is noticed on the Cu layer near the transition in figure 8 *b*, this may be eliminated by adjusting the N_2 flow rate around the wafer edge where the reaction takes place.

SUMMARY AND CONCLUSION

The SEZ S_PCE process has demonstrated the capability to effectively eliminate copper cross contamination in the dynamic semiconductor research and development environment at SEMATECH. Direct benefits include cycle time reduction (for copper and non-copper products) and reduction of production costs due to the corresponding virtual elimination of TXRF monitoring as copper lots process through non-copper tools. Versatility of the S_PCE operation has resulted in its formal implementation as the standard pre-litho clean process for all products. Aside from the responsibility of providing "Cu Free" status to all interconnect (Cu/low-k) products, this novel process technique eliminates the problematic issue of back surface particles and residue transferring from wafers to the MicraScan III chuck, thereby reducing cleaning frequency and stepper down time.

The introduction of highly porous low-k dielectric materials yields compounds that lack the rigidity common to SiO_2 and stress induced bow and warp from metal layers may become extreme to the point of wafer/vacuum seal failure. The S_PCE process has demonstrated the capability to "return to normal" wafer flatness as measured by whole wafer capacitance. Finally, Cu contamination control is achieved by backside etch processing of a spinning wafer with adjustable edge exclusion of frontside wraparound processing. The S_PCE process enables chemical selection and control appropriate for Cu/barrier material etch transition optimization and the edge exclusion may be adjusted over a linear range of 0.5 mm to 3 mm with corrosion free processing.

ACKNOWLEDGEMENTS

The authors wish to thank Ellwood Smith, Advanced Tool Development Facility (ATDF) Engineering Manager at SEMATECH for supporting this research, and Chris Sparks, SEMATECH Material Analysis Group, for TXRF and VPD-ICP mass analysis.

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SINGLE WAFER CLEANING

SINGLE WAFER POLYMER REMOVAL FOR <0.25μm TECHNOLOGY

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Abstract

In this study, a newly formulated cleaning chemistry was chosen to clean metal wafers using a single wafer spin processor. The current standard condition was selected as the control and the overall processing parameters were separated into 3 different studies which include Solvent Clean, Water Rinse and Dispense Arm Movement

We found the solvent cleaning process is dependent on time and to a lesser extent on spin speed. Movement of dispense arm improves cleaning uniformity. The speed of the arm movement will affect the cleaning of the wafer, and the wafer was cleaned at both high and standard arm movement speed. The water rinse is a critical factor to preventing metal corrosion, the longer time resulted in minimal corrosion, and megasonics had no impact on the metal corrosion. Water consumption is low with only one liter of water being used to clean the wafer. The chemical showed to clean the wafers even with aged solvent in the equipment.

Single wafer post etch residue removal with a unique chemistry has proved to be superior to commonly used systems such as spray tool and wet benches. This is due to shorter process time, precise control of chemistry application, reduced D.I. water with excellent cleaning results using high through put small footprint equipment resulting in low cost of ownership.

INTRODUCTION

The move to shrinking device features according to Moore's law marches onwards; approaching 100 nm features will necessitate new, improved materials and equipment to replace older, well-characterized process tools.

The drive to higher throughput and smaller footprint with lower solvent and water consumption are the main drivers for new improved materials and equipment.

New challenges are to clean sub-micron lines and vias containing plasma residues and polymers at room temperature in short process times and move away from the standard polymer removers which are generally used at 65-85°C for 20 to 30 minutes with an intermediate rinse to minimize corrosion.

EXPERIMENTAL

A single wafer spin processor, and a newly formulated cleaning chemistry was chosen for this study. The current standard condition was selected as the control and the overall processing parameters were separated into 3 different studies which include Solvent Clean, Water Rinse and Dispense Arm Movement. There was no intermediate rinse after the solvent cleaning and the wafers were rinsed for a standard time before being rinsed dry.

RESULT & DISCUSSION

I. Solvent Cleaning Process Study

A body centered factorial DOE was carried out based on spin speed, solvent flow, and time using the new chemistry on a single wafer spin processor to optimize the residue removal process. The metal wafers had a structure of Ti/TiN/AlCu/TiN and were etched using the latest state of the art De-Coupled Plasma source / Transfer Coupled Plasma source etcher in the semiconductor industry.

The conditions for cleaning were

Spin Speed	Control ± A rpm
Flow rate	Control ± B l/min
Time	Control ± C secs

SEM's showing the results can be seen in Figures 1A(a-e) and Figure 1B(a-d), and the result of the statistical analysis was given in Figure 1C. The results of the DOE show that the solvent cleaning process is dependent on time and to a lesser extent on spin speed. All wafers were cleaned after processing at a time above the control using the current testing conditions. For wafer samples cleaned at a time less than the control, higher spin speed seemed to show better cleaning result.

II. Water Rinse Study

The DI water rinse step is critical to ensuring corrosion free, particle free clean wafers. A simple face centered DOE was carried to examine the effects of megasonics and time on the rinsing efficiency.

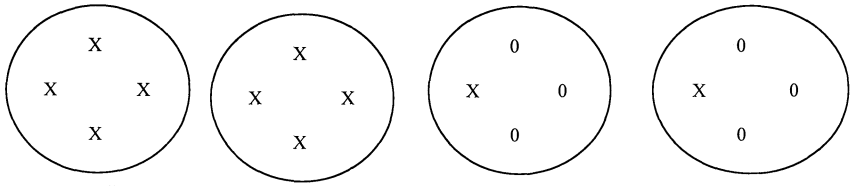
The KLA scan results (wafer map, defect type pareto and pictures) after 24 hr Wet box test did not show any corrosion. Since the KLA scan cannot scan the very edge of the wafer, the edge of the wafers was also inspected to see if there was any metal corrosion.

The conditions for cleaning were:

DI water rinse time: D sec and D+30 seconds
Megasonic: on and off

Below is a schematic showing the areas of corrosion results (4-point inspection)

X - Metal Corrosion
0 - No Metal Corrosion



WID #10 D sec, No Meg | WID #11 D sec, Meg on | WID #12 D+30 sec, No Meg | WID#13 D+30 sec, Meg on

Water rinse time is an important factor to prevent metal corrosion. At D sec rinse, all four edges of wafer have corrosion. Increasing time to D+30 sec rinse, only left edge of wafer has corrosion (1 or 2 points only). Turning megasonics on or off has no impact to preventing or reducing metal corrosion. The water usage is low with approximately one liter of water required to clean the wafers.

III. Dispense Arm Movement Study

In a single wafer spin-processor the remover is dispensed from above and across the rotating wafer by a moving dispense arm. In order to ensure excellent uniformity and process control, the movement and speed of this dispense arm requires to be optimized.

In the first study, the moving range of the dispense arm was set at ±0mm and at ± control. As can be seen in Figure 2(a-b), stationary (zero) movement of dispense arm results in non-uniformity of cleaning across the wafer. The rotational speed of the wafer results in the chemical being spun off before reaching the edge of the wafer. As can be

seen in Figure 2(c-d), when the dispense arm is moving across the wafer at the control range, there is uniform cleaning across the wafer.

In the second study, the range of the arm movement is fixed, and the speed of the arm movement is varied. The condition for study were:

Arm movement speed: control ± F mm/sec.

At the low speed of arm movement there was slight residue remaining on the metal lines Figure 3(a). At an arm moving speed equal to or above the control, all wafers were cleaned as shown in Figure 3(b-c).

In conclusion, dispense arm movement range is important to obtain uniform cleaning across the wafer. To ensure uniform cleaning across the wafer the dispense arm movement speed has to be equal to or above the control speed.

IV. Bath Life Study

Once the process had been completely investigated, a bath life study was carried out over a fixed time frame. Wafers were processed under identical conditions in fresh and used chemical and sent for SEM.

Figure 4(b) showed that the both the fresh chemical and aged chemical was able to clean the wafer in the single wafer spin processing tool.

CONCLUSION

Through this study, a process has been developed to clean metal wafers using a newly developed chemistry on a single wafer spin processor. Processing parameters in the solvent cleaning, DI water rinse, and arm movement steps were optimized, and their effect on the cleaning has been established.

ACKNOWLEDGEMENTS

Mihaela Cernat for all the SEM work, Tammy Alvarez for formatting and Richard Leonard on the lively discussions over the DOE analysis.

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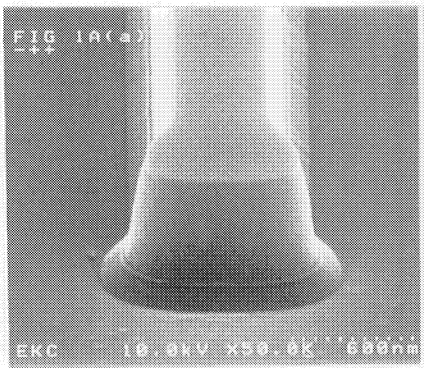


Figure 1A(a)*. Processing condition: -++

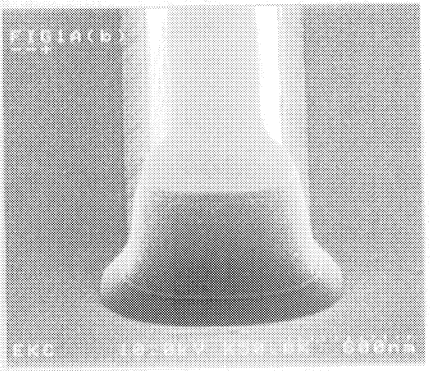


Figure 1A(b)*. Processing condition: --+

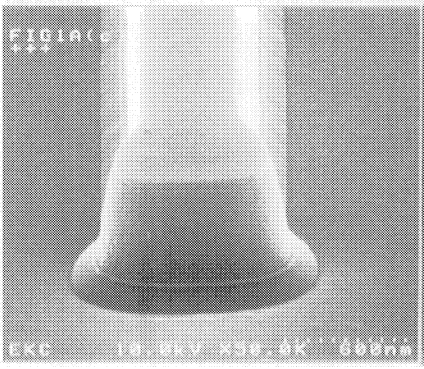


Figure 1A(c). Processing condition*: +++

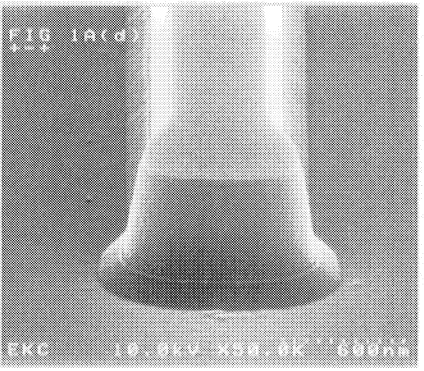


Figure 1A(d). Processing condition*: +-+

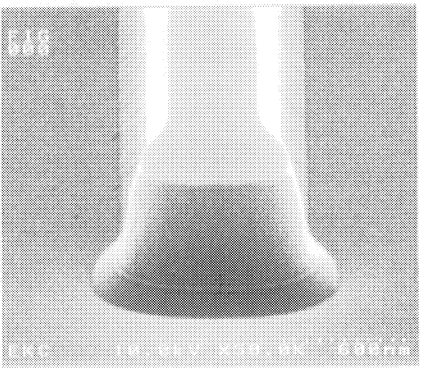


Figure 1A(e). Processing condition*: control (000)

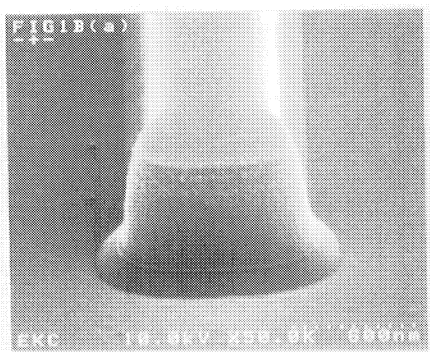


Figure 1B(a). Processing condition*: -+-

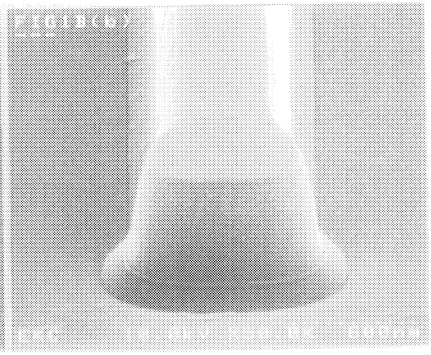


Figure 1B(b). Processing condition*: ---

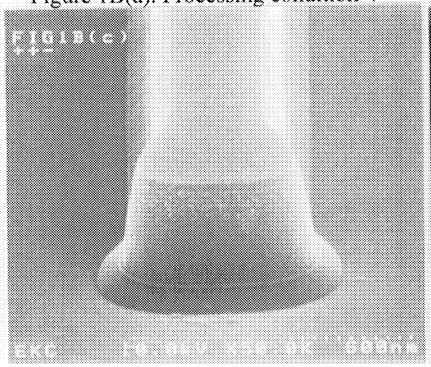


Figure 1B(c). Processing condition*: ++-

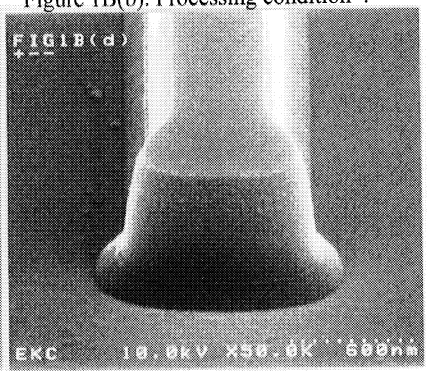


Figure 1B(d). Processing condition*: +--

*: Processing condition = (spin speed, solvent flow rate, cleaning time)

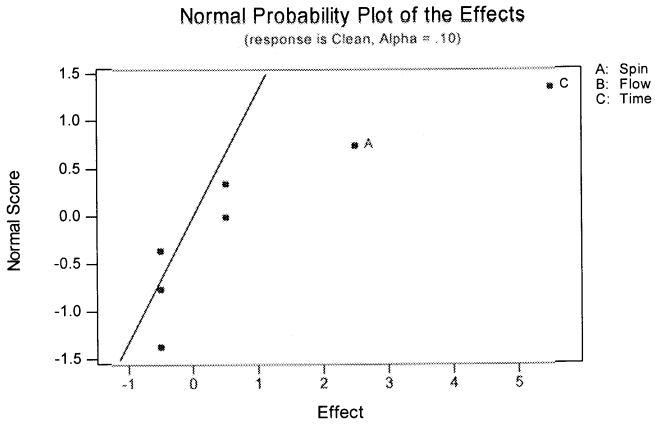
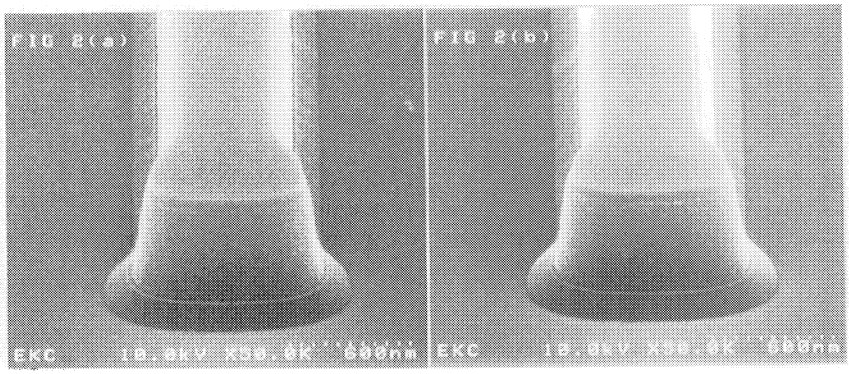
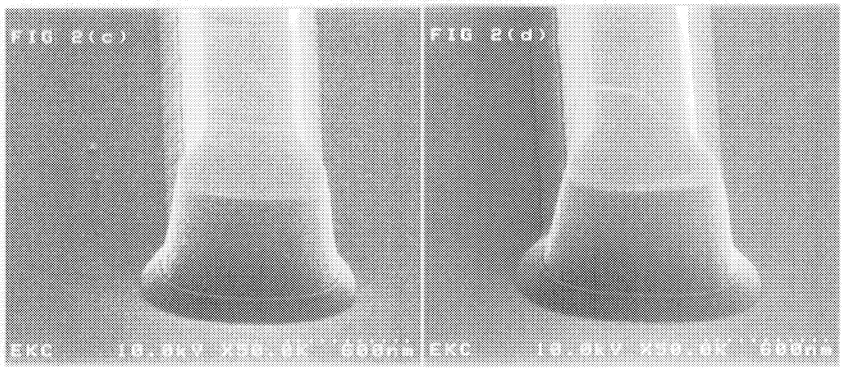


Figure 1C. Statistical analysis of the solvent cleaning study



(a) Edge (b) Center

Figure 2(a-b). Range of arm movement = ± 0 mm



(a) Edge (b) Center

Figure 2(c-d). Range of arm movement = ± control mm

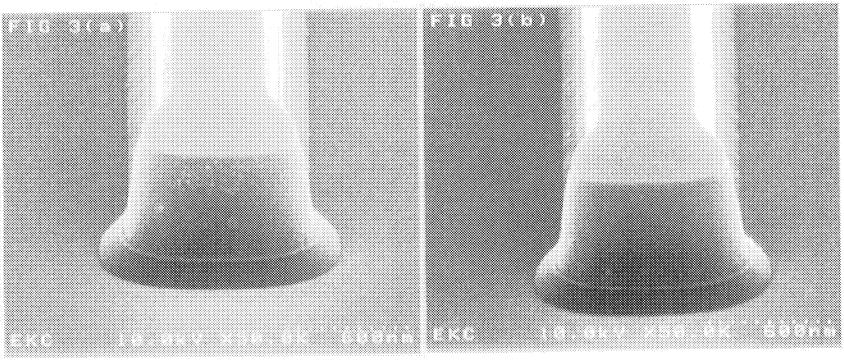


Figure 3(a) dispense arm speed = low; Figure 3(b) dispense arm speed = std

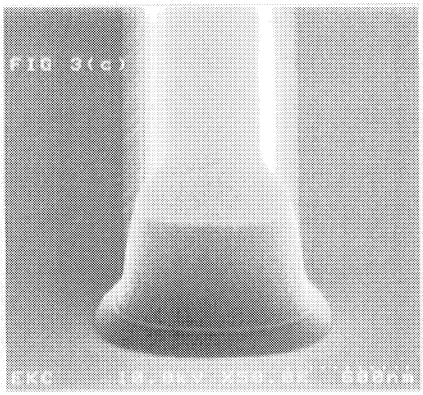


Figure 3c. dispense arm speed = high

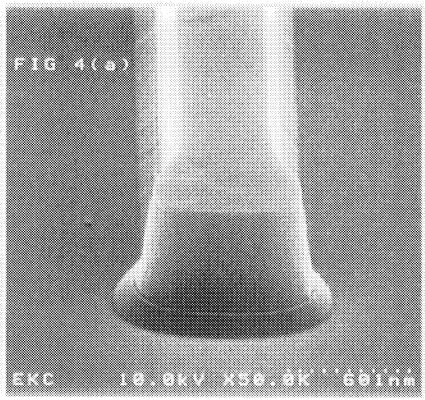


Figure 4(a). fresh bath

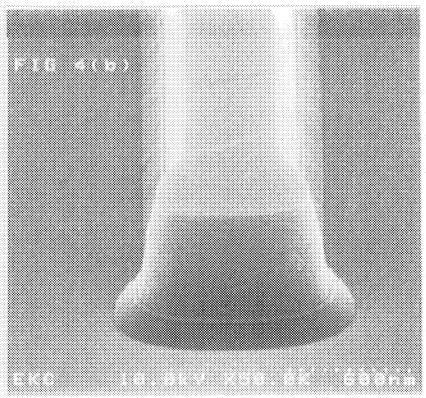


Figure 4(b). aged bath

ACOUSTIC PROPERTY CHARACTERIZATION OF A SINGLE WAFER MEGASONIC CLEANER

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The sound distribution for a single wafer megasonic cleaner was characterized by wafer cleaning tests, visual observations, sound measurements and modeling results. The cleaner consists of a horizontal wafer spinner and a megasonic transducer/transmitter assembly. Sound is transmitted from the transducer assembly to a horizontal quartz rod through a liquid meniscus to the wafer. The sound can travel in both radial and axial directions from the quartz rod. By varying parameters of the transducer and transmission components, the degree of radial and axial sound transmission from quartz rod can be controlled.

INTRODUCTION

Although megasonic cleaning is widely used in the semiconductor industry, the fundamental physical processes are not thoroughly understood. In addition to understanding the mechanism of particle removal, the distribution of sound within a cleaning chamber has been studied via experiments and modeling. Both flat and curved transducers have been investigated.[1]

A single wafer megasonic cleaning method was developed to address the semiconductor industry need for a single wafer cleaner that can be integrated with complementary process steps, such as dry-in/dry-out CMP processing.[2] To remove slurry and other particle contamination, a piezoelectric transducer assembly transmits sound energy along a quartz rod placed directly above the wafer. The sound is then transmitted to the wafer via a liquid meniscus between the quartz rod and wafer (Fig 1). Backside cleaning is accomplished by sound transmission through the wafer. In order to better understand how to optimize and improve cleaning performance, sound characterization investigation has been done. Impact of the quartz rod/wafer distance was previously reported.[3] This work concentrates on the sound distribution across the wafer, specifically the direction of sound transmission from the quartz rod.

EXPERIMENTAL

Cleaning Tool Details

Cleaning experiments were done in a *VERTEQ Goldfinger*, a single wafer, megasonic cleaner (Fig 1&2). The module includes: (1) a wafer chuck and spinner, (2) a megasonic transducer assembly and (3) a chemical delivery system. The megasonic assembly consists of a piezoelectric transducer assembly which is attached to a quartz rod. The transducer assembly consists of a circular piezoelectric material bonded to an aluminum cylinder. The sound (~830 MHz) is transmitted from the transducer through the quartz rod to the liquid meniscus and finally to the wafer. The quartz rod is only above the wafer; backside cleaning is done by sound transmission through the wafer. Chemicals are delivered to the wafer through spray nozzles above and below the wafer. The desired dilution is achieved by mixing H_2O with a concentrated chemical from a metering pump and reservoir in the module. For these experiments, 0.6% NH_4OH solution at 60°C was used. During standard cleaning processes, the chuck is rotated at approximately 20rpm. For characterization purposes, "static" wafer tests were run, where the wafer was not rotated during chemical processing. Afterwards, rinsing and drying (1500-2000 rpm rotation) were done on the same chuck.

Wafer Preparation

Slurry contaminated oxide wafers were prepared by (1) prewetting the wafers in water, (2) dipping for 10s in a bath of Cabot SS-25 slurry, (3) removing and placing in a dilute surfactant solution (Wako) for 10s, and (4) drying in a spin dryer prior to use. Wafer defects were measured on a Tencor 6400 (>0.20μm).

Sound Measurements

A megasonic cavitation meter (PPB-502) was used to measure the energy density of cavitation in liquids. The instrument consists of a sensing probe connected to the electronics case. The meter measures cavitation of the imploding solution bubbles and also the sound waves produced by a pressure transducer. The meter measures the energy twice per second. Experiments of interest include: (1) energy variations at a given point as a function of time, (2) energy distribution across the wafer, (3) energy changes with changes in operating parameters and (4) comparisons over the lifetime of a transducer assembly.

Modeling

Commercially available software (Wave2000) was used. The software uses a finite difference method to compute an approximate solution to a two-dimensional acoustic wave equation. The numerical solution is based on an algorithm published by Schechter.[4] The user defined parameters include geometries (of sound source, transmitter and receiver), physical properties of materials, boundary conditions, sound source conditions, receiver conditions, and parameters to control the simulation.

RESULTS

During normal processing, the wafer is rotated while megasonic energy is applied. To better understand sound distribution, "static" wafer cleaning tests were performed, during which the wafer was not rotated. Shown in figure 3 are defect maps after slurry contaminated wafers were processed under this condition. The defect maps are representative examples of processing under three different transducer setup conditions. Figure 3 also shows the orientation of the quartz rod and liquid dispense. The different transducer conditions produce different sound patterns. The radial:axial component ratio can be altered considerably.

Sound measurements were performed using the probe described in the experiment section. Figure 4 shows the normalized intensity values for transducer conditions A and B from figure 3. There is strong correlation between the clean areas on the wafers and the areas of higher signal from the sound probe. As with the wafer cleaning tests, transducer condition A has a significantly higher axial direction component than condition B.

The transmittance of the sound through the quartz rod was also modeled (2D) using commercially available software. The grid schematic is shown in Figure 5. Geometry and physical parameters of the transducer, quartz rod, wafer, water layer and receivers are inputted. The quartz rod shape was approximated as a rectangle, without considering the curved portion attached to the transducer assembly. The transducer shape was also approximated. The length and width of the quartz rod, and thickness of the water layer and wafer are consistent with experimental values. Receivers were placed in the water layer under the rod and near the end of the quartz rod. This was done to help understand the different axial and radial components seen in the previous experiments. Normalized to a sound source magnitude of 1, transducer condition A produced a signal of 0.2 at receiver 1. Since this receiver was placed just inside of the rod, a low magnitude signal indicates very little sound reflection back into the rod. In other words, the sound is transmitted efficiently in the axial direction. This is consistent with the wafer cleaning tests. On the other hand, transducer condition B produced a normalized signal of 1.1 at receiver 1, indicating inefficient transmission in the radial direction. This is also consistent with wafer cleaning data.

The sound distribution of the transducer assembly without the quartz rod was also evaluated. The flat surface of the cylindrical transducer base was placed horizontally and covered with water. After the transducer power was turned on, the water pattern was observed. Figure 6 shows photos of transducer conditions A, B and C. There is clear correlation of the water vibration pattern with the cleaning tests. Condition A shows vibration in the axial direction; "static" wafer cleaning tests show the same. Condition B shows mostly radial vibration. Condition C shows both axial and radial distribution.

CONCLUSION

Control of sound distribution has been demonstrated for a single wafer megasonic cleaner. This is accomplished by varying the transducer assembly operating conditions. Wafer cleaning tests, sound probe measurements, visual observations and modeling showed qualitative correlation regarding the radial:axial sound intensity. The single wafer cleaner can be integrated with complementary process tools in both front and back end applications. Different operating conditions may be necessary for the cleaning challenges of specific applications.

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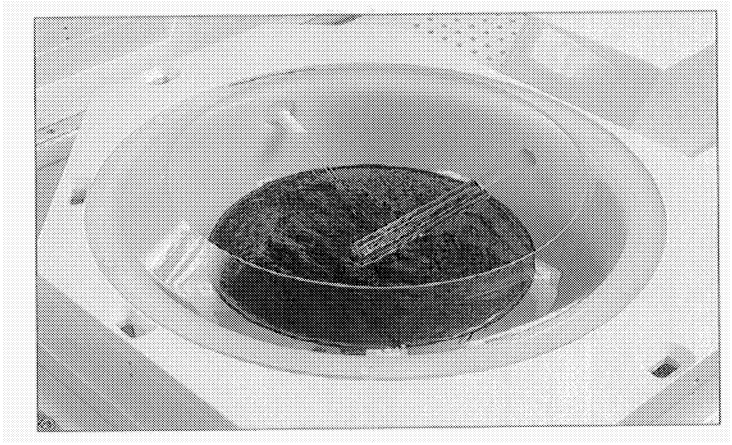

Figure 1. Cleaning module showing the quartz rod projecting over the wafer.

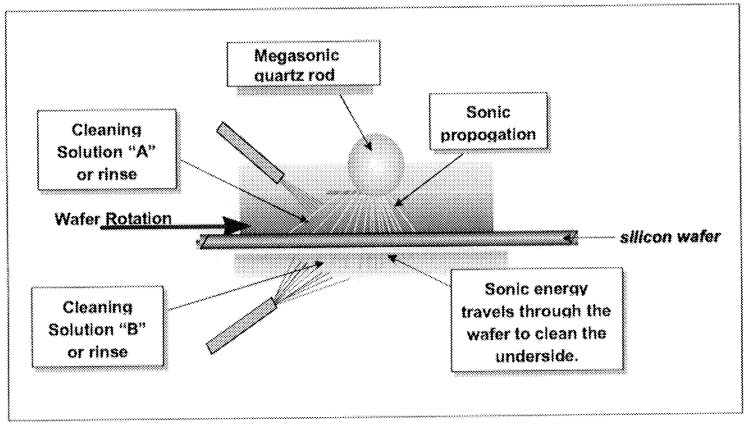

Figure 2. Schematic - megasonic energy propagation and liquid distribution.

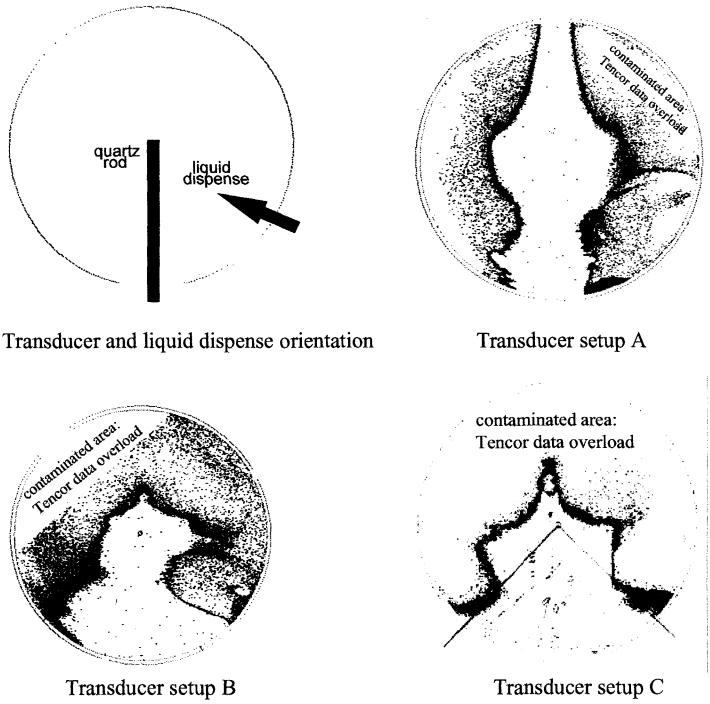

Figure 3. "Static" wafer tests - transducer and liquid dispense orientation; wafer defect maps for 3 different transducer setups.

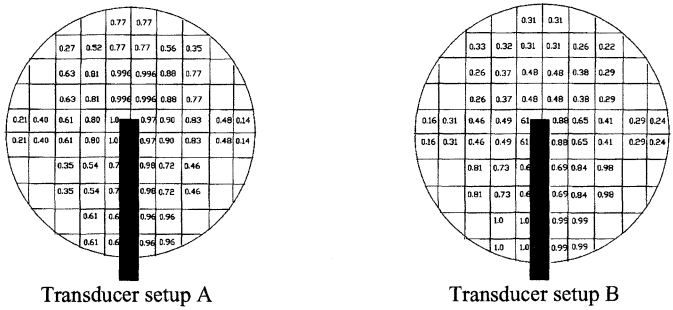

Figure 4. Megasonic probe intensity measurements - normalized

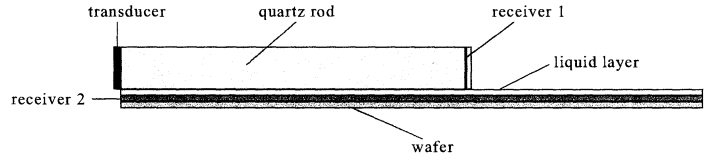

Figure 5. Schematic used for 2D simulation

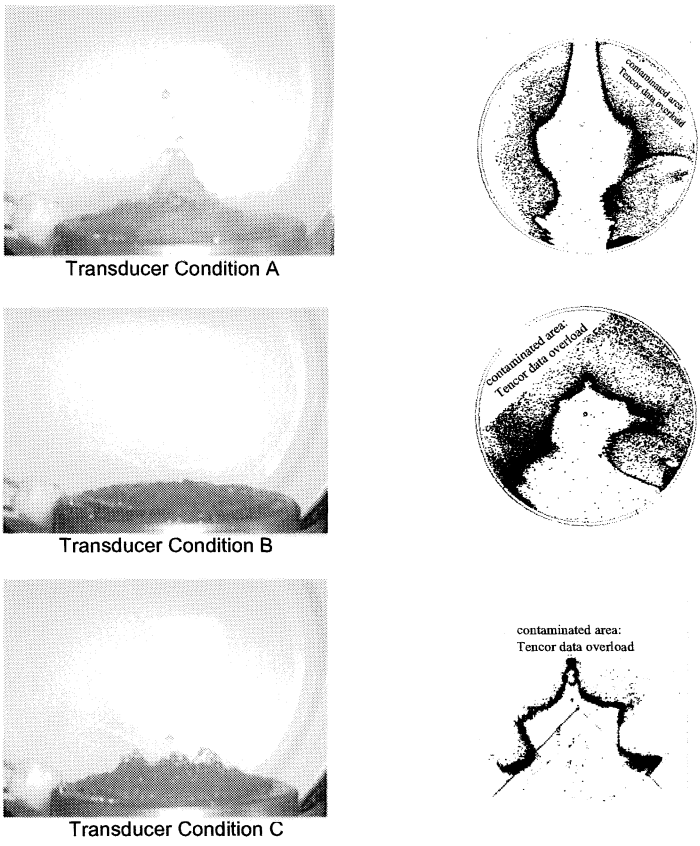

Figure 6. Photos - water placed on transducer assembly without quartz rod - transducer conditions A,B,C.

GENERAL CLEANING AND ETCHING

A LIFETIME ANALYSIS OF DILUTE CHEMISTRY WAFER CLEANING: FASTER, CLEANER, CHEAPER

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ABSTRACT

Metallic contamination introduced into the silicon lattice during the processing of integrated circuits is a main source of crystallographic defects and reduced carrier lifetimes. Silicon wafer cleaning removes particulate contamination, organic residues and surface metallic contamination while maintaining a smooth, polished surface. In this work, wafers were processed through single and multiple cleans using a modified RCA wafer cleaning process incorporating HF/HCl and various SC2 dilutions and clean times. The results show that even with a 50% time reduction and a factor of five reduction in SC2 concentration, improved particle removal and high diffusion lengths were observed. The modified clean yielded hydrophilic surfaces with no surface roughness degradation. The resulting clean process reduces chemical costs and manufacturing cycle time without impacting product quality.

INTRODUCTION

In semiconductor device manufacturing, wafer cleaning is the single most frequently used process step. Providing ultra-clean wafers significantly impacts both the product cost and process cycle time. Ultra-clean wafers are required as silicon lattice defects resulting from metallic contamination have been reported to cause yield degradations associated with leakage currents, refresh time, and MOSFET gate oxide integrity [1-4]. Since most wafer cleans are followed by a high temperature diffusion process which can drive the metallics into the silicon lattice, cleans which do not introduce metals on the surface of the wafers are imperative. As such, it is important to investigate cleaning effects not only for a single clean but for multiple cleans followed by heat treatments.

A typical wafer cleaning process, often referred to as the "RCA BClean", is presented in Table I [5]. Each chemical step is followed by an ultra pure water (UPW) rinse. This procedure is followed by a drying process, typically a spin dry.

Table I - Typical RCA BClean

Step	Chemicals	Mix
1	Sulfuric Acid (H_2SO_4) + Hydrogen Peroxide (H_2O_2)	5:1
2	UPW + Hydrofluoric Acid (HF)	40:1
3	Ammonium Hydroxide (NH_4OH) + H_2O_2 + UPW	1:1:5
4	Hydrochloric Acid (HCl) + H_2O_2 + UPW	1:1:5

A mixture of H_2SO_4 + H_2O_2, called piranha, is employed to remove organic films from previous operations. The dilute HF then removes any chemical oxide grown in the piranha and enhances the surface for particle removal. The NH_4OH + H_2O_2 solution, called SC1, is used for particle removal. Unfortunately, the SC1 also forms an oxide layer that can incorporate metals. A HCl + H_2O_2 solution, called SC2, then removes metals only from the surface of the oxide. Since this clean typically precedes a thermal anneal, metals incorporated in the oxide or on the silicon surface can be driven into the silicon and reduce the minority carrier lifetime [2, 6, 7, 8, 9].

Previous work has shown a significant lifetime improvement can be obtained by modifying the typical wafer cleaning sequence using SC1 and SC2. The modified cleaning sequence adds a HF/HCl step after the SC1 clean which removes the metallic containing oxide formed in the SC1. The subsequent SC2 cleaning step then grows a metallic free oxide allowing for a hydrophilic wafer surface [10]. Compared to the standard immersion cleaning sequence without the HF/HCl step, the diffusion length was reported to be increased by 50% for a single clean and 35% after four cleans and anneals with no degradation in particle removal efficiency [6, 7].

While previous work used inexpensive, Clean Room grade chemicals for additional cost savings, it is desirable to investigate more dilute mixtures and decreased clean times and their effects on lifetime, particle removal and wafer surface condition. It has been previously shown that the use of high purity chemicals results in improved lifetime. Equivalent results can also be achieved with Clean Room grade chemicals with the addition of the HF/HCl step [6]. Since particle removal efficiency, high silicon lifetime, and low surface roughness are desired, it is important to investigate these parameters relative to chemical dilutions and reduced clean times.

Various analytical techniques have been employed for metallic monitoring including Secondary Ion Mass Spectroscopy (SIMS), Total X-Ray Fluorescence (TXRF), Surface Photovoltage (SPV) and Electrolytic Metallic Analysis Tool (ELYMAT). In this

paper, metallic contamination will be inferred from ELYMAT diffusion length data, where higher diffusion lengths imply fewer metallic contaminants [11]. The minority carrier diffusion length is related to the lifetime by the relationship:

$$L = \sqrt{D\tau} \quad (1)$$

where L is the diffusion length, D is the minority carrier diffusion constant and τ is the lifetime in seconds. The recombination lifetime is the average time an excess electron-hole pair exists. The diffusion length is the average distance a carrier travels before recombining. Recombination properties of structural silicon defects, such as dislocations, depend upon whether or not the defects are decorated with metallic impurities. Therefore, lifetime and diffusion length measurements are good indicators of process cleanliness with respect to metallic contaminants.

This paper will present diffusion length, particle removal efficiency, etch rates and surface micro-roughness data from silicon wafers. These wafers were processed through single and multiple cleans using the sequence above incorporating the HF/HCl and various SC2 mixtures and clean times.

EXPERIMENTAL

Clean experiments were conducted in a Verteq Automated Wet Station. The Verteq Wet Station, located in a Class 10 clean room, contains piranha, SC1, and SC2 tanks which are constructed from quartz in a linear layout. HF tanks are made from perfluoroalkoxy (PFA). The UPW rinse tanks are made of polyvinylidene fluoride (PVDF). The post sulfuric UPW rinse, SC1 tank, and post SC2 UPW rinse are all equipped with quartz Sunburst turbo megasonic transducers operating at 250 watts. The concentration in the SC1 tank is continuously monitored and maintained by automated additions. Prior to the experiment, the Verteq was optimized to enhance particle removal efficiency and oxide etch rate by varying concentration, temperature and time. All cleans are completed in a Verteq Model 8201 horizontal spin rinse dryer with three steps: 1) 90 s at 900 RPM with heated nitrogen 2) 360 s at 750 RPM with heated nitrogen and 3) 60 s at 750 RPM with unheated nitrogen.

Wafers were processed through the Verteq using the standard BClean, the BClean with the HF/HCl step inserted between the SC1 and SC2 steps (ISilCln), and the BClean/HF/HCl flow with various SC2 dilutions and times (MISilCln). To simulate the cumulative effect of wafer cleaning on diffusion length over the course of device fabrication, experiments comparing the standard BClean, the ISilCln and the MISilCln with various SC2 dilutions and times were performed which repeated the clean flow and

anneal as many as five times. Wafers were pulled and analyzed after each clean flow/anneal cycle. The experimental layout is shown in Table II.

Table II - Experimental Layout

Wafer ID	Description	SC2 Formula	SC2 Time
Control	Box Controls	None	None
BClean	Standard clean, no HF/HCl between SC1 and SC2	1:1:5	10 minutes
ISilCln	Standard clean with HF/HCl between SC1 and SC2	1:1:5	10 minutes
MISilCln	Clean with HF/HCl between SC1 and SC2	1:1:25	5 minutes

Ashland Clean Room grade chemicals were used for all chemistries. Chemicals were introduced to the tools from a bulk supply, except HCl which was added manually to the 40:1 HF in the Verteq.

For lifetime experiments, p-type, 5-20 ohm-cm, 150 mm CZ silicon wafers were used. The wafers after each treatment were activated at 600°C for 1 hour prior to ELYMAT analysis [6]. The same furnace tube was used for all activations.

The minority carrier diffusion lengths were measured on a GeMeTec ELYMAT II operating in Backside Photo Current (BPC) mode. Injection levels of 1 to 2 mA were employed using a 905nm laser. The applied potential between the wafer and back cell was varied between 3V and 6V. A one percent HF solution was used as an electrolyte and to dissolve surface oxides. Diffusion lengths were calculated from diffusion current data assuming a 10 ohm-cm wafer resistivity [10].

All wafers for the particle removal experiments were contaminated in 9:1 buffered oxide etch solution, rinsed and spun dry. Particle counts greater than 0.2 μm were taken using a Tenor Surfscan 6420 prior to contamination, post-contamination and post-clean. The particle removal efficiency (PRE) was calculated based on following equation:

$$PRE = (\text{Post-contamination} - \text{Post-clean}) / \text{Post-contamination} \times 100 \quad (2)$$

Surface roughness after the standard clean and the modified clean was compared using Atomic Force Microscopy (AFM). A Digital Instruments Dimension 3000 operating in tapping mode with etched silicon tips was employed. The same wafers used in Table 2 were first measured for surface roughness, then later measured for diffusion length.

RESULTS and DISCUSSION

In order to understand the effects of the new cleaning sequence on wafer diffusion length, the experiment consisted of two parts. The first part evaluated the three cleaning sequences, the standard BClean, the ISilCln, and the MISilCln in a single pass. Three wafers were cleaned in each of the three solutions and two wafers were used as control wafers. To simulate the effects of full flow processing, the second experimental phase evaluated the three cleans under multiple clean/anneal cycles. After the first pass evaluation in part one, a single wafer was measured for diffusion length and surface roughness after two, three, four and five clean/anneal cycles.

Figure 1 illustrates the diffusion lengths measured for the three cleans and the two control wafers. Note: It is generally accepted that diffusion length values above 500 um are acceptable [6]. The two HF/HCl recipes are comparable, whereas the standard BClean exhibited slightly reduced diffusion lengths. However, it should be noted that the differences observed between the BClean and the ISilCln were not as dramatic as reported earlier [7]. The differences evidenced below may, in fact, be due to normal variation in diffusion lengths between wafers. Nonetheless, it is worth noting that both HF/HCl cleans performed as well or better than the standard BClean.

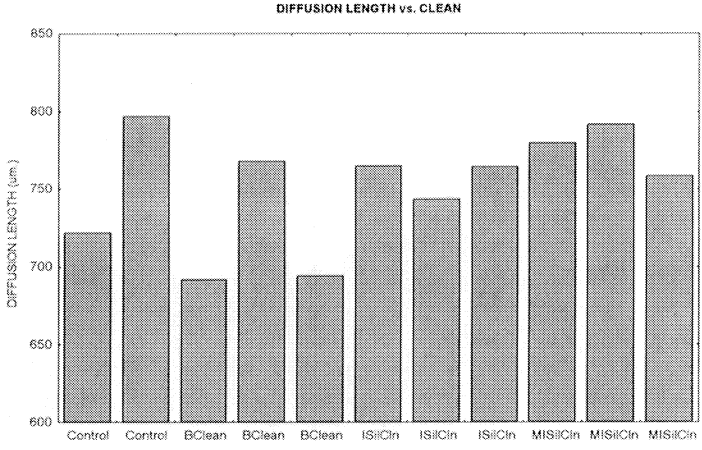

Figure 1. A comparison of the three wafer cleaning recipes, plus controls, after a single clean/anneal cycle. Each bar represents an individual wafer's average diffusion length.

Figure 2 contains the diffusion length measurements for the three cleans after multiple clean/anneal cycles.

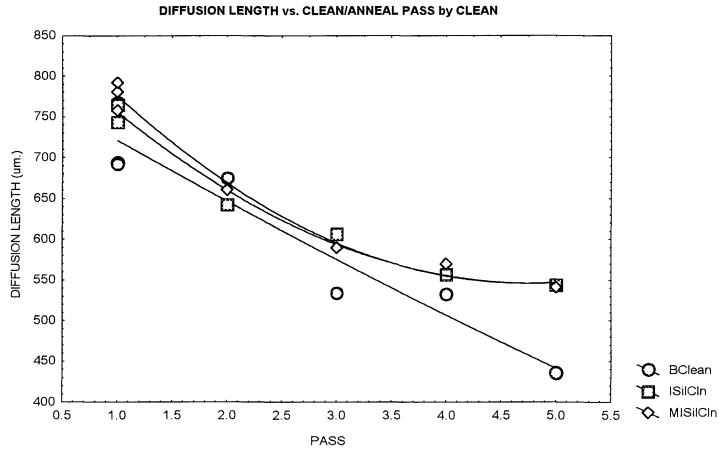

Figure 2. A comparison of the three wafer cleaning recipes after multiple clean/anneal cycles. A second order polynomial was fit to each of the three data sets. These models are for illustration purposes only.

A regression analysis revealed several interesting features. First, under the assumption that the same curve, +/- a fixed offset, could adequately explain the variation in the diffusion lengths for the HF/HCl recipes, there was not a statistically significant offset, p-value 0.212. In other words, the same curve could be used to model both sets of HF/HCl data without the need for a recipe additive effect. The empirical diffusion length model for the HF/HCl recipes is

$$\text{HF/HCl recipes Diffusion Length} = 897.0 - 147.4*\text{Pass} + 15.5*\text{Pass}^2. \quad (3)$$

This model accounted for 98.1% of the variation in the data. Second, a regression analysis identified a simple linear trend as the model suitable for the standard BClean data. This model accounted for only 91.8% of the variation in the data and is given below

$$\text{BClean Diffusion Length} = 789.6 - 70.4*\text{Pass}. \quad (4)$$

The results of these analyses are subject to interpretation. If the linear trend model holds for the BClean data and the quadratic model applies to the HF/HCl data then the HF/HCl recipes are asymptotically better than the BClean. The BClean first order model

may have been selected due to the additional noise in the data. If, in reality, a similar quadratic model applies for the BClean data then the root cause for the additional variation in the BClean data is a cause for concern. Does the BClean follow the same trend subject to higher levels of variation? This scenario is a less than ideal situation for device performance and process behavior and contrasts with our earlier findings [7]. Regardless of interpretation the net effect is the same - the HF/HCl recipes are superior to the BClean. In addition, the quicker, more dilute MISilCln is equivalent to the ISilCln.

Table III presents the average particle removal efficiency data from the BClean and the MISilCln in the Verteq. Post-contamination counts ranged from 315 to 2300. The particle removal efficiency is essentially the same in the Verteq for both cleans.

Table III - Particle Data and Oxide Removal

	Particle Removal Efficiency	Oxide Removal Rate (nm/pass)
BClean	97 %	8.8
MISilClean	99 %	9.0

In IC processing, total oxide etching has an effect on both the vertical and horizontal device dimensions. Understanding the amount of oxide removal during the multiple clean steps is important in adjusting the process times. Oxide removal was determined for both cleaning flows. Table III shows the oxide removal is within 3 %.

Figure 3 shows how the surface roughness changes as wafers go through a single pass with various cleans. The ISilCln and the MISilCln wafers were similar and appear to be somewhat smoother than the standard BClean wafers.

Figure 4 shows the surface roughness of wafers undergoing multiple clean and anneal cycles. Multiple clean and anneal cycles do not seem to cause the surface roughness to become worse. All roughness values approach a comparable value of 0.1 nm. Since the oxide surface is removed and grown as wafers go through the SC1 and SC2 process, surface roughness can vary.

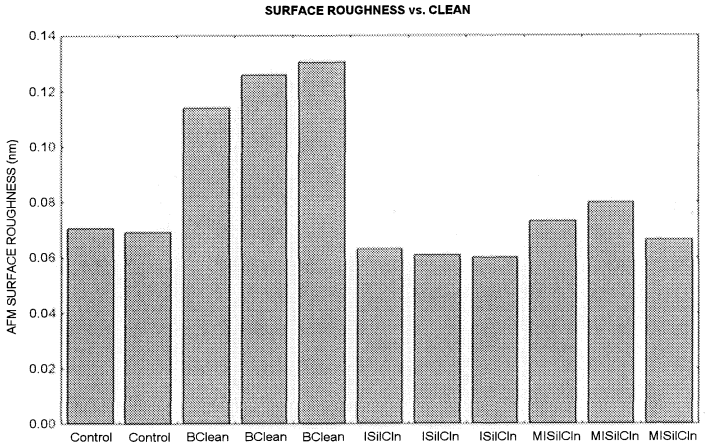

Figure 3. A comparison of the three wafer cleaning recipes, plus controls, after a single clean/anneal cycle. Each bar represents an individual wafer's surface roughness.

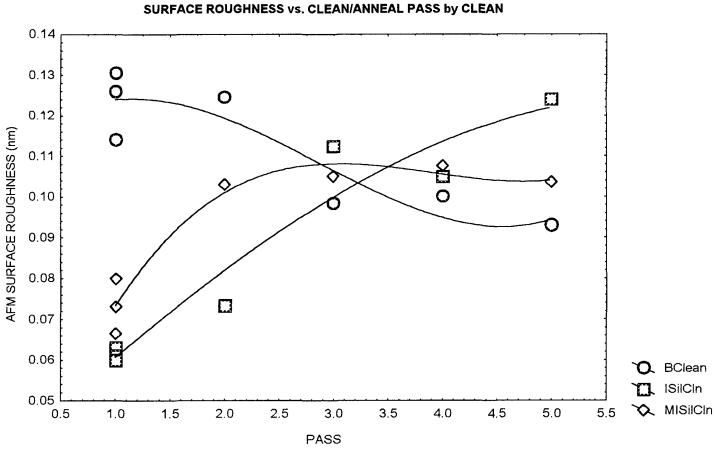

Figure 4. A comparison of the three wafer cleaning recipes after multiple clean/anneal cycles. A third order polynomial was fit to each of the three data sets. These models are for illustration purposes only.

CONCLUSION

The MISilCln with an 80% reduction in SC2 concentrations of HCl and H_2O_2 and a 50% reduction in the SC2 process time, still provided clean wafers with no loss of any quality metric when compared to the standard BClean or standard ISilCln. The MISilCln clean results in a direct SC2 chemical and disposal cost reduction with an estimated cost savings for the total clean of nominally 20%. The ISilCln in either form appears equivalent or superior to the BClean for metallic contamination and particle removal supporting previous findings. For multiple cleans, the MISilCln produces higher diffusion lengths than the BClean. All three cleans were comparable for surface roughness over the five passes investigated. The ISilCln employed on manufacturing product was shown to reduce microscopically observed point defects without any device yield degradation. Current efforts are focused on installing the MISilCln in production.

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THE CHEMISTRY OF CO-INJECTED BOE

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ABSTRACT

Buffered Oxide Etch (BOE) is an oxide etching solution based on HF chemical buffered by NH_4F. BOE does not attack photoresist and is preferred for patterned etching of oxides. Pre-mixed BOE is, however, more expensive than diluted HF and is only available in a limited number of blend ratios. It is also possible to create BOE by mixing HF with NH_4OH which allows a reduction in cost and the optimization of the etch process.

There are a large number of species present in BOE, including: HF, F^-, H_2F_2, HF_2^-, NH_3, NH_4^+, H_3O^+, OH^-. The rate of oxide etching depends on the concentrations of HF, HF_2^- and, to a lesser extent, H_2F_2. This work demonstrates a method of calculating the HF:NH_4OH blend ratio necessary to make the common formulations of BOE along with the species present in these formulations along with experimental results of this approach gathered from a production fab.

INTRODUCTION

Buffered Oxide Etch (BOE) is an etching solution widely used in the semiconductor industry to etch oxide layers through a photoresist mask. Many works have already been published on this subject (1, 2, 3, 4), presenting the behavior of doped and undoped silicon dioxide films under BOE etching (2, 5). The mechanism of SiO_2 etching is not fully understood, and many works provide different analyses (3, 4, 6).

Because photoresist is not attacked by solutions with a pH greater than 3, BOE is preferred for patterned etching of oxides. Premixed BOE is, however, more expensive than DHF (diluted HF) and is only available in a limited number of blend ratios. Often only one or two blend ratios are available at a facility. Making BOE in situ by co-injection of HF and NH_4OH allows a reduction in cost and the optimization of the etch process (1).

Co-injected BOE is an HF-based oxide etchant with added NH_4OH. The combination of HF and NH_4OH form NH_4F in solution which buffers the fluoride concentration. The description "BOE n/m" refers to a volumetric mixing ratio of n parts of 40 wt% NH_4F and m parts of 49 wt% HF. There are a large number of species present in BOE, including: HF, F^-, H_2F_2, HF_2^-, NH_3, NH_4^+, H_3O^+, OH^-. We have solved a system of eight equations to determine the concentration of each species. This work provides a method of calculating the HF:NH_4OH blend ratio necessary to make the common formulations of BOE along with the species present in these formulations.

We used the main results derived from the calculations to test the performance of co-injected BOE through an experimental implementation in the field, in ATMEL Fab 7, in Rousset, France.

THEORETICAL APPROACH

BOE n/m

The first important parameter is the quantity of HF in solution. Because co-injected BOE can be prepared with DHF of any concentration, hence of any density, the evaluation of the quantity (in terms of mass or moles) of HF introduced into the solution must be done as follows. If n is the number of moles of HF (molecular weight M) introduced by a volume V of x wt% HF (density d), then:

$$n = (V*d*x) / M \qquad \text{[Eq. 1]}$$

To calculate the " BOE n/m" ratio, we will introduce the following parameters:

* V_1 is the volume of the HF solution.
* x_1 is the wt% of the HF solution (wt% expressed as a fraction from 0.00 to 0.49).
* d_1 is the density of the HF solution.
* M_1 is 20 $g \cdot mol^{-1}$ for HF.

* V_2 is the volume of the NH_4OH solution.
* x_2 is the wt% of the NH_4OH solution (normally, $x_2 = 0.28$).
* d_2 is the density of the NH_4OH solution (the density of 28% NH_4OH is 0.895 $g \cdot cm^{-3}$).
* M_2 is 17 $g \cdot mol^{-1}$ for NH_3 (The wt% of NH_4OH actually refers to the wt% of NH_3 dissolved in H_2O).

Using Eq. 1 with the appropriate values, n_1, the number of moles of HF, and n_2, the number of moles of NH_4OH, can be determined.

When the HF acid solution is mixed with the NH_4OH basic solution, NH_4F is created by the following reaction:

$$HF + NH_4OH <=> NH_4F + H_2O \qquad \text{[Reaction 1]}$$

Reaction 1 is effectively not an equilibrium, but a reaction that proceeds very nearly to completion, because the constant of this reaction is close to 10^6 (ratio of HF/F^- acidic constant $10^{-3.2}$ and NH_4^+/NH_3 acidic constant $10^{-9.2}$). That is a very high value and means the reaction of HF with NH_4OH is fast and leads directly to NH_4F formation by a complete consumption of HF or NH_4OH, depending on which of these two compounds is in the minority. In our case, NH_4OH will be the limiting factor (in minority) to keep the final solution acidic. To ensure there is excess HF for the etching step, the mixture must be prepared so that $n_2 < n_1$. The assumption is that the reaction of HF and NH_4OH is total so that the initial n_2 moles of NH_4OH will be transformed into n_2 moles of NH_4F. During the reaction, n_2 moles of HF are consumed so that $n_3 = n_1 - n_2$ moles of HF is left at the end of the reaction.

Because the description "BOE n/m" refers to a volumetric mixing ratio of n parts of 40 wt% NH_4F and m parts of 49 wt% HF, the n_2/n_3 ratio of moles must be transformed

into the volume ratio of n/m. Regarding the NH_4F compound, the equivalent volume V_3 (virtual volume) of 40 wt% NH_4F solution that should contain n_2 moles of NH_4F can be determined by using Eq. 1, with : $n = n_2$, $x = 0.4$, $M = 37\ g{\cdot}mol^{-1}$ and $d = 1.09\ g{\cdot}cm^{-3}$.

Regarding the HF that remains, the equivalent volume V_4 (virtual volume) of 49 w% HF solution that should contain n_3 moles of HF can be calculated similarly by using Eq.1 with : $n = n_3$, $x = 0.49$, $M = 20\ g{\cdot}mol^{-1}$ and $d = 1.19\ g{\cdot}cm^{-3}$.

The V_3/V_4 ratio gives the n/m value ; In other words, mixing a volume V_1 of HF (x_1 wt%) with a volume V_2 of NH_4OH (x_2 wt%) gives a BOE n/m. Usually, we calculate the equivalent n/m ratio so that m = 1. In the industry, the current typical values of BOE are 7/1, 9/1, 20/1, and 100/1.

For example, 250 cc of 10% HF ($d = 1.05\ g{\cdot}cm^{-3}$) contains n_1=1.3125 moles, and 50 cc of NH_4OH contains n_2 = 0.7371 moles. When these two quantities are mixed together, 0.7371 moles of NH_4F (n_2) is created, and there is 0.5754 moles of HF (n_3) remaining. These molar quantities correspond to 62.55 cc of NH_4F (virtual V_3) and 19.74 cc of HF (virtual V_4), so a solution of BOE 3.2/1 is made by co-injection of the two initial volumes of HF and NH_4OH.

The above calculations are fundamental to BOE mixing. For a given target (e.g. BOE 7/1), the necessary adjustment in V_2 can be easily calculated and the correct mixture parameters be found. Figure 1 shows a sample application of 28% NH_4OH mixed with 150 cc of 49% HF. The 150 cc of HF 49% are neutralized by 297 cc of NH_4OH. For good stability of the BOE ratio, resulting in a 3.2/1 BOE solution.

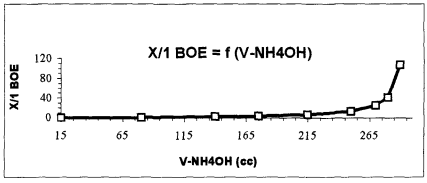


Figure 1: X/1 BOE for different NH_4OH volumes added to 150 cc of HF 49 wt%.

The different species of the mixture

For the following calculations, we suppose eight main species in aqueous solution: HF, F^-, H_2F_2, HF_2^-, NH_3, NH_4^+, $H_3O^+$and OH^- (1, 2, 4). The concentration of each of the eight species can be calculated by solving eight simultaneous equations.

HF acidic equilibrium $HF \Leftrightarrow H^+ + F^-$ [Reaction 2]

$Ka_1\ [H^+]\,[F^-]/[HF] = 6.85x10^{-4}\ mol{\cdot}l^{-1}$ (7) [Eq. 2]

NH_4OH acidic equilibrium $NH_4^+ \Leftrightarrow H^+ + NH_3$ [Reaction 3]

$Ka_2 = [NH_3]\,[H^+]/[NH_4^+] = 6.31x10^{-10}\ mol{\cdot}l^{-1}$ [Eq. 3]

Water dissociation $2\,H_2O \Leftrightarrow H_3O^+ + OH^-$ [Reaction 4]

$Ke = [H_3O^+]\,[OH^-] = 10^{-14}\ mol{\cdot}l^{-1}$ [Eq. 4]

HF complexation $HF + F^- \Leftrightarrow HF_2^-$ [Reaction 5]

$Kd_1 = [HF_2^-]/[HF]\,[F^-] = 3.963\ l \cdot mol^{-1}$ (7) [Eq.5]

HF dimerization $HF + HF \Leftrightarrow (HF)_2$ [Reaction 6]

$Kd_2 = [(HF)_2]/[HF]^2 = 2.7\ l.mol^{-1}$ (8) [Eq. 6]

Electroneutrality equation $[H_3O^+] + [NH_4^+] = [OH^-] + [F^-] + [HF_2^-]$ [Eq. 7]

Fluoride conservation $[HF] + [F^-] + 2[(HF)_2] + 2[HF_2^-] = A$ [Eq. 8]

Nitrogen conservation $[NH_3] + [NH_4^+] = B$ [Eq. 9]

Constants A and B are the initial total fluorine and nitrogen concentrations. In this system, there is only one source of fluoride: HF. In the case of a commercial BOE solution, two sources should be taken into account : (HF, and F^- coming from the NH_4F).

$A = (n_1$, number of moles of HF)/total volume [Eq. 10]

$B = (n_2$, number of moles of NH_4OH)/total volume. [Eq.11]

The total volume is the sum of all the volumes: HF, NH_4OH and DI water. DI water is often added to BOE to reduce the oxide etch rate. The addition of water will influence the values of A and B and shift the balance of species and the pH. We will present the role of the water and the influence of the factor of dilution. Similiarly, because B depends on the total volume, anytime the volume of the mixture is changed (even if it is only the DI water volume), the B constant changes.

Resolution of the system

To solve the complex system of eight equations, each concentration was expressed as a function of $[H_3O^+]$. To express $[OH^-] = f([H_3O^+])$, Eq. 4 was used. To express $[NH_3]$ and $[NH_4^+] = f([H_3O^+])$, a sub-system of two equations (Eq. 3 and Eq. 9) with the two nitrogen species needed to be solved.

To express [HF], $[F^-]$, $[(HF)_2]$ and $[HF_2^-] = f(H_30^+)$, first express $[F^-]$, $[(HF)_2]$ and $[HF_2^-]$ as a function of [HF] using Eq. 2, Eq. 5 and Eq. 6. Then, express [HF] = $f([H_3O^+])$ from Eq. 8 using the previous expressions. This last expression is a second-degree equation because of the ($[HF]^2$) term in Eq. 6. The resolution of this second-degree equation is easy because the negative solution has no physical meaning. The four fluorinated species are determined out from this four equation subsystem.

So far, for one $[H_3O^+]$ value, there is only one concentration for each species. And to determine which is the right $[H_3O^+]$ value, solve the last equation of the system: Eq. 7 (electroneutrality).

It is possible to express all the concentrations as a function of $[H_3O^+]$. The resulting expressions depending on the A and B constants, which are known if the initial volumes (HF, NH_4OH and DI water) are decided.

RESULTS

Theoretical results

During the acidic neutralization of HF by the basic NH_4OH solution, the fluoride element reorganizes itself between its four species. Figure 2 shows the calculated distribution of the different species in a solution using 1800 cc of DI water, 100 cc of 49 wt% HF and 0 to 200 cc of 28 wt% NH_4OH.

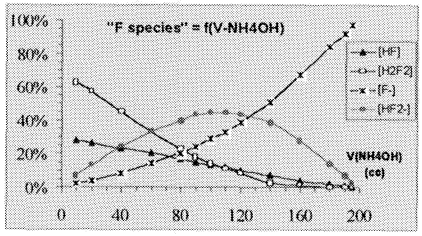
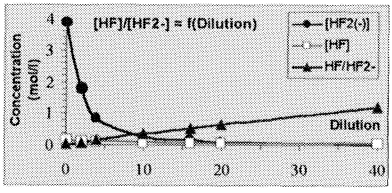


Figure 2: Distribution of the species depending on the mixture.

As more NH_4OH is added, more HF reacts to create NH_4F. The fraction of F^- increases, and at the same time the fractions of HF and the dimer, $(HF)_2$, decrease. The HF_2^- behavior is the most interesting. It is well known that HF_2^- is an etching species. Different works have shown an optimum value of etch rate or the correlation between fluorinated species and pH (3, 4, 5). Our simulation indicates that the optimum $[HF_2^-]$ corresponds to a 1:1 blend of HF:NH_4OH corresponding to a BOE ratio close to 3/1. We will see later that this is a critical value. In such conditions, we will experimentally observe the highest etch rates with no attack of the photoresist (Figure 8).

Using the system of eight equations, the correct concentrations of each species can be determined and correlated to the etch rate observed , thus the chemical species involved in the etching mechanisms may be revealed. Today, many works report different behaviors (4, 5, 6), including the participation of HF, $(HF)_2$ and HF_2^-, during the etch.

Making some simulations, the influence of water on the BOE system is observed. Figure 3 shows that $[HF_2^-]$ concentration decreases much faster than [HF] concentration with increasing water volume. The HF_2^-/HF ratio increases with higher dilution. In fact, the HF_2^- complex is dissociated into HF and F^- through the dilution. The dissociation of HF_2^- by water influences all the species are influenced. The pH also changes from 4.6 to 3.6 (Figure 4). The pH drops with increasing dilution due to the



dissassociation of HF_2^- leading to the generation of HF.

Figure 3: Influence of water on the BOE.

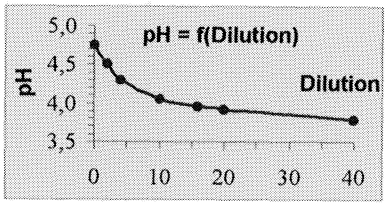


Figure 4: Influence of water on BOE.

Experimental results

The experimental results were obtained using an FSI MERCURY® MP Surface Conditioning System in ATMEL Fab 7 in Rousset, France. The tests have been performed using 8-inch wafers. The uniformities are given after nine point measurements.

Figure 5 shows the exothermicity of the reaction between HF and NH_4OH. In our experiments, we consider the reaction of different volumes of 28% NH_4OH with 100 cc of 49% HF. Because NH_4OH is the limiting factor of the reaction, the volume of NH_4OH is the key parameter to control the exothermicity and to allow optimization of the process in terms of etching uniformities -- by controlling the temperature of the chamber, for instance.

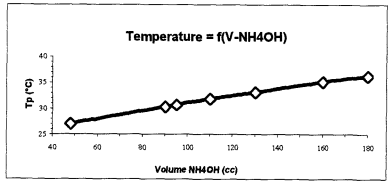


Figure 5: Exothermicity of the reaction between HF and NH_4OH.

Depending on the NH_4OH volume that will be used in the mixture, it is possible to optimize the process conditions and take into account the exothermicity of the co-injection. Figure 6 shows the etch rates of BOE made by co-injecting flows of HF, NH_4OH and DI water. A large range of etch rates are available, allowing process optimization.

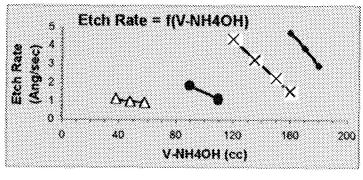


Figure 6: Etch rates obtained for different co-injected BOE.

It is possible to get relatively low etch rates (less than 1 Å/s) or higher values if necessary. The thickness to be etched will determine the choice of the best mixture. Also, different co-injected mixtures can be prepared to get a similar etch rate (e.g., 2 Å/s).The final choice will be determined by the etch uniformities performance.

Figure 7 shows the on-wafer non-uniformity for different co-injected BOE. Non-uniformity on wafer down to 0.7% with a good cross-boat non-uniformity (about 1%) can be reached. Slot 24 of the carrier is the worst, but with optimized conditions, we reach less than 2% on-wafer non-uniformity.

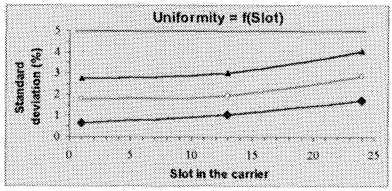


Figure 7: On-wafer non-uniformity for 3 different mixtures (test wafers in slots 1, 13 and 24).

It is observed that the less NH_4F is formed, the better the uniformity is. We correlate this result to the fact that NH_4F makes the final solution more viscous and influences the process in terms of uniformity.

Finally, it is most important to avoid any damage to the photoresist during the oxide etch. Figure 8 presents optimal conditions under which to use BOE. Our simulations confirm that while the BOE X/1 ratio is above 3 (pH greater than 3), the oxide is successfully etched without any damage to the photoresist. In the same figure, it is shown that HF solutions which are even very diluted (200 times) still have a pH under 3, making such solutions much less convenient than BOE for critical etchings.

CONCLUSION

Buffered Oxide Etch (BOE) has been studied from a chemical point of view. Through an eight equation system that we solved, we are able to estimate the concentrations of the etching species involved in the co-injected BOE etching. The blend ratios can be optimized for different applications.

The figures indicate the role of HF, NH_4OH and water dilution to the balance of species in the etching system. Predictions of the theoretical approach have been used successfully at a customer site over the last few months.

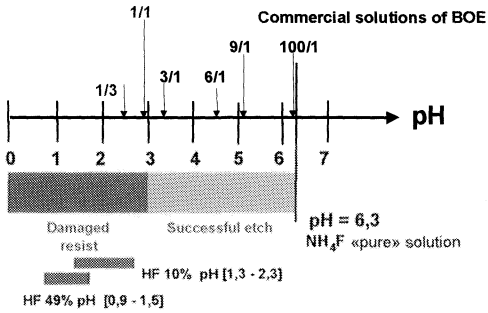


Figure 8: The optimal conditions under which to use BOE.

ACKNOWLEDGMENTS

The experimental data was obtained on an FSI MERCURY® MP Spray tool at ATMEL Fab 7 in Rousset, France. The authors thank Gaëlle Philit and Arnaud Coze from ATMEL for their contributions during the experiments.

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USE OF H_2SO_4 FOR ETCH RATE AND SELECTIVITY CONTROL OF BOILING H_3PO_4

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ABSTRACT

The etch rates of thermally grown SiO_2, densified and undensified atmospheric pressure chemical vapor deposited (APCVD) SiO_2 and low pressure chemical vapor deposited (LPCVD) Si_3N_4 in boiling H_3PO_4 are controlled by the addition of H_2SO_4 to the bath. The rate of the etch rates, referred to as the etch selectivity can be adjusted by varying the amount of H_2SO_4 used and the process temperature. Process stability and bath lifetime are improved by the H_2SO_4 addition as the etch rate of the different films can be made independent of the bath usage.

1-INTRODUCTION

High selectivity of silicon nitride etch towards silicon oxide has always been a key aspect for the nitride mask removal on LOCOS and STI isolation schemes. Boiling H_3PO_4 has been historically the etchant of choice for this application as selectivities greater than 35:1 can be easily obtained [1]. However, the etch rate of both films and the selectivity vary with the usage of the chemical due to the incorporation of silica to the bath from the etched nitride. Tight control of the selectivity and etch rate are very difficult, requiring careful seasoning of the chemicals with sacrificial silicon nitride coated wafers [2]. This approach reduces tool availability and demands that pilot wafers are regularly available to be used for tank seasoning. In this paper, a method for controlling the etch rate of different materials in boiling H_3PO_4 by the addition of H_2SO_4 is presented for the first time. This approach allows the optimization of the etch selectivity independent of bath usage, eliminating the need for tank seasoning.

2-EXPERIMENTAL

The materials selected for the tests represent the films exposed to H_3PO_4 during the hard mask removal step in an STI isolation scheme. Namely, LPCVD Si_3N_4 as the hard mask, thermally grown SiO_2 as the pad oxide, undensified and densified APCVD SiO_2 as the trench filling material. The thickness of the various films was measured with a Thermawave Optiprobe tool. All tests were conducted on a Dai-Nippon Screen (DNS) autohood model WS-820C with chemical recirculation-filtration and deionized-water spiking for boiling control.

The effect of the bath temperature was investigated in the range 150 to 170°C. As the boiling temperature of H_3PO_4 is determined by the acid concentration [3], the temperature range investigated corresponds to H_3PO_4 solutions in the range of 84 to 89wt%, respectively. H_2SO_4 (98wt%) was added to the H_3PO_4 (85wt%) bath for a volume percent in the range of 0 to 75%. The nitride wafers received a deglaze for 30sec in 1:100 HF prior to the immersion in the H_3PO_4 tank. Fresh chemicals were used for each condition and the oxide etch rate tests were performed first to prevent data distortion by the nitride dissolution.

3-RESULTS AND DISCUSSION

H_3PO_4 and H_2SO_4 have very similar physico-chemical properties (Table I) and no exothermic reaction was noticed upon mixing them. The addition of H_2SO_4 to H_3PO_4 does not disturb either the recirculation-filtration system or the temperature controller of the autohood. Hence, no hardware modification is required for the testing and implementation of any mixture ratio, in the range tested in this work, on standard tools that were configured for pure H_3PO_4 processing. Moreover, it has been observed [4] that the addition of H_2SO_4 prevents the polymerization of H_3PO_4. The mixture remains water soluble, indicating that pre-mixed H_2SO_4:H_3PO_4 solutions can be delivered by standard bulk delivery systems.

The addition of H_2SO_4 to H_3PO_4 significantly reduces the etch rate of all types of SiO_2 films tested as can be seen in Figure 1. This effect happens for all temperatures. The impact of the H_2SO_4 addition on the Si_3N_4 etch rate is much smaller and consequently the selectivity between the removal of Si_3N_4 and SiO_2 can be tuned by the addition of a known volume of H_2SO_4 to H_3PO_4 (Figure 2). This allows the setup of a high selectivity nitride etch without the need of conditioning the bath with Si_3N_4 pilots, which increases the tool availability and reduces pilot cost. In the case where a maximum selectivity is desired without a significant reduction of the Si_3N_4 etch rate, a treatment in 1:1 H_2SO_4:H_3PO_4 mixture at 165°C is the best option within the process window investigated.

It is suggested that a similar effect to the one presented by Gelder and Hauser [1] to explain the impact of water on the etch rate of Si_3N_4 and SiO_2 in H_3PO_4 is present. In their experiments, it was observed that the increase of the water content at a given temperature causes an increase of the nitride etch rate while decreasing the oxide etch rate. This behavior was attributed to the hydrolyzation of the Si_3N_4 leading to the formation of some form of hydrous silica and ammonia, which would result in a higher etch rate. The low etch rate of SiO_2 was related to the fact that the stronger Si-O-Si bonds are not as easily hydrolized as the Si-N bond and the main effect in this case is the dilution of the acid. The addition of H_2SO_4 might result in a change in the boiling point of the solution requiring a higher amount of water relative to the H_3PO_4 content for the solution to boil at a given temperature. The more H_2SO_4 is added to the H_3PO_4 the more water is present relative to the H_3PO_4 content at the boiling point. The conclusion that the SiO_2 etch rate is reduced by the dilution of the H_3PO_4 is supported by the fact that the SiO_2 etch rate decreases proportionally with the H_2SO_4 addition. In addition to the change

in the relative water content, there is the effect of the H_3PO_4 dilution by the H_2SO_4. In the case of the Si_3N_4 etch the higher water content partially compensates for the H_3PO_4 dilution and little reduction in the Si_3N_4 etch rate is observed with the addition of H_2SO_4. On the other hand, in the case of SiO_2 etch both water and H_2SO_4 would act in reducing the etch rate leading to the observed nearly zero removal.

The stability of the 1:1 mixture was tested by running daily etch rate tests for a week on a mixture that was kept at 165°C. The results, presented on Figure 3, show no degradation of the Si_3N_4 etch rate performance during this period. The variation on the SiO_2 etch rate was attributed to the silica incorporation from the nitride wafers used in the experiment. This indicates that the 1:1 mixture remains stable for at least a week when kept at process temperature.

Bath loading with silicon is known to cause the change in the etch rate of SiO_2 and Si_3N_4 in H_3PO_4. In fact this effect is the origin of the seasoning procedure of H_3PO_4 by the etch of Si_3N_4 pilots [2]. The drawback to the silicon loading of the tank is that the etch rate changes throughout the lifetime of the bath. The behavior of the etch rate and selectivity of pure H_3PO_4 bath is compared to that of a 1:1 H_2SO_4:H_3PO_4 mixture. It is clear from the results shown in Figure 4 that the H_2SO_4:H_3PO_4 mixture not only provides the desired higher selectivity values on the fresh bath but it also shows negligible effect from silicon loading as opposed to the pure H_3PO_4. This may also be a result from the relative higher water content on the H_2SO_4:H_3PO_4 mixture. The effect of the water on the Si_3N_4 etch rate should be independent from the silicon loading and it might help to keep the nitride etch rate stable. On the other hand, the H_2SO_4:H_3PO_4 mixture reaches saturation faster, as less H_3PO_4 is available, and the SiO_2 etch is completely suppressed if a little amount of silica is present in the bath. The fact that the etch characteristics of the H_2SO_4:H_3PO_4 bath do not change significantly with the silicon loading allows the bath lifetime to be extended saving in chemical consumption and tool qualification downtime. Moreover, as the 1:1 H_2SO_4:H_3PO_4 mixture is stable for long periods of time, it could be bulk delivered to the autohood as a replacement for the pure H_3PO_4 eliminating the need to convert existing tools.

It has been shown that as the acid is loaded with silicon from the nitride etch silicate particles deposit on the wafers [5]. The use of a 1:1:5 NH_4OH:H_2O_2:H_2O SC1 clean at room temperature with megasonic agitation efficiently remove these particles for all mixtures tested. A neutral particle addition performance is achieved for bath loading of more than 650 wafers, which is equivalent to loading the bath with 14 grams of Si_3N_4, and a lifetime of more than 150 hours. The use of megasonic agitation seems to be key for the good particle removal performance of the SC1 step.

4-CONCLUSIONS

The addition of H_2SO_4 to H_3PO_4 has shown to be an effective method to control the etch rate of SiO_2 and Si_3N_4 in boiling H_3PO_4. This allows the optimization of the etch selectivity between these films and eliminates the need for bath seasoning of the H_3PO_4. A significant improvement in the bath lifetime is observed for a 1:1 H_2SO_4:H_3PO_4 mixture compared to pure H_3PO_4.

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Table I: Physico-chemical properties of phosphoric acid and sulfuric acid

	H_2SO_4	98wt% H_2SO_4	H_3PO_4	85wt% H_3PO_4
Density (g/cc)	1.841	1.84	1.834	1.69
Melting pt (C)	10.4	-	42.4	-
Boiling pt (C)	338	290	213	158
Mol. wt.	98.08	-	98.00	-

FIGURES

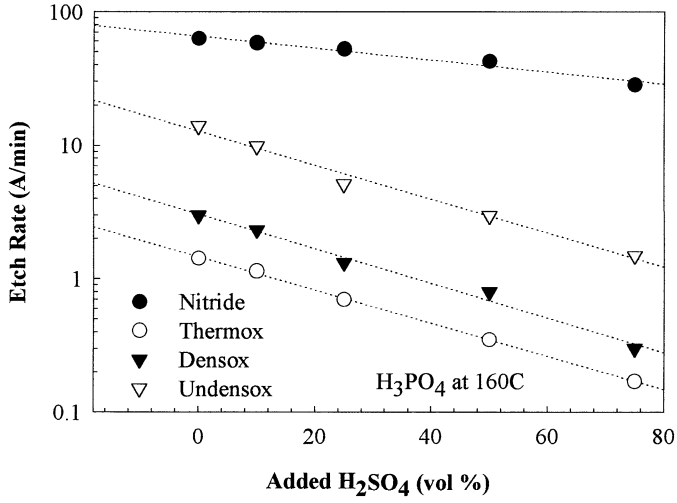


Figure 1: Etch rate in A/min of LPCVD Si_3N_4, Thermal SiO_2, Undensified and Densified APCVD SiO_2 in H_3PO_4 with various volumes of H_2SO_4 added. Process temperature was set at 160°C.

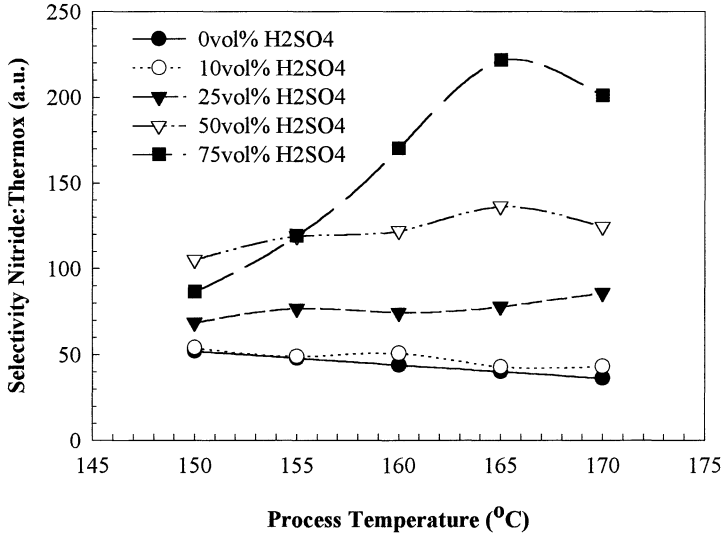


Figure 2: Selectivity between Si_3N_4 and Thermal SiO_2 etch in H_3PO_4 with various volumes of H_2SO_4 added. Process temperature was varied between 150 and 170°C.

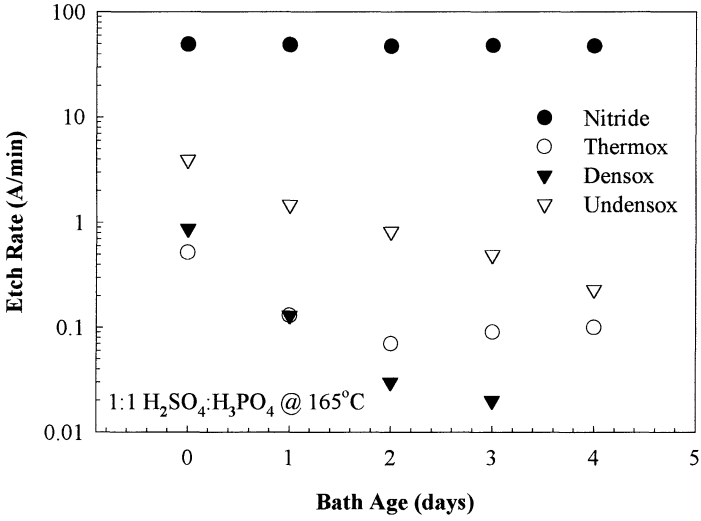
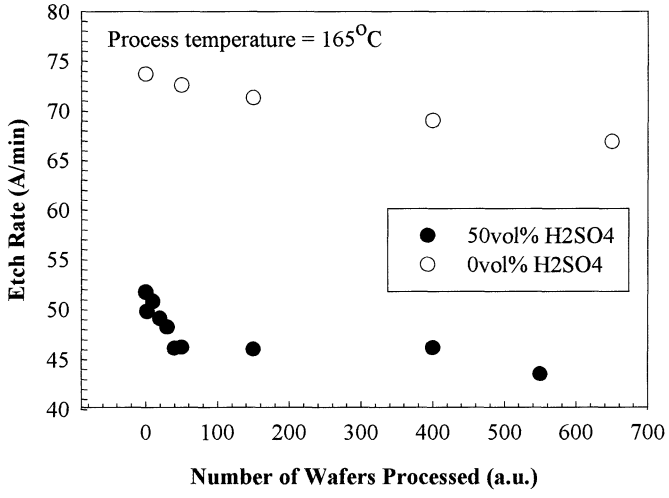


Figure 3: Etch rate of Si_3N_4, Thermal SiO_2, Undensified and Densified APCVD SiO_2 in 1:1 H_2SO_4:H_3PO_4 at 165°C as a function of the bath age.

a)



b)

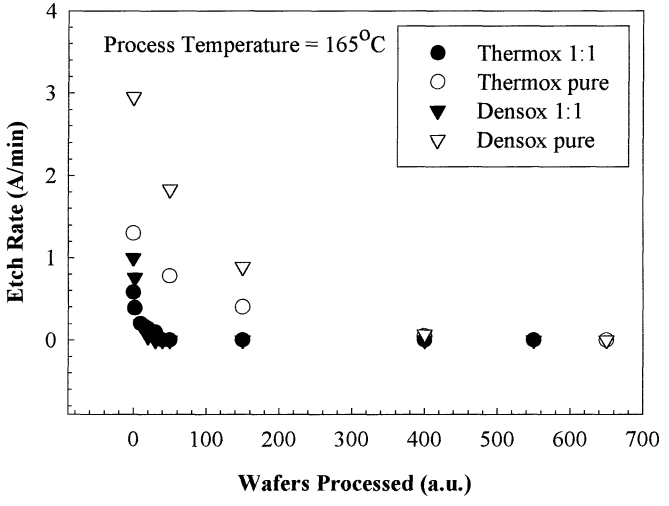


Figure 4: Etch rate of: a) Si_3N_4 and b) Thermal and Densified APCVD SiO_2 in pure H_3PO_4 and 1:1 H_2SO_4:H_3PO_4 at 165°C as a function of the number of nitride wafers stripped in the solutions.

EVALUATION OF OZONATED WATER SPRAY FOR RESIST CLEANING APPLICATIONS

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ABSTRACT

The application of [1]HydrOzone™, an ozonated water spray process, for resist removal purposes is discussed. The process efficiency is demonstrated for the removal of various advanced, non-ashed and post-ashed positive photoresist systems. Additionally, the process cleanliness and performance is considered. The process offers an environmentally friendly alternative for sulfuric acid based processing.

INTRODUCTION

The potential of ozonated (O_3) deionized (DI) water-based cleans for resist strip applications has been considered earlier [1, 2]. However, O_3 solubility in DI water, and mass transfer of O_3 to the wafer surface - thus reactivity towards photoresist - are the main limitations for successful implementation of these processes. Recently, a boundary layer controlled ozone concept has been introduced [3]. Since the O_3 solubility decreases with temperature, but its reaction efficiency increases with it, any optimized process should aim at maximizing the O_3 concentration at elevated temperatures. This can be done if one diverges from the standard immersion based processes.

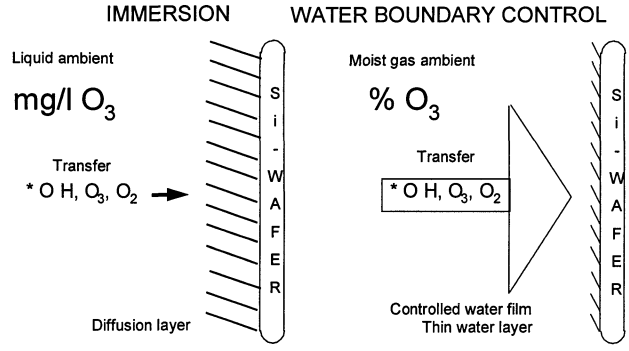

Figure 1 Illustration of a Boundary Controlled Ozone Process

The novel ozone cleaning concept, is shown in Figure 1. In this concept, only a thin layer of water is allowed on the wafer while the O_3 gas ambient maintains a continuous supply of high concentration O_3. The thin layer reduces the diffusion limitation and allows the short living reactive O_3 components to reach the wafer surface in abundance.

[11] HydrOzoneTM, is a registered trademark of Semitool Inc., Kalispell, USA

This concept can be simulated in various ways such as controlled spinning and water rinsing in spray tools or water adsorption by exposure to heated DI water vapors. Implementation in a spray processor, i.e. HydrOzone^{TM}, will be discussed with respect to resist strip rate as well as process performance and cleanliness.

EXPERIMENTAL

Experiments were performed on a Semitool Magnum tool, which is a fully automated spray process platform. During the process, hot DI water spray and ozone gas are simultaneously present inside the chamber, while the wafers are spun at a high rotational speed. All testing was done in the spin rinse dryer (SRD). This stainless steel chamber is not optimal, as the combination of hot water and ozone is seen to produce a metal signature over the longer term. However, this type of chamber allowed to run processes at higher rotational speeds (up to 1800 rpm). The process chamber is equipped with two manifolds of nozzles, one for introducing an aqueous solution at elevated temperatures (DI water with or without additives), the other for dry ozone gas. Ozone gas is produced by a Sorbios SEMOZON 90 generator. To maximize the residence time of the ozone gas in the process chamber and to minimize losses through the exhaust, the chamber is equipped with an exhaust valve. All experiments were run in a single-pass mode. The water is supplied from a temperature controlled tank and is used only once and drained after the process.

The process was evaluated for various advanced I-line and deep ultraviolet (DUV), non-ashed and post-ashed positive photoresist systems (also ion implanted). The experimental plan included combinations of resist with antireflective coating (ARC), as well as combinations of resist with HMDS. Optimum process parameters were obtained from a thorough Design of Experiments (DOE); the key range of values is listed in Table I. Strip rate, time to cleanliness, particles, metals, and organics were evaluated, and the results were compared with the standard sulfuric-based processes. Also the effect on the resist strip rate of OH-radical scavenger (i.e. acetate [3]) addition has been evaluated.

Table I Key Process Parameter Values From Design of Experiments (DOE)

Experimental Setting	O_3 liters/min O_2	Rotation Speed RPM	Temperature °C	DI flow liters/min
High	10	1800	85	10
Medium	6	1300	75	7
Low	2	800	65	4

To evaluate the resist strip rates, wafers were measured by spectroscopic ellipsometry on a Spectramap SM300. Based on the resist layer thickness before and after ozone processing, the strip rate can be derived. A Censor ANS100 light scattering tool was used to measure haze and light point defects (LPDs). Total reflectance X-ray fluorescence spectroscopy (TXRF) was used to detect metallic impurities on silicon surfaces using an Atomika 8010 instrument and a wafer surface preparation system (WSPS, GeMeTec) to improve the detection limits. ToF-SIMS was used to evaluate the process for cleanliness in terms of organics. Measurements were made with an IONTOF-IV instrument using an Ar^+ electron impact primary ion source.

Effect of O_3 Flow and DI Temperature on the Strip Rate

The contour plot indicating the DOE model-based strip rate dependency of DI temperature and O_3 flow at optimum settings for the other variables is shown in Figure 2 for I-line and implanted resist, respectively. Responses are quite similar. For all resists, a gain in strip rate of more than a factor of 2 is achieved when changing to the optimum process conditions in the DOE window. However, although the strip rate for all three resist types increases with a higher O_3 flow and DI temperature, it is far less for implanted (and DUV) resist. The maximum conditions are reached at an O_3 flow of 10l/min and a DI temperature of 85°C, representing a model-based strip rate of 563 nm/min for the I-line resist, of 361 nm/min for the implanted resist, and only 223 nm/min for the DUV resist (not shown).

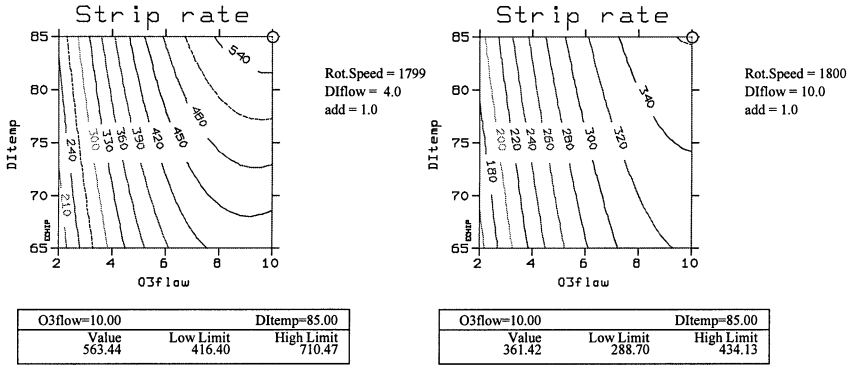

Figure 2 Impact of O_3 Flow and DI Temp. on Resist Strip Rate for a) I-line Resist and for b) Implanted Resist

Effect of Rotational Speed (and DI Flow) on the Strip Rate

A crucial factor for the efficiency of ozonated chemistries is the establishment of a thin water layer on the wafer surface that allows maximum diffusion of O_3 and its byproducts to the resist layer, and reaction products away from this layer. In a spray processor, this concept is achieved through rotational action of the wafer. Likely, the rotational speed influences the strip rate of the process. Therefore, a high range of rotational speed variation in the DOE was selected with rotational speeds between 800 rpm and 1800 rpm. From the DOE, it was found that the rotational speed was not always a significant factor and definitely not an influential factor. However the cross term with DI flow (also influences the water layer thickness in a spray processor) positively affects the strip rate.

Only at a fixed DI flow, the effect of rotational speed can be separated and its magnitude evaluated. The strip rate after the standard process was determined for all resists under consideration and is visually represented in Figure 3. For the DUV resist, the strip rate increases from about 75 nm/min to about 150 nm/min in the range between

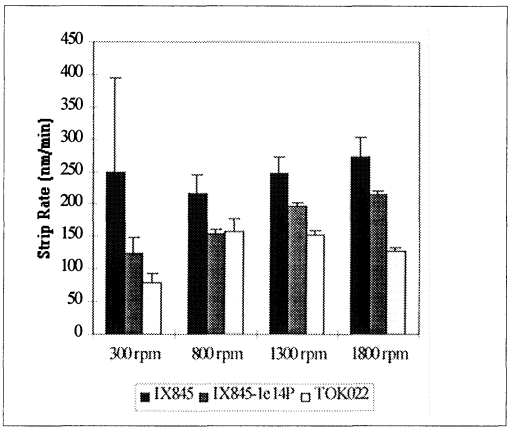

Figure 3 Average strip rates for different resist types as a function of rotational speed.

300 and 800 rpm. The strip rate for the implanted resist steadily increases with the rotational speed from about 120 nm/min at 300 rpm to 210 nm/min at 1800 rpm, whereas the strip rate for the I-line resist seems almost independent of the rotational speed. However, these presented strip rates are average data over the full wafer; at 300 rpm there is large variation between the strip rate in the center and at the edge (virtually no strip), explaining the large error bars for this condition.

Impact of Additives on the Strip Rate

For all the resists under study, an effect of the addition of an OH-radical scavenger on the strip rate was observed. The additive concentration in DI water was varied between 0, 0.5, 1, and 2 milli molar of NH_4OOCCH_3 (Ac). The settings for the other variables were kept fixed at intermediate settings (except DI temperature at maximum). The strip rate was determined for some resists under consideration and is visually represented in Figure 4. For the implanted I-line and DUV resist, the impact of the scavenger is small, but noticeable. Under the parameter conditions studied, an increase of about 20-25% is achieved. Moreover, an improvement seems to scale linearly with the concentration of the additive. However, for the I-line (IX845) resist a factor of almost 2 in strip rate improvement can be achieved by adding 1 milli molar of (Ac). At higher concentrations, the effect seems to level off. One can argue that in those cases the resist strip rate enters a rate-limited regime and therefore no further improvement can be obtained with the addition of OH radical scavengers.

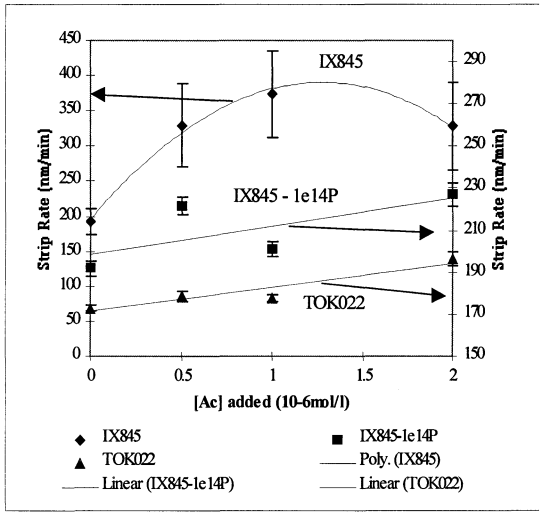

Figure 4 Average strip rates for different resist types versus additive concentration.

Process Reproducibility

The resist strip process reproducibility can be evaluated by considering the ratio of the process strip rate for one wafer vs. the average strip rate for all wafers at the DOE settings under consideration. Figure 5 plots this ratio for some of the resists under consideration, as well as the 10% and 20% variation levels. Except for a few outliers, the reproducibility is better than 10% for all resists.

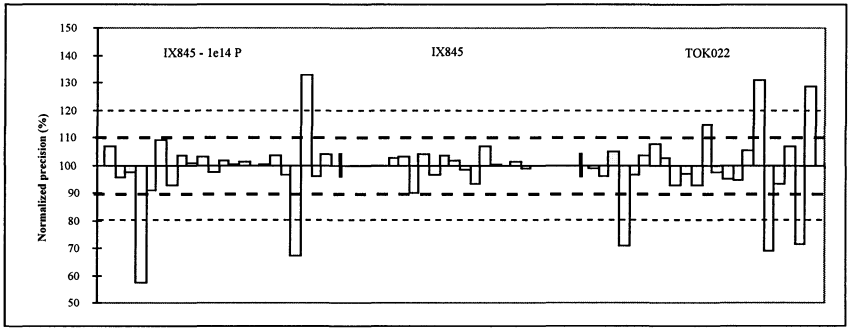

Figure 5 HydrOzone™ reproducibility for various resists under consideration

Impact of the Type of Resist

For cleaning processes, an important parameter is the process time until cleanliness. It can be assumed that this process time is the simple numerical quotient of the initial resist layer thickness (nm) divided by the average strip rate (nm/min) for the resist under consideration. Strip rate results after a two minutes HydrOzone™ process are shown in Figure 6. Strip rates vary from as low as 100 nm/min to almost 600 nm/min, depending on the resist type. This would indicate process times to cleanliness ranging from 2 to 5 minutes. However, practical observations are slightly different. At first, the resist removal process can be a quite non-uniform process (IX845, APEX). Therefore, process times until cleanliness are defined by the wafer areas that strip the slowest. Additionally, as is the case for the TOK022 resist on AR2, the applied DUV resist strips readily without difficulties, but the process hardly affects the anti-reflective coating (ARC). Addition of low quantities of ammonia however, allows complete removal of both resist and ARC layer, while it does not affect the resist strip rates negatively. Finally, the initial resist strip rate might also be lower than the actual strip rate for a full cleanliness process (UV6). Nevertheless, after a 6-minute process, all wafers except the UV6 wafers were clean (8-minute process required).

The latter observation of a slower initial strip rate also applies in the case of implanted resists. As a consequence of the implantation process, the resist top layer becomes hardened. Ultimately, at high implantation doses (above $1E^{14}$ at/cm^2) the crust becomes so cross-linked that neither ozone-based cleaning nor sulfuric-based processes are successful. To evaluate the impact of implantation element, UV6 resist-coated wafers were implanted at a $5E^{13}$ at/cm^2 level with either boron, phosphorous, or arsenic. Strip rates are shown in Figure 7.

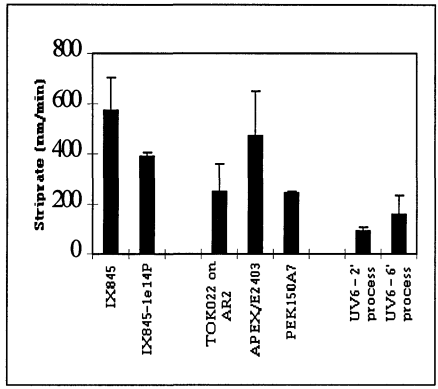

Figure 6 Average strip rates for after 2' HydrOzone™ processing for the various resists .

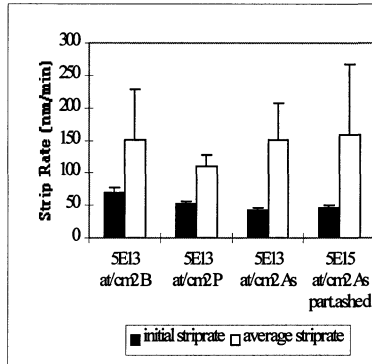

Figure 7 Initial and average resist strip rate for $5E^{13}$ and $5E^{15}$ at/cm^2 As implant UV6 resist (partly ashed).

The difference in initial strip rate and average strip rate, indicates the influence of the hardened top layer on the strip rate. As far as the impact of implantation element is concerned for the $5E^{13}$ at/cm^2 levels, the differences are nominal. Additionally, high dose implanted resist wafers (UV6 $5E^{15}$ at/cm^2 As) were processed. The hardened top layer was partly removed in a separate process (dry ashing). If so, the resist can readily be removed with an ozone process, although still some impact can be seen from the lower initial strip rates. Overall, visual cleanliness for all low dose implant wafers is achieved after a 6-minute process, whereas for the high dose implant wafers (after ash) process times up to 10 minute are required (to achieve particle cleanliness).

Process Cleanliness

At optimum DOE conditions, the process cleanliness was evaluated. Particle performance is presented in Figure 8. Wafers were coated with IX845 I-line resist and exposed to either: SPM, SPM/APM, HydrOzone™, or HydrOzone™/APM. By taking the initial particle levels into account, cleanliness can be expressed in terms of particles/defects added during the processing. It can be seen that the APM cleans can be considered particle neutral, whereas both the SPM and HydrOzone™ process are comparable in terms of particles added (or not removed) during processing. This indicates the necessity of an NH_4OH based clean-up after a wet oxidative clean for good particle performance.

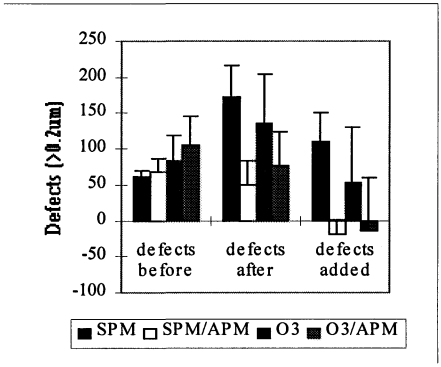

Figure 8 Defect Levels (>0.2μM) After Split Lot HydrOzone™/SPM On IX845

Metal cleanliness of the resist-cleaned wafers was evaluated using D-TXRF and VPD-DC-TXRF. Neither of the cleaned resist wafers under consideration did show contamination levels that allowed detection with D-TXRF (measured at three points/wafer). Therefore, it was decided to pre-concentrate the metal contamination by means of the Vapor Phase Decomposition-Droplet Collection procedure, thus improving the detection limits by a factor of almost 300 (depending on wafer size and element). TXRF results in Table II were obtained after split lot processing on IX845 resist-coated wafers. Split lots using SPM, SPM/APM, HydrOzone™, or HydrOzone™/APM were performed. For all wafers and all cleaning splits, metal contamination after processing is below detection limits. This indicates that the performance between ozone-based cleans and sulfuric-based cleans in terms of metal cleanliness is within comparable boundaries. Metal cleanliness was also evaluated after processing blanket resist wafers (UV6) exposed to various implantation processes. No contamination was observed, neither for the various implantation elements nor for the various implantation energies. Also, the partly ashed HDI As implanted wafers (on bare silicon) did not show elevated metal contamination levels after ozone processing.

Table II: Metal Cleanliness (10^{10} at/cm^2) After Split Lot HydrOzone/SPM on IX845 I-line Resist Coated Wafers

	S	Cl	K	Ca	Ti	Cr	Mn	Fe	Co	Ni	Cu	Zn	Br
						SPM-processing							
SPM	92.8	89.0	1.0	-	-	-	-	-	-	-	-	0.1	1.1
SPM - APM	103.5	101.5	0.9	-	-	-	-	-	-	1.4	-	0.3	1.3
						HydrOzone-processing							
O3	104.6	90.2	-	-	-	-	-	-	-	-	-	-	1.1
O3 - APM	91.2	63.5	4.2	0.5	-	-	-	1.4	-	0.4	0.0	0.1	0.9

ToF-SIMS was used to evaluate the cleanliness of SPM, SPM-APM, Hydrozone™ and Hydrozone™-APM processes in terms of organic contamination using wafers coated with I-line resist. As a reference, a standard pre-gate cleaned wafer (SPM-dHF/DHCl-O_3/HCl-Marangoni Dry) was prepared and stored in a clean-room wafer box for a length of time equal to the storage time until ToF-SIMS analysis for the resist cleaned wafers. Using these results for reference, distinction can be made between organic residues that originate from the cleanroom background, and organic residues remaining after the various resist cleans. Figure 9 displays the relative intensities (to reference wafer) of several peaks representative of different organic compounds. Very little differences exist between the various splits. Therefore, all wafers are considered equally clean or cleaner than the reference cleaned wafer. The exceptions are: (1) sulfate peak is much more intense after an SPM clean, which is straightforward, (2) Na intensities are higher for the SPM based cleans, (3) Mg and Al intensities are higher for the APM based cleans.
However, neither of the organic clusters (and compound classes) are more intense than on the reference cleaned wafer, nor is the cleanliness after any of the ozone processes worse than after any of the sulfuric based cleans. The efficiency of the ozone process is thus well demonstrated for this I-line unimplanted resist. An identical comparison was performed for the DUV resists. Little or no differences in cleanliness between the three types of resist is observed, as can be observed in Figure 10.

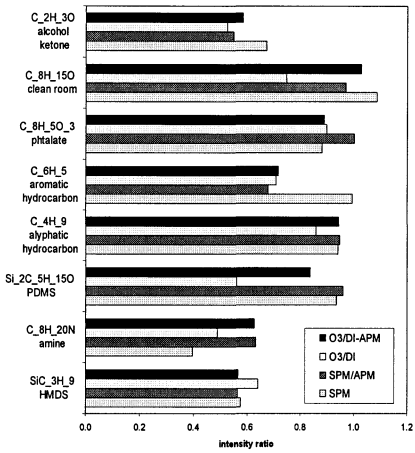

Figure 9: Normalized ion intensities for different cleans of IX845

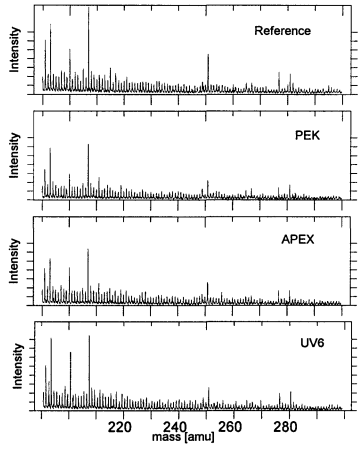

Figure 10: ToF-SIMS spectra of the ozone cleaned DUV unimplanted resists.

CONCLUSIONS

The HydrOzone™ process is an ozone/water based process capable of removing photoresist. Based on a DOE evaluation, O_3 flow, DI temperature and the cross term of DI flow with rotational speed were identified as the contributing factors to the resist strip rate. Also the nature and treatment of the resist influenced the results. General recommendations for an optimum process are high O_3 flow, high temperature, high rotational speed and intermediate DI flow levels. The addition of OH-radical scavengers also enhances the process efficiency. In terms of process cleanliness, the DOE optimized process performs identical to standard sulfuric based chemistries.

ACKNOWLEDGEMENTS

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PHOTORESIST STRIP PROCESS USING OZONE DIFFUSION THROUGH A CONTROLLED AQUEOUS BOUNDARY LAYER

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ABSTRACT:

The application of ozone dissolved in DI water for the replacement of sulfuric acid/ozone (SOM) and sulfuric acid/hydrogen peroxide (SPM) solutions in photoresist removal has been limited due to its relatively low strip rate. By diffusing ozone through a controlled aqueous boundary layer, rather than dissolving ozone in the aqueous film, this limitation can be overcome. Resultant strip rates approximately an order of magnitude higher than dissolved ozone systems have been achieved, rendering the process economically viable for semiconductor device manufactures.

INTRODUCTION:

Photoresist strip using ozone dissolved in water at low temperatures has generally shown higher strip rates than dry ozone ashers at temperatures less than 100C. Ozone ashers at elevated temperatures have significantly higher strip rates. It is thought that the water aids in the attack of ozone on photoresist by partially hydrolyzing the bonds in the photoresist. However, ozone, like all gases, has a limited solubility in aqueous solutions. At standard pressure and temperatures near ambient, ozone saturation occurs at around 20 ppm. Ozone solubility in water increases dramatically with decreasing temperature, to a maximum of a little over 100 ppm at temperatures approaching 0C and drops to almost zero at temperatures approaching 60C at 1 standard atmosphere. While increasing ozone concentration increases the kinetic reaction rate, a decrease in temperature simultaneously suppresses the rate.

The immersion process has been characterized and reaction mechanisms described **[1]**. However, the achieved strip rates are relatively low due to the low solubility of ozone in water as well as the suppression of reaction kinetics due to the low temperatures needed to maximize the ozone solubility. An optimized aqueous ozone photoresist strip process would maximize both the temperature and the ozone concentration available for reaction at the organic film interface.

EXPERIMENTAL:

The system used in these experiments was an on-axis chemical spray processor manufactured by Semitool, Inc. A simplified fluid-flow diagram is shown in **Figure 1**. The process system used for the bulk of the experiments reported here used a PFA Teflon® process chamber and rotor. The rotor was interchangeable in order to process either a 25 wafer load of 150mm wafers using a Fluroware® A190-60M cassette or 200mm wafers using an A182-90 cassette. Additional tests have been performed in a stainless steel process chamber, and in a system capable of processing 50-wafer load

sizes, in both Teflon® and stainless steel. Implementation in a single-wafer process platform has also been achieved.

The boundary layer controlled process was accomplished in the following manner: While the wafers were rotated in the chemical process chamber (CPC), a temperature controlled DI water stream was sprayed on the wafer surface, either from a point-of-use (POU) heater or a recirculated tank. Simultaneously, ozone was introduced into the process chamber, either through the same spray manifold as the liquid, or, preferentially, through a separate manifold. This process is marketed commercially as the Semitool HydrOzone™ process.

Photoresist strip rates reported herein are averages of 9-point measurements made on a Nanospec 4150 film thickness gage. The average photoresist thickness delta was divided by the strip time to calculate a strip rate.

Test wafers were also processed in order to establish metal ion contamination, residual organic levels, surface roughness and device parameters.

RESULTS AND DISCUSSION:

Figure 2 illustrates the impact that the temperature and rpm has on the photoresist strip rate. The data shows that the strip rate increased both with RPM and with temperature. Such could not be the case if ozone solubility in water was the controlling mechanism. As mentioned previously, it is thought that the increase in temperature results in an increase in molecular energy, thereby promoting reaction kinetics. The increase in RPM has been correlated with the DI water delivery flow and spray configuration, indicating that these parameters define the surface boundary layer which acts as a diffusion barrier for ozone reaching the photoresist surface. Thinning this boundary layer enables the ozone to diffuse to the surface more readily, resulting in a higher strip rate. Subsequent tests have shown a continuing increase in the strip rate with RPM, however, practical constraints impose limitations on this variable.

A series of tests was run to compare the strip rate of a process using ozone dissolved in water, applied in spray and immersion systems. It appears that this method of delivery is controlled by the dissolved ozone concentration in the water, and the strip rate is unaffected by the aqueous ozone delivery method, achieving a maximum of about 70 nm/minute. This is further supported by the strip rate observed in a conventional spray system at elevated temperature. Since the ozone has little solubility in hot water, the predicted reduction in strip rate is observed. However, when the surface boundary layer is thinned by increasing the speed at which the wafers are spun in the spray process chamber, the strip rate is observed to increase significantly. Since the ozone solubility in water at 90C would not have changed, it becomes apparent that a different mechanism must be responsible for the increased strip rate. It is proposed that this mechanism consists of diffusion through the boundary layer as illustrated in **Figure 3**.

The diffusion of ozone gas through the liquid boundary layer on the substrate surface in effect creates a disconnect between the ozone solubility and strip rate. Such a

disconnect would promote the use of elevated temperatures which would not only support higher diffusion rates but also provides a significant increase in the Boltzman distribution of molecular energy, thereby increasing the reaction rate. This may be characterized by the familiar *Arrhenius Equation.* Thus, an increase in temperature may result in a significant increase in the rate constant.

Studies have been performed to characterize the effect of hydroxyl radicals in solution resulting in the decomposition of ozone **[2, 3]**. As a further evidence of the unique mechanisms defining the thin boundary layer process, tests were run to evaluate the impact of hydroxyl radicals on the photoresist strip rate. Solutions of ammonium hydroxide ranging from 0% to 5% (weight) were prepared and used as the aqueous media in the strip process. No change in strip rate was observed. This indicates that the diffusion rate of ozone through the thin boundary layer combined with the reaction rate of ozone with photoresist is significantly faster than the hydroxide initiated decomposition of ozone in the boundary layer. More recent arguments have been posed asserting that the interaction of ozone with water will form hydroxyl radicals, which is a key step in the organic oxidation mechanism. In the controlled boundary layer process described in this paper, the addition of ammonium hydroxide to the aqueous solution had no effect on the observed strip rate, although minute residues appeared to have been more readily removed in the high pH solution. Corresponding tests were run wherein HCl was added to the aqueous solution and the impact on the photoresist strip rate was evaluated. Again, no impact was observed, indicating that the hydroxyl or hydronium ion concentration has no effect on the controlled boundary layer ozone strip process.

Figure 4 shows strip rate data from various photoresist types and treatments. Different resist types appear to show strip rate variations, but in general, positive resist strip rates in the range of 500 - 800 nm/minutes are typical in a batch processor, with results in the laboratory exceeding 1200 nm/minute in batch, and in excess of 2000 nm/minute in a single-wafer process chamber. These rates are for the removal of the photoresist bulk. As the photoresist clears, the rate appears to slow simply because many regions are fully stripped and minute residues remain to be cleared. A manufacturing process should be configured for approximately a 100% "over etch." No significant difference in strip rate was observed between 150mm wafers to 200mm wafers. While batch size appeared to have a slight impact on strip rate, the actual chamber volume had a more significant effect. This is thought to be due to the time required to approach an equilibrium concentration of ozone within the process chamber. Ion implanted resist at dosages 1E15 or greater have not been successfully stripped without additional treatment such as partial ashing of the surface layer. Negative photoresist and some polyimide films generally show much lower strip rates, rendering them unacceptable for aqueous ozone strip processes.

Particle monitors were coated with photoresist and processed in the HydrOzone™ strip. Summary particle results were essentially neutral and are shown in **Figure 5**. To further verify the complete removal of both photoresist and HMDS layers, test wafers were processed through various strip processes and analyzed using XPS. Comparison to virgin silicon was made, with results depicted in **Figure 6**, showing no residual organic

signature and results comparable to either a plasma ash or SPM strip process. Metals analysis via TXRF and VPD ICP-MS was also neutral.

In order to compare the cleanliness potential of the controlled boundary layer process to more conventional cleans, engineers at ST Microelectronics in Agrate, Italy prepared gate oxide test structures. Splits were performed between a conventional cleaning process consisting of sulfuric peroxide (SPM) followed by ammonium hydroxide, hydrogen peroxide, water (APM) and hydrochloric acid, hydrogen peroxide, water (HPM). Both cleans were performed in on-axis spray tools. The results are shown in **Figure 7**. The "conventional" clean shows the characteristic breakdown voltage curve, having a definite slope to the vertical portion of the curve. The controlled boundary layer clean (HydrOzone™) is distinctly different in that the slope of the vertical portion of the curve approaches infinity, coupled with a breakdown voltage approximately 10% higher than the control group. The elimination of chemical residues is thought to be responsible for the increase in dielectric breakdown strength. Various electrical parameters measured on device wafers were similar between the two splits. Device yield has also been evaluated in the manufacturing line, where SPM strip processes were replaced with the HydrOzone™ strip process at all steps in the process flow. No significant yield difference was observed. Additionally, beta tests conducted in device fabrication facilities in three locations in Europe have reported a process capability index (Cpk) for the controlled boundary layer strip process to be equivalent to the Cpk for SPM or SPM/APM processes. The process has also been used to successfully replace strip applications using fuming nitric acid.

CONCLUSIONS:

The controlled boundary layer strip process has been shown to have a unique reaction mechanism compared to conventional aqueous ozone processes which rely on ozone solubility in the aqueous media. The mechanism appears to rely on diffusion of ozone through rather than solubility in the thin boundary layer. This permits the use of much higher temperatures than conventional aqueous ozone processes. The diffusion rate appears to be fast enough that hydroxyl radicals, thought to play a key role in the decomposition of ozone, do not have an adverse impact on the oxidation capability of the process. The process has been demonstrated on a broad variety of resist types and treatments, and has been successfully used to replace SPM and SPM/APM processes in device fabrication lines.

ACKNOWLEDGMENTS:

The authors would like to acknowledge the assistance of ST Microelectronics TPA Agrate 6" fab (F3) and production staff for supporting the installation and testing performed on the spray processor in the fabrication line, and IMEC (Leuven, Belgium) for various confirmation tests of data reported herein.

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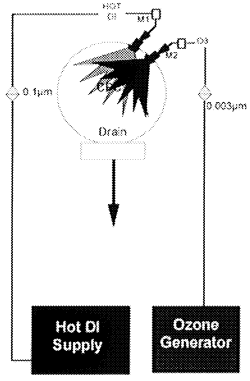
Figure 1: HydrOzone™ Test System



Note: shown is the case where hot water is single use. However, hot DI can be reclaimed, filtered and reused to decrease DI usage even more.

Figure 2: RPM and Temperature Effect On Photoresist Strip Rate

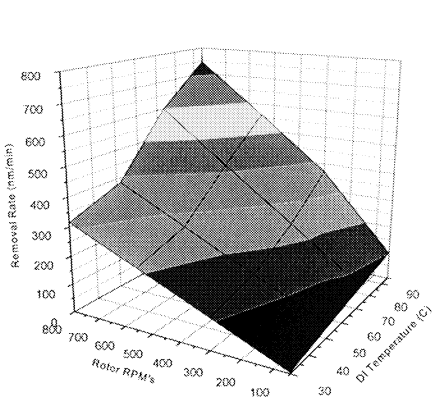
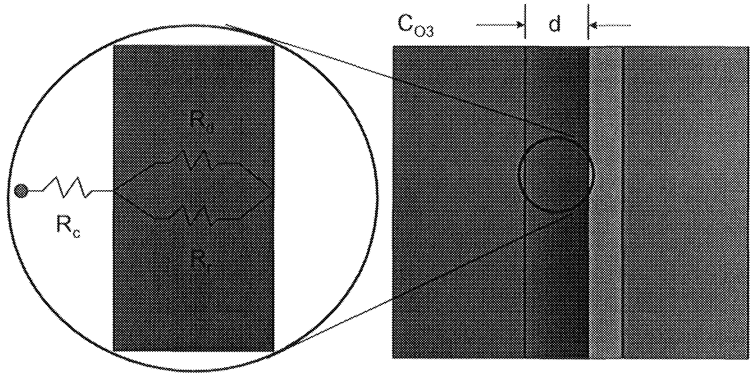


Figure 3: Diffusion Model



R_c = convective mass transport resistance of O_3 at BL-ambient interface
R_d = diffusion resistance for transport of O_3 through BL
R_r = resistance of transport due to reaction into benign/ineffective species

Figure 4: Strip Rates on Various Types and Treatments of Photoresist

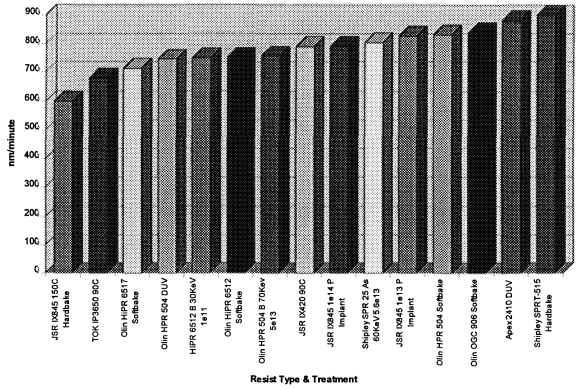


Figure 5: Particle Performance after aqueous ozone strip.

- Average (absolute) Particle Counts on HydrOzone™ Photoresist Stripped Wafers. 1.25 microns of Shipley SPRT 510 I-line resist. Treatments included softbake, hardbake, DUV at 230C and ion implant.

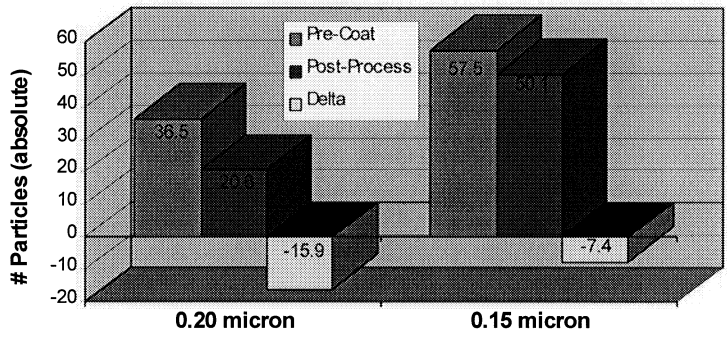


Figure 6: XPS Analysis. A comparison of various strip technologies with photoresist over HMDS.

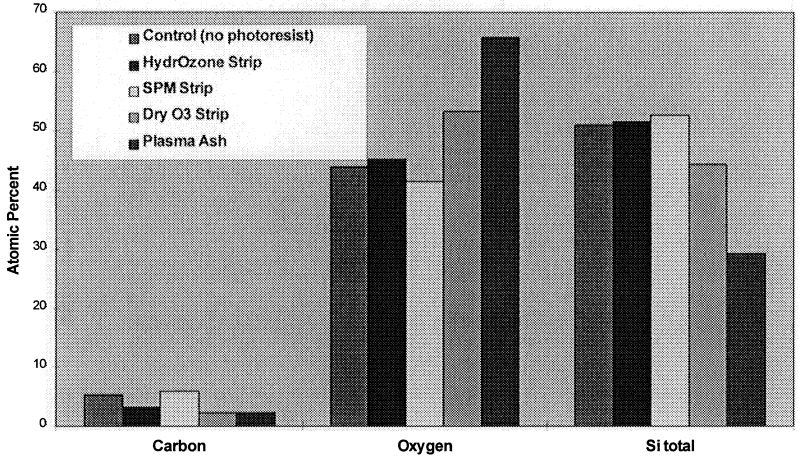
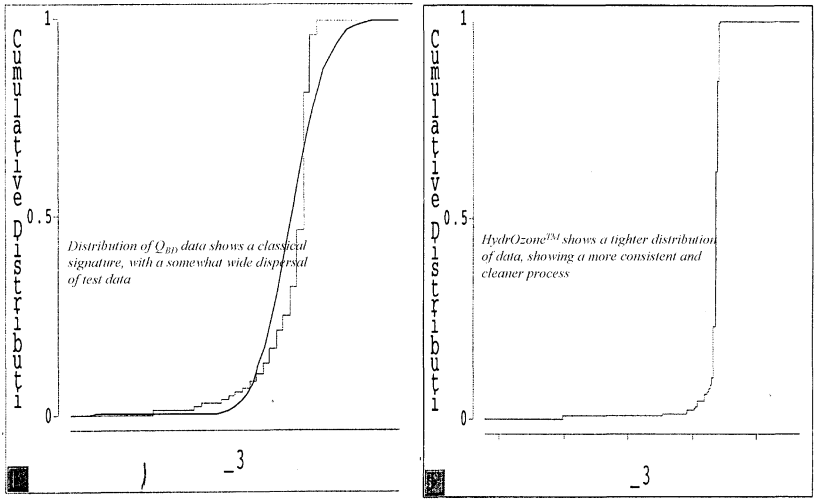


Figure 7: Oxide Breakdown Distribution: SPM>APM>HPM vs. HydrOzone™



A MECHANISM FOR THE SILICON OXIDE GROWTH BY OZONATED SOLUTIONS

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ABSTRACT

The oxidation of silicon using ozonated DI-water solutions was investigated as a function of several parameters: reaction time, pH, ozone concentration, temperature and influence of anions. The oxidation of silicon was dependent on ozone concentration especially near neutral pH. Lowering the pH leads to a less pronounced concentration-dependence with no specific anion-effect for Cl^- or NO_3^-. No temperature effect on the oxidation rate was found between 20 to 50 °C.
Various oxidation models were evaluated and the Fehnler-expression represents the experimental data fairly well. As hypothesis is proposed that ozone dissociates at the SiO_2/liquid-interface in a one-step reaction forming the oxidizing species, possibly O^-. This radical-ion diffuses through the SiO_2 layer under the influence of an electric field which develops over the oxide layer. The field-imposed drift is the limiting factor in the oxidation process. The bulk chemistry of the ozonated solutions is of no relevance for the oxidation rate of silicon.

INTRODUCTION

The use of ozone in wet and dry cleaning processes of silicon wafer surfaces is a common practice for a few years now. Some of these applications are already implemented in cleaning processes. In the wet processes, ozonated solutions are used for the removal of organic contamination [1], resist strip [2] and the oxidation of silicon surfaces [3].

Concerning the oxidation of silicon by means of oxygen, a few oxidation models are available, namely the Deal-Grove model (thermal oxidation) [4], the Cabrera-Mott model (oxidation of metals) [5] and the Fehnler-Mott theory[6] which is an expansion of the Cabrera-Mott model. It will be checked to what extend these models might be applicable to oxidation of silicon by ozone in solution.

The study described in this paper is a detailled look into the growth kinetics of the silicon oxide layer by ozonated DI-water solutions. The influence of several experimental parameters was investigated such as the oxidation time, pH, ozone concentration, nature of the anions and temperature.

The parameter pH needs to be controlled in all experiments involving O_3: not only the ozone solubility in the water is pH-dependend [7], but also its decomposition rate,

especially in neutral conditions and at high pH [8-10]. Moreover the pH is an important parameter controlling the possible build-up in the solution of radicals which are formed as products or intermediates of the complex decomposition mechanism of ozone [11-13]. These radicals could be the precursor for the oxidation process and their concentration is most certainly pH-dependent.
Besides the influence on the oxide growth of the process parameters mentioned above, also some silicon oxide growth mechanisms will be checked.

EXPERIMENTAL

Silicon wafers (Wacker Siltronic, p-type, B-doped, Cz, <100>) were used for the oxidation experiments and for the AFM-measurements. In the latter case epitaxial wafers (0.008-0.020 Ωcm, 4 μm thickness and 8 x 10^{15} (P/B) dopant level) were oxidized. HNO_3 70 v/v %, HCl 37 v/v %, HF 49 v/v % (all Ashland Chemicals, Gigabit grade) were used to either acidify the solution or to etch the SiO_2-layer away. DI-water was ultrapure quality (18 MΩ cm). Ozone was generated by a Sorbios ozone generator operating at a current of 2.5 A and an O_2 flow of 2 l/min. The ozone concentration in the solution was measured with a Orbisphere ozone sensor which measures the ozone concentration electrochemically. Before each oxidation step the wafers were exposed to a cleaning sequence of SOM ($H_2SO_4/O_3/H_2O$) - dHF/dHCl - O_3/dHCl - Marangoni dry, resulting in an hydrophylic surface [3]. Prior to the oxidation experiments the wafers were given a HF-dip (2 %). Subsequently the hydrophobic wafers were immersed in the ozonated solution for a time t ranging from 6 seconds to 20 minutes. The oxidation was performed in a static tank with no ozone bubbling at the time of oxidation. Then the reoxidized (hydrophylic) wafers were rinsed in an overflow rinse tank for 30 seconds followed by a drying procedure in the Semitool spin dryer PSC-101. Typically oxide layers of a few Angström thick were grown.
The oxide layer thickness was measured using the Molybdenum Blue method [14].

RESULTS AND DISCUSSION

Influence of the Oxidation Time and pH

Silicon wafers were oxidized at pH 4.6 and 1.2. The oxide layer initially grows fast and levels off at longer reaction time as is illustrated in figure 1 for a solution containing 1 mg/l ozone. An similar growth profile has also been seen in other studies [15,16]. A few experiments were performed for oxidation times till 40 minutes but the oxide layer thickness t_{ox} stayed nearly constant compared to the 20 minutes value.

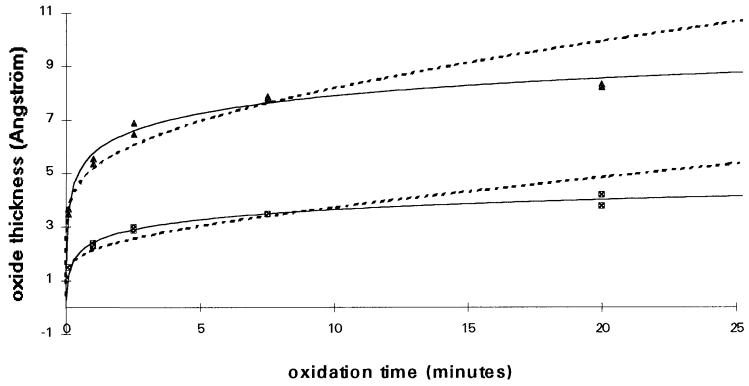

Figure 1: Growth profiles of SiO_2 under the following experimental conditions: 1 mg/l ozone, T = 22°C and pH 4.6 (■) and pH 1.2 (▲; nitric acid). Solid lines represent the fit based on the Fehnler expression and the dotted line the Cabrera-Mott formalism.

Since no model is available which describes the oxidation of silicon by ozone in solutions, some of the models derived from oxidation studies in the gaseous phase were applied to these experimental data. One of the most prominent models to test is the so-called linear-parabolic model of Deal-Grove ($t_{ox}^2 + A \cdot t_{ox} = B \cdot (t + \tau)$) which is based on a diffusion-controlled oxidation process. No values of the parameters A and B could be derived by numerical procedure since the convergence criterium of the fitting routine was not met. The fact that the Deal-Grove formalism can not be applied may be seen as a first indication that the transport of oxidizing species through the SiO_2-layer is not solely diffusion-controlled. In this way the role for uncharged species like oxygen or ozone as the oxidation precursors becomes unlikely. This can already be expected based on estimations of the diffusion rate of uncharged species.

Some authors claim the applicability of the Cabrera-Mott (CM) formalism ($\frac{1}{t_{ox}} = C - D \cdot \ln t$) for the growth of oxide layers in ozonated solutions [16]. When this formalism was applied t_{ox} was overpredicted at long oxidation times (figure 1). In addition an argument against the CM-formalism is that most probably no cation migration occurs during the oxidation of silicon. It is rather the oxidizing species which migrates towards the SiO_2/Si-interface. Isotope marker experiments for gas phase oxidation indeed have shown that O^- migrates through the oxide layer towards the silicon bulk and not silicon-atoms towards the SiO_2-gas interface [17].

Finally when the experimental data were fitted to the Fehnler equation ($t_{ox} = E \cdot \ln(1 + F \cdot t)$) a very good agreement between the model and the experimental data was obtained as is shown by the solid lines in figure 1. The oxidation should then be explained through a field-imposed drift mechanism of anions through the SiO_2-layer

towards the SiO_2/Si-interface. Possible oxidation precursors are thus all anions present at the SiO_2/liquid-interface, e.g. OH^-, O_2^-, O_3^-, O^-, ... Since reference experiments with O_2-saturated solutions at various pH's proved that the silicon wafers could not be oxidized in the time scale considered, the hydroxyl anion or the dissolved oxygen can be excluded as direct precursor for the silicon oxidation.

From figure 1, it is clear that the oxide thickness is dependent on pH with a factor of 2 higher at pH 1.2 than at pH 4.6. The oxide is always somewhat thicker at low pH but except for the 1 mg/l data this difference is minor and thus one may conclude that there is only a weak pH-effect on the final oxide thickness which can be grown. Although the ozone decay rate increases at higher pH thus forming more radical species in the course of a complex decay process [11-13], e.g. HO_3 and HO_2, no enhancement of the final oxide thickness is obtained at higher pH. This is an important indication that radicals or anions from the bulk of the solution are not directly involved in the oxidation process. The chemistry of ozone in the bulk is thus of no relevance to the oxidation process. Moreover at low pH, where the oxidation goes somewhat faster, less anionic species will be available. This is due to a shift in the chemical equilibria versus the protonation of the anions: $HO_3 \Leftrightarrow O_3^- + H^+$ and $HO_2 \Leftrightarrow O_2^- + H^+$ [18-20]. A variation of the pH between 1.2 and 4.6 changes the H^+-concentration with a factor of 2500 and this should strongly influence the O_3^- and O_2^--concentrations in the solution. Since the pH has only a minor effect on the oxidation, the anions present in the bulk can also be excluded as oxidation precursors.

Influence of the ozone concentration

Growth-profiles were also measured for various initial ozone concentrations at pH 1.2 and pH 4.6: figure 2 and 3.

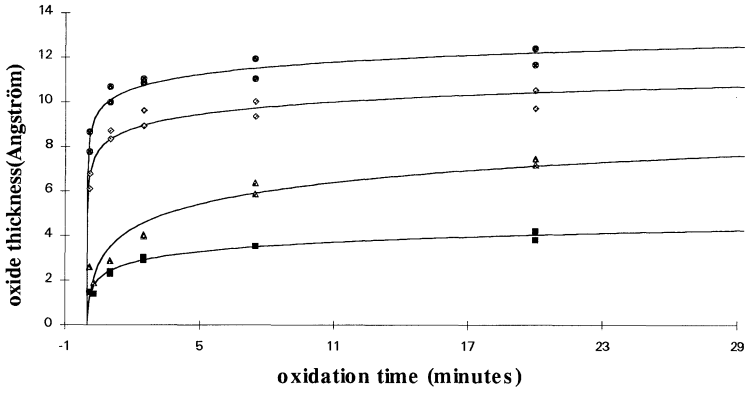

Figure 2: Growth profiles of SiO_2 as a function of the ozone concentration under the following experimental conditions: T = 22°C and pH 4.6 (■ = 1 mg/l; ▲ = 5 mg/l; ◊ = 15 mg/l; • = 17.6 mg/l)

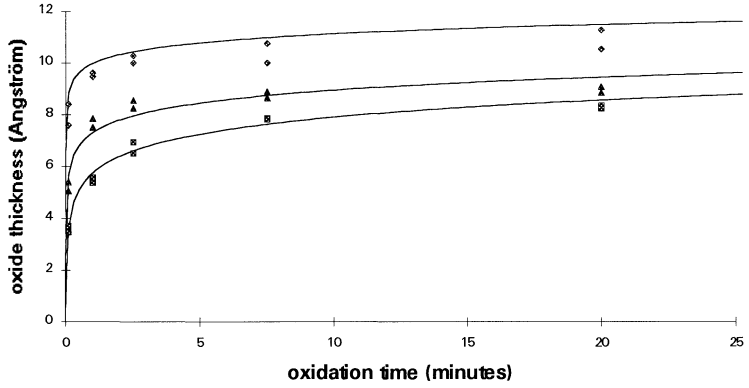

Figure 3: Growth profiles of SiO_2 as a function of the ozone concentration under the following experimental conditions: T = 22°C and pH 1.2 with nitric acid as additive (■ = 1 mg/l; ▲ = 5 mg/l; ◊ = 15 mg/l)

A clear concentration-dependence in the range between 1 and 18 mg/l is seen: $t_{ox,max}$, the oxide layer thickness at 20 minutes, increases with the ozone concentration. Although ozone itself is not the oxidizing species, it is logical that its concentration will in one or the other way be involved in the generation of the oxidizing precursor.
From figures 2 and 3 it can also be seen that the Fehnler expression fits the data reasonably well and the oxide thicknesses are predicted within 4 %.
The Fehnler model, when applied to silicon, is based on the theory that anions are the oxidation precursors which migrate through the oxide layer under the influence of a field over the oxide.
And since the bulk chemistry doesn't seem to play a role in the oxidation process the question remains how and which charged oxidizing species can be formed. One possible hypothesis is the reaction of ozone at the SiO_2/liquid-interface to form O^- ions in the following reaction sequence:

$$O_3 \Leftrightarrow O + O_2 \quad (1)$$

$$O + e \rightarrow O^- \quad (2)$$

Another possible pathway would be one in which O^- ions are formed directly [16].

$$O_3 + e \rightarrow O^- + O_2 \quad \text{n-type} \quad (3)$$

$$O_3 \rightarrow O_2 + O^- + hole \quad \text{p-type} \quad (4)$$

In this hypothesis a higher ozone concentration in the solution should result in a higher ozone concentration at the SiO_2/liquid-interface and this of course will enhance the O^- formation rate. However the oxide growth rate and the final oxide thickness level off. Indeed at higher ozone concentrations the oxide growth is limited by the field-imposed drift as the field in the growing oxide remains constant [15]. Moreover, O^- ions will be lost by a mechanism which up to now remains unknown [21] and which effect increases with increasing oxide thickness.

Influence of the anion

It is known that chloride ions have a strong influence on the ozone decay rate in solution. This is because chloride anions react directly with ozone ($Cl^- + O_3 \rightarrow ClO^- + O_2$) [22].To check the possibility that the nature of the acid (anion) is a crucial parameter in the growth mechanism, hydrochloric acid was used to acidify the solution to the same pH=1.2 as in the former experiments in nitric acid.
For oxidation times shorter than 12 minutes the oxide thickness t_{ox} is the same within 5 % in HCl or HNO_3. Only at an oxidation time of 20 minutes the oxide layer is somewhat thicker in hydrochloric acid than nitric acid. So one must conclude that there is no pronounced anion-effect on the growth rate. This confirms our finding that the ozone chemistry in the bulk solution has no serious effect on the oxidation kinetics. Indeed changes in the solution chemical composition due to variation of pH or additive hardly influences the growth kinetics. This indicates that the bulk of the solution and the chemical processes therein play no role and that rather processes at the SiO_2/liquid-interface will be important. At this interface the possible oxidation precursor O^- is formed and is subsequently transported towards the SiO_2/Si-interface. As already said, isotope marker studies indicated that the oxidizing species migrates through the oxide layer and thus that the oxidation occurs at the SiO_2/Si-interface rather than at the SiO_2/liquid-interface [17].This mechanism is confirmed by AFM-measurements which showed no roughnening of the wafer surface. After a 20 minute oxidation at room temperature, the surface microroughness R_a was found to be (0.035 ± 0.002) nm for 8.5 mg/l ozone at pH 4.6 (1.22 nm thick oxide) and (0.037 ± 0.001) nm for 14.0 mg/l ozone at pH 1.2 (1.14 nm thick oxide). The blanc, a HF-dipped wafer, had a R_a-value of 0.034 nm. When oxidation would have taken place at the SiO_2/liquid-interface one would have seen a much stronger surface roughening.

Influence of temperature

Thermal oxidation of silicon is characterized by a strong positive temperature effect on the oxidation rate. When seen as an Arrhenius temperature dependence $e^{-E/RT}$, values for E in the range of 190 kJ/mol were found [4]. In order to check the effect of temperature on the oxidation of silicon in ozonated solutions, silicon wafers were oxidized in a HCl-spiked bath (pH 1.2) at various solution temperatures in the range of 20-50°C with a quasi constant ozone concentration of about 15 mg/l.

No pronounced temperature-effect (positive or negative) could be observed in the range from 20 to 50°C. This again confirms that the bulk chemistry of ozone is

irrelevant for the oxidation process. Indeed the ozone decay rate itself is temperature dependent, i.e. an increasing temperature leads to a higher decomposition rate and thus to more radical production [23]. Also the equilibrium constants for the protonation reactions of the anionic species mentioned previously will be temperature dependent. Besides the decay rate, the diffusion of the oxidizing species in the solid phase is also temperature dependent. For example, the activation energy for diffusion through the SiO_2-layer is of the order of 113 kJ/mole for oxygen [15] and 77 kJ/mole for water [24] explaining the positive temperature effect of thermal oxidation. With an activation energy of 113 kJ/mole, the diffusion becomes a factor of about 70 faster between 293 and 323 K. So, even with a change in diffusion rate through the SiO_2-layer of almost two orders of magnitude, no temperature effect is seen on the oxidation rate by ozone and thus the diffusion of ozone or another precursor cannot be the rate determining step.

Concerning the possible O^- radical formation reactions (1) to (4), one can argue that the two-step reaction sequence (1) to (2) is not very probable because of the endothermicity of reaction (1) of about 105 kJ/mole. The one-step reaction at the SiO_2/liquid-interface is exothermic for about 40 kJ/mole. Based on the fact that no temperature dependence is seen, the one-step O^- formation reaction (4) is the most likely. The fact that reaction (1), the self-decomposition of ozone, is not responsable for the oxidation is again an indication that bulk processes play no role.

From the above it must be concluded that the electrical field over the oxide layer will be the limiting factor in the transport of the oxidation precursor(s) and thus for the oxide growth. This confirms the assumption made in the Fehnler formalism where diffusive transport of anions is negligible compared to field-imposed drift.

CONCLUSIONS

The oxidation of silicon by means of ozonated solutions was investigated at temperatures between 22 and 50°C. The growth profiles show an initially fast growth which after a few minutes drops to a negligible value. No pronounced pH-dependence is observed between 1.2 and 4.6 and no anion-effect was found when using Cl^- and NO_3^-. A concentration-effect was noticed in the range of 0-15 mg/l ozone. The maximum oxide thickness $t_{ox,max}$ increases (slightly) with increasing ozone concentration. This is caused by the fact that the oxidizing species O^- is formed directly from the ozone present at the SiO_2/liquid-interface. At higher ozone concentration this dependence disappears.
Increasing the solution temperature does not lead to an enhanced oxidation rate. Transport of the oxidation precursor by field-imposed drift is most probably the rate determining factor of the oxidation process.
The growth kinetics follow the relation $t_{ox} = E \ln (1 + F\ t)$ as proposed by Fehnler as an expansion of the Cabrera-Mott theory. An electric field is set up over the oxide layer which enables the charged oxidizing species to diffuse through the SiO_2-layer with the field-imposed drift as limiting factor. It is proposed that this charged precursor is generated at the SiO_2-liquid interface where ozone forms O^- in a one-step reaction. This O^--forming process at the interface and the transport of O^- through the

SiO_2-layer are the rate controlling steps, the chemistry in the bulk of the solution being of no importance.
From the processing point of view one may notice that there is no need for trying to achieve the highest possible ozone concentrations since experiments showed that a plateau in $t_{ox,max}$ is reached at about 15 mg/l. It is also clear that there is no need to work at elevated temperatures as there is no benefit in increasing the temperature in terms of oxide growth rates.

ACKNOWLEDGEMENTS

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A PROBE OF CHEMICAL OXIDE GROWTH CONDITIONS

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ABSTRACT

Silicon oxides on bare silicon wafers are often formed in either aqueous ozone or caustic solutions of hydrogen peroxide. We have evaluated these oxides, grown in a temperature range from 20C to 70C, using photo-thermal reflection spectroscopy (Therma-Probe). We find that this method is very sensitive to the type of oxide grown; for example, whether it is an SC1 oxide or ozone oxide. We are able to observe the replacement of one chemical oxide by another. In addition, the magnitude of the Therma-Probe signal is sensitive to the temperature at which the SC1 oxide is grown. Since the Therma-Probe signal has been used to measure residual stress in bulk silicon, these results suggest that chemical oxides grown by different chemistries and temperatures may leave significantly different levels of residual stress in the first few layers of the substrate silicon.

INTRODUCTION

Thermally grown and chemical vapor deposited silicon oxide films that are thinner than 20A are of great technical interest at the present time, as the device industry attempts to optimize the electronic properties of these very thin oxides. But chemically grown oxides which are <20A thick are also of great commercial interest, since almost all of the bare silicon wafers used by the industry are covered with such an oxide. The most common of these chemical oxides are those grown from SC1 chemistry and those grown from aqueous ozone (1,2). At a first step in their processes, device makers must decide what to do with this oxide. A cleaning step to remove or replace the oxide will add processing costs and therefore, a very high quality oxide is desired.

The growth kinetics, structure and chemistry of chemical oxides including SC1 and ozone oxides have been investigated in several recent papers (3- 9). Sugita *et. al* (7,8) investigated the density of chemical oxides by glancing incidence x-ray reflectivity (GXIR) and the density of Si-H bonds in the oxide and at the interface by ATR-FTIR. They concluded that the ozone oxide is denser than the SC1 oxide because the latter is made up of oxide islands surrounded by hydrogen-terminated silicon. Aoyama *et. al* (9) studied the size of various chemical oxide islands by combining an oxide-selective etch with AFM and STM imaging. They concluded that an SC1 oxide is composed of 30 to 70 nm wide islands with an island density of about $10^{10}/cm^2$.

We have directly observed that the type of chemical oxide present on a bare silicon wafer may affect the interpretation of photo-thermal reflection spectroscopic (Therma-Probe) data that is used to monitor ion implantation processes (10-12). In this application, the device maker uses a change in Therma-Probe signal as a measure of the ion

implantation density. The change in silicon crystal lattice stress is proportional to the Therma-Probe signal that is measured on monitor wafers before and after implantation.

However, some types of silicon wafers produce interferences by giving a very high signal before implantation. Residual sub-surface damage in the silicon wafer had been thought to be the cause however, we will show in this paper that the higher Therma-Probe reading is actually an indicator of the growth conditions of the chemical oxide and may be a sensitive measure of the oxide's structure.

EXPERIMENTAL

Materials. All tests were done using 200 mm diameter, P- type, Czochralski-grown silicon wafers that were stripped in HF to remove the oxide prior to intentional oxide growth.

SC-1 & Ozone baths. Standard SC1 bath concentrations were used for the experiments with NH4OH:H2O2:H2O ratios of 1:2:40. Temperatures were varied from room temperature to 70C. Ozone bath concentration was >10 ppm and the temperature was 20C +/- 3C.

Oxide undergrowth experiments. In "undergrowth" experiments that started with ozone-oxide growth followed by SC1-oxide undergrowth, the initial surface was first stripped with HF followed by ozone oxide growth for 10 minutes, yielding a 0.8 nm to 1.0 nm thick ozone oxide. Wafers were immersed in a 65C, 1:4:20 SC1 bath at various times. In undergrowth experiments that started with an SC1 oxide followed by ozone oxide undergrowth, the starting wafer was HF-stripped, immediately immersed in an SC1 bath for the indicated time and temperature, and then immersed in a room temperature >10 ppm ozone bath.

Thermal-probe measurements. All photo-thermal reflection spectroscopic measurements were made using a Therma-Probe TP-420 system at Motorola's facilities in Phoenix, AZ. In this measurement, an argon laser beam modulated at 1 MHz, pumps the surface. The laser beam spot diameter is 1 micron. Changes in the sample reflectivity induced by the pump-laser are probed using a helium-neon laser. The thermal wave (TW) signal is proportional to the change in reflectance divided by the total reflectance. Local inhomogeneities, such as lattice strain, induce modulation in the thermal reflectance wave. In some of these experiments, we report the TW at time zero ($TW_{0)}$. TW_0 is acquired "on-the-fly" in a 137 point raster scan of the wafer. In other experiments, the laser beam may be kept at one spot for 30 seconds. TW_{30} is the thermal wave signal intensity after this 30-second laser beam exposure. In this case, a decay factor (DF) may be calculated from the ratio TW_{30}/TW_0. This ratio is usually less than one.

RESULTS AND DISCUSSION

The typical TW_0 and TW_{30} signals for ozone-oxide and SC1-oxide are consistently and significantly different as shown in Table 1. It is thought that the difference is a result of different levels of strain in the near surface silicon caused by the oxide/silicon interfacial bonds. This residual strain could simply be a result of the oxide growth temperature, or a result of the chemical structure of the oxide/silicon interface that is unique for each chemical oxide type. These two hypotheses are tested in the following ways.

SC1 oxides are normally grown at temperatures between 45C and 90C, while ozone oxides are normally grown between 5C and 25C. If oxide growth temperature is the reason for the TW difference, an SC1 oxide grown at 25C should have a TW close to that of an ozone oxide. Figure 1 shows that this is not true, although there is a slight increase of the TW_0 signal as the SC1 temperature drops the value never approaches a TW_0 of 180 to 200.

As discussed in the introduction, SC1-oxides and ozone oxides are known to have significantly different stoichiometries. If this difference is the cause of the different TW signals, then the TW_0 signal should change as the oxide type is changed. The resulting TW_0 signal changes are shown in Figures 2 & 3. In Figure 2, one can see that the TW_0 signal changes as the ozone oxide is replaced at the interface by the SC1 oxide. Since the etch rate of silicon is about 0.45 nm/minute under these conditions (3), we would expect the TW_0 signal to approach that of an SC1 oxide in about two minutes, which it does. In Figure 3, various thicknesses of SC1 oxides are grown prior to a ten minute exposure to aqueous O_3. The change in TW signal shows that, after less than one minute of SC1 oxide growth, the SC1oxide is already too thick for subsequent penetration in 10 minutes by the O^- radical ion, thought to be the primary oxidizing species in an ozone bath (4). The thickest SC1 oxide in this test is certainly no more than 1.0 nm thick. However, for the very thin SC1 oxide, subsequent ozone oxidation increases the TW signal to match that of an ozone oxide.

However, the chemically grown oxides that are only 0.8 nm to 1.0 nm thick are not completely passivated. The oxide will continue to grow to a thickness of 1.4 nm to 1.5 nm if the wafer is exposed to high humidity for many days. See Figure 4. The change of the TW_{30} signals with time in high humidity is shown in Figures 5. Surprisingly, although both TW_{30} signals decrease, they do not reach the same signal level. The ozone-oxide TW_{30} approaches 78 while the SC1-oxide TW_{30} approaches 40. This suggests that the air oxide is not completely undercutting the chemical oxides.

All of these observations can be explained based upon the proposals, already made by Aoyama and by Sugita. They propose that the silicon surface is covered by islands of oxide, that these islands are separated by regions of hydrogen-terminated silicon- either O_xSi- H_y or Si-H_x, and that the total area of regions of less-oxidized silicon is proportional to the oxidation potential of the cleaning agent. This is thought to be so because the hydride coverage after ozone oxidation is less than $1/5^{th}$ of that after SC1 oxidation and also because the ozone oxide density is greater than that of the SC1 oxide. Therefore, the ozone oxide has less area between the oxide islands than the SC1 oxide.

This model allows one to predict that the near-surface stress in the first few silicon layers beneath an SC1 oxide should be less than that beneath an ozone oxide. This should be so because the larger area between the SC1-oxide islands should permit more relief of the stress created by the volume expansion created by oxidation. Further, the higher density of interface Si-H bonds in an SC1 oxide should also relieve this same stress. Our experiments confirm that the near surface region below the SC1 oxide has less stress (lower TW signal) than that beneath the ozone oxide (higher TW signal). They also show that stress increases when an ozone oxide is inserted under the SC1 oxide, as schematically illustrated in Figure 6, or decreases when the SC1 oxide is inserted beneath the ozone oxide.

Based upon these ideas about chemical oxides, one would expect that there should be a relationship between the stress in the near surface silicon, as measured by TW, the electrochemical potential of the chemical oxidant (13) and the normalized Si-H coverage (7,8) of the surface. Figure 7 shows the data we have thus far for these relationships. As one would expect, stress increases as the oxidation potential increases and as hydride coverage decreases.

Finally, this model suggests why the extended air oxidation of these oxides does not reduce the TW signal to the same value for both oxides. If the air oxidation is occurring around the edges of the islands rather than uniformly growing across the entire interface, then the stress, and corresponding TW signals, from the ozone and SC1 oxides should change at the same rate.

SUMMARY

The Therma-Probe measurement is very sensitive to chemical oxide type. Ozone and SC1 oxides are easily distinguished. The replacement of one oxide by another may be observed by this technique, and so is the further oxidation of these samples in air. The results appear to support previous proposals that chemical oxides have an island structure. The difference in island structures between oxide types is used to explain the difference in stress levels detected by the Therma-Probe method.

ACKNOWLEDGEMENTS

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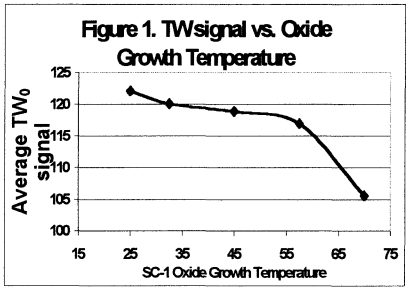
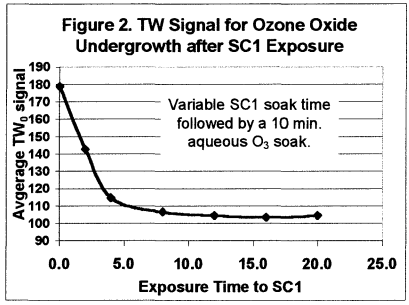
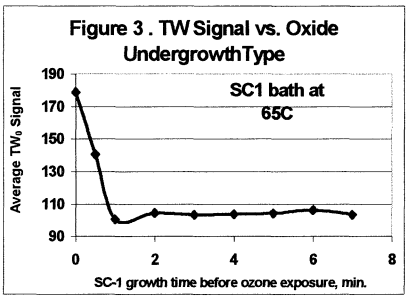
TABLES AND FIGURES

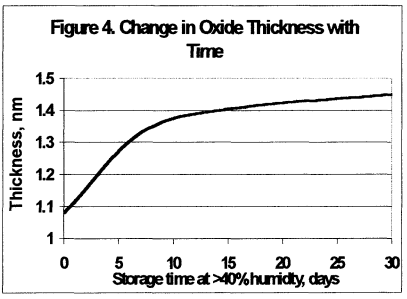
Table 1. Typical TW values for SC1 and ozone oxides.

	TW_0	TW_{30}
Ozone-oxide	**180- 200**	**90- 105**
SC1-oxide	**100- 120**	**45- 55**









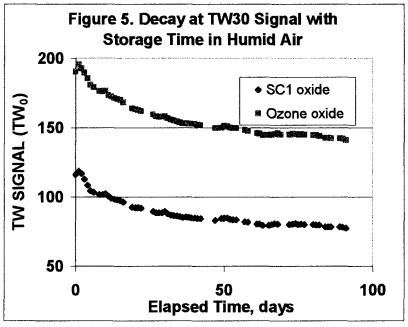
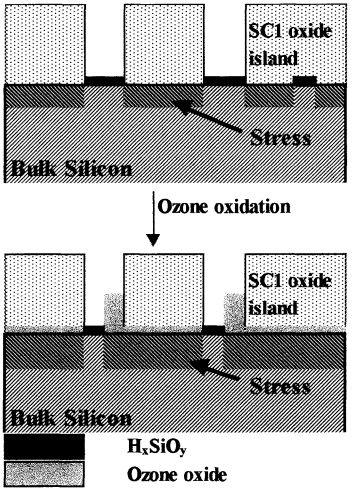
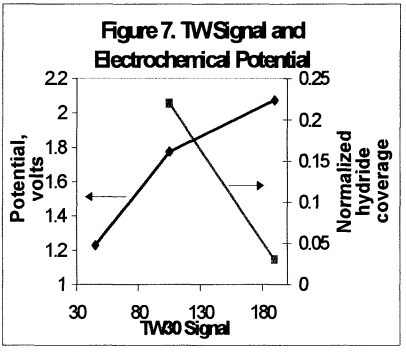


Figure 6. A Model of Stress under Chemical Oxides





CONSOLIDATING VIA CLEANING PROCESSES IN A MANUFACTURING LINE WHICH UTILIZES 3 DIFFERENT TYPES OF SPIN-ON-DIELECTRICS

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Abstract

This paper evaluates the complexity of different device technologies in a manufacturing line that utilizes 3 separate spin-on dielectric (SOD) materials for planarization requirements, namely 1) Silicate SOG; 2) Siloxane SOG; and 3) HSQ low-k material. The study shows the effect of the different SOD materials on post-etch residue formation; investigates multiple cleaning combinations and their effects on residue removal; and compares via resistance and device yield as a result of the different cleaning treatments. The data shows that manufacturing cleaning processes across all device technologies can be consolidated from 3 separate processes into 1 process. This optimized cleaning process also resulted in via resistance being reduced by as much as 14%, and overall yield increases on some devices by as much as 2%. This consolidation allowed for equipment and process backup, which did not exist prior to this work. As well, reduction in volumes of chemicals used of 7% was achieved, resulting in a reduction of chemical costs of 26%.

INTRODUCTION

Cleaning of post-etch residues remains a challenge in semiconductor processing. Numerous methods for achieving a clean interconnect at via level exist. These can include wet processes, dry processes, and a combination thereof. Many factors can influence the etch residues formed during a via etch step. These factors include photoresist type, geometry, plasma etcher, dielectric type, underlying metal stack, etc. The list can end up being quite large, with many factors that can change not only from run to run, but from day to day and week to week. Therefore, it is essential that a cleaning process be robust enough to account for the variations of these factors. It is much easier to choose a cleaning process that is robust than individually try to control the factors that affect sidewall polymer formation. Another problem that was seen at the Philips Fab has also been exhibited in other fabs where DI water usage is very strict, and water flow rates are minimal. This problem is rinsing of vias, specifically smaller, high aspect ratio vias after being subjected to the cleaning chemistry. Many times, intermediate rinse chemistries are chosen at random due to availability, and typically this is IPA. However, dissimilarity in cleaning chemistries, intermediate rinses, and the DI water can create a problem in which the vias are not completely rinsed with DI water.

This study focuses on consolidating the cleaning processes of a manufacturing facility that produces BiCMOS devices. The cleaning processes studied were contact and via level. The feature geometries ranged in size from 1.2 to 0.6 microns. The big challenge in cleaning was that the manufacturing line utilized 3 different types of spin-on-dielectric (SOD) material. These materials consisted of silicate spin-on-glass (SOG), siloxane SOG, and an Hydrogen Silsesquioxane (HSQ) material. The number of SOD's used was attributed to different generations of process transfers of device technologies from a central technology site. The most recent shift to the HSQ material allowed for easier integration of an SOD, and was not mainly used for its low-k properties. For example, the silicate and siloxane based SOG layers required a double coat process, which was time consuming. As well, historically, siloxane based SOG materials are very sensitive to cleaning when it comes to aqueous based materials. This has been documented in several papers and is generally termed "via poisoning" due to the effect of siloxane SOG outgassing and causing metal voids in the via. The existing cleaning processes in the Fab for via and contact cleans consist of a dry descum step, followed by a subsequent wet cleaning process, and then followed by a dry "clean-up" step. The purpose of the descum step is to remove the harder, cross-linked top skin of the photoresist layer. The wet cleaning steps used prior to the consolidation consisted of 3 separate cleaning processes used in 3 separate wet benches. Two of the processes were solvent/amine based chemistries, and the third was Hydroxylamine based. These processes were added over the years to meet certain technology requirements and the appropriate device technology and process level were segregated to go through the correct cleaning level. The subsequent dry "cleanup" step was performed in a microwave downstream system, and was used to remove any organic material that may be left after the wet cleaning step. The main thrust to undertake in this study also was due to the fact that the 2 solvent/amine processes currently used to remove via residues were ineffective at removing residues from the newer technology processes (MOBI3 and SACMOS) utilizing the HSQ SOD material. Therefore the need for an effective post-etch residue removal process for the

HSQ layer was coupled with a need for manufacturing requirements to minimize and consolidate the number of cleaning processes used in production.

EXPERIMENTAL

Initial testing was performed at Philips to identify a cleaning process that was capable of removing the post-etch residues generated by the HSQ layer. Time and temperature matrix testing of the existing solvent/amine based chemistries conclusively showed that they would not be effective. Subsequent trials performed at EKC showed that a Hydroxylamine based process was successful in removing the etch residues. Further testing was performed in-house at Philips with the EKC chemistries and electrical and optical results proved favorable.

RESULTS AND DISCUSSION

Split lots for each technology and device level were performed with the new chemical process. Comparison of the SEM's after cleaning can be seen in Figures 1 and 2. As can be seen from the SEM's, the QuBIC 2 contact process comparing the "old" vs. "new" show visually clean results after the wet cleaning step, as was seen with the other QuBIC 1 and QuBIC 2 process levels. Likewise, both the via resistance and yield data produce very similar results (Figures 3 and 4). This indicates that the cleaning processes are satisfactory for these levels. The MOBI3 and SACMOS SEM's, however, show a different story. The "old" solvent cleaning processes show residual polymer in the via structure, as can be seen by the SACMOS via level (Figure 5). The "new" EKC cleaning process does not show any signs of post-etch residue (Figure 6). Consequently, the via resistance data for the split lots which received the EKC treatment is lower than that of the other cleaning processes (Figure 7). As would be expected, the yield data for the split lots shows higher yields for the "new" EKC process than the "old" cleaning processes (Figures 8). The split lot data, therefore, indicated that from a visual and electrical standpoint, the "new" EKC cleaning process was equal to or better the existing cleaning processes at all levels tested.

CONCLUSIONS

In looking at the resulting achievements from a process consolidation standpoint, many benefits were gained from this change. First, three separate cleaning processes, each taking up its own wet bench, were consolidated into a single cleaning process. Due to the method in which technologies and process levels were split by cleaning chemistry, wetbench usage, both in terms of wetbench usage and wafer moves, was non-optimal. To go along with this, each wetbench, despite minimal usage in some cases, must be poured up to clean wafers, and thus chemical usage in the wetbench in some cases proved to be very inefficient. The new EKC chemical process significantly increases wetbench utilization while providing a cost effective process. The resulting chemical savings in terms of volume (gallons per year) and cost (dollars per year) can be seen in Figures 9 and 10, respectively. The consolidation to a single cleaning process also allowed for removal of one wetbench from the manufacturing area due to redundancy. This in turn

increased the amount of available cleanroom space, which is a premium in an already "full" Fab environment. The new cleaning process is being utilized in 2 separate wetbenches. This now allows for a backup wetbench in case one of the wetbenches requires maintenance. Prior to the consolidation, there was no backup capacity on any of the wetbenches running at this site. Even though the total number of wetbenches was reduced from 3 to 2 units, the consolidation provided for much better use of the equipment. Even with anticipated Q4 ramp-ups of certain devices, the wetbenches have excess capacity for future ramps in production, as can be seen by utilization levels of < 60% currently. Finally, the cleaning process was designed to be robust enough for different equipment types. Philips has evaluated the use of solvent spray tools in their 200 mm Fab expansion. Joint work with Philips and the chemical and equipment suppliers has resulted in a spray tool process capable of cleaning the newer technology MOBI3 and SACMOS processes with a process time approximately 50% lower than the current wetbench process.

Figure 1: JT Baker Process

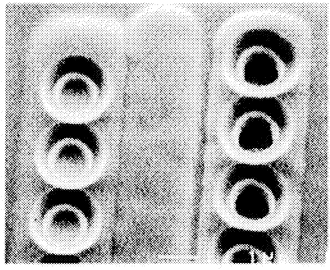


Figure 2: EKC Process

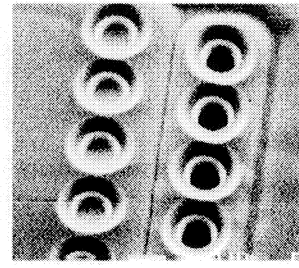


Figure 3: QuBIC 2 Contact Resistance

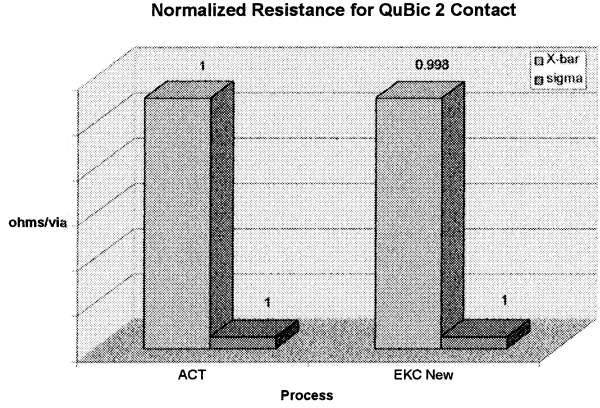


Figure 4: QuBIC 2 Contact Yield

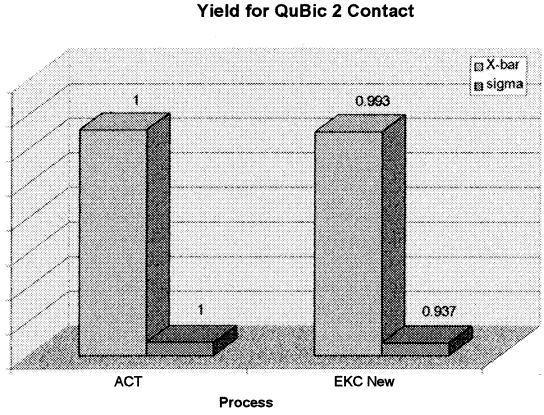


Figure 5: JT Baker Process

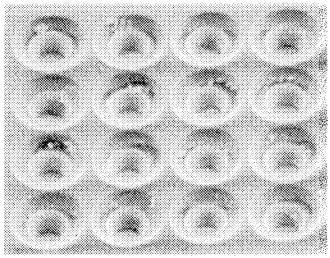


Figure 6: EKC Process

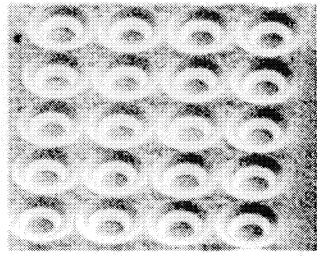


Figure 7: SACMOS Via Resistance

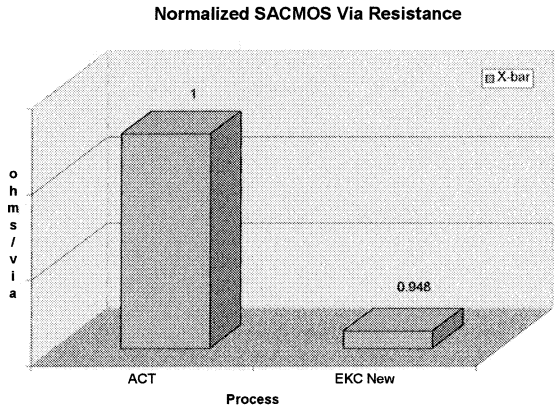


Figure 8: SACMOS Yield Data

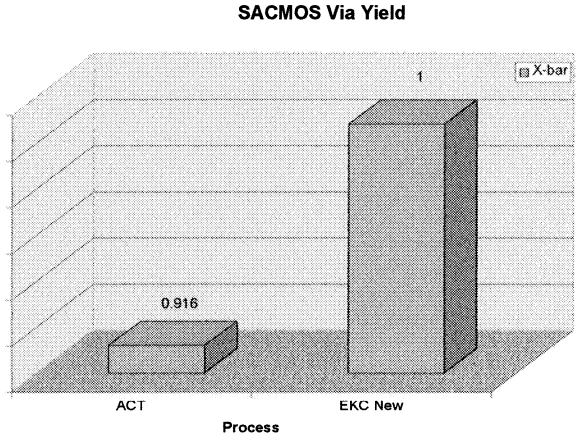


Figure 9: Chemical Volume Reduction with New Processes

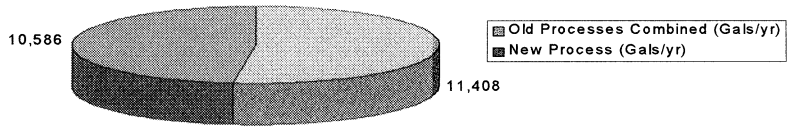
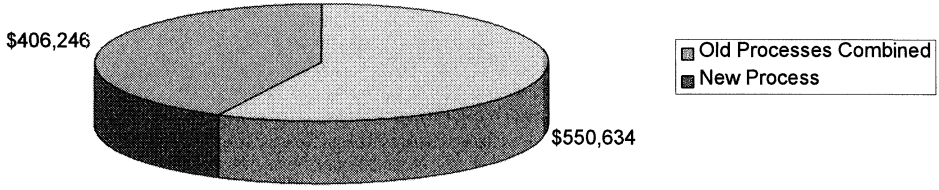


Figure 10: Chemical Cost Savings using New Processes



PRECISION SURFACE CLEANING USING MICROCLUSTER BEAMS

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ABSTRACT

This paper addresses a new cleaning technology for removing particles and thin films from semiconductor wafer surfaces. The technology depends on the formation of charged microcluster beams, accelerated to hypervelocities in vacuum. Particle contaminants, exposed to the impinging microclusters, are removed by transfer of impulsive forces during microcluster-particle collisions. A microshock mechanism, leading to material unloading, is hypothesized for film removal. Neutralization tests discussed show that wafer charging is prevented by injecting thermionic electrons into the microcluster beam. Wafer cleaning studies were conducted in a modified scanning electron microscope (SEM). Contaminants introduced on wafer samples by diamond-scribing the surface were cleaned in the SEM by the microcluster beam method. Analysis of before-and-after-cleaning SEM photomicrographs of the same local area verified that particles smaller than 0.05 micron were removed. The requirement to remove even smaller particle defects from future microdevices can be met by this in-situ cleaning method.

INTRODUCTION

As semiconductor device geometries continue to shrink (0.07 micron by the year 2006) and wafer sizes increase (300 mm), the limitations of existing cleaning methods on device yields will become more critical as the size of "killer" particles also shrink. Innovative technology is needed to specifically target removal of strongly adherent, submicron particles (0.1 micron and smaller). This new and important technology will not replace current cleaning methods that remove larger contaminants. Rather, the technology will play a supplemental role serving as a final, precision clean for removing submicron defects left behind by conventional cleaning methods. Energetic microcluster beams provide a new technology for precision surface cleaning. This in-situ vacuum surface cleaning process uses directed, energetic beams of submicron clusters to clean surfaces contaminated with solid particulates and organic films. Because this new technology can efficiently dislodge submicron defects, it can potentially reduce wet cleaning times, conserving water expended by non-productive "overcleans". The full merit of microcluster beam technology as a "topping-off" cleaning process may be realized in post CMP clean applications and after wet clean drying cycles that leave micron-sized water spots on wafer surfaces. Recently, focus has been placed on wafer cross-contamination brought about by copper interconnect deposition, requiring removal of trace copper from wafer bevels and backsides (1). Removal of backside wafer contaminates should be addressed by in-situ microcluster beam cleaning technology. Applying this potentially breakthrough technology for improving on-line yields will depend on the successful integration of microcluster cleaning modules with cluster tool platforms.

Microcluster beams are generated by the electrostatic atomization of a conducting solution exposed to high electric fields (2). The liquid (typically a water-solvent mixture) is fed under pressure to the tips of capillary emitters exposed to vacuum. Atomization occurs when voltage is applied to the emitters. Surface charging, followed by coulombic explosion forms a beam of hypervelocity, submicron clusters (Fig.1). Applying positive voltage to

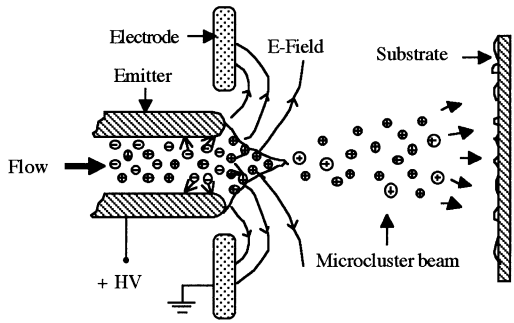

Fig. 1 Microcluster beam formed by electrostatic atomization.

the capillary preferentially pulls positive charges in the solution to the liquid-vacuum interface. Negative counterions migrate to the walls of the metal capillary where they transfer conducting electrons. When the electrostatic stress acting on the charged surface exceeds the liquid surface tension force, the meniscus disrupts forming a beam of positively charged microclusters. The microclusters are accelerated toward a substrate with an energy qV where q is the charge on the microcluster and V is the applied capillary potential. For surface cleaning, it is preferred to generate microclusters with diameters ranging from about 0.01 to 1μm.

Fig. 2 shows a microcluster emitter source design for surface cleaning studies. The source operates in vacuum starting at about 1 mtorr but lower vacuum (10^{-5} torr or less) is preferred. A fused silica transfer line delivers solution, stored in a reservoir, to the tip of the capillary emitter assembly centered within a circular aperture machined in the counter-

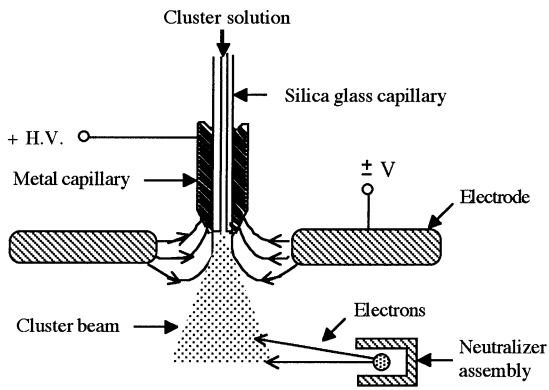

Fig. 2 Microcluster beam source.

electrode. The inner diameter of the fused silica transfer line is 50 μm and the outside diameter about 375 μm. The solution reservoir, exposed to constant atmospheric pressure, is located outside the vacuum housing enclosing the substrate to be cleaned. The solution flow rate is controlled by varying the length and inside diameter of the fused silica line to provide the proper impedance to flow - usually in the range 0.5 to 2 microliters/minute. A neutralizer assembly, consisting of a thermionic emitter and shield, is installed on the microcluster beam source. The neutralizer injects low-energy electrons into the beam to compensate for charge build-up on electrically insulating surfaces during the cleaning process.

CONTAMINANT REMOVAL MECHANISMS

Different mechanisms are proposed for the removal of particle and film contaminants when substrates are bombarded by energetic microclusters. For particle removal, we propose a removal mechanism whereby lift-off occurs when the impulsive force transmitted by an impacting microcluster is sufficient to overcome van der Waals adhesion forces. This hypothesis will be examined by comparing microcluster impact forces to the van der Waals adhesion forces bonding spherical particles to a flat surface. Consider the collision of a microcluster with a surface particle. The impulse I given to the particle is

$$I = \Delta p = p_i - p_f = F_i \Delta t \qquad [1]$$

where p_i and p_f are the initial and final momentum states, F_i is the transmitted impulsive force and Δt is the collision time. The analysis is simplified by neglecting any momentum enhancement due to microcluster or particle material ejected backward (that is, $p_f = 0$). The impulsive force acting on the particle during a head-on collision (microcluster diameter less than the particle diameter) in time Δt is,

$$F_i = mv/\Delta t \qquad [2]$$

where m and v are the mass and velocity of the impacting microcluster. Assuming the collisional interaction time approximates the time it takes a cluster having a velocity v to traverse a distance equal to the microcluster diameter, $\Delta t \approx 2r/v$, the impulsive force becomes,

$$F_i = mv^2/2r \qquad [3]$$

or, since $mv^2/2 = qV_a$ where q is the net charge carried by the microcluster and V_a is the applied emitter voltage, Eq.[3] can be expressed in the form

$$F_i = qV_a/r \qquad [4]$$

which states that the impulsive force is equal to the microcluster impact energy divided by its radius. The microcluster charge q is related to its radius r by (3)

$$q = 4\pi (\varepsilon_0 \gamma)^{1/2} r^{3/2} . \qquad [5]$$

Substitution of Eq.[5] into Eq.[4] yields the following expression for the impulsive force,

$$F_i = 4\pi (\varepsilon_0 \gamma)^{1/2} r^{1/2} V_a \qquad [6]$$

Assuming clusters are sprayed from a solution having a surface tension $\gamma = 0.05$ N/m and accelerated through a potential $V_a = 10$ kV (typical values for some cleaning applications), the impulsive force given by Eq.[6] reduces to

$$F_i \approx 8.4\, r^{1/2} \quad \text{(dynes)} \qquad [7]$$

for r in microns. This equation allows one to estimate the impulsive force exerted on surface particles as a function of the size of the impacting cluster.

A theoretical analysis by Bowling (4) for approximating van der Waals adhesive forces between spherical particles of radius r_s and a flat surface yields

$$F_v \approx hr_s/8\pi z^2 \qquad [8]$$

where h is the material dependent (particle and surface) Lifshitz-van der Waals constant and z is the adhesion distance assumed to be about 4 angstroms. Taking h = 8.0 ev (1.28×10^{11} erg), Eq.[8] reduces to

$$F_v \approx 0.032\, r_s \quad \text{(dynes)} \qquad [9]$$

for r_s in microns.

If the impulsive force generated by a single microcluster impact exceeds the van der Waals adhesive force (i.e., $F_i > F_v$), a high probability exists that a contaminant particle will be dislodged from the surface. Compared to van der Waals adhesive forces (Eq.[9]), microcluster impact forces (Eq.[7]) are significantly larger. Analysis has shown that contaminant particles with liftoff velocities in the range 1-4 m/s will completely escape a 300 mm wafer. Impacting microclusters have velocities greater than 1 km/s so even glancing collisions can transfer enough force to remove particulates.

A shock wave model is proposed for removing thin film contaminants since microclusters are accelerated to hypervelocities that exceed the speed of sound in some impacted materials (5). Microshock waves propagated in thin films can lead to unloading of material after passage of decompression waves. This process is pictured schematically in

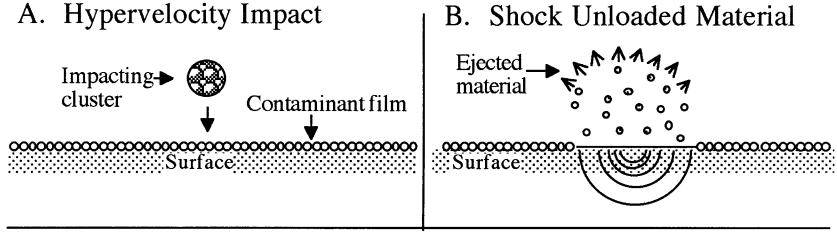

Fig. 3 Contaminant film removal by microshock unloading.

Fig.3. Local shock pressures generated by hypervelocity impacts can be roughly estimated by the Bernoulli pressure term, $P = \rho v^2/2$, where ρ and v are the density and velocity of the incident microcluster (6). Using this expression, shock pressures are estimated to exceed 1 GPa at surfaces impacted by microclusters. To prevent "hazing" of wafer surface materials, a damage threshold velocity for impacting microclusters is estimated at 1-5 km/sec.

WAFER CHARGING STUDIES

Microcluster Beam Neutralization

A neutralization method is required to prevent charging of wafers and other insulating surfaces impacted by charged microcluster beams. Neutralization can be achieved by injecting electrons into the microparticle beam. Compared to atomic or molecular ions, microclusters are sufficiently macroscopic and highly charged to promote neutralization by electron capture (7). In addition to reducing the net positive charge on microclusters, electrons can also suppress positive charge build-up on substrates. Although electrons can be generated by different methods, thermally emitted electrons from heated filaments are shown to prevent charging of wafers bombarded by low current (microamps) microclusters. Wafer neutralization, using plasma bridge devices, is also required during high-current (milliamps) ion implantation processes (8). Charge neutralization is less demanding for the microcluster beam cleaning process since beam currents are three to four orders of magnitude less than ion implantation currents.

Thermionic Emission

Thermionic emission of electrons from heated metals is governed by the Richardson-Dushman (R-D) equation (9),

$$J = A_o T^2 \exp(-\phi/kt) \qquad [10]$$

where J is the thermal electron emission current in A/cm^2, A_o is the R-D constant with a theoretical value of $120/cm^2\ deg^2$, T is the metal temperature in degrees Kelvin, ϕ is the effective work function of the metal and k is Boltzmann's constant = 8.6×10^{-5} eV/deg K. The effective work function varies with temperature according to

$$\phi = \phi_R + \alpha T \qquad [11]$$

where ϕ_R is the Richardson's work function (temperature independent) and α is the temperature coefficient of the work function of the order 10^{-4} eV/degree Kelvin. Substituting Eq.[11] into Eq.[10] yields,

$$J = A_o T^2 \exp(-\alpha/k) \exp(-\phi_R/kT) \qquad [12]$$

Although all metals can emit thermal electrons when heated, the high temperatures required to reach practical current densities limits the choice to refractory metals such as tantalum and tungsten. Inspection of Eq.[12] shows that electron emission depends strongly on the metal work function in the exponential term. Metal alloys, such as thoriated tungsten and dispenser cathodes, have lower work functions than tantalum or tungsten, but these materials require careful activation steps and are more susceptible to contamination. For simplicity, we selected tantalum as the material for conducting wafer neutralization tests.

Neutralizer Design

The heating element, used to conduct wafer charging measurements, consisted of a one inch long, 0.020 diameter tantalum filament. The tantalum filament was completely enclosed by a neutralizer housing except for a rectangular opening through which electrons pass. Electrical connections for operating the neutralizer filament are shown in Fig. 4. One leg of the neutralizer filament is grounded to provide a return path for the emitted electrons. The neutralizer housing is also connected to ground. Electron emission from the heated filament is self-regulated by the extraction field at the filament surface generated by the positive potential sustained in the region of the charged microcluster beam.

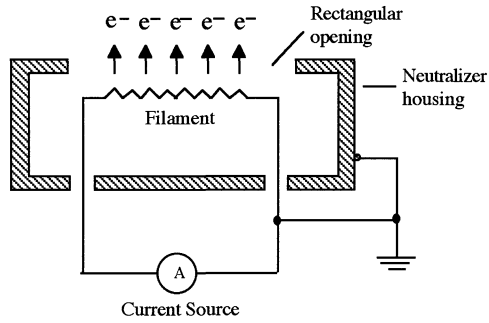

Fig. 4. Neutralizer assembly.

Wafer Neutralization Tests

Tests were performed to evaluate the effectiveness of the thermal electron emitter for preventing charge buildup on wafers exposed to the energetic, positively charged microcluster beams. Fig. 5 illustrates the experimental arrangement used to conduct these

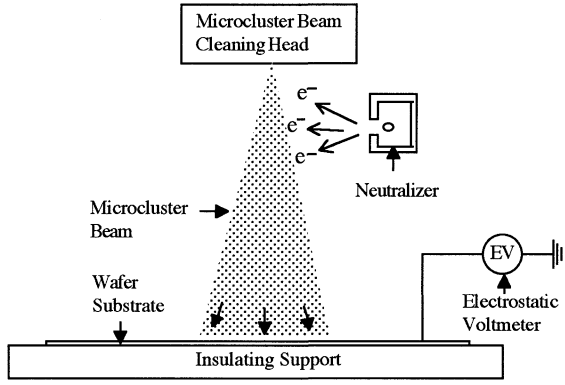

Fig. 5. Apparatus for measuring wafer charging.

tests. A patterned silicon wafer was mounted on a polystyrene platen to eliminate or minimize charge leakage from the wafer to nearby grounded surfaces. One lead of an electrostatic voltmeter, attached to the wafer surface, measured the potential rise due to accumulation of positive charge on the wafer surface. With the neutralizer off and the wafer exposed to a single emitter microcluster beam, the surface potential rose to +4.5 kV before discharging to the surroundings. The neutralizer was turned on and the electron emission varied by using different settings of the heater current. When the filament heating current was set to 9 amps, the wafer surface potential dropped to zero indicating that a sufficient number of electrons were pulled into the beam to prevent surface charging. The surface potential remained at zero even after two, three and four microcluster beam emitters were brought on-line, operating simultaneously. This indicated that the neutralizer was not emission limited but operating in the space charge limited mode (10). Surplus electrons

were extracted from the neutralizer controlled by the increase in the positive space charge density in the microcluster beam.

WAFER CLEANING STUDIES

A scanning electron microscope (SEM) was modified by mounting a microcluster beam cleaning head to a spare port on the SEM. Patterned wafer samples, diamond-scribed to generate a "wide trench" and surrounding debris particles, were placed in the SEM for cleaning. The wafer samples were exposed to a single 0.4 microampere beam accelerated by +17 kilovolts. Photomicrographs verified the in-situ removal of submicron particulates by visually inspecting the same local area on the wafer before and after microcluster beam cleaning. Particles removed, inside and outside of the scribed trench (4 micron wide by less than 1 micron deep), ranged in size from tens of microns to less than 0.05 microns. Fig. 6 is an SEM photo taken before cleaning and shows the wide range of particles generated from "trench" scribing. After exposure of the sample to the microcluster beam for five minutes, a second SEM photo, Fig. 7, was taken. Results show the cleaning action removed particles from a few microns down to the resolution of the microscope, estimated at 0.05 microns.

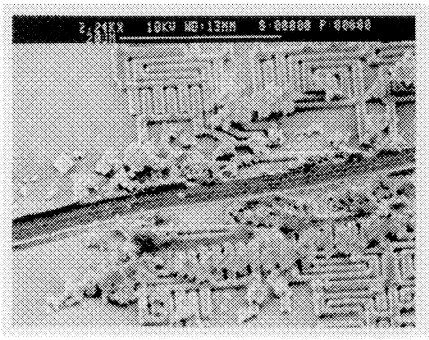

Fig. 6 Patterned wafer before cleaning.

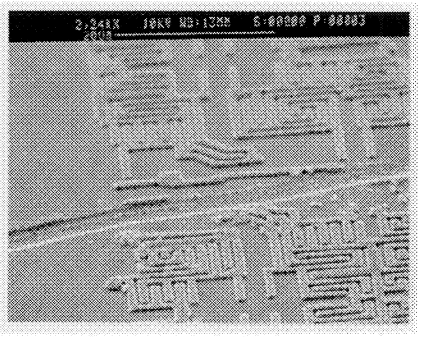

Fig. 7 Patterned wafer after cleaning.

SUMMARY

The microcluster beam cleaning process has demonstrated the ability to remove particulates from wafers less than 0.05 micron. Because of the cleaning mechanisms involved, no limit is foreseeable on particle sizes that can be removed, including surface metallic ion impurities. Compared to other cleaning methods, the process has several potential advantages. Microcluster beam cleaning is compatible with in-situ vacuum wafer processing steps. The cleaning head contains no moving parts and consumes ultralow quantities of cleaning solution - estimated at tens of microliters/wafer. During operation, the cleaning solution is not exposed to surfaces or components which could introduce secondary contaminants into the cleaning process. Compared to other cleaning processes, the capital cost of equipment is economical and the entire process consumes low power. A stand-alone cleaning system is projected to have a small footprint, 4'x4' or less.

Semiconductor wafer cleaning is only one of many potential uses for microcluster beam technology. Other areas of application pursued for microcluster beam cleaning technology

include flat panel display, photolithography masks, hard discs, MEMS devices, optical gyroscopes and space optics (windows, lenses, mirrors) in the aerospace arena.

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SELECTION OF POST PLASMA ETCH/ASH CLEANING METHODS USING A RESIDUE REMOVAL MODEL FOR INTEGRATED CIRCUITS BASED ON RESIDUE ELEMENTAL COMPOSITION

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A "Residue Removal Model" was developed to identify the best formulations for removing residues remaining on integrated circuits after plasma etch/ash processes. Auger Electron Spectroscopy (AES) coupled with metal and dielectric etch-rates determined for Al, Ti and SiO_2 led to a useful model. The model suggests that: 1) the composition of a cleaning formulation must be matched to the elemental composition of the residue, and 2) relatively high Al, Ti and SiO_2 etch-rates are required for successful residue removal, but must be balanced against underlying material etching. "Radar Plots" were used to compare various residue removal formulations.

INTRODUCTION

As semiconductor device dimensions continue to shrink, the importance of removing all plasma etch/ash residues without corroding these devices becomes even more critical. Until now, the industry has relied mainly on organic solvent mixtures to clean etch/ash residues from devices(1). There is a need to move away from these organic solvent mixtures for safety and environmental reasons. To meet these needs we have developed a series of new aqueous post plasma etch/ash residue removers known as the BAKER REZI™(2) product line that contain more than 80% water.

During the course of this work it became apparent that some residue removers cleaned post plasma etch/ash residues formed by certain processes more effectively than others. We have now developed a RESIDUE REMOVAL MODEL based on the results of Auger Electron Spectroscopy (AES) and thin-film and metal foil etch rates. While others have used AES to examine etch/ash residues formed by a single process(3,4), and other techniques such as Thermal Desorption Spectroscopy (TDS), X-Ray Photoelectron Spectroscopy (XPS), Energy Dispersive Spectroscopy (EDS), Fourier-Transform Infra-Red Spectroscopy (FTIR), Secondary Ion Mass Spectroscopy (SIMS) and Laser Ionization Mass Absorption (LIMA) have also been used to examine these types of residues(4, 5), we have combined AES data from several etch/ash processes for both metal-line and via processes to develop our model. This model enabled us to design the most effective formulations for removing the mainly inorganic residues found on devices after various plasma treatments used to remove bulk photoresist.

A common misconception about post etch/ash residue remover formulations is that they must have very low etch rates on the materials used in integrated circuits, or features will be damaged and device reliability affected. While low etch rates on materials such as Al, Al-Cu, Ti, TiN, W, Cu, Si and SiO_2 might be desirable from a reliability viewpoint, a balance must be maintained between removal of residues and underlying material etching. We have found that if the material etch rate is too low, particularly in the case of Al, Ti and SiO_2, the ability to remove post plasma etch residues on some samples will be lost. In the present work we have used our RESIDUE REMOVAL MODEL to determine the appropriate elemental etch rates required to remove these residues.

EXPERIMENTAL

Features from ten different wafer processes were used, vias V1-V5 and metal lines M1-M5. For V1-V4, wafers with unfilled vias were prepared by patterning and etching wafers with SiO_2/TiN/Al-Cu layers followed by an oxygen plasma ashing. The preparation of V5 was similar but employed intentional over-etching during via formation. Via dimensions were: V1 and V2, 0.35-0.50 microns; V3, 1.0 micron; V4 and V5, 0.5 micron.

For M1-M3, wafers with TiN/Al-Cu/TiN/Ti/SiO_2 layers were patterned, etched and oxygen plasma ashed to form 1.0 micron metal-line features. The preparations of M4 and M5 were similar, but employed intentional over-etching during metal line formation. Wafers M2 and M4 had significantly heavier residues on the metal lines than M1, M3 and M5.

Five J. T. BAKER formulations were used in the development of the RESIDUE REMOVAL MODEL. These were designated as R-1, R-2, and R-3, all BAKER REZI formulations, experimental hydroxylamine-based formulation X-1 and BAKER ALEG™-310(2). Comparisons were made to two competitive hydroxylamine-based products C-1 and C-2. Formulations R-1, R-2, and R-3 were each greater than 80% water. Formulations R-2 and R-3 contained additional components to enhance titanium removal. ALEG-310 is an amine/solvent-based residue remover/bulk photoresist stripper. Experimental formulation X-1 is a hydroxylamine-based formulation containing about 80% water. Competitive formulations C-1 and C-2 are also hydroxylamine-based, but contain less water (about 20%) as well as organic amines and catechol.

Etch rates were determined by weight or thickness loss or by analyzing solutions before and after metal contact using Inductively Coupled Plasma-Optical Emission Spectroscopy (ICP-OES). Scanning Electron Microscopy (SEM) micrographs were obtained using Hitachi S-4700 Field Emission (FE)-SEM and JEOL JSM-6100 SEM instruments.

AES was performed using a PHI-660 and field emission-AES was performed using a PHI-670, both at Charles Evans & Associates. Wafer samples V1 thru V5 had their vias cross-sectioned to expose the residues inside of the vias for AES analysis. Metal-line wafer samples M1 thru M5 were inspected at a 45° tilt to allow analysis of both side-wall and "fence" residues. Ar^+ sputtering was also used to remove approximately 50Å from the surface *in situ* to ensure that surface contamination was removed before AES analysis of the residues.

RESULTS AND DISCUSSION

AES Analysis of Post Plasma Etch/Ash Residues:

A summary of the AES results for post etch/ash residues found on the five metal-line wafers and five via wafers is shown in Table 1. Three elements (Al, Ti, and Si) were selected for incorporation into the model. The relative abundances of each of the three selected elements were then placed into one of three categories (low, moderate or high). Other elements such as C, O and N were also present. F was present in some of the via residues.

Formulation Etch-Rate Determinations:

Table 2 summarizes the Al foil etch rates of five of the formulations. ALEG-310 has the lowest Al etch rate of the formulations used to develop our RESIDUE REMOVAL MODEL. Formulation R-1 has a considerably higher Al foil etch rate, typical of the REZI formulations. The expected effect of temperature on the etch rates is also apparent. Table 3 lists the Al(0.5% Cu) thin film on Si etch rate determinations for R-1 and R-2. Table 3 also lists Al thin film on Si etch rates for R-1 which are similar to those found for Al(0.5% Cu) suggesting that Cu alloying in the film has little impact on the Al etch rates for formulation R-1. These thin film etch rates are considerably lower than the corresponding Al foil rates.

Table 4 summarizes the Ti foil etch rates of all the formulations used in this work. Formulation R-1 and ALEG-310 have the lowest Ti etch rates of the formulations used to develop our RESIDUE REMOVAL MODEL. The hydroxylamine containing formulations, R-3, X-1, C-1 and C-2 have considerably higher Ti etch rates. Table 5 lists the Ti thin film on Si etch rates for R-1 and R-2. The low Ti etch rates of formulation R-1 are again apparent. Similar to the Al thin film on Si etch rate determinations, Ti thin film on Si etch rates are lower than those measured using metal foil pieces.

Table 6 summarizes the SiO_2 etch rate determinations for all of the formulations used in this work. This table shows that X-1 at 65 °C has the highest silicon dioxide etch rate and that ALEG-310 at 85 °C and the competitive hydroxylamine-based products C-1 and C-2 at 65 °C have significantly higher silicon dioxide etch rates than any of the REZI formulations at 45 °C.

SEM Comparative Analysis of Residue Cleaning Ability:

Table 7 outlines the cleaning ability for the seven formulations on the five different metal-line and five different via patterned wafers. Treatment times of 30 minutes or less were used for each of the formulations. A time and temperature were selected that allowed maximum residue cleaning without significant etching or corrosion of the integrated circuit materials. The amount of etching or corrosion was determined using SEM micrographs.

FE-SEM inspection of cross-sectioned views of over-etched vias (V5) before and after cleaning with formulation R-1 indicated complete removal of residues. The over etch process

used to prepare V5 was shown to incorporate higher relative amounts of Al into the residues by AES (Table 1). We postulate that formulations with relatively high Al etch rates are required to clean this sample. Formulation R-1 etches Al at a relatively high rate (Tables 2 and 3) and successfully cleans V5 as shown by the SEM data.

SEM inspection using tilted views of the over-etched metal-line wafer sample M5 before and after cleaning with ALEG-310 indicated complete residue removal. The over etch process used in generating wafer sample M5 has been shown to incorporate higher relative amounts of silicon into the residues by AES (Table 1). We postulate that formulations with higher relative SiO_2 etch rates are required to clean this sample. ALEG-310 etches SiO_2 at a relatively high rate (Table 6) and successfully cleans M5 as shown by the SEM data.

FE-SEM inspection of cross-sectioned views of vias (V3) before and after cleaning with formulation R-2 indicated complete residue removal. The process used to generate wafer sample V3 caused the incorporation of higher relative amounts of Ti into the residues (Table 1). We postulate that formulations with higher relative Ti etch rates are required to clean this sample. R-2 etches Ti at a relatively high rate (Tables 4 and 5) and successfully cleans V3 as shown by the SEM data.

"Residue Removal Model" Expressed Using "Radar Plots":

The data outlined in Tables 1 and 7 have been combined into radar plot graphics (Fig. 1-4) to facilitate matching the cleaning potential of a formulation to the elemental composition of the residue. The radar plots are read as follows: The curved lines in the plots only serve to make it easier to follow where overlapping points occur. Each spoke in the radar plot represents a different wafer sample (M1-M5 and V1-V5). Each line at points 2, 3 and 4 represent one of the three elements and the solid shaded area at the center represents the cleaning ability of a formulation for a particular wafer sample. For the lines giving elemental information, "2" represents a low elemental content, "3" a moderate elemental content and "4" a high elemental content. The presence of a solid shaded area at the "1" position for a sample indicates that it was cleaned by that formulation in 30 minutes or less. The lack of a solid shaded area at the "1" position indicates that the sample was *not* cleaned with that formulation in 30 minutes.

Using this approach, Figure 1 shows that R-1 has strength for cleaning residues high in Al content and weakness for residues containing high amounts of Si or moderate to high amounts of Ti. Because of their lack of aggressiveness toward silicon, the BAKER REZI formulations have been shown to have excellent compatibility with low-k dielectrics, e.g., the sensitive material, hydrogen silsesquioxane(6). Figure 2 shows that ALEG-310 has strength for cleaning residues high in Si content and weakness for residues containing high amounts of Al or moderate to high amounts of Ti. Figure 3 shows that R-2 and R-3 have very similar cleaning performance. Both have strength in cleaning residues high in Al and Ti content and weakness for residues containing high amounts of Si. Figure 4 illustrates the performance of the hydroxylamine-containing formulations C-1 and C-2. These show strength for cleaning residues high in Si and high in Ti content and weakness for residues containing high amounts of Al. X-1 was similar to C-1 and C-2, but also cleaned V4 (Table 7) because of its higher Al and Ti etch rates.

CONCLUSION

Utilizing a RESIDUE REMOVAL MODEL, it is now possible to find solutions to residue cleaning problems which may involve changes in the wafer processing or in the cleaning formulation used. Highly aqueous formulations have been developed that effectively remove plasma generated residues comprising various combinations of the three elements that determine the difficulty of residue removal. Work is currently underway to extend the RESIDUE REMOVAL MODEL to copper-based metallizations.

ACKNOWLEDGMENTS

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Table 1: AES Results for Post Plasma Etch/Ash Residues						
Wafer	**% Ti**	**Residue Model Relative Amount Assignment for Ti**	**% Si**	**Residue Model Relative Amount Assignment for Si**	**% Al**	**Residue Model Relative Amount Assignment for Al**
M1	*	low	5.0	low	28	high
M2	0	low	18	moderate	8.0	low
M3	0	low	17	moderate	9.0	low
M4	0	low	27	high	6.0	low
M5	0	low	36	high	4.0	low
V1	2.0	moderate	16	moderate	8.4	low
V2	3.9	moderate	17	moderate	14	moderate
V3	12	high	16	moderate	14	moderate
V4	5.5	high	11	moderate	33	high
V5	0	low	22	moderate	38	high

*Sample drift during AES analysis of "fence" residues on top of metal-line resulted in detection of Ti from the underlying TiN layer. A low relative Ti content was inferred by results from formulations used in developing the "Residue Removal Model".

Table 2: Al Foil Etch-Rate Comparison of Formulations					
Temp. (°C)	**Al Etch-Rate (Å/hour)**				
	ALEG-310	**R-1**	**X-1**	**C-1**	**C-2**
85	1,200			3,400	3,100
65	210		2,700	730	800
45		4,600	0		
25		810			

Table 3: Thin-Film on Si Etch-Rate Comparison of Formulations			
Temp. (°C)	**Al(0.5% Cu) Etch-Rate (Å/hour)**		**Al Etch-Rate (Å/hour)**
	R-1	**R-2**	**R-1**
45	1,300 ±200		1,100
35	900		
30		570	
25	290 ±50	30 ±10	260

Table 4: Ti Foil Etch-Rate Comparison of Formulations							
Temp. (°C)	Ti Etch-Rate (Å/hour)						
	ALEG-310	R-1	R-2	R-3	X-1	C-1	C-2
85	<20						
65					6,800	2,400	990
45		30	120	2,000	2,600		

Table 5: Ti Thin-Film on Si Etch-Rate Comparison of Formulations		
Temp. (°C)	Ti Etch-Rate (Å/hour)	
	R-1	R-2
45	<2	80
25	<2	4

Table 6: Thermal SiO_2 on Si Etch-Rate Comparison of Formulations							
Temp. (°C)	SiO_2 Etch-Rate (Å/hour)						
	ALEG-310	R-1	R-2	R-3	X-1	C-1	C-2
85	12 ±1						
65	0.6 ±0.6				29 ±1	7.2 ±0.6	6.0 ±0.6
45		4.2 ±0.6	0	0	6.0 ±1.8		

Table 7: SEM Cleaning Results on Post Plasma Etch/Ash Wafer Samples							
Wafer	Formulation Cleaned Sample in 30 minutes or less?						
	ALEG-310 (85°C)	R-1 (20-45°C)	R-2 (20-45°C)	R-3 (20-45°C)	X-1 (65°C)	C-1 (65°C)	C-2 (65°C)
M1	NO	YES	YES	YES	NO	NO	NO
M2	YES	YES	YES	YES	NO	NO	NO
M3	YES	YES	YES	YES	YES	YES	YES
M4	NO	NO	NO	NO	NO	NO	NO
M5	YES	NO	NO	NO	YES	YES	YES
V1	NO	NO	YES	YES	YES	YES	YES
V2	NO	NO	YES	YES	YES	YES	YES
V3	NO	NO	YES	YES	YES	YES	YES
V4	NO	NO	YES	YES	YES	NO	NO
V5	NO	YES	YES	YES	NO	NO	NO

Figure 1

Figure 2

Figure 3

Figure 4

ISOTHERMAL EPI-SI DEPOSITION AT 800 °C

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ABSTRACT

In this work we present our investigation into the use of new cleaning procedures for low temperature epi. All cleaning sequences investigated were based on HF-last cleaning sequences for a short H_2 prebake epi process. We have investigated, SOM –HF, SC1-HF, HF only and HF/HCl combinations and investigated different rinsing procedures, rinsing times, rinsing pH modifications. We have determined the minimum H_2 prebake for these different cleaning strategies, the number of epi defects and the epi surface roughness. We have also examined the stability of these different surfaces in order to use these preclean strategies in an industrial environment.

INTRODUCTION

Conventionally, the epi pre-cleaning procedure ends with an RCA sequence. Then, the wafers typically undergo a H_2 bake at 1120-1170 °C for 90 s right before the epi deposition. Ideally the temperature of the bake should be reduced to the deposition temperature to achieve an isothermal process. The easiest way to decrease the H_2 prebake is to change the RCA cleaning sequence into an HF-last cleaning sequence. In a H_2 atmosphere, Si-F bonds dissociate at 930 °C, Si-C bonds dissociate at 1030 °C and SiO_2 bonds dissociate at 1060 °C. Therefore, traditionally, bake and deposition temperatures in excess of 1070 °C are being used. HF last cleaning processes have the potential of achieving a perfectly terminated Si-H surface and therefore, allow the bake/deposition temperature to be lowered substantially below 1070 °C. We have investigated, SOM –HF, SC1-HF, HF only and HF/HCl combinations and investigated different rinsing procedures, rinsing times, rinsing pH modifications. SOM refers to a Sulfuric acid solution saturated with O_3 gas (Sulfuric Ozone Mixture). We have compared an extensive list of cleaning performance metrics to formulate the best pre-epi cleaning process.

PARTICLE REMOVAL EFFICIENCY AND METALLIC IMPURITY ANALYSIS

We have compared the particle removal efficiency of different HF last cleaning processes by measuring the removal efficiency of city water contaminated wafers. All processes yielded removal efficiencies ranging from 93 to 98.7 %. We conclude that the particle removal efficiency is sufficient for

any of the different processes investigated and will not provide any distinguishing performance metric, since these pre-cleaning processes are usually not carried out on highly particle contaminated wafers. Next, We investigated the metallic impurity performance of different HF last processes and the metallic impurity removal efficiency of different HF-last processes. All metals are on the average for all processes in the $1*10^9$ at/cm^2 range using electronic grade chemicals in single pass mode. Multiple step recipes perform similar to simple recipes. This merely shows that there is no cross contamination from other experiments on clean wafers and that the process itself does not contribute to metallic contamination. Moreover, from these results is also clear that there is no metallic contamination contribution from the IPA dry. In a next set of experiments, we investigated the metallic impurity removal efficiency of different HF last recipes.
The results are shown in table 1.

Table 1. Metallic impurities on city water contaminated wafers. The reported values are averaged values over all measured points expressed in values of $1*10^{10}$ at/cm^2.

	TOFSIMS Li	TOFSIMS B	TOFSIMS Na	TOFSIMS Mg	TOFSIMS Al	TXRF K	Ca	Ti	Cr	Mn	Fe	Ni	Cu	Zn
Virgin Wafer	1	840	80	8.6	12.4	<	2.9	<	<	<	15	<	10	<
City water contaminated wafer	20600	1260	40000	71000	740	2567	42000	33	17	0.3	5	5.7	567	1100
SOM-HF/HCl-IPA dry	2.4	2.6	360	0.8	0.6	<	<	<	<	<	<	<	<	<
SOM-HF-IPA dry	1.4	1.8	200	2	1.4	<	11.7	<	<	<	1	<	<	<
SC1-HF/HCl-IPA dry	5	2.4	860	1.4	1	<	13	14	<	<	2	<	3.5	17
SC1-HF-IPA dry	4	4.4	80	2.8	0.8	<	2.7	<	<	<	0	<	2.3	<
SC1-HF-no rinse IPA dry	0.2	16.4	2.8	1.8	1.2	<	46	1.7	<	<	1	<	<	<
HF/HCl-IPA dry	3.4	5.2	720	2.8	1.2	<	2.7	<	<	<	1	<	<	<
HF-IPA dry	2.4	4.6	400	6.6	0.8	13	63	<	<	<	5	0.6	<	<

From table 1 it is clear that city water contamination leaves dominantly the light alkali and earth alkali metals on the wafer surface such as Li, Na, Mg, K and Ca. Additionally, city water deposits high amounts of Al and some Cu and Zn. Any of the wet chemical processes removes this contamination with efficiencies >99.8%. Furthermore, we can see that HF/HCl is more powerful [see also ref. 1,2] in removing metals from silicon surfaces than HF. The best overall process sequence for removing metallic impurities is SOM followed by HF/HCl. This is nothing more than the so-called IMEC clean and was reported before by Verhaverbeke et al. [2,3]. However, it is not clear if a difference in metallic impurity removal efficiency between 99.8 and 99.9% is still relevant for a pre-epi cleaning process, since usually wafers are not heavily contaminated with metals when these processes are applied.

SURFACE TERMINATION

In figure 1, the oxide, Si-H and F levels are shown as measured by TOFSIMS after different

preclean processes. Direct Displacement IPA dry without any rinse after the HF etch, leaves F on the surface, and the lowest oxide and highest Si-H termination. A DI rinse removes most of the F and exchanges it with oxide. Finally, a N2 dry leaves the least F. Interestingly, F was even found on virgin wafers. The stability of the surface passivation is dependent on the cleaning process. This is shown in figure 2. The wafer passivated with SC1-HF-no rinse- IPA dry is the most oxidation resistant up to 7 days of storage. After more than 7 days of storage, the oxidation resistance decreases. This shows that the highest level of SiH passivation with some level of F passivation, most probably at kink sites on the surface will increase the stability of the surface. A DI water rinse following an HF step decreases this stability by exchanging F with OH. The oxidation resistance increases with cleaning process as follows:
SC1-HF-N2 dry < SC1-HF-IPA dry < SC1-HF/HCl-IPA dry < SC1-HF-no rinse – IPA dry
It is clear that some reoxidation happens during a DI water rinse. In order to reduce this reoxidation during the final rinse, a closed system with point-of-use degassification in a single process vessel configuration provides the least amount of reoxidation. Alternatively, in a single process vessel configuration the IPA dry can be carried out immediately on top of an HF solution, without any water rinse. This can be done without particle addition as shown in figure 3. In this figure, the typical particle performance is shown for 25 wafers processed with HF/HCl followed by a Direct-Displace™ IPA dry where the IPA dry is carried out on top of the HF solution in the same process chamber. There was no rinse in between the HF etching and the IPA dry. The particles shown are particles > 0.16 μm. The average pre-count was 32 particles and the average delta is 1.32 +/- 7 particles. The highest delta is 12 particles added, which is below the spec limit of 30 particles added >0.16 μm. It is clear that a rinse is not essential in obtaining low particle counts after an HF etching and Si-H passivation.

LOW TEMPERATURE EPI PRECLEAN

Since for an epi preclean, the surfaces being treated, are normally not grossly contaminated, most different processes perform adequate in term of particle performance and metallic impurities performance. Therefore, the most distinguishing performance metric for selecting the proper cleaning process is the resulting surface termination. From the previous section, it is clear that the rinsing and drying are the most decisive elements in the cleaning process that determine the resulting surface passivation. Therefore, in order to investigate the cleaning for a low temperature epi process, we selected 3 different precleaning processes: SC1-rinse-HF-rinse-N2 dry, SC1-rinse-HF-rinse-IPA direct-displace™ dry and finally SC1-rinse-HF-IPA direct-displace™ dry (without rinse). The epi processes investigated included varying the bake/deposition temperatures between 700 °C and 900 °C.
In figure 4, the epi surface roughness is shown as a function of pre-clean process. In this case, only the drying process and the time between cleaning and epi bake/deposition was varied. The epi bake/deposition temperature was held constant at 800 °C. The roughness was measured with a Veeco TMS-2000 scatterometer. From this result, it is clear that for an 800 °C epi bake/deposition process, a more passivated surface and therefore, more stable surface allows a longer coupling time between clean and epi deposition. However, if very short coupling times are kept between the pre-clean and the epi deposition, even the N_2 dry process can yield good epi quality.

Finally, in Figure 5, the haze as measured with a Tencor 6200 is shown as a function of pre-clean and coupling time between cleaning and epi-deposition. Again, it is shown that the epi haze follows the same dependency as the surface stability after pre-clean. The haze increases steadily with coupling time

for all cleaning recipes. From this figure, one can see that the haze increase is the least for a SC1-rine-HF-IPA direct-displace^{TM} dry. This is the process, where the passivated surface, obtained during the HF etching is not exposed to rinse water after passivation.

OXYGEN FREE PROCESSING

Even though the degradation of the passivation of silicon surfaces during rinsing can be reduced by removing dissolved oxygen completely from DI water, there are some side effects of completely degassifying rinse water that should be taken into account. Metals are only soluble in ionized form, i.e. in a higher oxidation state. It is very important to keep metals ionized. This is usually accomplished by dissolved O_2. There are only a handful of metals, such as Au, which cannot be oxidized by O_2 and which are therefore prone to deposition on exposed silicon surfaces. If dissolved O_2 is removed from DI water, a solution is obtained which does not oxidize nor dissolve silicon at all, but at the same time a solution is obtained in which now almost all metals behave as noble metals when in contact with silicon. Even Fe is a noble metal in water which is completely deoxygenated and will plate out on silicon. This was reported by Greneche et al. [4].

$Fe^{++} + 2\,e^{-} \rightarrow Fe$ $\qquad E_o = -0.4$ V

$Si \rightarrow H_2SiO_3 + 4e^{-}$ $\qquad E_o = -0.8$ V

Dissolved oxygen is clearly a trade off: it keeps metals in solution by keeping them ionized, or oxidized, but it is also non-selective to silicon, i.e. dissolved oxygen will oxidize and dissolve silicon as much as it does other metals. Therefore, a small controlled amount of dissolved oxygen is desirable. Alternatively to oxygen, hydrogen can be added. Hydrogen has a lower oxidation potential than silicon ($E_o = 0$ V), but this is still high enough to keep many of the important metals in solution, i.e. ionized. Especially, Fe ($E_o = -0.4$ V) can be ionized by adding H_2 to the solution and this is one of the most important impurities in wet processing.

CONCLUSIONS

As a conclusion, we found that a simple 2 step cleaning process is recommended for a pre-epi cleaning process. There is no reason to use 3 steps or even longer cleaning processes. 2 of the best cleaning processes are SOM-HF/HCl and SC1-HF/HCl. SOM-HF/HCl has a slightly higher metallic impurity removal efficiency than SC1-HF/HCl, but it is not clear how relevant this is for a pre-epi cleaning process. Furthermore, we have shown that a Direct-Displacement^{TM} IPA dry on top of HF, skipping the rinse leaves the best passivated surface and the least amount of oxygen. Finally, we have shown that with an optimized pre-clean in a closed process chamber with single pass chemicals, an iso-thermal process at 800 °C is possible with coupling times between clean and epi deposition of up to 7 days.

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FIGURES

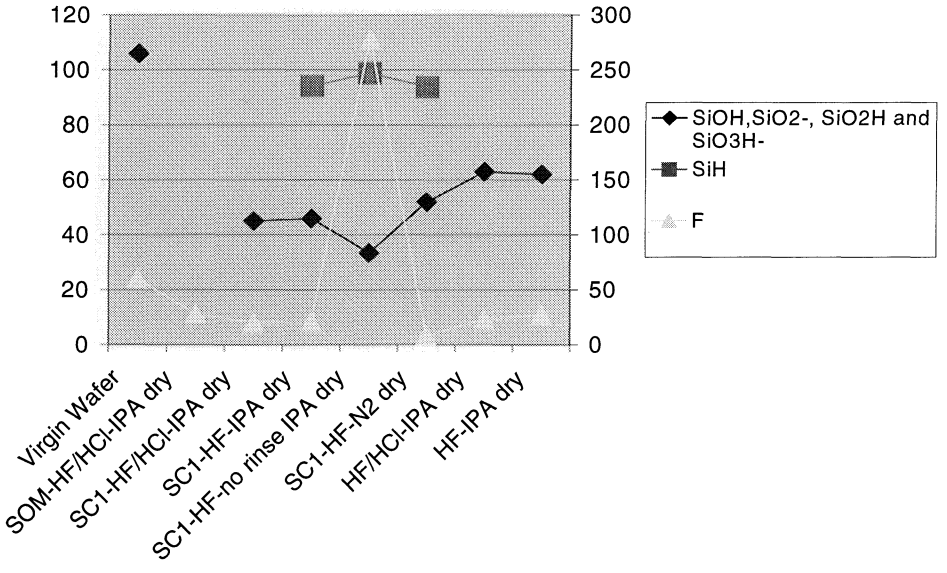

Figure 1. Oxide, SiH and F as % of Si signal measured by TOFSIMS

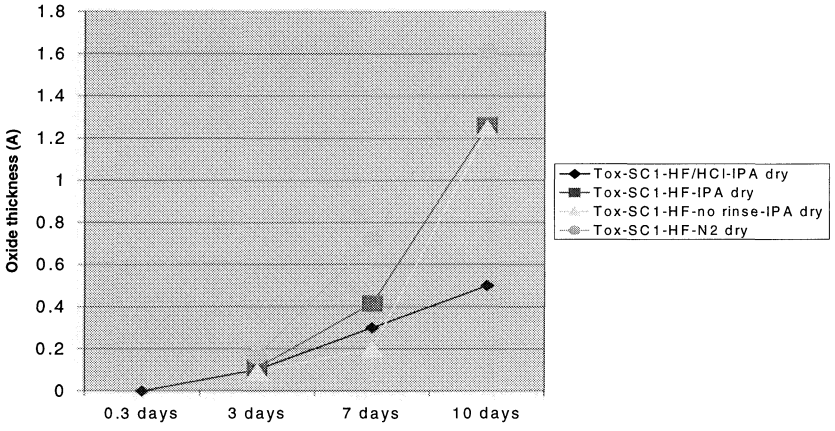

Figure 2. Oxidation Rate after cleaning

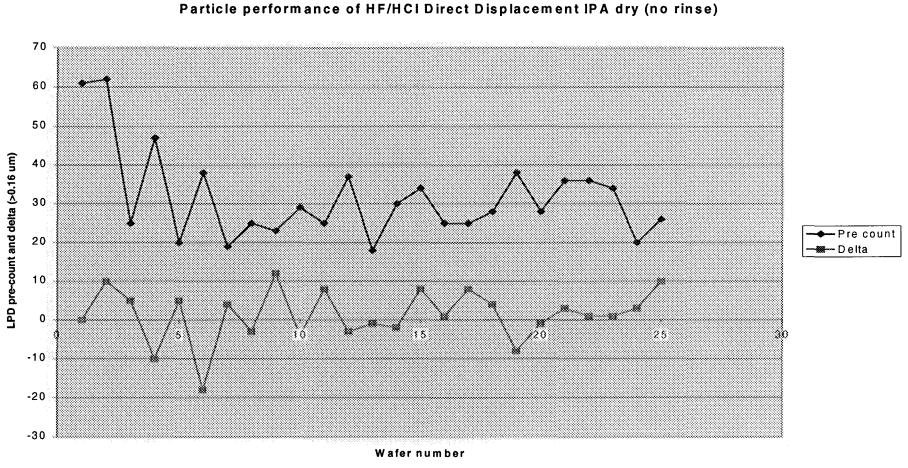

Figure 3. Particle addition after HF-IPA dry without rinsing

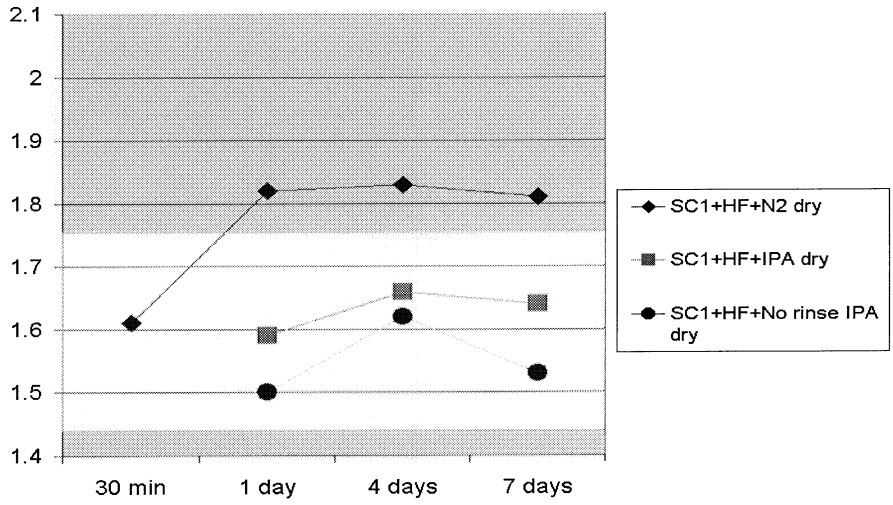

Figure 4. Epi roughness (Angstroms RMS value) as a function of Drying for a 800 °C process isothermal bake/deposition.

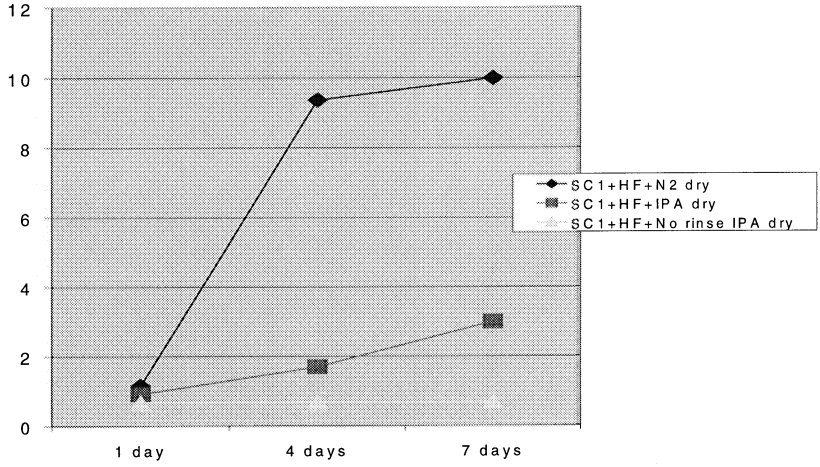

Figure 5. Haze on epi (ppm) as a function of drying technology and coupling time for 800 °C epi.

PARTICLE STUDIES

A NEW APPROACH FOR PARTICLE REMOVAL

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In this paper experimental and theoretical investigations are performed in order to understand the particle removal mechanism. The new theory presented here is based on a stochastic simulation method where the particle/substrate system is represented as two parallel planes of uniform surface charge. The influence of cleaning parameters such as pH, dielectric constant of media, bath temperature and valence, size and concentration of ions contained in the solution are studied under well controlled conditions and compared with simulation data. Results show that the conditions which favor particle removal are: high surface charge (small or high pH), dielectric constant, temperature, ionic strength, and a low counter-ion valence and small counter-ion radius.

INTRODUCTION

Small particles on wafer surfaces still represent a major limitation for device yields. Because of integrated-circuit down-sizing, the characteristic size of damaging particles is decreasings. As demonstrated by H. Krupp (1), the smaller the particles the more difficult they are to remove. Particle cleaning therefore has to be improved. Integrating colloid science in microelectronic cleaning processes therefore becomes necessary.

Much work has been done to describe the particle deposition mechanism from solutions on wafer surfaces using basic concepts of colloid chemistry and physics. Traditionally colloidal interactions are described by the DLVO (Derjaguin-Landau-Verwey-Overbeek) theory(2). In this theory the net attraction between two charged surfaces results in a competition between the attractive Van der Waals forces and the repulsive or attractive electrostatic contribution. This electrostatic term is calculated by solving the Poisson-Boltzmann equation for point-ions. This approach presents some limitations.

The electrostatic term in the DLVO approach is always repulsive between two charges of the same sign. But it has been demonstrated that attractive electrostatic interaction between two surfaces of the same electrical sign is possible as well(3) ! These surprising simulation results are already correlated with experiments(4). In fact the DLVO theory is strictly valid in case of large particle/substrate separation, monovalent ions, low surface charge density and high dielectric constant(5). As far as particle removal study is

concerned the hypothesis of large particle/substrate distance is not correct, since this distance is null at the beginning of the removal process.
In this paper, for the first time, an approach (well-known in biological and materials science) is applied in the field of micro-electronics in order to achieve a profound understanding of particle cleaning. The numerical simulations are validated from comparison with experimental data obtained under controlled conditions. The influence of parameters such as ionic strength, temperature, solvent dielectric constant, surface charge density, counter-ion valence and size is also studied, aiming at optimizing the cleaning solutions.

EXPERIMENTAL

All the experiments are performed in a class 1 clean room on Silicon substrate [p-doped, (100)-oriented, 200 mm] covered with a TEOS silicon oxide (TetraEthOxySilane). The wafers are intentionally contaminated by dipping in a DI water bath contaminated with studied particles. As the under-etching conditions play an important role, the different cleaning solutions used in the experimental tests are adjusted in concentration and time to etch exactly 50Å of PECVD TEOS oxide with the most similar etching rate possible (for one test).
The studied particles (0.2 to 2 μm) are made of Al_2O_3 from Duke Scientific Corporation, Si_3N_4 from Matthey Regent or home-made SiO_2 particles obtained by scraping the TEOS wafer surface. The particle surface charge is characterized by means of a Penkem 500 Zetameter. The TEOS layer charge is characterized using TEOS particles.
The particle contamination is measured by means of a 6420 TENCOR light-scattering device. The etching thickness is determined with a 1280 TENCOR spectroscopic ellipsometer.
For cleaning processes, a wet bench equipped with a filtered recirculation is used, which allows the particles to be removed from the bath. In addition the bath solutions can be heated. The cleaning solutions are prepared with 1 ppb grade chemicals.
Where no high-grade chemical was available, which was the case for potassium chloride (KCl), iso-propanol (IPA), formamide (CH_3NO) and furfural ($C_5H_4O_2$), the cleaning solutions were recirculated and filtered extensively (12 hours) before being used.

FORCES INVOLVED IN PARTICLE REMOVAL

In practice chemical cleaning consists in etching substrate and/or particle surfaces. Thus repulsive forces opposing the short range Van der Waals forces enable particles to be lifted off from the substrate.
In aqueous media, particle and substrate present some charges on the surface by electrolyte adsorption, dissociation or ionization of surface groups(6). When the particle starts to detach from the substrate, ions which have a charge of the same sign as the surface charge (counter-ions) can enter the separation space and the considered forces can then be calculated. As far as the removal study is concerned, the particle/substrate distances are so small that the particle surface in interaction with the substrate can be assimilated to a plane surface. In this study the surface charges (particle and substrate) have the same sign (repulsive system).
The particle is considered just above the substrate after the under-etching mechanism is performed. In fact what happens at particle/substrate separation less than 20 Å is not

studied here because other complex forces such as solvation, structural and hydration forces occur(2). Furthermore it would be necessary to take the variation of the media dielectric constant near the interfaces into consideration.
As shown in figure 1, different forces compete to generate pressure on the particles: Van der Waals(2), thermal (entropy), contact(7) and electrostatic pressures.

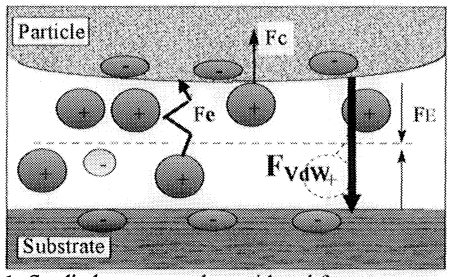

Figure 1: Studied system and considered force representations
(F_{VdW}: Van der Waals force, F_E : Electrostatic force, Fe :entropy, Fc : contact force)

The electrostatic pressure is defined from calculation of the Coulomb potential generated by all the electrostatic interactions in the system. This pressure is divided into 3 contributions: counter-ion/surface attraction and ion/ion plus surface/surface repulsions. Finally, the sum of all these pressures determines the attractive or repulsive behavior. The variation of one parameter can induce opposing effects in the 4 above-described contributions. Therefore it is impossible to predict the general tendencies without calculations.

SIMULATION

The particle/substrate system is modeled by two identical parallel planes with a uniform electrical charge density. The solvent is taken to be a continuous medium without local variation of the dielectric constant near the interface. Simulations are performed using a statistical model based on a Monte-Carlo simulation(8).
The model can predict when particle removal is enhanced, in others words when the algebraic sum "S" of the different pressures is maximum (the Van der Waals pressure is directly calculated).

$$\text{Total pressure} = S = P_{\text{electrostatic}} + P_{\text{hard core}} + P_{\text{thermal}} + P_{\text{Van der Waals}}$$

Throughout the removal process, the particle/substrate distance increases. Therefore we have to consider a dynamic mechanism for particle removal. In particular, we can imagine that one critical step occurs near the beginning when the particle/substrate distance has not yet reached the equilibrium point where the Van der Waals pressure is annulled by the other pressures. During this step, competition between under-etching and re-adhesion probably occurs.

In this first simulation, the different pressures have been calculated at one distance only: 20Å. Therefore our calculations can only give a partial indication as the whole removal process is not considered. i.e correlations between experimentals and this model can only be performed in terms of tendencies.

RESULTS AND DISCUSSION

One parameter only is modified each time from a reference set of experimental and calculation conditions. The reference conditions are given in table I.

EXPERIMENTAL	SIMULATION
- Etched thickness = 50Å - Material layer = PECVD TEOS oxide - pH<2 or pH>10 (repulsive conditions)[13] - Initial particle number on wafers ~ 3000	- Monovalent ions - Ion radius = 2.5Å - Particle/substrate distance = 20Å - Dielectric constant = 78.5 - Surface charge = 1.58 10^{14} cm^{-2}
- Temperature = 298 K - Ionic strength = 2 10^{-2} M (adjusted by adding KCl).	

Table I : Reference conditions used in this work

Influence of the etching rate

During the removal process, a competition between under-etching and re-adhesion probably occurs at a small distance when the particles start to lift off. Figure 3 shows that particle removal is in fact improved when the under-etching rate is increased and a minimum of 50Å is necessary to be etched on oxide.

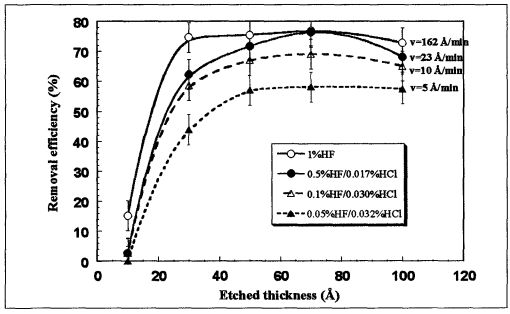

Figure 3 : Influence of the etching rate and etched thickness on the cleaning efficiency (pH= 1.42 and ionic strength = 0.024 M are kept constant).

Influence of the surface charge density

The influence of the surface charge density was studied by varying the pH of different etching solutions. The charge density was characterized by Zeta potential measurements. As demonstrated in figure 4, a higher absolute value of the Zeta potential experimentally leads to a higher particle removal efficiency.

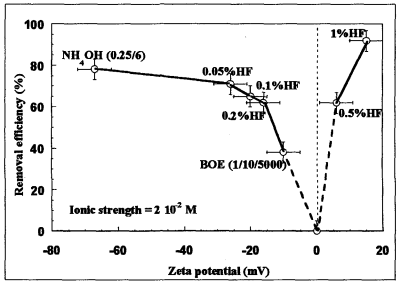

Figure 4 : Influence of the surface charge on the cleaning efficiency

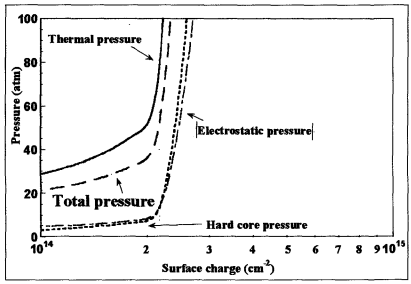

Figure 5 : Pressure calculation as a function of the surface charge

As seen in Figure 5, the tendency of the simulations is in good agreement with experimental data.
The competition between the attractive electrostatic and the repulsive thermal and contact contributions finally gives a better repulsion.

Influence of the dielectric constant

As shown in figure 6, the particle removal efficiency is drastically enhanced by using high dielectric constant solutions.

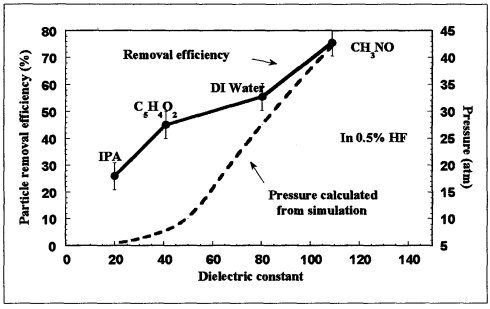

Figure 6 : Dielectric constant influence on particle removal efficiency and total calculated pressure

The simulation results are set out in the same figure 6. They show the same tendency as the experimental data. Indeed the dielectric constant which represents the ability of the media to screen the electrical field contributes to decreasing the attractive electrostatic pressure and increase the thermal repulsion. The practical consequences of this behavior are limited as it is difficult to use non-aqueous solutions.

Influence of the bath temperature

Figure 7 depicts the influence of the bath temperature on the particle removal efficiency and on the total pressure. For simulation, the water dielectric constant parameter which decreases with increasing temperature(9) is adjusted. Results demonstrate that a

temperature increase enhances the particle removal efficiency. These experimental results cannot be predicted by our model because for temperatures lower than 80°C a very modest repulsive total pressure only is calculated.
The experimental results can be explained by the etching rate increasing with the temperature which cannot be uncoupled.

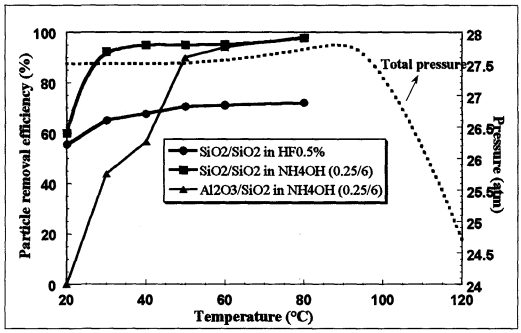

Figure 7: Influence of temperature on cleaning efficiency and interaction pressure

Influence of counter-ion valence

The graph in figure 8 shows the theoretical and experimental influences of the counter-ion valence. The co-ion used is Cl^-.

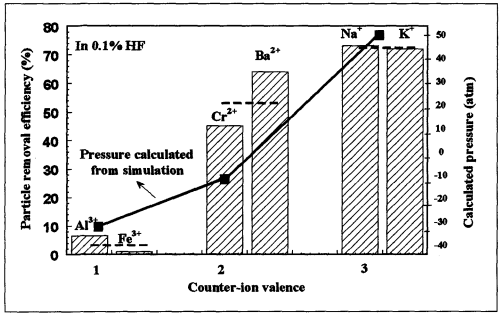

Figure 8 : Counter-ions influence on the particle removal efficiency and simulation results

Results demonstrate that when the counter-ion valence is greater than one, particle removal efficiency is drastically decreased. As predicted by simulation for counter-ion valences of 2 and 3, the system becomes attractive which explains this experimental behavior. This results from ionic correlations which enhance the electrostatic attraction. Therefore in order to optimize cleaning efficiency, solutions containing monovalent counter-ions must also be used.

Influence of counter-ion size

Figure 9 depicts the influence of counter-ion radius on particle removal efficiency. Results show that the larger the counter-ions, the worse the particle removal efficiency.

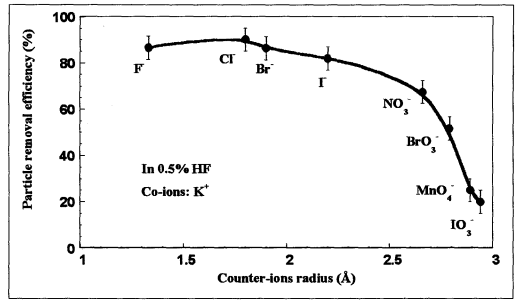

Figure 9 : Influence of counter-ion size on cleaning efficiency

The simulation is not in agreement with this result. The discordance between experimental data and simulation is due to the fact that our plane/plane system is considered as being infinite. Indeed Delville(10) demonstrated, by means of simulation of two charged disk systems neutralized by monovalent counter-ions, that the number of confined counter-ions varies as a function of the interdisk separation. As a result, if the net force between these two interacting bodies depends only on the ionic density contrast (osmotic pressure) between the inter-disk region and the outside, the weak cleaning efficiency obtained with the larger counter-ions may result from some deficit of larger confined counter-ions.

Influence of the ionic strength of the medium

Figure 10 shows the particle removal efficiency as a function of ionic strength in several solutions commonly used in microelectronics.

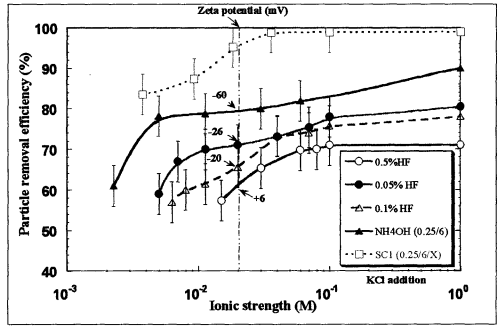

Figure 10 : Influence of the ionic strength on cleaning efficiency in different solutions

As experimentally demonstrated, a low ionic strength is favorable to optimize cleaning solutions which unfortunately limits the use of diluted chemistries. These results do not correlate with this first simulation because of the same reason as before.

CONCLUSION

In order to optimize particle cleaning solutions, several cleaning parameters are tested under well controlled conditions and compared with the theoretical results of a new physical model.
Simulations are in good agreement with experimental data for surface charge, dielectric constant and counter-ion valence parameters. For counter-ion size and ionic strength parameters, the experimental results can not be compared with this first simulation which does not consider the ionic density contrast between the inter-disk region and the outside.
Finally all of these results show that an optimized particle cleaning solution is a solution where particles and substrates have high zeta potential (same sign), which present a high concentration of small monovalent ions and the maximum of etching speed compatible with industrial equipment. Increasing the cleaning solution dielectric constant tends to improve particle removal as well but is difficult to achieve in practice.
All these results are valid in static media, i.e. without microstreaming flows generated by megasonics for example.

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Optimisation of dHF-based Cleaning Recipes: TO REMOVE OR NOT TO REMOVE A PARTICLE ?

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ABSTRACT

In this paper it is described how dHF-based cleaning recipes, such as the Imec-clean, have to be optimized in order to have a good particle removal performance and at the same time minimize the (re–)deposition of particles. The mechanism behind the deposition and removal of particles on a wafer surface is described in terms of van der Waals and electrostatic interaction forces. It is shown that the first oxidizing step during an 'Imec'-clean can chemically modify particles and hence influence the particle removal efficiency. In order to make the cleaning recipe independent upon this first oxidizing step and obtain an optimal removal for all kinds of particles and substrates, the final rinse step has to be optimized. This is achieved by rinsing at a low pH, where the electrostatic attraction forces are shielded, and in combination with megasonic irradiation to overcome the van der Waals attraction that otherwise will cause the particles to re-deposit.

INTRODUCTION

Particles are an important source of killer defects during IC manufacturing and with shrinking dimensions of the IC structures, the impact of particles upon device yield becomes more and more important. Therefore, there is a growing need for a more fundamental understanding of the factors that control the removal of particles on silicon wafers. This knowledge is required to engineer a cleaning mixture with optimal particle removal efficiency. In the traditional RCA cleaning cycle, particles are removed by the SC1-step (1). Low cost alternatives based on an oxidizing step (SPM, SOM or O_3-DI) followed by a dHF/HCl-etch step are introduced as a replacement and are implemented in *e.g.* the 'Imec-clean'-concept (2). Such novel cleans have to be optimized to demonstrate an excellent particle removal performance.

The dHF-step plays an important role for breaking the forces that are holding the particle on the wafer. This is accomplished by underetching (2) or by megasonic irradiation in combination with surfactants (3). Finally, the particle has to be lift-off from the surface by some kind of repulsive force in order to prevent re-deposition. So clearly, the dHF step plays a critical role in achieving a good particle performance. In this paper, it is shown that the final rinse conditions such as pH and the application of megasonic irradiation significantly influences the final amount of particles measured after a HF-clean.

As a model system, the particle removal is determined on thermal oxide substrates using different types of particles, namely particles that have a positive (Si_3N_4 and Al_2O_3) or a negative (PSL-spheres) charge over the pH range of interest and particles having the same charge as the oxide substrate (SiO_2) (see Figure 1). The mechanism behind the deposition and removal of particles on a wafer surface is described by taking into account

van der Waals interactions and electrostatic attraction/repulsion forces between the particle and the substrate. Using this basic model, the behavior of particles during different rinse treatments after dHF clean will be explained and an optimal final rinse-recipe is proposed in order to remove all particles using an 'Imec-clean' type of recipe.

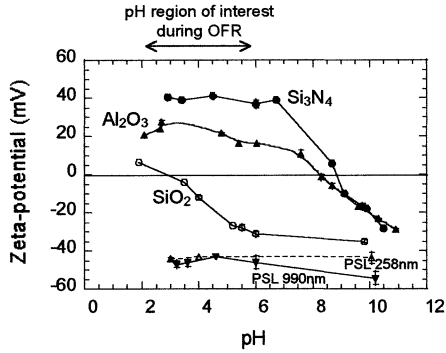

Figure 1: Zeta-potential of various particles as measured using electrophoretic light scattering (Nicomp Model 370 PSS).

EXPERIMENTAL DETAILS

Particle removal experiments

Particle removal is studied on 500 nm thermal oxides using an immersion based controlled contamination procedure. In Table I, an overview of the used particles and chemicals is given. The different cleaning sequences are evaluated in recirculating baths with filtration in a semi-automatic wet bench. Both the SOM (H_2SO_4/O_3 mixture) and SPM (1:4 H_2O_2/H_2SO_4 mixture) consist of a 10' immersion at 90 °C followed by a 15' overflow/quick dump rinse. O_3-DI water is at room temperature (± 10 ppm O_3 dissolved); moist O_3-gas was tested in a static tank at 90 °C (4). Two dHF-cleaning mixtures are tested, namely 0.5% HF (denoted as 'dHF') and 0.5% HF with 0.5 M HCl ('dHF/HCl'). The pH during the subsequent rinse is adjusted between 2 – 4 – 6 by spiking HCl in the rinse tank. The megasonic transducer in the overflow rinse bath is operated at 300 Watt. Final Marangoni dry is at the same pH as the overflow rinse.

Table I: Overview of particles and chemicals used for controlled contamination and cleaning experiments.

Chemical	Vendor/source	Quality
Si_3N_4-particles	Johnson Matthey	
SiO_2-particles	Rodel ILD1300 slurry	
Al_2O_3	Rodel	
PSL (258 and 990 nm)	Duke Scientific	
H_2O_2 30 %	Ashland	GB
H_2SO_4 95 %	Ashland	GB
HCl	Ashland	MB
HF	Ashland	GB

Particle removal efficiencies are calculated by measuring particle counts before and after contamination, and after clean on a Tencor Surfscan 6400 or Tencor SP1[TBI] using:

$$PRE = \left(1 - \frac{After\_Clean - Before\_Cont}{Before\_Clean - Before\_Cont}\right) \times 100 \quad [1]$$

Calculation of interaction forces between a particle and a substrate

According to the classical DLVO-theory (5, 6), the main forces that are working on a particle in the vicinity of a surface are van der Waals interaction forces and electrostatic attraction/repulsion forces. The van der Waals interaction energy, corrected for retardation effects, between a particle (medium 1) and a flat surface (medium 2) in a liquid environment (medium 3) can be described by (7)

$$W_{vdW} = -\frac{A_{132}\,R}{6\,D} \cdot \frac{1}{1 + 14\,\frac{D}{\lambda}} \quad [2]$$

with A_{132} the effective Hamaker constant, R the radius of the particle, D the distance between particle and surface and λ the characteristic wavelength for interaction (~90 nm). The effective Hamaker constant A_{132} for the different particle/substrate combinations interacting across water depends upon the materials that are interacting and is calculated from the individual Hamaker constants according to (8)

$$A_{132} = \left(\sqrt{A_{11}} - \sqrt{A_{33}}\right)\left(\sqrt{A_{22}} - \sqrt{A_{33}}\right) \quad [3]$$

with A_{11} and A_{22} the Hamaker contstants for respectively the particle and the surface, and A_{33} the Hamaker constant for the liquid.

Table II: Calculated Hamaker A_{132} constants for two media interacting across another medium.

Substrate-medium-particle	A_{132} (J)
SiO_2-H_2O-SiO_2	$3.4\ 10^{-21}$
SiO_2-H_2O-Al_2O_3	$1.07\ 10^{-20}$
SiO_2-H_2O-PSL	$3.9\ 10^{-21}$
SiO_2-H_2O-Si_3N_4	$1.6\ 10^{-20}$

The electrostatic interaction energy, which arise between charged surfaces, can be either positive or negative and is given by (9)

$$W_{el} = \frac{\varepsilon R}{4}\left(\Psi_0^2 + \Psi_{part}^2\right)\left\{\left(\frac{2\,\Psi_0\Psi_{part}}{\Psi_0^2 + \Psi_{part}^2}\right) \cdot \ln\left[\frac{1 + \exp(-\kappa D)}{1 - \exp(-\kappa D)}\right] + \ln\left[1 - \exp(-2\kappa D)\right]\right\} \quad [4]$$

with ε the permitivity of the medium (7×10^{-10} F m^{-1}), Ψ_0 the surface potential of the surface, Ψ_{part} the surface potential of particle and κ the Debye-Huckel inverse double-layer thickness. The surface potentials are approximated by their zeta-potential (*i.e.* the potential at the shear plane) determined by electrophoretic light scattering (Figure 1). The Debye-Huckel inverse double-layer thickness can be calculated as

$$\kappa = \left(\frac{2000\,e^2\,N_A\,I}{\varepsilon\,k\,T}\right)^{1/2} \quad [5]$$

with I the ionic strength and T the temperature.

RESULTS AND DISCUSSION

Effect of pH and megasonic irradiation during final rinse

The particle removal efficiency from oxide substrates using dHF or dHF/HCl clean followed by final rinse at different pH with and without megasonic irradiation, is summarized in Figure 2 for the different particles.

In absence of megasonic irradiation, it is observed that the removal efficiency increases for the positively charged Si_3N_4 and Al_2O_3-particles when the pH during the final rinse step is lowered and a better removal is obtained using the dHF/HCl-clean compared to the dHF-clean. A final rinse and Marangoni dry only (*i.e.* without a dHF-clean) cannot remove these particles from the substrate. As far as the removal of SiO_2-particles is concerned, the efficiency drops upon lowering the pH during final rinse. In this case, no difference between a dHF or a dHF/HCl clean is observed. Finally, for the negatively charged PSL-particles, at low pH during final rinse the removal efficiency decreases significantly for the 258 nm spheres. The 990 nm particles are found to be easily removed for all pH values.

In order to explain the observed effect of the pH during overflow-rinse upon the particle removal efficiency, it is assumed that the majority of the particles (if not all) are carried from the dHF-bath to the overflow rinse tank via the carry-over layer. The actual particle removal requires then the transport of the particle through the static boundary layer away from the surface. Since the particles diffuse slower compared to small ions such as H^+ (diffusion constant for a 0.12 μm particle amounts to 10^{-12} m^2s^{-1} whereas for a H^+-ion the constant is 10^{-10} m^2 s^{-1}), it is likely to assume that, at the moment the ion concentration in the static boundary layer is the same as in the overflow-rinse bath, the particle would still be close enough to the surface to experience interaction forces with that surface. A more exact and quantitative description involves the calculation of the interaction forces as function of time (*i.e.* changing pH, HF-concentration, ionic strength ...) and the solution of the resulting diffusion equation which is a rather difficult task.

The van der Waals and electrostatic interaction energies calculated as function of separation distance between particle and substrate for different post-rinse conditions are represented in Figure 3. The total interaction energy being the sum of both the van der Waals and the electrostatic interaction is also indicated. At very close separation distances (below 3 nm), this total interaction energy may deviate from the 'real' interaction due to short-range solvation forces (10). However, by taking into account only the van der Waals and electrostatic interaction between the particles and the substrate, the observed trends as function of pH can be readily explained:

For the positively charged particles, such as Si_3N_4 and Al_2O_3, at a pH above the iso-electric point of SiO_2-substrate where both the particle and the substrate have opposite charge, an electrostatic attraction dominates resulting in low removal efficiencies. When the pH is decreased, the electrostatic attraction is shielded and replaced by a small electrostatic repulsion (both the particle and the substrate bear the same charge) resulting in a better removal. However, due to the relatively high ionic strength, van der Waals attraction is still present which will cause not all of the particles to be removed from the surface (only ± 75 % removal).

SiO_2-particles have always the same charge as the SiO_2-substrate, consequently the electrostatic interactions are always favorable. When the pH is lowered, this electrostatic repulsion becomes less important due to screening of the double-layer interactions at high

ionic strength. Consequently, upon lowering the pH, the van der Waals attraction starts to play a role resulting in a decrease of the removal efficiency.
For the negatively charged PSL-spheres, there is a strong electrostatic repulsion at high pH giving a good removal. When the pH is lowered, electrostatic attraction is added up to the van der Waals attraction and the removal decreases significantly. This decrease in removal efficiency, however, is not observed for the bigger 990 nm PSL-particle (for which the electrostatic repulsion also exists...).
The application of megasonic energy in the overflow-rinse bath significantly improves the particle removal and is needed to overcome both van der Waals and electrostatic attraction forces. In addition, PSL-spheres and in a lesser extent SiO_2-particles can be removed by a rinse only (no dHF-clean) if megasonic irradiation is available indicating that these particles are very loosely bound to the oxide substrate.

Effect of first oxidizing step upon particle removal efficiencies

Si_3N_4 and SiO_2 particle removal efficiencies for different 'Imec-clean' type of recipes consisting of an oxidizing step (SOM, SPM, O_3-DI or O_3-gas) and a 0.5 % HF/0.5 M HCl-clean are summarized in Table III.

Table III: Si_3N_4 and SiO_2 particle removal from thermal oxide substrates using a 'Imec-clean' type of recipe followed by neutral or acidified rinse as measured on Tencor Surfscan6400 (>0.2 μm).

Recipe	Final rinse	Removal efficiency (%)	
		Si_3N_4	SiO_2
SPM + dHF/HCl	pH 6	37 ± 2	99 ± 1
	pH 2	84 ± 1	87 ± 1
	pH 1	10 ± 17	NM
SOM + dHF/HCl	pH 6	97 ± 1	100 ± 0
	pH 2	76 ± 3	86 ± 2
O_3-DI + dHF/HCl	pH 6	25 ± 1	NM
O_3-gas + dHF/HCl	pH 6	36 ± 4	NM
	pH 2	95 ± 3	88

Removal of Si_3N_4-particles using SPM as an oxidizing step is significantly improved by lowering the pH of the final rinse to pH 2; when the pH is lowered further to pH 1, the removal efficiency drops significantly. For SiO_2 particles a decreased removal is observed upon lowering the pH. This dependence upon the pH during the final rinse has been explained above. When an SOM is used, both Si_3N_4 and SiO_2 particles show the same pH dependence, *i.e.* decrease in removal efficiency at low pH. Ozonized DI water and moist O_3-gas as a first oxidizing step have a comparable effect as an SPM. These results suggest that Si_3N_4 particles are chemically modified by the SOM and most likely converted to SiO_2 or SiO_xN_y (11).

Implementation of optimized rinse conditions in 'Imec-clean' concept

The particle removal efficiencies determined using the full Imec-clean consisting of a SOM, hot QDR, dHF/HCl followed by the optimised final rinse (*i.e.* dHCl-rinse with megasonic irradiation) and Marangoni dry in an automated wet bench (see Table IV), show that all particle types can be removed with nearly 100% efficiency from various substrates (data from reference (12)).

Table IV: Removal efficiency of different particles with an Imec-clean run in a STEAG automated wet bench (Tencor Surfscan 6400 measurements).

	Particle removal efficiency (%)		
Substrate	Si_3N_4	Al_2O_3	SiO_2
Si	99	100	100
TEOS	100	99	100
SiO_2	100	100	100
Si_3N_4	94	98	100

CONCLUSIONS

It is shown that the first oxidizing step of an 'Imec'-clean influences the measured particle removal efficiency probably by modifying the chemical composition of the particle (and/or substrate). In order to make the cleaning recipe independent upon this first oxidizing step and obtain an optimal removal for all kinds of particles and substrates, the final rinse step has to be optimized. This is achieved *(1)* by rinsing at a low pH where the electrostatic attraction forces are shielded, and *(2)* by using megasonic irradiation to overcome the van der Waals attraction that otherwise will cause the particles to re-deposit.

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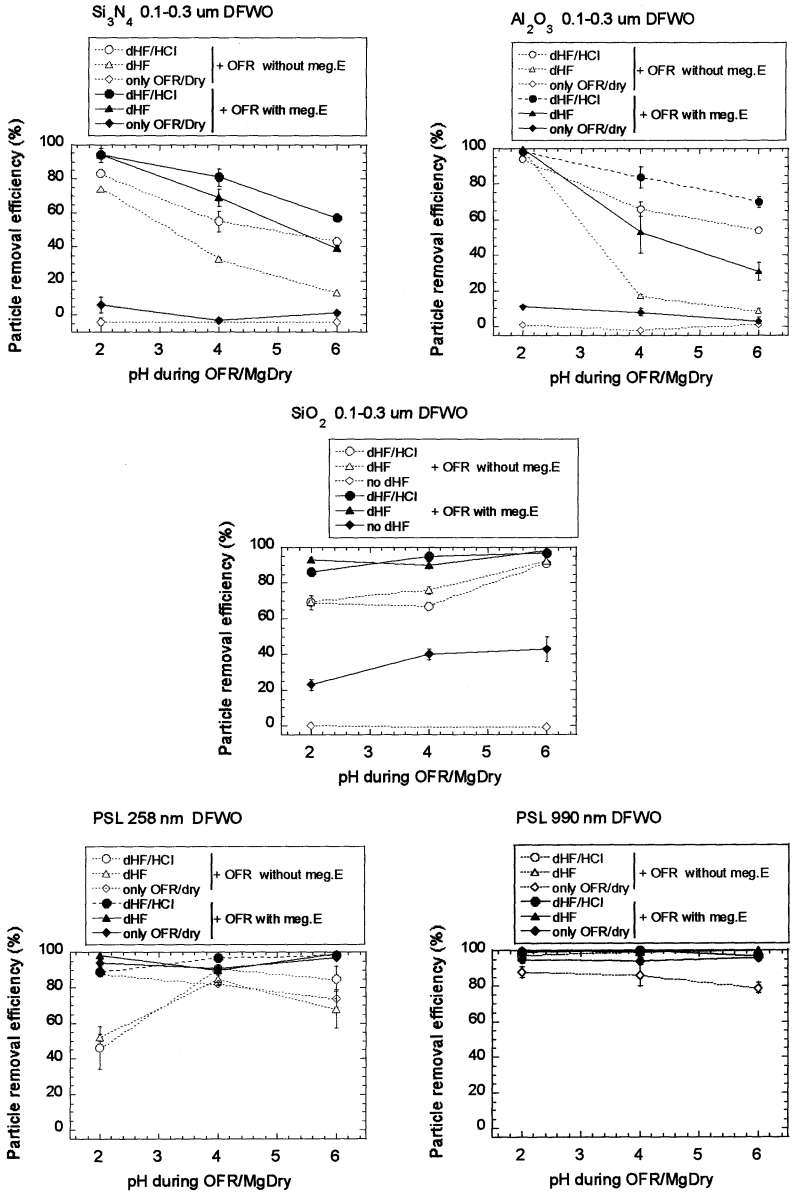

Figure 2: Si_3N_4, Al_2O_3, SiO_2 and PSL-particle removal efficiencies for different dHF-cleans as function of pH and megasonic irradiation during final rinse and Marangoni dry (Tencor $SP1^{TBI}$ – DFWO measurements).

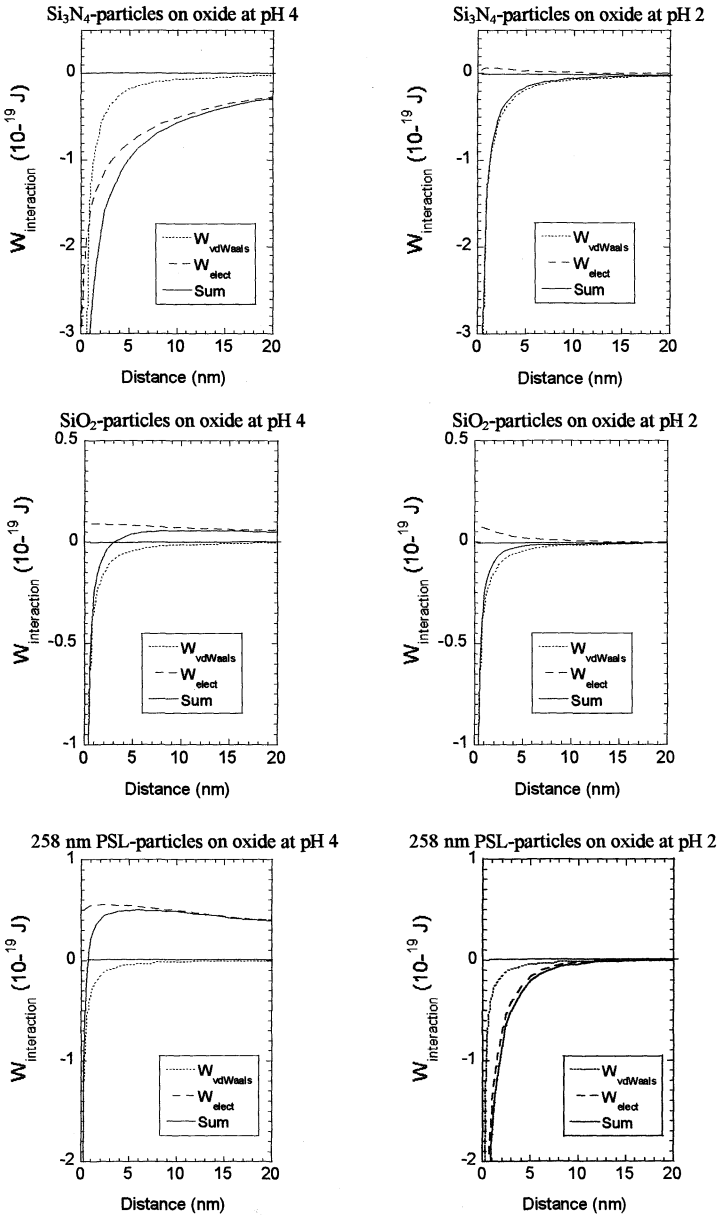

Figure 3: Calculated van der Waals, electrostatic and total interaction energy for Si_3N_4, SiO_2 and PSL particles with a thermal oxide substrate as function of separation distance.

METHOD FOR EVALUATION AND OPTIMIZATION OF PARTICLE REMOVAL PROCESSES

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ABSTRACT

An improved method for evaluating particle removal processes is presented that involves a new test-wafer preparation technique. Process particles are "dry" deposited using an electrostatic deposition tool, simulating real-world processes. Particles are deposited as monodispersed or polydispersed groups and their distribution is controlled to minimize background-particle "noise". Cleaning efficiency results are based on particle sizes determined using correlation curves that relate the deposited and scanner sizes for the appropriate process particles. The new technique successfully captures the effects of the removal mechanisms and allows meaningful comparison of diverse processes. Evaluations for a wet clean and a CryoKinetic clean are described, illustrating the technique.

INTRODUCTION

Results of particle-removal efficiency evaluations are routinely published in the literature for a variety of cleaning processes (1-10). It is not easy, however, to compare and contrast the results of these studies, since they differ from one another in several aspects. A significant difference, other than the cleaning mechanism itself, is the method of test wafer preparation. Differences also arise from the use of wafer scanners of different capabilities and calibrations. These issues make it difficult to identify and compare the true effects of the different particle removal mechanisms. Due to the continued interest in particle removal technology and the development of novel cleaning techniques, there is an urgent need for a test methodology that allows meaningful comparison of diverse processes.

Common test-wafer preparation techniques include "wet" methods such as spraying of a particle-laden solution onto the wafer using an atomizer (3) and dipping of a wafer into a solution containing suspended particles (11). The advantage of these methods is their simplicity. However, they may have certain undesirable effects such as alteration of the wafer surface by contact with the solution (a serious issue for hydrophobic wafers) and wafer "aging", i.e., increase in adhesion of the particles to the wafer surface with time. These deposition processes cannot therefore guarantee the similarity of test wafers, prepared independently or at different times, to the extent necessary for accurate comparison of different process results.

In this study, a new test-wafer preparation method is presented. The efficacy of this method is demonstrated through application to particle removal experiments in a wet clean and a CryoKinetic clean process.

METHODOLOGY

Test Wafer Preparation

The wafer preparation technique involves "dry" deposition of process particles (e.g. Si, SiO_2, Si_3N_4, W, Cu) using a commercially available tool (Model 2300 PSL/Process Particle Deposition System, MSP Corporation, Minneapolis, MN). The operating principle (12) of this tool is as follows (refer to the schematic in Fig.1). Particles are first dispersed in de-ionized (DI) water or another liquid and atomized to form a polydispersed aerosol. The aerosol is passed through a differential mobility analyzer (DMA) that allows only those particles that have the desired electrical mobility (particle size) to pass through. The concentration of the exiting monodispersed aerosol is measured in a condensation nucleus counter (CNC). The particles then enter the deposition chamber where they are electrostatically deposited onto the wafer. The DMA-indicated particle sizes are accurate to within 4% of the geometrical size measured using a scanning electron microscope (12). The particles are deposited either uniformly over the entire wafer surface (Fig. 2a) or in a specific spot of a few centimeters diameter (Fig. 2b). The spot technique can be used to deposit multiple regions of monodispersed particles on a single wafer (Fig. 2c). If desired, the DMA can be bypassed to deposit a polydispersed group of particles either in a spot or over the entire wafer surface.

There are several advantages to this deposition method. First, it is a "dry" technique in which the particles are more or less free of the liquid in which they were originally suspended. Therefore, no impurities from the liquid are deposited onto the wafer surface. Wafer "aging" is reduced (Separate experiments performed using this deposition technique to study CryoKinetic cleaning efficiency indicated this to be the case; – a more rigorous study is being performed to confirm this.) Further, since there is no direct interaction between the wafer surface and the liquid, the wafer surface condition is believed to remain unaltered (a desirable condition, particularly for hydrophobic wafers). A high degree of control is achieved over deposited-particle size and count, ensuring that the "noise" due to background particles is minimized. Finally, the dry deposition method better simulates particle deposition in real-world systems such as plasma-based etching and ashing tools, compared to conventional deposition methods.

Particle Sizing

The accuracy of particle-removal efficiency evaluation is improved through the use of calibration curves indicating the response of the wafer scanner to real process particles. The response curves are generated by depositing process particles of different sizes in monodispersed spots on a wafer and then sizing them using the scanner. The results for a scanner such as the KLA-Tencor Surfscan SP1^{TBI} for 0.06- to 0.6-μm sized particles are shown in Figure 3. It is observed from the plot that the sizes indicated by the scanner deviate quite significantly from the deposited (DMA-indicated) sizes for several of the particle types. Also, the curves for the process particles differ from that for PSL, which is

the standard particle used to calibrate the scanner. This is because process particles have refractive indexes and shapes, and hence scatter light differently compared to the PSL spheres. It is therefore critical that the cleaning efficiency results are based on a consistent representation of particle size (either the DMA size or the scanner size).

EXPERIMENT

The new methodology of test wafer preparation and particle sizing was applied to two typical particle removal processes: (a) an SC-1 based wet clean in a MERCURY® Surface Conditioning System, an acid spray processor and (b) a CryoKinetic clean ("cryo clean") in an ARIES® CryoKinetic Cleaning System.

Particle Removal Mechanisms

It is generally understood that in wet cleans based on SC-1 type chemistries, particles are removed by chemical attack of the surface oxide layer to which the particles are adhered (4). The particle removal ability of the chemistry may be independent of the particle material type, since it interacts more with the underlying oxide than with the particle itself. However, the overall efficiency of the particle removal process may be affected by particle redeposition due to zeta-potential-induced electrostatic attraction between particles and wafer surfaces, depending on the particle material type and wafer surface condition.

In the cryo clean, particles are removed primarily by impact of frozen aerosol clusters (8,9). The particle material density and size affect the impact force and thereby particle removal. The overall cleaning efficiency depends also on processes influencing redeposition, such as flow recirculation and thermophoresis (9).

Test Wafer Preparation

Prior to deposition, 200-mm-diameter bare silicon wafers were cleaned using the FSI B-Clean process (SPM, HF, SC-1, SC-2)[1]. Silicon nitride (Si_3N_4) and tungsten (W) particles were chosen for the tests. Identical sets of wafers were prepared for the two particle types for the two cleaning processes. For example, for Si_3N_4, six wafers (three spot-deposited and three full-deposited) were prepared for each of the two cleans. The spot-deposited wafers comprised four spots each (see Fig. 2c), corresponding to particles of size 0.064, 0.087, 0.107 and 0.202 μm, respectively. Each spot had approximately 5000 particles, yielding a distribution density of about 5/mm^2. The full-deposited wafers comprised a mixture of particles of sizes between 0.06 and 0.3 μm. The particle count varied between 26,000 and 55,000, yielding a distribution density of about 2/mm^2. The wafer preparation procedure for the W particles was identical to that for Si_3N_4.

Cleaning Recipes

For the wet clean, the recipe used was a modified (and less aggressive) variation of the FSI B-Clean, geared primarily toward capturing the effect of the particle removal mechanism. It involved the following chemistry: SC-1 ($NH_4OH/H_2O_2/H_2O$), HF, SC-1,

[1] SPM = H_2SO_4/H_2O_2, SC-1= $NH_4OH/H_2O_2/H_2O$, SC-2 = $HCl/H_2O_2/H_2O$.

SC-2 ($HCl/H_2O_2/H_2O$). For the cryo clean, a standard 3:1 mixture of argon and nitrogen was used as the cryogenic fluid.

Cleaning Efficiency Calculation

The cleaning efficiency was based on the particle counts indicated by the KLA-Tencor Surfscan SP1[TBI] wafer scanning system and was calculated using the following formula:

$$Efficiency = (N_d - N_c)/(N_d - N_i) \times 100$$

where N_i is the pre-deposition (background) particle count, N_d is the post-deposition count and N_c is the post-removal count. The measurements were made either within the wafer quadrant that included the spot region or over the whole wafer surface, depending on the deposition type. For the monodispersed particles, the DMA-indicated sizes were converted to the sizes indicated by the scanner, using the appropriate calibration curves from Figure 3. The cleaning efficiency for a given particle size was determined by combining results for the particle bins covering that specific size. The "oblique" mode of the scanner (capable of detecting particle sizes below 0.09 μm) was employed throughout the tests, for all particle sizes.

Results

The calculated cleaning efficiencies for Si_3N_4 and W are shown in Figures 4 and 5, respectively. The results indicate the following:

(a) The removal efficiency decreases with decrease in particle size, in general.
(b) Si_3N_4 particles appear to be easier to remove than W particles, in both cleans. For example, for the 0.064-μm spot-deposited particles, the efficiency is 95% for the cryo clean and 94% for the wet clean for Si_3N_4, and 91% and 76%, respectively, for W. For 0.202-μm spot-deposited particles, the removal efficiency is over 99% in both cleans, for both particle types.
(c) The cryo clean is more effective than the wet clean for W, whereas the wet clean is more effective than the cryo clean for Si_3N_4, for a given kind of particle distribution (full wafer or spot).
(d) The cleaning efficiency is higher for the spot deposition cases (again, more so for W than for Si_3N_4) compared to the full deposition cases.

The effects of the different cleaning mechanisms in the wet clean and cryo clean are evident from the above results.

Result (a) for the cryo clean suggests that the ratio of the removal force to adhesion force decreases with decrease in particle size. Since the particles are deposited in a "dry" manner, the adhesion forces are primarily of the van der Waals type and therefore proportional to the particle diameter (d_p). A simple model of impact-induced particle removal indicates that the impact force could be of the order of $1/d_p^4$ (13), supporting the hypothesis. Particle recirculation and redeposition due to thermophoresis may also affect the overall removal efficiencies at the smaller (particularly 0.064-μm) particle sizes. It is conjectured that for the wet clean, the decrease in removal efficiency with decrease in particle size is due to increased particle redeposition caused by zeta-potential effects.

Result (b) for the cryo clean is due to the lower material density of Si_3N_4, as compared to W. A model of particle removal by impact indicates that the impact force is proportional to $E_p^{2/5}/\rho_p$, where E_p is the modulus of elasticity and ρ_p is the density of the particle material. The values of E_p for Si_3N_4 and W are comparable. Therefore, the removal force is proportional only to the inverse of the material density. The density of Si_3N_4 is about 2.8 g/cc whereas that of W is about 19.3 g/cc. Thus, the impact force transmitted to the particle is lower for W, reducing its removal efficiency. In the wet clean, the observed lower removal efficiency for W may perhaps be due to the effect of particle redeposition due to particle charging (zeta potential). The net electrostatic attraction of W particles to the Si surface is probably greater than in the case of Si_3N_4, thereby reducing the net removal efficiency for W.

The greater effectiveness of the cryo clean for W and of the wet clean for Si_3N_4 [result (c)] again points to the removal and redeposition mechanisms discussed above.

The higher removal efficiencies for the spot-deposition cases [result (d)] can be explained in terms of the particle distributions obtained in the spot and full depositions. In the full-wafer case, the number of deposited particles is larger at the smaller particle sizes (see histogram in Fig. 2d). Even within a single bin (e.g., the 0.06- to 0.08-μm bin), the particle count is much higher at the lower size limit. The histogram for 0.064-μm spot-deposited particles (Fig. 2e), however, shows a distinct peak for the same bin, indicating the concentration of deposited particles of that particular size. The size distribution within each spot is quite narrow. Based on the theory of the DMA, the particle diameter range for the 0.064-μm particles is estimated to be ± 0.007 μm at the ± 3σ level. Since smaller particles in general have lower removal efficiencies than larger particles, and the number of smaller particles is greater in the full-wafer case for the same bin, the full-wafer case yields a lower removal efficiency value. The same effect is observed for larger particles as well (larger-size bins), but the increased flattening of the distribution within these bins for the full-wafer case and the naturally higher removal efficiencies at these sizes reduces the discrepancy between the spot and full-wafer results.

SUMMARY

A new methodology for particle removal efficiency evaluation was presented. The key features of this technique are as follows:

(a) It involves a new "dry" method for particle deposition on test wafers, simulating real-world particle deposition processes.
(b) It allows comparison of multiple cleaning processes and helps to determine if they have different underlying cleaning mechanisms.
(c) The accuracy and consistency of the cleaning efficiency results are improved through accurate sizing of process particles.

Application of the new method to the study of particle removal in an SC-1 type wet clean and in a cryo clean for Si_3N_4 and W particles of sizes 0.064 μm and larger revealed the differences in the two cleaning mechanisms. The removal efficiency for Si_3N_4 was 95% for the cryo clean and 94% for the wet clean, for the 0.064-μm particles. The corresponding values for W were 91% and 76%, respectively. The efficiency values were higher for larger particles, in both cleans.

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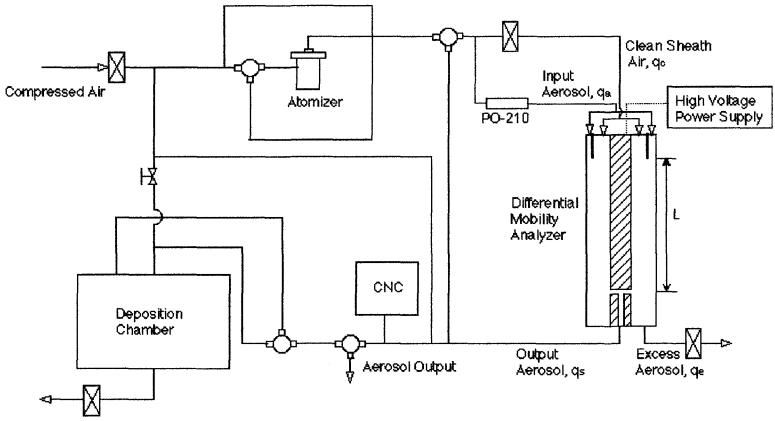

Figure 1. Schematic of the MSP-2300 system for dry deposition of PSL/process particles onto test wafers. The Differential Mobility Analyzer (DMA) controls the size of the deposited particles. Particle concentration is measured in the Condensation Nucleus Counter (CNC) before electrostatic deposition in the Deposition Chamber.

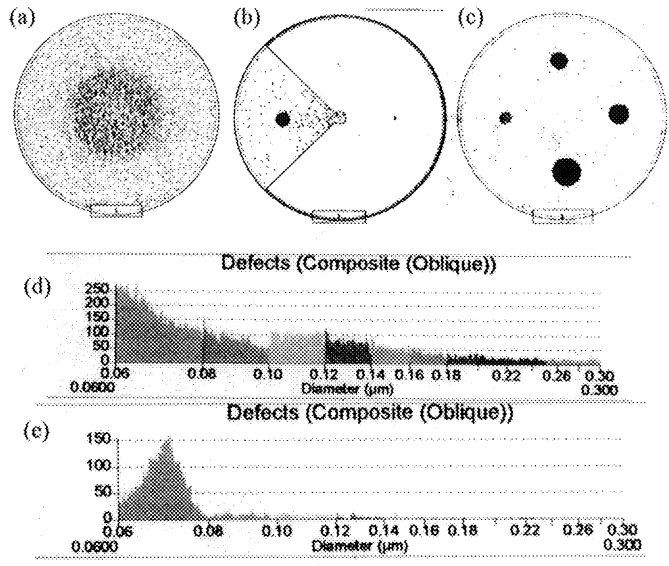

Figure 2. (a) Polydispersed full-wafer deposition (higher concentration in the center is due to the use of a showerhead of less than wafer-diameter size), (b, c) single and multiple monodispersed spot depositions, (d, e) histograms for (a) and (b), respectively.

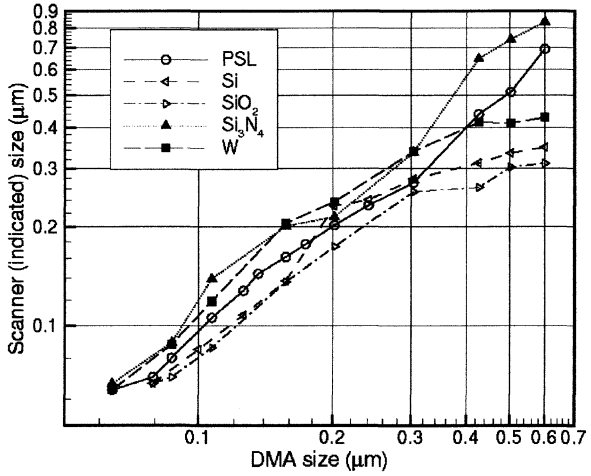

Figure 3. Correlation curves showing the size indicated by the KLA-Tencor Surfscan SP1^{TBI} wafer scanner vs. the size indicated by the differential mobility analyzer (DMA) of the MSP-2300 particle deposition tool, for various process particles. The curves are shown for the oblique mode of the scanner.

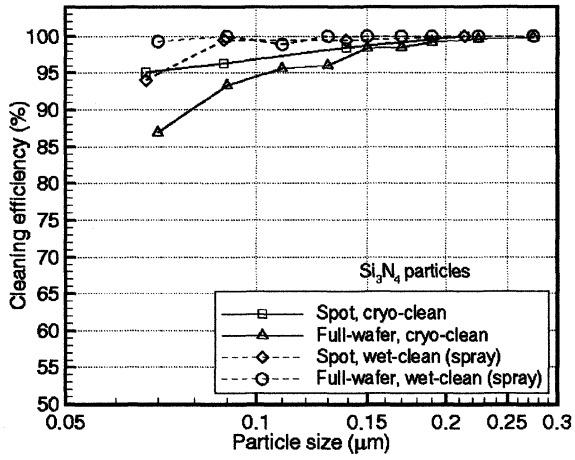

Figure 4. Removal efficiency results for Si_3N_4 particles in a CryoKinetic clean and a wet clean (a less aggressive version of the FSI B-Clean). In the legend, "Spot" indicates wafers with monodispersed groups of particles and "Full-wafer" indicates wafers with a polydispersed distribution of particles over the entire surface.

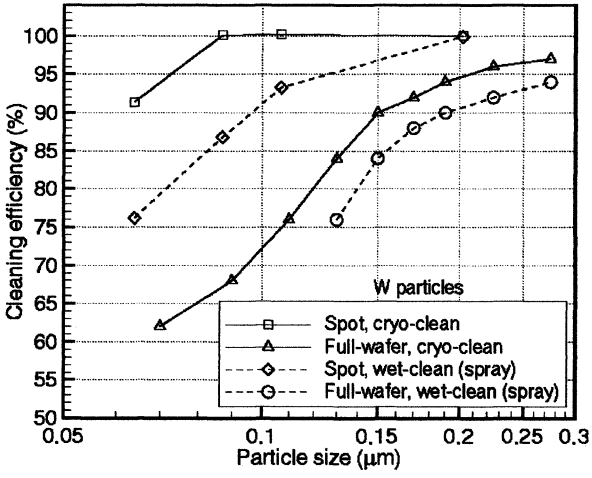

Figure 5. Removal efficiency results for W particles in a CryoKinetic clean and a wet clean (a less aggressive version of the FSI B-Clean). In the legend, "Spot" indicates wafers with monodispersed groups of particles and "Full-wafer" indicates wafers with a polydispersed distribution of particles over the entire surface.

LIQUID INFILTRATION AND PARTICLE REMOVAL FOR CLEANING IN DEEP TRENCHES

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Cleaning the deep, high aspect ratio trenches of highly integrated semiconductor devices is necessary for high device reliability. It was clarified that the dependence of the liquid infiltration and the particle removal on the microhole width using high aspect ratio model structures, enabling us to observe microhole interiors without braking them open. When a liquid such as ultrapure water (UPW) or buffered oxide etchant (BOE) does not form bubbles, it infiltrates completely into microholes. However, the infiltration rate ([infiltration length/microhole depth] x 100) of SC-1 (NH3/H2O2/H2O) is lower for narrower microholes, probably because of bubbles forming in the SC-1 solution, and it is difficult for SC-1 to remove particles in microholes.

INTRODUCTION

Highly integrated semiconductor devices, like 256 Mbit dynamic random-access memory (DRAM) and 1 G DRAM cylindrical capacity memory cells are expected to have high aspect ratio (depth/width) deep trenches (1,2). Contact holes are also expected to have a high aspect ratio. The ratio for 256 M DRAM is projected to be more than 5 (1). Contaminants like SiO2 residue and particles after wet etching (3), and sidewall polymers

after dry etching can significantly effect the quality of memory cells and device reliability. Cleaning high aspect ratio deep trenches is challenging because of the decrease in opening area. The objective of our research effort is to develop wet cleaning technology for the deep trenches of 4 G DRAM technology and beyond.

Wet cleaning of microholes and deep trenches includes liquid infiltration, removal by chemical reactions (e.g., etching), rinsing, and drying. In this paper, liquid infiltration into microholes and particle removal from them were investigated. High aspect ratio model structures were fabricated, enabling us to observe liquid infiltration and particle removal by optical microscope and SEM without breaking the model structures open. The dependence of the particle removal rate on the liquid infiltration rate is also discussed.

EXPERIMENTS

High aspect ratio model structures were fabricated to observe liquid in microholes and particle removal. Figure 1 shows the model structures. The inner and outer surfaces of the microholes are Si with native oxide. They were processed in SC-1 (NH3/H2O2/H2O, liquid temperature 60°C), buffered oxide etchant (BOE, HF/NH4=1/6, Olin Microelectronic Materials), and ultrapure water (UPW) for 15 min. After taking the model structures out of the liquid, we observed liquid infiltration into microholes with an optical microscope (Leica, model DMRM).

To make the photo resist residue model particles adhere in the microholes, the model structures were processed in photo resist (Shipley, Microposit S1813) diluted with acetone, baked for 2 min at 120°C and plasma ashed for 50 min (Drytec, DRLE100). After immersing the model structures in SC-1, we observed particle removal from deep trenches within the model structures using a SEM (Hitachi S-800).

RESULTS AND DISCUSSION

Liquid infiltration into microholes

Figure 2 shows the infiltration of SC-1 into microholes as observed by optical microscope. One side of the model structures is a thin Si3N4 layer of 0.025 μm thickness. Since this layer is transparent, we were able to observe microhole interiors without breaking them open. Figure 3 shows the liquid infiltration rate plotted as a function of the microhole width for both UPW and SC-1. We define the liquid infiltration rate as (infiltration length/microhole depth) x 100. For these samples (microhole depth equal to

2 μm) the infiltration rate of UPW was independent of microhole width. The same results were obtained for microholes 4 μm deep. We have also confirmed that BOE completely infiltrated into the microholes.

Figure 3 shows that the infiltration rate for SC-1 is lower for narrower microholes. The SC-1 infiltration is only about 25 % for a 0.2 μm opening width. However, the infiltration rate is about 75 % for 1-1.6 μm opening widths and is in good agreement with theoretical calculations based on capillary phenomena we are investigating. Because the SC-1 solution is more than 60°C, gas bubbles form, reducing the ability of gases trapped in the microholes to diffuse into the SC-1 solution (4). Figure 3 also shows that the infiltration rate for microholes with less than a 0.5 μm opening width decreased sharply. Possible explanations for this observation include:

1) Trapped gas bubbles force SC-1 out of microholes.

2) Bubbles adhering to the inside surfaces of microholes prevent SC-1 from infiltrating.

Particle removal from microholes

We also investigated the removal of particles from microholes using SC-1, and the dependence of particle removal on liquid infiltration. Figure 4 shows particles in microholes observed by SEM. Figure 5 shows the particle removal rate plotted as a function of the width of the hole for SC-1. We count microholes with no particles adhering before and after cleaning because it is difficult to count particles in microholes, as compared to counting particles on wafer. Therefore, we defined the particle removal rate as (the number of microholes with no particles adhering/ the total number of microholes) x 100.

Using diluted SC-1 solution (60°C, immersion time 20 min), the removal rate is about 5 % for particles in microholes of width 0.2 μm. Even using diluted SC-1 solution at 80°C (10 min), the removal rate is about 40 %. This is compared to more than 99.9 % removal of particles on flat wafers. We derived the wafer particle removal rate from the number of particles on the wafer and the inside areas of microholes.

We further qualified these results by classifying the appearance of microhole interiors as follows:

1) particles are completely removed; 2) a few particles (1-3 particles) remain; 3) more than 4 particles remain. Figure 6 shows the above -mentioned classification and figure 7 shows particle removal rate plotted as a function of SC-1 immersion time for several micro hole widths. Most of the particles at the bottom of microholes remain after cleaning. However, the particle removal rate increases with cleaning time.

A possible explanation for this observation is that the SC-1 solution contacts the bottom of microholes slightly in a short time because the turbulence caused by SC-1 gas bubbles forces some SC-1 to the bottom.

CONCLUSIONS

High aspect ratio model structures were fabricated, enabling us to observe liquid infiltration and particle removal by optical microscope and SEM without breaking the model structures open.

If a liquid like ultrapure water or BOE does not form bubbles, it infiltrates completely into microholes regardless of microhole width. However, the infiltration rate of SC-1 is lower for narrower microholes, probably because of bubbles forming in the SC-1 solution, reducing its removal of particles in microholes.

ACKNOWLEDGMENTS

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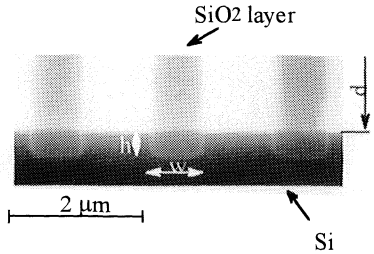
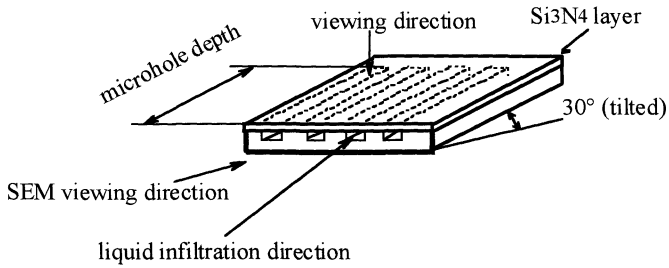


width h	width w	depth d
1.6	1.6	1-4
1.1	0.9	"
0.5	0.4	"
0.2	0.2	"

Unit : μm

(a) Cross section of model structure (b) Size of microhole



(c) Model structure

Figure 1 Model structure for observing liquid infiltration and particle removal

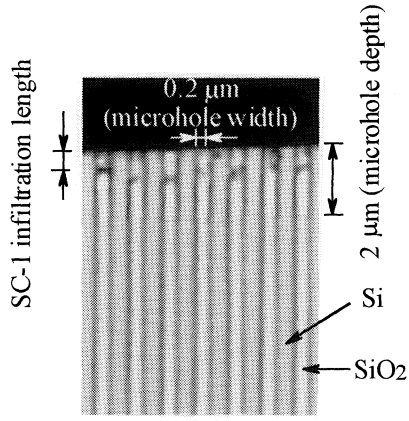


Figure 2 Infiltration of SC-1 into microholes

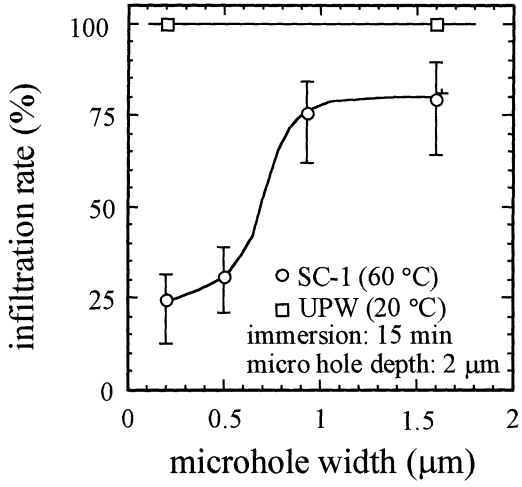
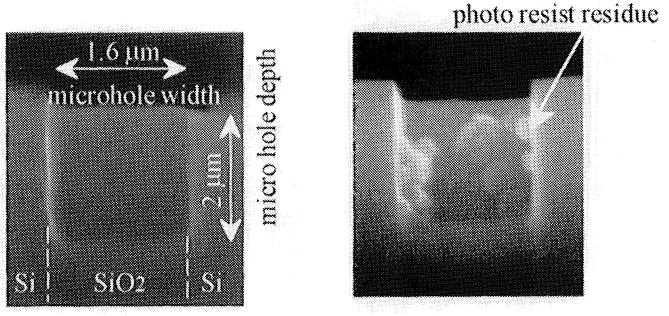


Figure 3 Infiltration rate of SC-1
infiltration rate=
(infiltration length/ microhole depth)x 100



(a) Initial (b) photo resist residue after plasma ashing

Figure 4 Photo resist residue in microholes

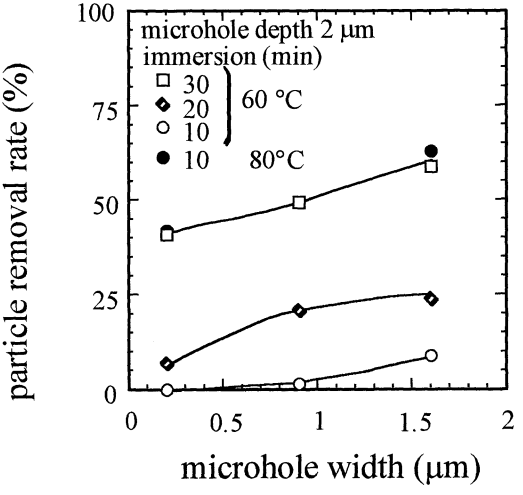
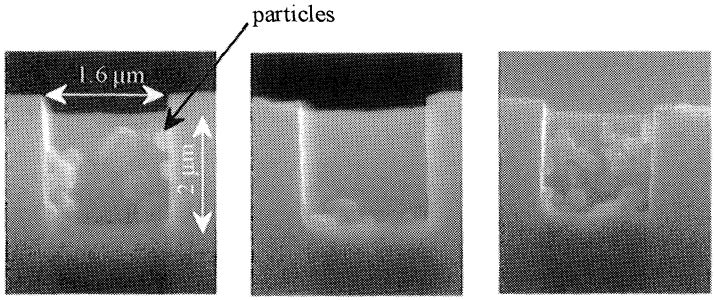


Figure 5 Particle removal rate of SC-1
particle removal rate=
(number of microholes with no particles adhering/ total number of microholes)x 100



(a) before cleaning by SC-1 (b) after cleaning (a few particles) (c) after cleaning (many particles)

Figure 6 Photo resist residue model particle in microholes

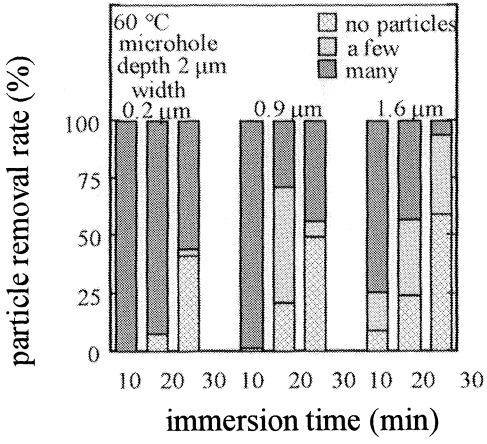


Figure 7 Distribution of particle removal rate for SC-1

ANALYTICAL STUDIES

THEORETICAL ANALYSIS OF THE ADHESION OF ASYMMETRICAL ALUMINA PARTICLES TO THIN FLIMS

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ABSTRACT

The removal of micron and sub-micron alumina particles from interlayer dielectric (ILD) and metal films represents a challenge in post-CMP cleaning. Proper modeling of the adhesive force between alumina particles and these films is needed to develop optimal solutions to post-CMP cleaning. We have previously developed and experimentally validated a model to describe the adhesion between spherical colloids and thin films. This simulation expands previous models to characterize the adhesive interaction between asymmetrical alumina particles, characteristic of a polishing slurry, and various films. Our simulation accounts for the contact area between particles and substrates, as well as the morphology of the surfaces. Previous models fail to accurately describe the contact of asymmetrical particles interacting with surfaces. Therefore, these models have typically underestimated the adhesive interaction between alumina particles and surfaces. By properly accounting for these parameters, the simulation predicts a more accurate adhesive force than predictions based upon an ideal van der Waals model.

INTRODUCTION

The removal of micron and sub-micron particulate contamination from inter layer dielectric (ILD) and metal films represents a challenge to post-CMP cleaning. Development of optimal methods for the removal of these particles is of significant value to the semiconductor industry. Improved understanding of the interactions that cause particle adhesion is key to the development of optimal cleaning methods. The dominant attractive force at close particle-substrate separations is van der Waals (vdW) interactions. Therefore, models to describe the adhesion for ideal systems have centered around modeling vdW interactions. These models include both ideal vdW models and equilibrium models (1-6). The appropriate equilibrium model depends upon the type of deformation a particle undergoes when in contact with a surface. A model developed by Johnson, Kendall, and Roberts (JKR) describes the adhesion interaction when particles deform elastically, and a model developed by Maugis and Pollock (MP) describes the adhesion interaction when particles deform plastically (4,5). Unfortunately, modeling adhesion is a complex problem that involves many variables. Therefore, these models are limited to describing ideal systems. Ideal systems are characterized by smooth, spherical particles interacting with smooth, rigid, flat surfaces, as seen in Figure 1A. However, particles deposited on wafer surfaces during CMP can not be classified as ideal. These particles are characterized by asymmetrical geometries, chemical and morphological heterogeneities, and varying mechanical properties. Figure 1B displays an alumina particle. This alumina particle is larger, but otherwise representative of the type of particles present on polished surfaces after CMP.

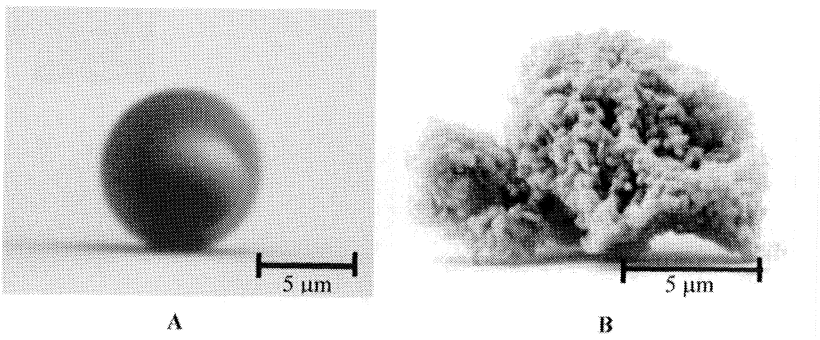

Figure 1: A: SEM image of a 5 µm PSL sphere on a silicon surface. B: SEM image of a 5 µm alumina particle in contact with a silicon substrate at 88 degrees tilt.

We have previously presented an expanded vdW model to describe the adhesion of non-ideal spherical particles to flat surfaces (7). Our expanded model accounted for both the morphology of the particle and the surface and mechanical properties of the interacting bodies. Our model displayed the significant effect of surface roughness on adhesion interactions. Using an atomic force microscope (AFM), we validated this model by measuring the adhesion interaction between rough polystyrene (PSL) spheres and rough and smooth silicon surfaces in aqueous media (8). We have since incorporated this model into a simulation that can predict the adhesion interaction for non-ideal particle/substrate systems (9). In addition to not being constrained to ideal systems, our

simulation offers several advantages. First, all parameters needed to predict adhesion interactions can be easily measured. Second, our simulation provides statistical information on particle adhesion. This is very important in the modeling of particle removal during post-CMP cleaning. It allows the user to determine a specific force necessary to remove a desired fraction of particles from the surface.

The basic procedure for our simulation involves determining the area in direct contact between a particle and a surface, constructing two solid surfaces (with desired roughness), bringing the surfaces towards each other so that vdW interactions may become important, and then summing the vdW interactions calculated for individual volume elements placed in one of the interacting surfaces.

Below we compare adhesion predictions from our simulation and from an ideal vdW model for the interaction of alumina slurry particles with SiO_2, W, and Cu films in air and liquid media.

EXPERIMENTAL PROCEDURE

The contact area between alumina particles and flat substrates and the morphology of the particles and substrates were measured by scanning electron microscopy (SEM) and atomic force microscopy, respectively. These parameters along with literature values for the elasticity (E, N/m) and the Hamaker constant of each material were then inserted into the simulation.

The contact area between an alumina slurry particle ($R \approx 0.15$ μm) and a flat substrate was estimated by measuring the contact area for model alumina slurry particles ($R = 5$ μm) through cross sectional SEM micrographs and scaling down.

The morphology of each surface was measured with a Molecular Imaging© AFM operated in contact mode. Three parameters were obtained that described the roughness of each surface: the average asperity height (ε_s, nm), the standard deviation in asperity height (std, nm), and the fractional coverage of the surface by asperities. The average asperity height and the standard deviation were determined by measuring the height of each roughness peak from a topographic AFM scan. The fractional coverage of the surface by asperities was determined by measuring the average number of roughness peaks per unit area, converting this number to an area, and dividing it by the scan area.

RESULTS AND DISCUSSION

The contact area of 50 alumina particles was determined from SEM micrographs. Figure 2 plots the frequency of occurrence of a given contact radius for R=5 μm alumina particles in contact with a silicon substrate. These particles are similar to alumina slurry particles used during CMP, as verified through field emission scanning electron microscopy (FESEM). The data displays an extended contact radius between particle and surface that slowly tails off. This extended contact area is not predicted by current models. An ideal vdW model would predict a singular contact point and equilibrium models can not be used to predict the interaction for asymmetrical or rigid particles. A normal distribution can not be employed to model the data because it would not accurately represent the extended tail seen in Figure 2. Both a chi-square and a F distribution can be used to model the data. These distributions tail off slowly, therefore more accurately represent the trend seen in Figure 2. Because a larger percent of particles can be expected to have extended contact area with the surface, a larger percent of particles would have a stronger adhesive interaction with the surface than would be

predicted by a normal distribution. The average contact radius between particle and surface is 2.26 μm. The average maximum possible contact radius, the length of the particle parallel to the substrate surface, is 9.4 μm. Scaled down to a 0.15 μm alumina slurry particle, the contact radius is 68 nm and the maximum possible contact radius is 282 nm.

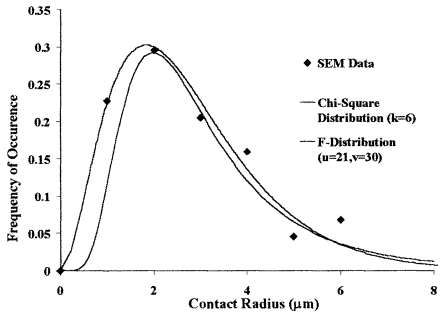

Figure 2: A plot of the frequency of occurrence as a function of contact radius (μm). This figure is for the interaction of R = 5 μm alumina in contact with a smooth silicon.

The roughness of alumina slurry particles and SiO_2, W, and Cu films after CMP was determined with an atomic force microscope. Table 1 lists the average roughness, the standard deviation in the roughness, and the fraction of the surface occupied by asperities for each surface.

Material	ε_s (nm)	Std (nm)	Frac. Coverage
SiO_2	1.7	0.7	0.01
Cu	53.8	25.2	0.33
W	139.8	78.1	0.80
Al_2O_3 particle	1.6	0.7	0.03

Table 1: The roughness of different surfaces.

It is important to point out that since the roughness on Cu and W substrates is comparable to the size of slurry particles, the shape of the slurry particles becomes important. Both the model and actual slurry particles exhibit a kidney shape, as seen in Figure 1B. Since the roughness for Cu and W films is comparable in size to the radius of the arc in the kidney shape, the area in contact between these substrates and the slurry particles could range from the average contact area to more than the maximum estimated contact area. Figure 3 displays topographic AFM scans of each substrate.

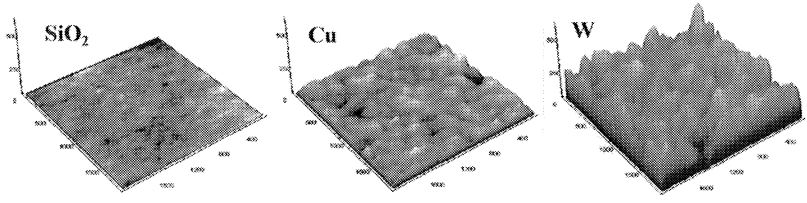

Figure 3: Topographic AFM scans of SiO_2, Cu, and W substrates following CMP.

Using these roughness and contact area measurements, our simulation was employed to predict the adhesion interaction between alumina slurry particles and each

substrate in air and water. Literature values for the Hamaker constants and Lennard-Jones equilibrium distances were used for each system (10-14). Simulation predictions are compared to predictions based on an ideal vdW model ($F= AR/6D^2$). Each prediction is an average of 10000 simulation predictions.

The simulation predicts a wide range of forces for the adhesion interaction. The simulation predicts a lower value than an ideal vdW model when the contact area is equal to the average contact area but a higher value than an ideal vdW model when the contact area extends up to the maximum contact area. Several factors could cause the contact area to extend to the maximum contact area including roughness and compression/deformation of the particle. During CMP, slurry particles are under large loads (> 5 psi). This could cause them to deform, compress, or embed into the substrate surface. This could extend the contact area between particle and substrate to the maximum contact area. Therefore, it is likely that there will be a much wider range of adhesive strengths than predicted by an ideal vdW model.

ACKNOWLEDGEMENTS

The authors are grateful to Speedfam-IPEC Corporation for both financial support and technical guidance on this project. The authors are also grateful to the Centers for Solid State Electronics Research and Solid State Science at ASU and to the NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing.

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CYCLIC VOLTAMMETRY OF PPB-LEVEL COPPER IN AQUEOUS POTASSIUM HYDROXIDE SOLUTION

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We have established a method for in-line monitoring of ppb-level copper (Cu) and lead (Pb) in strong potassium hydroxide (KOH) solution which is used for silicon (Si) etching. The method is cyclic voltammetry which employs stirring of solution, adsorptive stripping and high scan rate of potential. This method can serve as the direct monitoring of Cu and Pb in etching procedure, at the detection limit 0.5ppb. This in-line monitoring method reveals that Si surface etched with KOH solution becomes rough when the solution is contaminated by 300ppb Cu.

INTRODUCTION

Strong aqueous potassium hydroxide (KOH) solution is widely used for anisotropic etching in silicon (Si) micromachining [1]. It was recently demonstrated that etching characteristics such as rate and surface-smoothness were varied by ppb-level copper (Cu) and lead (Pb) in KOH solution [2,3]. Sequentially, in-line monitoring of ppb-level Cu and Pb in KOH solution is of great importance in the production of micromachined Si structures (e.g. beams for acceleration sensors) in compliance with the design.

However, the analyses of trace elements in strong alkaline solution are hampered by dilution and neutralization, while these treatments are necessary to

avoid contaminant dissolved from equipment. Dilution results in reducing the quantity of trace elements and having difficulty in detecting the elements. The conditions of neutralization are not well understood. Additionally, dilution and neutralization require sampling and make an in-line monitoring impossible. The goal of this study is to accomplish the in-line monitoring of ppb-level Cu and Pb in strong KOH solution.

EXPERIMENTAL

In an attempt to detect Cu and Pb in KOH solution, cyclic voltammetry was used and improvement of the detection limit was examined. All cyclic voltammograms were recorded with BAS 100B/W of Bioanalytical Systems. The working electrode was a glassy carbon disk of 3mm in diameter and the counter electrode was a platinum mesh. Potentials were measured with respect to a saturated calomel electrode (SCE) as reference.

The specimen was 32wt.% (13mol.%) aqueous KOH solution introduced Cu and Pb by dilution of atomic absorption standard reagents (CuNO3 and PbNO3). The KOH solution was contained in a polypropylene vessel which was tolerant to alkaline solution.

RESULTS AND DISCUSSION

In order to improve the detection limit of cyclic voltammetry, the following techniques were tested,

(1) stirring of sample solution by a PTFE rod,
(2) adsorptive stripping (15min. at –0.8V),
(3) high scan rate of potential (5V/s),
(4) neutralization of sample solution with hydrochloric acid.

Neutralization was also adopted to understand the detection limit of sampling inspection. Then, the conditions of neutralization were examined. Cyclic voltammograms were measured in the KOH solutions neutralized with hydrochloric, nitric, sulfuric and perchloric acid. It was found that hydrochloric acid did not cause precipitation in the wide range of pH (2~6) and enhanced the peak currents of Cu

and Pb. Accordingly, hydrochloric acid, which contained impurities less than 0.1ppb, was employed as a neutralization agent.

The cyclic voltammograms of Cu (50ppb) and Pb (50ppb) in 32wt.% KOH solution were shown in Fig.1. It was found that no signals were detected by the measurement without the techniques (1) stirring of the solution, (2) adsorptive stripping, (3) high scan rate of potential and (4) neutralization of solution. Cu and Pb became detectable by Method I which was the combination of the techniques (1), (2) and (3). The currents of Cu and Pb moreover increased by Method II which was introduced neutralization (technique (4)) to Method I .

Table 1 depicted the detection limits obtained in the present study. The detection limit (DL) was determined by the equation [1].

$$DL = 50ppb/ (\text{peak height at } 50ppb)*(\text{measurable peak height}) \quad [1]$$

Tab.1 Detection limits of cyclic voltammetry for Cu and Pb in the aqueous KOH solution.

Condition	Detection limit (ppb)
Cyclic voltammetry	1500
Neutralization + Cyclic voltammetry	500
Cyclic voltammetry +Combined techniques (Method I)	0.5
Neutralization + Method I (Method II)	0.1

Method I = stirring + adsorptive stripping + high scan rate

The results indicated that neutralization of the solution raised the detection limit. The detection limit of Method I (stirring of the solution + adsorptive stripping + high scan rate of potential) was evaluated to be about 0.5ppb and was improved to 0.1ppb with the neutralization treatment (Method II). These results display that Method I and II can serve as the in-line monitoring and the sampling inspection of ppb-level Cu and Pb in KOH solution, respectively.

Figure 2 displayed that surface roughing of Si was occurred in Si etching procedure with 32wt.% aqueous KOH solution. The Si surfaces etched with the KOH solutions (a) and (b) were smooth and rough, respectively. Using Method I, the in-line monitoring of Cu and Pb was performed and the concentrations were determined. The results were illustrated in Fig.3 and it was indicated that the solution (b) was contained 300ppb Cu. Consequently, the roughing was attributed to Cu contamination in the KOH solution.

CONCLUSION

We established the method for in-line monitoring of Cu and Pb in strong KOH solution, at the detection limit 0.5ppb. The method named Method I was cyclic voltammetry which employed stirring of solution, adsorptive stripping and high scan rate of potential. Using Method I, it was revealed that Si surface etched with KOH solution became rough when the etchant (KOH solution) was contaminated by 300ppb Cu.

When the neutralization treatment with hydrochloric acid was introduced to Method I, the achieved detection limit was evaluated to be 0.1ppb. This method can serve as the sampling inspection of ppb-level Cu and Pb in KOH solution.

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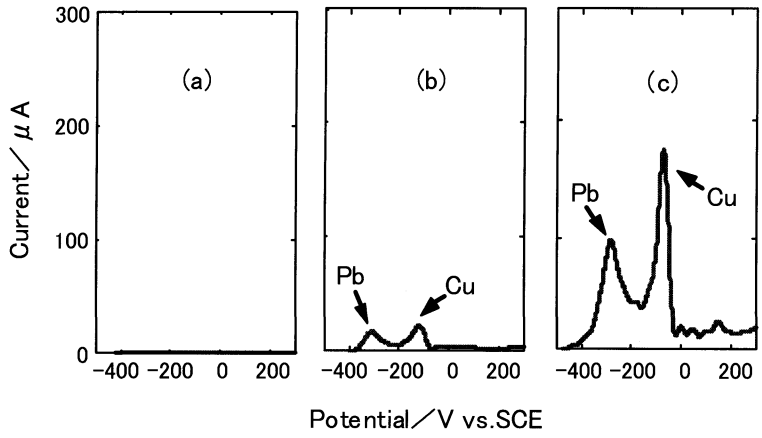

Fig. 1 Cyclic voltammograms of 50ppb Cu and Pb in 32wt.% KOH solution at carbon disk electrode, (a) potential scan rate was 0.5V/s, (b) Method I (stirring + adsorptive stripping + high scan rate (5V/s)), (c) Method II (neutralization + Method I).

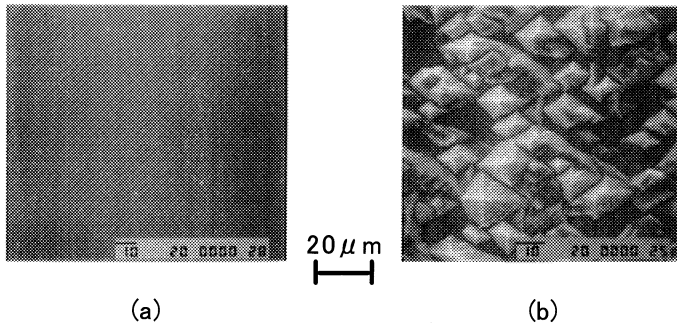

Fig. 2 Images of Si surface obtained with scanning electron microscopy. The surfaces of (a) and (b) were smooth and rough after etching with 32wt.% aqueous KOH solution.

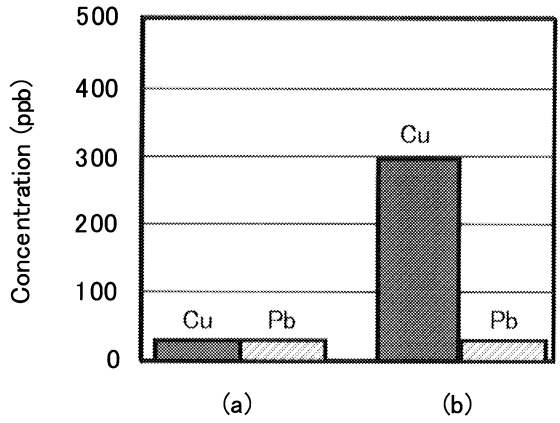

Fig.3 Cu and Pb concentrations determined directly in the etching procedure, using Method I. The Si surfaces etched with the KOH solutions (a) and (b) were smooth and rough, respectively.

SCANNER CALIBRATION FOR PARTICLE DETECTION AND WAFER CLEANING SYSTEM EVALUATION

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Wafer surface scanners are important tools for evaluating wafer-cleaning systems. Proper calibration of a scanner is important in order to have consistent measurement results. This paper describes the technical issues involved in the calibration of wafer surface scanners.

In this study, a MSP Model 2300 system has been used to deposit PSL spheres and process particles of Si, SiO_2, Si_3N_4, and W on wafer to study the response of a KLA-Tencor Surfscan SP1^{TBI} and for cleaning system evaluation. The MSP system makes use of a Differential Mobility Analyzer (DMA) to give a NIST (National Institute of Standards and Technology) traceable particle size to an accuracy of ± 2%. Results show that the particle material effect is significant not only in the scanner response but also in the measured efficiency of the wafer cleaning system.

INTRODUCTION

Particulate contamination of wafer surfaces is an important problem in semiconductor manufacturing. One study indicates that more than 80% of the product yield loss is due to particulate contamination [1]. Wafer surface scanners are widely used to detect particulate contaminant on wafer surfaces and to evaluate the performance of defect reduction tools. The surface scanner generally makes use of light scattering techniques to detect the presence of particles on the wafer surface. Figure 1 shows the optical design of the KLA-Tencor SP1^{TBI} scanner used in this study.

There have been considerable advances in wafer scanner technologies in recent years. A traditional scanner may utilize a single illuminating and light collecting system to detect particles on the wafer. A state-of-the-art wafer scanner such as KLA-Tencor SP1^{TBI} , however, has both a normal and oblique incident laser light source and two photo-detectors to collect scattered light over a narrow and a wide angular range. The system is capable of detecting particles to the 0.06 μm level that is required for the next generation, 0.18 μm device according to the SIA (Semiconductor Industry Association) roadmap [2].

The complexity of the state-of-the-art scanner makes it necessary to use software recipes to simplify system operation. However, software recipes at the same time make the system operation less obvious and transparent to the user. The job of data interpretation has become more difficult. A change in recipe often causes a large difference in the measured particle count and the lower detection limit of the instrument is also affected. It has become necessary to verify the system operation, including the effect of the software recipe on the response, by means of standard particles of an accurately known particle size and well-defined material properties. The traditional method of calibrating a wafer scanner by means of PSL calibrating spheres is no longer adequate for the modern scanner.

Polystyrene latex (PSL) spheres are traditionally used to calibrate wafer scanners because of their uniform size and spherical shape. PSL spheres of an accurately known particle size are available from the National Institute of Standards and Technology (NIST) in the form of Standard Reference Material (SRM) and they can be used as particle size standard for calibrating the scanner. When known sized spheres are deposited on the wafer and scanned, they produce the standardized light scattering signal to calibrate the scanner. A scanner calibrated with PSL will give a PSL-equivalent light scattering size. The measured size of a particle is then the size of a PSL sphere that scatters the same amount of light as the particle being detected. The measured size will generally differ from the geometrical size of the particle, the difference being dependent upon the particle material, its refractive index and shape, and the optical design of the measuring system [3]. This paper describes the method for generating and depositing PSL spheres and real-world process particles on wafer surfaces to calibrate the scanner and determine its response.

An important application of a wafer surface scanner is to measure the efficiency of wafer cleaning tools. The cleaning efficiency is usually measured by making a wafer surface particle count before cleaning, and then counting the particles again after the wafer has been cleaned. Since the adhesion or bonding force between a particle and the wafer is dependent on the size, shape, and chemical composition of the particles, the test results are usually very difficult to interpret when the contaminant particles used in the test are not well defined. Using particulate contaminants of well-defined characteristics will make the results more meaningful and easier to interpret.

In this paper, calibration and standardization of wafer surface scanners are described. Emphasis is on methods to create wafer particle standards and to demonstrate the effective use of such standards to evaluate scanner performance and the performance of wafer cleaning systems.

PARTICLE DEPOSITION SYSTEM

Calibration of a wafer surface scanner requires test wafers on which known material, size and number of particles are deposited. A commercial system (Model 2300 PSL/Process Particle Deposition System, MSP Corporation, Minneapolis, Minnesota) was used in the present study to prepare the test wafers. The system is capable of depositing PSL spheres in the 0.04 to 1.0 μm range and process particles, such as Si, SiO_2, Si_3N_4, W among others, in the 0.04 to 0.5 μm range on wafers up to 300 mm in diameter.

Figure 2 is a schematic diagram of the MSP system. In the system, PSL spheres or process particles to be deposited are first dispersed in deionized water and atomized to form an aerosol. The aerosol is then passed though the differential mobility analyzer (DMA) for size classification and determination. The output aerosol from the DMA is then deposited on the wafer by enhanced electrostatic deposition.

The DMA method used in the Model 2300 is the same method used by NIST to measure the size of its reference PSL spheres [4]. If reference PSL spheres from NIST are used to standardize the DMA in the Model 2300, the system can then be used as a transfer standard to determine the NIST traceable particle size of the commercial PSL spheres. Three particle size standards are currently available from NIST. These are referred to as Standard Reference Materials (SRM). The sizes available are 0.1007±0.0020 μm, 0.269±0.007 μm, and 0.895±0.008 μm. The Model 2300 is calibrated by MSP in the factory using SRM # 1963 from NIST with a certified size of 0.1007 μm.

Since process particles of interest are generally not available as uniform dispersions, the polydisperse particles can be suspended in liquid and atomized in the usual manner to form a polydisperse aerosol. This polydisperse aerosol can then be introduced into the DMA for size classification. The output aerosol from the DMA then consists of monodisperse particles of a well-defined electrical mobility, hence, particle size. These particles can then be deposited on a wafer for scanner calibration, cleaning efficiency measurement, and other applications where real-world process particles, rather than ideal PSL spheres, are needed.

In the Model 2300, particles are deposited on the wafer in a deposition chamber by enhanced electrostatic deposition. Particles can be deposited uniformly over the entire wafer surface or in several concentrated spots of a few centimeters in diameter. Enhanced electrostatic particle deposition has made it possible to deposit all particles entering the deposition chamber. This in turn has made it practical to count the airborne particles prior to deposition and determine the total number of particles deposited on the wafer.

An example of multiple spot deposition on a wafer is shown in Figure 3. PSL spheres of 16 different sizes have been deposited on a 300-mm bare silicon wafer. The PSL size ranges from 0.079 μm to 0.890 μm. The deposition spot diameter is seen to increase with increasing particle diameter because of the decreased electrical mobility of the large particles. By controlling the magnitude of the electric field inside the chamber, the spot diameter on the wafer can be controlled.

The spot deposition is particularly advantageous for scanner calibration and cleaning system evaluation. Several spots of uniform PSL spheres or process particles of several different sizes can be deposited on the same wafer to obtain information for several particle sizes in a single test. When such a wafer is used, it can greatly reduce the cost of the wafer and the labor involved in scanner calibration. The cost saving in wafer alone is substantial in the case of 300-mm wafers or patterned wafers, both of which are expensive. For wafer cleaning system studies, wafers carrying uniform spots of process particles of several different sizes on each are most useful. After cleaning, particles remaining in each spot can be scanned to determine the cleaning efficiency for each particle size. Since all spots are cleaned under identical conditions on a single wafer, exceptionally consistent results can be obtained with this approach. Migration of particles from each spot to different parts of the wafer can also be easily seen in the wafer map.

WAFER SCANNER CALIBRATION

A calibration of the KLA-Tencor Surfscan SP1^{TBI} was made using the test wafer created with the Model 2300. The SP1^{TBI} scanner is operated by light scattering principles and designed for inspecting un-patterned wafers. The acronym TBI stands for triple beam illumination. Two beams used for dark field inspection for normal and oblique incidence and the third beam in bright field inspection. During each scan, the wafer spins and translates so that the spiral inspection is carried out. The system uses two photo detectors. One covers a wide angular range and the other a much narrow range of angles. They are referred to as the "dark field wide" and the "dark field narrow" detectors respectively. The two detectors measure the surface defects independently and the two measurements are combined to produce a composite map [5].

Wafer particle standard prepared with 20 different size PSL spheres are used and the calibration curves are shown in Figure 4 for both normal and oblique recipes. For the case of normal recipe, the indicated diameter by the Surfscan SP1^{TBI} matches reasonably well with the PSL size calibration up to 0.423 μm. Above this size, the indicated diameter does not agree with the actual value of the PSL sphere size used. It is believed that the difference is caused by the phenomenon of Mie resonance, where the scattered light intensity can actually decrease with increasing particle size in certain particle size range for the specific wavelength of the laser used [6]. For oblique recipe, the resonance takes place when PSL spheres larger than 0.653 μm are measured.

In addition to calibration by PSL, the response of the SP1^{TBI} is also determined with process particles deposited on the wafer. Since the process particles have different indices of refraction than the PSL, the response curves are expected to be different from that for PSL shown in Figure 5. Process particles of Si, SiO_2, Si_3N_4, and W have been deposited on the wafer. For each particle material, several different sizes were used on a single bare silicon wafer.

Figure 5 shows the particle map of tungsten particles of 4 different sizes - 0.064, 0.087, 0.107, 0.202 μm –deposited on a 200-mm bare silicon wafer. The monodisperse tungsten particles produced by the DMA are quite narrow in size distribution – the standard deviation of particle size is approximately 4% of the mean particle size as measured by their mobility. Previous research on monodisperse particle generation by the DMA [7] shows that the DMA mobility size of irregular particles is very close (about 4%) to their geometrical size measured by the scanning electron microscope. The size distribution of the tungsten particles indicated by the scanner, however, are broader due to the irregular shape of the particle and their random orientation on the wafer surface.

The process particle response curves for Surfscan SP1^{TBI} are shown in Figure 6 and 7 for normal and oblique recipes respectively. The curves for process particles are shifted from the PSL curve but, generally, the indicated diameter increases with the increasing particle diameter. The different response characteristics of the PSL sphere and process particles are believed to be the result of the different refractive index of the particle material. Table 1 shows the index of refraction of some of the materials of interest in scanner calibration and performance evaluation [8].

The refractive index of the calibrating PSL sphere is 1.59 and the material is non-absorbing. Refractive indices of SiO_2 and Si_3N_4 are 1.46 and 2.02 respectively. Both particles are also non-absorbing. For tungsten (W), the particle is moderately absorbing, and the real part of the refractive index is 2.76. Because the real part of the refractive

index of these materials is not greatly different, the ability of these particles to scatter light is also quite similar near the lower limit of detection of the SP1[TBI]. The data in Figure 6 and Figure 7 shows that at the smallest particle size used in these tests, Si_3N_4 and W have the larger indicated particle size than PSL, while SiO_2 shows the smaller indicated size than PSL. This is because the refractive index of Si_3N_4 and W is larger than PSL but SiO_2 particles have smaller refractive index than PSL. In contrast, the case for Si is quite different. Since the Si particles are deposited on bare silicon wafer, indicated size of Si particle is smaller than PSL even though its refractive index is much higher than PSL. This result appears to be an anomaly. It needs to be further studied before it can be confirmed.

CLEANING SYSTEM EVALUATION

Wafer surface cleaning or conditioning is an important process in semiconductor manufacturing. Since the particulate defect is the major source of yield loss, wafer cleaning is the most repeated single process in semiconductor manufacturing. In cleaning system evaluation, the real-world process particles should be used because the adhesion or bonding force between a particle and the wafer substrate is highly dependent on particle material. Using appropriate process particles, each cleaning step, a specific recipe, or the entire cleaning process can be evaluated and fine tuned to achieve optimal performance in terms of increased cleaning efficiency and reduced cleaning time.

In the previous studies, process particles of polydisperse size distribution are used as the artificial contaminant by dipping a wafer into DI water containing the dispersed particles [9]. The dipping method may produce realistic results for particulate contamination through the wet deposition process. However it is not realistic when contaminant particles are deposited in a dry process such as vacuum-based chemical vapor deposition or etching process. Using wafers contaminated by dipping may lead to the erroneous conclusion that a specific cleaning tool is inadequate, even though it may, in actuality, be a better and more efficient method for the specific cleaning step being evaluated. The dry-deposition methodology employed by the Model 2300 deposition tool used in this study simulates more realistically the deposition of particles in dry processing tools.

In this study, several monodisperse spots of particles were deposited on each wafer using the Model 2300. Since the size of particles in each spot is known from the Model 2300 deposition tool, the scanner was used only to count particles in each spot before and after cleaning to determine the removal efficiency. Sizing errors due to measurement anomalies of the scanner and particle refractive index are thus eliminated.

Chemical cleaning is one of the most common wafer cleaning methods used in the semiconductor industry. It usually has several steps of cleaning using different chemicals mixture to remove organic, particulate and metallic contaminants. Between the steps, a hot DI water rinse and drying process is used to remove the residual chemicals and improve the performance of drying [10]. Since rinse/dry is a basic step in chemical cleaning, it is studied here as a way to develop methodology for cleaning system evaluation. For this study, process particles as well as PSL spheres were deposited on 200 mm bare silicon wafer using the Model 2300 tool. The test wafers were then cleaned by a simple rinse/dry step involving hot DI water rinse followed by spin drying with dry nitrogen purge.

Figure 8 shows the rinse/dry cleaning results. The particle sizes used are 0.157 μm and 0.202 μm. Particle material used includes Si, SiO_2, W, Cu and PSL. The greatest rinse/dry efficiency is achieved for W, followed by Cu and PSL, and the lowest efficiency is achieved for Si and SiO_2, all carried out under identical cleaning conditions. The result suggests that W, Cu and PSL particles are attached to the wafer by pure physical adhesion, while Si and SiO_2 particles are more likely to have developed chemical bonds with the Si substrate. The strong chemical bonds for Si and SiO_2 make these particles more difficult to detach during the rinse/dry step.

SUMMARY

A KLA-Tencor Surfscan SP1^{TBI} scanner was calibrated with test wafers specially prepared by the MSP Model 2300 PSL/Process Particle Deposition System. The calibration was made using PSL spheres of an NIST traceable size and process particle such as Si, SiO_2, Si_3N_4, and W. The effect of refractive index on the wafer scanner is studied. The test wafer prepared with particles of a known chemical composition and size using the Model 2300 makes it possible to simulate real particulate contamination process occurring in dry processing tools. It also allows the fine-tuning of wafer cleaning tools. This effort of fine tuning of wafer scanner and cleaning tool performance will be critical in the next generation fabs in achieving consistency of measurement and improved product yield.

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TABLE 1. Refractive Index of Particles

Material	Refractive Index
Polystyrene latex (PSL)	1.59 - i0.00
Silica (SiO_2)	1.46 - i0.00
Silicon (Si)	3.88 - i0.02
Silicon nitride (Si_3N_4)	1.10 – i2.13
Tungsten (W) (λ=579nm)	2.76 – i0.98

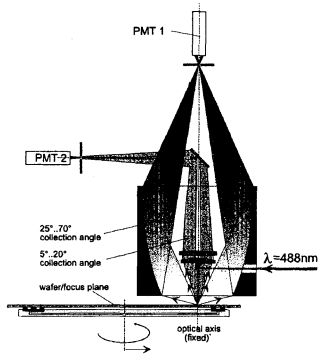

Figure 1 Optical Geometry of the KLA-Tencor SP1

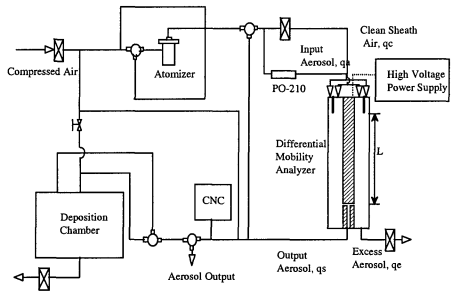

Figure 2 Schematics of MSP Model 2300 PSL/Process Particle Deposition System

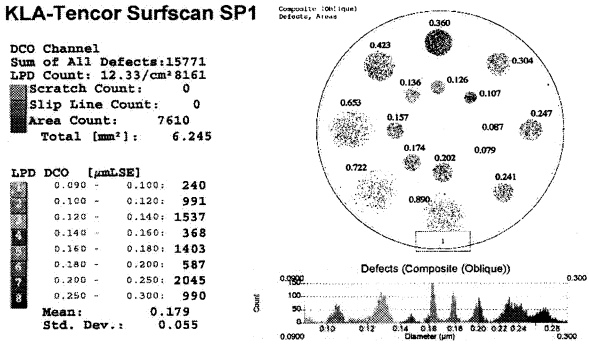

Figure 3 The Scanner Measurement for PSL Spheres

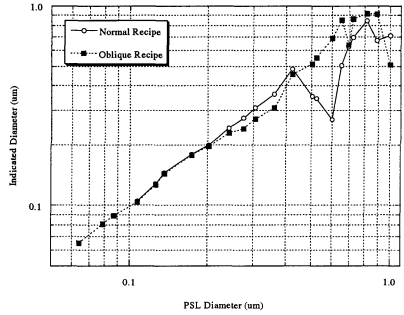

Figure 4 Calibration Curves of SP1 for PSL Spheres

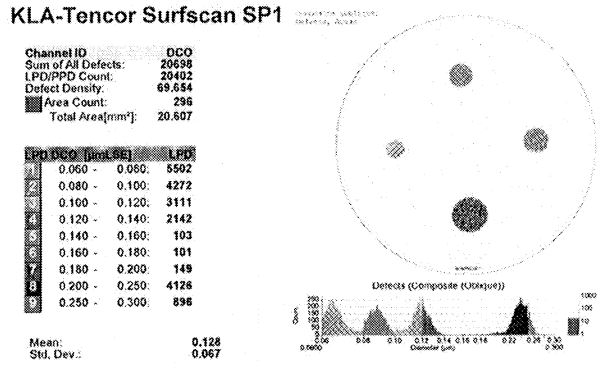

Figure 5 The Scanner Measurement for W Particles

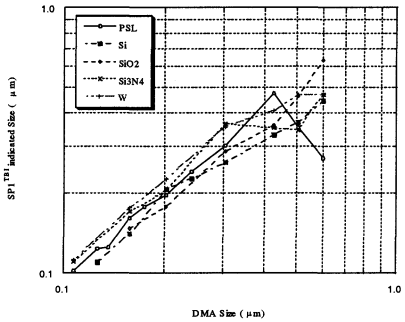

Figure 6 Calibration Curves of SP1 for PSL and Process Particles (Normal Recipe)

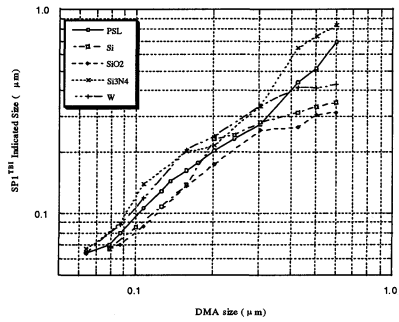

Figure 7 Calibration Curves of SP1 for PSL and Process Particles (Oblique Recipe)

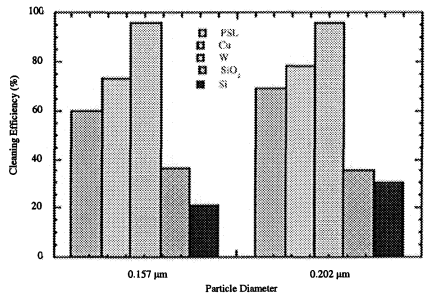

Figure 8 Cleaning Efficiency of PSL and Process Particles by Rinse Dry Process

INFRARED MONITORING SYSTEM FOR WET CLEANING ON 300 MM SILICON WAFERS

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ABSTRACT

We have developed a new monitoring system for surface characterization of a 300-mm Si wafer, which is based on infrared multiple internal reflection spectroscopy. This system is able to monitor surface chemical conditions on commercially available 300-mm wafers without additional cutting and polishing. This monitoring system has a high sensitivity for the detection of absorbed molecules on wafer surfaces, and has a short inspection time. The experimental result clearly shows this system has real-time monitoring capabilities and is suitable for in-line monitoring on the wafer cleaning process.

INTRODUCTION

Cleaning a Si wafer surface is one of the important fabrication processes in order to achieve a high yield production of semiconductor devices. It is necessary to evaluate contamination, hydrogen termination and water on the wafer after the cleaning process. However, appropriate tools are not available to analyze chemical conditions in high sensitivity on the wafer surfaces in short inspection time.

Infrared multiple internal reflection spectroscopy (IR-MIRS) is a powerful tool for analyzing the chemical state of a semiconductor surface (1). This method, however, has the following disadvantage; it is applicable only to a small sample piece of a Si wafer that is polished on the front and back surfaces. This method, therefore, has not been utilized for characterizing commercially available Si wafers which have only a polished front side.

We have developed a new wafer surface monitoring system for a 300-mm wafer,

which is based on IR-MIRS. Recently, SEMI (Semiconductor Equipment and Materials International) has been defined as the international standard for the next generation of 300-mm wafer (2). This standard states that the back surface gross for the 300-mm wafer must have >80% of the front surface gross. This implies that IR-MIRS can be applied to the surface characterization of the commercially available 300-mm wafers without additional cutting and polishing for the analysis. IR-MIRS is non-destructive and non-contact measurement. It is highly sensitive to sticking molecules on the wafer surface. The detection limit of the monitoring system has been estimated as 10^{11} carbon atoms/cm^2, from absorbance in the C-H stretching vibration region of dioctyl phthalate (DOP) (3). This monitoring system also has rapid inspection speed. This means that real-time monitoring of chemical conditions on wafer surfaces is practicable on the device production line after the wet cleaning process.

IR MONITORING SYSTEM

Figure 1 shows the experimental setup of a surface monitoring system that we have developed. This system consists of an IR source (Globar lamp), focusing mirrors, a wafer stage, an IR spectrometer (BOMEN MB-100 FT-IR), and a LN_2 cooled InSb IR detector (3).

An IR light that exits from the IR source is focused onto an edge of the wafer and the IR light propagates through the wafer by internal reflection between both surfaces. An IR evanescent wave is emerged on the wafer surfaces when the total reflection occurs at the silicon-air interface. The absorbed molecule on the wafer is identified from the wavelength of IR absorption which is caused by the sticking molecules on the surface.

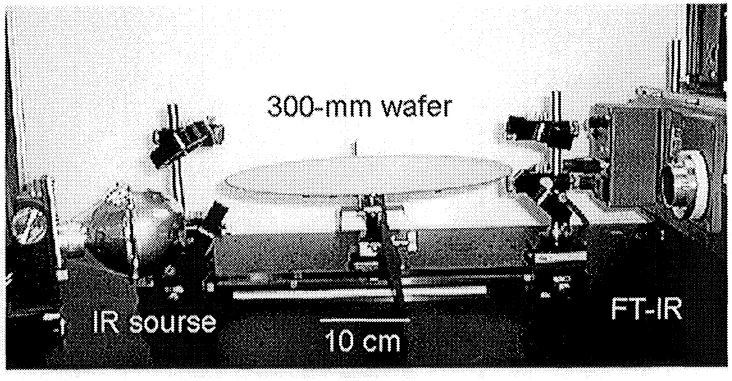

Fig.1. The surface monitoring system for the 300-mm wafer.

We select the incident angle of the IR light onto the edge at about 30°. This angle satisfies that the internal reflection angle is greater than 17°, the critical angle of total reflection at the silicon-air interface. The number of internal reflections reaches to about six hundred, which makes it possible to detect very small amounts of contamination on the silicon wafer surface (4).

The inspection speed of this system depends mainly on the noise level of the IR detector and the data acquisition speed of the IR interferometer. The data acquisition interval time of the interferometer we used is less than 1 second/scan. This means that this system is usable as a real-time monitoring system for a rapid change of surface chemical conditions.

This system is also able to detect very small amounts of the molecules which stuck on the wafer surface in a short inspection time. Our previous results show that this system can detect a 10^{11} carbon atoms/cm^2 density of organic contamination on the 300-mm wafer within 2 minutes, at an average of 200 scans of the FT-IR interferometer (3)(4). This inspection time is much shorter than the other surface analysis tool for the silicon wafer, such as the TDS-GC/MS system that has almost the same sensitivity for hydrocarbon contamination.

EXPERIMENTAL

In order to demonstrate the efficiency of this monitoring system, we carried out several chemical treatments onto 300-mm wafers and then monitored chemical conditions on the surface. These chemical treatments are Isopropyl alcohol (IPA) treatment, DHF (dilute hydrofluoric acids) treatment, and UV/O_3 (ultraviolet/ozone) treatment, commonly used in the wet cleaning process on the fabrication line of the semiconductor device (5).

The 300-mm wafer surface was cleaned up by acetone and was followed by UV/O_3 cleaning (Hg lamp: λ=184.9 nm and 253.7 nm, 20 mW/cm^2 at working distance 10 mm) during 1 hour before each treatment. In the measurement of the IPA treatment, 2 ml of IPA dropped on the wafer which was spin rotating at 200 rpm. The data acquisition of the FT-IR interferometer was set at an interval of 0.5-seconds in order to monitor vaporization process of IPA. The resolution of the FT-IR interferometer was set at 16 cm^{-1}. In the case of the DHF treatment, the wafer was treated by dipping in 1 % HF solution and then dipping pure water to make a hydrophobic surface. The immersion time was 5 minutes for both treatments. The IR spectrum measurement was carried out by averaging 200 scans of spectra at a resolution of 16 cm^{-1}. The duration required for collecting the spectrum was only 2 minutes. In the case of UV/O_3 treatment, the DHF treated wafer irradiated by the UV light for 30-seconds and then the surface was analyzed. The FT-IR interferometer operated under the same conditions as the measurement of DHF treated surfaces. This procedure was repeated until the total UV/O_3 irradiation time reached to 5 minutes.

RESULTS AND DISCUSSION

Surface Monitoring on the 300-mm Wafer after the IPA Treatment

IPA is used in the IPA vapor drying process after the ultra pure water treatment in order to remove water droplets on the wafer. It has been reported that IPA still remained

on the wafer surface after the IPA vapor drying process and that the residual IPA molecules affect gate-oxide reliability (6). The residual IPA is able to observe by using our monitoring system because this system is highly sensitive to sticking molecules on the wafer surface.

Figure 2 shows the C-H and the O-H stretching vibration region of IPA vaporization on a UV/O_3 treated wafer. This figure illustrates the absorption peak intensity of the O-H stretching vibration and the C-H stretching vibration decrease with the time due to vaporization of IPA. This result clearly demonstrates that our monitoring system has real-time monitoring capability. The O-H absorption peak disappeared within 1 minute from the IPA was dropped on the surface, but the C-H absorption peak still remained. This monitoring system is sufficiently sensitive for the detection of very small amounts of residual IPA on the wafer surface.

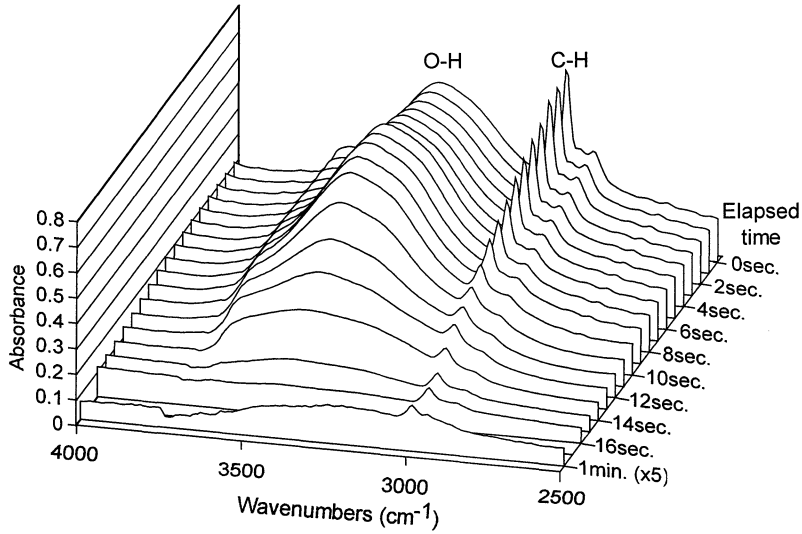

Fig.2. Time dependent profile of the C-H & the O-H absorption at IPA vaporization on UV/O_3 cleaned wafer.

Figure 3 shows the time dependence of the peak intensity of the C-H and the O-H stretching vibration region during IPA vaporization. The C-H peak intensity linearly decreased with the time. On the other hand, the O-H peak intensity has a maximum at 8 seconds and then decreases. This result suggests that additional molecules, which have the O-H structure stick on the wafer surface during IPA vaporization.

Figure 4 shows the movement of the O-H stretching vibration absorption peak during IPA vaporization. In spite of the peak position of the C-H stretching vibration is the same during IPA vaporization, the peak position of the O-H absorption shifts to higher wave numbers with vaporization of IPA. The additional absorbed molecules must have been H_2O contained in the air. It may condense on the wafer because IPA vaporization decreases wafer temperature. The peak position of the O-H stretching vibration in pure IPA is 3350 cm^{-1} and the O-H stretching vibration in H_2O on the wafer is

around 3400 cm^{-1}. At the initial state of IPA vaporization, the peak position of the O-H stretching vibration is almost the same value as pure IPA. When the intensity of the O-H stretching vibration begin to decrease, the peak position of the O-H stretching vibration shifts and approach the O-H peak position of H_2O. This suggests that absorbed molecules on the wafer surface change from the IPA to the C-H fragment of IPA + H_2O. These rapid surface changes can be clearly observed by using this monitoring system.

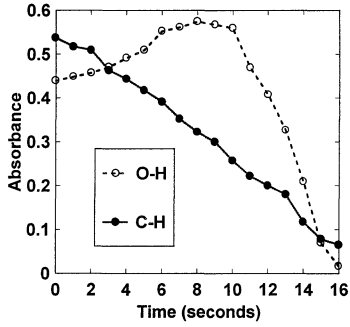

Fig.3. Time dependence of the absorption peak intensity of IPA.

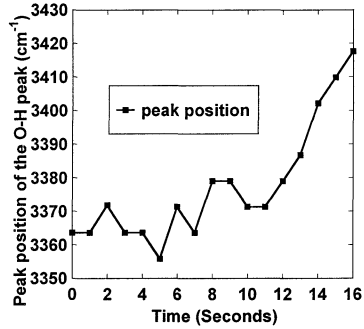

Fig.4. Movement of the O-H absorption peak position at IPA vaporization

Surface Monitoring on the 300-mm Wafer after the DHF Treatment

It is well known that treatment in dilute HF solution produces a Si surface terminated by hydrogen. Figure 5 shows the IR absorption spectra for the 300-mm wafer surface, which was treated with 1 % HF solution.

The upper portion of Figure 5 shows the spectrum collected just after DHF treatment. An intense absorption band due to O-H stretching vibration was observed, suggesting that H_2O still remained on the wafer surface, probably in the form of mist. The lower spectrum of Figure 5 shows that after 5-min storage in room air the O-H stretching vibration peak completely disappeared. This indicates that the water evaporated. On the

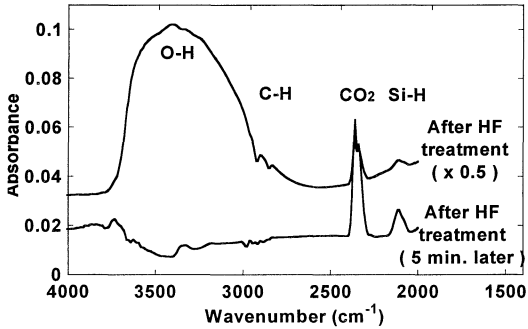

Fig.5. Spectra for 300-mm wafer surface after DHF treatment.

other hand, a peak at 2100 cm^{-1}, which is due to Si hydrides, is clearly observed, which indicates that hydrogen termination remains intact for 5-min storage in room air.

Surface Monitoring on the 300-mm Wafer after the UV/O_3 Treatment

The UV/O_3 treatment is applied to decompose organic contamination and improve hydrophilicity on the wafer surface. It is quite easy to evaluate the result of the UV/O_3 treatment by using our monitoring system.

Figure 6 shows a surface chemical condition change which occurred during UV/O_3 treatment on the DHF treated 300-mm wafer. The absorbance spectrum before UV/O_3 treatment (0 seconds) shows an intense absorption of O-H stretching vibration around 3400 cm^{-1}. This downward peak comes from H_2O absorption in the spectrum of the UV/O_3 treated wafer, which was used as the background reference spectrum of the absorbance spectrum. The UV/O_3 treated Si surface shows hydrophilicity and H_2O molecules contained in the air are easier to absorb than the DHF treated hydrophobic Si surface. This downward peak shows that the UV/O_3 treated wafer absorbs more H_2O on the surface than the DHF treated surface.

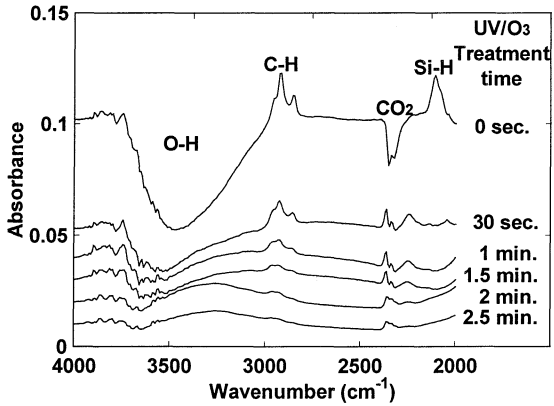

Fig.6 UV/O_3 treatment on DHF treated wafer.

Though the intensity of the O-H stretching vibration peak decreases with the UV/O_3 treatment time, it means that H_2O is sticking on the wafer surface during UV/O_3 treatment. As was mentioned above, the DHF treated wafer absorbs less H_2O on the surface than UV/O_3 treated wafer. As the result of UV/O_3 treatment, the DHF treated surface change from hydrophobic to hydrophilic and H_2O begin to stick on the wafer surface. As the UV/O_3 treatment time increases, the amount of the water on the surface increases to the same as the reference UV/O_3 treated surface and the intensity of the O-H stretching vibration peak decreases.

This absorbance spectrum also shows the Si-H absorption produced by the DHF

treatment and the C-H stretching vibration due to contamination from a chemical bath. Hydrogen termination on the wafer surface decomposed completely after 30 seconds of UV/O_3 treatment. On the other hand, the intensity of C-H stretching vibration decreased with the UV/O_3 treatment time, but it was observed after 2.5 minutes of UV/O_3 treatment. Because the C-H bond has higher bond dissociation energy than the Si-H bond, the Si-H bonds on the wafer surface decomposed easier than the C-H bonds.

This result clearly shows our monitoring system is quite useful in order to determine the end-point of the surface treatment. In this case, it is enough to destroy hydrogen termination on the wafer surface with UV/O_3 treatment for 30-seconds, but longer treatment time is needed to remove organic contamination on the wafer surface.

CONCLUSION

We have developed a new monitoring system for the characterization of a 300-mm Si wafer. The system is based on the IR-MIRS method. It has important advantages; (1) highly sensitive for the surface, (2) rapid, (3) non-destructive. The result shows this system is superior in relation to the observation of water, organic contamination and hydrogen termination on the Si wafer. It is also capable of the real-time observation for rapid change of the surface chemical condition. This monitoring system gives us useful information on the Si wafer surface in short inspection time and high sensitivity. The present experimental result shows that the system is quite suitable for the in-line monitoring of cleaning process in the fabrication of Si devices.

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COMPETITIVE ADSORPTION OF CATIONS ONTO THE SILICON SURFACE: THE ROLE OF THE AMMONIUM ION IN AMMONIA-PEROXIDE SOLUTION

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Study of metal ion adsorption in aqueous solutions using a spin-contamination method has shown that NH_4^+ can effectively prevent Ca^{2+} adsorption onto the hydrophilic, oxidized silicon surface. In ammonia-hydrogen peroxide-water solution (APM), the relatively low Ca^{2+} adsorption on the wet oxidized silicon surface can be explained by its competition for adsorption sites with NH_4^+, which is the dominant cation in APM. NH_4^+ prevents Ca^{2+} adsorption onto the oxidized silicon surface, by an ion-exchange mechanism. NH_4^+ is at least as effective as H^+ in removing metals from the oxidized silicon surface and in keeping metal ions off the surface.

INTRODUCTION

The ammonia-hydrogen peroxide-water solution (APM) and hydrochloric acid-hydrogen peroxide-water (HPM) recipes, originally parts of the RCA cleaning procedure,[1,2] are both used for aspects of silicon wafer surface cleaning. Metal contamination and cleaning due to APM and HPM have been studied for many years.[3] Recently, Mouche *et al.*[4] have measured contamination of the silicon surface by metals in APM, finding surface contamination in decreasing order by Al > Fe > Ca, Cu. Mori *et al.*[5] found contamination in APM decreasing as Fe > Zn > Ni. Mertens *et al.*[6] have found Al and Fe contamination relatively independent of $[NH_3]$, while Ni and Zn surface contamination were inversely proportional to $[NH_3]$ in APM. Complexation by NH_3 has been proposed as the mechanism for Ni and Zn removal,[5,6] and for Ca.[4,7]. Ni^{2+} and Zn^{2+} form ammine complexes, but Ca^{2+} and Mg^{2+} do not appear to form them according to a thermodynamics data compilation.[8] Since Ca is a known contaminant appearing on wafers in semiconductor manufacturing, and can degrade electrical performance along with other alkaline earth elements,[9,10] it is worthwhile to improve our understanding of contamination and removal of Ca and other alkaline earth elements in the context of APM exposure.

We have previously developed a model describing the competition of metal ions and hydrogen ions for adsorption sites on the oxidized silicon surface.[11,12] This surface, which oxidizes slightly in both air and water, forming a hydrophilic oxide layer, has charged oxide groups ($\equiv$Si-O^-), which act as adsorption sites.[13] The adsorption site density of the oxide surface controls the number of metal ions that can adsorb to the silicon surface by ionic attachment. When H^+ attaches to a $\equiv$Si-O^- group on the surface, an OH group is formed. When a metal ion, M^{n+}, attaches to the O^- group, the surface group becomes $OM^{(n-1)+}$:

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$$\equiv Si-O^{-}(s)+M_i^{+}(aq) \rightarrow \equiv Si-O-M_i(s) \qquad [1]$$

In HPM solution, high $[H^+]$ favors protonation of the surface, forcing off metals.[11,12] In basic solution, there needs to be another cation present besides H^+ to maintain charge neutrality. In 1:1:5 APM, the dominant cation is NH_4^+ with $[NH_4^+] \cong 7.9\text{x}10^{-2}$ mol/L. The strength of NH_4^+ adsorption to the silicon oxide surface is likely smaller than that of metal ions, since the charge of NH_4^+ is low and its radius relatively large in comparison to those ions.[14] The relatively high concentration of NH_4^+in solution can make up for its weaker attraction to the surface.

In this work we demonstrate the effect of NH_4^+ in preventing Ca^{2+} adsorption on the hydrophilic, oxidized silicon surface from aqueous solution. We measure the magnitude of the ammonium ion's attraction to the oxidized silicon surface. We show how NH_4^+ affects Ca^{2+} adsorption from APM onto the oxidized silicon surface.

MODEL

We first develop the chemical concepts related to metal ion adsorption from APM onto the silicon oxide surface. Metal adsorption has previously been described for acidic solutions,[11,12] so here we concentrate on the role of the base and its conjugate acid – here, NH_3 and NH_4^+ – present in APM. We consider Ca^{2+} as a representative metal cation. For this treatment, the chief requirement of the metal is that it exists as a cation in aqueous solution at the pH and chemical environment of interest.

Cation Adsorption on the Oxidized Silicon Surface

We posit that NH_4^+, H^+, and metal ions, M^+–indeed, all the cations in aqueous solution–compete with each other for places to adsorb on the oxidized silicon surface. Following Langmuir's model for gas adsorption onto a surface with a limited number of attachment sites, as adapted for the silicon oxide surface,[11,15] we find that

$$\sigma_i = \frac{\sigma_0 K_i [M_i^+]}{1+\sum_i K_i [M_i^+]} \qquad [2]$$

where σ_0 is the areal density of adsorption sites, σ_i is the areal density of adsorbed metal, M_i, $[M_i^+]$ is M_i^+'s solution concentration. K_i is an equilibrium constant for the attachment of M_i to the surface according to Equation [1].[11]

For a system with H^+, NH_4^+, and Ca^{2+}, the surface concentration of Ca^{2+} is given by

$$\sigma_{Ca} = \frac{\sigma_0 K_{Ca} [Ca^{2+}]}{1+K_H [H^+]+K_{NH_4} [NH_4^+]+K_{Ca} [Ca^{2+}]} \qquad [3]$$

In APM, we find

$$\frac{1}{\sigma_{Ca}} \approx \frac{1}{\sigma_0} + \frac{1+K_{NH_4}[NH_4^+]}{\sigma_0 K_{Ca}[Ca^{2+}]} \qquad [4]$$

EXPERIMENTAL

Two separate experiments are described. The first delineates the role of NH_4^+ in preventing metal ion adsorption from aqueous solution. The second demonstrates the low metal adsorption of metal ions from APM, which we will interpret in terms of competitive adsorption in the presence of NH_4^+.

Common to both experiments was the controlled contamination technique in which wafers were exposed to prepared solutions containing metal ions. The 150-mm diameter Si(100) wafers received a pre-clean using the IMEC clean ™ (H_2SO_4/O_3, followed by dilute HF/HCl, ending with hydrophilic Si surfaces from an $HCl-O_3$ step).[16] Ca^{2+} came from solid $Ca(NO_3)_2 \cdot 4H_2O$. After exposure to the treating solution for 10 min at room temperature, about 20 °C, we spun the wafers for 30 sec on a high-speed wafer spinner to rapidly remove the solution from the wafer surface and dry the wafers.[11] No other rinse or drying procedure was used. We measured contaminant surface concentrations by total reflection x-ray fluorescence (TXRF) with the Atomika Model XSA 8010 spectrometer, first pre-concentrating the metals using vapor-phase decomposition/droplet collection (VPD/DC) using the GeMeTec PAD-Scan, and then drying the droplets with a heat lamp.

Effect of NH_4^+ on Ca^{2+} Adsorption from Aqueous Solution

The effect of NH_4^+ on Ca^{2+} adsorption was explored using a g-optimal quadratic design. There were 11 distinct trial conditions, with $3x10^{-5}<[NH_4^+]<1x10^{-2}$ mol/L, and $2x10^{-7}<[Ca^{2+}]<2x10^{-6}$ mol/L. Three to four replicates were performed for each design point, and two replicates for each checkpoint. We used NH_4Cl from Merck.

Ca^{2+} Adsorption from APM and Acid Solution

In this work, we compared Ca^{2+} adsorption onto an oxidized silicon surface, produced by an $HCl-O_3$ rinse at the end of an IMEC clean ™, from intentionally contaminated APM to Ca^{2+} adsorption from nitric acid solution at pH 3, 4.5 and 5.7. APM was prepared as 1:1:5 by volume mixing ratio ($NH_3:H_2O_2:H_2O$). In trials under acid conditions, HNO_3 was used. Solutions were prepared and used at room temperature, about 20 °C.

RESULTS AND DISCUSSION

We analyze here the results of our experiments that study the effect of NH_4^+ on Ca^{2+} adsorption and those that examine Ca^{2+} adsorption from APM and from HNO_3 solution.

Effect of NH_4^+ on Ca^{2+} adsorption

Figure 1 contains a contour plot of Ca concentration on the wet oxidized silicon surface. $1/\sigma_{Ca}$ correlates positively with both $[NH_4^+]$ and $1/[Ca^{2+}]$. That is to say, σ_{Ca} decreases as $[NH_4^+]$ increases, and as $[Ca^{2+}]$ decreases. Moreover, the curvature in Figure 1 indicates that surface concentration decreases as the ratio, $[NH_4^+]/[Ca^{2+}]$, increases. This behavior follows from Equation [4], which we can rearrange to give

$$\frac{1}{\sigma_{Ca}} = \frac{1}{\sigma_0} + \frac{1}{\sigma_0 K_{Ca}[Ca^{2+}]} + \frac{K_{NH_4}[NH_4^+]}{\sigma_0 K_{Ca}[Ca^{2+}]} \qquad [5]$$

A full quadratic fit to the data is of the form

$$\frac{1}{\sigma_{Ca}} = C_0' + C_1'[NH_4^+] + \frac{C_2'}{[Ca^{2+}]} + C_3'[NH_4^+]^2 + C_4'\frac{1}{[Ca^{2+}]^2} + C_5'\frac{[NH_4^+]}{[Ca^{2+}]} \quad [6]$$

We need only three terms to describe most of the observed behavior:

$$\frac{1}{\sigma_{Ca}} = C_0 + \frac{C_1}{[Ca^{2+}]} + C_2\frac{[NH_4^+]}{[Ca^{2+}]} \quad [7]$$

The full quadratic model of Equation [6] has only slightly better regression statistics than does the three-term model of Equation [7]. Coefficients from our empirical model are presented in Table I, and a contour plot is shown in Figure 1.

The coefficients of Equation [7] can be related to physical constants. C_0 corresponds to $1/\sigma_0$. We thus obtain a value of $(2.2\pm0.94)\times10^{11}$ cm^{-2} for σ_0. Since the coefficient of $1/[Ca^{2+}]$ is statistically indistinguishable from zero, we cannot properly interpret it as the equilibrium constant, K_{Ca}. The ratio of the interaction term to the constant gives a measure of the ratio K_{NH4}/K_{Ca}, 4.5×10^{-4}. As other results of ours indicate that K_{Ca} is about $(1.0\pm0.9)\times10^7$ L/mol; K_{NH4} could thus be 5×10^3 L/mol. In the previous study,[11] we found $\sigma_0=(4.3\pm2.5)\times10^{11}$ cm^{-2} in good agreement with this work. In that work, we also found K_H=360±120 L/mol, and so possibly an order of magnitude smaller than K_{NH4}.

Metal Adsorption from APM.

Results from our controlled contamination experiments, where we exposed wafers to HNO_3 solutions and APM containing Ca, are plotted in Figure 2. An enlargement of the origin in Figure 2 is shown in Figure 3. This shows the *common intercept* on $1/\sigma_{Ca}$-$1/[Ca^{2+}]$ plots of all four pH conditions. Numerical results are tabulated in Table II.

We interpret this common intercept according to

$$\frac{1}{\sigma_{Ca}} = \frac{1}{\sigma_0} + \frac{1 + K_R[R^+]}{\sigma_0 K_{Ca}[Ca^{2+}]} \quad [8]$$

where R^+ is either H^+ or NH_4^+. In standard APM (1:1:5 NH_3:H_2O_2:H_2O), equilibrium calculations indicate that NH_4^+ is the major cationic species. We note that σ_0 does not depend on R^+. Thus the common intercept for surface contamination plots where we have both H^+ and NH_4^+ as dominant cationic species strongly suggests that the competitive adsorption mechanism applies in APM. Within the error limits, the intercepts are indeed the same, with an average value of 1.03×10^{-12} cm^2/at., corresponding to $\sigma_0=9.7\times10^{11}$ at./cm^2.

An alternative explanation for these results is that Ca^{2+} reacts with NH_3, forming a species like $Ca(NH_3)_x^{2+}$ (x=2, 4, or 6).[4,7] Such species are known for some cations in aqueous solution: e.g., $Ag(NH_3)_2^+$, $Cd(NH_3)_4^{2+}$, $Cu(NH_3)_4^{2+}$, $Ni(NH_3)_4^{2+}$, $Ni(NH_3)_6^{2+}$, and $Zn(NH_3)_4^{2+}$. When considering adsorption of any of these metal ions, due consideration should be paid to the NH_3 species.[6] For many other metal ions – Ca^{2+} and other alkaline

earth metal ions, for instance – the ammine complexes do not appear to be important, and cannot explain our results.

Studies by Hall *et al.*[7] of the effect of APM dilution with water showed that neither Al or Fe adsorption depended on the dilution, 1:1:5 or 1:1:30 (NH_3:H_2O_2:H_2O). On the other hand, they saw that Zn, Mg, and Ca adsorption increased when diluting the APM chemistry. Mertens *et al.*[6] similarly saw surface concentrations of Al and Fe independent of [NH_3], while Ni and Zn surface concentrations decreased with increasing [NH_3]. We can account for these observations: Al appears to exist in APM as AlO_2^- and $Al(OH_4)^-$ (from calculations using the chemical thermodynamics software package, HSC),[8] and Fe as FeOOH (Ref. 8) or $Fe(OH)_3$(aq) (Ref. 5). These compounds adsorb on the silicon surface through a non-ionic or physical mechanism – for example, by dipole-dipole, dipole-induced dipole or London dispersion force interactions[17] – not mediated by the presence of NH_4^+ or NH_3.

The metals – Zn^{2+}, Mg^{2+}, and Ca^{2+} – that adsorbed more on surfaces as the APM was diluted exist as hydrated metal ions, and thus compete with NH_4^+ for adsorption sites on the oxidized silicon surface. Since [NH_4^+] is lower in 1:1:30 APM than 1:1:5 APM – 1.75×10^{-2} mol/L as compared to 7.94×10^{-2} mol/L – more metal ions can adsorb from dilute APM than from standard APM.

Another issue of potential concern to adsorption models is the silicon etching caused by APM. The etching does not significantly affect metal ion adsorption of species like Ca^{2+} because the metal ion adsorption is fast compared to the etching of the surface. The metal ions on the surface and in solution remain in chemical equilibrium. This contrast to the adsorption of Al and Fe, for instance, which show marked time dependence.[14]

CONCLUSION

NH_4^+ prevents Ca^{2+} adsorption onto wet oxidized silicon surface. The equilibrium constant, K_{NH4}, describing the adsorption of NH_4^+ is about 5000 L/mol, comparable to or larger than the adsorption equilibrium constant of H^+, meaning that NH_4^+ is at least as effective as H^+ in removing metals from the oxidized silicon surface and in keeping metals off the surface. In APM (1:1:5 NH_3:H_2O_2:H_2O) at room temperature, the relatively low Ca^{2+} adsorption on the wet oxidized silicon surface of Si can be explained by competition for adsorption sites with NH_4^+, which is the dominant cation in APM. Our model also helps explain the Ca^{2+} contamination as a function of APM dilution that has been observed by others.

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Table I. Model coefficients for Ca^{2+} adsorption on wet oxidized silicon surface from aqueous solution at room temperature, where σ_{Ca} is in units of 10^{10} atoms cm^{-2}, and concentrations are in units of mol/L.

Term	Coefficient	Std. Dev.
C_0	0.0449	0.0433
C_1	-4.13×10^{-9}	7.49×10^{-9}
C_2	2.03×10^{-5}	1.24×10^{-6}

Table II. Statistics of lines fitting Ca adsorption for different pHs. Units of the slope, *m*, are 10^{-10} cm^2-mol/L-at; units of the intercept, b, are 10^{-10} cm^2/at. r^2 is the correlation coefficient, and df the degrees of freedom for the fit.

pH	3	4.5	5.7	APM
m	$(6.06\pm0.15)\times10^{-08}$	$(4.60\pm0.47)\times10^{-10}$	$(2.87\pm0.27)\times10^{-10}$	$(4.86\pm0.09)\times10^{-08}$
b	$(1.06\pm1.40)\times10^{-02}$	$(1.24\pm0.46)\times10^{-02}$	$(8.54\pm5.19)\times10^{-03}$	$(9.54\pm4.61)\times10^{-03}$
r^2	0.992	0.802	0.829	0.999

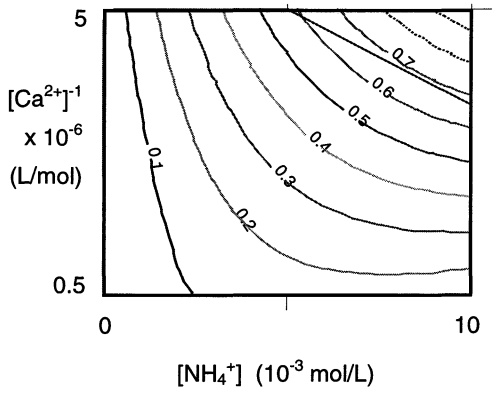

Figure 1. Contour plots of $1/\sigma_{Ca}$ (10^{-10} cm^2/atom) as a function of $[NH_4^+]$ and $1/[Ca^{2+}]$ based on fit of measured areal densities of Ca using full quadratic model (Equation [6]).

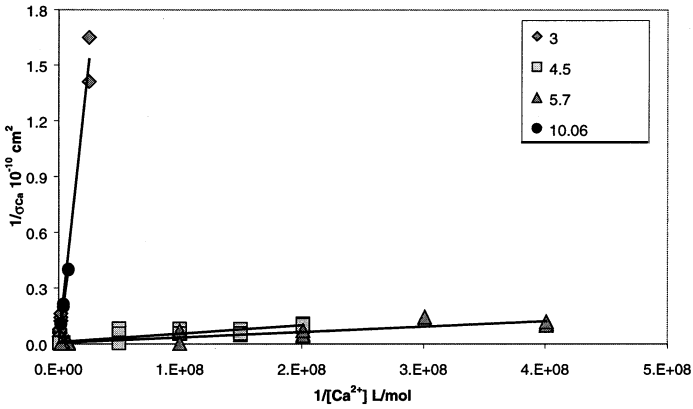

Figure 2. Dependence of inverse Ca surface concentration, $1/\sigma_{Ca}$, on the inverse solution concentration, $1/[Ca^{2+}]$, at pH 3, 4.5, 5.7 (HNO_3), and 10.6 (APM), at room temperature.

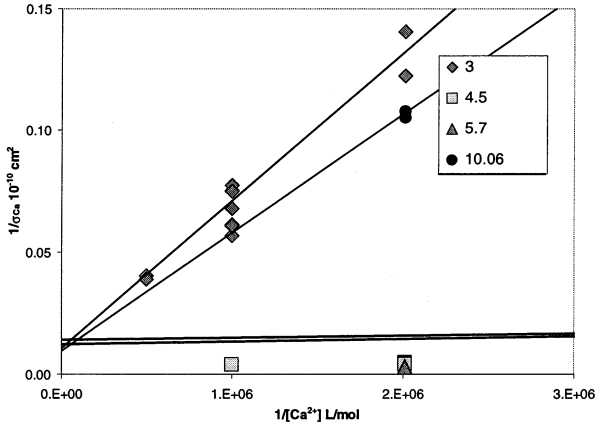

Figure 3. Enlargement of dependence of inverse Ca surface concentration, $1/\sigma_{Ca}$, on the inverse solution concentration, $1/[Ca^{2+}]$, at pH 3, 4.5, 5.7 (HNO_3), and 10.6 (APM), at room temperature.

WETTING PROPERTY OF A LIQUID DROP ON A GEOMETRICAL MICRO SUBSTRATE COMPOSED WITH DIFFERENT SURFACE ENERGY MATERIALS

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Contact angle θ_C for a sessile drop on a heterogeneous (complex) substrate is analyzed experimentally based on the Cassie equation. By using a technique of photo-microfabrication, artificial geometrical lattice pattern which is composed with different surface energy materials are formed. The area ratio for materials was changed widely. When a polar (high surface energy) area isolates in nonpolar (low surface energy) one, it acts to prevent drop extension extremely. As the empirical equation for explaining the contact angle θ_C' on these substrates, $\cos \theta_C' = (2\sigma - 1) \cos \theta_C$, is obtained. (The symbol σ denotes area ratio.) Based on the energy change per unit area during the drop extension, contact angle deviation from the Cassie equation can be explained qualitatively

1. INTRODUCTION

Analysis for wetting property of various liquids on a solid is one important problem on improvement of surface cleaning or etching techniques. As increasing of density of integrated circuits, various wetting processes such as particle removal, etching and plating have been focused. A contact angle of liquid drop has been regarded as one meaningful value to characterize the surface nature of substrate thermodynamically, that is, surface energy. Meanwhile, interest in the drop shape dependence of contact angles of sessile drops on solid surfaces has increased rapidly. (1-5) Present author has also studied for wetting property of a liquid on a geometrical rough surface in microscale.(1)

Generally, in macroscale, contact angle θ_C of a liquid on a complex substrate is analyzed by Cassie as the following equation, Cassie equation.(2)

$$\cos \theta_C = \sigma \cos \theta_1 + (1 - \sigma) \cos \theta_2, \qquad [1]$$

where the symbols, in this case, θ_1 and θ_2, denote contact angles on the nonpolar and polar materials, respectively. The symbol σ denotes area ratio of nonpolar material to polar one on the substrate. By changing the area ratio precisely, contact angle change due to the heterogeneous surface energy is characterized. In this paper, the one aim of this study is to verify the Cassie equation in microscale. Moreover, cleaning processes for G-bit devices manufacture is also studied.

2. EXPRIMENT

The photoresist micro patterns (as the nonpolar material) were formed on the various kinds of inorganic substrates (as the polar materials) in order to fabricate the complex substrates. Figure 1 shows the schematic diagram of the typical test pattern formed by photolithography. The photoresist pattern shape is 50μm square, and the pattern pitch T was changed from 71 to 158 μm. The positive tone (Type-A) and negative tone (Type-B) patterns were also fabricated. Therefore, the area ratio σ of nonpolar material to polar one can be changed from 10 to 90%. An i-line positive working resist of non-commercial version was used for the experiment. The resist contained a resin of mixture with m-cresol/p-cresol/xylenol/formaldehyde novolak. A solvent contained was ethyl-cellosolve-acetate (ECA) of which boiling temperature was 156℃. The photoresist thin films were coated on the 6-inch size Si(100) wafers by the spin coat technique. The wafers were then baked at 200℃ for evaporating the solvent. The film thickness after hard baking was about 2.0μm. The test patterns as illustrated in Fig.1 were exposed to the resist layer. The stepping exposure system, NSR1505i3A made by Nikon was used. After the exposure, photoresist patterns were developed. As the developer, TMAH (tetra-methyl-ammonium-hydroxide) 2.38% solution was used. Subsequently, the photoresist patterns were exposed to the deep ultraviolet light (λ=350nm) and then baked at 200℃ for 5min. By these treatments, a slight hardened layer can be formed of the resist surface, which has an effect to protect to intrusion of a liquid into resist materials. The static sessile drop technique for contact angle measurement was adopted using a goniometer. In the sessile-drop technique, the sample substrates examined were placed in a controlled atmosphere chamber. The chamber with sample substrate remained closed 1-2h to achieve equilibration between the phases. As a liquid drop, deionized water was used. The liquid drop was introduced onto the sample surface through a microsyringe, and the needle remained in contact with the drop. Precautions were taken in the measurements to avoid distortion of the drop shape by the needle. Any immersion of the needle into the liquid drop and any pulling of the liquid with the needle was avoided and thus there was no distortion of a shape of the liquid drop. Therefore, in this case, an intermediate contact angle can frequently be

observed instead of the advancing or receding contact angle.

3. RESULTS AND DISCUSSION

In Fig.2, the plan views of water drop on the complex substrates are shown. After visual observations of water drops at the complex substrates, the drop shapes on the Type-A substrate are mostly circle, however, those on the Type-B substrate are slightly distorted into square. A highly irregular shape of the water drop base at the Type-B substrate, especially for higher area ratio σ, significantly affected the contortion of the water-air interface in the vicinity of the solid-liquid-air contact (three-phase) line. In this case, spontaneous jumps of a segment of the three phase contact line from one site of the complex surface onto another site were observed, indicating energetic barriers in the system. One can safely state that the polar substrate on which the nonpolar materials locate has an effect to prevent the extension of drop of polar liquid, that is, "pinning effect". In this case, a crimping will lead to a tendency for the microscopic three-phase line to elongate spontaneously, provided that the radius of curvature of the drop is not too much larger than the distance between polar sites in the case of 90% of σ for Type-B. Good et al. discussed that isolated polar sites or patches on a nonpolar surface would lead to microscopic convolution of the liquid-vapor interface near the solid, associated with contortion of the three-phase line.(3) Moreover, they mentioned that the microscopic contortion of the three-phase line would exist despite an apparent smooth, e.g., circular, nature of the macroscopically observed drop perimeter.

In Fig.3, the variation of cos θ_C value on the complex substrates are shown. The calculation values based on Cassie equation are also plotted. The cosθ_C value on the Type-A substrate are in good agreement with the theoretical one, however, those on the Type-B substrate are not. The empirical equation for explaining the contact angle θ_C' on type-B substrate is shown as follows.

$$\cos \theta_C' = (2\sigma - 1) \cos \theta_C \qquad [2]$$

In this case, the density of the polar material pattern isolated on the nonpolar substrate is strongly affect to the drop shape distortion and contact angle change. Drelich et al. also proposed an equation which is a modification of Cassie equation, to incorporate the line tension contribution to the analysis of the wetting properties of complex surfaces.(4)

Hence, the drop extension on the both type substrates can be explained based on the free energy model as illustrated in Figs.4(a) to 4(c). These figures present sectional view of the liquid-substrate system on the view point of wetting resistance. In some

systems, the contortion of the drop surface may extend over the entire drop volume, particularly for a Type-B substrate. It is expected that the isolated polar site acts to prevent the extension of the drop when contortion of the drop surface takes place. Moreover, when the front of a polar liquid (deionized water) extension, there is a tendency for the liquid to stay at polar sites of the complex surface, due to stronger interactions between polar phases than between polar liquid and nonpolar surface sites. Li et al. also considered a model which surface is a smooth but heterogeneous, consisting of two type patches.(5) However, it should be pointed out that the Young equation is derived by assuming that the solid surface is rigid, smooth, and homogeneous. Under this condition, the three phase contact line of a sessile drop on the solid surface is a smooth circle. As shown in Fig.4(a), Young equation can be derived based on the energy balance when a liquid drop extends slightly and, defined as a following equation.

$$\gamma_s \Delta x \Delta t - \gamma_{sl} \Delta x \Delta t - \gamma_l \Delta x \Delta t \cos\theta = 0 \qquad [3]$$

$$\gamma_s - \gamma_{sl} - \gamma_l \cos\theta = 0 \qquad [4]$$

and

$$\gamma_s' - \gamma_{sl}' - \gamma_l \cos\theta' = 0 \qquad [5]$$

where symbols, γ_s', γ_{sl}' and θ' represent surface energies and contact angle after liquid extension.

Hence, if we then make the approximation,

$$\gamma_s >> \gamma_{sl} \quad : \quad \gamma_s' >> \gamma_{sl}' \qquad [6]$$

then,

$$\cos\theta / \cos\theta' = \gamma_s / \gamma_s' \qquad [7]$$

If the surface energy γ_s' is greater than γ_s, i.e., $\gamma_s' > \gamma_s$ (Type-A), contact angle θ' should be less than θ, i.e., $\theta' < \theta$. On the contrary, in the case of $\gamma_s' < \gamma_s$ (Type-B), $\theta' > \theta$ can be derived. This may lead to an increase in the excess energy of the entire drop per unite length of the three-phase contact line in the case of Type-B substrate. One can safely state that there is a tendency for the advancing liquid front to locate at polar sites of the complex surface. It should be remembered, in a formulation of such theoretical relationship, that the solid surface heterogeneity causes irregularities in the shape of the three-phase contact line of liquid drop, and these may affect a variation of the internal free energy of the liquid drop at such complex surface. Therefore, as seen in Figs.4(b) and 4(c), the value of contact angle of a sessile drop on the complex substrates will

depend not only on the area ratio of composed materials, σ, but also on the density of the polar material pattern isolated.

As a consequence, the contact angle θ_C on the Type-B substrate is larger than the contact angle value expected theoretically from an analysis of thermodynamics for the system as seen in Fig.3. A reverse situation is for the contact angle θ_C on the Type-A, and the contact angle value is good agreement with that expected theoretically.

4. CONCLUSION

For a sessile drop on an artificial complex substrate, the observed area ratio dependence of contact angle cannot be simply interpreted in terms of the Cassie equation, because the liquid drop perimeter is not a circular nature. The model used in this paper indicates that an experimental observation of an distortion in the liquid drop shape with changing area ratio of complex materials is due to pinning effect of isolated polar site on the complex substrate. On the view points of electronic device manufacturing, the complex substrate can be regarded as one typical meaningful structure. The present author believe that the results in this article would affect to improve reliability of wetting processes, such as cleaning, etching, drying and pattern developing.

ACKNOWLEDGEMENTS

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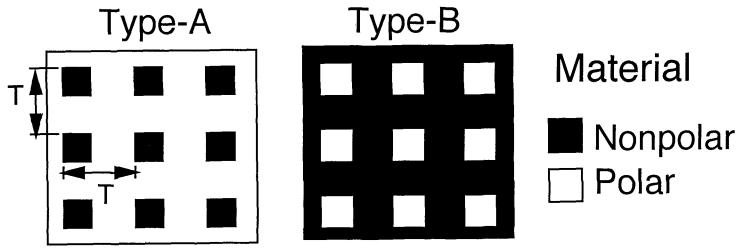

Fig.1 Geometrical complex substrates fabricated by photolithography.

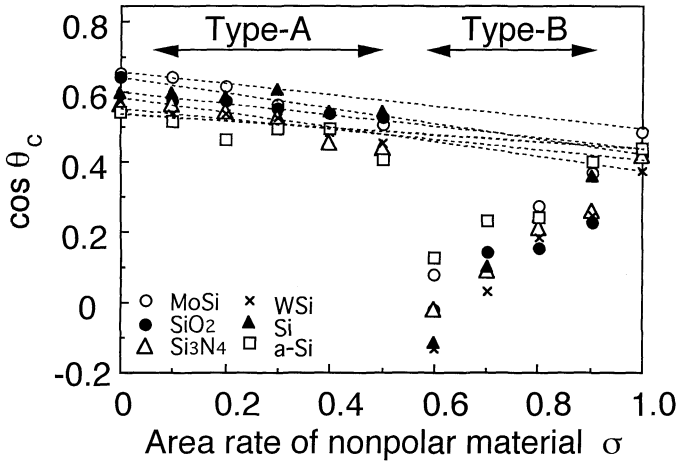

Fig.3 Contact angle of water drop on the complex substrates.

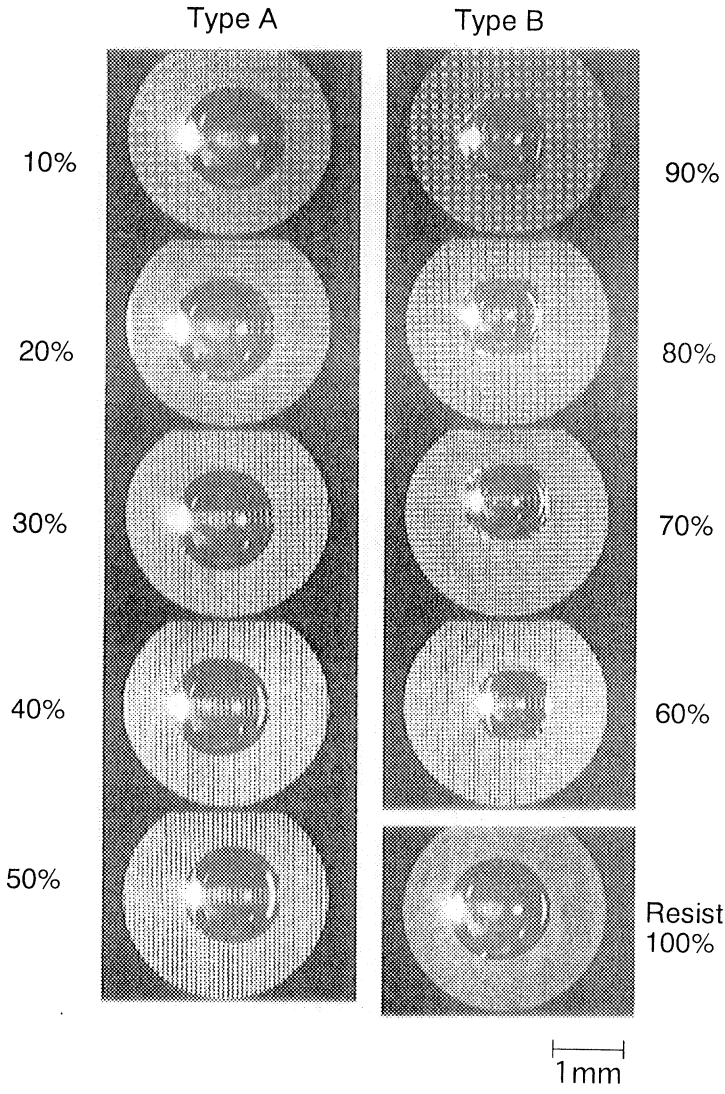

Fig.2 Photograph of liquid drop shape (plan view) on the complex substrate.

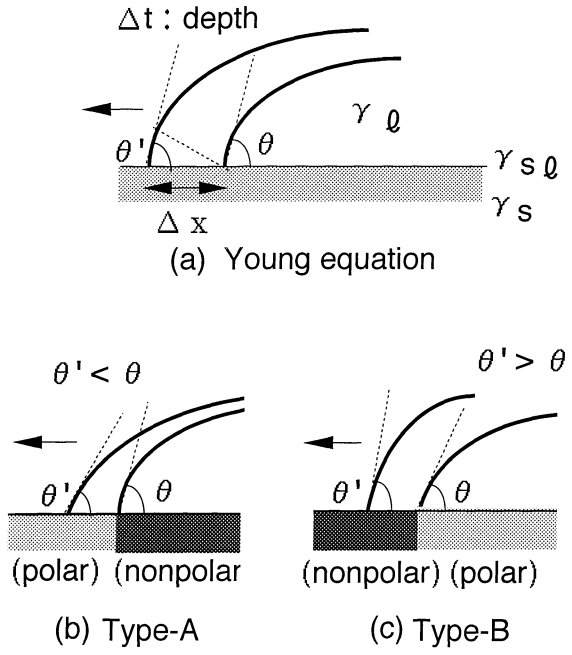

Fig.4 Drop extension model on the complex substrates.

ELECTROCHEMICAL STUDY OF THE ETCHING RATE OF SILICON SUBSTRATES BY DILUTE AMMONIA SOLUTIONS

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The surface reactivity of silicon substrates during etching by ammonia solutions either pure or containing H_2O_2 was characterized by electrochemical methods, mainly open circuit potential monitoring, current/voltage diagrams and electrochemical impedance spectroscopy. Results were complemented by scanning electron microscopy. The general trend is that pure ammonia solutions either degassed or oxygen saturated induce a rapid etching of the silicon surface leading to the formation of non protecting silicon oxide micropyramids. In the presence of H_2O_2, the ammonia solution promotes the formation of a polished surface protected by a passivating layer of oxide. But a smooth hydrophilic surface obtained by SC1 treatment shows the appearance of corrosion pits when immersed in a NH_4OH solution.

Finally data derived from the current/potential diagrams and electrochemical impedance spectroscopy lead to common values of the polarization resistance which can be used for the evaluation of the electrochemical etching rate.

INTRODUCTION

RCA cleaning procedures are constantly used for the surface conditioning of the silicon wafers utilized for the preparation of integrated circuits. More studies are required for the optimization of the performance and the economy of the processes. Dilute ammonia solutions are known to be efficient etchants often used for the micromachining of silicon substrates. The anisotropic etching of silicon surface in aqueous alkaline solutions has been applied to produce various microstructures such as grooves, cantilevers or diaphragms [1]. Some papers also deal with the silicon or silicon oxide etching rate using masks which protect part of the surface. Then the steps obtained after reaction are viewed and their height measured by atomic force microscopy [2]. On the other hand, the addition of H_2O_2 leads to a cleaning solution, standard clean SC1, promoting a pol-

ished hydrophilic surface of the semiconductor. This reactant, first introduced by Kern and Puotinen [3], was efficient to build up a passivating oxide layer, characterized by the vibrations of Si-OH and Si-O-Si bonds observed by HREELS [4] spectroscopy. The OH groups are suggested to be responsible for the surface hydrophilicity. The etching mechanism was studied by Van den Meerakker [5] who found that a minimum concentration of 3.10^{-3} M H_2O_2 was necessary to generate passivation. The residual etching rate was determined by masking part of the silicon surface, and measuring the step height after immersion in SC1. Kobayashi [6] found a steady regime value of 7 Å/mn, in SC1 at 80°C, while more recently Storm et al. [7] determined the rate at room temperature, at 60°C, and 85°C.

The aim of the present work was to undertake a fundamental study of the silicon reactivity in ammonia solutions, using electrochemical methods implying open circuit potential (OCP) monitoring, voltammetric diagrams and impedance spectroscopy. The silicon surface behaviour was studied as a function of the electrolyte composition, with or without added H_2O_2, and also depending on the previous treatment, hydrophilic or hydrophobic. The surface morphology after etching was examined by atomic force and by scanning electron microscopy. The electrochemical parameters will give useful informations on the corrosion/passivation processes at the semiconductor surface.

EXPERIMENTAL

Silicon wafers used in our experiments, (100) oriented, 200 mm diameter and 705-745 μm thick, produced by MEMC Electronic Materials, were provided by IBM France.

p-type wafers, boron doped, ($\approx .10^{15}$ at.cm^{-3}), R = 9-18 Ω.cm

n-type wafers, phosphorus doped, ($\approx 5.10^{14}$ at.cm^{-3}), R= 8-24 Ω.cm

The samples were mirror polished for MOS applications, and their back side covered with a Ga-In alloy. Before each experiment, the silicon samples were thoroughly rinsed with ultra pure water and cleaned by a HF+ HCl solution during 25 min at room temperature to promote a hydrophobic H-terminated silicon surface, and then treated by a SC1 solution during 40 min at room temperature. The studied sample surfaces were either hydrophobic, the final treatment being HF+HCl, or hydrophilic the final step being SC1 reagent.

The solutions were prepared by using SLSI grade (Sub Large Scale Integration, metal elements below 1 ppb) reagents, and diluted with 18.2 MΩ ultrapure water UPW obtained after deionization and ultramicrofiltration (0.05 μm). Most often the solutions were used as prepared. But in order to examine the influence of dissolved oxygen some experiments were conducted with solutions deaerated by bubbling high purity argon gas N60 grade, or saturated by oxygen gas N55 grade. In this case bubbling was achieved under isopiestic conditions, i.e. the gas flow was beforehand saturated with ammonia at the same chemical potential. All experiments were performed in the dark at room temperature generally equal to 25°C. These experiments were achieved with a home-built electrochemical cell [8], for reproducible open-circuit potential recordings by rigorous

control of the oxygen content, exposure to light and purity of the chemicals. In our cell the silicon wafer was in contact with a Teflon tube, filled with the electrolyte, and pressed between two polyvinyl plates. The whole cell is protected against room light by means of a closed cylinder made of black polyvinyl polymer. A special device [8] provides the feeding of the cell with beforehand conditioned electrolyte. The reference electrode was a saturated calomel electrode (SCE), connected to the electrolyte by means of a saturated KCl-agar salt bridge made of a Teflon tube.

The OCP measurements, voltammetric curves, and electrochemical impedance spectra were obtained using an EG&G PAR Model 273A potentiostat connected to an impedance analyzer, Solartron 1260. The AC and DC experimental points were respectively acquired by means of Zplot and Corrware softwares, driven by an IBM PC. The impedance data, obtained under potentiostatic control with a signal amplitude of 10 mV, generally in two frequency ranges, 10 KHz to 1 Hz, and 10 Hz to 0,05 Hz, were plotted following a Nyquist diagram and most generally were represented as a well shaped semicircle centered very close to the x axis. This result indicates that the impedance could be represented as a RC parallel circuit with a small value series resistance. From these diagrams, the polarization resistance values were calculated using a circular regression fitting. It is interesting to indicate that these values were quite identical to those obtained from the slope of the voltammetric curves recorded in a $\pm$ 50 mV/SCE range near the OCP, by means of a Stern regression method software. The frequency values were chosen in such a way that the time required to record a spectrum was 52 s in the high frequency range and 2 min 22 s in the low frequency range. Successive series of OCP measurements, current voltage diagrams, and impedance plots were recorded as a function of time in order to follow the kinetics of the surface transformation.

RESULTS

The large number of obtained results were characteristics of a corrosion/passivation system, and showed the striking influence of H_2O_2 even at very low concentration in the NH_3 solution.

Open Circuit Potentials. OCP was quite interesting, in that it is characteristic of the anodic and cathodic surface sites reactivity, as it was shown in our recent publication [9]. The present results indicate that, when the Si surface, either n- or p- type, is not protected by a passive layer, the OCP in deaerated ammonia solutions is extremely negative, say near -1150 mV for n-type and near -1050 mV/SCE for p-type Si in the dark. For example, using a n-Si substrate, after hydrophobic HF+HCl treatment, in contact with a deaerated 1% NH_3 solution, the curve a in figure 1 was obtained. From our concept, this value of OCP was characteristic of a high anodic site reactivity. The observation with scanning electron microscope (SEM) showed that, after a few minutes, the surface smoothness was considerably altered by the appearance of corrosion pits and Si oxide micropyramids generation.

On the contrary, a hydrophilic Si surface, protected by a passivation layer after SC1 treatment, remains quite stable in NH_3+H_2O_2 1% each solutions. The OCP values

were more positive and equal to -800 to -850 mV/SCE (curve e). At the end of the experiment, the surface appeared perfectly bright; no defect could be detected by SEM nor AFM observation.

When H_2O_2 is present in ammonia solutions even at such a low concentration as 0.03%, a protective passivating layer was built up leading to a bright smooth surface.

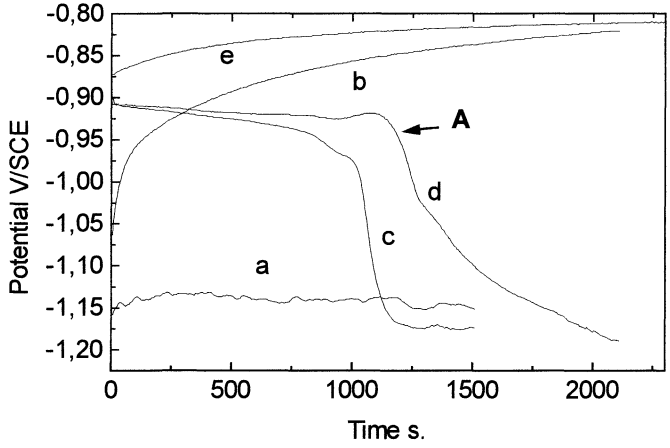

Fig.1 : Open circuit potential records of n-Si in contact with 1% NH_3 solutions, in the dark.
a : Hydrophobic surface in deaerated NH_3 solution.
b : Hydrophobic surface in NH_3+H_2O_2 solution.
c and d : Hydrophilic surface in deaerated NH_3 solution.
e : Hydrophilic surface in NH_3+H_2O_2 solution.

Thus, in a NH_3+H_2O_2 1% each solution, the OCP of a hydrophobic Si sample, starts from a rather negative value (curve b) and gradually moves towards more positive values reaching -800 mV/SCE after 20 min. At the end, the surface became hydrophilic, and the corrosion rate dropped to a negligible value, as if the sample was treated by SC1 reactant.

Finally, a hydrophilic Si surface after SC1 last treatment behaves firstly as passivated when immersed in a 1% NH_3 solution; But after a few minutes, a sudden drop of potential to values near -1200 mV/SCE appears (curves c and d), while a steep increase of the corrosion rate was observed. This behaviour is typical of the breaking down of the passivating layer. The shift of potential to quite negative values is interpreted as being the consequence of the activation of anodic sites initiating pitting corrosion.

Electrochemical Impedance Spectrocopy (EIS). Quantitative parameters related to the kinetics of surface properties evolution were obtained by electrochemical impedance spectrocopy and confirmed our interpretation based on the build up or the breakdown of

a protective passivating layer. The measurements were constituted of a series of impedance diagrams inserted in the OCP monitoring experiments. The range of frequencies was selected in order to obtain the significant part of the diagram within a short time so as to have a constant surface state during the data acquisition. Typical experiments were constituted of a series of sequences, OCP record 1 min., EIS at zero current in the range 10Hz-0.05Hz 3 min, again OCP 1 min, etc.. . Indeed, from a preliminary study of the impedance diagrams we could check that the simple equivalent circuit proposed by Morrison [10] was valid with a good approximation. As shown in fig.2, the interface in the dark could be modeled by 2 loops corresponding respectively to the semiconductor space charge region and the electrolyte double layer including the charge transfer reaction R_{ct}; the uncompensated solution resistance was negligibly small in our experiments. In fact we obtained well shaped semicircle Nyquist diagrams, the center being very close to the real axis as expected from the model.

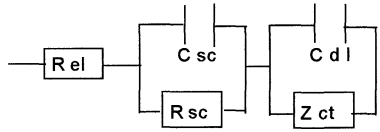

Fig. 2. Simple equivalent circuit representing the Si/electrolyte interface in the dark.

To support our interpretation of a corrosion/passivation process, the significant part of the circuit was the loop corresponding to the double layer capacity in parallel with the charge transfer resistance giving the surface electrochemical reaction rate.

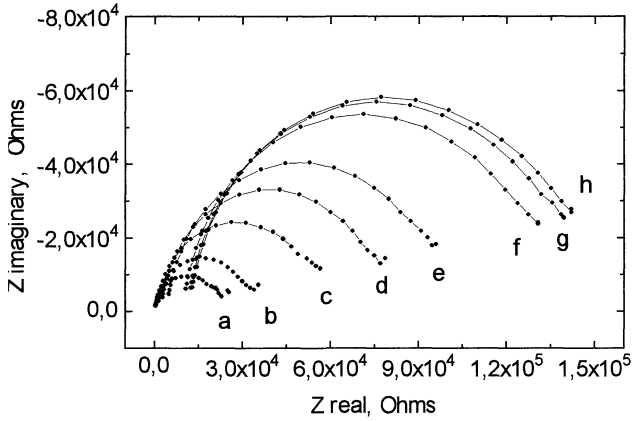

Fig. 3: Successive Nyquist diagrams of hydrophobic n-Si surface in NH_3+H_2O_2 solution
a: initial: b,c,d,e,f,g,h,: subsequent curves obtained at 4 min time intervals.

The first example is given in fig.3 representing the time variation of the Nyquist diagram resulting from the build up of a passivating layer after reaction of NH_3+H_2O_2 on a n-Si initially hydrophobic surface. The experimental procedure corresponds to curve b of fig.1. The EIS diagrams show a steep increase of the polarization resistance, from 14 to 134 kΩ.cm². Meanwhile the capacitance decreased from 11 to 3 μF/cm², the effect could be assigned to a thickening of the protecting layer. The observed shift of the semi circle was due to a simultaneous growth of the semiconductor space charge impedance.

The reverse phenomenon was obtained with a hydrophilic n-Si surface, protected by its passivating layer, in a degassed NH_3 solution (Fig 4), the situation corresponding to curve c of fig.1. In this case, the initial charge transfer resistance was high, near 200 kΩ cm² and dropped rapidly to less than 4 kΩ cm² but the capacitance, derived with the use of the circular regression software, changed moderately from 10 to 6 μF/cm².

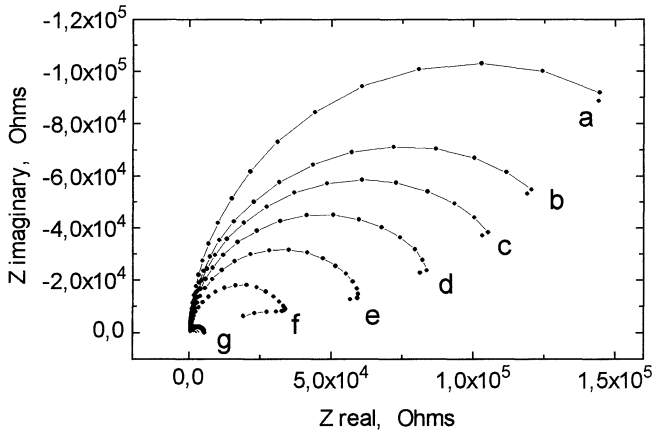

Fig. 4: Successive Nyquist diagrams of hydrophilic n-Si surface in NH_3 solution
a: initial: b,c,d,e,f,g,: subsequent curves obtained at 4 min time intervals.

An interesting feature of these results is that the two sets of curves are similar except that the changes are opposite in direction. Moreover, the resistance value of the so-called « not protected » surface is identical to that obtained from EIS diagram obtained with hydrophobic n-Si in a 1% NH_3 deaerated solution. Finally, the real component of the impedance was identified as being the charge transfer reaction rate as determined by linear sweep voltammetry.

Current/Potential diagrams. More informations concerning the anodic and cathodic site reactivity were obtained from voltammetry in a narrow range of potential, for example ±50mV around the OCP, so as to have current density values less than a few μA/cm². These studies were highly interesting in several respects.

First, as shown on fig. 5, the slope $(dE/di)_{i=0}$ of the voltammetric curve in the narrow range of potential gave a value of the polarization resistance quite identical to that obtained by EIS and then supported the attribution of the recorded impedance loop.

Second, a voltammetric study in a wider range of potential i.e ± 200 mV near the OCP lead to an estimation of the respective contributions of anodic and cathodic current values. The log.i processing software, showed very clearly that, during the surface pas-

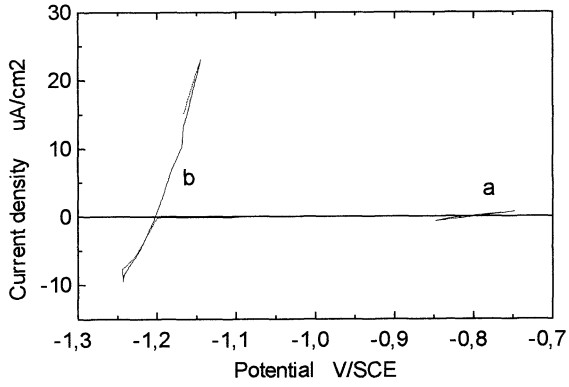

Fig.5: Voltammetric curves for hydrophyllic n-Si in NH3 solutions. Same experiment as described in fig.4. a: initial passivated surface, b: final corroding surface.

-sivation after $NH_3+H_2O_2$ treatment, both anodic site and cathodic site reactivities are inhibited but the inhibition of anodic sites is much more effective.

This result agrees with our interpretation that the shift of OCP towards negative values could be correlated with the appearance of corrosion pits initiated at anodic sites. In fact the electrochemical data of this study were confirmed by SEM and AFM surface analysis. The passivated surfaces appeared smooth and clean, but the initiation of pitting corrosin was identified by stopping an OCP monitoring experiment at a time represented by point A on fig.1. A few first pits were clearly observed by SEM as shown on fig.6.

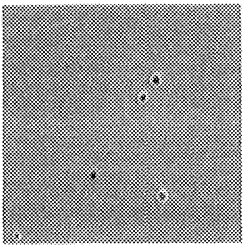

Fig.6: SEM view of corrosion pits initiated at a n-Si surface passivated by SC1 last treatment.

DISCUSSION

These accurate studies of surface characterization by their electrochemical properties lead to several useful conclusions regarding the behaviour of Si substrates in alkaline ammonia solutions, in the dark. The OCP monitoring together with the analysis of voltammetric diagrams permit to separate the contribution of anodic and cathodic charge transfer reactions which are responsible for the material transformation at the interface. Only one reaction can occur on the anodic sites, corresponding to the ionization of elemental silicon, which results in electron injection in the semiconductor. These electrons are consumed on cathodic sites ending at the evolution of H_2 molecules or reduction of H_2O_2 depending on the composition of the solution. The expression of the O.C.P.value, Er, is derived from the mixed potential resulting of these electrochemical reactions:

$$E_r = \frac{\alpha E_1 + \beta E_2}{\alpha + \beta} + \frac{RT}{nF(\alpha + \beta)} \ln \frac{j_{0C}}{j_{0A}}, \qquad (1)$$

where E1, E2, α and β are respectively the equilibrium potentials and the transfer coefficients of the electrochemical reactions. j_{0A} and j_{0C} are the exchange current densities, characteristic of the electronic transfer rate at anodic and cathodic sites.

The reaction of Si with ammonia aqueous solutions is generally assumed to be purely chemical, the diffusion of molecules in the surface layer being rate determining. We also could assume that EC mechanisms (electrochemical coupled with chemical reactions), with the same diffudion rate control could be involved. For example the transfer resistance determined by EIS can be related to the corrosion current by the expression:

$$R_T = RT/(\alpha+\beta)nF\, i_{corr} \qquad (2)$$

From the R_T value obtained for n-Si in SC1 solutions in the dark at room temperature the corrosion rate was found equal to 0.2 $\mu A/cm^2$, which leads to an etching rate estimated to 0.86 nm per hour, which is in agreement with the 0.95 nm value determined by Storm et al. [7] experiments. Such close results are certainly due to a mere coincidence, because experimental values are somewhat scattered. But the determination of the electrochemical polarization resistance appears as a good tool for the evaluation of the etching rate [11], and the optimization of the ammonia-hydrogen peroxide mixture (APM) for the Si wafer wet treatment.

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THE VISUALIZATION AND THE SIMULATION OF ULTRASONIC TRANSMISSION THROUGH SI IN MEGA-SONIC SINGLE WAFER CLEANING SYSTEM

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During Mega-sonic backside wafer cleaning in fabricating LSI's, some patterns on the surface-side were damaged. It was caused by ultrasonic vibration transmitted through Si. The damage density was closely related to the transmissivity. The ultrasonic transmissivity by measuring sound pressure depended on the incident angle and Si wafer thickness. There was the special area around 30degree of incident angle where the transmissivity had maximum value. To confirm these phenomena we simulated the ultrasonic transmission using "Finite Element Method (FEM)" and visually observed them by "Schlieren Method System". According to these results, we understood that maximum transmissivity was caused by the Lamb wave which was asymmetrical bending motion of the plate. It was generated on a certain condition of wave incident angle and Si thickness, and also mega-sonic frequency. And it regenerated new vibration into water toward both side of the wafer. It was observed as a part of transmission.

INTRODUCTION

As the VLSI integration scale increases, it becomes more important to decrease particles on the Si wafer surface during semiconductor manufacturing. We found that especially before bath type wet cleaning process, backside wafer cleaning is necessary to prevent "recontamination" on the wafer surface. 1) To remove backside particles, the single wafer scrubber shown in Fig. 1 is applied. It is called Mega-sonic because of having an ultrasonic water jet around 1.0MHz frequency. 2) During Mega-sonic backside cleaning, some VLSI devices on the surface-side of the wafer, were damaged by ultrasonic vibration of water transmitted through Si. To confirm this transmission, we measured ultrasonic sound pressure in water through Si and without Si, in condition of 0~60degree wave incident angle and 280~3000μm Si wafer thickness. Transmissivity is defined as the ratio of a sound pressure through Si wafer to the one without Si wafer. As the

results of these experiments, we found that the transmissivity depended on both of incident angle and Si thickness. 3) Typical θ-dependence of transmissivity data for 1.5MHz ultrasonic wave at 550μm Si thickness is shown in Fig. 2. Transmissivity is gradually decreased with increasing incident angle θ, and there is the special area around 30~40degree of θ where the transmissivity has maximum value. Incident angle for the starting point of this special area is 15 degree. We understood this by "Principle of Agreement" theory 4). There are two kinds of waves near Si surface. They are the longitudinal wave of incident ultrasonic sound in water, and the transverse wave on Si surface caused by sound impact. According to this theory, the maximum transmission is generated if these two waves are "in phase".

$$\sin\theta = (\lambda w / \lambda ss) = (Vw / Vss)$$

$$\therefore \theta = \arcsin (Vw / Vss)$$

Where θ is incident angle, λw is wavelength of longitudinal ultrasonic wave in water, λss is wavelength of transverse wave on Si surface, Vw and Vss are velocity of these waves.

$$\therefore \theta = \arcsin(1483[m/sec] / 5843[m/sec]) = 14.7°$$

Therefore the angle of starting point for transmission increase is actually 14.7 degree. In spite of changing thickness, this starting point is at constant value that is corresponding to maximum transmission of bulk Si. And when Si thickness becomes thinner, less than 2000μm, incident angle θ causing maximum transmission value become larger than that of bulk Si. Vss also can be shown as,

$$Vss = \sqrt{(G / \rho)}$$

where, ρ is the density of Si and G is shear modulus of (100) bulk Si. We speculated that the "regarded shear modulus" of thin wafer Si (Gt) became smaller than "real shear modulus" of bulk Si (Gb), then velocity of wafer Si (Vss) became smaller than that of bulk Si, and finally maximum transmission angle of wafer Si became bigger than that of bulk Si. But this speculation was wrong as descrived later. Because this experiment was done at intervals of 5degree and transmissivity data by sound pressure was rather inacurrate, therefore we could not distinguish between phenomena of the starting point and the maximum area.

SIMULATION

The simulation of the ultrasonic transmission was achieved using "Finite Element Method (FEM)" 5) for the coupled piezoelectric-acoustic problem. Simulation tool was PZFlex Ver. 2.6 (Weidlinger Associate Inc.). Calculation was done in various Si thickness (280~3000μm) and in various incident angle (0~60 degree) at 1.567KHz. Furthermore, to compare with the data from visualization

experiments, additional calculations were done in various ultrasonic frequencies (1, 1.5MHz), with not only Si but also GaAs wafer. Firstly observing the sound propagation in water to Si wafer calculated at every microsecond, we can easily see that the transmission through 550μm Si wafer at 30degree was larger than that at 0 degree. And continuously observing the inside of Si wafer especially at 30degree, like as a slow motion video picture, we also can see "Lamb wave". "Lamb wave" is the asymmetrical bending motion of the thin Si plate generated by the incident ultrasonic vibration (Fig. 3).

The result of transmissivity vs. incident angle data of 550μm Si is shown in Fig. 4. At the maximum transmissivity area, the simulation result shows clearer peak than experimental data of sound pressure values measured by acoustic sensor. Furthermore there are two peaks in the simulation curve. The lower peak is located around 15degree, therefore it must be correlative with sound velocity in bulk Si. The higher peak is located around 30degree, therefore it depends on the "Lamb wave" generated in Si wafer. 6) The results of transmissivity data of various Si thicknesses are shown in Fig. 5. The lower peak is independent of Si thickness. And the higher peak is changed with thickness, θ max which is incident angle for higher peak becomes bigger with decrease of thickness. According to further calculations, the lower peak is also independent of ultrasonic frequency. This tendency of GaAs is clearer than that of Si. And higher peak is changed with frequency and thickness. And if the product of thickness and frequency is the same, θ max of two cases become the same value. This will be discussed later.

VISUAL OBSERVATION

The visualization of the ultrasonic transmission was achieved using "Schlieren Method System". In this system the deviation of index of refraction caused by ultrasonic wave in water was optically observed by CCD camera (Fig. 6). 7) The visualization was done in various incident angle (0~45degree) and in various Si thickness (280~3000μm) at various frequency (0.96, 1.5, 3.36MHz). In Fig.7 which is an example view of the results of 550μm Si thickness. The strongest ultrasonic transmission is observed especially at 30degree incidence. According to the image analysis of this picture, intensity of incident wave becomes larger than original value. This increase is remarkable at 0degree and 30degree. At 0degree, we can easily understand that the reflection wave is added to incident wave. On the contrary, the phenomenon at 30degree is a little bit complex. The reflection wave is gone to other direction and the new vibration generated by Lamb wave is added to both directions of incident wave and transmitted wave. From all of these pictures of Schlieren image, we picked up θ max values in each thickness wafer at each frequency. The relationship between θ max and thickness was plotted. As described in last paragraph of simulation, θ max data seems to be the function of the b*f product. Therefore when the θ max data were plotted against the product of thickness and frequency (b*f), they were almost on the same line. And they were agreement with the results of the simulation as shown in Fig8.

DISCUSSION

In case of thin plate, not only the surface wave but also "Lamb wave" (asymmetrical bending motion) is generated. "Lamb wave" is propagated between two surfaces of Si wafer as a result of combination between P-wave (longitudinal wave) and SV-wave (transverse wave). The boundary condition of the propagation of "Lamb wave" is that Si wafer is thin enough and approximately infinite plate. According to "the principle of agreement" between the velocity of incident wave in water (Cw) and the phase velocity (ω/k) of Lamb wave, following equation is concluded. 4) 6)

$$(\omega/k)\sin\theta \max = Cw$$

Where ω is angular velocity, k is wave number and θ is incident angle. On the assumption that Si thickness b is much smaller (negligible) than wavelength in Si (λsi), and applying asymmetric mode, the equation is changed to

$$(Cw/\sin\theta \max)2 = (\omega/k)2 = 2b\omega/Ct \sqrt{-}\{1-(Ct/Cd)2\}/3$$

Where Cd is the velocity of longitudinal wave in Si and Ct is the velocity of transverse wave in Si. Substituting these numerical value 4) 8) and equation; Ct: 5843m/sec, Cd: 8431m/sec, Cw: 1483m/sec, $\omega=2\pi f$, for each item in above equation, θ is calculated as follows.

$$(1483/\sin\theta \max)2 = 2b*2\pi f*5843 \sqrt{-}\{1-(5843/8431)2\}/3$$

$$\sin\theta \max = \sqrt{-}(144\mu m MHz/2b*f)$$

$$\theta \max = \arcsin \sqrt{-}(144\mu m MHz/2b*f)$$

From this equation we can easily understand that θ max is the function of the product of thickness and frequency (b*f). And this fact agrees with the results of the visualization data using Schrielen method. (Fig. 9)

CONCLUSION

According to the result of the simulation using "Finite Element Method (FEM)" and the visual observation by "Schlieren Method System" for ultrasonic transmission through Si, we can understand that maximum transmissivity was caused by "Lamb wave" which was asymmetrical bending motion of thin Si plate. "Lamb wave" is generated on a certain condition of wave incident angle and Si thickness, and also Mega-sonic frequency. The new vibration regenerated into water by "Lamb wave" is observed as a part of transmission. We offer the condition of generating "Lamb wave" to think about the mechanism of

simultaneous both side cleaning system using Mega-sonic.

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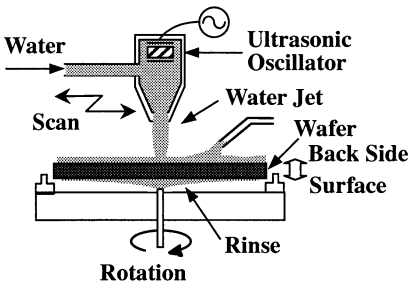


Fig. 1 Single Wafer Scrubber

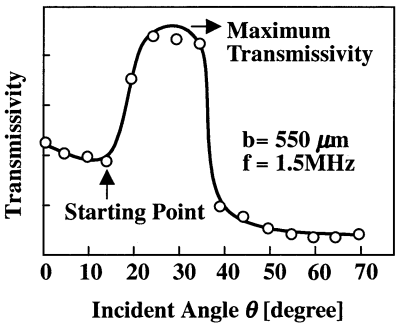


Fig. 2 Ultrasonic Transmissivity

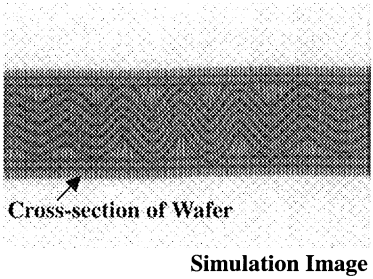


Fig. 3 The Lamb Wave

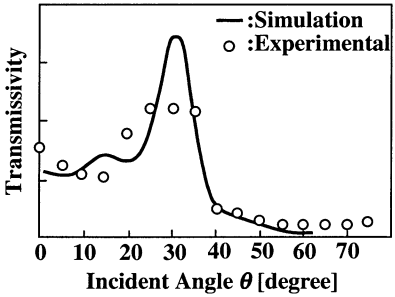


Fig. 4 The Result of Simulation

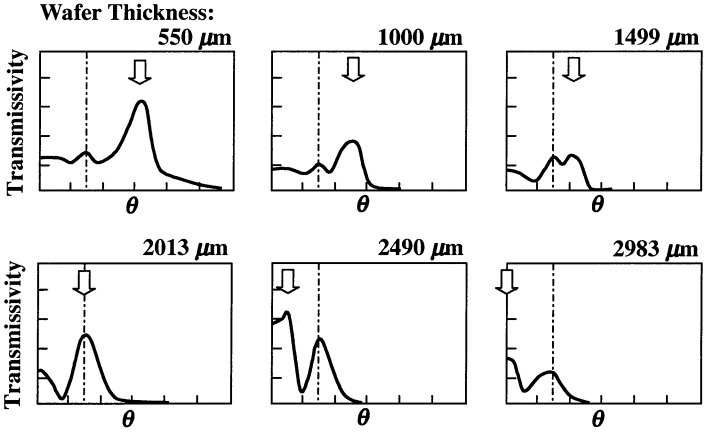


Fig. 5 The θ -dependence on Ultrasonic Transmissivity through various Thickness Si Wafers

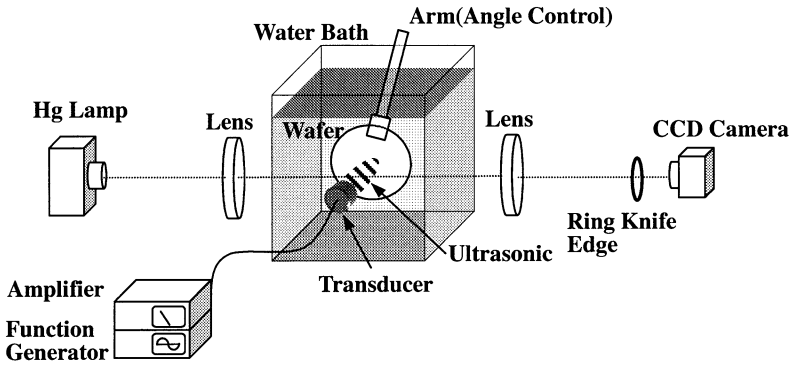


Fig. 6 Observation Arrangement of Schlieren Method

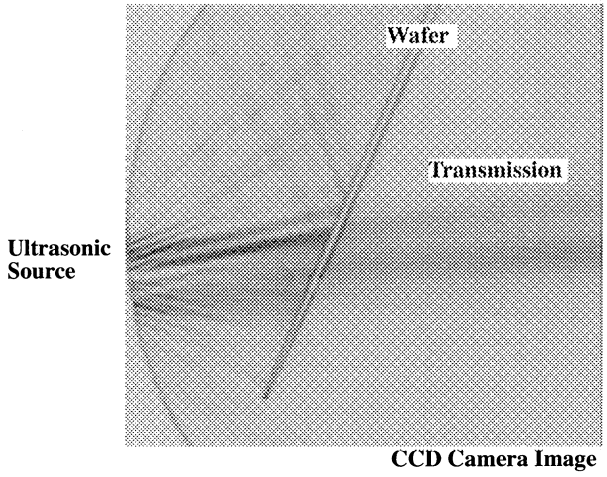


Fig. 7 Schlielen Image of 550 μm Si at 30 degree Incident angle (1.5MHz)

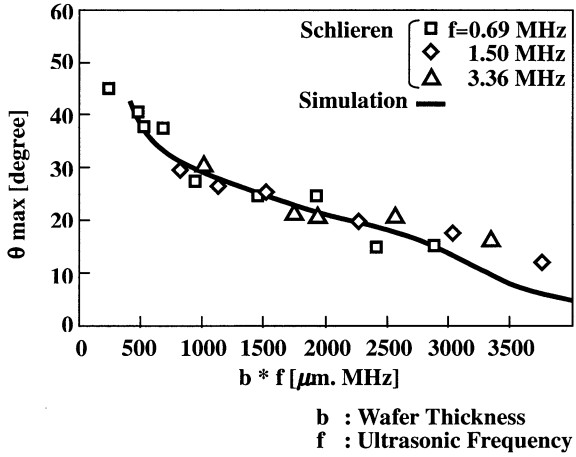
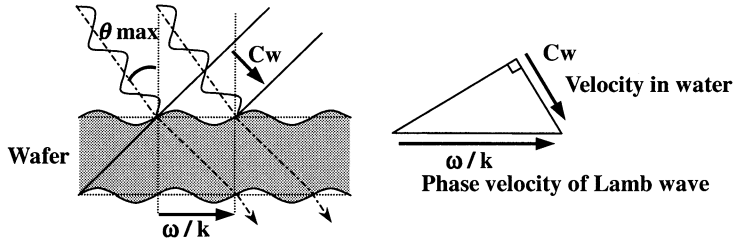


Fig. 8 The Incident Angle θ max at Maximum Transmissivity



$$(\omega / k)\sin\theta \max = Cw$$

Lamb wave motion is unsymmetric mode.

$$\therefore (Cw / \sin\theta \max)2 = (\omega / k)2 = 2b\omega Ct\sqrt{-}\{1-(Ct / Cd)2\} / 3$$

where Cd is the velocity of longitudinal wave in Si and Ct is the velocity of transverse wave in Si. Substituting these numerical value and equation;

Ct : 5843 m/sec,
Cd : 8431 m/sec,
Cw : 1483 m/sec,
$\omega = 2\pi f$,

for each item in above equation, θ max is calculated as follows.

$$\sin\theta \max = \text{arc sin}\sqrt{-}(144\ \mu m\ MHz / 2b*f)$$

Fig. 9 The Phase Agreement of Lamb Wave and Incident Wave

ATOMIC-SCALE MECHANISTIC STUDY OF IODINE/ALCOHOL PASSIVATED SI(100)

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Solutions of iodine in alcohol have been shown to passivate H_x-Si(100), decreasing the number of surface states. The degree of passivation depends upon the structure of the alcohol; methanol provides the most stable surface, with an order of magnitude fewer unpassivated sites than H_x-Si(100). Our experiments have allowed us to develop a mechanistic understanding of the reaction of the iodine/alcohol solution with the hydrogen-terminated surface. The passivation mechanism appears to be light activated iodination of the surface followed by nucleophilic substitution by the alcohol.

Our data suggests that this methoxy-terminated surface is exceptionally stable in the cleanroom ambient because the Si-O bond and the unreactive methoxy moiety hinder further reactions with contaminants. Upon annealing, we find that the passivation is readily removed, and the surface reconstructs to clean Si(100) 2x1 without the formation of silicon carbide.

INTRODUCTION

The immediate goal of this work is a chemically well-defined surface that is more stable in the cleanroom ambient than the hydrogen-terminated surface, yet cleanly and reproducibly replaced by the next solid phase. A surface passivated in this manner would eliminate the need for recleaning in between steps and provide for longer queuing times. The practice of duplicate cleaning steps, both after a process and before the next step, provides a unique opportunity for minimizing the chemical usage and water waste in a front-end-of-the-line cleaning scheme, as wafer cleaning is the most frequently repeated cycle in semiconductor processing, consuming 30% of all processing steps and 25% of all processing time.[1]

Using Radio Frequency Photoconductance Decay (RFPCD) as an *in situ* monitor of surface quality, we have demonstrated that a dilute solution of iodine in methanol provides highly effective electronic passivation[1]. The solution provides a passivation that

has an order of magnitude fewer unpassivated sites than hydrogen-terminated Si(100), as demonstrated by surface recombination lifetime measurements. Our iodine in methanol treatment is superior to the hydrogen-terminated surface in that the air stability is dramatically increased, allowing for longer queuing times and greater reliability from batch to batch. RFPCD is an extremely sensitive probe of the electronic condition of the surface but gives no chemical information about the surface species. Developing a structural description of the surface is key to elucidating a mechanism for the reaction. It is essential to understand the nature of the surface on an atomic level, if we are to minimize environmental impact, while maintaining effective surface passivation.

Our studies indicate that the passivation mechanism involves light induced iodination of the surface, followed by nucleophilic substitution by the methanol, as shown in Figure 1. Light dissociates I_2, and the resulting atomic iodine removes a hydrogen atom from the surface. The radical chain reaction is perpetuated by attack of the silicon radical on another molecule of I_2 to form the Si-I bond and another atom of I. The Si-I bond is susceptible to nucleophilic attack by the methanol, as iodide anion is an excellent leaving group. The resulting surface is methoxy-terminated.

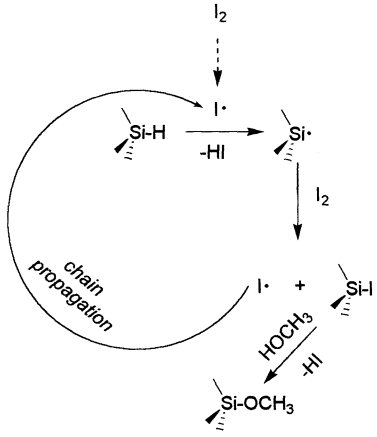

Figure 1. The passivation mechanism for H-Si treated with 5 X 10^{-4} M I_2 in methanol.

EXPERIMENTAL

Hydrogen-terminated silicon (H-Si) samples were prepared by two different methods. For the Si(111) samples, n-type Si (0.1-0.9 ohm-cm resistivity) wafers were cleaned in a 1:4, 30% H_2O_2: H_2SO_4 solution at 100°C for 10 minutes, rinsed with ultra pure water (UPW), and etched in 40% NH_4F for 15 minutes. For Si(100) samples, p-type Si (1-4 ohm-cm resistivity) wafers were etched in 1:100, 49% HF:H_2O solution for 2 minutes, rinsed with UPW, cleaned in a 1:4, 30% H_2O_2: H_2SO_4 solution at 100°C for 4 minutes, rinsed with UPW, and etched in 1:50, 49% HF:H_2O solution for 2 minutes. For the Si(100) samples, the final etching process was performed in a glovebox under a nitrogen atmosphere to eliminate the effects of molecular oxygen and water on the hydrogen-terminated surface.

The H_x-Si(100) surfaces were passivated by immersion in solutions of 5 X 10^{-4} M I_2 in alcohol for 20 minutes. The methanol solution was made with dry methanol and

sparged with argon to remove dissolved oxygen. All passivations were performed in a nitrogen atmosphere.

Iodination of the Si(111) surface was achieved on a diffusion-pumped glass vacuum line with a base pressure of 10^{-5} torr. UV exposure was performed using a broad band 365 nm light (Spectroline MB100). The iodinated surface was transferred under Ar to the analysis chamber.

Conventional X-ray photoelectron spectroscopy was performed with a Surface Science Model 150 XPS spectrometer. Peak fitting and scaling with atomic sensitivity factors were accomplished using the instrument software package.

For the synchrotron radiation photoemission measurements, the samples were introduced through a glovebox to a nitrogen purged load-lock for transfer into the analysis chamber. The analysis chamber is equipped with a cylindrical mirror analyzer (PHI) and has a base pressure of 10^{-10} torr. Analyses were performed at BL 8-1 and BL 10-1 of the Stanford Synchrotron Radiation Laboratory. The fitting procedure for the spectra is described in a previous study[2]. The monolayer coverages of surface species were determined from the photoelectron signal, accounting for exponential attenuation of the electrons from the bulk, as described by Himpsel, *et. al.*[3]

Infrared spectra were obtained with a Mattson RS-10000 Fourier-transform infrared spectrometer in the ATR geometry, and the 5 cm x 2 cm x 1 mm ATR crystals (Harrick) had 45° bevels to enable the light to enter and exit the crystal. The light exiting the crystal was collected using a liquid-nitrogen cooled narrow-band MCT detector (EG&G Judson). Spectra were obtained at 4 cm^{-1} resolution and ratioed against spectra of silicon with a chemical oxide present.

RFPCD measurements were performed with an instrument described elsewhere[4]. The lifetimes measured are inversely proportional to the number of surface states, thus the lifetimes reflect the relative degree of surface passivation.[1]

RESULTS AND DISCUSSION

Conventional XPS measurements reveal that after the iodine/methanol passivation, carbon, oxygen, and iodine are present in a 10:10:1 ratio, comprising nearly a monolayer of surface coverage. The high coverage of carbon and oxygen suggest that the passivation process is more complex than the simple iodine bonding to the silicon dangling bonds on the surface that had been previously postulated[5] because that model would show a minority species of silicon bound to iodine, as the hydrogen-terminated surface should provide few sites that require passivation.

Synchrotron photoemission studies of the Si 2p core level confirm that the passivation process is dramatically changing the bonding at the Si surface. If iodine were only to react with the few dangling bonds on the surface, the Si 2p spectra would be largely unchanged , with mostly Si-H bonds and a few Si-I bonds as previously suggested in reference 5. Yet the Si 2p spectrum in Figure 2(c) shows large amounts of silicon in the +1, +2, and +3 oxidation states, and these oxidized silicon atoms correspond to 0.8 monolayers of the surface atoms. This suggests that the passivation has surface silicon atoms with multiple bonds to methoxy groups. If iodine is not present in solution (Fig. 2(b)), the core levels remain unchanged from the hydrogen-terminated sample (Fig. 2(a)).

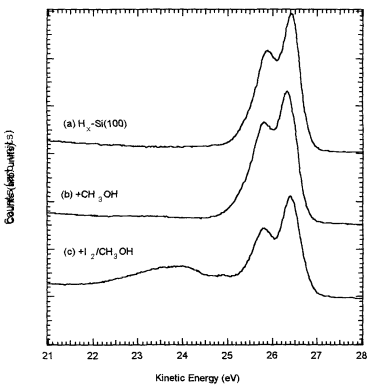

Figure 2. Si 2p photoemission spectra for Si(100) at a photon energy of 130 eV for (a) H_x-Si(100), (b) after treatment with methanol, and (c) after treatment with iodine in methanol.

It is possible to directly observe the disappearance of the hydrogen termination after the methoxy passivation by examining the IR spectra. The Si-H stretching region shown in Figure 3 indicates that if the H_x-Si(100) is immersed in methanol alone (b), the hydrogen-termination is preserved, but if the methanol solution contains iodine (c), the hydrogen-termination disappears. The initial H_x-Si(100) surface is microscopically rough, as evidenced by the mono-, di-, and tri-hydride stretches[6] in 3(a), so it is not surprising that multiple oxidation states are seen in the Si 2p spectrum (Fig. 2(c)) after reaction with I_2/methanol.

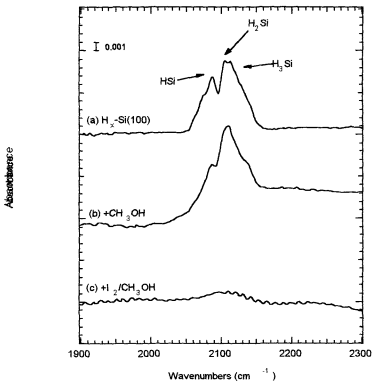

Figure 3. The Si-H stretching region of the IR spectra of Si(100) for (a) H_x-Si(100), (b) after treatment with methanol, and (c) after treatment with iodine in methanol.

If the alkoxy passivation of the surface involves the nucleophilic substitution reaction shown in Figure 1, there may be a decreased degree of reaction for more sterically hindered alcohols because bulky alcohols should be less able to displace the iodine. The IR spectra for H_x-Si(100) incubated in various iodine/alcohol solutions (Fig. 4) confirms that less sterically hindered alcohols more thoroughly remove the hydrogen termination. H_x-Si(100) treated with iodine in ethanol has more H-termination remaining than when treated with I_2/methanol, but less than with I_2/isopropanol. We have observed that bulkier alcohols result in less effective passivation of the surface.

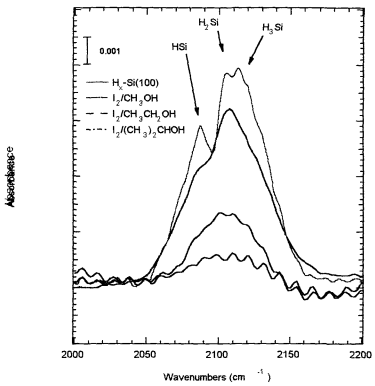

Figure 4. The IR spectra of H_x-Si(100) treated with solutions of iodine in alcohol.

Valence band photoemission at a photon energy of 55 eV reveals structure in the carbon 2s based molecular orbitals that is consistent with an alkoxy-terminated surface. The spectra shown in Figure 5 for iodine solutions of (a)methanol, (b)ethanol, and (c)isopropanol indicate that the appropriate alkyl group is present. The C 2s region of the valence band from kinetic energies of 30-38 eV contains one molecular orbital per carbon atom in the alkoxy group. The alkoxy groups appear to remain intact after bonding to the surface. This result is directly analogous to our study of alkyl adsorbates on the simpler Si(111) surface.[2]

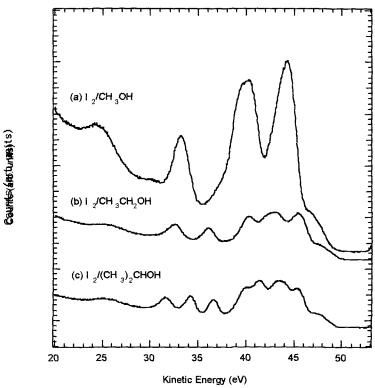

Figure 5. The valence band photoemission spectra at 55 eV photon energy for H_x-Si(100) after treatment with (a) I_2/methanol, (b) I_2/ethanol, and (c) I_2/isopropanol.

The kinetic energy of the oxygen 1s photoelectrons from a H_x-Si(100) sample after 20 minutes in I_2/methanol exhibit a chemical shift that is 0.4 eV higher than SiO_2. The oxygen in the methoxy group is chemically bonded to the electron donating Si atom and is distinct from the chemical shift of physisorbed methanol, confirming that the alkyl signal in the valence band (Fig. 5) is due to an alkoxy moiety bound to Si.[7]

Iodine is necessary to passivate the surface but is not the major species present after reaction, so it must form an activated intermediate. To begin to understand how iodine activates the Si surface, we examined gas phase reactions on the simpler H-Si(111) surface. Chlorine photodissociates and terminates this surface,[2] so iodine should behave in

a similar manner. The Si 2p photoemission spectra at 130 eV photon energy of H-Si(111) after exposure to I_2(g) for 15 minutes, both (top panel) with UV light and (bottom panel) in the dark, are shown in Figure 6. When UV light is present, the resulting surface has a 0.6 ML coverage of Si^{+1} iodine termination. Yet when the dosing is performed in the absence of light, the surface has only 0.1 ML of Si^{+1} iodine termination.[3] The gas phase reaction of iodine with H-Si(111) is clearly photoinduced. We have attempted to reproduce these experiments in methanol, but the result was ambiguous. The dark surface had the same termination as the surface prepared in room light, however this result could be due to the difficulties involved in liquid transfer in the dark.

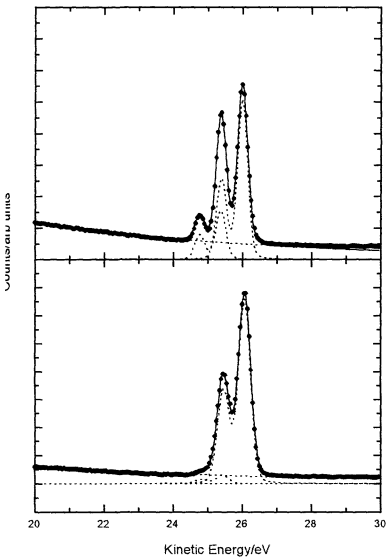

Figure 6. The Si 2p photoemission spectra at 130 eV for H-Si(111) dosed with I_2(g) for 15 minutes under UV light (top panel) and in the dark (bottom panel).

If this passivation is to be incorporated into a semiconductor fabrication scheme, it will be necessary to remove the alkoxy termination. An I_2/methanol passivated sample was annealed step-wise in vacuum in an attempt to remove the methoxy termination. The Si 2p photoemission spectra at a photon energy of 130 eV are shown in Figure 7. Annealing to 725°C results in the characteristic high kinetic energy surface peak of the clean Si(100) 2x1 reconstruction.[8] The 2x1 structure has also been confirmed by LEED.

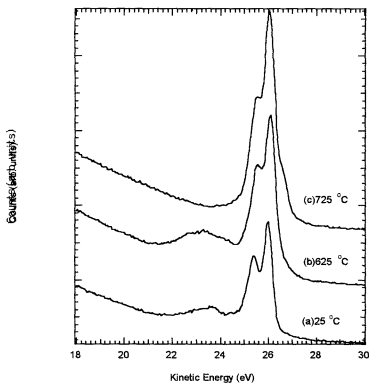

Figure 7. Si 2p photoemission spectra at a photon energy of 130 eV (a) prior to annealing, after reaching (b) 625°C, and after reaching (c) 725°C.

After reaching 675°C, the valence band annealing data for the same sample (Fig. 8) has no features in the 30-38 eV kinetic energy C 2s region of the spectra. The absence of carbon features confirms that silicon carbide is not formed during the anneal.

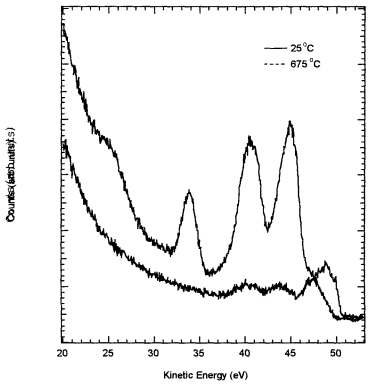

Figure 8. Valence band photoemission spectra at a photon energy of 55 eV prior to annealing and after reaching 675°C.

This annealing study was conducted under UHV conditions. Annealing the surface in the presence of an oxidizing agent, such as in a furnace, should afford even less potential for silicon carbide formation.

CONCLUSION

Dilute solutions of iodine in methanol provide an effective surface passivation. Spectroscopic evidence supports iodine-activated nucleophilic substitution as the mechanism for passivation. The resulting surface is predominantly methoxy-terminated.

Our results confirm that the passivation may be removed without silicon carbide formation by annealing in vacuum. Thus, the passivation shows potential for incorporation

into a fabrication scheme to eliminate the need for redundant cleaning steps, lengthen queuing times, and increase batch reliability. Additional experiments are necessary to determine the resistance of this surface to metal contamination and to investigate the properties of devices built on this surface.

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THE STRUCTURE AND COMPOSITION OF WET CHEMICAL OXIDES: A PHOTOEMISSION AND INFRARED STUDY

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ABSTRACT

X-ray photoemission spectroscopy (XPS) and infrared (IR) spectroscopy have been used to compare the structure and composition of chemical oxide films grown by a variety of different methods. The photoemission and infrared data show that different types of wet chemical oxides are defective and non-stoichiometric to varying degrees. Furnace oxidation in O_2 under mild conditions after wet processing causes significant changes in the structure of chemical oxides and is used as a chemical way to probe the as-grown chemical oxide structure.

INTRODUCTION

Because wet chemical processing is usually the last step before gate oxidation, the structure and composition of the wet chemical oxide affects quality of the gate oxide. Previous reports have shown that numerous types of defects such as dangling bonds (1), voids (2), sub-stoichiometric regions (2), physically trapped hydrocarbons (3), Si-H bonds (4), and OH groups (5) characterize chemical oxide films. Other studies have made correlations between the quality of the chemical oxide films and the quality of the subsequent furnace oxide films (6, 7). In the current study, we have used x-ray photoemission and infrared spectroscopy to characterize chemical oxides grown by common surface preparation recipes (viz., RCA, modified RCA (mRCA), O_3/H_2O, HNO_3, and H_2SO_4/H_2O_2). To gain additional structural information, we have examined these oxides after they were subjected to a mild furnace anneal in O_2. The O_2 annealing step causes significant changes in the quality of the as-grown oxides by reducing Si/SiO_2 interfacial roughness and/or voids, as well as sub-stoichiometric regions. By probing relative changes in the chemical oxide films, we use the O_2 annealing as a chemical way to probe the initial structure of the chemical oxides.

EXPERIMENTAL

The Si(100) samples were cut from double-side polished FZ Si(100) wafers that had been capped with a 34 Å protective oxide. Prior to growing the chemical oxides, the samples were pre-cleaned in a 1:1:4 $NH_4OH:H_2O_2:H_2O$ solution for 5 minutes at 85 ^oC to remove surface organic contamination, rinsed with de-ionized water, and immersed in a

concentrated HF solution for 60 seconds to remove the oxide. The H-terminated Si(100) samples were then exposed to five different chemical treatments, as outlined in Table 1.

Infrared spectra were recorded in transmission mode with the incident radiation at 60° relative to the surface normal. This optical geometry gives approximately equal sensitivity to vibrations that are parallel and perpendicular to the sample surface, and in particular, makes it possible monitor both the longitudinal optical (LO) mode and the transverse optical (TO) mode simultaneously. As seen below, the ability to monitor the changes in the LO and TO modes can provide important information about how the structure of the chemical oxide films changes as a function of processing. All of the IR spectra shown herein are referenced to H-terminated Si(100) samples prepared by immersing a reference sample in an SC1 solution (85 °C, 1 min) and then stripping off the oxide with concentrated HF. As a result, we do not show the Si-H stretching region, because it has strong negative excursions from the reference that mask the Si-H features of the chemical oxide films.

Table 1: Chemical Oxide Preparations

Preparation	Conditions
RCA	SC1(1:1:4 NH_4OH:H_2O_2: H_2O) at 85°C, 10 min SC2 (1:1:4 HCl:H_2O_2:H_2O) at 85°C, 10 min
Modified RCA (mRCA)	SC1(1:1:4 NH_4OH:H_2O_2: H_2O) at 85°C, 10 min Concentrated (49%) HF etch (60 s) SC2 (1:1:4 HCl:H_2O_2:H_2O) at 85°C, 10 min
Sulfuric	4:1 (H_2SO4:H_2O_2) at 85°C, 10 min
Nitric	Concentrated HNO_3 at 85°C, 10 min
O_3/H_2O	O_3 bubbled into de-ionized water, 25 °C,10 min.

The Si 2p photoemission spectra were recorded using Al Kα x-rays at 1486.6 eV to produce photoelectrons that were detected at a 45° take-off angle. The pass energy was set at 11.75 eV. In the analysis of all photoemission spectra, a Shirley background subtraction was performed prior to fitting the peaks. To quantify the amount of silicon suboxides in the chemical oxide films, the Si 2p photoemission spectra were fit with Gaussian-Lorentzian functions, assuming that the $Si2p_{3/2}$ and $Si2p_{1/2}$ components are separated by 0.61 eV and have a relative intensity ratio of 2:1. The Si^{+1}, Si^{+2}, and Si^{+3} features were taken to be shifted 1.0, 1.8, and 2.5 eV towards higher binding energy, respectively, relative to the Si^0 feature (8). The thickness of the chemical oxides was estimated roughly by using the integrated intensities of the Si^{+4} and Si^0 features according to the equation (9):

$$d_{ox} = \lambda_{ox} \sin\alpha \ln\left[1 + \frac{1}{C}\left(\frac{I^{Si^{+4}}}{I^{Si^{0}}}\right)\right]. \quad (1)$$

Here, the constant C, taken to be 0.80, represents the ratio of the photoelectron intensity of pure SiO_2 to pure Si. The take-off angle α is 45°, and λ_{ox}, the mean free path of the photoelectrons is taken to be that in SiO_2, 35 Å (10). Note that chemical oxides are

typically less dense than pure SiO_2, so that with these approximations, the calculated thickness values are systematically underestimated.

As an additional probe of the chemical oxide quality, the chemically oxidized Si(100) samples were furnace oxidized. The initial stages of the oxidation procedure involved inserting the samples into a quartz boat, placing the boat into a quartz tube furnace, and evacuating the furnace to 2×10^{-7} Torr. Next, the furnace was purged with O_2 gas at a flow rate of 1000 sccm to minimize residual water vapor. The samples were then heated to 350 °C for ten minutes (heating rate 1 °C/s) and allowed to cool to < 100 °C before they were removed from the oven.

RESULTS AND DISCUSSION

In order to present the infrared results in proper context, we begin with a short review of the interpretation of infrared spectra of thin (< 100 Å) SiO_2 films on silicon substrates. It is well known that infrared spectra of such films recorded with radiation at an oblique angle relative to the surface normal typically have two prominent phonon modes between 1000 – 1300 cm^{-1}: a transverse optical (TO) mode at ~1050 cm^{-1}, and a longitudinal optical (LO) mode at ~1250 cm^{-1}. The TO mode arises from mechanical coupling of the Si-O network, while the LO mode, though also related to Si-O vibrations, derives much of its intensity from long range coulombic coupling of Si-O oscillators (11). Obtaining structural information about the films from these two features is challenging because they are relatively broad and featureless. And although recent ab-initio calculations have added greatly to our understanding of the origins of these features (12, 13, 14), a complete detailed microscopic picture does not yet exist. However, recently Queeney et al. showed that macroscopic optical modeling using the Bruggeman Effective Medium Approximation can semi-quantitatively describe how varying certain film structure parameters, such as SiO_2 film density, interface roughness, and sub-stoichiometry, can cause changes in the appearance of the LO and TO features (15).

Three conclusions arising from the optical modeling studies (15) are pertinent for the current studies. First, the inclusion of voids in an SiO_2 matrix (to simulate a decrease in SiO_2 film density) decreases the spacing between the LO and TO modes, with a redshift of the LO mode and a blueshift of the TO mode, relative to the TO/LO pair of pure SiO_2. Second, incorporating regions of pure Si in the SiO_2 matrix (to simulate interface roughness) also decreases the spacing between the TO/LO pair, but concomitantly, a drastic attenuation in the integrated area of the LO mode is observed with an increasing fraction of Si. This phenomenon is easily attributed to the ability of the silicon regions to screen the long-range coulombic coupling that gives rise to the LO mode. Finally, adding regions of SiO (to model sub-stoichiometric regions) causes the TO/LO pair to shift *in the same direction*, towards lower frequency.

Infrared spectra of the as-grown chemical oxide films, along with the thickness of the films calculated according to Equation (1), are shown in Figure 1. An inspection of the Si-O stretching region (Figure 1a) allows the classification of the chemical oxide films into three groups based on the separation of the TO/LO modes. The first group consists of the mRCA oxide only, with TO/LO features at 1055/1180 cm^{-1} (a separation of 125 cm^{-1}).

The second group consists of the RCA oxide, HNO_3 oxide, and H_2SO_4/H_2O_2 oxide, all of which have TO/LO pairs that are approximately at 1050/1205 cm^{-1} (separated by approximately 155 cm^{-1}). Finally, the O_3/H_2O oxide, with TO/LO pair at 1047/1217 cm^{-1} (a spacing of 170 cm^{-1}) constitutes the third group. For comparison, also note that the TO/LO pair of a high quality furnace oxide, thinned to 5.2 Å by immersion in dilute (0.05%) HF, occurs at 1054/1227 cm^{-1}, a separation of 173 cm^{-1} (not shown). On the basis of this comparison, as well as the results of the macroscopic optical modeling studies (15), several qualitative statements can be made about the as-grown chemical oxide films. For example, the modeling studies clearly show that the inclusion of voids into the SiO_2 matrix (to model less dense films) or the inclusion of Si regions (to model interface

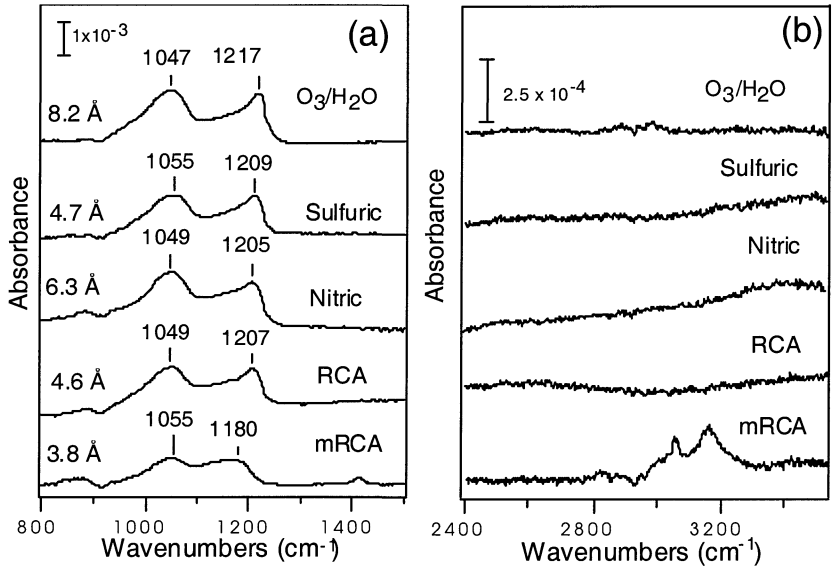

Figure 1: (a) Infrared spectra showing the LO and TO mode of the as-grown chemical oxide films. (b) Infrared spectra monitoring the C-H stretching region.

roughness) leads to a reduced separation between the TO/LO pair. Thus, an inspection of the TO/LO separations for the chemical oxide films indicates that most of the chemical oxides, with the exception of the O_3/H_2O oxide, have more voids and/or Si regions as compared to a thinned thermal oxide. It should be noted that it is not possible to quantify the relative contributions from voids and interface roughness, based on this data alone. However, it is possible to conclude that the degree of interfacial roughness is roughly similar for all of the chemical oxides, because the integrated intensities of the LO modes of all oxides are comparable. Finally, note that mRCA films are also the most hydrocarbon contaminated, as seen by the strong C-H stretching modes in Figure (1b). Previous vacuum annealing studies of mRCA films have shown that these hydrocarbons are either chemically adsorbed on the silicon oxide surface or physically trapped in the bulk of the silicon oxide film (3). Upon annealing, those hydrocarbons containing

oxygen decompose, such that the carbon, oxygen, and hydrogen are incorporated into the SiO_2 film.

After subjecting the chemical oxides to a mild O_2 oxidation, significant shifts are observed for the TO/LO modes. As seen in Figure 2a, the frequency spacing between the TO/LO modes of all oxides increases after oxidation. In particular, note that the TO modes generally are redshifted upon oxidation, while the LO modes are blueshifted (cf. Figure 3). This behavior indicates that the mild oxidation tends to improve the quality of the film by removing inhomogeneities such as voids and/or Si regions (i.e., decrease interface roughness). A notable exception to this trend is the nitric acid oxide, which has both TO and LO modes shifting towards higher frequency. As discussed above, this behavior indicates that the dominant effect in the mild oxidation of nitric acid oxide films is the removal of sub-stoichiometric regions, rather than the removal of voids or Si regions.

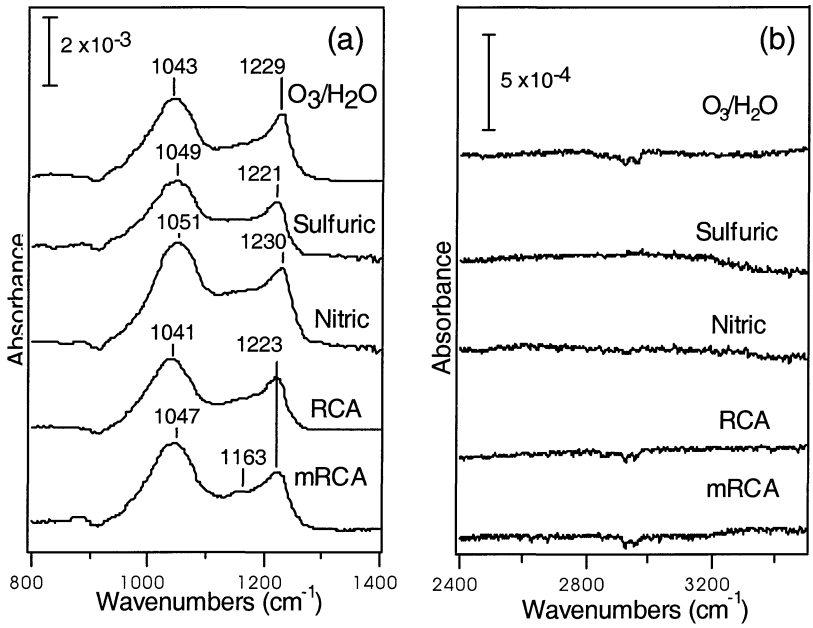

Figure 2: (a) Infrared spectra of the TO/LO modes of the chemical oxide films after a mild oxidation in O_2 (350 °C, 10 min, 1000 sccm O_2). (b) Infrared spectra of the C-H region of the oxidized chemical oxide films. Note the sharp attenuation of the C-H stretching modes of the mRCA films (cf. Figure 1b).

Despite the ability of the mild O_2 oxidation to reduce certain types of defects in the chemical oxide films, it should be noted that some defects persist in the film. This behavior is suggested by the feature at 1163 cm^{-1} in the oxidized mRCA films. Previous studies have indicated that mode intensity in this region results from the vibrational modes

of hydrogenated silicon oxides (3). It is plausible that such regions can form in mRCA oxides from the decomposition of hydrocarbons, as indicated by vacuum annealing studies, as well as by the sharp attenuation of the C-H modes of the mRCA film, as shown in Figure 2b (3). The remaining weak negative-going C-H features in Figure 2b result from variations in the degree of hydrocarbon contamination of the reference wafers.

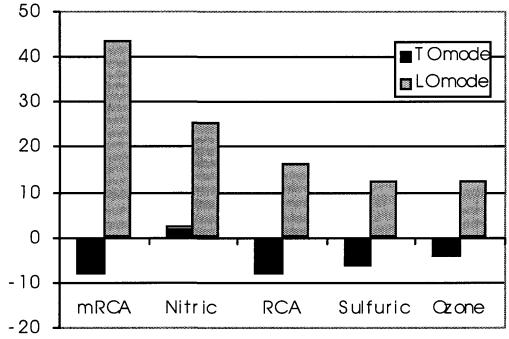

Figure 3: A summary of the direction and magnitude of the shifts experienced by the TO/LO modes following mild oxidation of the chemical oxides.

Because characterizing sub-stoichiometric oxide regions is an important issue in understanding the structure of the chemical oxides, we obtained photoemission spectra for the chemical oxide films, before and after the O_2 oxidation. These data are summarized in Table 2. The boldface numbers correspond to values for the chemical oxide films after the

Table 2: Summary of photoemission measurements of chemical oxide thickness and the amounts of sub-oxide (in percent relative to Si^{+4}). The numbers in normal type correspond to the as-grown chemical oxides, while the numbers in boldface type correspond to the O_2-oxidized chemical oxide films.

Preparation	Thickness (Å)	Oxidation State Si^{+1}	Si^{+2}	Si^{+3}	Si^{+4}
mRCA	3.8	20	10	0	100
	8.1	**10**	**2**	**7**	**100**
RCA	4.6	19	0	11	100
	7.2	**7**	**1**	**11**	**100**
H_2SO_4/H_2O_2	4.7	11	20	0	100
	6.1	**14**	**4**	**15**	**100**
HNO_3	6.3	10	0	15	100
	7.6	**5**	**3**	**7**	**100**
O_3/H_2O	8.2	10	7	7	100
	9.3	**7**	**7**	**10**	**100**

mild oxidation. Several trends can be seen from these data. First, the mild O_2 oxidation increases the thickness of the chemical oxide films to varying degrees, depending on the initial quality of the film. For example, the thickness of the mRCA oxide (the most defective as-grown oxide) increases by a factor of 2.1 after annealing, while the thickness of the O_3/H_2O oxide (the least defective as-grown oxide) only increases by a factor of 1.1. Additionally, a larger increase in thickness of the chemical oxides appears to correlate with a larger initial relative amount of Si^{+1}. In particular, while the as-grown mRCA, RCA, and H_2SO_4/H_2O_2 oxides characteristically all have about 30% sub-oxide (as judged by comparing the sum of the areas of the sub-oxide peaks to the area of the Si^{+4} peak), the mRCA and RCA oxides have a larger relative amount of Si^{+1} and experience a greater thickness increase upon mild oxidation. Although the mechanistic reason for these differences is not known at this time, one hypothesis is that large amounts of Si^{+1} corresponds to defective, low-density films that are easily oxidized. Because oxygen atoms tend to agglomerate in sub-stoichiometric silicon oxide films (16), the large number of Si^{+1} could make the oxidation reaction with O_2 extremely facile by providing oxide nucleation centers, causing the initially defective, low-density (17) silicon oxide films to become significantly denser. Such behavior would also be consistent with the infrared results described above. For the H_2SO_4/H_2O_2 oxides, which are initially dense (17) and possess smaller amounts of Si^{+1}, the oxidation reaction with O_2 is less facile, and the thickness increase is correspondingly smaller.

CONCLUSIONS

Based on these infrared and photoemission studies, it is evident that the quality of the chemical oxide films depend on the method of preparation, and that as-grown chemical oxides are more defective than thermal oxides of comparable thickness. Mild oxidation of the chemical oxide films in O_2, a process used as a chemical probe of the as-grown oxide films, causes significant changes in the structure of the oxide film by reducing the amount of film inhomogeneities such as sub-stoichiometric regions, interface roughness, and voids. By measuring the thickness increase of the films due to O_2 oxidation, the tendency of the films towards oxidation can be correlated with the initial quality of the as-grown oxide, as well as the relative sub-stoichiometry.

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USING TOF-SIMS FOR THE ANALYSIS OF METAL CONTAMINATION ON SILICON WAFERS.

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ABSTRACT

The current methods of choice for the analysis of metal contaminants on silicon wafers are Total Reflection X-Ray Fluorescence (TXRF) and SurfaceSIMS. However each of these techniques has some limitations which do not allow either of them to provide a full information set on all the potential metal contaminants of interest. TOF-SIMS (Time-of-Flight Secondary Ion Mass Spectrometry) is a survey technique with extreme surface sensitivity that has been investigated and characterized as a complementary tool to these more established techniques. Investigation of the factors affecting TOF-SIMS detection limits and an analysis of the accuracy and precision of TOF-SIMS analyses of Si wafers will be described.

INTRODUCTION

This paper will detail the development of Time-of-Flight SIMS (TOF-SIMS) as a technique to measure all common metal contaminants on a wafer, with excellent detection limits and high accuracy and precision. The current methods of choice for this measurement are TXRF and SurfaceSIMS. TXRF does not typically detect elements lighter than silicon on silicon wafers, and it has relatively poor detection limits for the heavier alkali metals. However, TXRF does have a large analytical area compared to SurfaceSIMS or TOF-SIMS, and it is also highly automated. SurfaceSIMS, a dynamic SIMS profiling technique, has high sensitivity for species such as aluminum and the alkali metals (i.e. species not detected well by TXRF), however it is not usually utilized as a survey technique, due to throughput constraints. TOF-SIMS has an advantage in that it can easily provide a survey of all common elements of interest and can analyze both blanket and patterned whole wafers. This has particular relevance in the area of CMP and post-CMP clean characterization (1), where the characterization of surface contamination between features within dies is of particular interest.

EXPERIMENTAL

The instruments used for the analyses discussed in this paper were a Charles Evans & Associates TRIFT I mass spectrometer and a Physical Electronics TRIFT II mass spectrometer (2). TOF-SIMS data are acquired by bombarding the surface of interest with a primary ion (in this case $^{69}Ga^{+}$), and measuring the intensities of the secondary ions which are produced by the $^{69}Ga^{+}$ impacts. Time-of-flight mass spectrometers are not scanning instruments like conventional magnetic sector or quadrupole mass spectrometers, so no choices must be made about which species to

monitor, since all ions formed are measured. These instruments operate in the 10^{-8} to 10^{-10}Torr range, so the sample of interest must be vacuum compatible.

Both molecular and atomic ions are formed by the Ga^+ primary ion beam, hence TOF-SIMS is an appropriate technique to use when molecular contamination is suspected, in addition to cases of elemental contamination. TOF-SIMS has previously been used extensively for the characterization of molecular contamination (3). However, the instrumental conditions used for good molecular detection do not necessarily match the conditions needed for the best elemental sensitivity. With the most intense primary ion beam current used (20nA), elemental information is obtained with high sensitivity, but at the expense of molecular information. This is because the density of primary ions impacting the sample at such currents is high enough to damage the surface and break intramolecular bonds. Under optimal conditions, the detection limit for iron can be significantly below 1E9atoms/cm^2, and is much lower for the alkali metals. However, the sensitivity of the measurement is not only instrumental dependent but is also sample dependent, as will be discussed below.

Several different analyses were carried out to investigate the factors affecting TOF-SIMS detection limits and also to investigate the accuracy and precision of TOF-SIMS analyses of Si wafers. The main approaches are detailed below:

1) A cross correlation of TOF-SIMS with established techniques, including TXRF and SurfaceSIMS was carried out. Other techniques were also used, including TOF-SIMS with a primary ion beam of $^{115}In^+$; laser SNMS (Sputtered Neutrals Mass Spectrometry) and XPS (X-Ray Photoelectron spectroscopy).

2) The short term variability of data from a standard spin coated wafer was investigated. Data were acquired on two different TOF-SIMS instruments from five specific regions on a $1cm^2$ piece of wafer, over a five day period, by seven different analysts.

3) The long term variability of TOF-SIMS data over a six month period was investigated. Data were acquired several times a week from the same piece of the same wafer as used in the short term variability study. In this case the data was acquired by two analysts using one TOF-SIMS instrument.

4) An investigation into the variation of the detection limits achievable by TOF-SIMS was carried out. This was done by analyzing 100 wafers from multiple sources within the semiconductor industry.

5) A detailed comparison of data obtained using SurfaceSIMS and TOF-SIMS was carried out on 100 different wafers. This enabled the two techniques to be correlated for a selection of different elements.

RESULTS

1) Comparison with other techniques

Table I shows the results obtained from a spin coated reference wafer using five different techniques. A wafer prepared concurrently and identically with the one used in this study had previously been analyzed by VPD/AAS (Vapor Phase Decomposition/ Atomic Absorption Spectroscopy). There are significant differences in the sampling areas and depths of the three main techniques of interest in this current study (i.e. TOF-SIMS, SurfaceSIMS and TXRF). For this data, the TOF-SIMS spectra were acquired using a raster size of 25μm; SurfaceSIMS used a raster size of 125μm and the TXRF

analytical area was $1cm^2$. In terms of sampling depth, TXRF samples the top 80-100Å of a surface; TOF-SIMS samples the top 10-20Å and SurfaceSIMS integrates through the contaminant distribution until there is no contaminant left. This depth is element dependent, but it may be up to 1000Å. It can be seen from *Table I* that the results are comparable between techniques, giving good confidence in the TOF-SIMS data. The TOF-SIMS data is typically within a factor of two of the SurfaceSIMS and TXRF data, showing good accuracy, based on data from two independent techniques, with vastly different physical characteristics.

Table I.

Experimentally Determined Surface Concentrations of Elements of Interest ($atoms/cm^2$).

	K	*Cr*	*Fe*
VPD/AAS	-	1.1E13	9.2E12
TXRF	2.1E13	2.3E13	2.1E13
SurfaceSIMS	8.0E12	9.7E12	9.9E12
TOF-SIMS (Ga)	7.9E12	1.2E13	1.5E13
TOF-SIMS (In)	1.4E13	1.4E13	1.8E13
SNMS	1.E013	2.0E13	2.0E13
XPS	-	-	6E12

2) Short Term Variability

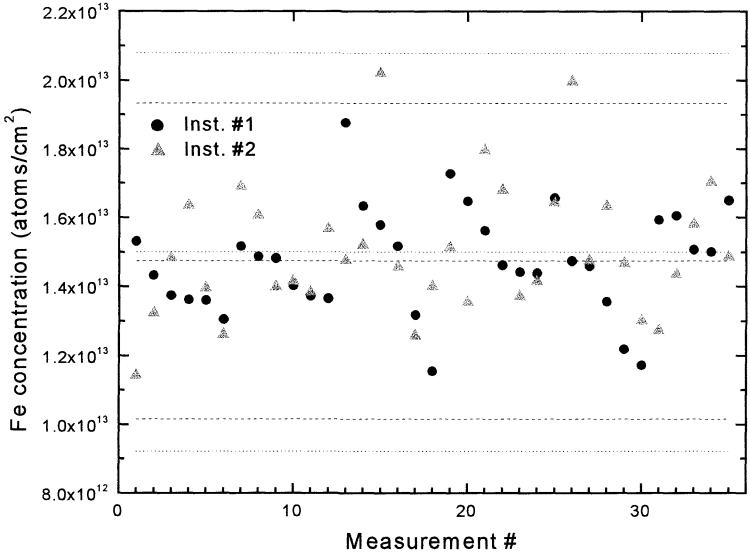
The short term variability for two different instruments is summarized in *Table II*. This data was compiled from five measurements carried out on each instrument, by seven analysts, giving 35 data points per instrument. It can be seen that the means are identical for Fe and Cr, but there is a greater spread in the data from instrument #2. Part of the variation in K is likely to be due to a heterogeneous distribution of K on the wafer compared to the transition metals. This is discussed in greater detail below. Assuming that the Fe was uniformly distributed across the wafer, this data gives a current 'best-case' for the precision of a TOF-SIMS measurement. Improvements in the precision are likely to be achievable with instrumental and protocol improvements. Figure 1 shows the distribution of Fe concentrations determined on the two instruments. It can be seen that the data from the two instruments and multiple analysts is extremely similar.

Table II.

Short term variability comparison on two TOF-SIMS instruments ($atoms/cm^2$).

Inst. #1	*K*	*Cr*	*Fe*
Mean	7.3E12	1.2E13	1.5E13
%RSD	19%	19%	10%
Inst. #2	*K*	*Cr*	*Fe*
Mean	8.6E12	1.2E13	1.5E13
%RSD	35%	23%	13%

Figure 1. Short term (one week) variation in Fe concentration, (measured on two instruments)



3) Long Term Variability

Table III shows the long term variability data for K, Cr and Fe. All data were acquired on instrument #2 of the two available. It can be seen that the %RSD increased significantly for Cr (23% to 38%) to and Fe (13% to 21%), but the increase was less significant for K (35% to 40%). This larger spread in the values determined for K is again likely to be due to a more heterogeneous distribution of K on the sample. The larger spread in concentrations for Fe and Cr compared to the short term data is currently representative of the reproducibility obtainable over a longer timescale. The long term variation in the calculated Fe concentration is shown in Figure 2.

Table III.
Long term variability (atoms/cm^2)

	K	*Cr*	*Fe*
Mean	8.4E12	1.1E13	1.4E13
%RSD	40%	38%	21%

4) Detection Limit Variation

Quantification by TOF-SIMS is ultimately dependent on the intensity of the matrix ion being monitored, since the intensity of the contaminant ion of interest is divided by the intensity of the matrix ion. The matrix ion used in these studies was ^{30}Si. It is commonly observed in TOF-SIMS analyses using high beam currents that the count rate of secondary ions drops almost exponentially with respect to time. This has dire consequences for the achievable detection limit for a given species, since it is not possible to use excessively high starting count rates due to possible detector saturation.

The initial high count rate during a TOF-SIMS data acquisition is mainly due to surface adsorbed molecular species, which are quickly removed as the static SIMS limit is exceeded. After that, the lower count rate is mainly from inorganic substrate species such as Si, SiOH and elemental contaminants. This is shown in Figure 3, which shows various hydrocarbon and substrate species with respect to acquisition time. Also shown is the Ga intensity, which increases near linearly with acquisition time.

Figure 2. Long term variation in Fe concentration (six month period)

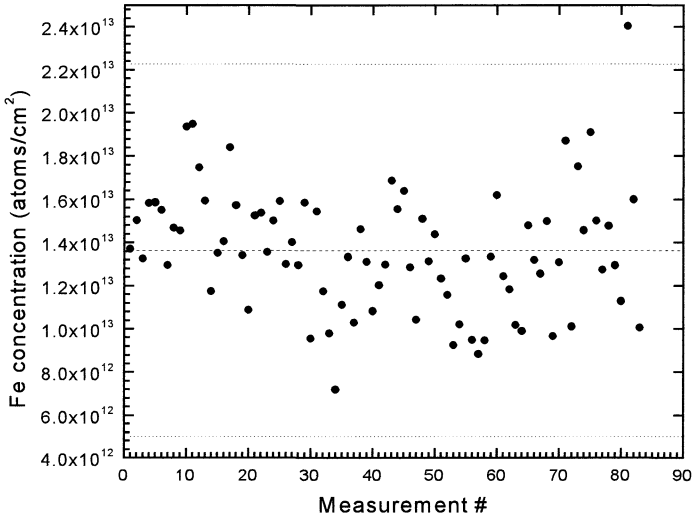
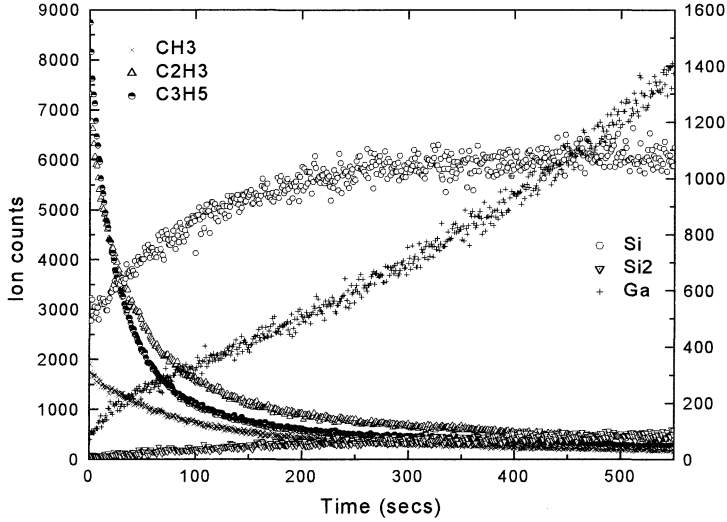


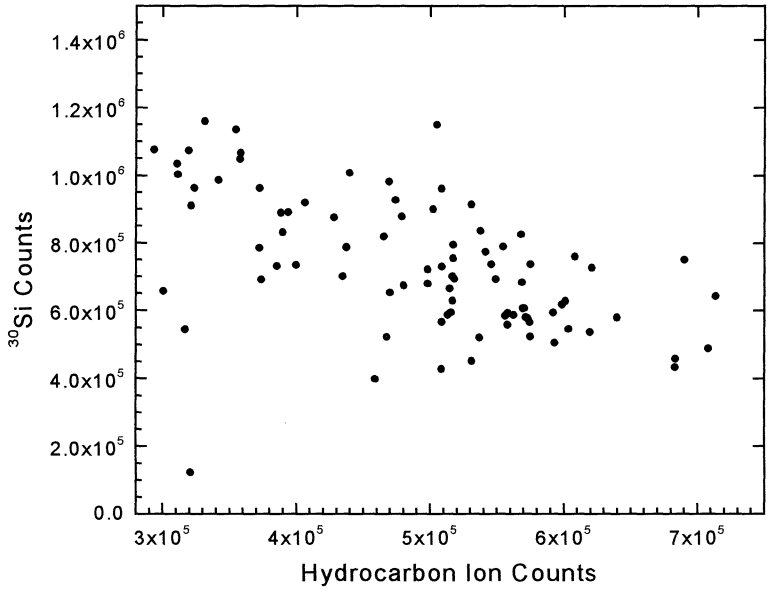
Figure 3. Dummy profiles of various species of interest



This potential severe loss in sensitivity can be avoided by introducing a pre-acquisition sputter prior to the main data acquisition step. This brief sputter serves to remove surface adsorbed hydrocarbons, enabling data to then be acquired with high sensitivity in the subsequent acquisition step.

However, not all wafers are the same, and depending on various factors such as age, surface chemistry and prior chemical exposure, the amount of hydrocarbon left, even after a pre-sputter, can vary significantly from wafer to wafer. This was investigated by analyzing 87 different wafers from various different sources, using a brief pre-sputter protocol. Figure 4 shows ^{30}Si counts plotted against hydrocarbon ion counts. It can be seen that most of the points lie on a line which shows a decrease in ^{30}Si intensity with increasing hydrocarbon intensity.

Figure 4. ^{30}Si Counts Against Hydrocarbon Intensity



The data shown in Figure 4 was then converted into a detection limit for iron, to determine the typical sensitivity of TOF-SIMS for a transition metal of interest. The mean detection limit was 5.1E8atoms/cm^2 with an RSD of 53%, using data from 87 wafers and was 4.8E8atoms/cm^2 with an RSD of 26%, with the removal of one outlying point. Iron lies in the middle of the sensitivity range of TOF-SIMS for metals, so the detection limits for mobile alkali metals are much lower, but are somewhat higher for other transition metals such as copper and zinc.

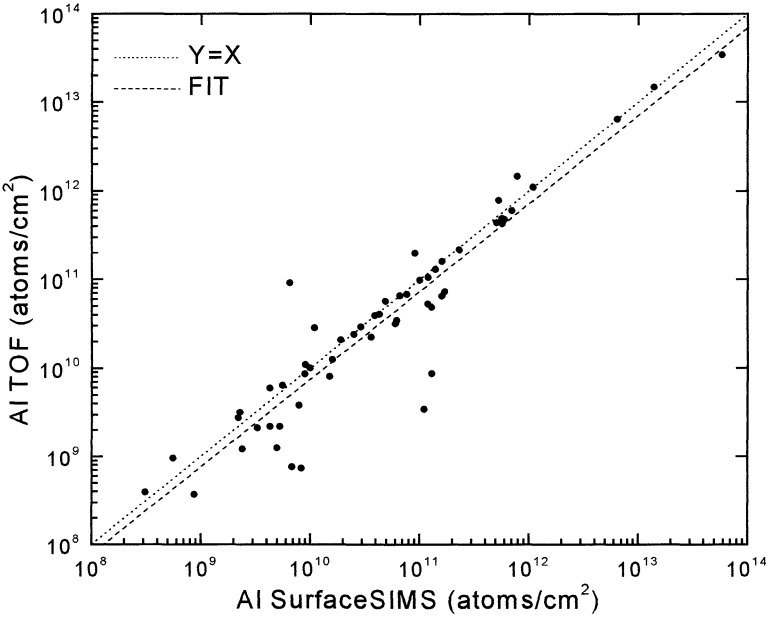
5) Comparison with SurfaceSIMS

Having investigated the variability of TOF-SIMS reproducibility over short and longer timescales, and also the factors affecting variations in detection limit, a detailed comparison of SurfaceSIMS and TOF-SIMS was carried out, using data from

approximately 100 wafers from many different sources. The surface concentrations of Na, Al, K and Ca were determined by both techniques and the results compared.

Figure 5 shows the concentration of Al as determined by TOF-SIMS compared to Al as determined by SurfaceSIMS on 56 different wafers. It can be seen that the agreement is extremely close, over almost six orders of magnitude, with a correlation coefficient of 0.9936. However, there are some data points which require explanation. In general, there is more scatter below the line than above the line, showing that TOF-SIMS determined a lower Al concentration more often than SurfaceSIMS did. This is not unsurprising, given the differences between the sampling methods of the two techniques: TOF-SIMS probes only the extreme surface for a set period of time, whereas SurfaceSIMS integrates through the contamination layer to baseline levels. This means that any significant amount of buried Al will not be detected by TOF-SIMS and hence the concentration determined will be underestimated. It is rarer for TOF-SIMS to significantly overestimate the Al concentration since there is no Al that TOF-SIMS measures that is not included in the SurfaceSIMS integration through the full contaminant layer. Data from Na, and Ca showed similar trends, with correlation coefficients of 0.8998 and 0.9734 respectively. Other elements such as K, and Cr did not correlate so well and possible reasons for this are currently under investigation.

Figure 5. Comparison Al by TOF-SIMS and SurfaceSIMS



CONCLUSIONS

The ultimate utility of TOF-SIMS is its ability to obtain a full survey of surface metal contaminants quickly and accurately. It has several other advantages, particularly

its ability to also obtain molecular contaminant information using only slightly different instrumental conditions. Its other important advantage is it's ability to analyze whole wafers (either blanket or patterned), and to thus enable information to be obtained without the destruction of the wafer. This has particular applications in the area of CMP process development, where the control of metal contamination (particularly copper and aluminum) is of vital importance. Contaminant levels can be measured between metal features within dies, separated by distances as small as 10μm. No other current surface analytical technique has such spatial resolution available with such excellent detection limits.

This paper has illustrated the investigation of TOF-SIMS as a tool for metal contamination measurement. Detection limits in the sub E9atoms/cm^2 range have been demonstrated for transition metals such as iron. Short term variability has been shown to be in the 10% range and long term variation is in the 20% range. The reduction of these values to levels approaching those attainable by SurfaceSIMS and TXRF is one of the ultimate challenges facing the development of TOF-SIMS as a complementary tool to these other established techniques.

ACKNOWLEDGMENTS

Many thanks to members of the TOF-SIMS, RBS and MALDI groups at Charles Evans and Associates who also contributed to this work.

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FUNDAMENTALS OF UPW RINSE: ANALYSIS OF CHEMICAL REMOVAL FROM FLAT AND PATTERNED WAFER SURFACES

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ABSTRACT

The interaction between theoretical and experimental approaches to semiconductor wafer rinse analysis is presented, particularly regarding the rinsing of sulfuric acid from oxide surfaces. Both unpatterned and patterned (trench) wafer rinsing are addressed, with preliminary simulation results discussed. Experimental observations indicate that immersion/mixing effects are the dominant mechanisms of sulfuric acid removal during the initial stages of rinse. Other important mechanisms to be considered, including chemical/surface interaction, are discussed in relation to experiment and theory.

INTRODUCTION

Increasing environmental and economic concerns have resulted in the need to reduce ultrapure water (UPW) consumption in semiconductor fabrication. About 2000 gallons of UPW per wafer are consumed in a typical 200 mm fabrication facility. With 300 mm technology on the horizon, this figure will certainly increase.

One of the major uses of UPW in the industry is wet chemical processing, specifically wafer rinsing. Unfortunately, "overrinsing" occurs frequently. In order to reduce water consumption, it is necessary to optimize the rinse process. A number of rinse optimization studies have been performed; however, these studies have focused primarily on full-scale processes (1-4). Knowledge of the fundamentals of rinse is required to better understand rinsing phenomena and, ultimately, to enable more effective rinse optimizations.

The focus of this research effort is multifaceted. Two experimental approaches are pursued to understand the fundamental mechanisms of chemical removal from both flat and patterned wafer surfaces. Theoretical analysis of both rinse scenarios has lead to the development of simulation code to describe and predict rinse behavior. The theoretical and experimental investigations are closely tied together, each providing insight to the other.

APPROACH

The experimental approach studying chemical removal from a flat surface involves obtaining temporal variations of the concentration of hydronium ions at specific distances from the wafer surface during rinsing. An unpatterned wafer is exposed to a wet chemistry, such as sulfuric acid, before moving it into a flow cell where it is rinsed. An ion selective microprobe system is used to measure the concentration of H^+ ions during the rinse. Ion selective microprobes have been used for biological and corrosion studies (5-7). The microprobe has a tip of 1-2 μm, which enables high spatial resolution in the measurements.

The fundamentals of process chemical removal from the patterned is explored experimentally using an in-situ conductivity device to measure the temporal and spatial variations in chemical concentration in the trench during a UPW rinse. Previous experimental techniques have relied upon measurements of the used water after rinse baths (8, 9). The aspect ratio of the experimental trench is 5.3 to 1. Figure 1 shows a cross-section of the trench device, which is held in an enclosed flow cell during experiments. Relationships between solution conductivity and ionic concentration enable the full range of rinse to be seen.

Rinse simulation code has been developed in FORTRAN to describe concentration profiles as a function of time for various rinse scenarios. Previous rinse modeling attempts have focused on incomplete pictures of chemical removal (10, 11). Suni et al. have recently performed a similar investigation with an emphasis on metal dissolution kinetics (12). This code solves a scaled form of the diffusion/convection equation utilizing a power law scheme and the alternating direction implicit (ADI) method. Various boundary conditions as are applied as appropriate.

UNPATTERNED WAFER RINSING ANALYSIS

Literature recognizes the important role that both molecular diffusion and forced convection play in wafer rinse processes (1-4, 10-12). The initial simulation developed for the rinsing of unpatterned wafers focuses on these two transport mechanisms. Using the coordinate system shown in Figure 2, the diffusion – convection equation in two dimensions is:

$$\frac{\partial c}{\partial t} + u\frac{\partial c}{\partial x} + v\frac{\partial c}{\partial y} = D_{AB}\frac{\partial^2 c}{\partial y^2} \qquad [1]$$

In this equation, diffusion along the direction of flow has been neglected, and the diffusion coefficient has been taken to be constant.

The determination of the velocity field can be determined from solving the momentum equation. Literature provides good approximations for the cases of interest in wafer rinsing. Tonti observed that the velocity profile of water flowing past a single wafer could be approximated by the boundary layer theory of flow past a flat plate (10). Rosato et al. showed that, for typical wafer spacing, flow between two wafers transitioned to fully developed laminar flow within the first 1.5 cm (11). These approximations have been utilized to provide velocity profiles for use in unpatterned wafer rinse simulations.

Figure 3 shows simulated concentration profiles for a two wafer flow configuration. The sulfuric acid carryover layer thickness was taken to be 20 microns, and of that chemical, 90 % was stripped off and dispersed through the bulk water due to initial immersion effects (13). There was no chemical interaction with the wafer surface. The average water velocity was 1.0 cm/s. The centerline between the two wafers is a line of symmetry; Figure 3 shows the profile for one of the two wafers in the configuration. As can be seen, after 120 seconds, the water has cleaned up everywhere except down the wafer near the surface, where the concentration is 0.1 – 0.4% of the initial concentration near the surface.

TRENCH RINSING ANALYSIS

Many process steps during a typical wafer flow involve cleaning patterned wafers. The rinsing of trenches has been proposed to be a diffusion controlled process that takes place on a time scale of tenths of a second (8, 14) The initial trench rinsing simulations focus on this transport mechanism. Referring to Figure 4, the removal of chemical from the trench is described by

$$\frac{\partial c}{\partial t} = D_{AB}\frac{\partial^2 c}{\partial x^2} + D_{AB}\frac{\partial^2 c}{\partial y^2} \qquad [2]$$

If there is no surface – chemical interaction at the walls of the trench, there is only variation in concentration in the y direction. Figure 5 illustrates the simulated rinsing of sulfuric acid out of a ~5:1 aspect ratio trench. Clearly, diffusive transport cleans up the trench in well under a second, in agreement with previously reported results.

SULFURIC ACID RINSE CONSIDERATIONS

The emphasis of both the experimental and modeling efforts has been on sulfuric acid chemistry, used as a model for sulfuric acid hydrogen peroxide mixtures (SPM or pirhana). While other chemistries will be investigated in future work, the researchers felt it was important to begin with a chemistry that has a reputation for being difficult to rinse. Several approaches for optimizing the post-SPM rinse have been reported in literature (15-17). Such rinse studies are typically performed on an industrial – scale

system, using bulk resistivity and surface analysis techniques as metrics of rinse progress and effectiveness. The novel experimental approaches taken here are on the microscale, which will ultimately lead to a more fundamental understanding of the SPM rinse process and better enable its optimization.

Buoyancy – Driven Flow

Important physical and chemical aspects of sulfuric acid/water interactions need to be addressed when considering this rinse process. The density of sulfuric acid at 100°C is 1.76 g/cm^3 (18), while the density of water is 0.997 to 0.972 g/cm^3 over the temperature range of 25 - 80°C, the range of typical SPM rinse temperatures (17, 19). Such density and temperature differences will result in buoyancy – driven flows that may influence the convective removal of chemical from the wafer. Also, when sulfuric acid and water come into contact, large amounts of heat are evolved due to mixing effects. This heat will elevate the solution temperature in the region of the wafer, which will further contribute to these free convective flows.

The experiments have helped to shed light on the importance of these effects. Measurements taken by the ion-selective microprobe indicate similar pH vs time curves at different distances from the wafer. Figure 6 shows typical experimental results for a 50:1 sulfuric acid process chemical. As can be seen, there is essentially no difference in the pH profiles for different distances. These results suggest that initial chemical and physical phenomena such as immersion stripping and buoyancy – driven flows play an important part in the rinse process. The experiments can be also be used to provide empirical information for use in rinse simulations.

Dissociation and Carryover

Sulfuric acid is a strong, diprotic acid, with $Ka_1 = 100$ and $Ka_2 = 0.012$ at 25 °C. A consideration of the electrochemistry of sulfuric acid/water interactions is important, especially in interpreting experimental pH measurements.

Equations 3 and 4 describe the two dissociations of sulfuric acid:

$$H_2SO_4 \xleftrightarrow{ka1} H^+ + HSO_4^- \qquad [3\text{-}4]$$
$$HSO_4^- \xleftrightarrow{ka2} H^+ + SO4^{-2}$$

The pH is also affected by dissociation of water:

$$H_2O \xrightarrow{kw} H^+ + OH^- \qquad [5]$$

Furthermore, when UPW comes into contact with air, the water quickly absorbs CO_2. The CO_2 then reacts with water to form carbonic acid, which, in turn, can undergo two dissociations:

$$\begin{aligned} CO_2(aq) + H_2O &\xleftrightarrow{ka3} H_2CO_3 \\ H_2CO_3 &\xleftrightarrow{ka4} HCO_3^- + H^+ \\ HCO_3^- &\xleftrightarrow{ka5} CO_3^{-2} + H^+ \end{aligned} \qquad [6\text{-}8]$$

Performing a mass balance on C and S and implementing conservation of charge makes it possible to determine the equilibrium concentrations of all ions involved.

One use of these dissociation calculations is in relating the final pH of a stagnant rinse bath to the initial chemical carryover. As can be seen in Figure 6, the pH for any given experiment becomes constant for long time. This figure shows that for rinsing in a static bath after 4.6 M H_2SO_4, the pH levels out at about 3.25. Figure 7 shows the pH as a function of volume of sulfuric acid. In a stagnant rinse bath, this volume is the amount carried over by the wafer. Figure 7 shows that for the example above, the volume carried over is about 25 μL. The volume carried over can be then related to the carryover thickness. Table I shows experimental calculations of carryover layer thickness for a 50 mm (2 inch) wafer. For this example, a 25 μL volume corresponds to an experimental carryover layer thickness of 9 microns.

Surface Interactions and Trench Experiments

Another important interaction to consider occurs between sulfuric acid and the silicon dioxide wafer surface. There is little in literature regarding adsorption/desorption of sulfate from the SiO_2 surface. The difficulty of the post – SPM rinse in industry, though, does suggest sulfate – SiO_2 interaction (15-17). One of the ongoing key components of this research is to take this surface interaction into account and to assess its impact on rinse effectiveness. Formulation of a relationship between the bulk fluid concentration and the surface concentration is in progress, and that relationship will then provide more realistic boundary conditions for both the unpatterned wafer and trench rinse simulations.

Experimentation will provide a means for determining the level of importance of surface interactions. The trench experiments are designed to replicate the transport conditions in a typical trench while making non-intrusive measurements. Design factors in preserving trench rinse transport include fabrication of the electrode surfaces flush with the trench sidewalls and maintaining a high oxide to electrode thickness ratio (17.5 to 1). This allows the majority of the trench sidewall area to exhibit the adsorption/desorption of ionic species to the dielectric. In addition, with a thin electrode the spatial resolution of the measurement becomes more precise. This experimental approach can be used to illuminate specific mechanisms and their relative importance in trench cleanout.

CONCLUSIONS AND FUTURE WORK

The benefit of the joint approach of experimentation and theoretical analysis is quite clear. Experimentation indicates that buoyancy-driven flows may be the predominate transport mechanisms during the initial stages of rinse, and that knowledge can be utilized in simulations to better describe the rinse process. Simulation has confirmed literature observations that for trench rinsing with no surface interactions, the cleanup time is on the order of tenths of a second. This will provide a benchmark to compare experimental data to in determining the effects of surface phenomena such as adsorption/desorption.

Using sulfuric acid as a model chemical for SPM provides information on what is regarded as one of the more difficult rinses to perform efficiently. The versatility of the simulation code will allow expansion to multiple wafer scenarios which ultimately will be able to be compared to wet tool resistivity measurements.

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Table I: Relationship between carryover volume and carryover thickness for a 2-inch oxide wafer

Volume carried over, mL	Carryover thickness, μm
0.01	4
0.025	9
0.05	19
0.1	37
0.3	111
0.4	148

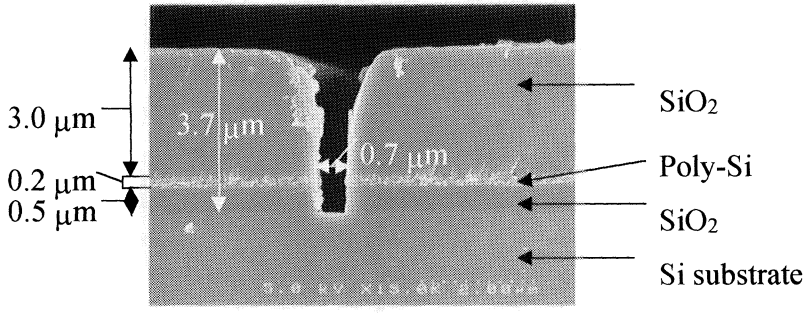

Figure 1: SEM photomicrograph of vertical slice through trench. Roughness and poly-Si fracturing are due to sample preparation.

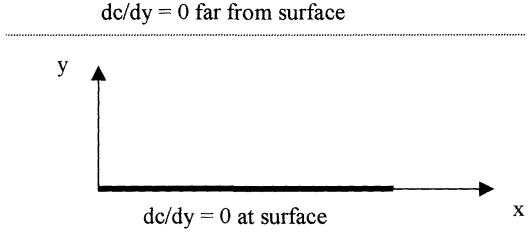

Figure 2: Coordinate system for unpatterned wafer rinsing.

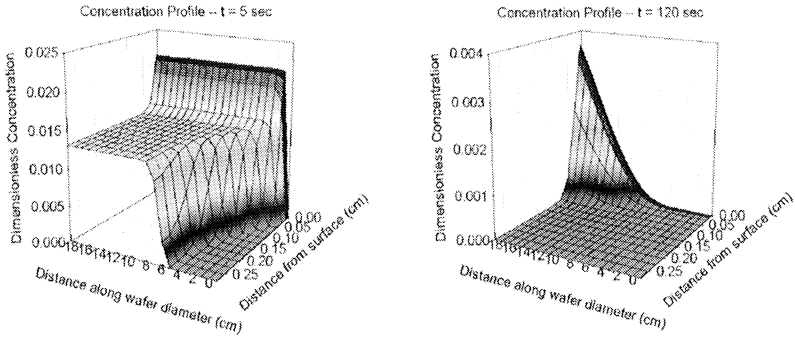

Figure 3: Two wafer rinse profile, sulfuric acid carryover layer, no surface interaction; wafer to centerline shown for 20 cm wafer

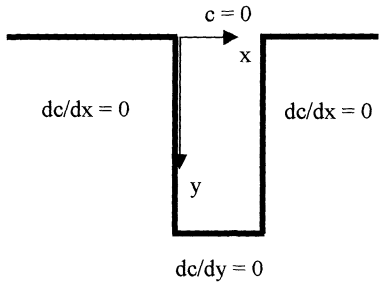

Figure 4: Coordinate system for trench rinsing.

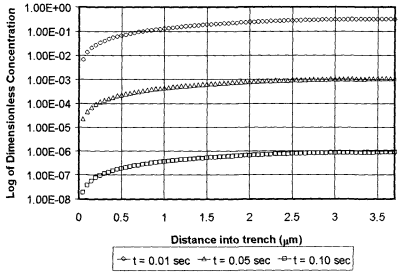

Figure 5: Concentration vs distance into trench; rinsing of 3.7 μm by 0.7 μm trench

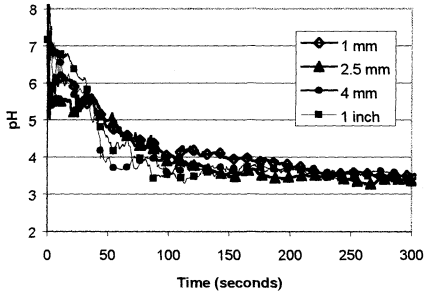

Figure 6: Stagnant rinsing of flat oxide wafer after 4.6 M sulfuric acid, pH vs time

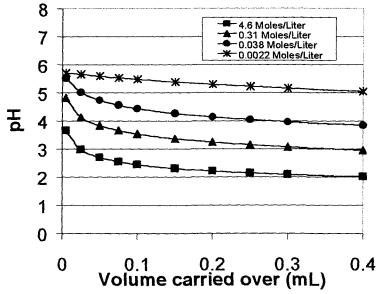

Figure 7: Relating pH to chemical carryover; pH vs volume of H_2SO_4

IN-SITU ANALYSIS OF WAFER SURFACE AND DEEP TRENCH RINSE

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ABSTRACT

A major concern in the semiconductor industry has been the significant environmental and economic impacts of ultra-pure water (UPW) use. Wafer rinse baths contribute to more than half a fabrication facility's UPW use. The objective of this work is to determine mechanisms by which UPW usage in rinse processes can be reduced without sacrificing overall wafer cleanliness. Specifically, the fundamentals of process chemical removal from the patterned surface during UPW rinse are studied. This has been explored through in-situ experiments measuring the temporal and spatial variation of contaminant removal using an ion-selective microprobe and a simulated rinse of a sub-micron wide trench.

INTRODUCTION

There are increased environmental and economic concerns in the semiconductor industry due to ultrapure water (UPW) usage. The manufacture of microchips today requires over 200 processing steps (1) of which wafer cleans comprise approximately one third of the steps. It is estimated that about 70 million liters a month of UPW per chip manufacturing plant (fab) are used both for front-end-of-line (FEOL) and back-end-of-line (BEOL) rinse processes. Surface contamination by metals, organics, particles, or by

chemical residue from the previous step can affect device yield. Consequently, it is desired to rinse the wafer to the point of cleanliness without "overrinsing" and wasting water.

Various investigations have attempted to improve these rinses. These optimized rinses can achieve better device performance, shorter cycle times, higher tool utilization and throughput, and reduce the amount of water used (2-9). Water use reduction studies typically employ process tank, in-situ resistivity probes to monitor the ionic concentration in the rinse tank water. Resistivity probes, however, reveal the concentrations in the bulk of the rinse water, not the wafer surface contamination or device cleanliness. It is desired to more exactly determine when the wafer reaches cleanliness, and to achieve this, it is essential to measure the contaminants close to the wafer surface and in the trenches while the wafer is being rinsed.

To understand the rinse process, it is needed to measure the temporal variation of the concentration of acid in UPW as a function of distance from the wafer. An ion selective microprobe, which has been previously used in biological systems (10-14), is used to measure H+ ions close to the wafer surface in the rinse process. This microprobe has a spatial resolution of about 2 microns and a response time in the order of a few milliseconds.

The second method involves measuring the contaminant concentration in the water trapped within the structure of the wafer while the structure is being rinsed. Limited work has been done on rinsing high aspect features like vias and trenches. The few investigations focused on the dominating effect of diffusion over fluid velocity in trenches (15-17). It has been estimated that the bottom of a typical DRAM trench (4 μm x 0.5 μm x 0.5 μm) decreases in concentration by seven orders of magnitude in a 10^{th} of a second (15). Previous experimental work has measured the contaminants in the trench after the processing steps (17,22), but no real-time measurements have been reported. The device used in this project provides in situ measurements during the rinse of a trench.

METHOD OF APPROACH

Trench Device

For the rapidly changing concentration and temperature in a trench during rinse an accepted and robust measurement technology is required. Although not typically utilized on the micro-scale, resistivity measurement is the semiconductor industry standard for measuring aqueous ionic concentrations. The resistivity is easily calculated from the measured resistance and the cell constant (the electrode separation distance divided by the electrode facial area), Equation 1. Empirical data of the resistivity-concentration relationship is readily available for most semiconductor aqueous chemistries. Additionally, at lower concentrations the resistivity of an ionic solution is well described by the infinite dilution approximation from Kohlrausch's Law, Equation 2. H^+ and X^- are the dissociated ions of imaginary monoprotic acid HX.

$$R = \frac{\rho \, l}{A} \quad [1]$$

$$\rho = \frac{1}{\lambda_H \cdot [H^+] + \lambda_{OH} \cdot [OH^-] + \lambda_X \cdot [X^-]} \quad [2]$$

λ = limiting ionic conductivity (cm^2 x S/mol)
R = Resistance (Ω)
$[X^-]$ = molarity of ion X^- (mol/l)
A = Electrode area (cm^2)
ρ = resistivity (Ω/cm^2)
l = length (cm)

The experimental device is a 6.39 x 9.7 die with 5 circuits each featuring a deep trench (3.7 x 0.7 μm). Each trench has a conductive band exposed 0.5 μm from the bottom of the trench. Figure 1 is an SEM photomicrograph of the device trench.

An AC signal frequency range between 10 and 100 kHz was employed to avoid migration of ions from one trench electrode to the other. Diffusional transport out of the trench should be relatively unimpeded by the alternating current.

Highly doped (10^{19} cm^{-3}) n-type polycrystalline silicon (poly-Si) was chosen as the electrode material for its corrosion/etch resistance to most wafer clean wet chemistries. The poly-Si circuit was designed with considerable width (mostly >= 500 μm) to minimize the line resistance ($\approx 10^4$ Ω). Contact pads are also poly-Si with a minimal contact resistance in comparison to the line resistance. The dielectric is TEOS oxide.

Analysis of the complex impedance enables determination of the solution resistivity. The primary circuit features are shown in Table I. The trench parasitic capacitance is primarily the charge storage between the poly-Si and the Si substrate. The equivalent circuit diagram is presented in Figure 2.

The device complex impedance follows the general formula for a parallel resistor and capacitor, Equation 3. Equation 4 is the complex impedance specific to the device.

$$|Z| = \frac{R}{\sqrt{1+\omega^2 C^2 R^2}} \quad [3]$$

$$|Z| = \frac{R_1 + \frac{2R_2}{\sqrt{1+\omega^2 C_2^2 R_2^2}} + \frac{R_3}{\sqrt{1+\omega^2 C_3^2 R_3^2}}}{\sqrt{1+\omega^2 C_1^2 \left(R_1 + \frac{2R_2}{\sqrt{1+\omega^2 C_2^2 R_2^2}} + \frac{R_3}{\sqrt{1+\omega^2 C_3^2 R_3^2}} \right)^2}} \quad [4]$$

|Z| = Complex Impedance (Ω)
ω = frequency (rad)
C = Capacitance (F)

The resistivity of acid solutions can span more than six orders of magnitude from concentrated processing solution ($\approx 10^5$ μS/cm) to UPW (0.052 μS/cm). The solution resistance of the trench should be at least on par with the poly-Si circuit line resistance. Thus, a minimum solution resistance of 10^4 Ω is required. Cell constants > 100 cm^{-1} meet this need. The device is equipped with electrode lengths of 100, 50, 20, 10 and 5 μm producing cell constants of 700, 1400, 3500, 7000, and 14,000 cm^{-1}, respectively.

Ion Selective Microprobe

After the oxide wafer was dipped into sulfuric acid and subsequently rinsed in a cell, the H+ ions were measured by an ion selective microprobe during the rinse. This ion selective electrode is made up of a galvanic half-cell that contains a liquid membrane, an internal filling solution, and an internal reference electrode. The other half-cell is an external reference electrode in contact with a reference electrolyte. When the ion selective electrode and the external reference electrode are both in contact with the sample solution, a cell potential (electromotive force (EMF)) is established across the membrane. The ion to be measured is selectively transferred from the sample solution to the liquid membrane, and this potential difference is generated between the internal filling solution and the sample solution.

The ion selective microprobe follows Nernstian behavior, which has a potential determined by the following equations:

$$EMF = E_o + s\log[a] \qquad [5]$$

$$s = \frac{2.303(RT)}{zF} \qquad [6]$$

EMF: electromotive force [mV]
E_o: reference potential [mV]
s: Nernstian slope
a: ion activity [mole/liter]
R: gas constant (8.314 J K^{-1} mol^{-1})
T: absolute temperature [K]
z: charge of the ion
F: Faraday equivalent (9.6487×10^4 C mol^{-1})

The relationship between the voltages and concentrations are determined by measuring the potential of the probe while placing it in calibration solutions of known concentration.

Microelectrode Fabrication. Glass micropipettes were made from borosilicate glass capillaries without a filament using a P-97 Flaming/Brown micropipette puller. The resulting tip diameter of the micropipettes was in the range of 1.5 - 2 μm. The glass micropipettes were then heated in an oven and silanized at 250°C. After silanization, the micropipettes were back-filled with electrolyte and then the tip was front-filled with a hydrogen-selective ion exchange resin. The probe was then mounted to a Ag/AgCl wire that served as the internal reference electrode. The external reference electrode was obtained through World Precision Instruments (SDR-2). The electrodes were connected

to a preamplifier that was subsequently connected to an amplifier to obtain the potential measurements. The electrodes were calibrated for the responses with pH standard buffer solutions (pH 4 and 7). For details on microelectrode fabrication, silanization methods, and theoretical background, see (19).

Measurement Procedure. A 2-inch oxidized wafer was dipped into sulfuric acid of different concentrations. The wafer was then transferred to a rinsing cell with stagnant or flowing water. While the wafer was being rinsed, the ion selective microprobe was measuring the H^+ ions at a specific distance away from the wafer.

RESULTS AND DISCUSSION

Trench Device

To measure impedances from 10^4 to 10^8 Ω and record on the order of milliseconds an HP 4294A precision impedance analyzer with an HP 42941A probe adapter was used. The capacitance to ground was found to dominate. At the parasitic capacitance measured (88 pF), the equivalent circuit calculation predicts no discernable impedance variation between highest and lowest trench resistances. The full ionic concentration range was not experimentally resolvable in comparison to electronic noise. Increasing the electrode area by approximately 265X through wet etching of SiO_2 with buffered HF mostly eliminated the parasitic capacitance in the higher ionic concentrations and lower frequencies (10-50 kHz). Figure 3 presents the resistance resolution of the decreased cell constant device in KCl solution.

Despite poly-Si favorable chemical resistivity, metals and metal silicides are being investigated to further lower the circuit line and electrode surface resistances. This will allow much thinner circuit lines. This combined with a thicker base oxide and more intrinsic Si substrate will produce less influential parasitic capacitance.

Ion Selective Microprobe

Figure 4 shows typical experimental results obtained from the microprobe. After the oxide wafer was dipped into 4.6 M H_2SO_4, it was placed in a static cell to rinse while the microprobe measured H^+ ions at a specific distance from the wafer. Figure 4 shows that there is a quick drop in the pH after a few seconds of rinsing. It also shows that the pH levels out for the various distances from the probe at essentially the same time (~200 sec.). If molecular diffusion were the only force driving the chemical off of the surface ($t = l^2/D$), it would take about 17 minutes to notice a change in H^+ concentration if the probe were 1000 microns from the surface. The change happens much quicker and at relatively the same time for all positions. This indicates that there are other forces occurring when the wafer is being rinsed. There are buoyancy effects from dipping the wafer into the cell, aside from convective forces caused by heats of mixing and density differences between the sulfuric acid and the water. The same phenomenon is observed

while rinsing in a flowing cell. There are no measurable differences in concentration profiles at various distances away from the wafer surface.

Figure 5 shows the concentration profile of a wafer pre-dipped into 4.6 M H_2SO_4 and rinsed in a cell with water flowing at different flow rates. At higher flow rates, the wafer was cleaned faster. Typical water velocities in a wetbench are about 0.8 cm/s, which corresponds to a flow rate of 1.6 liters/min in our flow cell. At this flow rate, the concentration leveled out at approximately 1 minute. To investigate residence time the equation of a continuously stirred tank reactor (CSTR) is considered.

$$C_a = C_{ao} \exp^{-t/\tau} \qquad [7]$$

C_a: Concentration of the acid
C_{ao}: Initial concentration of the acid
t: Time
τ: Residence time

Table II shows the differences in residence times between the theoretical values of τ, obtained by dividing the volume of the cell by the flow rate, and the fitted values of τ from the concentration curves. Figure 5 also shows the experimental data and fitted data, which is the smooth line. The differences in the residence times may be due to eddies in the flow cell used that prevent the water from coming out quickly.

CONCLUSIONS

Despite the difficulties encountered, a trench resistivity device still holds promise in resolving the process chemical evolution out of a sub-micron trench. Decrease of parasitic capacitance and use of well understood electrode materials will be incorporated in the development of a second generation device. The ion selective microelectrode has proved to be useful in measuring concentrations of H^+ while the wafer is rinsing in stagnant and flow conditions. It can be deduced from the microprobe data that the initial rinsing mechanisms are convective rather than diffusive, due to density differences in the chemicals, heats of mixing, and buoyancy effects from immersion of the wafer into the water.

ACKNOWLEDGEMENTS

This work is supported by the National Science Foundation and the Semiconductor Research Corporation through the Center for Environmentally Benign Semiconductor Manufacturing. The assistance Michael Schabel, Bert Vermiere, and Sarah Dahl of the University of Arizona and Francisco Machuca of Stanford University has been greatly appreciated. The invaluable help of Eric Karplus of Science Wares is also appreciated.

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Table I: Circuit element evaluations

Symbol	Description	Evaluation
R_1	Poly-Si circuit line resistance	Measured
R_2	Electrode-electrolyte interface resistance	$R = V/(10^{-13} * A\ (\mu m^2))$ *
R_3	Trench solution resistance	$R = \rho\ (l/A)$
C_1	Trench circumventing capacitance	Measured
C_2	Double layer capacitance	$C = 10^{-13} * A\ (\mu m^2)$ **
C_3	Trench gap capacitance	$C = k\varepsilon_0 A / l$ ***

* 10^{-13} A/μm^2 current density for n-type silicon (19)

** 10^{-13} F/μm^2 common double layer capacitance (20)

*** k = 80 for water (21) - varies less than order of magnitude under operational frequencies, aqueous concentrations, and temperatures - $\varepsilon_0 = 8.85 * 10^{-18}$ F/μm

Table II: Comparison of Experimental and Fitted Residence Times

Flowrate, liters/min	Theoretical τ, sec.	Fitted τ, sec.
0.5	29	66
1.0	13	29
1.6	10	22

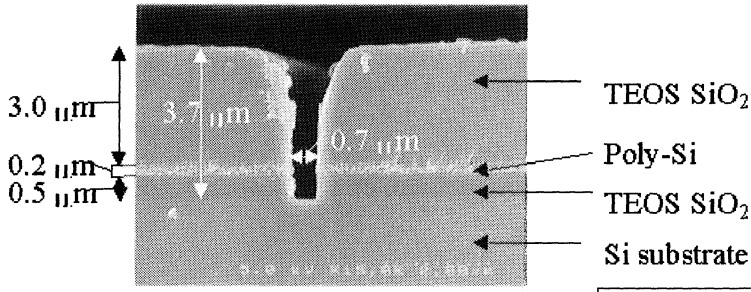

Figure 1: Trench device cross section

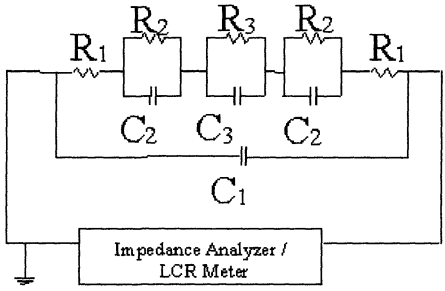

Figure 2: Equivalent Circuit Diagram

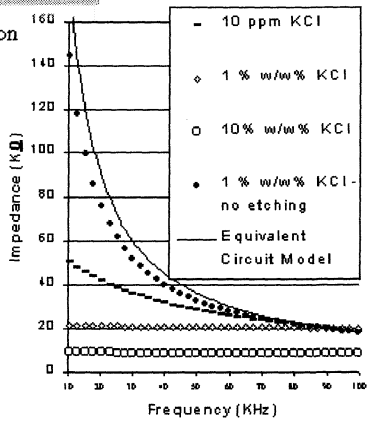

Figure 3: Impedance Profile

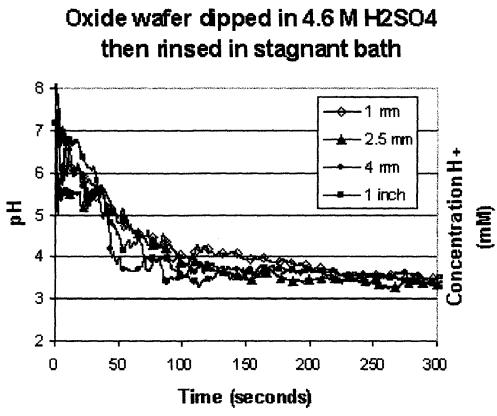

Figure 4: Concentration Profile Obtained with H^+ Microelectrode in Stagnant Conditions

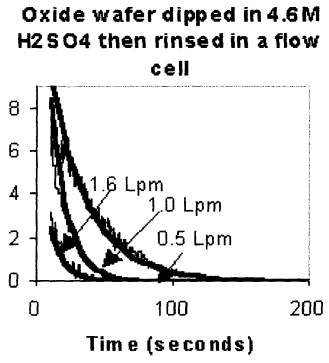

Figure 5: Concentration Profile Obtained with H^+ Microelectrode at Flow Conditions

MECHANISM OF METAL HYDROXIDE ADSORPTION ONTO Si SURFACES IN ALKALI SOLUTIONS AND ITS PREVENTION

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It is found that metallic impurities such as Al, Fe and Zn are more likely to adhere onto SiO_2 surfaces than bare Si surfaces in both neutral and alkali solutions. Speculating that "mechanism of metal adhesion in alkali solution is caused by the dehydration reaction between OH-terminated Si surface and OH bound with metals", authors tried quantum chemical calculation of potential energy change during the reaction, and found that calculated results were in good agreement with experimental results and adhesion models. Use of chelate-added alkali cleaning solution significantly reduces metal adhesion from cleaning solution. This will lead to improvement of Si surface cleanliness and cost reduction.

INTRODUCTION

The existing wet process faces the following four problems: i) too many cleaning process steps, ii) too much chemical and ultrapure water consumption, iii) too large tool footprint and iv) hard to improve wafer surface cleanliness due to re-adhesion of impurities. These problems become increasingly visible in addressing devise integration, introduction of 300mm wafer, reduction of device manufacturing costs and compliance with environmental requirements (ISO14001). It is strongly required to develop a new cleaning technology in order to overcome these problems.

Table I summarizes target contaminants and adverse effects of major cleaning solutions which are currently used in the wet process of semiconductor production line. Target contaminants to be removed by each cleaning solution are limited, and one of the adverse effects in the wet process is re-adhesion of contaminants. Some contaminants re-adhere onto wafer surface from cleaning solution in cleaning step, which is designed to remove other type of contaminants. Each cleaning step has its own adverse effects. With the conventional wet process technology, the multi-step cleaning process is the only available solution to this re-adhesion problem. To suppress re-adhesion of contaminants as much as possible, chemicals need to be replaced frequently in the current wet process. Consequently the conventional wet process faces the four problems mentioned above.

Table I. Typical wet cleaning sequence currently used and its problems.

Cleaning Solutions	Target Contaminants	Adverse Effects (Contamination)
H_2SO_4/H_2O_2 (SPM)	Organic (Photoresist), Metals	Particles, Sulfate
HF/H_2O (DHF)	Metals (in oxide)	Noble Metals, Particles
$NH_4OH/H_2O_2/H_2O$ (APM)	Particles, Organic	Metals
$HCl/H_2O_2/H_2O$ (HPM)	Metals (on surface)	Particles, Chlorine
HF/H_2O (DHF)	Oxide, Metals (in oxide)	Noble Metals, Particles

In an attempt to establish an advanced wet cleaning technology free from adverse effects, authors have been studying the mechanisms of contaminant adhesion in solutions and the methodology to prevent the contaminant adhesion (1-4). This paper reports the mechanism of metal adhesion from alkali solutions and the measures to prevent metal re-adhesion.

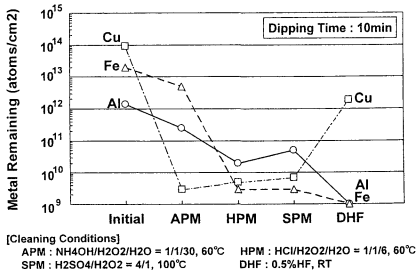


Figure 1. Removal of metallic contamination with various cleaning solutions. Initial contamination was deposited from APM with metals.

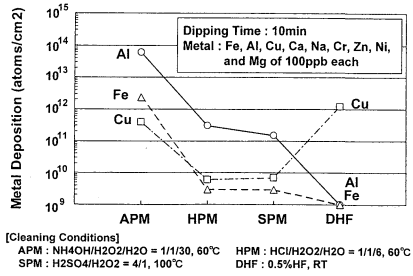


Figure 2. Metal adhesion onto Si surfaces from various cleaning solutions containing metallic impurities.

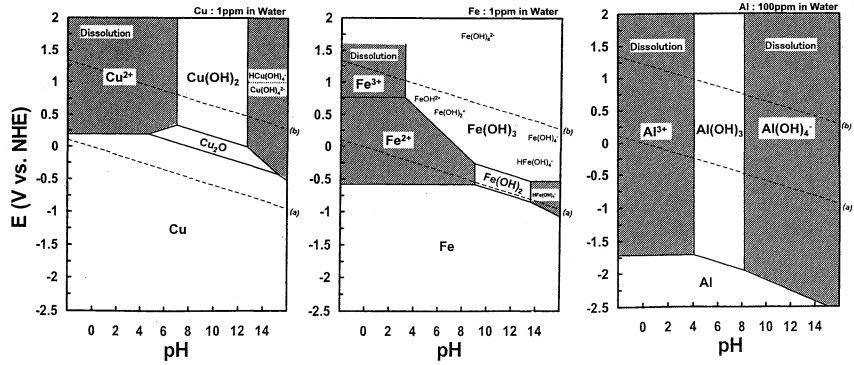
MECHANISM OF METAL ADHESION FROM SOLUTIONS

Metallic Contamination in Semiconductor Wet Processes

Figure 1 shows residual metals on Si wafers which are contaminated with metallic impurities and treated with various cleaning solutions (semiconductor grade high-purity chemicals and ultrapure water are used). APM cleaning can not effectively remove Al or Fe, and DHF cleaning hardly removes Cu. Figure 2 shows the amount of metal adhesion onto Si surfaces from solutions containing metals (100 ppb). Figures 1 and 2, when compared each other, indicate very similar trends, which suggests that prevention of metallic impurity adhesion in solution should be one of the important factors to impurity removal efficiency.

The critical types of metallic contamination in semiconductor wet processing are: i) noble metal (Cu, Ag, etc.) adhesion onto bare Si in solutions such as HF solutions and ii) metal adhesion in alkali solutions such as APM solution. It has already been found that noble metal adhesion in HF occurs as a result of electrochemical (oxidation-reduction) reaction between noble metal ions and bare Si (1-3). On the other hand, adhesion of metals such as Fe, Al and Zn in alkali solutions has been thought to occur as a result of metal hydroxide precipitation (3,5).

State of metals in solution (atom, ion, hydroxide, oxide etc.) strongly depends on redox potential and pH of solution. For three typical metals, Figure 3 shows potential-pH diagrams which authors have calculated by using equilibrium constant (6).



(a) Cu-H_2O system (Cu 1ppm) (b) Fe-H_2O system (Fe 1ppm) (c) Al-H_2O system (Al 100ppm)

Figure 3. Potential-pH diagrams for three typical metals (at 25℃).

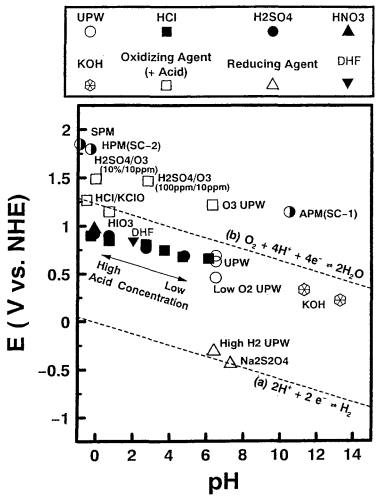


Figure 4. The pH level and redox potential (E) of various solutions (E of SPM, HPM and APM are calculated. Others are measured).

Figure 4 shows pH and redox potential (measured and calculated) of various solutions. Cu is picked up as an example for more detailed explanation here. As pH is higher than 7, Cu^{2+} concentration in solution exceeds solubility to be precipitated in a form of $Cu(OH)_2$. To form metal hydroxide in alkali solution is a common characteristic among a number of heavy metals. APM solution features pH of 10 to 11. According to the conventional interpretation, metals form non-ionic metal hydroxides in this pH region, which eventually adhere onto Si surface (3,5). This interpretation, however, can not explain the entire phenomenon. In alkali solutions of pH10-11 (same as APM), almost all Cu and Fe exist in a form of insoluble $Cu(OH)_2$ and $Fe(OH)_3$, respectively. However, Al forms the soluble $Al(OH)_4^-$. Therefore, a simple explanation such as "insoluble metal hydroxides formed in alkali solution adhere onto the substrates" can not explain the adhesion phenomenon of Al. In fact, Al most easily adheres to Si substrate in alkali solutions such as APM.

Mechanism of Metal Adhesion in Alkali Solutions

The authors considered that some chemical reaction between Si surfaces and metals induces metal adhesion in alkali solutions, and investigated the influence of Si surface conditions on metal adhesion. Figure 5 indicates that Fe, Al and Zn are more likely to adhere onto SiO_2 surfaces than bare Si surfaces in both neutral and alkali solutions. This tendency is obvious in the case of Al adhesion. (The reason why Cu adhesion is greater in the case of bare Si is that Cu adheres to bare Si by another adhesion mechanism: i.e. electrochemical adsorption. However, Cu adhesion to oxide surface is significantly more in alkali solution of pH 10.5 than in pure water. Cu forms $Cu(OH)_2$ in this alkali solution.)

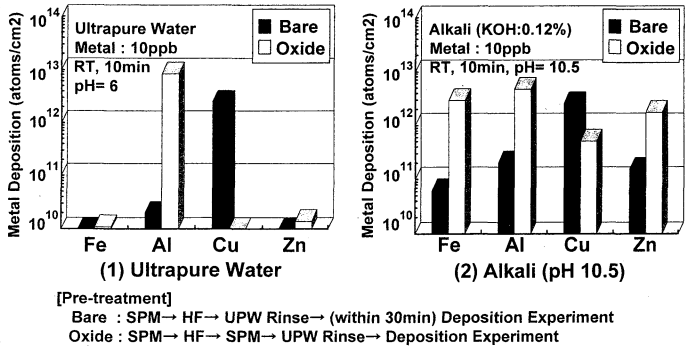


Figure 5. Influence of Si surface conditions (bare or chemical oxide) on metal adhesion from ultrapure water and alkali solution with metals (Fe, Al, Cu, Ca, Na, Cr, Zn, Ni and Mg of 10 ppb each are added).

Oxide surfaces are covered with OH-termination (Si-OH) in the solution, while HF pretreated bare Si surfaces are covered with H-termination (Si-H). Figure 5 suggests that OH-termination of Si surface should have a lot to do with adhesion of metal hydroxides.

We have speculated that "metal adhesion in alkali solution is caused by the dehydration reaction between OH-termination of Si and OH bound with metals (equation [1])", and calculated the potential energy change during adsorption reaction by using quantum chemical calculation (with density functional theory).

$$Al(OH)_4^- + HO\text{-}Si\ surface \rightarrow [Al(OH)_3\text{-}O]^-\text{-}Si\ surface + H_2O \qquad [1]$$

Figure 6 shows change of atomic configurations and potential energies when $Al(OH)_4^-$ adheres onto OH-terminated Si surface (Si-OH group). For comparison, Figure 7 shows change of atomic configurations and potential energies when $Al(OH)_4^-$ adheres onto H-terminated Si surface (Si-H group). As shown in Figure 6, when $Al(OH)_4^-$ adheres to OH-terminated Si surface, first adsorption state is energetically very stable and activation energy of adhesion reaction is low enough to be passed at room temperatures. Moreover, from the viewpoint of chemical equilibrium, $Al(OH)_4^-$ adhesion to OH-terminated Si surface is stable as potential energy after adhesion is lower than that before adhesion. On the other hand, $Al(OH)_4^-$ adhesion to H-terminated Si surface requires high activation energy. Also in this adhesion, potential energy is higher after adhesion reaction than before, which suggests unstability of the adhesion state. These calculation results clearly indicate that metal hydroxides are more likely to adhere to OH-terminated surface than to H-terminated surface. They are in good agreement with experimental results shown in Figure 5 and an adhesion model shown in equation [1].

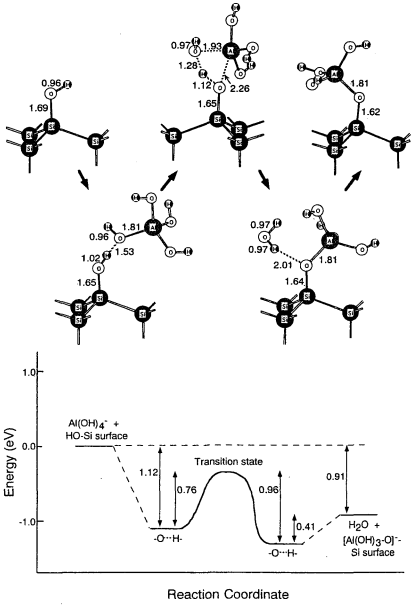


Figure 6. Change of atomic configurations and potential energies when $Al(OH)_4^-$ adheres onto OH-terminated Si surface (Si-OH group).

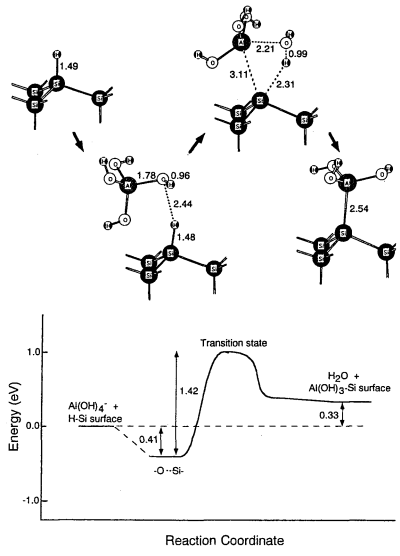


Figure 7. Change of atomic configurations and potential energies when $Al(OH)_4^-$ adheres onto H-terminated Si surface (Si-H group).

Figure 5 also indicates that more Al adheres to bare Si surface in solution with pH of 10.5 than in pure water. This is considered because H-termination of Si surface is partially replaced with OH-termination. Although Fe and Zn adhesion to oxide surface is very marginal in pure water, their adhesion sharply increases in alkali solution. When pH of solution is close to neutrality, Fe and Zn mostly form neutral hydroxides such as $Fe(OH)_3$ and $Zn(OH)_3$. As pH rises to 10.5, a part of or most of neutral hydroxides change to ionic hydroxides such as $Fe(OH)_4^-$, $Zn(OH)_3^-$ and $Zn(OH)_4^{2-}$. The fact that more metals adhere to Si surfaces at pH 10.5 implies that ionic hydroxides are more likely to have dehydration reaction with OH-terminated surfaces.

Table II picks up two important metal adsorptions in wet processes and summarizes their mechanisms and conditions to trigger adsorptions.

Table II. Mechanisms of the critical types of metallic contamination from solutions.

Adsorption Mechanisms	Metals	Solutions	Surfaces
Electrochemical Adsorption → Oxidation-Reduction Reaction	Cu, Ag, Au... (Noble Metals)	DHF, Water Alkali Polishing Slurry (without Oxidizer)	Bare Si ≫ SiO_2 (including p-Si, a-Si) *Generally: Base Metals
Hydroxide Adsorption → Dehydration Reaction	Al, Fe, Zn... (Metal Hydroxides)	Alkali, Water	SiO_2 > Bare Si *Generally: OH-terminated Surfaces

MEASURES TO PREVENT METALLIC CONTAMINATION IN ALKALI SOLUTIONS

Significance of Prevention of Metallic Contamination from APM Solution

APM cleaning step is widely adopted in semiconductor manufacturing process as it features outstanding removal efficiency for particles and organic impurities. One of the drawbacks of APM cleaning step is that trace metallic impurities, if contaminated in APM solution, adhere to Si surface in large amount. Metal adhesion to Si wafer in APM solution is one of the most serious metallic contamination in the semiconductor manufacturing processes. It is reported that when APM cleaning step comes last in the wet process, charge-to-breakdown (Qbd) of gate oxide is deteriorated due to metallic contamination (7). Recent reports reveal some other problems relating to metallic contamination due to APM solution. i) Fe contamination of Si wafer in APM solution triggers increase of local surface microroughness (8). ii) When inside of deep-submicron holes with diameter of 0.2 μ m or less is contaminated with metallic impurities in APM solution, these impurities are hard to be removed even in the subsequent acid (SPM) cleaning (9). The conventional measure against metallic contamination caused by APM solution is "to treat contaminated wafer with acid cleaning to remove metallic impurities". The facts mentioned above indicate that "the post- cleaning step is unable to perfectly remove induced contaminants". What is more important is "not to allow metallic impurities to adhere to Si surface to begin with".

Technology to Prevent Metal Adhesion

As discussed above, metallic impurities adhere to Si surfaces in a form of metal hydroxides in alkali solutions. In order to prevent metal adhesion in alkali solutions, therefore, it is important to prevent metal from binding with OH. Presence of a chelating agent is effective to prevent metal hydroxide generation. Authors developed a chelate-added alkali cleaning solution (Mitsubishi Chemical. MC-1) to use instead of conventional NH_4OH solution (4, 10). Figure 8 indicates the effectiveness of the chelate-added solution (MC-1) in preventing metal adhesion from APM solution with metals of 1ppb added. When MC-1 is used to replace NH_4OH in APM, adhesion of Al, which is very easy to adhere to Si wafer, can be reduced by more than two orders. Adhesion of the other metals is reduced below detection limit.

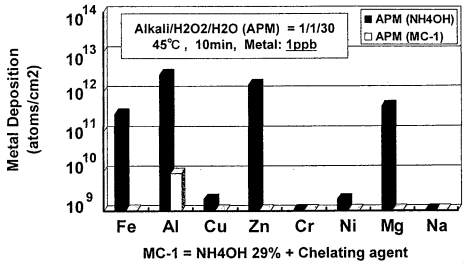


Figure 8. Effectiveness of chelate-added alkali cleaning solution (MC-1) in preventing metal adhesion from APM with metals of 1ppb added. Comparison of the conventional $NH_4OH/H_2O_2/H_2O$ and MC-$1/H_2O_2/H_2O$.

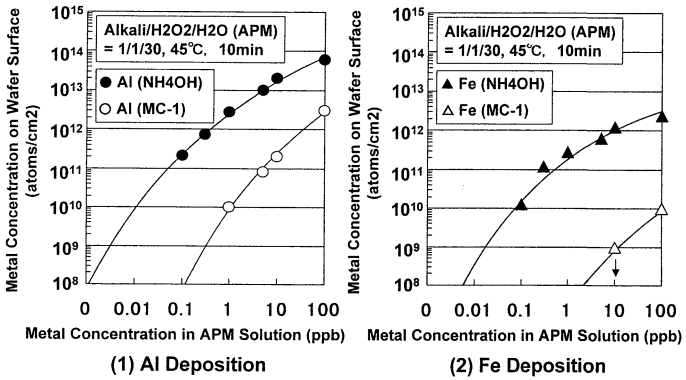


Figure 9. Dependence of metal concentration in APM solution on metal adhesion. Comparison of the conventional $NH_4OH/H_2O_2/H_2O$ and MC-$1/H_2O_2/H_2O$.

Figure 9 compares the conventional $NH_4OH/H_2O_2/H_2O$ and MC-$1/H_2O_2/H_2O$ in terms of metal concentration in solutions and that of on the Si surfaces. Concentration of metallic impurities in APM solution as received is less than 0.01 ppb (10 ppt) when APM is prepared with semiconductor grade high-purity chemicals and ultrapure water. In reality, however, APM is contaminated as it is used in the wet process, and concentration of metallic impurities often rises to 0.1 ppb. At this contamination level, metal concentration on Si surface is about 2×10^{11} atoms/cm^2 for Al and 2×10^{10} atoms/cm^2 for Fe, as shown in Figure 9. According to the SIA technology road map published at the end of 1997, required cleanliness level of wafer in process is less than 2×10^{10} atoms/cm^2 for Al and less than 4×10^{9} atoms/cm^2 for Fe in the case of 0.18 μ m devices (11). This means APM cleaning step can not be used as the final step. APM must be followed by some acid cleaning step such as HPM, which can remove metals. On the other hand, chelate-added APM is able to suppress Al and Fe contamination on Si surface below 10^8 atoms/cm^2 even if metals in solution is 0.1 ppb as shown in Figure 9. This wafer cleanliness level can satisfy SIA requirement for 0.05 μ m device shown in the SIA road map. By using chelating agent, it would be perfectly possible to use APM cleaning step as the final step of the wet process.

Removal of Metallic Contamination by means of Chelate-Added Cleaning Solution

With chelating agent added, APM cleaning is capable of removing metallic contamination. Figure 10 compares various cleaning solutions in terms of Cu removal efficiency.

As shown in Figure 10, MC-1/H_2O_2/H_2O to which chelating agent added is more effective in removing Cu than the conventional acid cleaning solutions and APM solution. Bare Si wafer used in this experiment was first treated with DHF, and then immersed into ultrapure water containing Cu in order to be contaminated with Cu. With this method, Cu adheres to Si wafer in a form of fine metallic particle (1), which is very hard to be removed. In DHF cleaning, for example, Cu which is noble metal re-adheres to bare Si surface electrochemically in DHF solution, and is hard to be removed. HPM cleaning step can not sufficiently remove Cu because a part of Cu is included into chemical oxide film and HPM solution, which does not have etching capability, can not remove chemical oxide (3). APM cleaning step is not effective in general in removing metallic impurities. It can remove Cu, however, because NH_4OH in APM solution forms complex with Cu. Chelating agent is able to form complex with Cu by far more efficiently than NH_4OH. This is why chelate-added APM features higher Cu removal efficiency than the conventional APM.

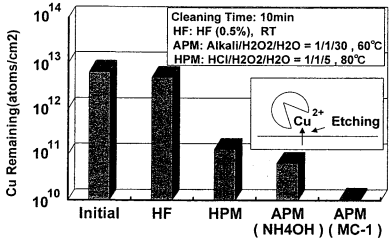


Figure 10. Effect of various cleaning solutions in removing Cu deposited on the Si surfaces. Initial contamination was deposited from Cu-added pure water to bare Si surfaces.

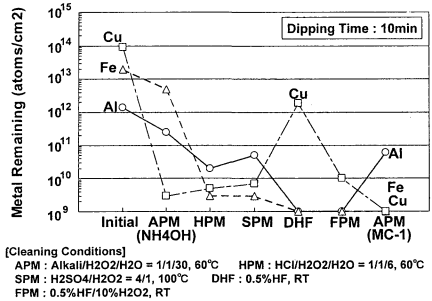


Figure 11. Effect of various cleaning solutions in removing metals deposited on the Si surfaces. Initial contamination was deposited from APM with metals.

Figure 11 compares various cleaning solutions in terms of Fe, Al and Cu removal efficiency. For Cu removal, chelate-added APM is found most effective. For Fe removal, chelate-added APM and HF cleaning solutions such as DHF and FPM (DHF/H_2O_2/H_2O) are found most effective. HF cleaning solutions are most effective in removing Al. In this experiment, bare Si wafer was contaminated by being dipped into APM solution containing metallic impurities. It is reported that Al adhering to Si wafer with this procedure is partially included in oxide (12). Al inclusion in oxide can be prevented when chelating agent is added to APM solution, which would be a preferred approach. If Al inclusion in oxide takes place for some reason, however, DHF cleaning is most effective as it etches oxide off.

Combination of DHF cleaning and chelate-added APM cleaning should be very effective in achieving both wafer surface cleanliness improvement and cost reduction. The cleaning step using chelate-added APM is capable of removing particles, organic contaminants and numerous metallic contaminants, but it is less effective in removing Al than DHF cleaning. On the other hand, DHF cleaning features low removal efficiency for particles and noble metals although it is effective in removing Al. If these two steps are combined each other in the wet process, it will be possible to take advantage of strength of the two steps to realize the highest surface cleanliness level.

The existing wet process is often composed of the conventional APM, DHF and HPM cleaning. By introducing chlate-added APM, HPM will be eliminated in the process, which will lead to considerable reduction of costs for cleaning tools, chemicals and ultrapure water.

If chemical oxide may remain on Si surface after the cleaning process, the wet process can be composed of two steps: "DHF cleaning → chelate-added APM cleaning". In the conventional wet process, the acid cleaning step must be used at the final stage because APM

cleaning step leaves large amount of metallic impurities on Si wafer surface. The final acid cleaning step, however, may allow particles to re-adhere to Si wafer surface. Use of the chelate-added APM cleaning as the final cleaning step will lead to reduction of both metallic and particle contamination as this cleaning step is free from adverse effects. It is also proven that no chelating agent remains on Si surface. The wet process procedure of "chelate-added APM cleaning → DHF cleaning" is suitable for manufacturing processes which require absolutely bare Si surface such as a process before fabrication of contact with metal interconnect. By replacing the conventional APM with the chelate-added APM, it is also possible to overcome the problem of metal cross-contamination (in particular Cu) from the conventional APM step to the subsequent DHF step. Elimination of the cross-contamination problem will increase lifetime of each cleaning solution.

CONCLUSIONS

Metal adhesion to Si wafer in alkali solutions is found to depend greatly on status of Si wafer surface. Speculating that "mechanism of metal adhesion in alkali solution is caused by the dehydration reaction between OH-terminated Si surface and OH group bound with metals", authors tried quantum chemical calculation of potential energy change during the reaction, and found that calculated results were in good agreement with experimental results and adhesion models. To suppress metal adhesion onto Si surfaces in alkali solutions, it is important to prevent metals from binding with OH. Use of chelate-added APM solution is found to significantly reduce metallic contamination on Si wafer. This will lead to improvement of Si surface cleanliness and cost reduction (longer lifetime of cleaning solutions and fewer acid cleaning steps).

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VAPOR PHASE DECOMPOSITION - DROPLET COLLECTION EVALUATION OF A WAFER SURFACE PREPARATION SYSTEM

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ABSTRACT

In order to meet the Semiconductor Industry process monitoring requirements, a metal contamination pre-concentration method is required. The Wafer Surface Preparation System (WSPS) is capable of performing a fully automatic Vapor Phase Decomposition-Droplet Collection procedure. The functionality and performance of this WSPS tool was extensively tested. Both the evaluation of WSPS tool specific parameters and VPD-DC process specific parameters will be discussed.

INTRODUCTION

The Semiconductor Industry does not stop to shrink device structures. This miniaturization of ULSI circuits puts stringent demands on the purity of silicon wafers [1], independent of the capability of analytical instruments. Moreover, the specifications are often beyond the sensitivities achievable with routine analytical techniques [2]. Vapor Phase Decomposition - Droplet Collection (VPD-DC) is a well established, but laborious procedure to improve the sensitivity for metal contamination monitoring on silicon wafers[3]. In a first step the surface oxide of a wafer is etched in an HF gas atmosphere. Subsequently a small liquid droplet is scanned over the entire surface to collect and pre-concentrate the surface impurities within the droplet. Wet chemical analysis by means of Inductively Coupled Plasma Mass Spectrometry (ICPMS) or Atomic Absorption Spectroscopy (AAS) can be performed on this sample. Alternatively, in a third step the droplet is dried for Total Reflection X-Ray Fluorescence Spectroscopy (TXRF). Analysis of the dried droplet residue shows for 150mm wafers a detection limit enhancement by a factor of 300 compared to direct TXRF. A major achievement for succesful implementation of the VPD-DC process came from the development of a fully automated tool, the Wafer Surface Preparation System* (WSPS) [4]. Aim of this paper is to present results on the robustness and performance of the WSPS tool for subsequent analysis.

EXPERIMENTAL

The WSPS (Wafer Surface Preparation System) performs fully automated cassette to cassette VPD-DC processing and consists of three process modules. These modules are a PAD-Fume (Programmable Automatic Decomposition Fumer), a PAD-Scan (Programmable Automatic Droplet Scanner) and a PAD-Dry (Programmable Automatic Droplet Dryer). A cassette station and a robot module for wafer transfer complete the modular design of the WSPS. The PAD-Fume provides an HF resistant reaction chamber with Peltier cooled wafer stage. Dry nitrogen is driven through an HF bubbler bottle

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under controlled gas flow. The HF vapor condenses on the cooled wafer, dissolving the native or thermal surface oxide. After the etching process, the chamber is purged by nitrogen to remove the HF vapor. The PAD-Scan consists of two rotating wafer stages for scanning and droplet deposition, one automated microvial for AAS or ICP-MS analysis, two rotating and lifting arms for pipetting and scanning liquid droplets and one automated diluter. Once the freshly etched wafer is placed on the scanning stage, aligned and flat/notch oriented the scanning procedure is started. The pipette is sucking a predefined volume out of the beaker with the VPD solution and dispenses it onto the wafer. Now the scan tube takes the drop and guides it over the wafer surface in a spiral trace. After completion of the scan, the tube is detached from the droplet with a short nitrogen pulse. The pipette is sucking up the droplet again to determine the residue volume and to deposit it at the predefined position on the scanned wafer, a deposition wafer or into a vial. Both pipette and tube can be chemically cleaned and rinsed with DI-water before and after each scan. The PAD-Dry performs the last (optional) step in the WSPS process, prior to subsequent TXRF analysis. The droplets are dried by evacuating the chamber and heating the wafer stage. The cassette station provides one load position for 100 to 200mm wafer cassettes and one for 300mm wafer cassettes. The robot can handle all wafer sizes without any hardware change. This structure allows to operate all modules in parallel which leads to a high throughput of the complete system.

For the tool evaluation, both pregate cleaned wafers, either with native or thermal oxide (up to 400nm) and wafers with controlled metal contamination (10^{10} - 10^{12} at/cm^2 range) were used. The controlled metal contamination was achieved from spin contamination from acid solutions, or from immersion in metal contaminated SC1 solution (1/4/20 $NH_4OH/H_2O_2/H_2O$) at room temperature. The collection mixture was either dilute acid based (2/100 HNO_3/H_2O) or hydrogenperoxide based (1/3/96 $HF/H_2O_2/H_2O$). For analysis purposes, both AAS (Perkin Elmer 4110ZL) and TXRF (Atomika 8010, with Mo tube excitation) were used.

RESULTS AND DISCUSSION

Evaluation of the PAD-Fume

The PAD-Fume module is designed to be compatible to HF exposure. During a VPD-DC process, the wafer surface oxide (chemical or thermal) is dissolved by exposure to hydrofluoric acid, and according to the reaction (or an equivalent) given below.

$$SiO_2 + 6HF \rightarrow H_2SiF_6\,(g) + 2\,H_2O \qquad (1)$$

As such, all (metal) contamination embedded in, or on top of the original oxide layer remains in the moist water film formed on the wafer surface. Another advantage of this HF etch process is that the surface becomes hydrophobic in nature. In Figure 1, the remaining oxide thickness (starting from 400nm thermal oxide) is plotted as a function of time; for different HF concentration and wafer size. It can be seen that the process is relatively independent from the wafer size. The HF concentration however, influences the etch process dramatically, a factor of two reduction causes a fourfold increase in the time needed for complete removal of the 400nm thermal oxide. The etch rate can be derived from Figure 2, where the etch time is plotted for various thermal oxide thicknesses; the three minutes offset is due to the arbitrary time taken for removal of a chemical oxide

layer. An overall etch uniformity better than 10% is achieved for all thicknesses, whereas the slope allows to estimate an average etch rate of more than 40nm/min. This etch rate is valid for an HF concentration of 49%. Also, the correlation between HF concentration and Pad-Fume operation time was determined (not shown). This results in the following relation, where [HF] is the remaining concentration (%) and T the process time (hours) [HF] = -0.0953 * T + 48.90. As such, almost 2000 chemical oxide wafers can be processed before [HF] < 40%, arbitrarily choosen as treshold value before a significant decrease in throughput (longer etch times) is observed.

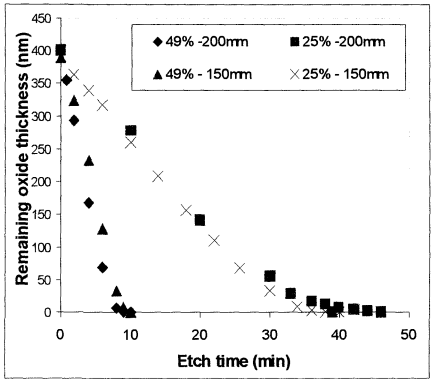

Figure 1 Remaining oxide thickness (nm) vs. etch time a.f.o. [HF] and wafer size (400nm initial)

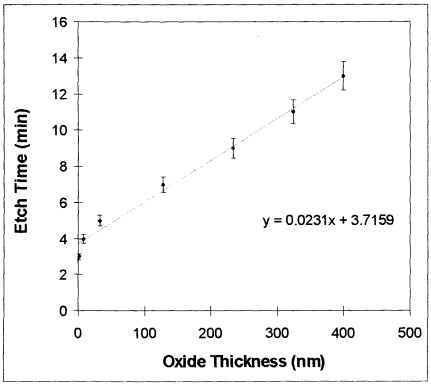

Figure 2 Etchtime vs. Oxide Thickness (nm) for 150mm wafer and 49% HF

Evaluation of the PAD-Scan

The PAD-Scan module is the heart of the WSPS tool. After the wafer oxide surface is etched hydrophobic in the PAD-Fume, the metal contamination should be preconcentrated in a microliter quantity of a scan solution. This chemical collection procedure is done on the PAD-Scan. Among the scan variables are the droplet volume (between 50 and 150µl), the scan speed (between 10 and 80 mm/s) and the track distance

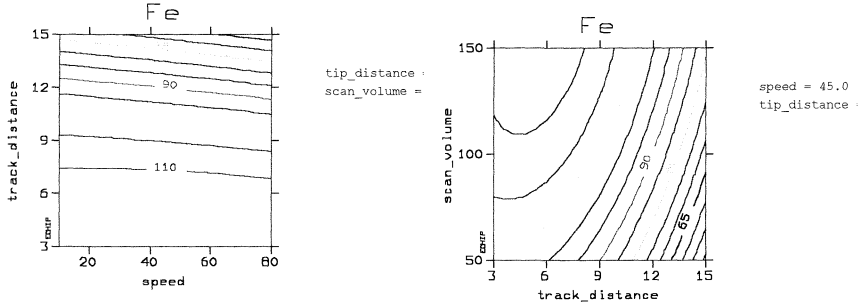

Figure 2 Impact of the PAD-Scan parameters (rotational speed, droplet volume and track distance) on the Fe collection from SC-1 contaminated wafers

(distance between consecutive spirals, between 3 and 15mm). Of course, also the chemistry of the scan mixture is a crucial factor under consideration. The interdependency of the various parameters was evaluated by means of a Design of Experiment (DOE). The response being the amount of collected Ca, Fe and Zn from an identical set of SC1 contaminated wafers processed with a variable setting of speed, track distance and scan volume. The obtained contourplots for Fe are presented in Figure 2, the results for the other metals are comparable. The effect of chemistry will be discussed later. It can be seen from the horizontal response line that the rotational speed does not influence the collected amount of Fe, whereas both droplet volume and track distance do have an influence. Optimized collection is achieved at small track distances, allowing for good overlap between the subsequent spirals (and complete scan of the wafers). Therefore also, a large droplet volume is beneficial. The effect of droplet volume has nothing to do with solubility limitations and thus saturation of the droplet volume. If a smaller variation range is selected for track distance, also the effect of droplet volume is strongly reduced, having virtually no impact on the collected amount of metal. The relative independency of the collection of factors other than the scanned area (i.e. track distance) seems to indicate that the Fe collection is fully quantitative for the collection chemistry under consideration (1/3/96 $HF/H_2O_2/H_2O$).

To demonstrate the impact of the collection chemistry a round robin was organized. Wafers were contaminated with Fe at controlled concentration level (88 $\pm$ 14 * 10^{10} at/cm^2). A standard VPD procedure and dry procedure was applied by all participating partners whereby variations in collection chemistry were considered. Neither of the procedures studied (various $HF/H_2O_2/H_2O$ mixtures, DI water or HF/H_2O) seemed to outperform any of the other procedures as seen in Figure 3. This allows the important conclusion that the VPD-DC collection of Fe is not affected by the scan chemistry. Additionally, comparison of the VPD-DC-TXRF with the D-TXRF measurement (i.e. before collection) indicates that in all cases the collection efficiency is close to 100%.

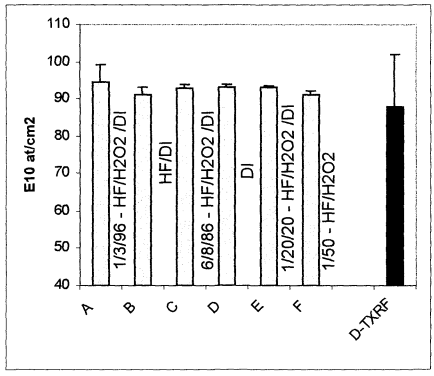

Figure 3 Measured Fe concentration a.f.o. collection chemistry

As seen above, the behavior of elements that are less noble than silicon is relatively straightforward. Neither the collection chemistry nor the scan parameters (other than scanned area) seem to affect the collection efficiency. In most cases a fully quantitative collection (i.e. 80 - 100%) is feasible. Problems however can be expected upon collection of elements that are more noble than silicon (e.g. copper), as they might be subjected to chemical outplating from the HF-based scan solutions onto the bare silicon surface. If this occurs, the collection mixture should contain a sufficiently high oxidans (see further) in order to reverse the electrochemical reaction. If we assume the following equation (2) as rate determining.

$$Cu(s) + \text{oxidans} \;\text{<====>}\; \text{reductans} + Cu^{2+}\,(aq) \qquad (2)$$

It can be understood that reaction kinetics are limiting the collection efficiency. Collection is dependent on the copper and oxidans concentration, but also the scan parameters are seen to affect the collection process, as can be seen in Figure 4.

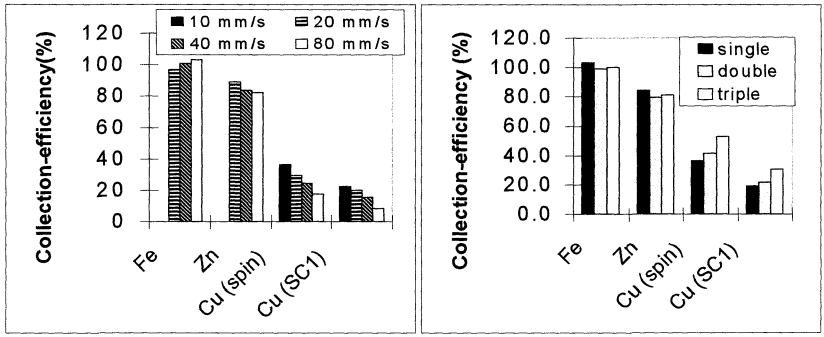

Figure 4 Collection efficiency for Fe, Zn and Cu as a function of scan speed and number of wafer surface scans

The collection efficiency for Fe and Zn, being almost fully quantitative, is barely affected by the scan speed and number of wafer scans, as also shown from the DOE evaluation. For Cu however, either originating from acid spin contamination (i.e. as nitrates) or from SC-1 contamination (i.e. as hydroxides), a clear dependency with scan speed and number of wafer scans can be seen. A likely explanation is that at slower scan speed, a longer droplet - wafer contact time occurs, thus allowing a better establishment of the equilibrium presented in equation (2). A similar event occurs when the wafer surface is scanned more than once, resulting in a better collection for noble elements. It should be noted however that the reaction equilibrium is also dependent on the concentration of oxidans as will be discussed further.

Evaluation of the PAD-Dry

The droplet drying process done in the PAD-Dry module is optional since it is only required for subsequent TXRF analysis. As such, the main requirement is that the droplet drying occurs in a fast and reliable manner, whereby the shape of the droplet residue does not influence the subsequent TXRF analysis. To demonstrate the robustness of the droplet drying procedure, wafers were contaminated with Fe at controlled levels (88 $\pm$ 14 * 10^{10} at/cm^2). A standard VPD procedure and DC-chemistry was applied by all participating partners whereby variations in drying procedure were considered. Neither of the procedures studied (ambient air, IR drying, hot plate

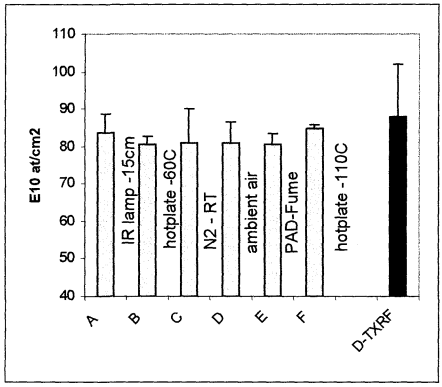

Figure 5 Measured Fe concentration a.f.o. droplet drying procedure

at 60 and 110C, N_2 purging, PAD-Dry) seemed to outperform any of the other procedures as seen in Figure 5. It can therefore also be concluded that the VPD-DC collection of Fe is not affected by the droplet drying method as was the case for the collection chemistry. Additionally, also for all drying procedures, the collection efficiency is close to 100%. Also, since these samples were processed in different labs, the results also give an indication of both the reproducibility and the repeatability of the VPD-DC procedure. The main benefit of the PAD-Dry however, is the reproducibility of the automatic system and the short cycle time; i.e. < 5 minutes for a 50µl droplet compared to almost an hour for ambient air. The reproducibility is extremely important with respect to the dried droplet residue shape, as this will influence the TXRF response.

Evaluation of the VPD-DC Procedure

A comparison of the surface concentrations of metal contaminants as measured without any pre-concentration method, with the surface concentrations resulting from GeMeTec's Wafer Surface Preparation System (WSPS) and a manual method (manual wafer handling, HF fuming, PAD-Scan and infrared drying) is presented in Figure 6 for Ba and Cu. In general, also wafers with surface concentrations ($1E^9$ till $5E^{12}$ at/cm^2) of metals, Ca, Cr, Fe, Ni, K, Sr, and Zn were prepared (with varying implantation and anneal).

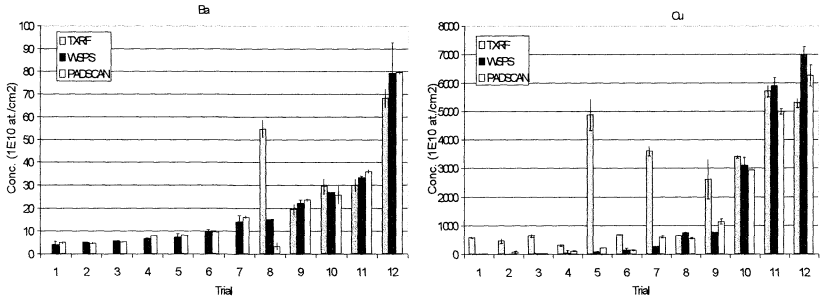

Figure 6 Comparison of D-TXRF and VPD-DC-TXRF for Ba and Cu contamination

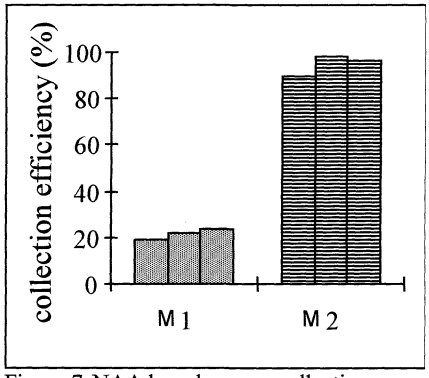

Figure 7 NAA based copper collection efficiency for H_2O_2 mixtures

For Ba (and all other elements, except Cu), the collected and uncollected metal concentrations generally agree. It should be noted that for trial 1 – 7 Ba could only be detected when a VPD-DC procedure was applied indicating the increased sensitivity obtained from such a preconcentration method. Also, trial 8 behaves different, most likely due to the high dose BF_2 implantation ($5x10^{15}$ cm^2) given to the wafers, prior to contamination (under investigation, but likely a fast reoxidation process). For copper however, a general poor collection efficiency (order of 20%) is observed, which is caused by the

collection mixture used (1/3/96 $HF/H_2O_2/H_2O$). This poor collection efficiency has been reported before [3], as well as the strong dependency of copper collection with scan parameters. In earlier work [5], the copper collection efficiency was studied as an equilibrium between outplating and collection of copper. A good collection mixture should demonstrate low metal outplating. Also, the driving force for metal to transfer from the wafer surface into the droplet should be high and quantitative (see reaction(2)). Besides of variation of the scan parameters, both requirements can be met if a mixture with a sufficiently high concentration of oxidans is used, as can be seen in Figure 7. Results are shown from NAA measurements for two different peroxide mixtures (M1 = 1/3/96 $HF/H_2O_2/H_2O$ and M2 = 1/5 HF/H_2O_2) to scan copper contaminated wafers (i.e. $5x10^9$ at/cm^2 Cu). If sufficiently high oxidating power is present in the mixture(M2), equilibrium is achieved in the short droplet wafer contact time, independent of the nature of the copper contamination and full quantitative copper collection is possible.

Evaluation of the WSPS Tool Performance

The WSPS has been tested and evaluated over a 15 month period. Besides of some intermittent hardware problems which were beta tool related excellent Mean Time Between Failure (MTBF) results were obtained. As such, the MTBF increased from about 200hrs at the start of the evaluation period, to well above 1000hrs in the further frame of the evaluation project, with an uptime between 90 and 95% in the final stages of the evaluation project.

Upon processing of a contamination monitoring wafer, care should be taken that neither the operating system adds significant blank levels, nor that cross contamination between wafers can occur. It should be noted that in order to achieve blank levels better than $1E^8$ at/cm^2, the overall analytical procedure, including the clean room ambient, the initial wafer cleanliness and the purity of the chemicals determines the result. Specifications for process chemicals of 0.1 ng/l already results in an upper limit contribution from the scan volume in the order of $1E^8$ at/cm^2. During pre-acceptance testing, for most elements these blank values were obtained from scanning pre-gate cleaned wafers. As such, it is fair to state that the WSPS does not introduce any measurable contribution to the blank values. Therefore, the practical lower limit of detection for the VPD-DC procedure is defined by the purity of the scan solution chemicals available and the clean room ambient, rather than by the WSPS system itself.

Another valuable and tool related parameter is the Cost-of-Ownership (CoO). It was found that the main contributors to the CoO are the WSPS tool depreciation, the clean room and the operator cost, while the chemicals and DI usage is negligible. An estimated total cost of almost 3 euro / wafer might seem a reasonable high value for a sample preparation step prior to a metrology process. However, one should keep in mind that an equal throughput (6 wafers/hour), relying only on manual operation, would cost a multitude of this price in terms of manpower. Also, it should be emphasized that the WSPS allows to reduce the consumption of monitor wafers since the VPD-DC process is in fact a micro cleaning process (efficient collection of potential metal contamination). Therefore, re-use of the wafers is possible, especially since the droplet can be transferred to a deposition wafer. Thus no wafer damage is caused or residues are remaining after the drying step. If then, we assume a purchase cost of 600 euro per 300mm wafer and about 100 euro per 200mm wafer, it can be seen that a reduction in consumption of less than

100 (300mm), or less than 600 (200mm) wafers matches the yearly capital depreciation of the tool. The other major contributors to the cost-of-ownership are the operator and clean room cost, mainly required to mix the chemicals for the VPD-DC collection procedure (hood, worktable, drain, exhaust, ...). It can be anticipated that the availability of small quantities pre-mixed bottles of collection solutions (e.g. 500ml bottles), with a sufficiently long shelf lifetime (e.g. 3 months) would therefore improve the cost-of-ownership and definitely the ease of tool operation in a fab-like environment, where often the required chemical handling facilities are lacking.

CONCLUSIONS

Metrology is frequently viewed as a non-value-added monitoring step that has no effect on device performance. However, today's continuing reductions in feature size and increasing demands on device specifications are squeezing the process window and pushing the limits of analytical tool capabilities. Although demonstrated earlier, Vapor Phase Decomposition – Droplet Collection is a very robust and reliable metal contamination preconcentration method. In the past however, it has been often objected because of the tedious and labor intensive sample preparation procedure, and related problems such as uncontrolled or poor collection efficiency (e.g. copper). With the introduction of automated equipment, a breakthrough of the VPD-DC method is anticipated. The method offers an improvement in the sensitivity of routinely used metal contamination monitoring techniques by almost two orders of magnitude. Beyond process improvement gains, the next most obvious benefit of integrated and automated metrology is a reduction of process defects caused by human material handling. This highlights another benefit of the WSPS; a process step that requires an operator to transfer and handle wafers, thus putting them at risk, could be eliminated.

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6. Semiconductor Equipment Assessment - SUPRA (SEA@RL.AC.UK)

APPLYING A HMDS LAYER AS AN ORGANIC RESIDUE CLEANING EFFICIENCY MONITOR

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ABSTRACT

The organic residue removal efficiency of four resist stripping procedures was evaluated by using hexamethyldisilazane (HMDS) primer as an efficiency monitor. Bare silicon wafers together with thermally oxidised wafers and low temperature oxide covered wafers were primed and subsequently put through the different cleaning steps. Analysis of the primed and cleaned samples with contact angle measurements, Secondary Ion Mass Spectrometry (SIMS), Purge and Trap Gas Chromatograph Mass Spectrometry (P&T-GC/MS) and Low Energy Ion Scattering spectroscopy (LEIS) revealed organic contamination on all samples. Furthermore, an organic solvent based remover bath was found to leave significant amounts of HMDS residues on the surface but when combined with an SC1 cleaning step the residues were significantly reduced. A difference in bonding of HMDS to non-densified LTO in comparison to silicon wafers or wafers with thermal oxide was observed. Unreacted HMDS was found on silicon and thermal oxide wafer surfaces after priming.

INTRODUCTION

As semiconductor device dimensions grow smaller the role of organic contamination and especially its removal gain in importance [1]. Therefore, four typical cleaning sequences used in IC manufacturing were chosen for investigation into their cleaning efficiency. Hexamethyldisilazane (HMDS), which is typically used for surface priming in litography, was selected as a model agent for organic contamination hard to remove. Due to its high reactivity towards SiO_2 surfaces HMDS is well suited for monitoring effectiveness of the different wafer cleaning procedures. Bare silicon wafers, thermal oxide wafers and non-densified low temperature oxide (LTO) covered wafers were used as test samples.

To evaluate the cleaning processes several measurement techniques were employed. Contact angle measurements were conducted to determine the hydrophobic/hydrophilic nature of the surfaces studied, revealing presence of primer or cleaning bath residues. Surface modification was also studied with chemical analysis techniques: volatile

trimethylsilanol was detected with Purge and Trap Gas Chromatography Mass Spectrometry (P&T-GC/MS) and the bonded trimethylsiloxy (TMS) groups were detected with Secondary Ion Mass Spectrometry (SIMS) in static mode. Low-Energy Ion Scattering (LEIS) data was collected to gain insight into the elemental composition of the outermost atom layer of the treated surfaces.

EXPERIMENTAL

Test samples

As test samples, silicon wafers as well as wafers with a 200 nm thick non-densified low temperature oxide (LTO) layer and wafers with a 100 nm thick thermal oxide layer were used. Priming was done in a YES vapor priming oven the process consisting of a dehydration step followed by 5 minutes vapor prime at 10 Torr at 150° C. The cleaning baths studied were a H_2SO_4 + $(NH_4)_2S_2O_8$ bath at 90°C (Piranha), a solvent/amine type remover bath at 90°C, and the remover bath combined with a H_2O+NH_3+H_2O_2 (SC1) bath at 65°C. Manual wet benches were used for the baths and all handling was performed in a class 10 clean room facility. After the chemical baths wafers were rinsed in a quick dump with deionized water and dried in a centrifugal rinse and dryer. In addition to the chemical baths also an ozone asher treatment was included in the study scheme.

Static and dynamic contact angle measurement

Two different contact angle measurement techniques were used – static and dynamic [2]. DI water was used as a model liquid in both. In static contact angle measurement a drop of water is placed by a micropipette on the examined substrate. The drop is reflected onto a monitor and the contact angle of the drop is measured. The measuring system is based on video technology with image analysis developed in-house. In dynamic contact angle measurement (Wilhelmy plate technique) the sample is moved back and forth through the liquid and the meniscus force is measured by an electrobalance using a SIGMA70 method. The sample was prepared by attaching two wafer pieces together to produce a sample with similar front and back sides.

Low Energy Ion Scattering (LEIS)

The composition of the outermost atom layer of the primed, remover stripped and remover/SC1 stripped silicon and LTO wafers were analysed by LEIS. Description of the LEIS technique and instrumentation used can be found in references [3-6]. Here, measurements were carried out using 3 keV $^3He^+$ ions. For each spectrum an ion dose of $0.1x10^{15}$ He-ions/cm^2 was used while the measured area was 2x2 mm^2. This removes roughly 0.01 atomic layers from the surface if the sputter yield is assumed to be about 0.1 (number of sputtered target atoms per incident ion). The peak areas were calculated by subtracting the background and fitting a Gaussian peak with the data.

SIMS in static mode and P&T-GC/MS

SIMS data was acquired with a VG IX70S double focusing magnetic sector instrument operated in static mode, using a Ga^+ primary ion beam of 8 keV energy [7]. Positive secondary ion mass spectra at low resolution were recorded to detect the presence of TMS on the wafer surface, and to check for other impurities possibly introduced in the cleaning stage. Relative TMS coverage was obtained by measuring the signal ratio of peaks at *m/z* 73 ($SiC_3H_9^+$) and 28 ($^{28}Si^+$) at a higher resolution of approximately 1000 ($m/\Delta m$ at *m/z* 28) to separate the TMS peak from the interfering Si_2OH^+. The normalised TMS signal was assumed to be linearly related to the surface coverage as described in literature [8].

A detailed description of the P&T-GC/MS system used is given elsewhere [9]. In short, the test wafers were heated to 100°C in He carrier gas, the emanating volatile compounds trapped at liquid nitrogen temperature and then desorbed into the analytical column of a GC/MS. Trimethylsilanol, the volatile reaction product of HMDS with adsorbed water, was detected by its main mass peak at *m/z* 75.

RESULTS

Contact angle measurements

The static and dynamic contact angle measurement results are given in Tables I and II. Static contact angle measurements show the modification of the silicon and thermal oxide surface from a high-energy hydrophilic non-treated surface to a primed low energy hydrophobic surface. Different cleaning steps change the silicon and silicon oxide surfaces again, making them more hydrophilic [8,10]. By a static contact angle measurement this is not observed for an LTO wafer, where the droplet has too flat a profile for accurate measurement. However, the dynamic contact angle measurement detects the difference also between the non-treated and primed LTO wafer surfaces. Combining the results of static and dynamic measurements, it can be seen that the remover bath seems to clean the surface less efficiently than the other treatments, either being unable to remove TMS or leaving other organic residues on the surface.

Table I. Static contact angles.

	silicon	thermal oxide	low temperature oxide
non-treated	30	46	12
primed	72	84	16
+ remover	39	49	14
+ remover + SC1	16	29	19
+ Piranha	15	44	18
+ ozone ashing	17	37	13

Table II. Dynamic contact angles.

	thermal oxide	low temperature oxide
non-treated	0	14
primed	63	68
+ remover	40	43
+ Piranha	18	21

LEIS spectra

The LEIS spectra of the silicon and LTO samples are shown in Figures 1a and 1b, where the spectra of the three samples treated differently are overlaid. In all spectra peaks of C, O and Si are identified. The presence of a Si peak can be assigned both to the exposed oxide surface of the wafer and HMDS, which also contains Si, whereas C would originate from HMDS or other organic contamination, and O from the exposed SiO_2 and from the modified HMDS layer. As the sensitivity of the LEIS measurement varies from one element to another a straightforward determination of absolute amounts of elements on the surface without reference samples is not possible. It is, however, possible to compare the LEIS signals of a certain element in different samples.

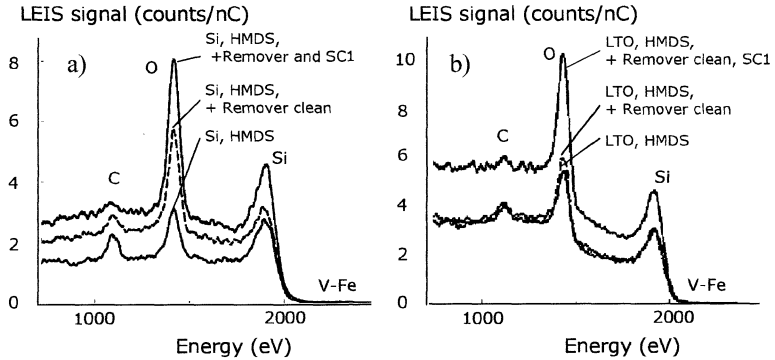

Figure 1. LEIS spectra of a) a primed silicon wafer and wafers after stripping baths b) a primed LTO wafer and wafers after stripping baths. Smaller amount of heavier elements, possible V, Fe or another element with similar mass was also detected.

In the case of LTO wafers, the remover bath has very little effect on the LEIS peaks. It does, however, significantly change the primed silicon wafer surface. The C amount on the silicon wafer surface decreases by 35 % and the O amount increases by 85 % while the observed change in the Si peak is negligible. These changes suggest that the remover bath has not changed the HMDS coverage of the silicon wafer, but has modified HMDS layer. The subsequent SC1 clean has quite a similar effect on both the silicon wafer and the LTO wafer. It decreases the HMDS coverage of the primed silicon and LTO wafers, which is seen as a 50 % and 55 % increase in Si amounts, respectively. The SC1 clean increases

also the oxygen amount on the silicon and LTO wafer surfaces by 70 % and 105 %, respectively. Further, SC1 clean reduces the carbon amount by 35 % and 40 %, respectively. These changes can be attributed mainly to the increased exposure of the clean wafer surface, and also to modification of the HMDS layer.

Presentation of the carbon peak area as a function of the oxygen peak area in Figure 2, shows how carbon is substituted by oxygen in the cleaning process. For a zero oxygen signal the carbon peak area would be 65, which would represent a 100% HMDS coverage of the wafer surface. In agreement with the finding of O in the top layer of primed samples, this indicates that the wafer is not fully covered by the primer. It also demonstrates that even after SC1 bath about 37 % of the wafer surface is still covered by carbonaceous compounds. It might be, however, that part of the contamination detected was deposited during transportation.

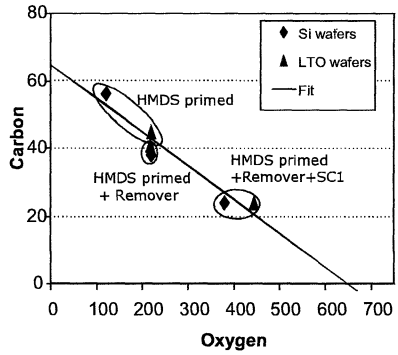

Figure 2. Correlation of carbon and oxygen LEIS peak areas after different treatments.

Static SIMS and P&T-GC/MS

The analysis of SIMS spectra also showed presence of organic contamination on all treated samples often more abundant than was detected in the spectra of the non-treated wafers. However, monitoring the characteristic peaks of TMS revealed differencies in the cleaning efficiency of the treatments applied. After the organic remover treatment the peaks assigned to TMS at *m/z* 73 and 43 were still high when compared to those on the primed surface and considerably higher than in other samples. A similar result was obtained for all different wafer types. The normalised TMS signals, presented in Figure 3 for silicon wafers, give a good indication of the cleaning efficiency with respect to TMS residues and are in good agreement with the contact angle and LEIS measurements. A high variation in the coverage measurement results implies that HMDS is spread unevenly over the wafer surface and in the case of primed wafers, surplus HMDS is 'floating' on top of the bonded layer.

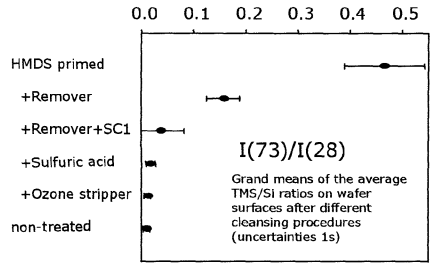

Figure 3. Static SIMS: normalized TMS intensities, related to HMDS coverage, for Si samples treated in various ways.

P&T-GC/MS, detecting the volatile trimethylsilanol, or unreacted HMDS, on the surface, gave different results for different wafer types. This is exemplified in Figure 4, where the ion chromatograms of the primed wafers are shown. When heated, trimethylsilanol and/or HMDS is released from the primed silicon wafer and thermally oxidised wafer but no volatile trimethylsilanol peak was detected in the case of LTO wafers. However, performing a further hydrolysis of the primed LTO surface with H_2SO_4 in dichloromethane and analysing the extracts with a GC/MS, proved that the surface was covered with HMDS. The observed phenomenon thus reflects a difference in bonding of HMDS to non-densified LTO in comparison to silicon wafers or wafers with thermal oxide - a difference implied also by the analysis of the LEIS spectra. This is due to the different structure of the SiO_2 surface depending on oxide growth method.

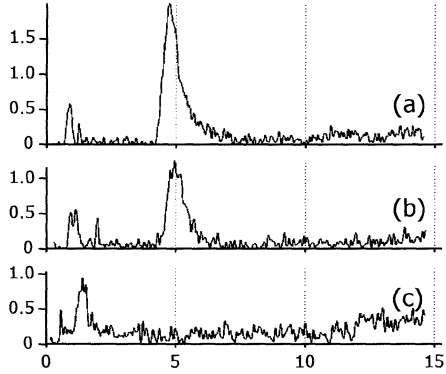

Figure 4. Ion chromatogram of *m/z* 75 as a function of time. *m/z* 75 is a characteristic peak for HMDS. a) HMDS primed silicon wafer b) HMDS primed thermal oxide wafers and c) HMDS primed LTO wafer.

On the other hand, P&T-GC/MS results for silicon wafers exhibit the same trend in cleaning efficiency as observed with contact angle measurements, LEIS and SIMS: the remover bath alone does not remove HMDS from primed wafer surfaces. This is seen clearly in the data of Table III.

Table III. Ratio of mass peak 75 in treated silicon samples to that of HMDS primed silicon wafers.

Non-treated	primed	primed + remover	primed + remover + SC1	primed + Piranha	primed + ozone ashing
0	1	0.5	0.1	0.1	0.3

CONCLUSIONS

All characterization techniques used showed organic contamination on all test wafers after different cleaning procedures. The organic solvent based remover bath was also found to leave significant amounts of TMS on the surface, suggesting that the solvent bath is able to remove only unreacted HMDS from the surface. According to SIMS and P&T-GC/MS measurement results, the SC1 and Piranha baths were found to reduce the amount of HMDS to approximately 1/10 of the starting level. However LEIS, which is sensitive only to the outermost atom layer, showed that even after SC1 bath still 1/3 of the surface is covered with organic contamination. This discrepancy is due to the difference in information depth of the techniques used.

By P&T-GC/MS unreacted HMDS was found on silicon and thermal oxide wafers even though the primer coverage observed by LEIS was only 85 % for silicon wafer. Curiously, unreacted HMDS was not detected on LTO wafers by P&T -GC/MS, which is indicative of differences in HMDS bonding on different types of oxide surfaces. By LEIS the effect of the remover treatment on a primed LTO surface was found to be negligible whereas the elemental composition on the primed silicon wafer was clearly modified by the same treatment. SIMS did not detect any differences between different types of wafers, but the large variation in TMS coverage measurement results of the primed wafers is in accordance with the finding of unreacted HMDS on wafer surfaces. These results show that it is important, when monitoring cleaning efficiency using HMDS, to take into account sample type and specific characteristics of the analysis techniques chosen.

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